Optimum Quality in the Semiconductor Foundry Business

Matthew S. Jones[1]

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[1]Advisor: Dr. Houssam Abbas

Abstract

The semiconductor foundry business must provide a quality product at a reasonable price. As semiconductor manufacturing becomes more and more expensive, the cost of quality must be optimized to help control overall cost.

Chapter 1

Optimum Quality

The concept of Optimum Quality (OpQ) comes from the "U-Curve" (see Figure 1.1) created by the sum of Failure Costs and Prevention Costs on a Cost versus Quality axis. As companies invest more in prevention costs, quality increases, assuming the investment is done well. As quality increases, failure costs decrease. The sum of these two costs is the Total Cost of Quality (TCQ). Optimum Quality is the minimum TCQ.

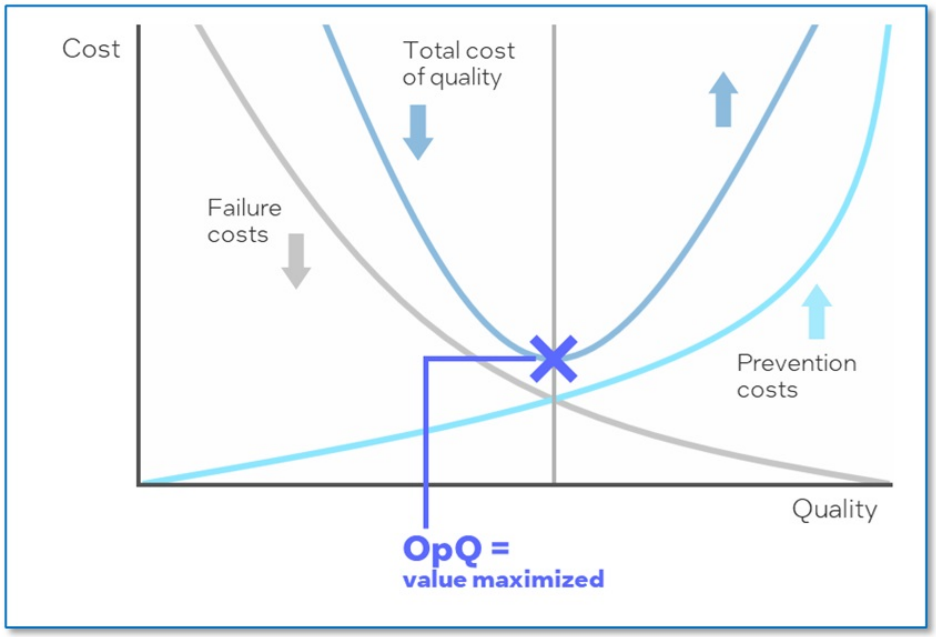

Figure 1.1: The U-Curve

Understanding how to optimize investment in prevention costs is critical since not all prevention costs are equal. That is, each cost is an investment that has a potential return. This return is initially in the form of quality, but is eventually in the form of failure cost avoidance. Of course, as the Kano Model (see Figure 1.2) suggests, over time "Normal Quality" is expected to increase, which implies that prevention costs must also increase. Further, "Exciting Quality" will be the result of additional spending, but it is not clear what any individual customer would find exciting.

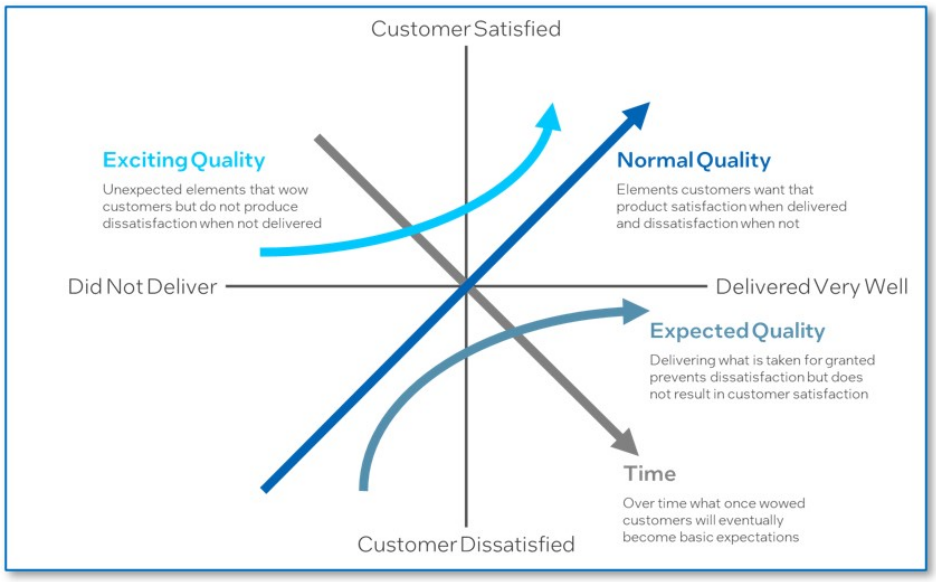

Figure 1.2: The Kano Model

Organizations must, over time, seek to achieve higher normal quality, an amount of exciting quality that customer appreciate, but at a cost that does not bankrupt the business. Artificial intelligence can help ensure this.

> "Semiconductor manufacturing on the production-level consists of lengthy complex processes that are reentrant competing for limited equipment capacity, subject to waiting time and precedence constraints and frequency-based setups. Meanwhile, as semiconductor manufacturing continuously migrates to advanced technology nodes for feature shrinkage, process challenges for yield enhancement have called for interrelated efforts involving advanced process control, advanced equipment control, and advanced quality control." [Chi+21]

The purpose of this paper is to provide an overview of the semiconductor industry, the design flow for integrated circuits, and the semiconductor manufacturing process. Throughout, opportunities for the use of Artificial Intelligence to alleviate cost and quality "pain points" will be introduced.

Chapter 2

Integrated Circuits

The Semiconductor Foundry Business cannot be properly put into context without first understanding how integrated circuits (ICs) are designed. An IC consists of multiple distinct electronic components that are *integrated* and interconnected into a single device such that the new device is considered distinct. The first IC was built by Jack Kilby of Texas Instruments in 1958 (See Figure 2.1). "His method was really a hybrid circuit, where the individual components, after being fabricated on the device surface...were interconnected manually by stitching bonding wires between them." [BW20]

The first monolithic IC, which is made from etching components onto a single piece of material, was invented by Robert Noyce of Fairchild Semiconductor and built on technology developed by Jean Hoerni. Modern ICs are based on monolithic, rather than hybrid, integrated circuits. The first operational monolithic semiconductor IC was created at Fairchild Semiconductor on September 27, 1960. Five years later, Gordon Moore observed that the number of transistors in an integrated circuit (IC) doubles about every two years ([Moo65]), and for the most part, this has held true. Today's modern CPUs (Central Processing Units, the "brains" in a computer) are made up of billions of transistors.

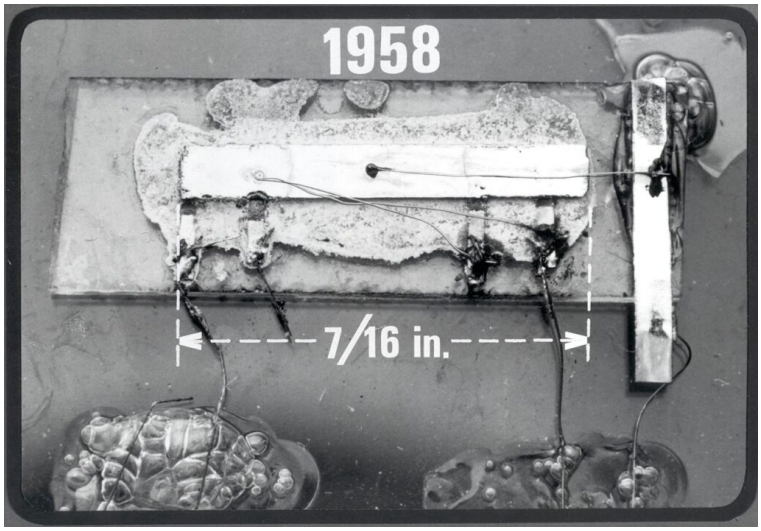

Figure 2.1: The First Integrated Circuit [Cen13]

Figure 2.2: The Author outside the late Gordon Moore's Office/Shrine in Intel's Robert Noyce Building in Santa Clara, California

Integrated circuits are not just computer CPUs, though. Integrated circuits are used in everything from cars and airplanes to communications equipment to household appliances. As more and more get "smart," the more integrated circuits they will need. Most modern ICs are made using Metal-Oxide-Semiconductor (MOS) Transistors.

2.1 MOS Transistors

Metal-Oxide-Semiconductor, or MOS, transistors are the "switches" that make up most of the integrated circuits in the world. The "semiconductor" in MOS is silicon (Si), the "oxide" is silicon-dioxide (SiO_2), and the "metal" is aluminum (Al) or tungsten (W). Transistors operate like switches because when a particular voltage is applied to the gate, current flows between the source and the drain. Figure 2.3 shows a simple N-type MOS transistor.

The source and drain are created by implanting phosphorus (P) or arsenic (Ar) ions into the silicon. This process is called "doping." Because these two elements have five valence electrons and silicon has only four, doping silicon with either of them will add extra electrons to that area. The "well" in which the source and drain sit is doped with boron (B), which has only three valence electrons, so that area will have extra "holes" (missing electrons). When the gate voltage exceeds the threshold voltage of the transistor, a channel is created connecting the source to the drain, allowing current flow. The "critical dimension" for a semiconductor manufacturing process is usually the length (distance between the source and the drain) of the channel. The smaller the channel length, the faster the switch.

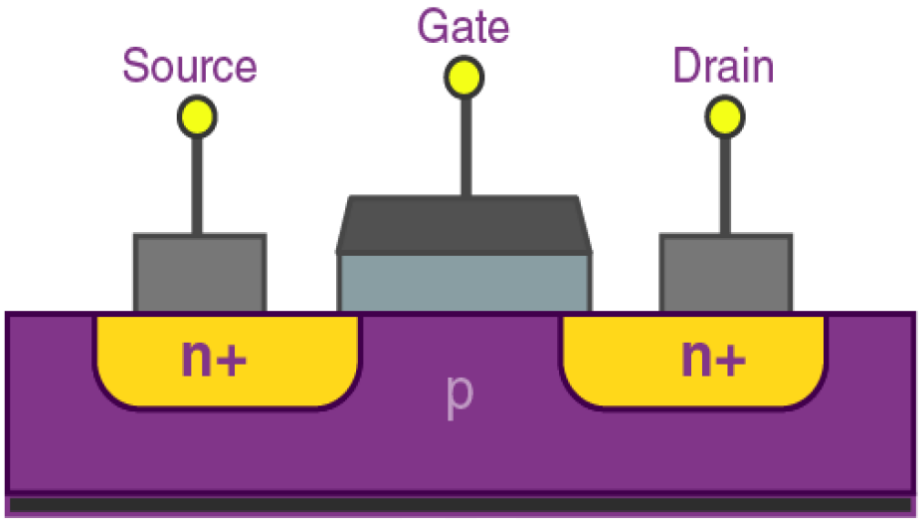

Figure 2.3: Basic NMOS Transistor [unk23]

A P-type MOS transistor is where the source and drain are doped with boron and the well is doped with phosphorus or arsenic. A P-type transistor is "on" when the gate voltage drops *below* a threshold voltage. Together, N-MOS and P-MOS transistors make up a CMOS (Complementary Metal-Oxide-Semiconductor) process. It is complementary because the threshold voltages that turns one on turns the other off, and vice versa. This comes in very handy when designing the basic logic gates that make up most digital design.

2.2 The IC Design Flow

The design flow for integrated circuits requires two paths: One for analog design and another for digital design. Where the two converge is referred to as "mixed-signal." (See Figure 2.4) The skills and tools required for each path are distinct and have diverged over the years (decades) as these two disciplines have become more and more complex. The next section will provide more information on the Electronic Design Automation industry.

The ultimate goal of the IC design flow is to produce a physical description of the design that can be used to manufacture it. This process is called "tape-out" because, historically, the patterns were written *out* to a *tape* that would be read by the fab.

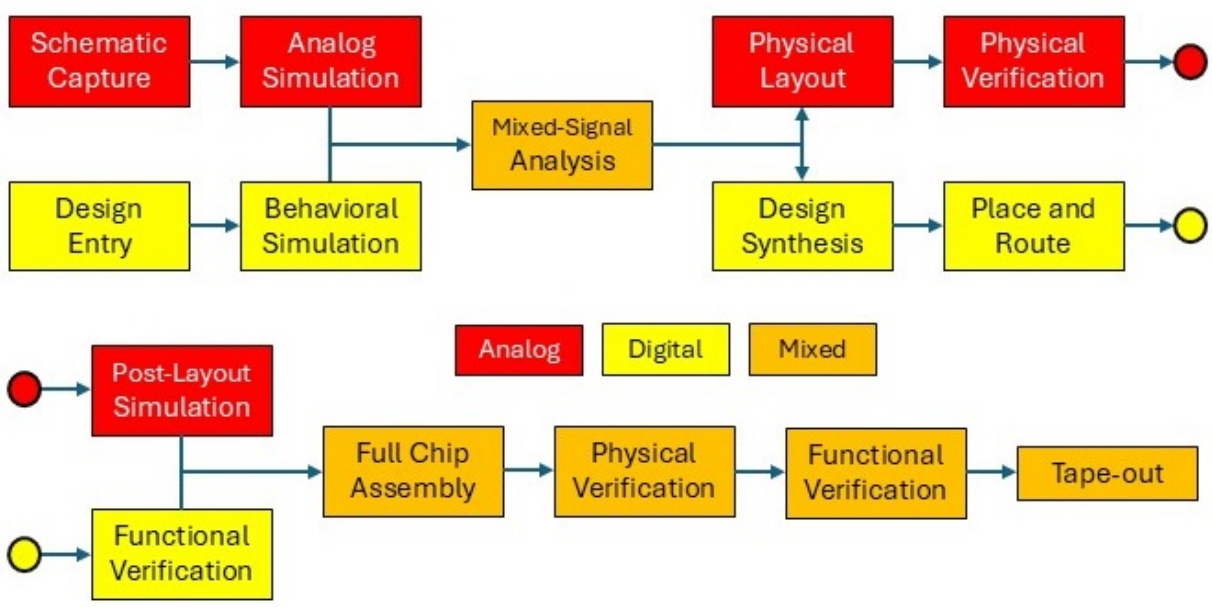

Figure 2.4: The IC Design Flow [DeL20]

2.2.1 Electronic Design Automation

Before describing the IC design flows in detail, it makes sense to first cover how the Electronic Design Automation (EDA) industry "grew up" alongside the semiconductor industry. "The commercial design tool business flourished when designs got too large for hand-crafted approaches and most semiconductor companies realized they did not have the expertise or resources to develop all their own tools." [NM13] Today, two of the Top 25 software companies in the world (by revenue) are EDA vendors, Synopsys and Cadence Design Systems [For23].

Two of the most-important inputs to EDA tools are the standard cell libraries and the process design kit. While these are typically provided by the fab/foundry, it makes sense to cover them in the context of EDA because of how they are used. Standard cell libraries are the menu of pre-defined IP/logic blocks that the designer (analog) or synthesis tool (digital) may choose from while designing their circuit. The robustness and completeness of these libraries provides flexibility and customization, but at the cost of complexity. Designs that use many different standard cells may be smaller, but they will take longer to design and validate.

Process design kits are how fabs/foundries communicate the specifications of their manufacturing process to designers. A typical PDK contains a primitive device library (e.g., basic transistors), verification checks (e.g., design rules), process constraints (e.g., minimum channel length), and simulation models. The design tools will use the PDK to ensure that the design can be manufactured by the factory and will perform as expected when it is.

2.2.2 Digital Design

Digital designs are those with a signal that is either "high" or "low" representing states (zeroes and ones) in Boolean logic. The exact voltage values that define the states are a function of the circuit's overall power voltage values. Digital designs typically consist of logic gates that interpret the inputs above a certain voltage threshold as ones and the inputs below a certain threshold as zeroes. In modern integrated circuits, Design Entry is done in a hardware description language (HDL), such as VHDL or Verilog, and divided into blocks

of smaller designs that each have their own functional requirements. The code then undergoes Behavioral Simulation to ensure it is functionally accurate. Following Mixed-Signal Analysis to ensure compatibility with corresponding analog circuits, the HDL code blocks undergo Design Synthesis to transform the code into the physical patterns. The Place and Route function then combines all of the blocks into one by *placing* each of them and *routing* the outputs of some to the inputs of others.

> This is an opportunity for optimization using artificial intelligence. There are often competing goals during place and route: Cost and quality. Cost usually comes in the form of die size. The larger the die, the more expensive it is to make. This is because fewer die will fit on each wafer, packaging costs may be higher, and overall yield (the number of good die per wafer) may be lower. Quality consists of reliability and performance. By spacing the blocks and interconnect wires further apart, the design will less noisy and more reliable. Greater spacing also makes signal matching easier. There are often corresponding groups of wires that should have the resistance so that the timing between them from block to block is similar. AI could be used to minimize die size within noise constraints while also achieving matched signals, where necessary.

Functional verification involves using testbenches to *verify* that the *functionality* of the design is correct per the specification. All possible input combinations should be used to ensure that there are no unexpected results.

> This is an opportunity for generative AI to create the testbenches from the spec. Ensuring complete formal verification is critical for digital design and using AI to create as many tests as needed, but as few as necessary, would ultimately save time and money.

2.2.3 Analog Design

Unlike digital designs, which are interpreted as 0 or 1 depending on the voltage level, analog designs are those with a continuously variable signal. There may still be digital logic within analog circuits. In fact, the goal of an analog circuit is often to create digital signals that interact with digital design elsewhere within the chip, but the tools and methods for analog design are quite different. Analog design starts with schematic capture. This is the symbolic representation of the circuit using individual transistors. See Figure 2.5 below for an example of an operational amplifier circuit.

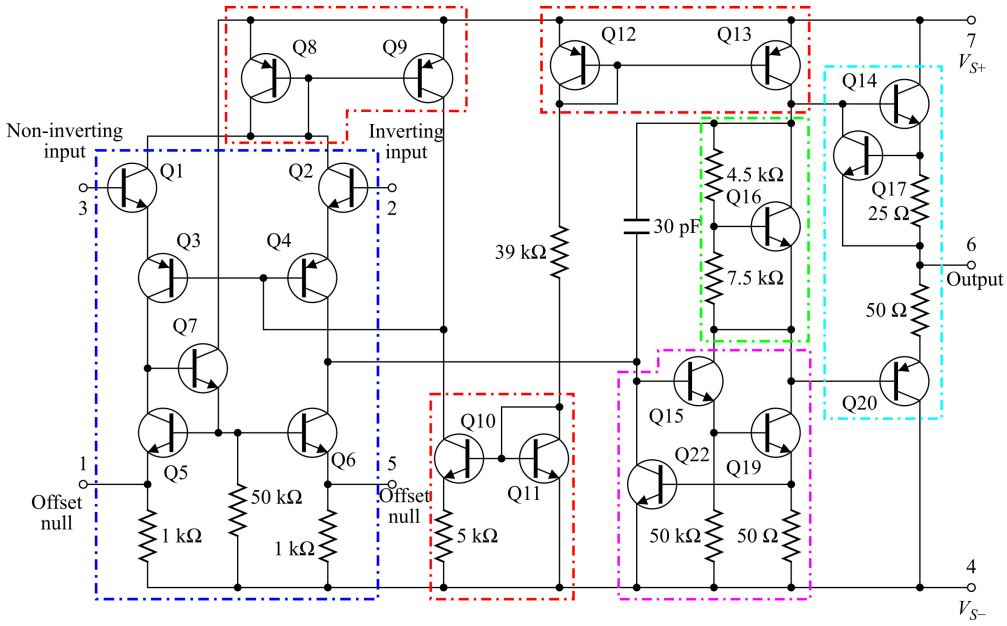

Figure 2.5: Operational Amplifier [Bra07]

Next, the schematics are complied into a netlist, a text file that contains every point (or net) in the design and what each is connected to. The netlist is used by an analog simulator in a test environment to ensure the design behaves as expected. Following Mixed-Signal Analysis to ensure compatibility with corresponding digital circuits, the schematics are *laid out* in their *physical* (geometric) form. See Figure 2.6 for an image of part of the physical layout of a high speed serial-deserializer reciever circuit (U.S. Patent No. 6,407,682, held by the author). Physical verification involves both ensuring that the layout matches the schematic, but also that the layout conforms to the design rules of the process. (More on this later.) Post-layout simulation will perform the same tests, using the same test environment as analog simulation, but with a netlist that is generated from the layout. This netlist will be much more detailed in that it will include parasitic effects of the devices and the wires used to connect them. Post-layout simluation is necessary because these effects impact the performance of the circuit, particularly timing, power, and signal integrity.

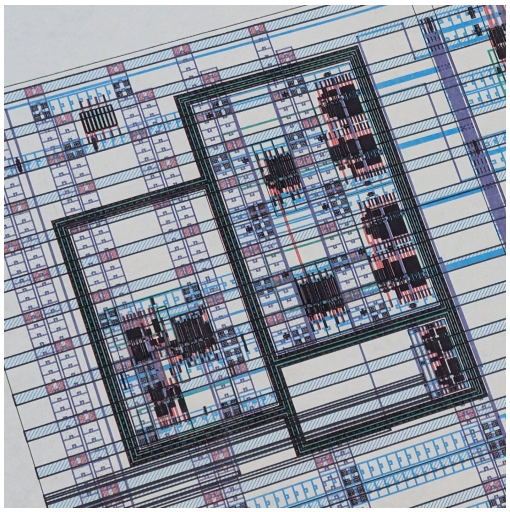

Figure 2.6: Partial Layout of an Analog Circuit

2.2.4 Mixed-Signal Design

In the context of a typical integrated circuit, mixed-signal design is when analog design and digital design come together to create the final product. Full chip assembly is the building of the entire chip by combining the digital and analog blocks together into a single unit that has to undergo physical verification (Does the physical design match the full-chip schematic and pass all the design rules?) and functional verification (Does the full chip design pass all of the functional tests proving that the analog and digital blocks were connected properly and work together?)

> This is another opportunity for AI to optimize space and accelerate the verification processes by creating testbenches.

Tape-out is the final step of the IC design process. Tape-out is specifically the point at which the graphic for the photomask of the circuit is prepare to be sent for fabrication. "The name originates from the use of magnetic tape to send the data to the manufacturing facility." [Mag99]

Chapter 3

The Semiconductor Industry

Before covering the manufacturing technology itself, it would be helpful to better understand the semiconductor industry and its key players. According to Investopedia, here are 10 Biggest Semiconductor companies by revenue. All data is as of June 20, 2024 and comes from TradingView.

Rank	Name	Revenue	Net Income	Market Cap
1	Samsung Electronics	$202.2B	$14.9B	$275.8B
2	NVIDIA Corp.	$78.9B	$42.6B	$3.35T
3	TSMC Ltd.	$71.5B	$27.7B	$932.0B
4	Intel Corp.	$55.24B	$4.07B	$130.4B
5	Broadcom Inc.	$42.6B	$10.3B	$839.1B
6	Qualcomm Inc.	$36.4B	$8.4B	$253.4B
7	SK Hynix Inc.	$28.7B	$-3.5B	$28.7B
8	ASML Holding NV	$28.3B	$7.7B	$418.8B
9	Applied Materials Inc.	$26.5B	$7.3B	$205.2B
10	Advanced Micro Devices	$22.8B	$1.1B	$249.9B

It's also helpful to understand that not all semiconductor companies are the same. On this list, only Samsung, TSMC, Intel, and SK Hynix manufacture semiconductor chips, and that's all that TSMC does. The latter is called a "pure-play foundry" (Foundry) and the former three are called "integrated device manufacturers" (IDMs). ASML and Applied Materials manufactures capital equipment used to manufacture semiconductors, so they are neither a foundry nor an IDM.

Because this paper will focus on the semiconductor foundry business, let's look at just the companies that are either pure-play foundries or IDMs. The revenue numbers are for Q1 2023 in USD, using data sourced from Trendforce.

Rank	Name	Country	Revenue
1	TSMC	Taiwan	$16,735M
2	Samsung	South Korea	$3,446M
3	GlobalFoundries	US	$1,841M
4	UMC	Taiwan	$1,784M
5	SMIC	China	$1,462M
6	HuaHong Group	China	$845M
7	Tower Semiconductor	Israel	$356M
8	PSMC	Taiwan	$332M
9	VIS	Taiwan	$269M
10	DB Hitek	South Korea	$234M
	Other		$556M

TSMC overtakes Samsung on this list because 100% of TSMC's revenue is in the foundry business, because that's all they do. Intel is not on this list because it doesn't earn enough revenue from its foundry business to earn a spot. SK Hynix is just an IDM, not a foundry.

Now that we've covered which semiconductor companies are foundries, which are IDMs, and which are both. Let's go over what a foundry actually does for its customers. The rest of this paper will be written from the perspective of the semiconductor foundry. In some cases, this could be an IDM that also has a foundry business. These companies have unique business challenges that also deserve mention.

3.1 The Foundry Business Model

The semiconductor foundry business model is very complex complex. Foundries don't design, build, and market their products directly to consumers. (IDMs do!) Instead, foundries develop and market their *technologies* to companies that design and market products. The goal of a semiconductor foundry is to convince a semiconductor company that they can be trusted to help the customer realize their vision of a product. This not only means they must have the necessary technology, but also be able to provide it on time, under budget, and at sufficient quality. As technologies get more advanced they get more expensive, take longer to develop, and are subject to new, different, and more extreme quality issues. In Project Management terms, this is a version of *The Iron Triangle* with "technology" replacing "scope" as the baseline (See Figure 3.1).

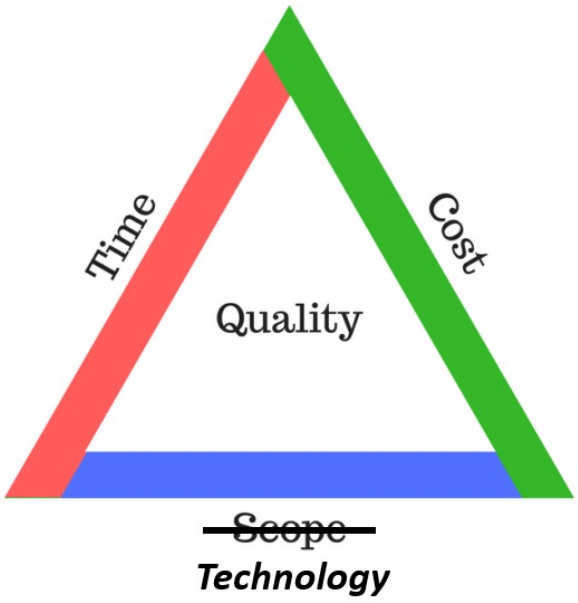

Figure 3.1: The Iron Triangle

In addition to manufacturing services, semiconductor foundries also provide design services and the intellectual property (IP) that are the building blocks of integrated circuit chips. These building blocks may be as simple as standard logic cells and libraries, or as complex as image sensors and high-speed I/O interfaces. Each of these blocks may be part of an a la carte menu of IP and design services that allow the foundry to meet the specific needs of each customer.

3.2 Integrated Device Manufacturers (IDMs)

Most semiconductor companies started out as Integrated Device Manufacturers, or IDMs. "When the CEO of AMD, Jerry Sanders said 'Real men have fabs,' he was suggesting that chip design and process technology had to be tightly coupled." [NM13] TSMC's success has proven this to be largely false. However, IDMs face unique challenges when they also enter the foundry business.

> "Before TSMC, a couple of small companies, mostly based in Silicon Valley, had tried building businesses around chip design, avoiding the cost of building their own fabs by outsourcing manufacturing. These 'fabless' firms were sometimes able to convince a bigger chipmaker with spare capacity to manufacture their chips. However, they always had second-class status behind the bigger chipmakers' own production plans. Worse, they faced the constant risk that their manufacturing partners would steal their ideas. Not having to build fabs reduced startup costs, but counting on competitors to manufacture chips was a risky business model." [Mil22]

These fears, not getting access to capacity and having their ideas stolen, create barriers to entry for IDMs who want to *also* be foundries.

Chapter 4

The IC Manufacturing Process

The integrated circuit manufacturing process has been (for all intents and purposes) following Moore's Law since 1965. What follows is a high-level explanation of fab operations, then an explanation of how these operations are combined to manufacture an integrated circuit.

Figure 4.1: Inside a Semiconductor Fab [Cal23]

4.1 Fab Operations

Fab operations are the different actions taken throughout the manufacturing process. Some are done several times, some are done several different ways, and some are done only once. Understanding these actions is critical to understanding the overall process flow, so it makes sense to explain them first.

4.1.1 Deposition

Deposition puts new material onto the wafer. There are several ways this is done and each is for a specific purpose. Thermal oxidation is done in a quartz furnace at 1000°to 1200°C. Once the wafers reach the desired temperature, they are exposed to pure oxygen and a layer of SiO_2 is grown on the surface. Wet oxidation is done at much lower temperatures (about 95°C) and uses water. Thermal oxidation produces higher quality, but is slower and more expensive.

Chemical vapor deposition (CVD) reacts gasses above the wafer to form a thin film of the desired material on the surface. Atomic layer deposition (ALD) is similar to CVD, except the reactant gasses are supplied separately, creating the film one atomic later at a time on the wafer surface. ALD is slower than CVD, but it is easier to control and allows for extremely precise film thickness and uniformity.

Sputtering uses plasma ions to bombard a suspended metal target, knocking metal atoms free that then coat the wafer below. Electroplating places a voltage across a metal target and the wafer surface while both are in an electrolyte solution. The voltage differential causes metal ions to enter the solution and travel to the surface of the wafer. Typically, sputtering is done first to create the metal base layer, then electroplating is done to add volume.

4.1.2 Polishing

Chemical mechanical polishing or planarization (CMP) removes excess material from the wafer, leaving a flat surface. This is typically done with a rotating polish wheel and a solvent. Because the center of the wheel doesn't move as fast at the edges, the wafer also rotates to ensure uniformity. This is critical at many stages of the manufacturing process, because "each step builds up on the previous steps, and must provide a well controlled structure for the following steps." [Oli10]

4.1.3 Lithography

Lithography creates a pattern on the wafer in photoresist, which breaks down in reaction to light. First, the resist is "spun" onto the wafer. That is, while the wafer rotates, resist is dispensed in the middle and spreads evenly across the wafer's surface. Next, the resist is exposed to UV light through a mask, which creates a pattern on the wafer. This is either done one die at a time or several. A stepper is used to move across the wafer and ensure all die are exposed. Finally, the resist is developed, which causes the UV-exposed resist to wash away, leaving the desired pattern.

"Lithography is a critical bottleneck technology that's enabled geometric scaling to keep pace with Moore's prediction over the last several decades. Each generation of lithographic equipment enables fabs to etch smaller substrate features and pack more transistors on each chip, which improves speed, lowers costs, and boosts power efficiency across the board." [Ric23]

4.1.4 Etch

Etch follow lithography and, like polishing, removes excess material from the wafer. However, the material that etch removes is that which is exposed after the development step in lithography. There are two types of etch: Dry and wet. Dry (plasma) etch removed material from the wafer etching vertically (patterned etch). Wet etch removes/cleans material from the wafer both vertically and horizontally. Following the etching process, the wafer is then put in an asher, which removes the remaining photoresist that was left behind to create the pattern.

> "The AI technologies can be used to adjust tool parameters to achieve greater accuracy by deploying real-time tool-sensor data, metrology readings, and tool-sensor readings from earlier process steps, enabling ML algorithms to capture nonlinear relationships between process time and outcomes (e.g., etch depth)." [Luc+21] Given that tools are never perfectly identical, using AI to optimize an individual etching tool's "recipe" would create better tool matching between production lines of the same process.

4.1.5 Implant & Anneal

Implant is the injection of dopant ions (n- or p-type) into the wafer by accelerating them into it at high speed there by changing the conductivity of the material. As mentioned earlier, the source and drain of an n-type

transistor are created by implanting phosphorus (P) or arsenic (Ar) ions into the silicon; the well in which the source and drain sit is implanted with boron (B). For a p-type transistor, the implanted ions are the opposite.

Anneal is the quick heating of the wafer to heal the damage and activate the dopants. During the ion implantation process, the crystalline structure of the wafer is damaged. Repairing it with heat (up to 1300°C) by placing the wafer in furnace chamber filled with nitrogen gas for hours, will give the structures the consistent conductivity required to function properly as a switch.

4.1.6 Metrology, E-Test, & Sort

Metrology steps are done after key points in the process to ensure that it stays in control. For example:

- Before/after some deposition steps, a particle check is done that detects and maps the implanted particles.
- After some deposition steps, the thickness of the deposited layer is measured.
- After some planar steps, the thickness of the polished layer is measured.
- After some etch steps, the height or depth of the etched feature (including the critical dimension) is measured.
- After lithography, the critical dimension is measured and alignment to earlier patterns is checked.
- After some metal polish steps, the metal layer resistance is measured and used to calculate the metal layer CD.

At E-Test, the wafer is tested to ensure it has been processed correctly. Testing is not done on the die, but rather on test structures that were created in the "scribeline" during processing. A scribeline is the space between die where the cuts separating them will be made. Multiple test structures are created all across the wafer. Some are tested in-line (like metal interconnects) to catch problems early. All can be tested after the wafer is fully processed. The results can be used to improve the process and identify bad wafers. These are example of structures and the tests performed on them:

- Resistors: resistance, thickness, critical dimension
- Capacitors: capacitance, dielectric thickness, gate leakage, breakdown voltage
- P/N Junctions: breakdown voltage, leakage
- Transistors: threshold voltage, saturation current, off-state leakage, length, width
- Isolation Structures: punchthrough

Wafers that pass E-Test are sent to Sort. At Sort, each die is tested to ensure that it functions properly. Each product has its own test program that runs the tests and collects the results. Bad die are noted on the wafer map so that at Assembly; only good die are packaged. Sort data test results may also be used to further analyze and improve the process.

> Sort testing is getting harder and taking longer due to advanced processes being more sensitive to variation, so more defects are getting through. Test capabilities are not keeping up and haven't really changed in many years. Using AI to improve sort would save money by finding more defects before system testing.

4.2 Fab Process

The fabrication process steps utilize each of the operations, repeating some multiple times. Starting with a polished wafer, here is a typical ordered list of process steps:

1. Lithography: create the pattern for the n-type isolation trenches (wells)
2. Polishing: ensure the layer of oxide is smooth and consistent
3. Implant: create the n-wells for the transistors by doping the silicon with arsenic or phosphorous
4. Anneal: heal the damage and activate the n-well
5. Lithography: create the pattern for the p-type isolation trenches (wells)
6. Polishing: ensure the layer of oxide is smooth and consistent
7. Implant: create the p-wells for the transistors by doping the silicon with boron
8. Anneal: heal the damage and activate the p-well
9. Lithography: create the pattern for the transistor gates
10. Deposition: create the poly-silicon transistor gates
11. Lithography: create the pattern for the transistor sources and drains
12. Deposition: create the sources and drains of the transistors by doping the silicon with arsenic, phosphorous, or boron
13. Lithography: create the pattern for the transistor gates
14. Etch: remove the poly-silicon transistor gates
15. Deposition: replace the poly-silicon gates with aluminum by sputter
16. Deposition: add a layer of insulating oxide over the whole wafer
17. Polishing: ensure the layer of oxide is smooth and consistent
18. Lithography: create the pattern for the transistor contacts
19. Deposition: add the tungsten contacts by sputter
20. Polishing: ensure the top of the contacts are smooth and consistent
21. Lithography: create the pattern for the lowest aluminum metal layer
22. Deposition: add the initial aluminum by sputtering
23. Deposition: add the rest of the aluminum by electroplating
24. Polishing: ensure the top of the metal layer is smooth and consistent
25. *Repeat last four for each metal layer*
26. Metrology, E-Test, and Sort

Bibliography

[Moo65] Gordon Moore. "Cramming more components onto integrated circuits". In: *Electronics* 38.8 (1965). DOI: http://cva.stanford.edu/classes/cs99s/papers/moore-crammingmorecomponents.pdf.

[Mag99] Mike Magee. *What the Hell is... a tapeout?* 1999. URL: https://www.theregister.com/1999/07/14/what_the_hell/. (Accessed: 12.04.2024).

[Bra07] Daniel Braun. *Redrawn png file (from User:Omegatron), Page #4 of datasheet, CC BY 2.5*. 2007. URL: https://commons.wikimedia.org/w/index.php?curid=2205381. (Accessed: 12.04.2024).

[Oli10] Michael R. Oliver. *Chemical-Mechanical Planarization of Semiconductor Materials*. 2010. ISBN: 9783540431817. DOI: https://doi.org/10.1007/978-3-662-06234-0.

[Cen13] IEEE History Center. *History of Engineering and Technology*. 2013. URL: https://engineeringhistory.tumblr.com/post/48118429233/first-integrated-circuit-1958. (Accessed: 12.08.2024).

[NM13] Daniel Nenni and Paul McLellan. *Fabless: The Transformation of the Semiconductor Industry*. A SemiWiki.com Project, 2013, pp. 70, 86. ISBN: 9781497525047.

[BW20] Luc Oliver Bauer and E. Marshall Wilder. *The Microchip Revolution: A Brief History*. 2020, p. 15. ISBN: 9798677250699.

[DeL20] Jean-Jacques DeLisle. *What Is Mixed-Signal IC Design?* 2020. URL: https://www.allaboutcircuits.com/technical-articles/what-is-mixed-signal-ic-design/. (Accessed: 12.08.2024).

[Chi+21] Chen-Fu Chien et al. "Production-Level Artificial Intelligence Applications in Semiconductor Manufacturing". In: *2021 Winter Simulation Conference (WSC)*. 2021, pp. 1–8. DOI: 10.1109/WSC52266.2021.9715399.

[Luc+21] Cristina Luca et al. "AI in Semiconductor Industry". In: Sept. 2021, pp. 105–112. ISBN: 9788770226646. DOI: 10.1201/9781003337232-10.

[Mil22] Chris Miller. *Chip War*. Scribner, 2022, p. 168. ISBN: 9781982172008.

[Cal23] Swagelok Northern California. *Components for Semiconductor Fab Equipment for Northern California Manufacturers*. 2023. URL: https://northerncal.swagelok.com/semiconductor-fab-equipment-snc. (Accessed: 12.11.2024).

[For23] Forbes. *2023 Forbes list for the "Software & Programming" industry*. 2023. URL: https://en.wikipedia.org/wiki/List_of_the_largest_software_companies. (Accessed: 12.09.2024).

[Ric23] Corey Richard. *Understanding Semiconductors*. Apress Media LLC, 2023, p. 63. ISBN: 9781484288467.

[unk23] unknown. *Silicon Transistor Diagram*. 2023. URL: https://artpictures.club/autumn-2023.html. (Accessed: 12.09.2024).