CENG 442 Digital System/Lab

Lab Assignment 1

The purpose of this lab is to construct the datapath and the instruction decoder for a basic RISC-V (RV32I) core. Your VHDL code will be verified through simulation. Figure /reffig:datapath shows one possible design. This design should be capable of expcuting all of the Register-Register, Register-Imeediate, Jump, and Branch instructions. Load/Store instructions may be handled by a separate unit.

There are several inputs to the datapat that will be provided by the instruction decoder. They are described in the following table:

Name	**Bits**	**Description**
Asel	5	Select register to read from port A of the register file.
Bsel	5	Select register to read from port B of the register file.
Dsel	5	Select register to be written to.
Dlen	1	D latch enable. When this signal is 1, the register selected by Dsel will be latched (written to) on the rising edge of the clock.
PCAsel	1	Select the source for the A input to the ALU: **0** Feed the register selected by Asel into the A input of the ALU. **1** Feed the program counter into the A input of the ALU.
IMMBsel	1	Select the source for the B input to the ALU: **0** Feed the register selected by Bsel into the B input of the ALU. **1** Feed the immediate data (IMM) into the B input of the ALU.
PCDsel	1	Select the source for the D input to the register file: **0** Feed the output of the ALU into the D input of the register file. **1** Feed the program counter into the D input of the register file.
PCie	1	Program Counter increment enable. When this signal is 1, the program counter will be incremented (by 4) on the rising edge of the clock.
PCle	1	Program Counter latch enable. This signal does not come directly from the instruction decoder, but is generated by the branch test unit. When this signal is 1, the program counter will be loaded with a new value from the ALU on the rising edge of the clock.
isBR	1	Branch enable. When this signal is 1, the branch test unit is enabled to load the program counter with the branch target address on the rising edge of the clock. The branch test unit determines whether or not to perform the load.
BRcond	3	The Branch condition code selects the test performed by the branch test unit.
ALUFunc	4	The ALU function code selects which operation is performed by the ALU
IMM	32	The immediate data contained within the instruction

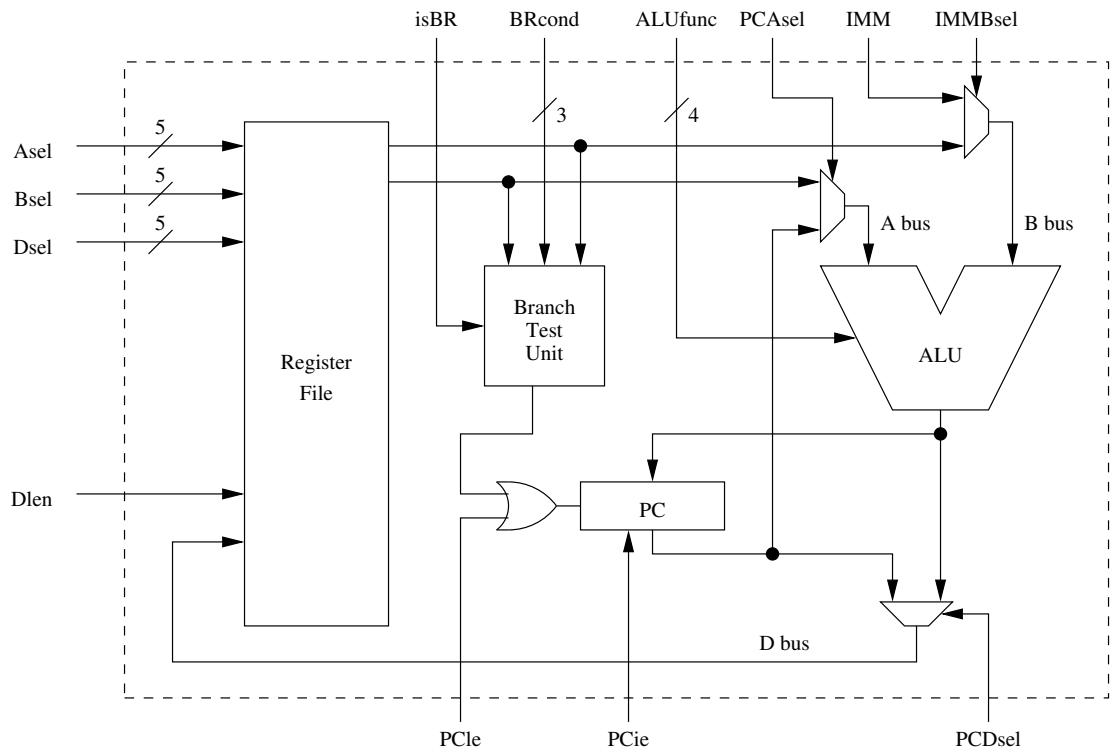

Figure 1: Basic RISC-V datapath.

All of the control signals could be bundled together in a control word, using the VHDL record type. This will make the schematic for the complete CPU much easier to read. For example, the following code could be placed in a package, and then used by the instruction decoder and the datapath.

```
type control_word is record
  Asel    : std_logic_vector(4 downto 0);
  Bsel    : std_logic_vector(4 downto 0);
  Dsel    : std_logic_vector(4 downto 0);
  Dlen    : std_logic;
  PCAsel  : std_logic;
  IMMBsel : std_logic;
  PCDsel  : std_logic;
  PCie    : std_logic;
  isBR    : std_logic;
  BRcond  : std_logic_vector(2 downto 0);
  ALUFunc : std_logic_vector(3 downto 0);
  IMM     : std_logic_vector(31 downto 0);
end record control_word;
```

What to Turn In

You must demonstrate your design to the Lab instructor, and you must turn in a lab report. Your lab report must be a file in Portable Document Format (PDF) submitted to the D2L dropbox. Your lab report should contain an overview, the design simulation/verification results, and conclusions. **VHDL code and user constraint files should be included as appendices to your report.**