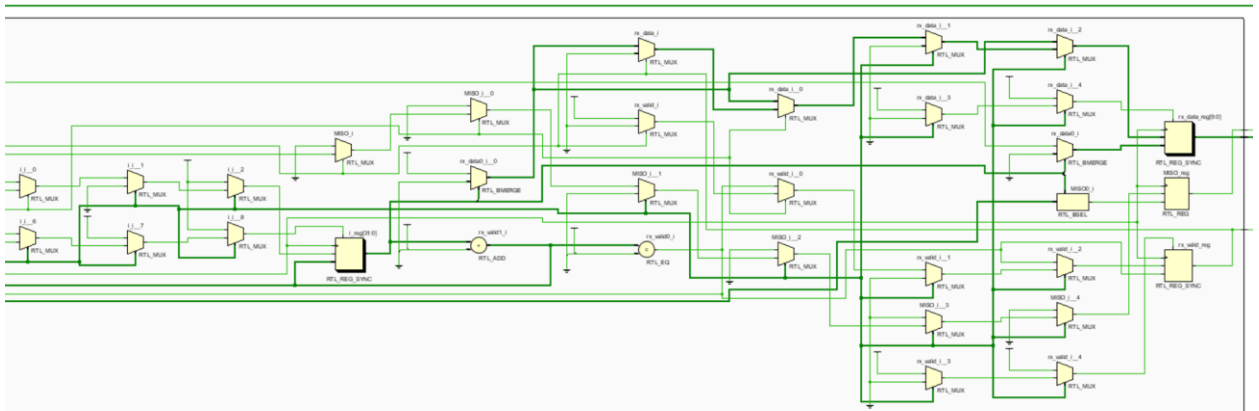
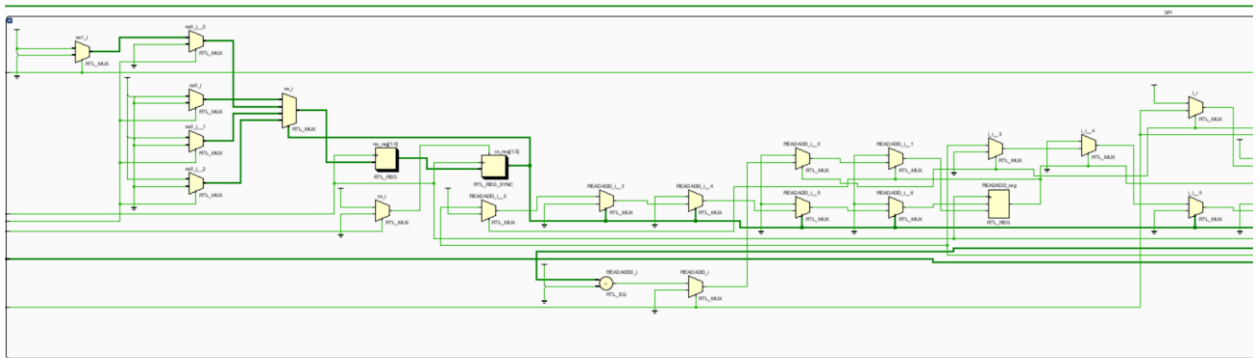
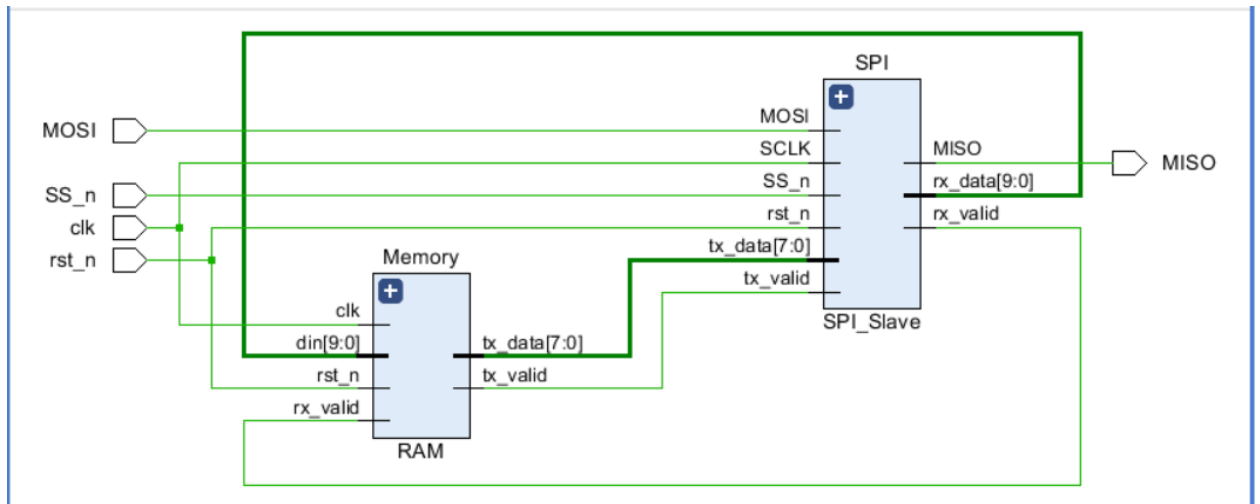
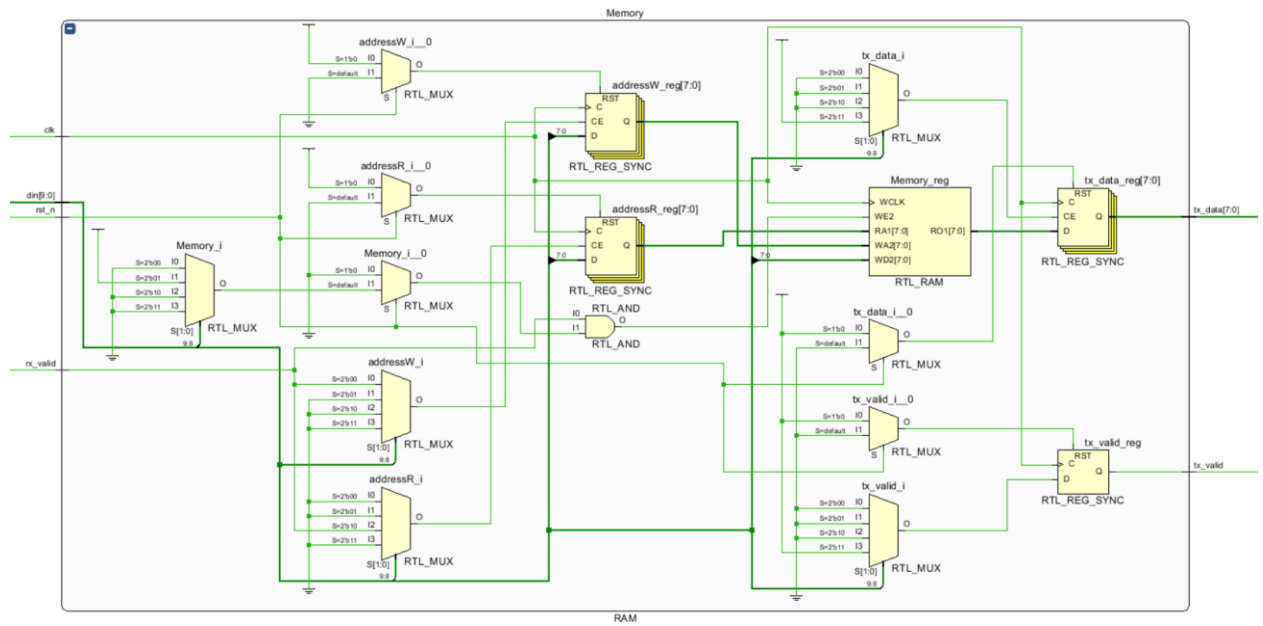


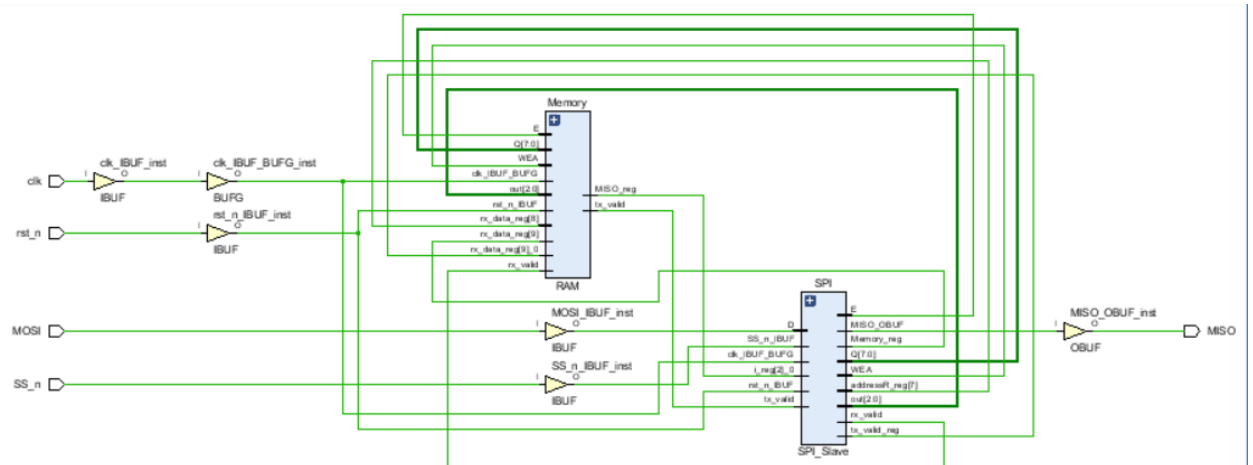
2-Synthesis:

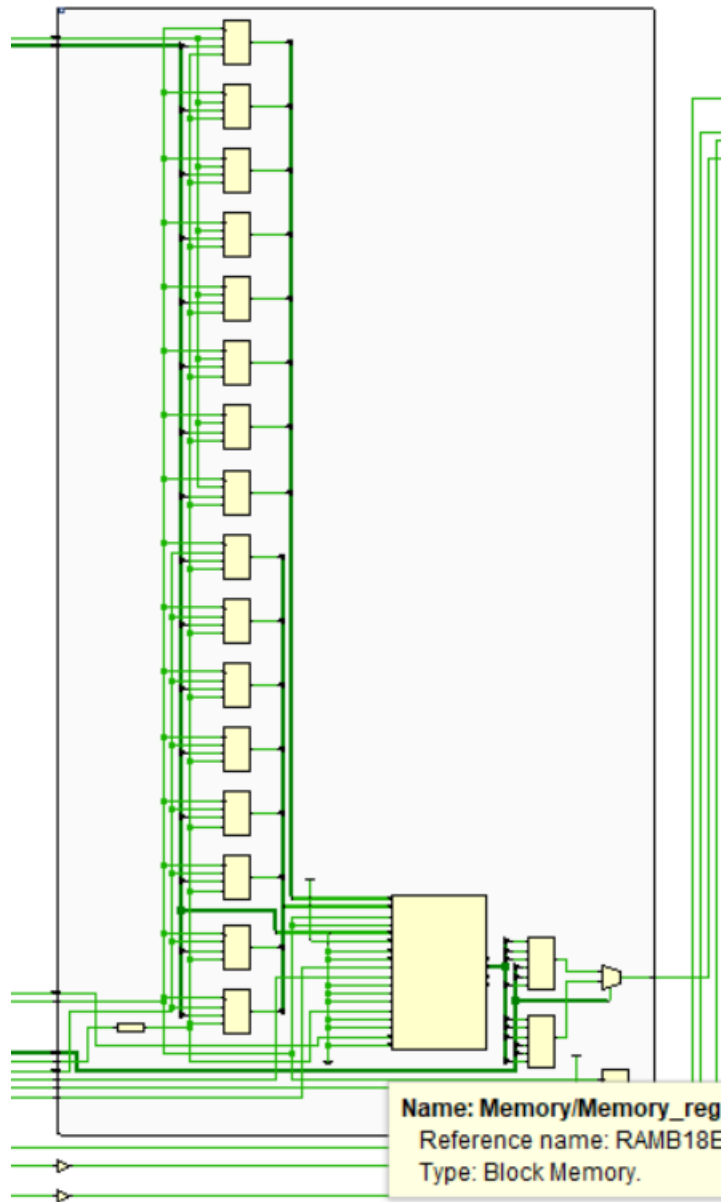
- Elaboration:

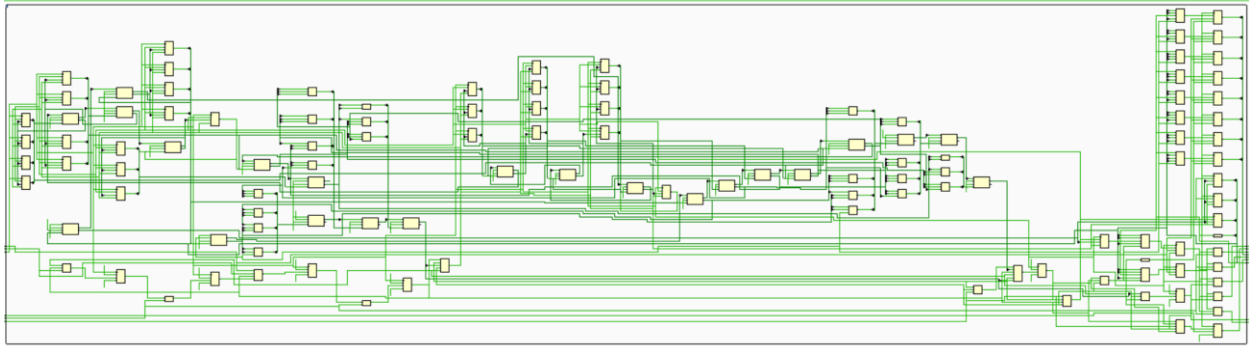




- Synthesis:(seq)







INFO: [Synth 8-5544] ROM "ns1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

State	New Encoding	Previous Encoding
IDLE	00	00
CHK_CMD	01	01
READ	10	11
WRITE	11	10

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'

Tcl Console Messages Log Reports Design Runs **Timing** x Debug ? _ □ □

Design Timing Summary

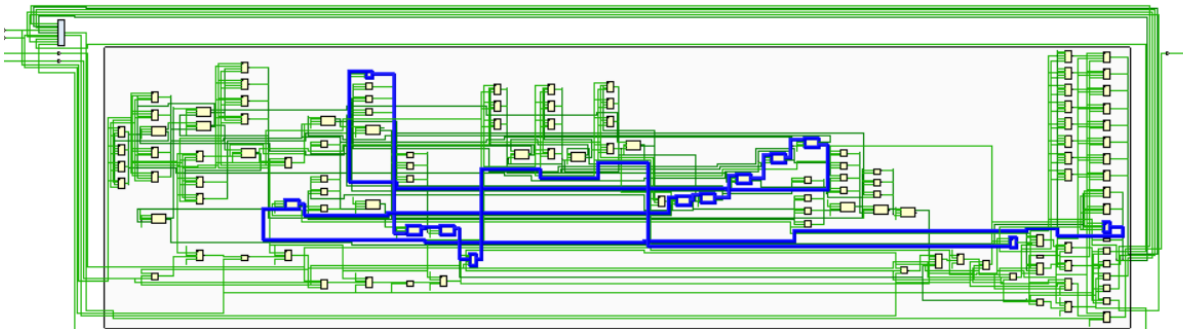
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (4)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.000 ns	Worst Hold Slack (WHS): 0.149 ns	Worst Pulse Width Slack (WPWS): 3.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 185	Total Number of Endpoints: 185	Total Number of Endpoints: 69

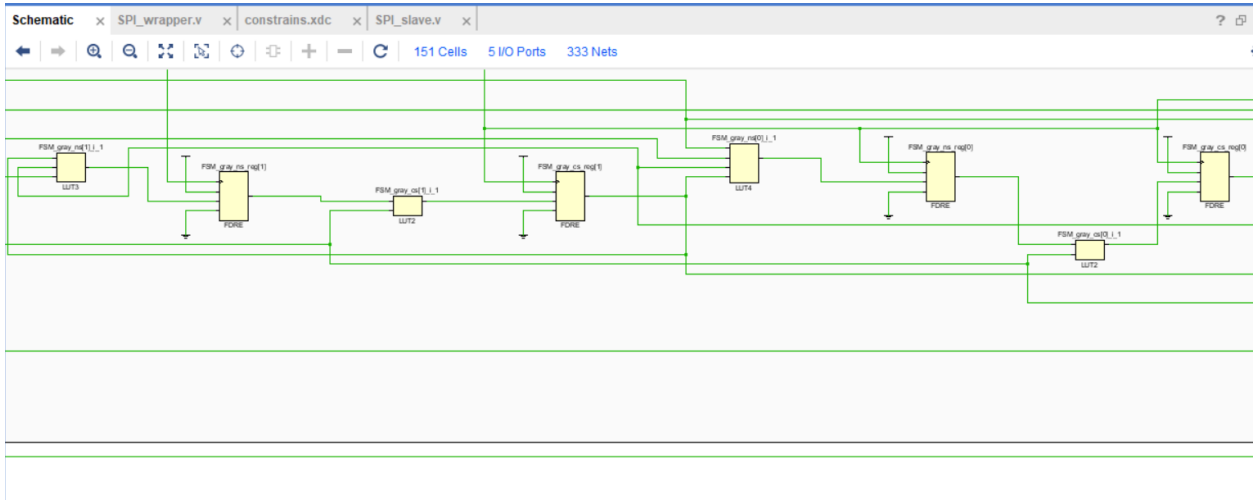
All user specified timing constraints are met.

Timing Summary - timing_1

@142.86 MHZ

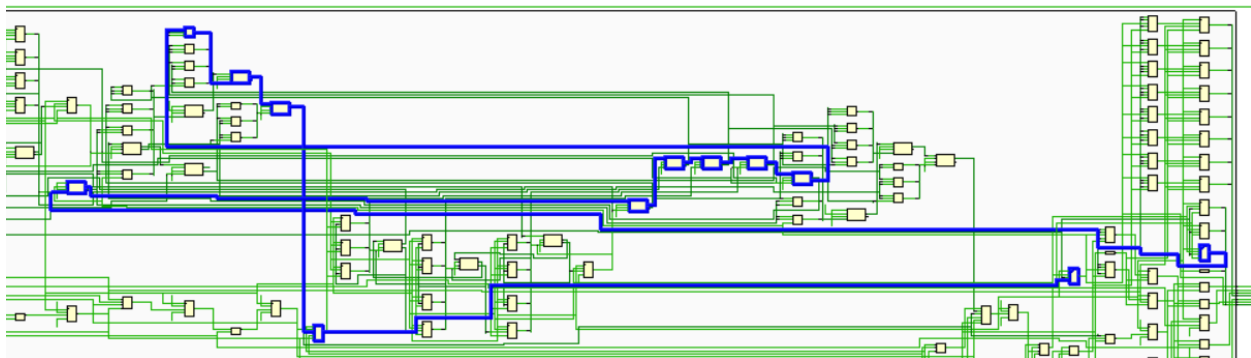


- Synthesis :(gray)

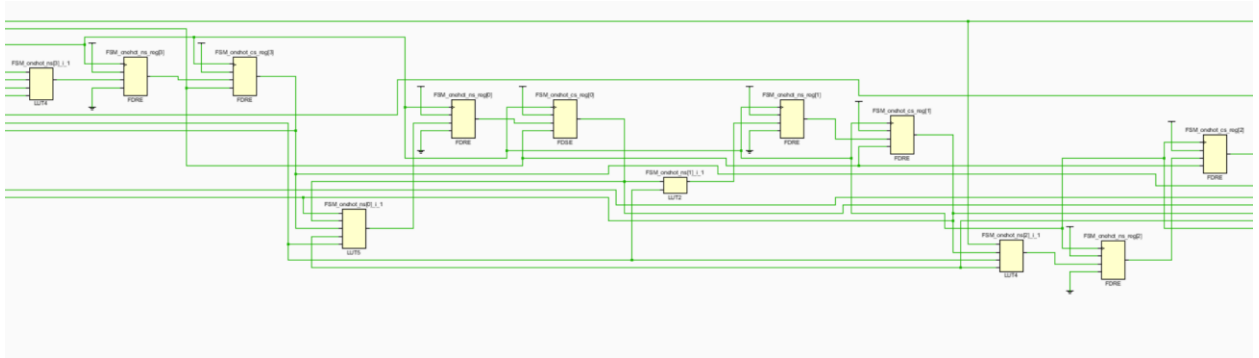


@142.86MHZ

State	New Encoding	Previous Encoding
IDLE	00	00
CHK_CMD	01	01
READ	11	11
WRITE	10	10



- Synthesis :(one_hot)

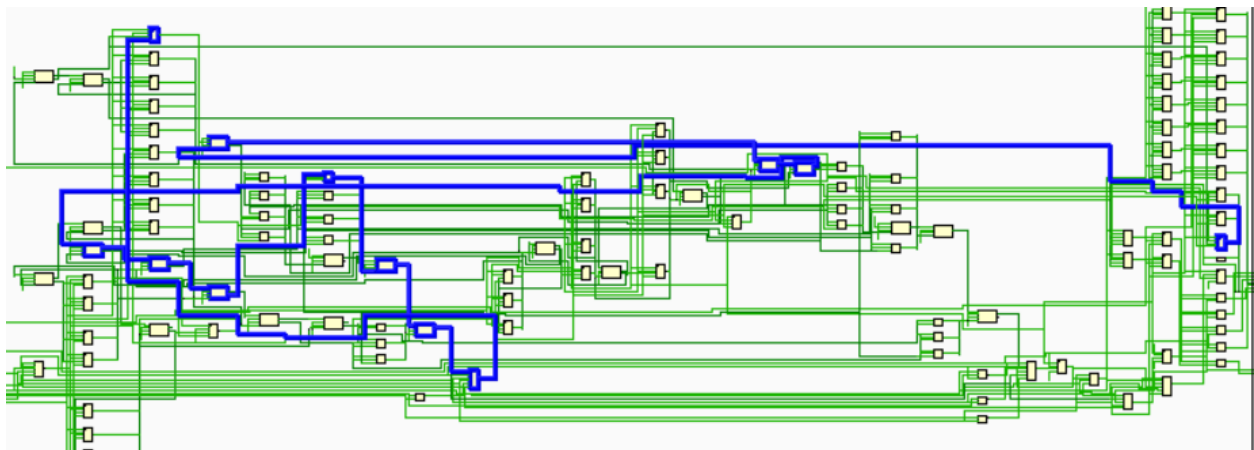


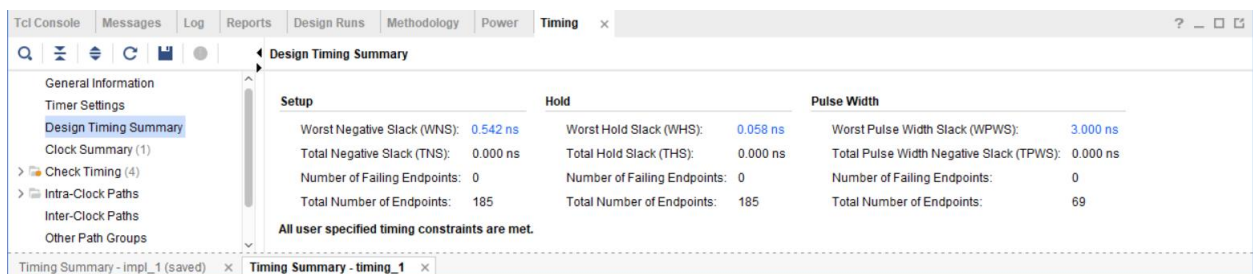
Tcl Console Messages Log Reports Design Runs Timing x Debug			
Design Timing Summary			
<div>General Information</div> <div>Timer Settings</div> <div>Design Timing Summary</div> <div>Clock Summary (1)</div> <div>Check Timing (4)</div> <div>Intra-Clock Paths</div> <div>Inter-Clock Paths</div> <div>Other Path Groups</div> <div>User Ignored Paths</div> <div>Unconstrained Paths</div> <div>Timing Summary - timing_1</div>			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 0.000 ns	Worst Hold Slack (WHS): 0.146 ns	Worst Pulse Width Slack (WPWS): 3.000 ns	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	
Total Number of Endpoints: 189	Total Number of Endpoints: 189	Total Number of Endpoints: 73	
All user specified timing constraints are met.			

@142.86 MHz

State	New Encoding	Previous Encoding
IDLE	0001	00
CHK_CMD	0010	01
READ	0100	11
WRITE	1000	10

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'





Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▼ N SPI_wrapper		51	66	1	37	51	8	0.5	5	1
I Memory (RAM)		3	17	1	5	3	0	0.5	0	0
I SPI (SPI_Slave)		48	49	0	36	48	7	0	0	0

- > Vivado Commands (3 infos, 2 status messages)
- > Elaborated Design (10 infos, 13 status messages)
- > Synthesis (2 warnings, 31 infos, 11 status messages)
- > Synthesized Design (1 warning, 9 infos, 6 status messages)
- > Implementation (92 infos, 225 status messages)
- > Implemented Design (10 infos, 5 status messages)