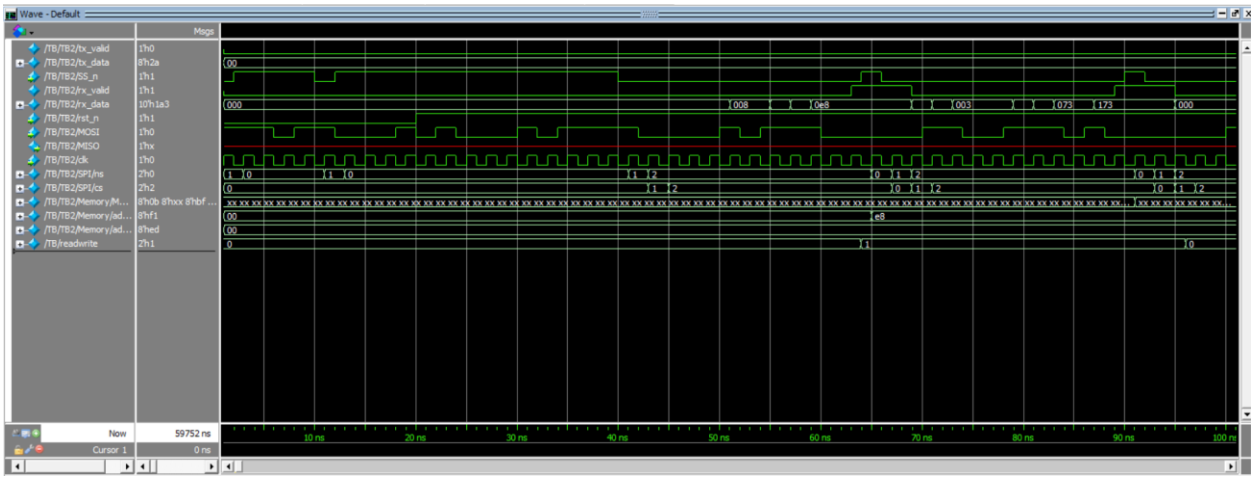
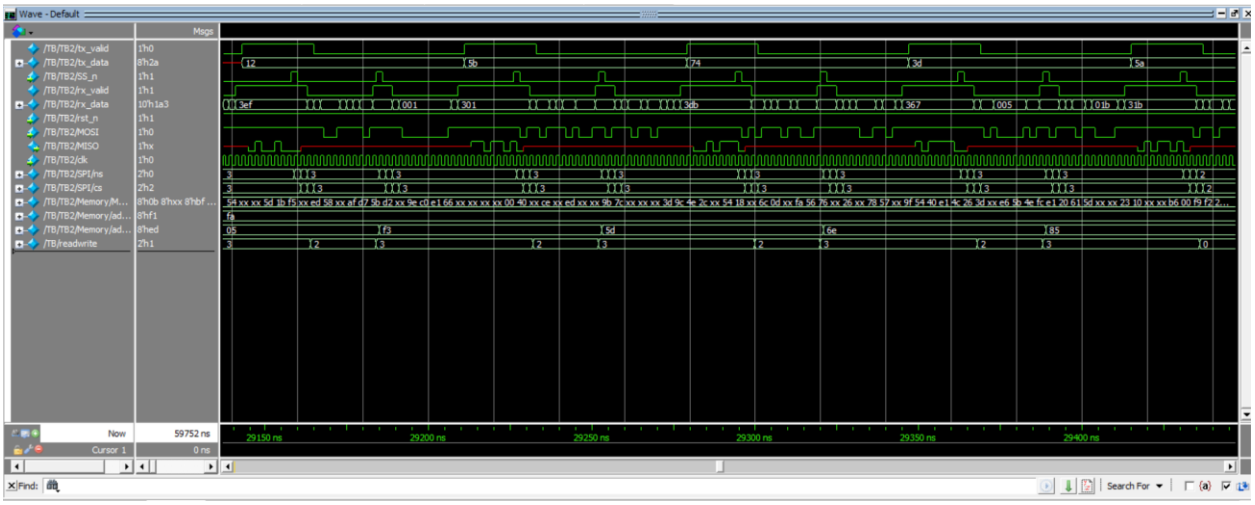
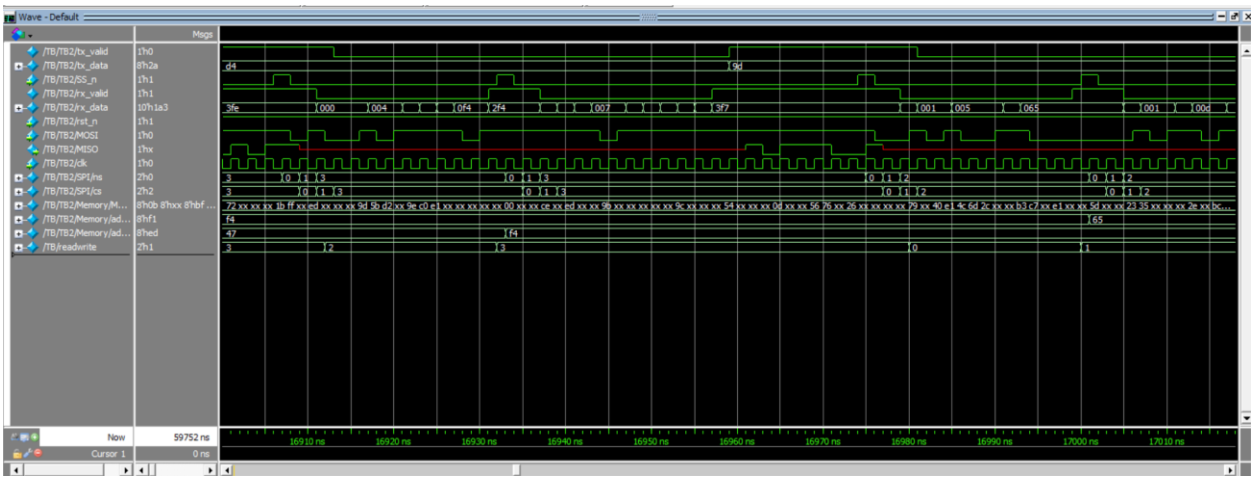
SPI Project

1-Waveforms:

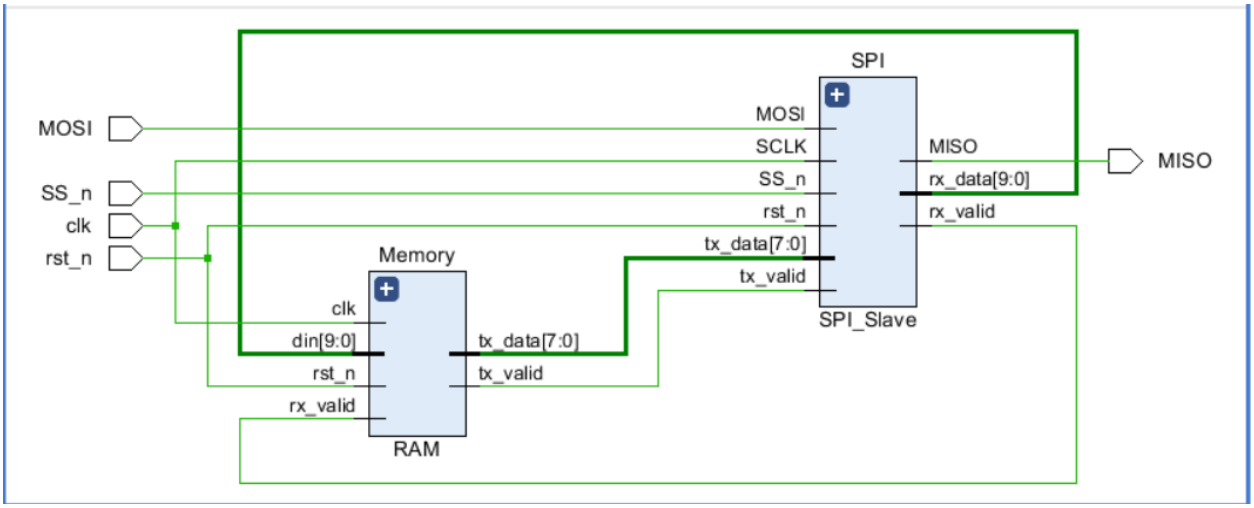


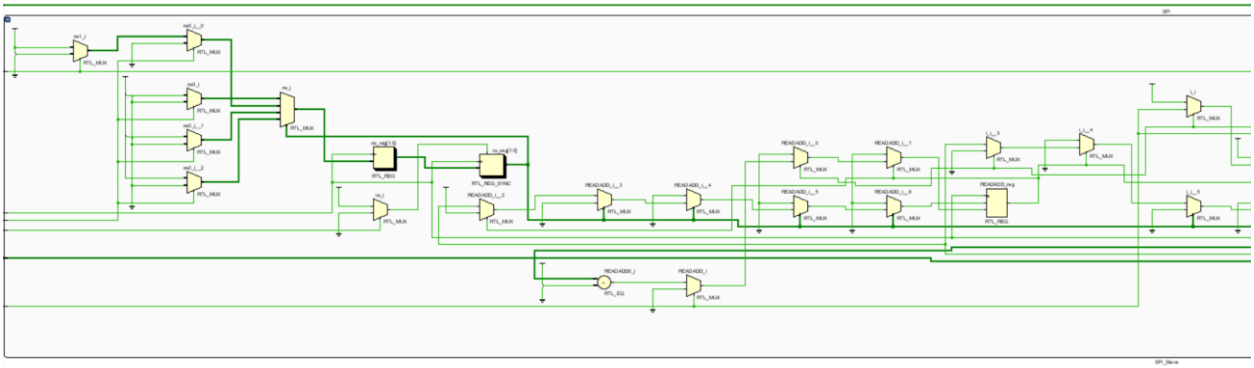


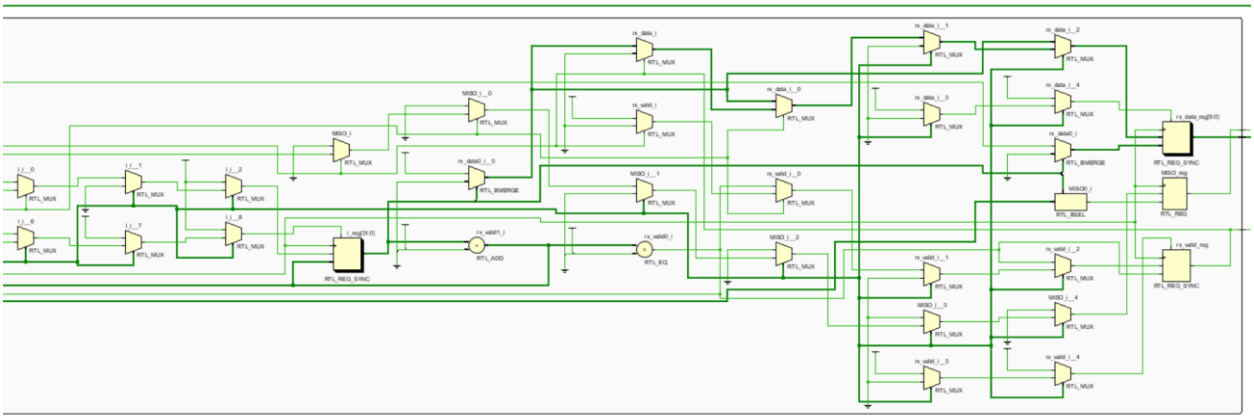


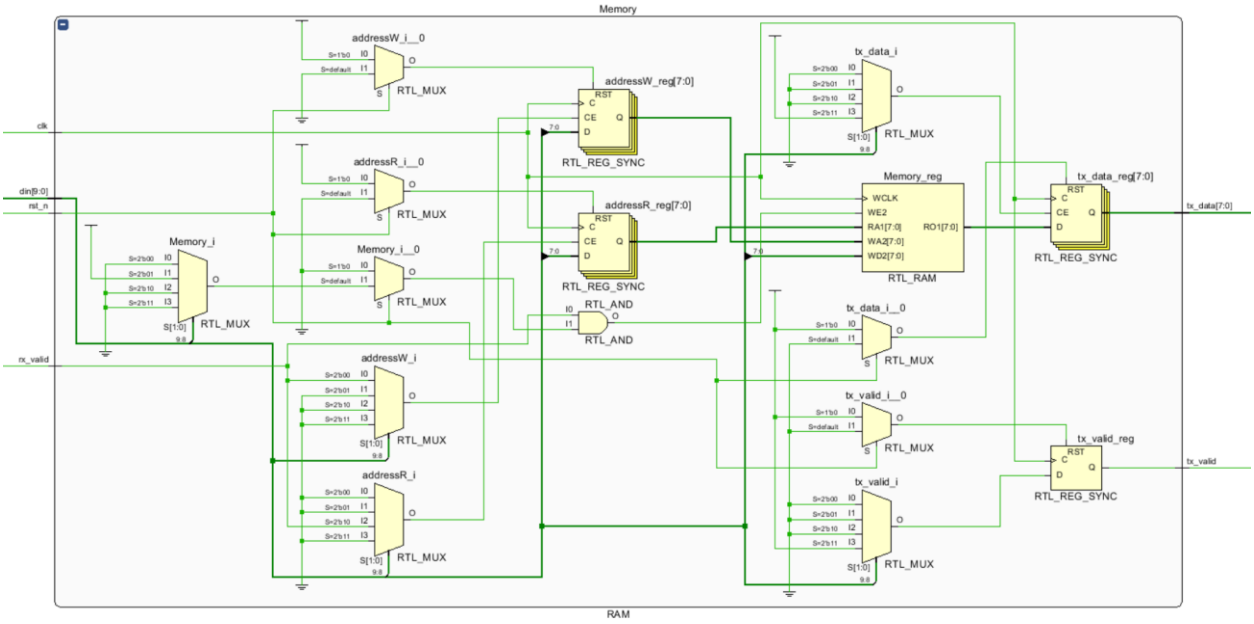
2-Synthesis:

- Elaboration:

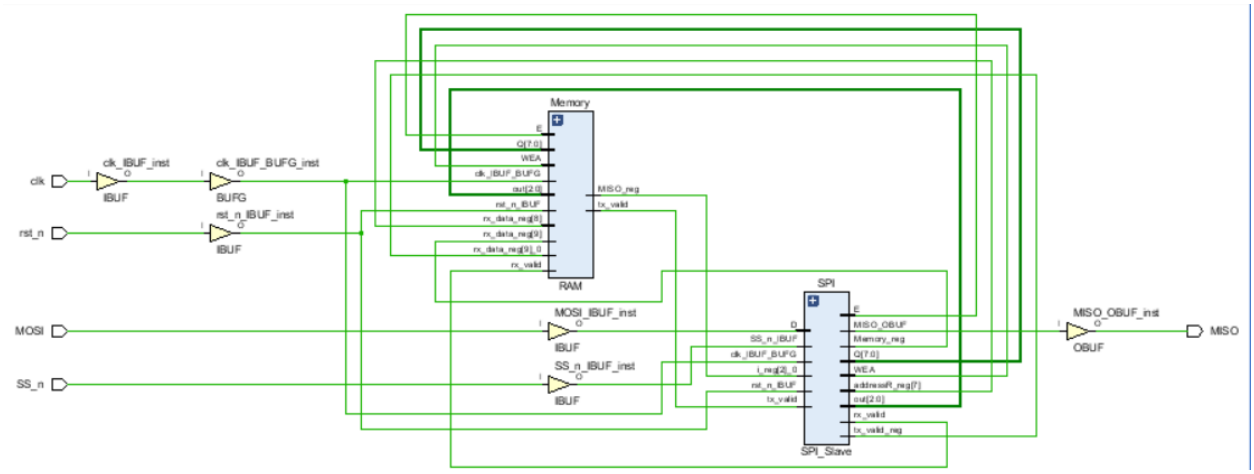


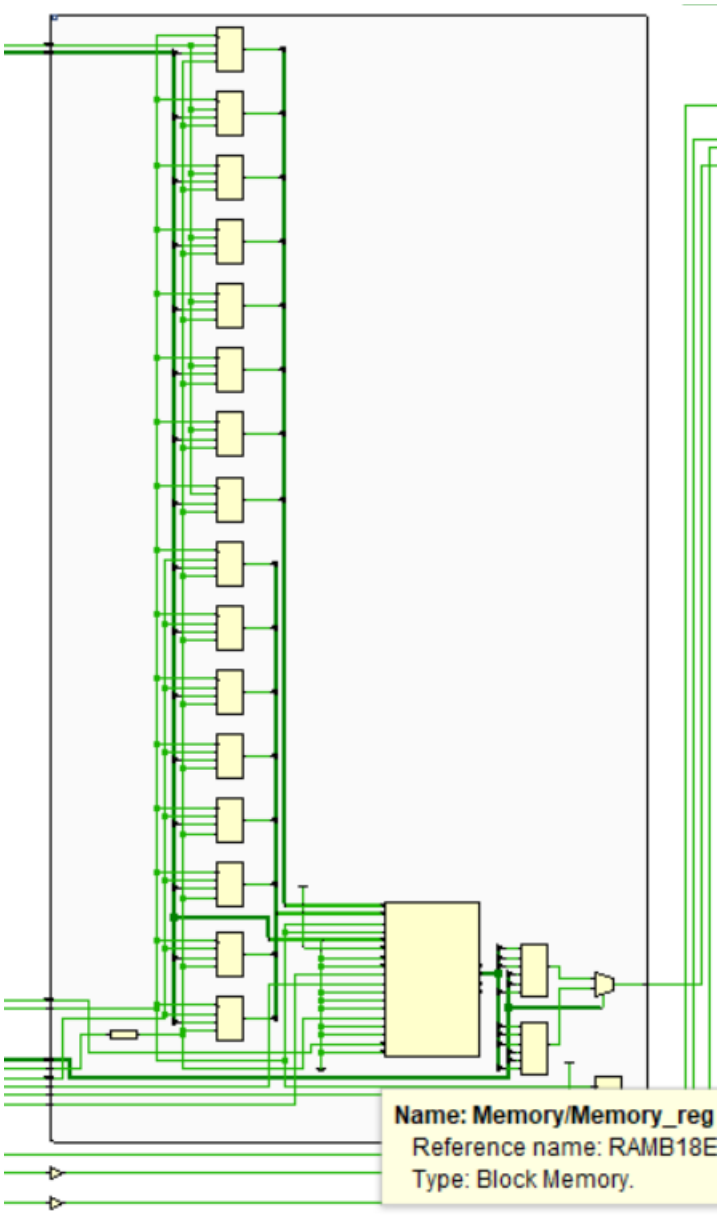


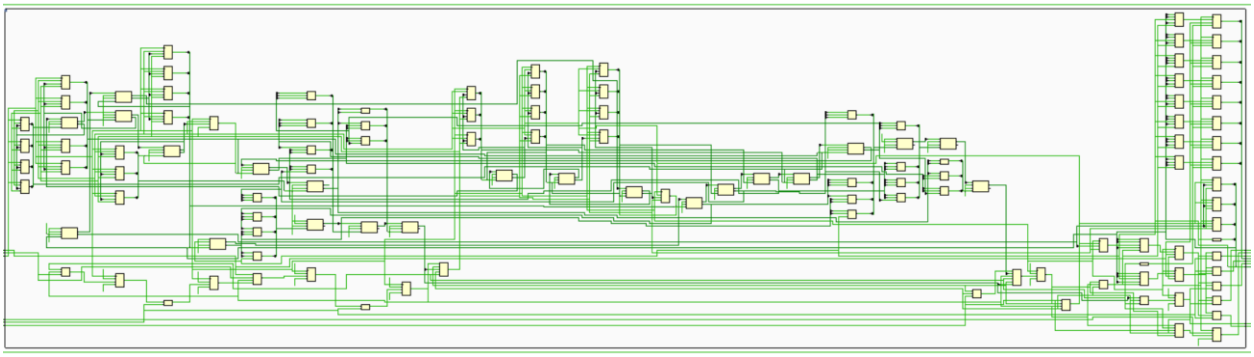




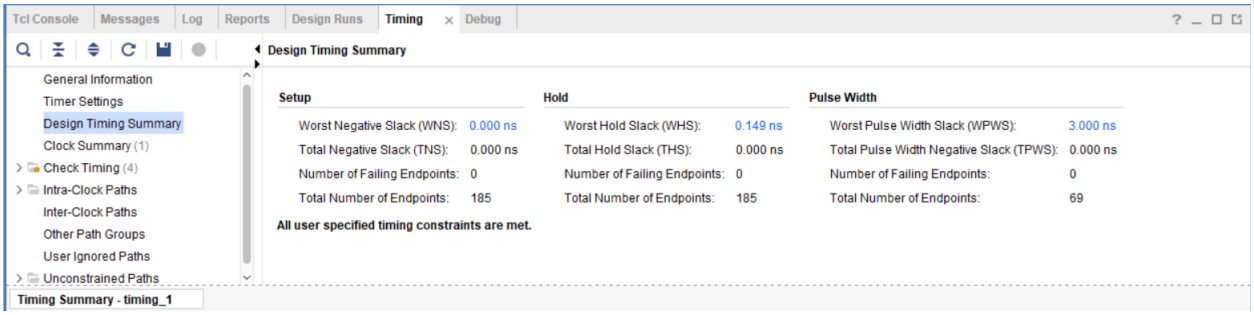
- Synthesis:(seq)



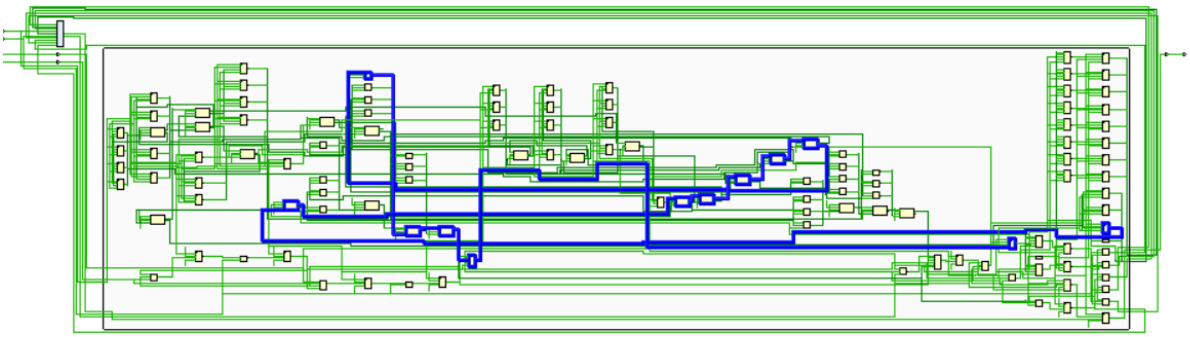

Name: Memory/Memory_reg
Reference name: RAMB18E
Type: Block Memory.



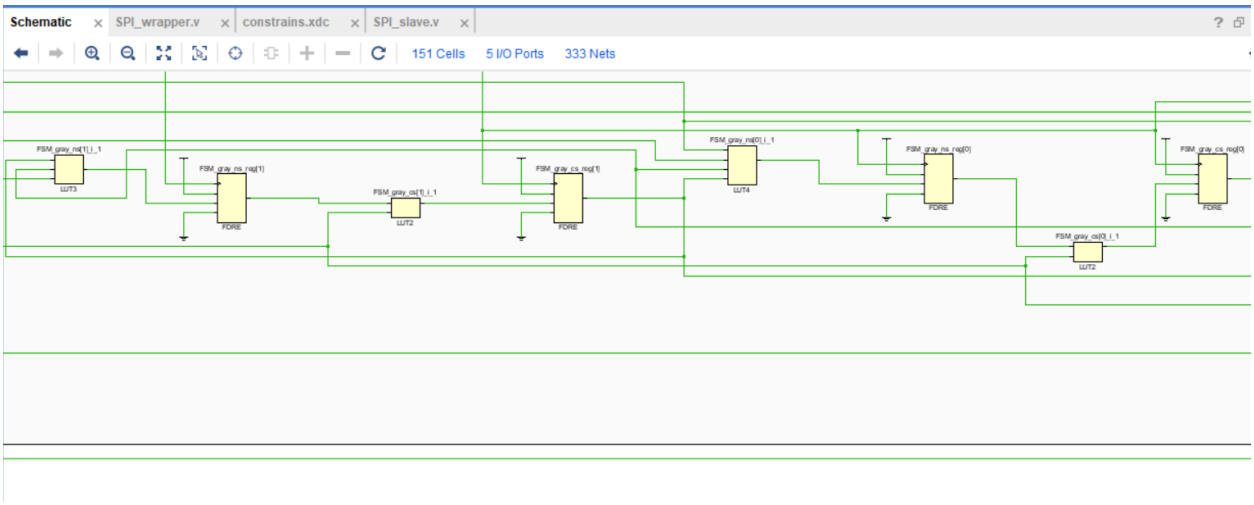
```
INFO: [Synth 8-5544] ROM "nsl" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
-----------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
-----------------------------------------------------------------------------------------------
                    IDLE |                               00 |                               00
                 CHK_CMD |                               01 |                               01
                    READ |                               10 |                               11
                   WRITE |                               11 |                               10
-----------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'
```



@142.86 MHZ

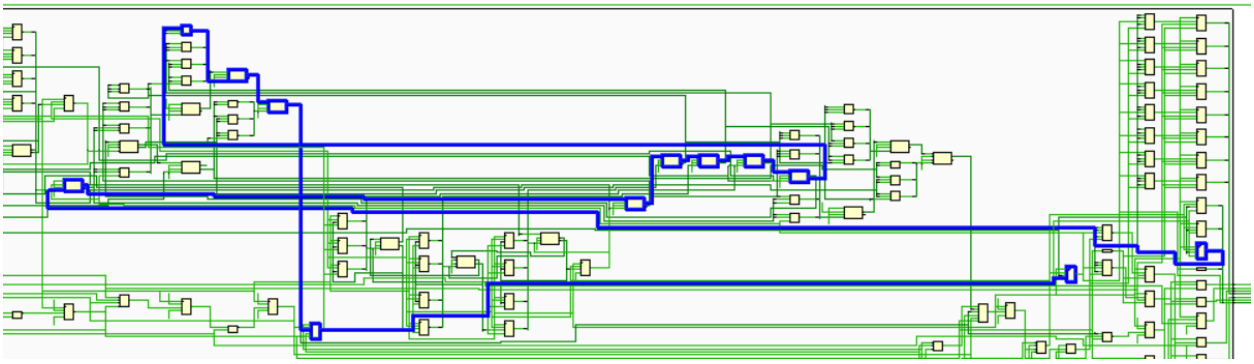


- Synthesis :(gray)

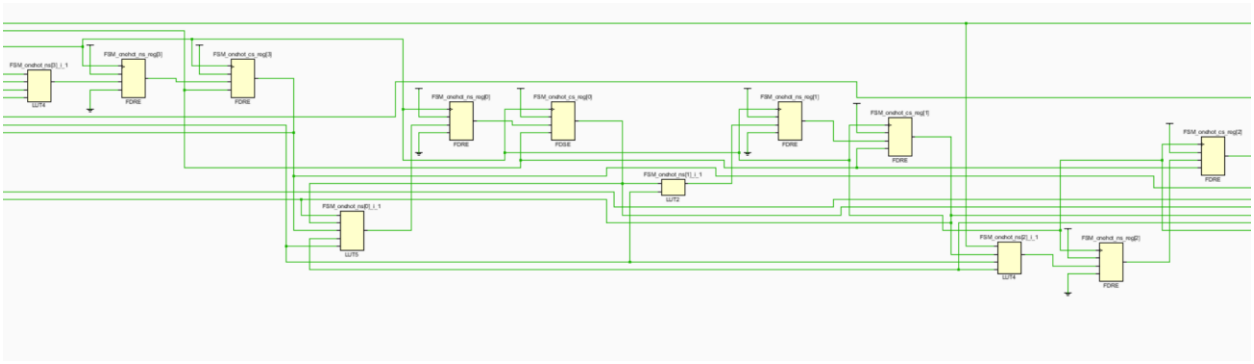


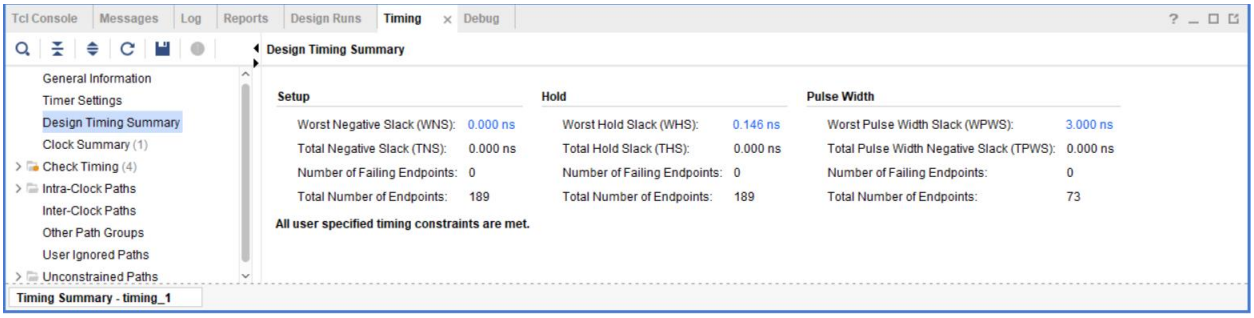
@142.86MHZ

State	New Encoding	Previous Encoding
IDLE	00	00
CHK_CMD	01	01
READ	11	11
WRITE	10	10



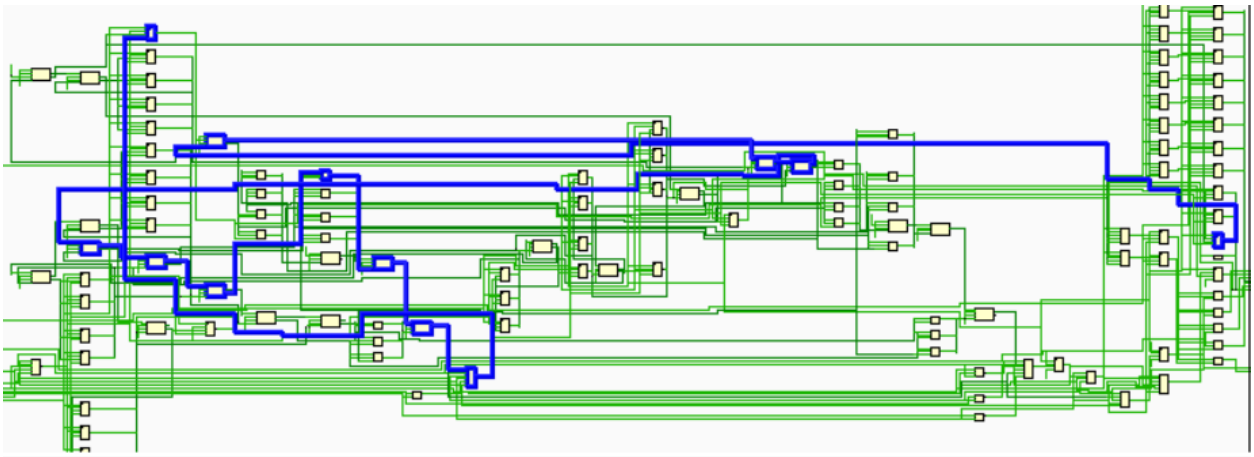
- Synthesis :(one_hot)





‘@142.86 MHZ

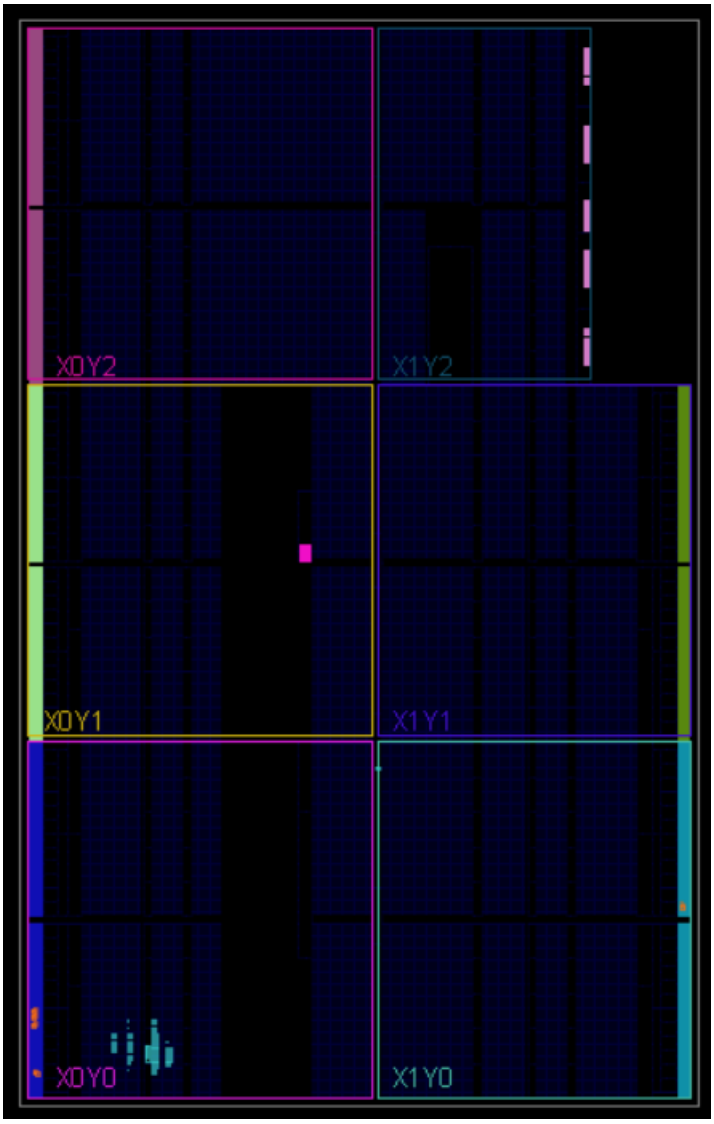
```
-------------------------------------------------------------------------------------------------
               State |                     New Encoding |                Previous Encoding
-------------------------------------------------------------------------------------------------
                IDLE |                             0001 |                              00
             CHK_CMD |                             0010 |                              01
                READ |                             0100 |                              11
               WRITE |                             1000 |                              10
-------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
```

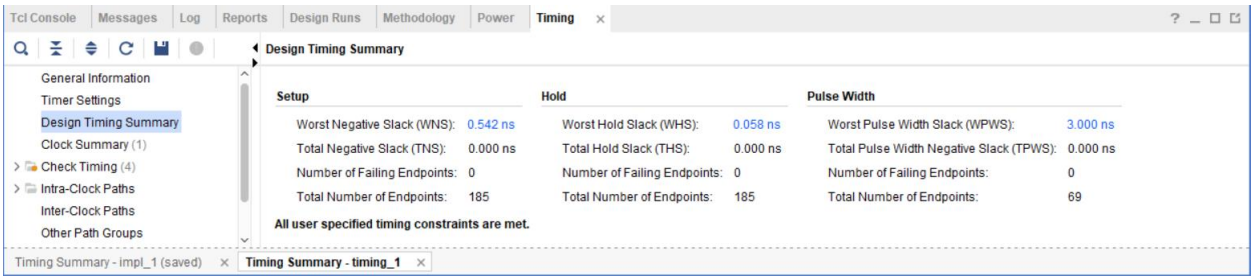


Implementation:

Since gray and seq had the same timing implementation is done with gray .

Schematic:





Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	51	66	1	37	51	8	0.5	5	1
Memory (RAM)	3	17	1	5	3	0	0.5	0	0
SPI (SPI_Slave)	48	49	0	36	48	7	0	0	0