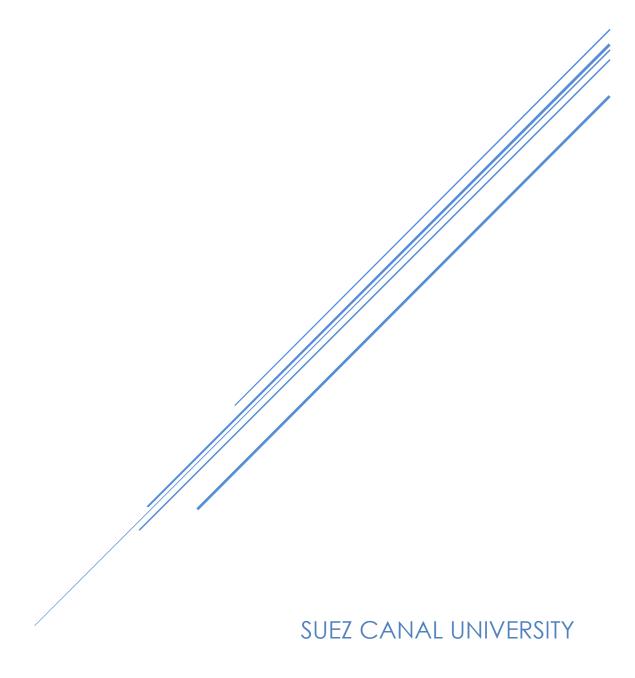
INTEGRATED CIRCUITS 1 LAB03



Yossef Ibrahim Abdel Aziz El Sayed Nada

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{V_A}{I_D} = \frac{2V_A}{V_{ov}}$$

 $|A_v| pprox g_m r_o = rac{2I_D}{V_{ov}} imes rac{V_A}{I_D} = rac{2V_A}{V_{ov}}$ Interestingly, the gain only depends on λ and V_{ov} . However, to derive this expression we used $g_m = 1$ $rac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $rac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^st) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

 $V^* = \frac{2I_D}{g_m} \leftrightarrow \ g_m = \frac{2I_D}{V^*}$ For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is

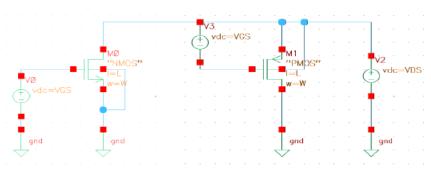
$$|A_v| \approx \frac{2V_A}{V^*}$$

The lower the V^* the higher the gain, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200 mV$.

₽ X′	We wa	nt to	design CS	and casc	ode amplifie	rs with the	parameters belo	ow.

Parameter	0.13um CMOS	0.18um CMOS
L^1	0.5μm	0.5μm
V*	200mV	200mV
Supply	1.2V	1.8V
Current consumption	20μΑ	20μΑ

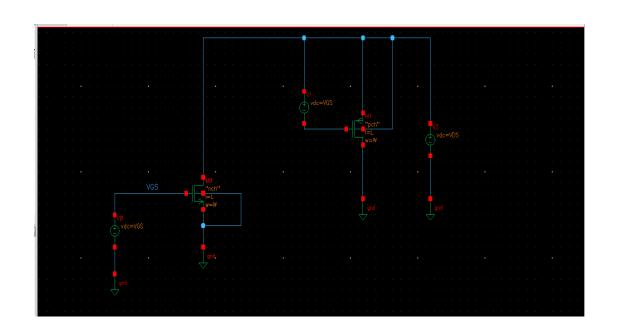
The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS transistor as shown below (we will use NMOS only in this lab). Use $W=10\mu m$ (we will understand why shortly) and $L=0.5\mu m$ (the same L selected before).



- Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
- We want to compare $V^*=2I_{\cal D}/g_m$ and $V_{ov}=V_{GS}-V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov} . You can save the expressions to reuse them later.
- Plot V^* and V_{av} overlaid vs VGS. Make sure the y-axis of both curves has the same range. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov} : velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
- An often used sweet-spot that provides good compromise between different trade-offs is $V^* =$ 200mV. On the V^* and V_{ov} chart locate the point at which $V^*=200mV$. Find the corresponding V_{ovQ} and V_{GSQ} .
- \checkmark 8) Plot I_D , g_m , and g_{ds} vs V_{GS} . Find their values at V_{GSQ} . Let's name these values I_{DX} , g_{mX} , and g_{dsX} . Now back to the assumption that we made that $W=10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ}=20\mu A$ as given in the specs. Calculate W as shown below.

W	I_D
10μm	I_{DX} @ V_Q^* (from the chart)
?	$I_{DQ}=20\mu A$ (from the specs)

10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is inversely proportional to $W(I_D)$ as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (crossmultiplication).



L = 0.5 Hm

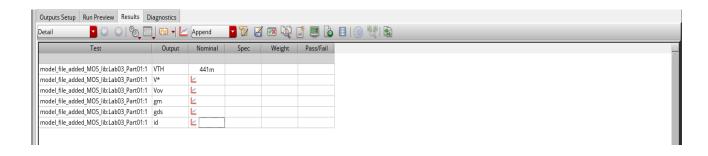
$$V^* = 200 \text{ mV}$$

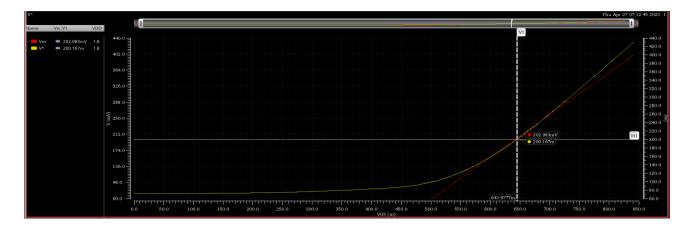
Supply = 1.8 U

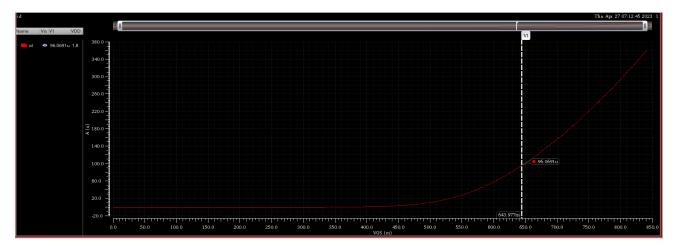
Cowart = 20 HA

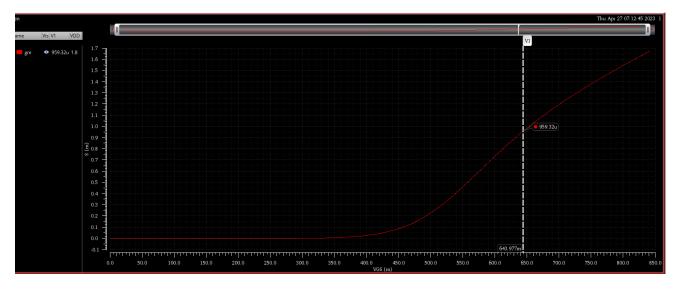
Comoump.

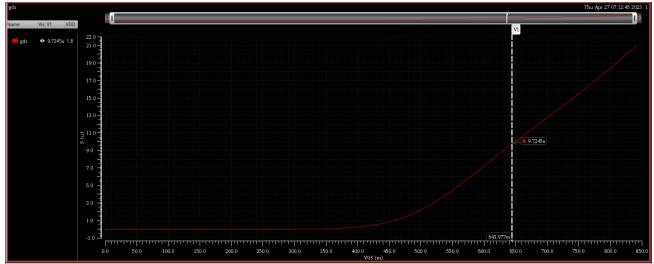
 $V_{1} = 4411 \text{ mV}$
 $V_{2} = 200 \text{ mV}$
 $V_{3} = 200 \text{ mV}$
 $V_{4} = 4411 \text{ mV}$
 $V_{5} = 200 \text{ mV}$
 $V_{6} = 643.977 \text{ mV}$
 $V_{6} = 643.$











$9_{ds} = \frac{I_D}{V_A} - I_D \Delta$	/
So at L Const.	
9dg × ID	
$\frac{9ds_1}{s} = \frac{w_1}{w_2}$	
9.7545 _ to 9ds_ = 2.0244 HS 8ds_2 2.0818	
	9
pavametes	2
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4
IDQ 20 MA	
9mQ 199.7 MS	=
946 2.0244 Hs	
ro 493,97 KS2	_
W 2,0818 Hm	
L 0,5 Hm	•
Supply Volt 1.8 v	•
200 mV	
Vava 202.983 mv	
VGSQ 643.977 mv	_

PART 2: Cascode for Gain

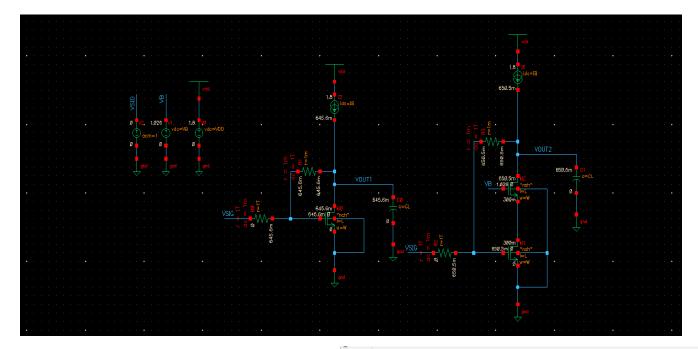
OP Analysis

- Create a new cell and schematic. Construct the circuit shown below. Use I_B = 20μA, L = 0.5μm, W as selected in Part 1, and C_L = 1pF.
- 2) Choose V_B (the cascode device bias voltage) such that M2 has $V_{DS} \approx V^* + 100 mV$ (you may sweep VB and plot VDS vs VB to help you choose a good value for VB).
- 3) We need to bias transistors in saturation; however, the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal_resistor). The input transistor is diode connected for DC simulation (always in saturation), while in AC simulation the feedback is disconnected, and the AC input source is connected. Set the feedback resistance 1mΩ DC and 1TΩ AC and set the source resistance oppositely. We will study how to do biasing practically later in this course inshaAllah.
- Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly annotated.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

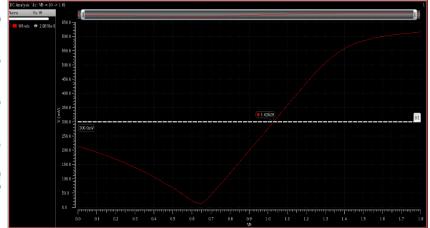
"vdsat" is the minimum drain-source voltage required to bias the transistor in saturation. It is equal to V_{ov} for a square-law device. It is also referred to as "vdss" (drain-source saturation voltage).

- Check that all transistors operate in saturation.
- 6) Do all transistors have the same vth? Why?
- 7), What is the relation $(\ll, <, =, >, \gg)$ between gm and gds?
- What is the relation $(\ll, <, =, >, \gg)$ between gm and gmb?
- What is the relation $(\ll, <, =, >, \gg)$ between cgs and cgd?
- $(\ll, <, =, >, \gg)$ between csb and cdb?

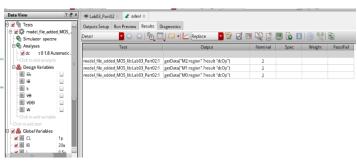


 $V_{DS} \simeq V^* + 100 \text{ mw} \simeq 300 \text{ mw}$ White ~ 2.08160 M1

From The graph $VB \simeq 1.02629$ v



5) all transistors operate in Sad as they all have the region 2



Snap shots required in Question 4:

	1
w	2.082E-6
M0:id	20.00E-6
M0:vgs (V)	645.6E-3
M0:vds (V)	645.6E-3
M0:vth (V)	442.1E-3
M0:vdsat (V)	155.1E-3
M0:vdss (V)	155.1E-3
M0:gm	199.7E-6
M0:gds	2.253E-6
M0:gmb	53.96E-6
M0:cdb	-1.748E-15
M0:cgd	-983.0E-18
M0:cgs	-7.497E-15
M0:csb	-3.743E-15
M0:region	2

	1
w	2.082E-6
M1:id	20.00E-6
M1:vgs (V)	650.5E-3
M1:vds (V)	300.0E-3
M1:vth (V)	444.7E-3
M1:vdsat (V)	156.7E-3
M1:vdss (V)	156.7E-3
M1:gm	196.3E-6
M1:gds	4.440E-6
M1:gmb	53.09E-6
M1:cdb	-1.910E-15
M1:cgd	-1.011E-15
M1:cgs	-7.508E-15
M1:csb	-3.735E-15
M1:region	2

·	
	1
W	2.082E-6
M2:id	20.00E-6
M2:vgs (V)	726.3E-3
M2:vds (V)	350.5E-3
M2:vth (V)	530.5E-3
M2:vdsat (V)	160.2E-3
M2:vdss (V)	160.2E-3
M2:gm	199.8E-6
M2:gds	3.608E-6
M2:gmb	48.50E-6
M2:cdb	-1.759E-15
M2:cgd	-997.6E-18
M2:cgs	-7.444E-15
M2:csb	-3.327E-15
M2:region	2

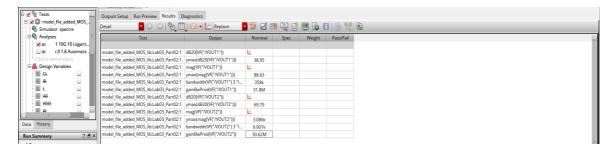
	Ch to	
6)	Uth = VGS-Vdsat	u,L
	These values differ to	on
	one transistor to the other	
as	we can see the first two transistors are	
	e to each other in 1th as their body effe	
Con	be regreted by the third one has body.	effect
as	the body is not connected to the Source	6 M2
7)	In >> gds from 50 to 100 times	
(8)	8m > 9mb 3-4 times	
9)	gs > gd 3-5 time,	14
10)	96 > 96 3-5 times	
	This Think	
	the state of the s	

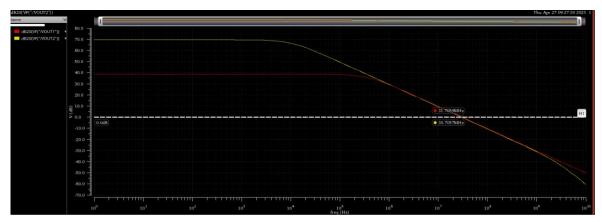
2. AC Analysis

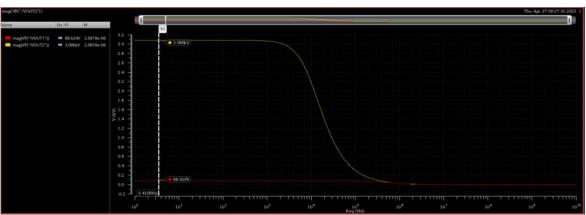
- Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
- Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.
 - Cadence Hint: Use the following expressions in the calculator, and send them to adexl to quickly calculate circuit parameters.

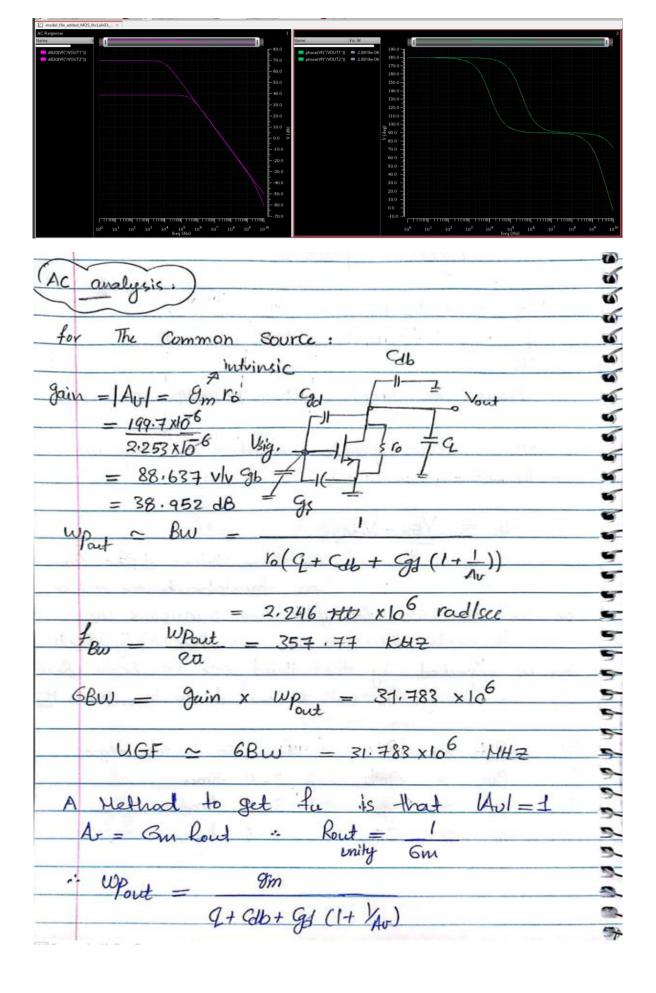
Туре	Expression/Signal/File	EvalType	Plot
e×pr	dB20(VF("/vout1"))	point	✓
expr	ymax(dB20(VF("/vout1")))	point	✓
expr	ymax(mag(VF("/vout1")))	point	V
expr	bandwidth(VF("/vout1") 3 "low")	point	✓
expr	gainBwProd(VF("/vout1"))	point	✓
expr	dB20(VF("/vout2"))	point	<u>~</u>
e×pr	ymax(dB20(VF("/vout2")))	point	✓
expr	ymax(mag(VF("/vout2")))	point	✓
expr	bandwidth(VF("/voutZ") 3 "low")	point	V
expr	gainBwProd(YF("/vout2"))	point	<u>~</u>

- Report the Bode plot (magnitude) of CS and cascode appended on the same plot.
- 4) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
- Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.
- 6) Comment on the results.









Don't forget the body effect	
For The Cascode Gd2 Vout	30
Raut = $r_0 + r_{02} + 9m_2r_0 r_{02}$	19
$Raut = ro_1 + ro_2 + 9m_2ro_1ro_2$ $Sm = \frac{iasc}{Vsig} \simeq -9m_1 Vsig$ $Sig = \frac{iasc}{Vsig} \simeq -9m_1 Vsig$	50
AGE = 10,002 MSL , (293) I	18T
" Sain = - 9my (ro, + roz + 9mz ro, roz) = - 3086.7 VIV	Age I
dB => 69.789 dB	
3c - (dm2 + raz (-15cto	
· BW C WPOLL =	vsig)
$isc (1 + 9m_2 ro_1 + \frac{ro_1}{ro_2}) =$	
Rout [9+ 8b2+ gg2] reglected - gm, ro, (9m	$\frac{1}{2} + \frac{1}{ro_2}$
- 0.0 11137 VSI	9.
-2/201316 Ide 13	
fow = 9.923 Kelz 1+9102 ro1+	Y02
$= -1.9989 \times 10.8$	
6BW = 30,629 H	
fu = 6BW = 30.629 HUZ	
FE Spanned with Cameranney	

	dimu.	hand	Simu.	hand.
De gain	38,95 JB	38.95 dB	69.79 dB	69,78936
Bw			9,901K	
UGF	31. 705 NH2	31.783 H	30.705 H	30.62 M
6BW	31.8 HHz	31.783 H	30,62 M	30 · 62 H

My comment on the previous data:

- The addition of The Cascode increased
The output resistance to a high Value Thus
it increased the gain but at the same
lowered The dominant pde Thus lowered
With Cascode gain & But swing &
O O
an in the
to get fu: $ Au = Gm Rout = 1$ if Rout = 1 Onity = Gm
: Rout 1
onity Gm
$\therefore f_{u} = 1 \times 6m$
$\frac{1}{2a} = \frac{1}{2a} \times \frac{6m}{q + Qb_2 + Qd_2}$
Ju Common Source Gain x BW = 9m, Pout x 1 2 9m1 Cout Cout
Put Cout
GRW - 9m Part x 1 ~ 9m
GBW = 9m Pout × 1 ~ 9m Pout Cout Cout
Cas code doesn't change The GBW much
because the output pole is dornard for
som topologies and thus if The gain me. og
a factor K with The Cascode the gain will
deerease by the same factor thus 6BW
would be constant
6BW is independent of The owlput
impedance
Caseading might change the GBCW if the
dominant pole Changed from the output to the
dominant pole changed from the output to the input but this diff didnot happen here.
-03

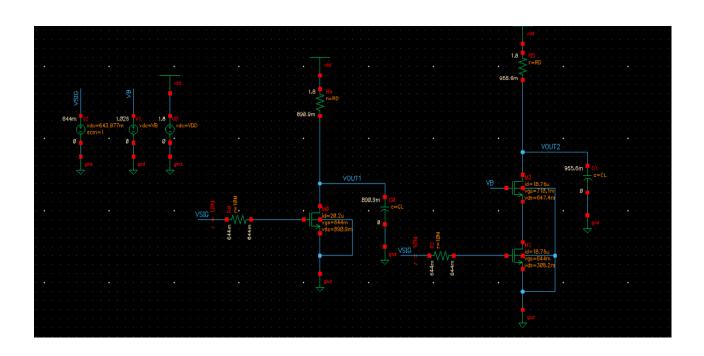
PART 3 [Optional]: Cascode for BW

1. OP Analysis

- 1) Create a new cell and schematic. Copy the old schematic instances to the new one. Make the following modifications: remove the feedback resistance, set $\mathcal{C}_L=1fF$, replace the current source with a resistor RD, make the signal source resistance = $10M\Omega$ (remove the AC value). Set VGS of the input device as calculated in Part 1.
 - 2) Calculate R_D analytically such that the voltage drop on it is $\approx V_{DD}/2$ (the current remains roughly the same as in Part 2 because we are using the same VGS).
 - 3) Note that the DC voltage of the output node is set by the resistance (R_D) ; thus, we don't need a feedback loop as in the previous case.
 - 4) Simulate the DC OP point of the new CS and cascode amplifiers. Add monitors and report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

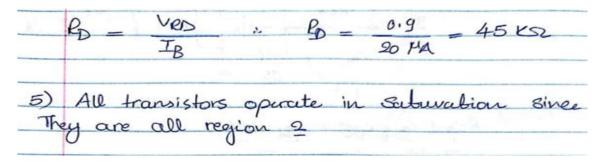
5 Check that all transistors operate in saturation.



	1
W	2.082E-6
M0:id	20.20E-6
M0:vgs (V)	644.0E-3
M0:vds (V)	890.9E-3
M0:vth (V)	440.3E-3
M0:vdsat (V)	155.3E-3
M0:gm	201.3E-6
M0:gds	2.083E-6
M0:gmb	54.34E-6
M0:cdb	-1.672E-15
M0:cgd	-981.6E-18
M0:cgs	-7.494E-15
M0:csb	-3.744E-15
M0:region	2

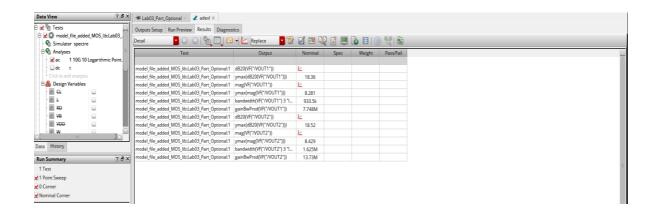
	1
w	2.082E-6
M1:id	18.76E-6
M1:vgs (V)	644.0E-3
M1:vds (V)	308.2E-3
M1:vth (V)	444.6E-3
M1:vdsat (V)	152.4E-3
M1:gm	190.6E-6
M1:gds	3.942E-6
M1:gmb	51.61E-6
M1:cdb	-1.903E-15
M1:cgd	-1.007E-15
M1:cgs	-7.502E-15
M1:csb	-3.735E-15
M1:region	2

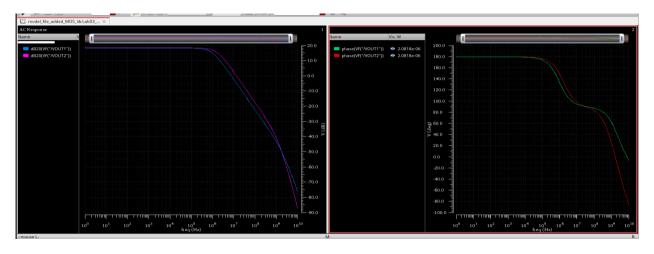
	1
W	2.082E-6
M2:id	18.76E-6
M2:vgs (V)	718.1E-3
M2:vds (V)	647.4E-3
M2:vth (V)	530.5E-3
M2:vdsat (V)	154.8E-3
M2:gm	195.9E-6
M2:gds	2.220E-6
M2:gmb	47.45E-6
M2:cdb	-1.657E-15
M2:cgd	-982.0E-18
M2:cgs	-7.427E-15
M2:csb	-3.321E-15
M2:region	2

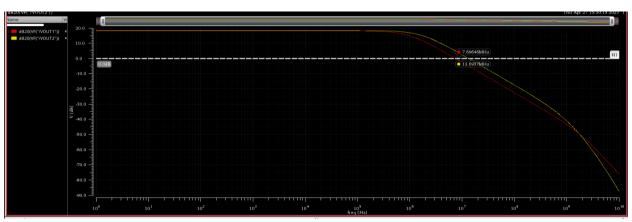


2. AC Analysis

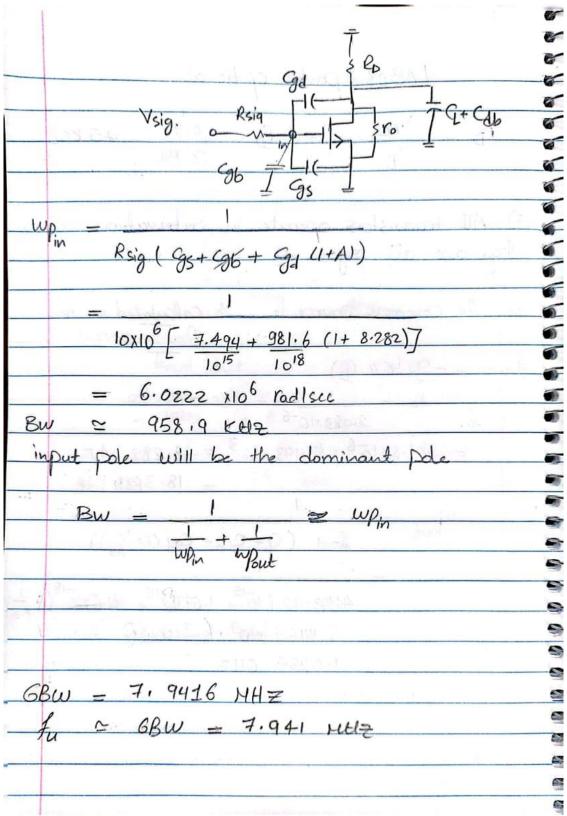
- 1/2 Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
- 2) Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.
- 3) Report the Bode plot (magnitude) of CS and cascode appended on the same plot.
- Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
- 5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. Comment on the results.







for	The Common Source: As calculated in the
	Previous part
gair	2 = - gm(ro// Rp)
	ro = 1 = 480.076 KS
	2.083×10-6
	$= 201.3 \times 10^{-6} \times 41.143 \times 10^{3} = -8.282 \text{ VIV}$
	= 18,3628 dB
1	Went = 1
	but Rout (G+ Gb+ Gg (1+ /4))
	- delet
	4143.42 (10+ 1.67 x10+ 981.6 x10 (1+ 1
	= 6.4467 x109 rad/see
	= 1.0265 GHZ
1.	



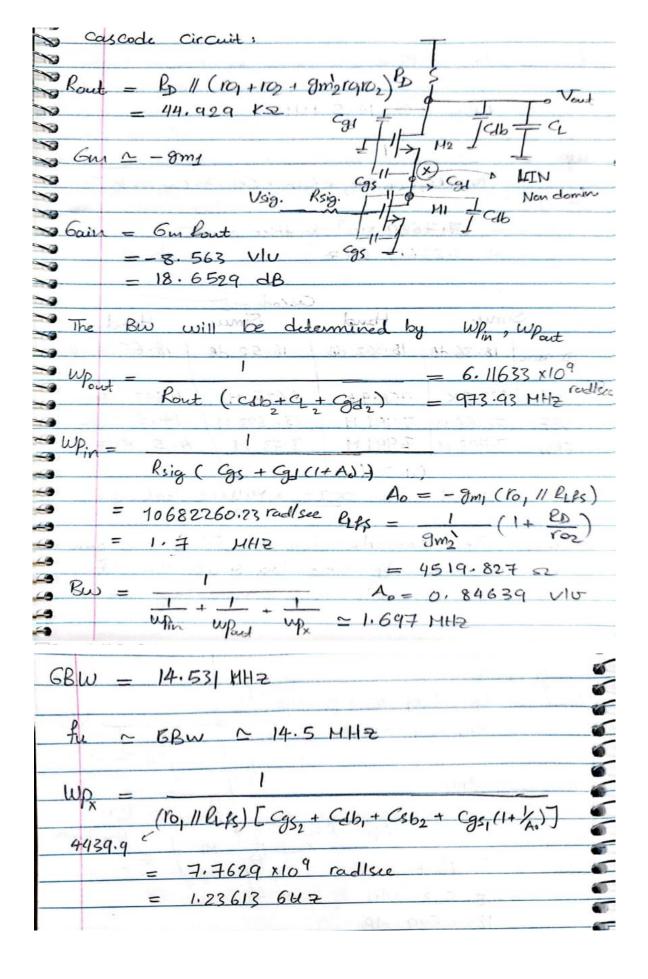


Table and comment:

				Cas Code 1	7
	5	Simu	Hond	Simu-	Hand
	to gain	18.36 AB	0	18.52 dg	The same of the sa
CŞ	BW	933.5 K	958.9 K	1.625 H	1.697 HHZ
	UGF	7.696 M	7.941 M	13. 693 M	14,5 KHZ
	6BW	7.748 M	7.941 M	13.73 M	4.5 HHZ
qo nu pn	Ding web	The observations	Cascali de la ma	diduot char is too small	-technique uge the gein I that it using the to it thus the
Ja	ur dic	mo i Ci	age.		
1	e inf	out pole	and ac	lding the co	et pole is ascode dures thus caused
bar	This	h exten	the gain	. bardwidth	