INTEGRATED CIRCUITS 1
LAB02

SUEZ CANAL UNIVERSITY

Yossef Ibrahim Abdel Aziz El Sayed Nada

PART 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (V_{GS}), and the resistive load (R_D).

Spec	0.13um CMOS	0.18um CMOS
DC Gain	-5	-8
Supply	$1.2V$	$1.8V$
Current consumption	$100\mu A$	$100\mu A$

2) The first design decision is to choose L. Since there is no spec on bandwidth (speed), we may choose a relatively long L to provide large r_o and avoid short channel effects. Note that r_o appears in parallel with R_D. Assume we will choose $L = 2\mu m$.
3) We can show that the gain is given by

$$|A_v| \approx g_m R_D = \frac{2I_D}{V_{ov}} \times R_D = \frac{2V_{R_D}}{V_{ov}}$$

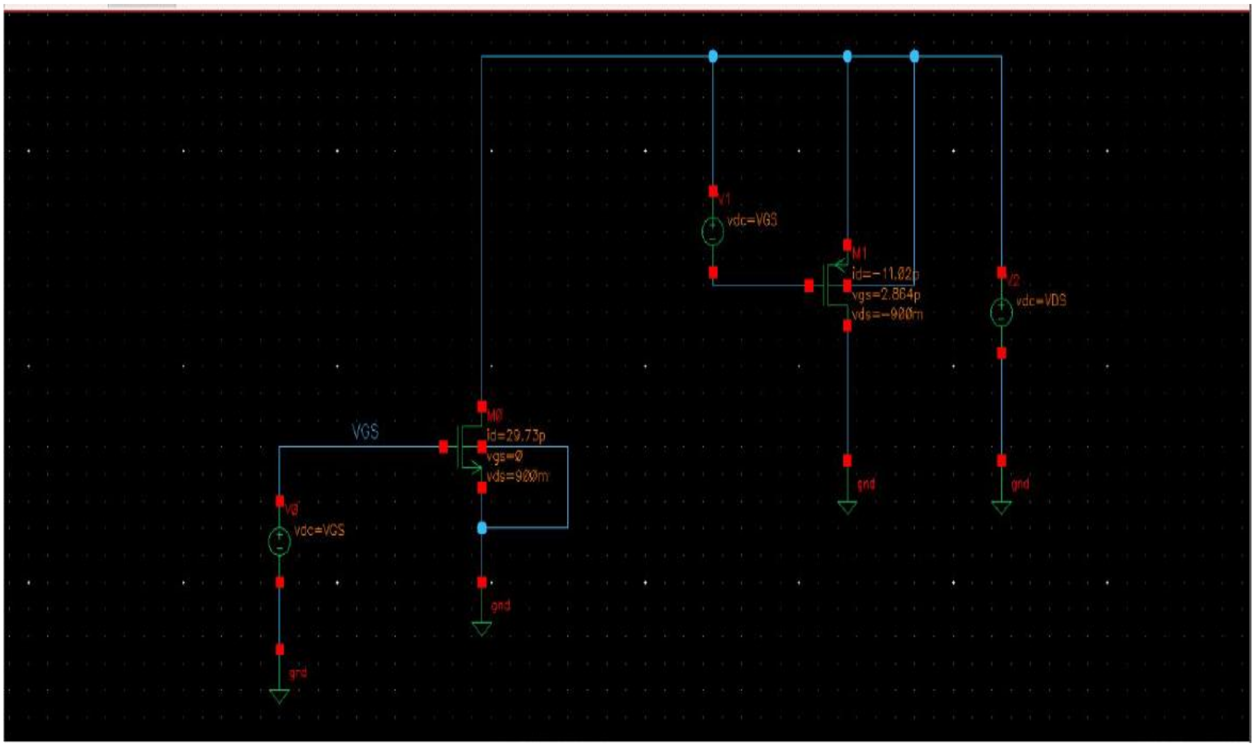
Interestingly, the gain only depends on the voltage drop across V_{R_D} and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2V_{R_D}}{V^*}$$

4) The choice of V_{R_D} is constrained by the output signal swing. Since we usually want to provide large output swing, we choose the common-mode (CM) output level (DC output level) around $V_{DD}/2$. Thus, although increasing V_{R_D} increases the gain, but the choice is limited by the supply voltage which is aggressively scaled down in modern technologies. That's one reason it is difficult to get high gain in modern technologies. Assuming CM output = $V_{R_D} = V_{DD}/2$ and given the DC bias current, determine the value of R_D. Again, it is interesting to note that although the gain equals $g_m R_D$, it actually does not depend on R_D itself, but on the voltage drop across it, i.e., the product $I_D \times R_D$.
5) Given A_v and V_{R_D}, calculate the required V^* (again note that $V^* \neq V_{ov}$ for a real MOSFET). Let's name this value V_Q^*.
6) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS and PMOS characterization (we will use the PMOS later in Part 2 of this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 2\mu m$ (the same L that we chose before).



large L → Large r_o ; → avoid short channel effect } He didnot specify Band width limit choose L freely

$$V^* = \frac{2 I_D}{g_m} \qquad A_v \simeq \frac{2 V_{RD}}{V^*}$$

from The Simulation we found That :

V_{th} = 383.8 ~~nm~~ mV

⇒ Don't forget to add the save.txt to save parameters to DC tab.

The file ee214b.sp shows That we are using 180 nm technology.

Specs 0.18 μm CMOS

DC gain ⟶ −8 V/V

Supply ⟶ 1.8 V

Current Consumption ⟶ 100 μA

$A_v = -8 \;, \quad I_D = 100\ \mu A$

to get The Value of R_D :

$$R_D = \frac{V_{RD}}{I_D} \quad \because V_{RD} = \frac{V_{DD}}{2} = \frac{1.8}{2} = 0.9\,V$$

$$R_D = \frac{0.9}{100 \times 10^{-6}} = \underline{\underline{9\,K\Omega}}$$

given: $|A_v| \simeq \frac{2V_{RD}}{V^*}$, $g_m = \frac{2I_D}{V^*}$

$$V^* = V_{ov}^* = \frac{2V_{RD}}{|A_v|} = \frac{2 \times 0.9}{8} = 0.225\,V$$

↓

for a real mosfet

$V^* \neq V_{ov}$

→ We cannot Calculate The Sizing from the Square law model because it's not accurate so we will use a sizing chart.

↳ from Simulation

assume $W = 10\ \mu m$, $L = 2\ \mu m$

First: $V_{th} = 382.6\ mV$

Test	Output	Nominal
model_file_added_MOS_lib:Lab02_Part01:1	VTH	383.8m

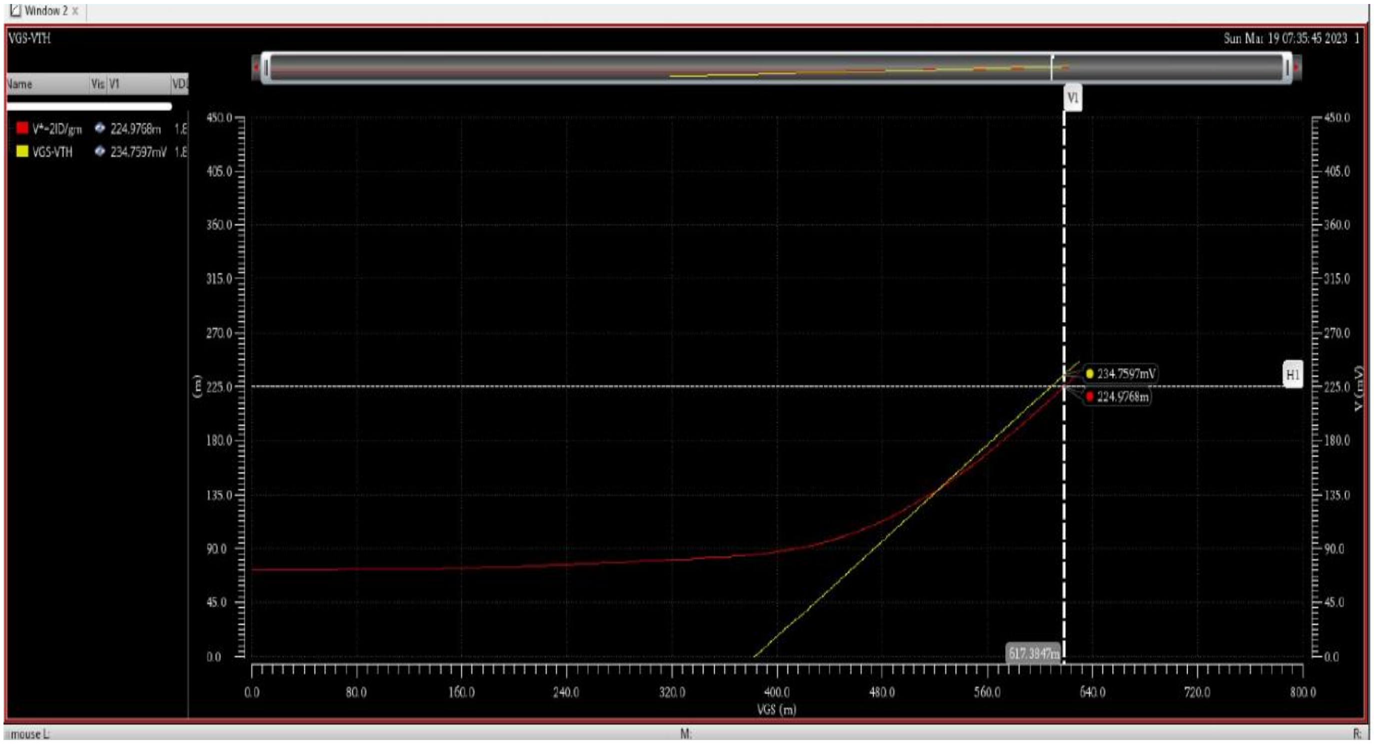
Test	Name	Type	Details	EvalType	Plot
mod...	VTH	expr	pv("M0" "vth" ?result ...	point	✓
mod...	V*-2ID...	expr	((2 * getData("M0:id"...	point	✓
mod...	VGS-VTH	expr	(v("M0:vgs" ?result "...	point	✓

7) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.

8) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. Export the expressions to adexl.

9) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law (although we are using $L = 2\mu m$).

10) On the V^* and V_{ov} chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{ovQ} and V_{GSQ}.



From the plot of V^* and V_{ov} we find that

→ At The begining of The inversion region V^* and V_{ov} are indeed close to each other but in Threshold and subthreshold they are far from each other

10) at $V_Q^* = 0.225\ v$ ⇒ at $V^* = V_Q^*$
Locate on Y-axis

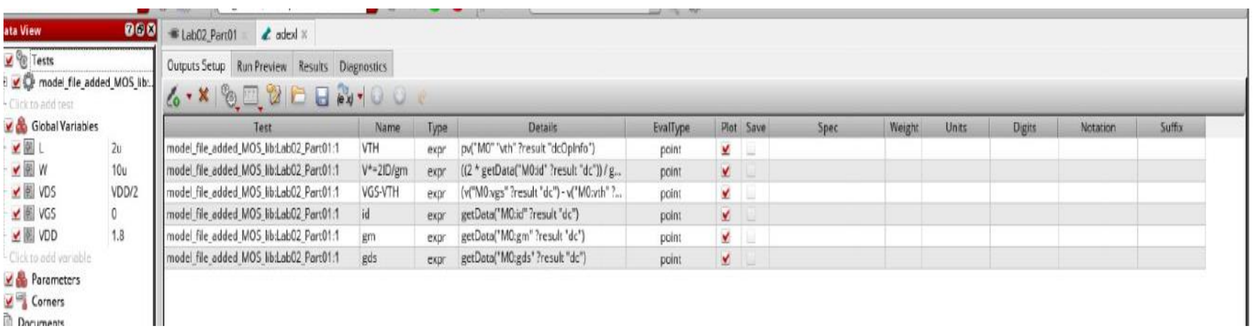
$V_Q^* \longrightarrow 0.225\ v$
$V_{ovQ} \longrightarrow 234.759\ mv$
They are not The Same
$V_{GSQ} \longrightarrow 617.3847\ mv$

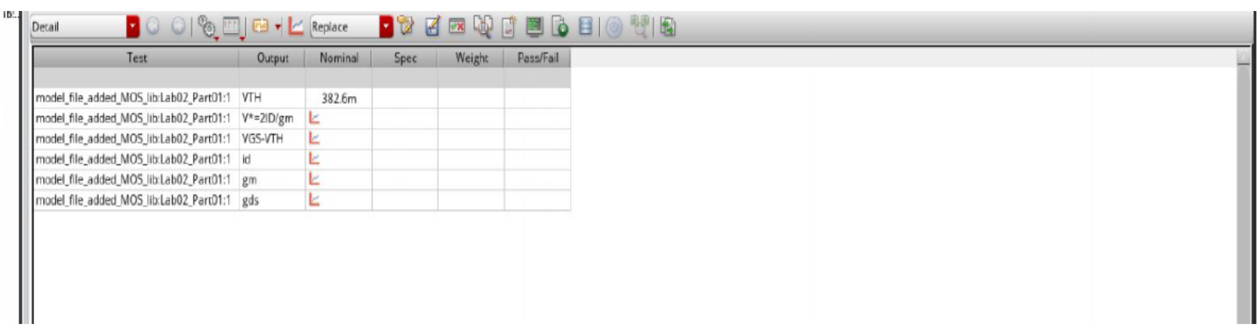
11) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.

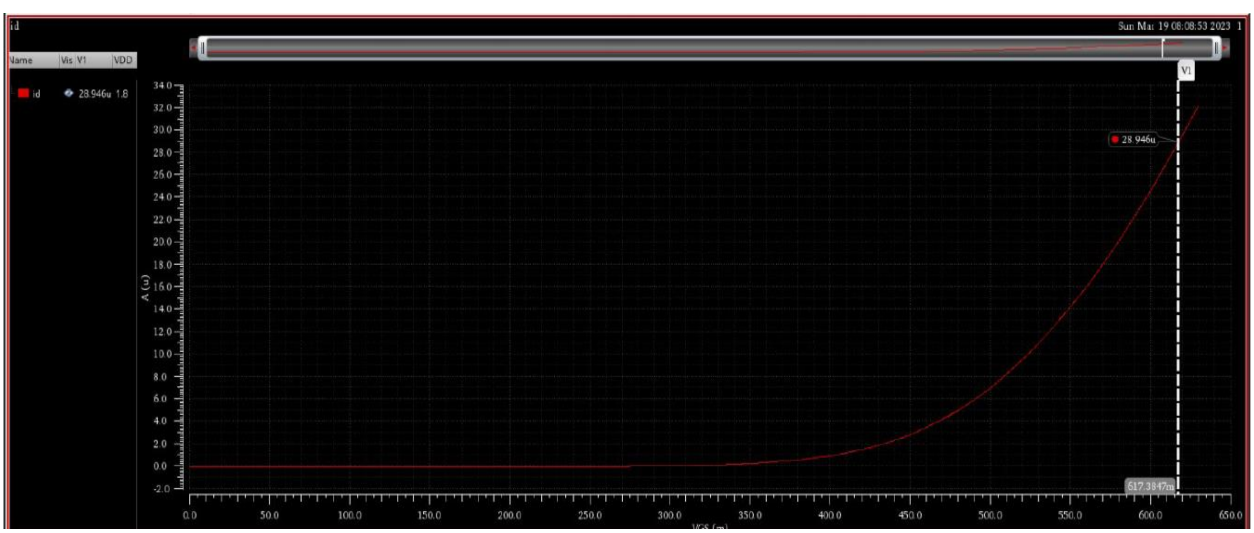
12) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 100\mu A$ as given in the specs. Calculate W as shown below.

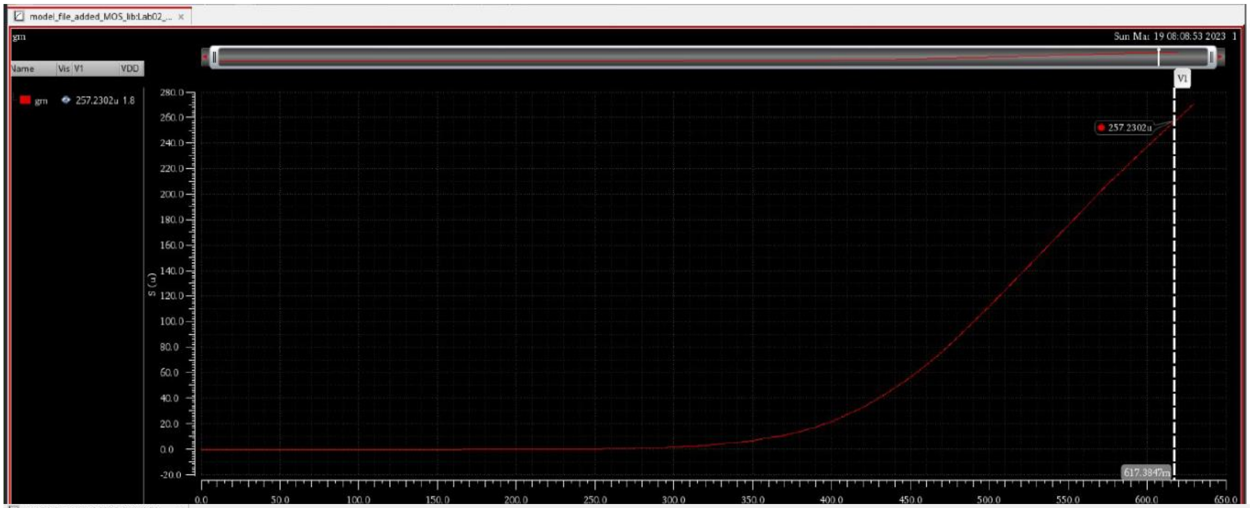
W	I_D
$10\mu m$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 100\mu A$ (from the specs)

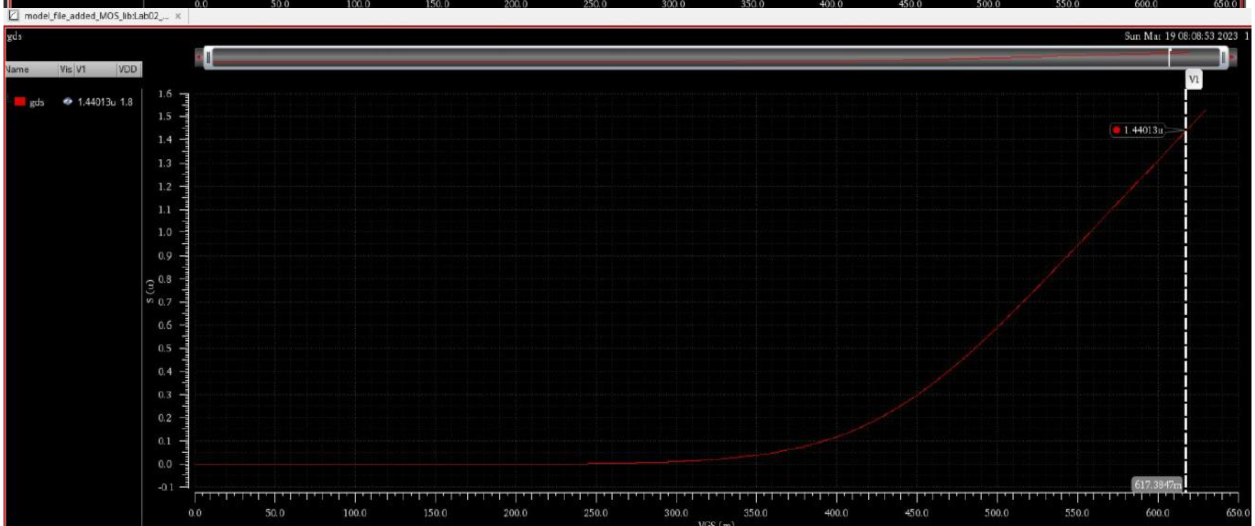
13) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication) and double check that $A_v = -g_m(R_D||r_o)$ meet the required gain spec.











11) Plot g_m, I_D, g_{ds}

at V_{GSQ} : $\Rightarrow$ 617.3847 mV

I_{DX} = 28.946 μA

g_{mX} = 257.2302 μS

$g_{ds}X$ = 1.44013 μS

12)

W	I_D
10 μm	28.946 μA
34.547 μm	100 μA

I_D is proportional to W regardless of The model used.

Calculating The remaining parameters

→ g_m is proportional to W when V_{ov} is constant

$$\therefore \; g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

→ r_o is inversly proportional to W (I_D) as long as L is Const.

$$\therefore \; r_o = \frac{1}{\lambda I_{DS}} \quad \text{and} \quad \lambda \propto \frac{1}{L}$$

$$\frac{g_m}{g_{mQ}} = \frac{W}{W_Q} \quad \therefore \frac{g_m}{257.2302} = \frac{34.547}{10}$$

$$\therefore g_m = 888.65317 \; \mu S$$

$$\frac{g_{ds}}{g_{dsQ}} = \frac{W}{W_Q} \quad \therefore \frac{g_{ds}}{1.44013} = \frac{\cancel{10}\; 34.547}{\cancel{34.547}\; 10}$$

Carefull !! r_o is inversly proportional to W but g_{ds} is directly prop.

$$g_{ds} = \frac{g_{dsQ} \times W}{W_Q} = \frac{1.44013 \times 34.547}{10} = 4.9752 \; \mu S$$

$\therefore$

$I_D = 100 \; \mu A$

$g_{ds} = 4.9752 \; \mu S$

$g_m = 888.65317 \; \mu S$

to get The gain, $A_v = -g_m (R_D \,//\, r_o)$

$$r_o = \frac{1}{g_{ds}} = 200.9962 \; k\Omega$$

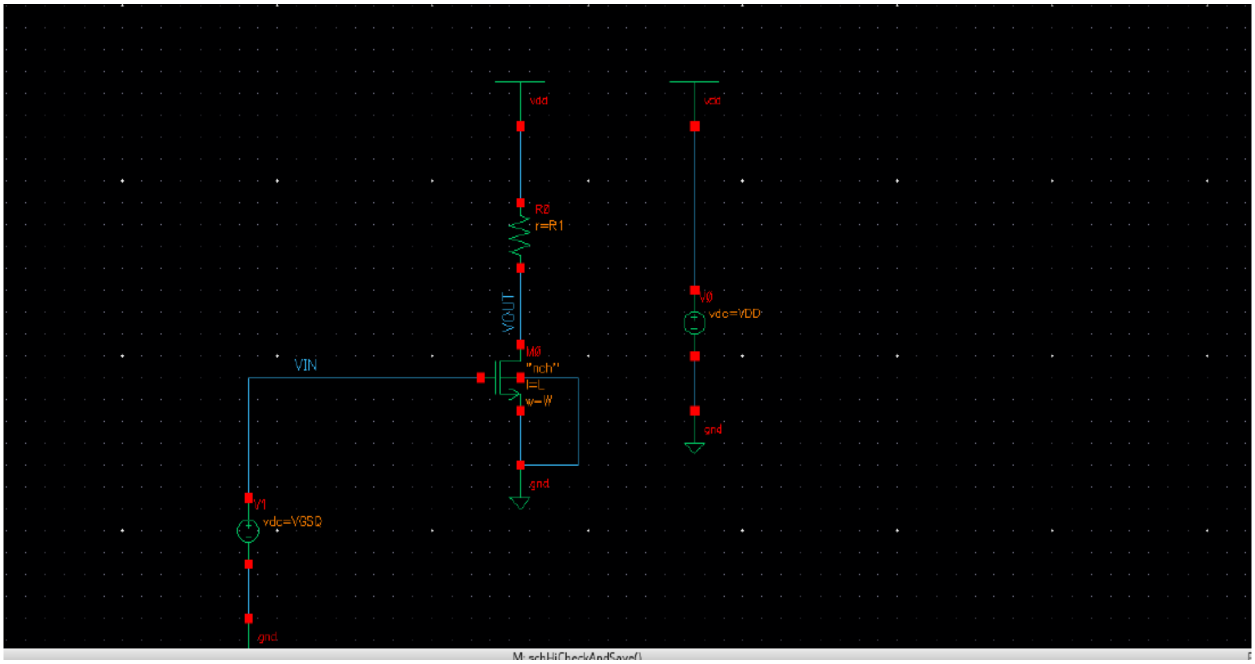
$$\therefore \; A_v = -888.65317 \, (9\,k\Omega \,//\, 200.9962\,k\Omega) \times 10^{-6}$$

$$\boxed{A_v = -7.655 \; V/V}$$

∴ Then parameters and Their Values,

Parameters	I_{DQ}	g_{mQ}	g_{dsQ}	L	W	R_D
Values	100 μA	888.653 μS	4.7452 μS	2um	34.547 um	9 kΩ

PART 2: CS Amplifier



1. OP and AC Analysis

1) Create a testbench for the resistive loaded CS amplifier using the $V_{GSQ}, R_D, L,$ and W that you got from the previous part.
2) Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used chart-based design, the results should agree well.
   - ➔ Cadence Hint: The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).
3) Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?
4) Calculate the intrinsic gain of the transistor.
5) Calculate the amplifier gain analytically. What is the relation $(\ll, <, \approx, >, \gg)$ between the amplifier gain and the intrinsic gain?
6) Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec.

→ problem encountered when named The line VDD and The terminal V_{dd}, They gotta be The same

DC op parameters

W	34.55E-6
M0:region	2
M0:id	100.3E-6
M0:gm	892.1E-6
M0:gds	4.993E-6
M0:vgs (V)	617.4E-3
M0:vth (V)	382.7E-3

from part (1)	In part (2)
$I_D = 100\ \mu A$	$I_D = 100.3\ \mu A$
$g_m = 888.653\ \mu s$	$g_m = 892.1\ \mu s$
$g_{ds} = 4.794\ \mu s$	$g_{ds} = 4.993\ \mu s$
$V_{GS} = 617.384\ mv$	$V_{GS} = 617.4\ mv$
$V_{Th} = 382.6\ mv$	$V_{Th} = 382.7\ mv$
$r_o = 200.9962\ K\Omega$	$r_o = 200.28\ K\Omega$
$V_{ov} = 234.759\ mV$	$V_{ov} = 234.7\ mv$

↓

This is in Region 2 which is Saturation

3) $r_o = 200.28\,K\Omega \ggg R_D = 9\,K\Omega$

$R_{out} = r_o // R_D \simeq 8.6\,K\Omega$ which is very close to R_D

So Yes, ignoring r_o in This case is Justifiable

$A_v = -g_m (r_o // R_D) = -7.253\ v/v \rightarrow g_m = 888$

$= -7.682\ v/v \rightarrow g_m = 892$

$A_v = -g_m R_D = -888.65 \times 9000 = -7.997\ v/v$

So gains are close to each other so we can ignore r_o.

→ by using smaller (L) ⇒ $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 \times (1 + \lambda V_{DS})$

$I_D \propto \frac{1}{L}$ thus (I_D) increases

and $\lambda \propto \frac{1}{L}$ thus λ increase

and since $r_o = \frac{1}{\lambda^{\uparrow} I_D^{\uparrow}}$

Thus r_o decreases

Thus at min L, r_o would become Comparable to R_D and Then it Cannot be ignored because it would only increase The error → $A_v = -g_m (r_o // R_D)$

4) Intrinsic gain, $A_v = -g_m r_o = -888.65 \times 200.9962 \times 10^{-3}$

$\downarrow$ $= -178.615$ V/V

from sizing chart

$A_v = -g_m r_o = -892.1 \times 10^{-6} \times 200.28 \times 10^{3} = -178.66$

$\downarrow$

This simulation V/V

5) we already Calculated the Analitical gain

$|A_v| = 7.682$ V/V $\lll$ Intrinsic gain

the existence of the ~~R~~ resistance itself Lowers The gain very much.

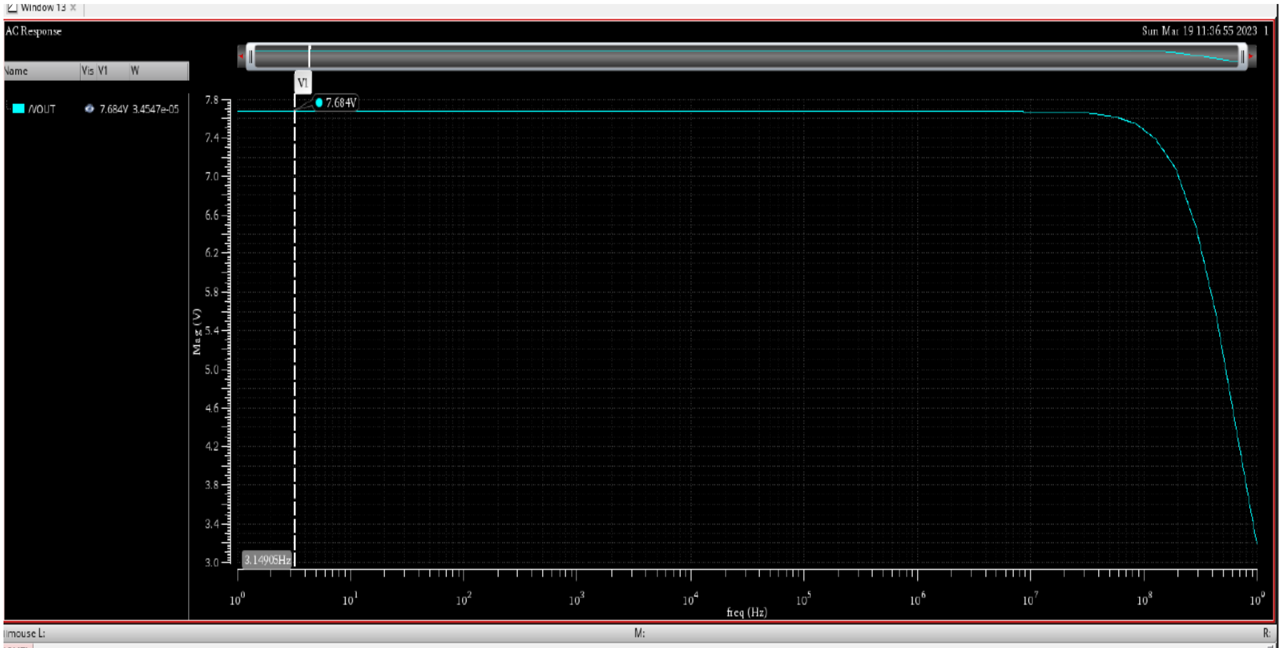
6)

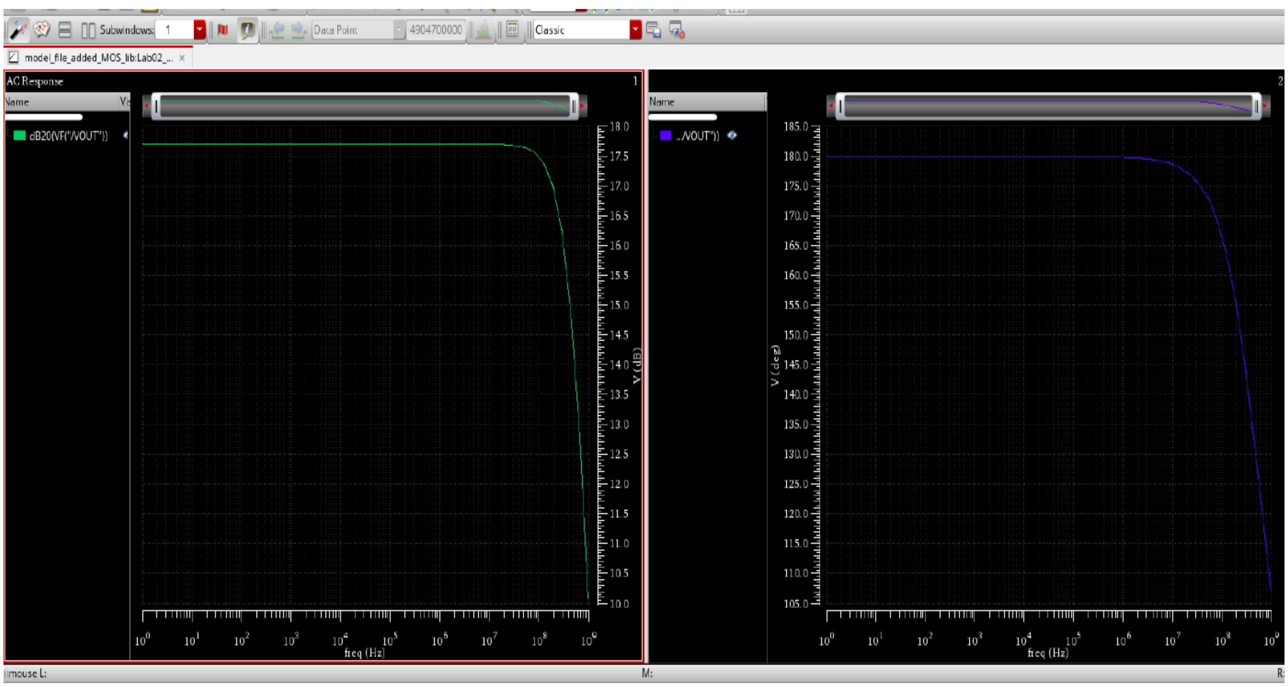
From The Ac analysis, we ~~find~~ found that

Low pass filter → parasitic capacitance exists

Gain No Coupling or bypass Capacitors

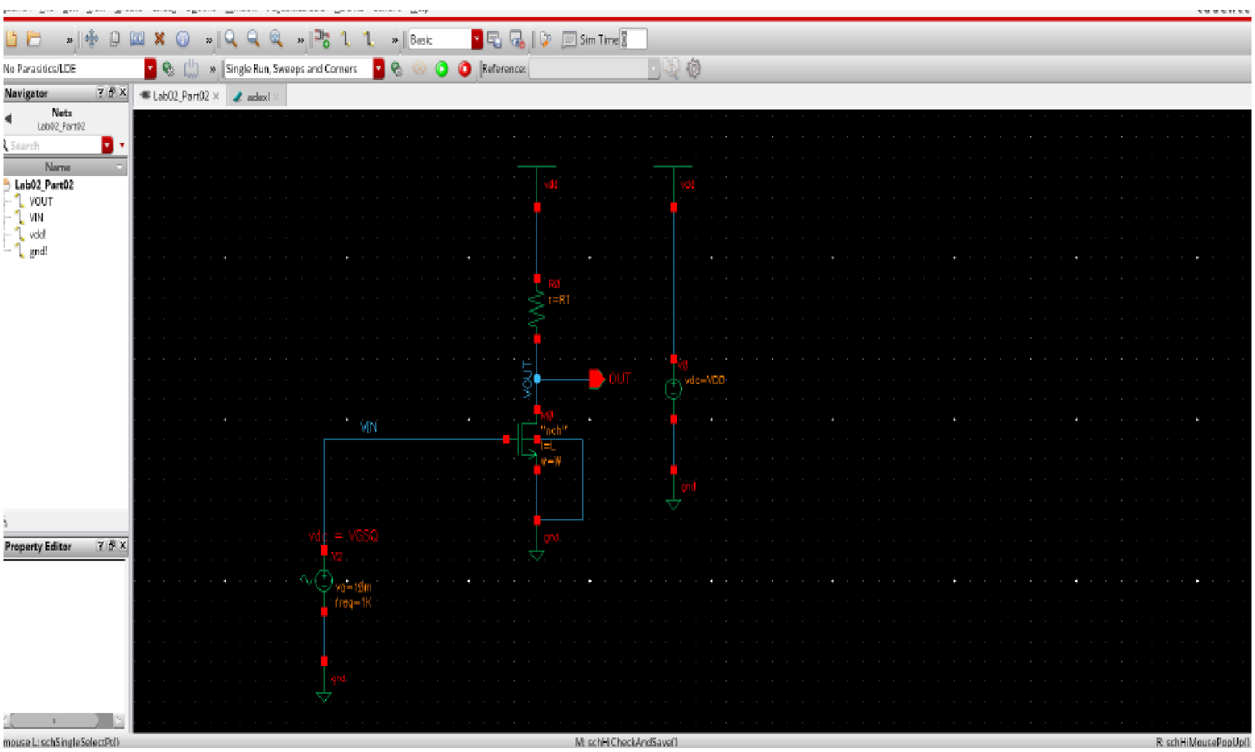
Gain = 7.684 V/V → meets the spec

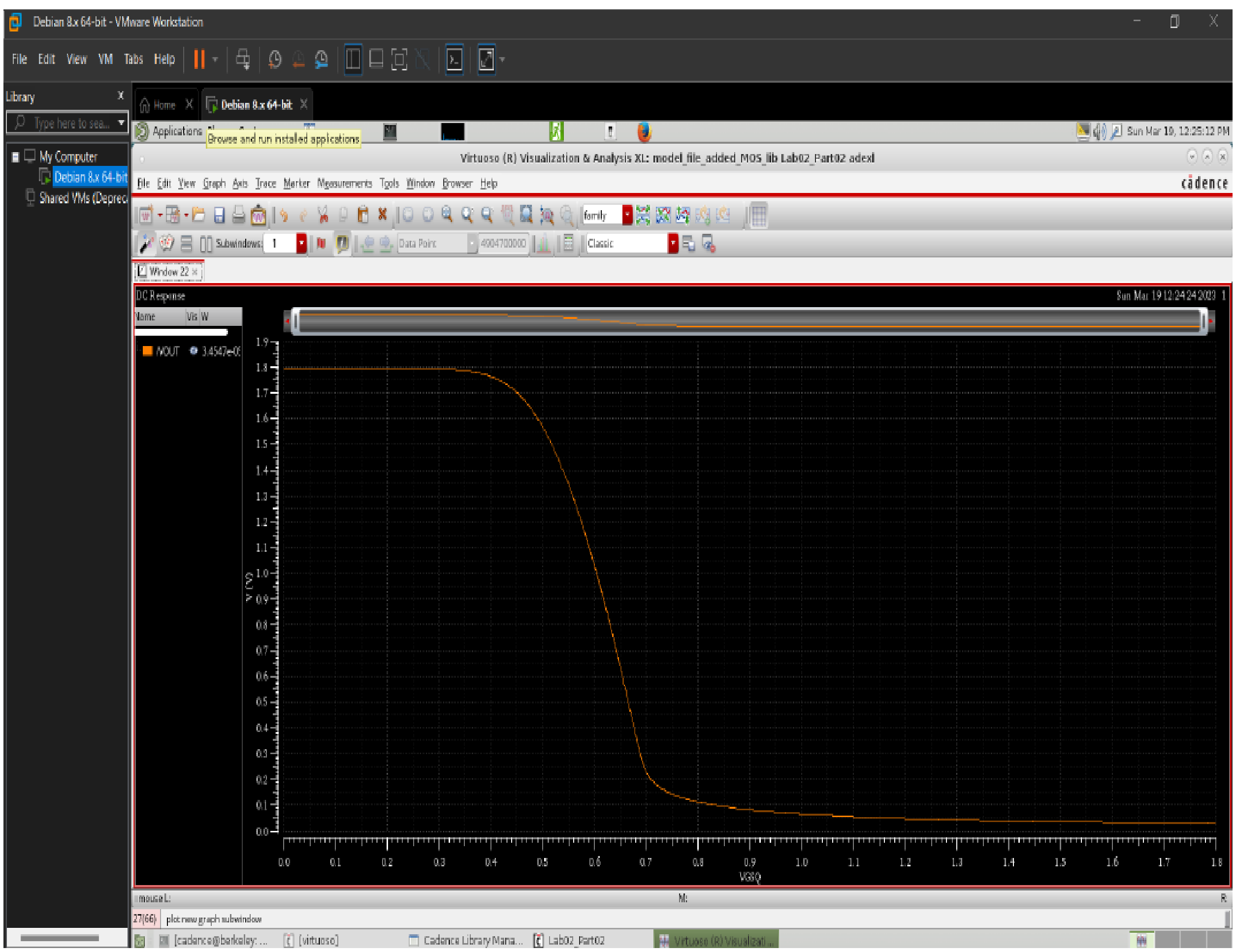




2. Gain Non-Linearity

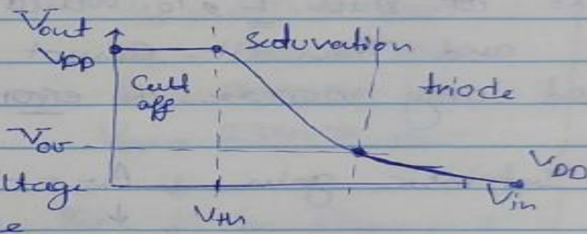
1) Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to V_{DD} with 2mV step.
2) Report VOUT vs VIN. Is the relation linear? Why?
3) Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?
4) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage).
5) Create a new simulation configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?
   - ➔ Cadence Hint: In order to save gm vs time, create an empty text file and write the following statement: save *:gm sigtype=dev. Add this text file in the model libraries. Enable DC simulation.
6) Is this amplifier linear? Comment.


Lab02_Part02
VOUT
VIN
vdd!
gnd!
OUT
Property Editor


Debian 8.x 64-bit - VMware Workstation
Virtuoso (R) Visualization & Analysis XL: model_file_added_MOS_lib Lab02_Part02 adexl
DC Response
VOUT
V (V)
VGSQ

Gain Non-linearity

2) The relation between V_{out} and V_{in} is non-linear



as it passes through three different regions

in Cutt off, $I_D = 0$

Thus $V_{out} = V_{DD}$, No voltage drop over the resistor once $V_{in} > V_{th}$, $I_D \uparrow$ and then $V_{out} > V_{ov}$, then this Saturation region $I_D = \frac{1}{2} k_n V_{ov}^2 (1 + \lambda V_{DS})$, where $V_{ov}^2 = (V_{in} - V_{th})^2$

$V_{out} = V_{DD} - I_D R_D \Leftarrow$ Quadratic depence on V_{GS}

and then $V_{out} < V_{ov}$ this is the triode region

$I_D = k_n (V_{DS} V_{ov} - \frac{V_{DS}^2}{2})$

Quadratic dependence on V_{DS}

$V_{out} = V_{DD} - I_D R_D$

In triode, $V_{out} = V_{DD} - R_D \cdot \frac{1}{2} k_n (2 V_{DS} V_{ov} - V_{DS}^2)$

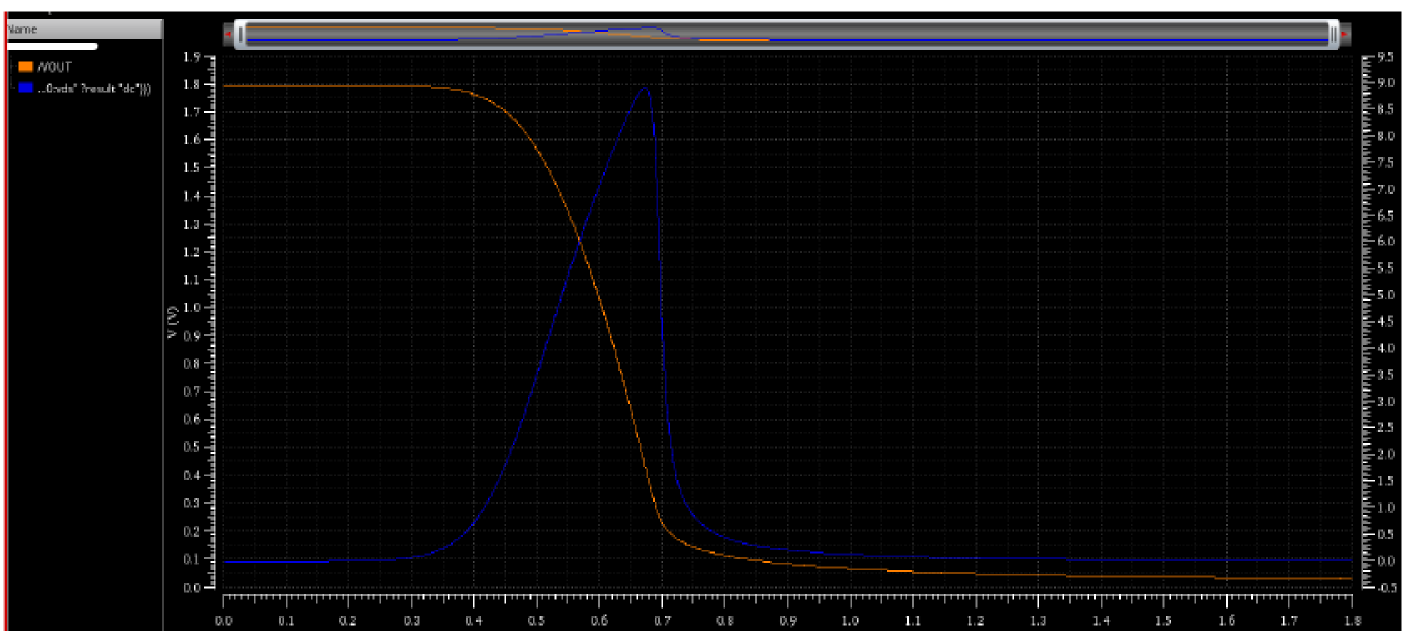
at deep triode,

$I_D \simeq 0$

more than zero by small amount $\leftarrow I_D > 0 \quad \therefore 2 V_{DS} (V_{in} - V_{th}) - V_{DS}^2 > 0$

$\therefore \boxed{V_{DS} < 2 (V_{in} - V_{th})}$

$\boxed{\text{we too abs. } \frac{\partial V_{out}}{\partial V_{in}}}$



3) The $\frac{\partial V_{out}}{\partial V_{in}}$ is non-linear too

since in cutt off region $V_{out} = V_{DD} \rightarrow$ Const.

thus $\frac{\partial V_{out}}{\partial V_{in}} = \text{zero}$

$\rightarrow$ in Saturation

$$V_{out} = V_{DD} - R_D \cdot \frac{1}{2} K_n (V_{in} - V_{th})^2 (1 + \lambda V_{out})$$

for simplicity

$$\frac{\partial V_{out}}{\partial V_{in}} = - K_n R_D (V_{in} - V_{th})$$

$\downarrow$

Semi-linear, but if we neglect the short channel effects and CLM it would be linear

triode ;

$$\frac{\partial V_{out}}{\partial V_{in}} = -\frac{1}{2} R_D K_n \left(V_{out} + (V_{in} - V_{th}) \frac{\partial V_{out}}{\partial V_{in}} - 2 V_{out} \frac{\partial V_o}{\partial V_{in}} \right)$$

$$\cancel{-2 R_D K} \quad \cancel{-2 R_D} \quad \frac{-2A}{R_D K_n} - (V_{in} - V_{th}) A + 2 V_{out} A = V_{out}$$

$$\therefore A = V_{out} \Big/ \left[2 V_{out} - (V_{in} - V_{th}) - \frac{2}{R_D K_n} \right]$$

dependent on the input

$\uparrow$

as we saw, the gain is non-linear

also $g_m = \frac{\partial I_D}{\partial V_{GS}} \rightarrow$ Semi Linear in Saturation

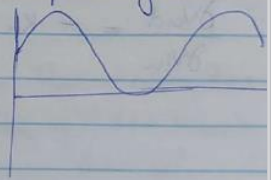
but in triode $\rightarrow I_D = K_n (V_{DS} V_{OV} - \frac{V_{DS}^2}{2})$

$$\therefore g_m = K_n (V_{DS}) \rightarrow \text{const.}$$

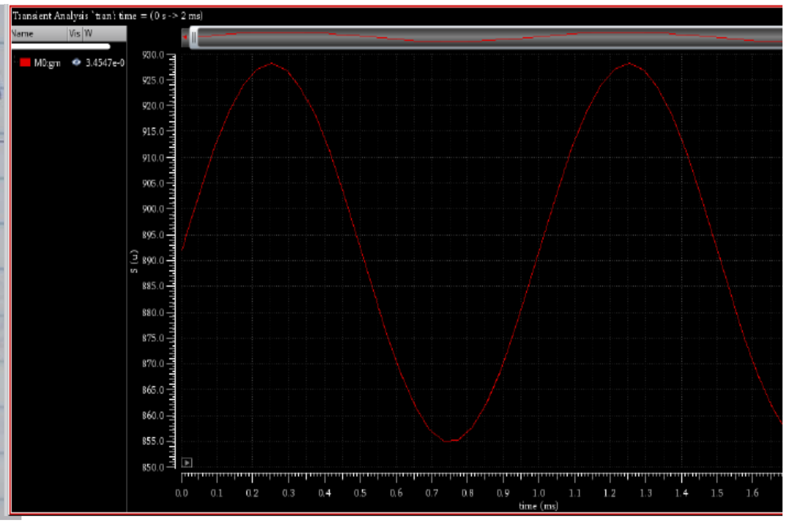
in Sat. $g_m = K_n (V_{in} - V_{th})$

$\rightarrow$ g_m depends on the input signal
this leads to dependence of the gain
on the signal which leads to non-linearity
if there is a large signal swing, non-linearity will follow.

5) Yes, gm varies with the input signal



as we can see from the gm plot vs time that it varies around the g_{mQ} value.



* when gm depends V_{GS} (dc-value) but doesn't depend on v_{gs} (AC-swing) the gain becomes linear.

as $I_D = \frac{1}{2} k_n (V_{ov})^2$

$$i_D = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_{th})^2$$

$$i_D = \frac{1}{2} k_n \left[(V_{GS} - V_{th})^2 - 2 (V_{GS} - V_{th}) v_{gs} + v_{gs}^2 \right]$$

$$i_D = \underbrace{\frac{1}{2} k_n \left[(V_{GS} - V_{th})^2 \right]}_{I_D} - \underbrace{\boxed{k_n (V_{GS} - V_{th}) v_{gs}}}_{i_d} + \underbrace{\frac{1}{2} k_n v_{gs}^2}_{\text{Non linear distortion}}$$

$$\frac{1}{2} k_n v_{gs}^2 < k_n V_{ov} v_{gs}$$

$\therefore$ $\boxed{v_{gs} < 2 V_{ov}}$ for us to neglect the distortion

→ here gm depends on the input signal swing which shows non-linearity in gain.

→ if g_m is biased at a certain V_{GS} and constant when relative to v_{gs}, the gain V_{out} related v_{gs} will be linear.

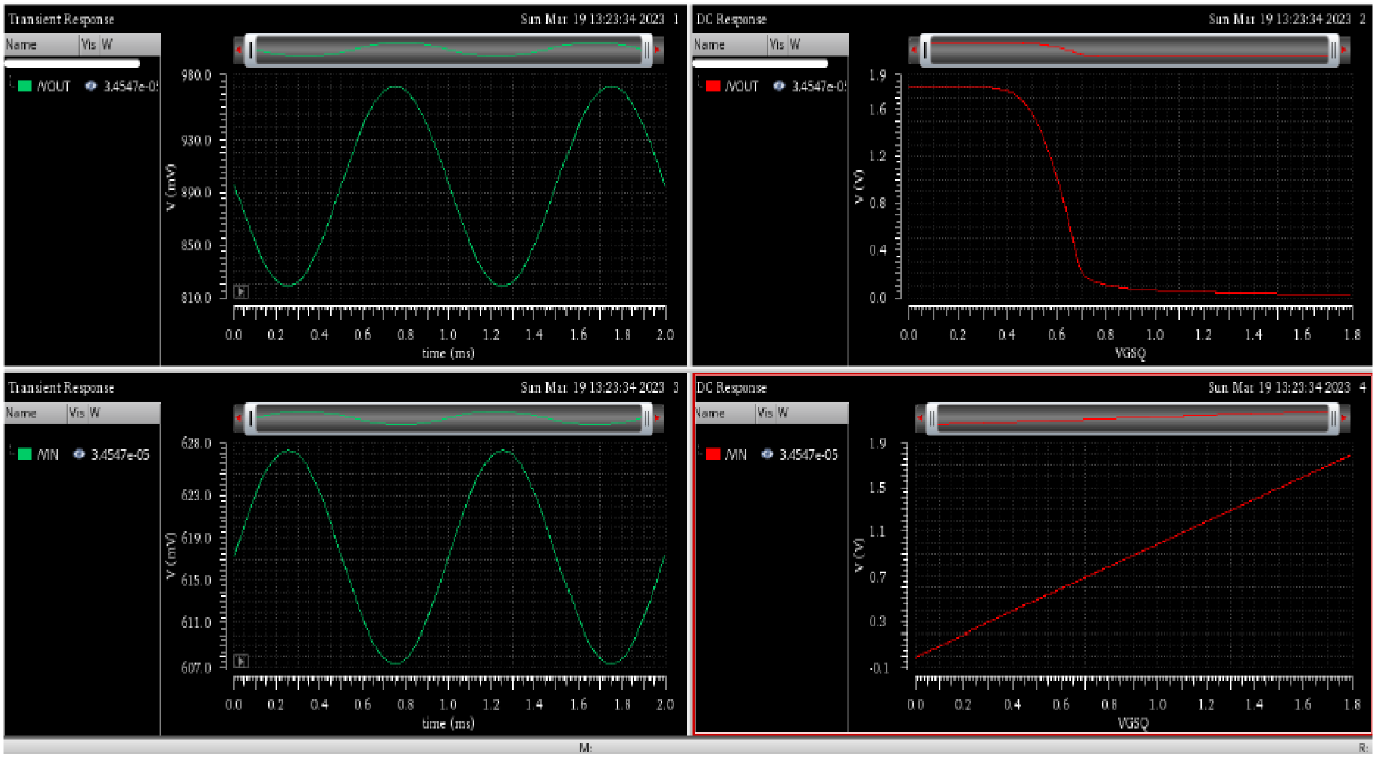
6) The gain is non-linear because gm varies with the input signal swing.

← يعني أنا لو الـ V_{GS} عندي ثبتت خلاص (أنا عاملة Bias) فخلاص لا gm ثبتت

قيمة مثلاً $g_m V_{ov}$ فلما أجي أدخل الـ V_{in} (AC) الـ V_{out}، علاقة الـ V_{out} مع الـ

Gain هتبقى linear إنما لو الـ gm بتتغير مع كل V_{in} بدخله فالـ gain

هيتغير، وبالتالي الـ V_{out} هيتغير هيا كمان ودي هتعمل Nonlinearity في الـ gain



← في البداية أنا عملت Biasing $g_m = K_n V_{ov}$ لا تعتمد
على الـ V_{gs} ولا تتغير معاها هيبقا الـ gain ← linear
علشان الـ V_{out} هتعتمد على الـ V_{gs}

$$V_o = g_m V_{gs} R_D$$

$$\frac{V_o}{V_{gs}} = \underline{\underline{g_m R_D}} \longrightarrow \text{linear}$$

إنما لو الـ g_m هيا كمان
بتتغير مع الـ V_{gs} ساعتها
العلاقة ده

$$\frac{V_o}{V_{gs}} = g_m R_D$$

↳ function of V_{gs}

هيبقا Non-linear
↓
وده الـ Gain

← التغير في الـ Curve بتاع الـ transient مش ظاهر
أوي بس هيا Non-linear ← لو عملت fft
لـ input هلاقي فيها single tone بس الـ output
هلاقيه single tone مع شوية Harmonics

← لو تغير الـ g_m مع الـ V_{gs} كبير ده
هيسبب Non-linearity في الـ Curve
إنما لو التغير مش كبير مش هيظهر
جامد.

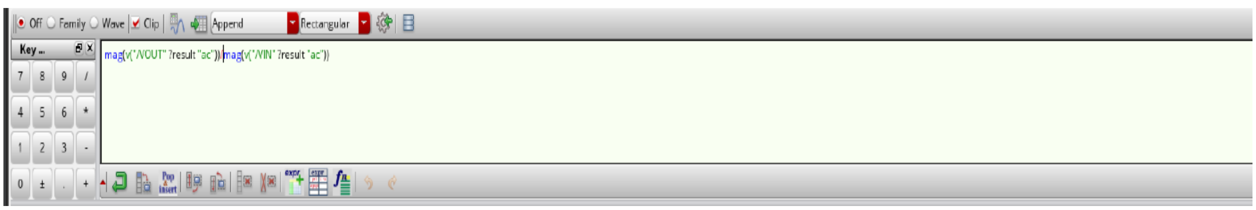
← الـ g_m دائماً بتتغير مع الـ V_{gs} $g_m = \frac{\partial i_D}{\partial v_{gs}}$
↓
Mixed signal

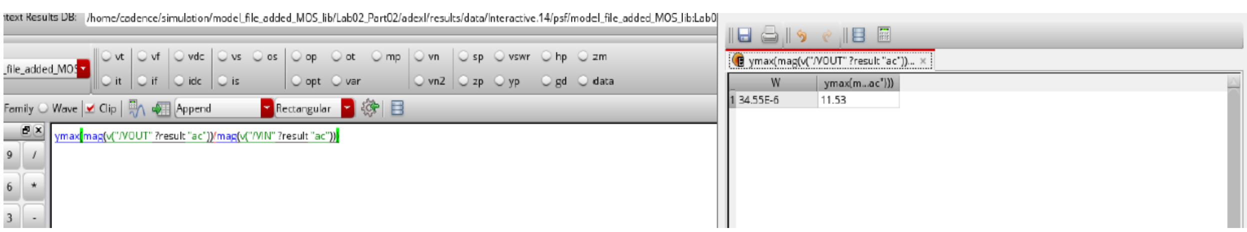
بس في بعض الـ Circuits
ممكن تقلل من التغير ده وده بيديني linearity
في الـ gain

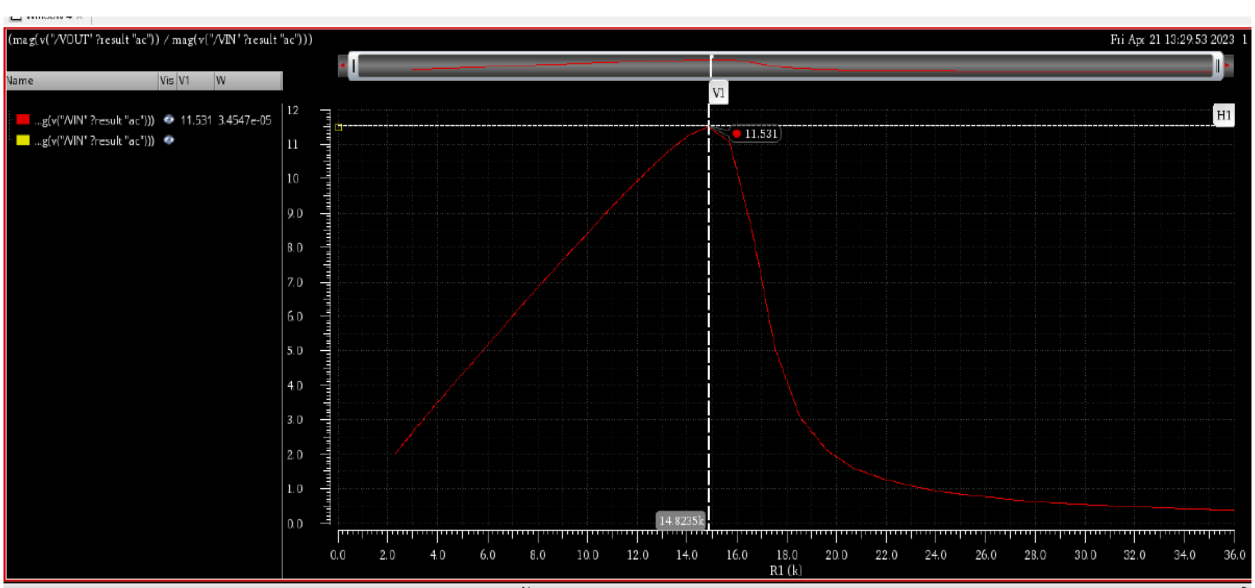
زي الـ Source degeneration ← $A_v = \frac{-g_m}{1+g_m R_s}$ ⇐ $A_v \simeq \frac{1}{R_s}$

3. [Optional] Maximum Gain

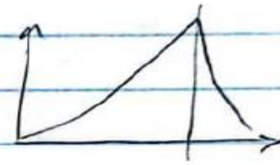
1) We want to investigate the variation of gain vs RD. We will use AC analysis to calculate the small signal gain. Set the source AC magnitude = 1. Note that AC analysis is a linear analysis, so we use a magnitude of one such that the output is itself the gain. Keep the DC value of VGS constant at the DC value you selected in Part 1.
2) Set AC simulation to sweep design variable (RD from ¼ the value you selected in Part 1 to 4 times the value you selected in Part 1). Set the AC simulation frequency at 1 Hz (single frequency point). The purpose of the AC analysis here is just to get the small signal gain and not to investigate the frequency response.
3) Use the calculator to plot the gain vs RD.
4) You will find that the gain increases with RD and then decreases with RD. Justify this behavior.
5) What is the value of RD that gives the highest gain? What is the highest gain?
6) Analytically calculate the value of RD that gives the highest gain and the highest gain using the expressions in Part 1. Compare simulation and analysis results.
7) What is the available signal swing at the point of maximum gain?
8) Is scaling down the supply voltage good for gain? Comment.





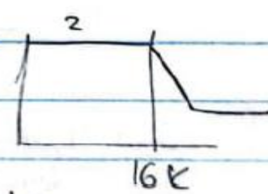


4) The gain increased at first with R_D then drops at a certain point

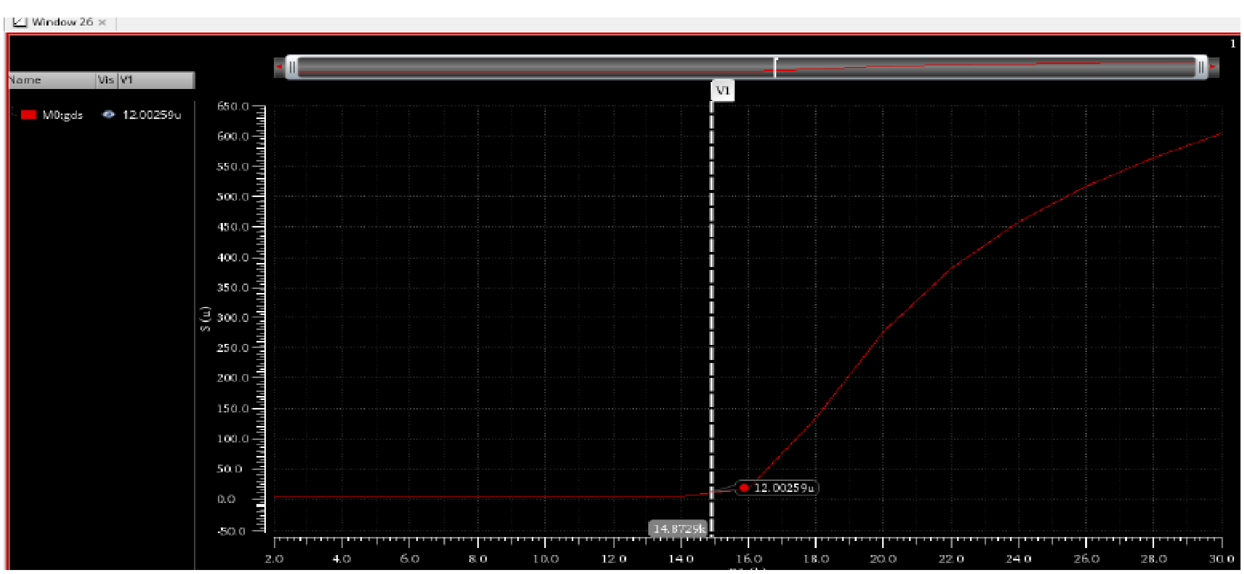


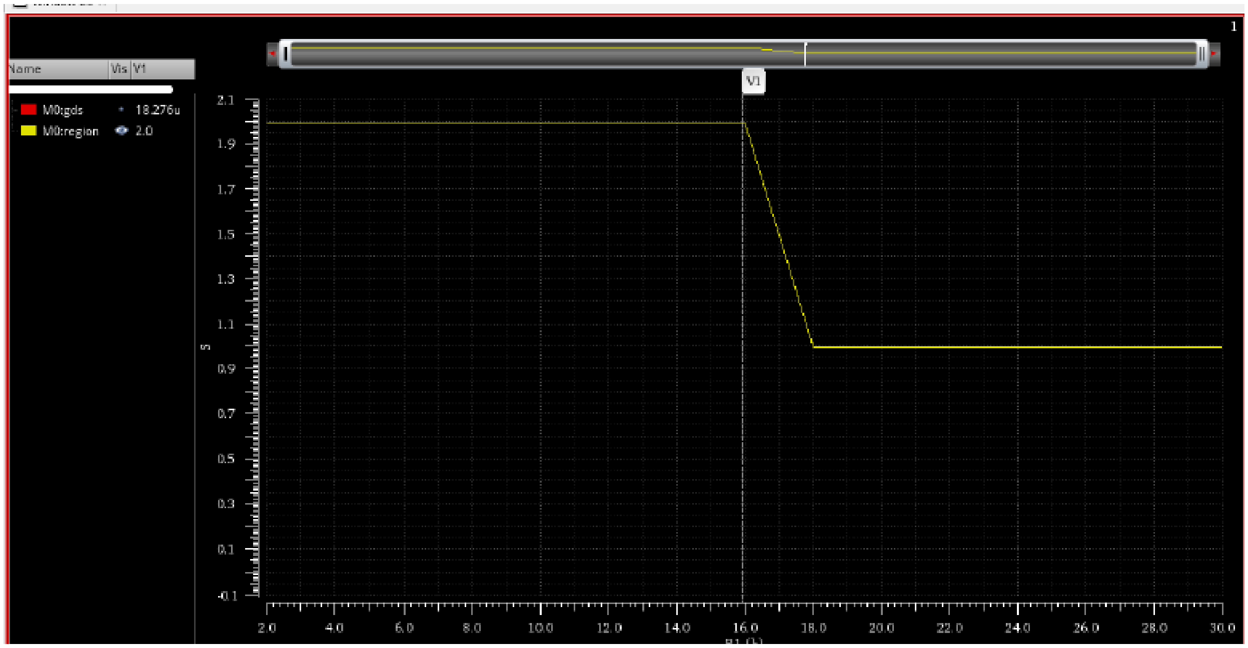
because : as R_D increases and The current remains The same, The drop on R_D inc. and Thus at a certain point, The devices enters the triode region where the r_o is small Thus gain is small.

I plotted a graph of g_{ds} that shows an inc. at $R_D = 14.8\,k\Omega$ ~~and~~ after being constant This means that the device entered The triode region.



Also There is a graph of The region That shows that the device entered the triode region at around $16\,k\Omega$ of R_D





By simulation highest R_D is 14.823 KΩ
highest gain is 11.53 V/V

6) By analysis:

$$|A_v| = g_m (R_D // r_o)$$

$$|A_v| = g_m \cdot \frac{R_D\, r_o}{R_D + r_o}$$

from part (1)

$I_D = 100\ \mu A$ and $V^*_Q = 0.225\ V$

$\therefore V_{RD} = 1.575\ V$

Then $R_{D_{max}} = 15.75\ K\Omega$

$\downarrow$ at this R_D the device will enter the triode

and A_v (hypothetically)

$$|A_v| = g_m (R_D \| r_o)$$

$$= 888.653 \times 10^{-6} \left[15750 // 200.28 \times 10^{3} \right]$$

$$= 12.9 \text{ V/V}$$

* if we ~~Through~~ Threw in the other effects simu. analysis would be right

	analysis	Simulation
A_v	12.9	11.53
R_D	15.75 KΩ	14.83 KΩ

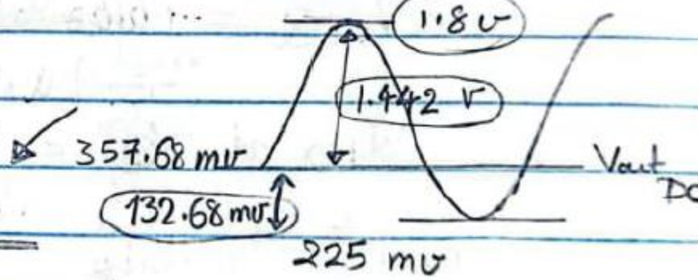
→ The effect of the triode region starts at some point at the edge of saturation.

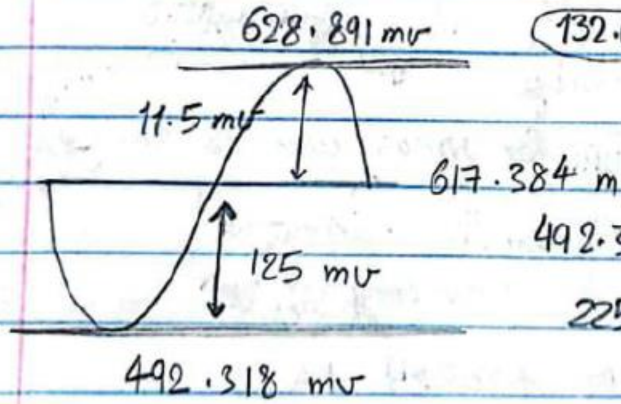
7) output Signal Swing:

$$V_{out_{max}} = V_{DD} = 1.8\ v$$

$$V_{out_{min}} = V_{OV} \simeq V_{Q}^{*} = 0.225\ v$$

and since the max gain is $\boxed{11.53\ v/v}$





$$492.318\ m < V_{in} < 628.891\ mv$$

$$225\ mv < V_{out} < 1.8\ v$$

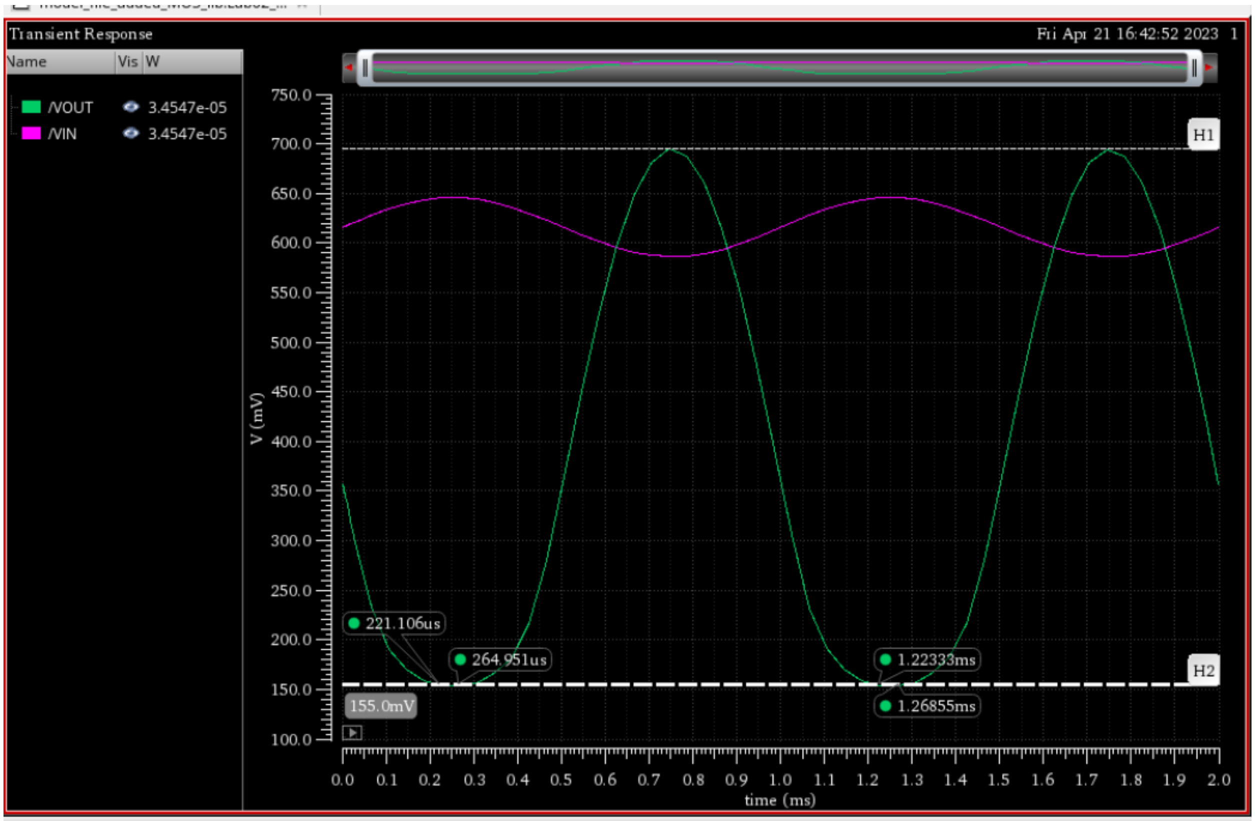
Since The input is sinosuidal if we choose 125 mv ac signal it would rise over the max. Limit.

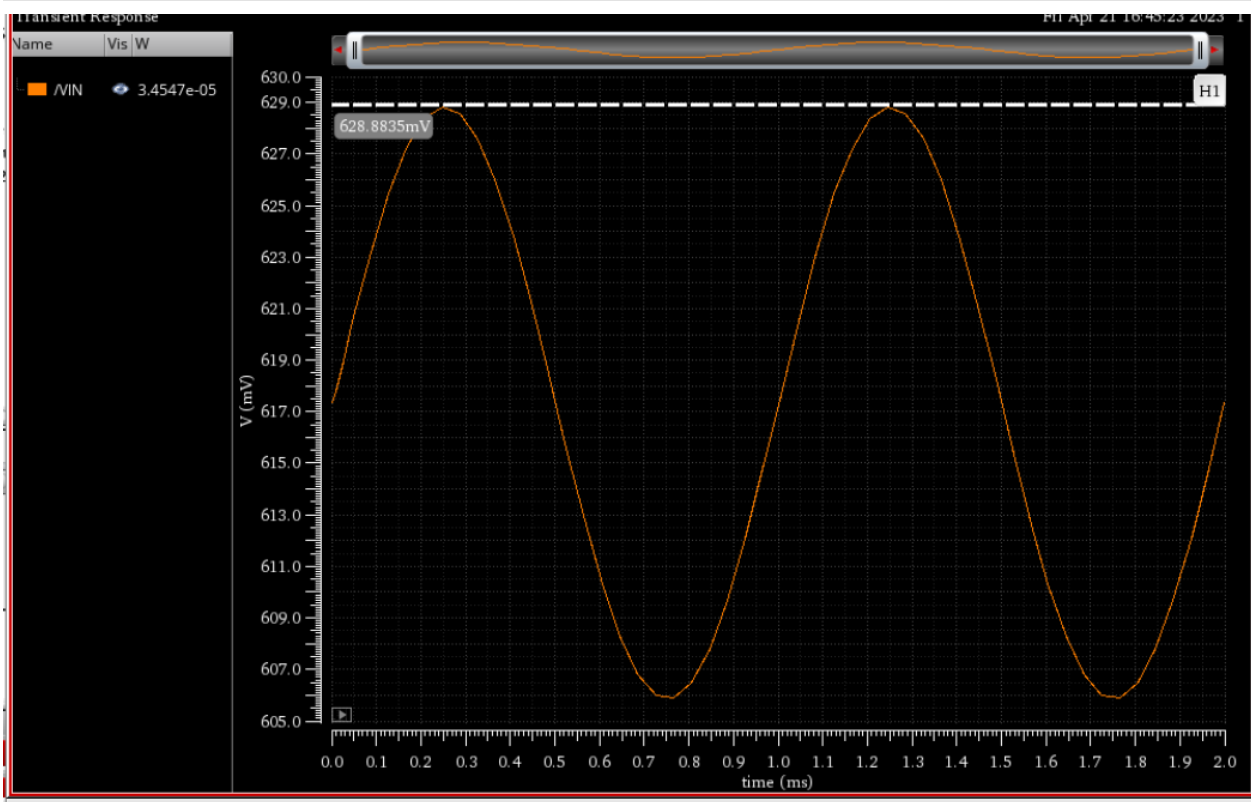
so The max. sinosoidal amp. is 11.5 mv

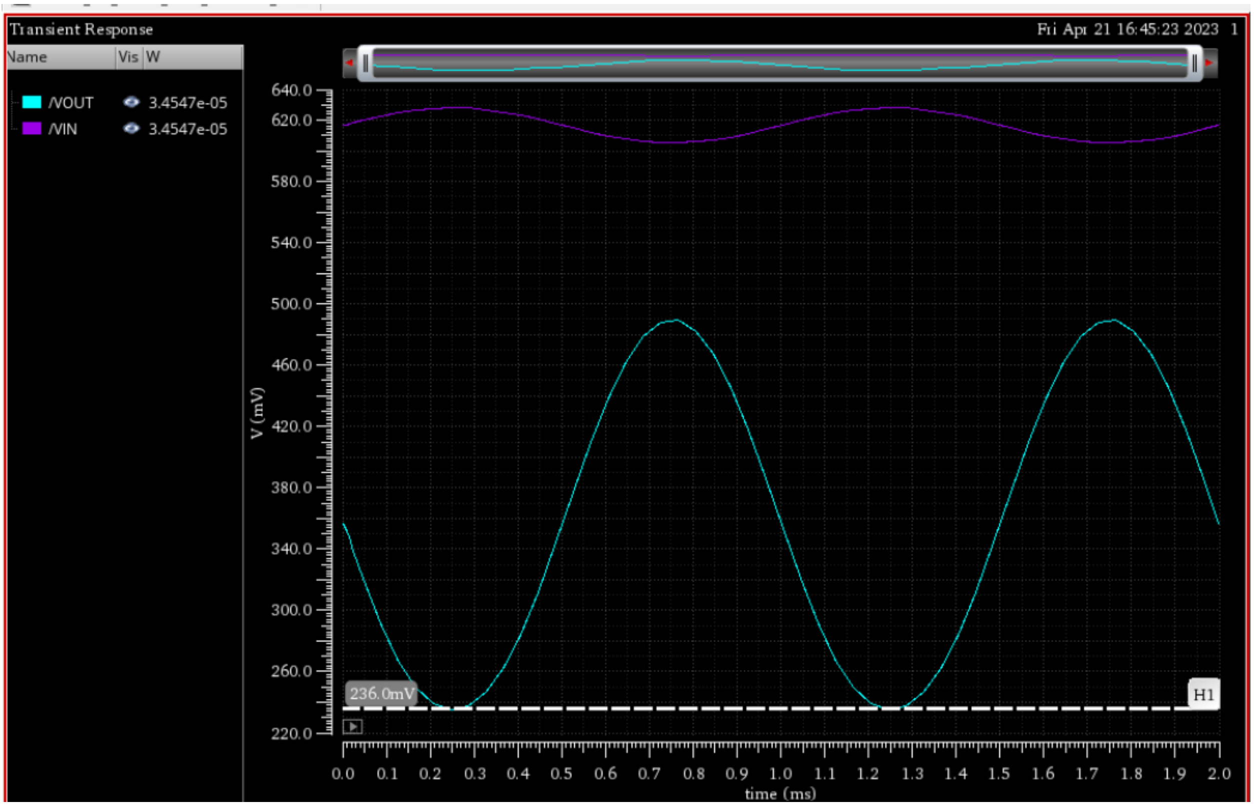
↓

Rough estimation

if we deviate from the input Range distortion occurs.


Transient Response
Fri Apr 21 16:42:52 2023
/VOUT 3.4547e-05
/VIN 3.4547e-05
H1
H2
221.106us
264.951us
1.22333ms
1.26855ms
155.0mV
V (mV)
time (ms)


/VIN 3.4547e-05
H1
628.8835mV
V (mV)
time (ms)



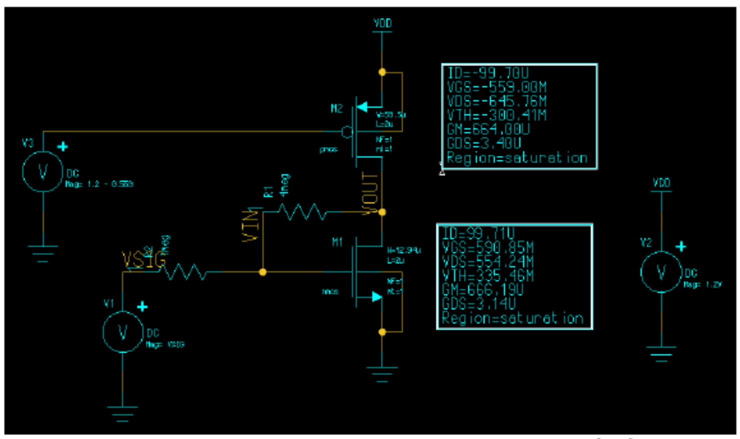
8) Yes, it might actually be good for gain as we would go down to moderate inversion and weak inversion region as $A_v = \frac{2V_A}{V^*}$

as $V^* \downarrow$ $A_v \uparrow$ also $\lambda \downarrow$ $r_o \uparrow$ gain $\uparrow$

4. [Optional] Gain Linearization (feedback)

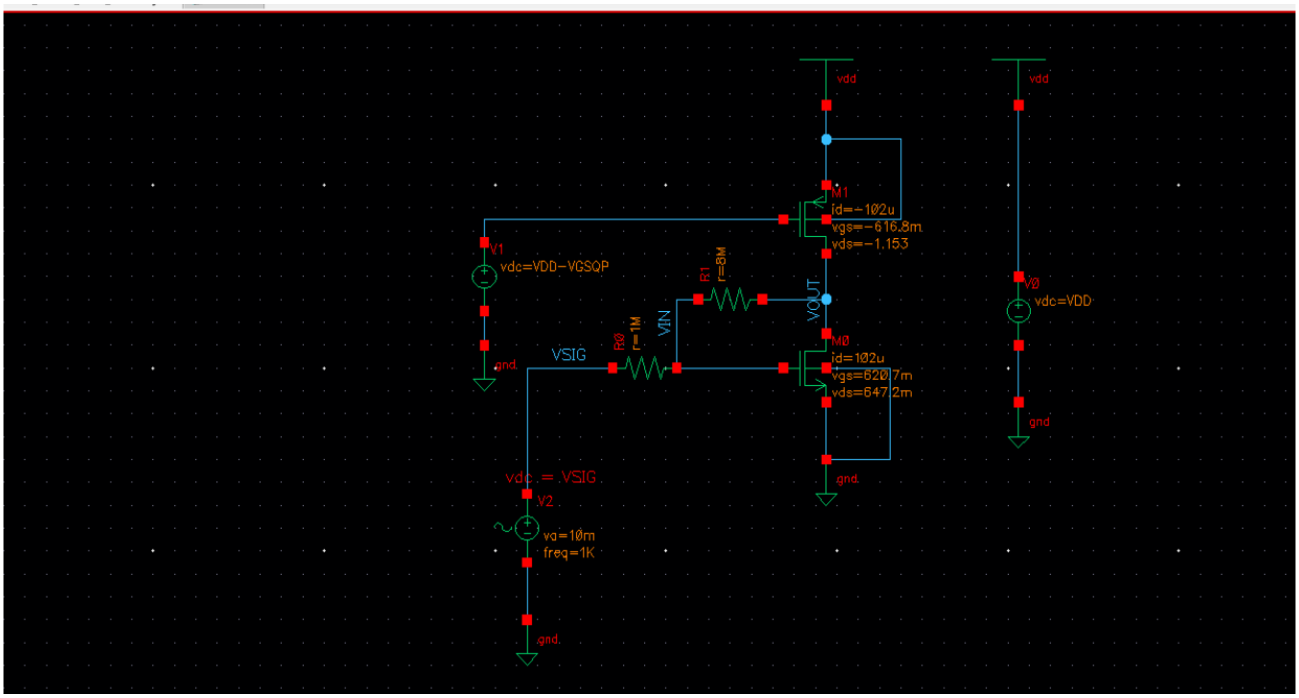
1) We will use feedback to improve the gain non-linearity. We will study feedback in more details later.
2) Create a new schematic and copy the old schematic into it.
3) Replace the resistive load with a PMOS current source (active load) as shown below. Create a sizing chart for the PMOS similar to what we did for NMOS in Part 1 using $L = 2\mu m$ and $W = 10\mu m$ (you may use the same test bench used in Part 1). From the chart, assuming V_Q^* similar to NMOS, determine V_{GSQ} and I_{DX}. Using ratio and proportion (cross-multiplication) determine W similar to Part 1. Note that the PMOS load must have the same bias current as the NMOS input device.
4) Note that it is better to bias the PMOS using a voltage source between the gate of the PMOS and VDD.

W	I_D
$10\mu m$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 100\mu A$ (from the specs)



5) Add two resistors: input resistor (R_{in}) = 1M and feedback resistor (R_f). Choose R_f to give a voltage gain approximately equal to $R_f/R_{in} = |A_v|$ as given in the specs.
6) Perform a DC sweep for the input voltage (VSIG) from 0 to V_{DD} with 2mV step.
7) Report VIN and VOUT vs VSIG (overlaid). At what voltage do the two curves cross? Why?
Hint: Compare this voltage to VGS of M1. The center value of the amplification region is itself VGS of M1. At this point VOUT is also equal to VIN because no current flows in the two resistors.
8) Is VOUT vs VSIG linear? Why?

9) Calculate the derivative of VOUT. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?
10) What is value of VIN in the part where the gain is linear?
11) Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.
Hint: When VSIG deviates from V_{GS1} current flows and VOUT deviates. The amplifier fails when M1 or M2 gets out of saturation ($V_{DS} < V^*$). You can get the input range by dividing the output range by the gain $\approx \frac{V_{DD}-2V^*}{|A_v|}$.



$\boxed{\text{Gain Linearization:}}$

$V_{tp} = -393.4$ mV for M1

at $V_Q^* = 0.225$ V

$\therefore V_{ov_Q} = 223.4515$ mV

and

$V_{GSQ} = 616.8054$ mV

I_{Dx} at $V_Q^* = 7.20924$ µ

which is possibly right as ∀ I_D for Nmos was 28 446 µA

which is 4 times this current

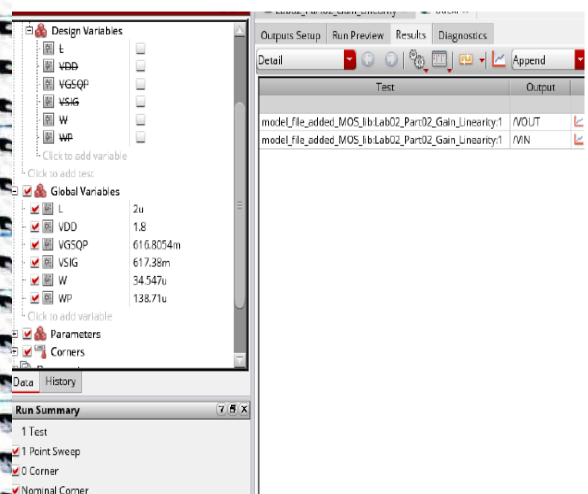
This is due to mobility of e^-

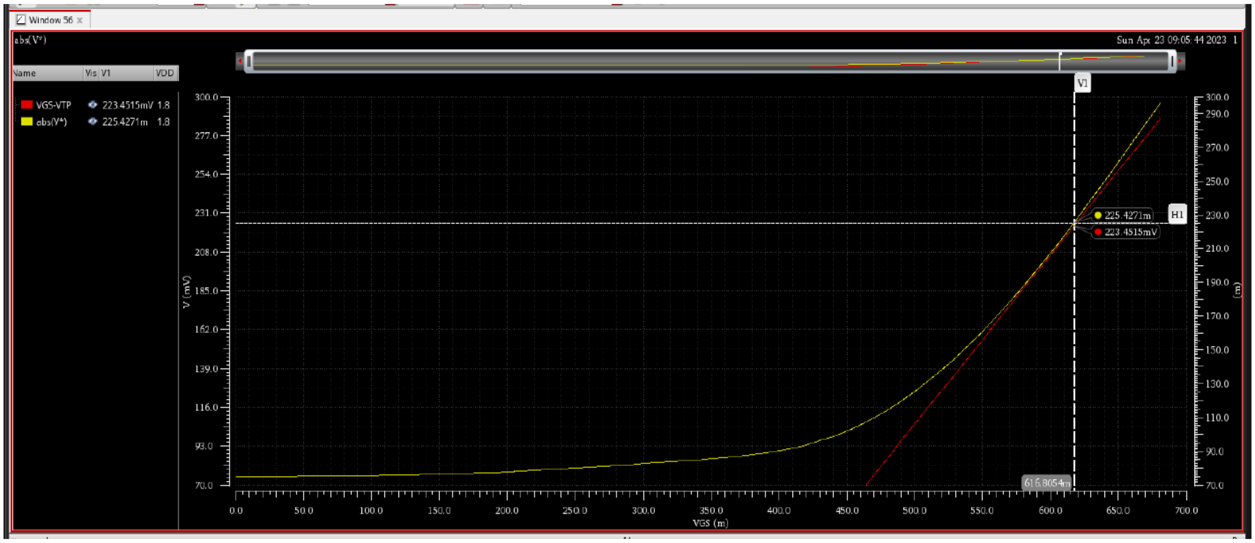
So µm ⟶ 7.20924 µA

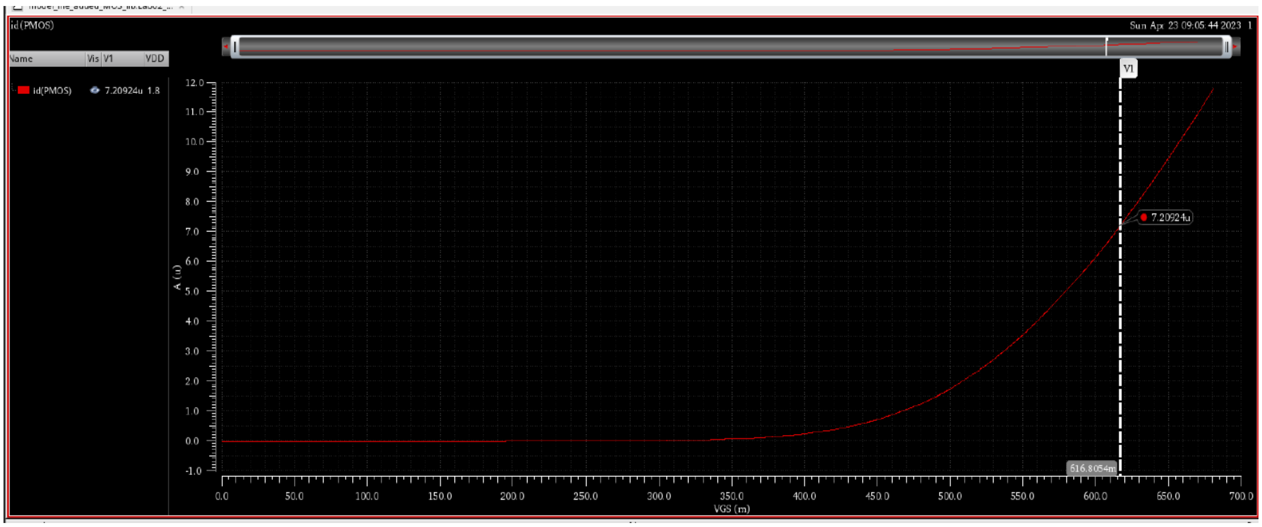
? ⟶ 100 µA

$\therefore \boxed{W_{Pmos} = 138.71 \text{ µm}}$

Test	Output	Nominal	Spec	Weig
model_file_added_MOS_lib:Lab02_Part01:1	VTH	382.6m		
model_file_added_MOS_lib:Lab02_Part01:1	V*=2ID/gm			
model_file_added_MOS_lib:Lab02_Part01:1	VGS-VTH			
model_file_added_MOS_lib:Lab02_Part01:1	id			
model_file_added_MOS_lib:Lab02_Part01:1	gm			
model_file_added_MOS_lib:Lab02_Part01:1	gds			
model_file_added_MOS_lib:Lab02_Part01:1	Vtp	-393.4m		
model_file_added_MOS_lib:Lab02_Part01:1	V*(PMOS)			
model_file_added_MOS_lib:Lab02_Part01:1	abs(V*)			
model_file_added_MOS_lib:Lab02_Part01:1	VGS-VTP			
model_file_added_MOS_lib:Lab02_Part01:1	id(PMOS)			





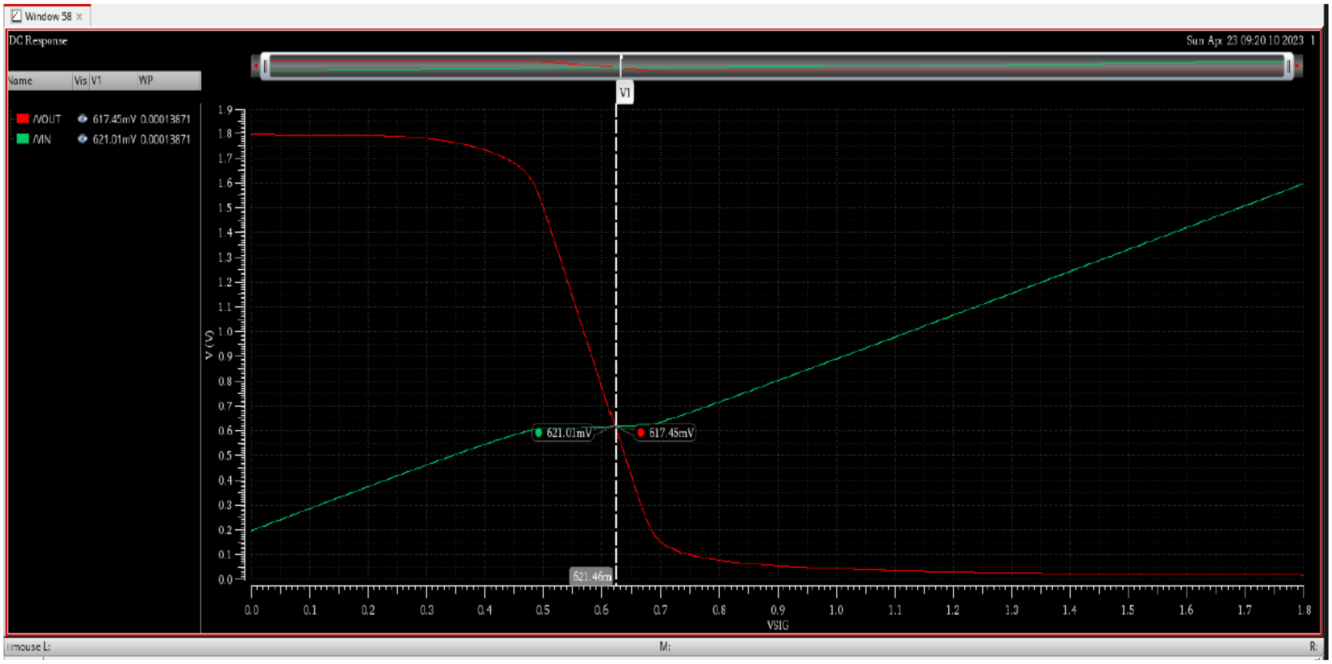


$$|A_v| = \frac{R_f}{R_{in}} \quad \therefore \quad \frac{R_f}{1M} = 8 \quad \therefore \quad R_f = 8\ M\Omega$$

7) The two curves cross at 621.46 mV which is nearly equal to V_{gs} of M0 The NMOS

$\simeq 620.7$ mV

Since No current flows through the resistors at This point Thus $V_{in} = V_{out}$

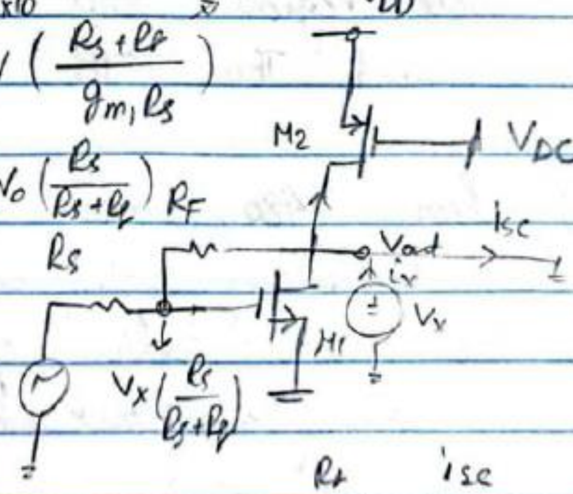


8) Yes in the saturation region (middle region) Vout is Quite linear to Vsig, since due to the presence of The feedback

$177.24\times10^3 \quad 9\times10^6 \quad 177.24\times10^3 \Rightarrow 11.451\times10^3$

$$R_{out} = r_{o2} \parallel (R_f+R_s) \parallel R_{o1} \parallel \left(\frac{R_s+R_f}{g_{m1}R_s}\right)$$

$$i_x = \frac{V_o}{r_{o2}} + \frac{V_o}{R_f+R_s} + \frac{V_o}{R_{o1}} + g_{m1}V_o\left(\frac{R_s}{R_s+R_f}\right)$$

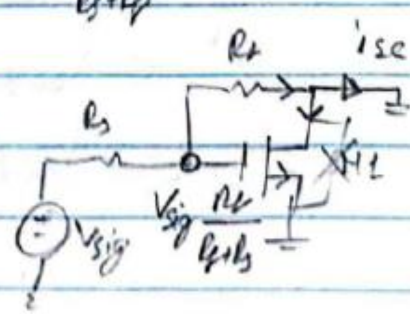


$G_m = ?$

$$\frac{V_{sig}}{R_s+R_f} = i_{sc} + g_{m1}V_{sig}\frac{R_f}{R_s+R_s}$$

$$\left(\frac{1-g_mR_f}{R_s+R_f}\right)V_{sig} = i_{sc}$$

$$\therefore G_m = \frac{1-g_mR_f}{R_s+R_f}$$



gain = Gm Rout is linear

from the graph we see that

M1	cutoff	sat	sat.
M0	triode	sat.	cutoff

⇓

input trans

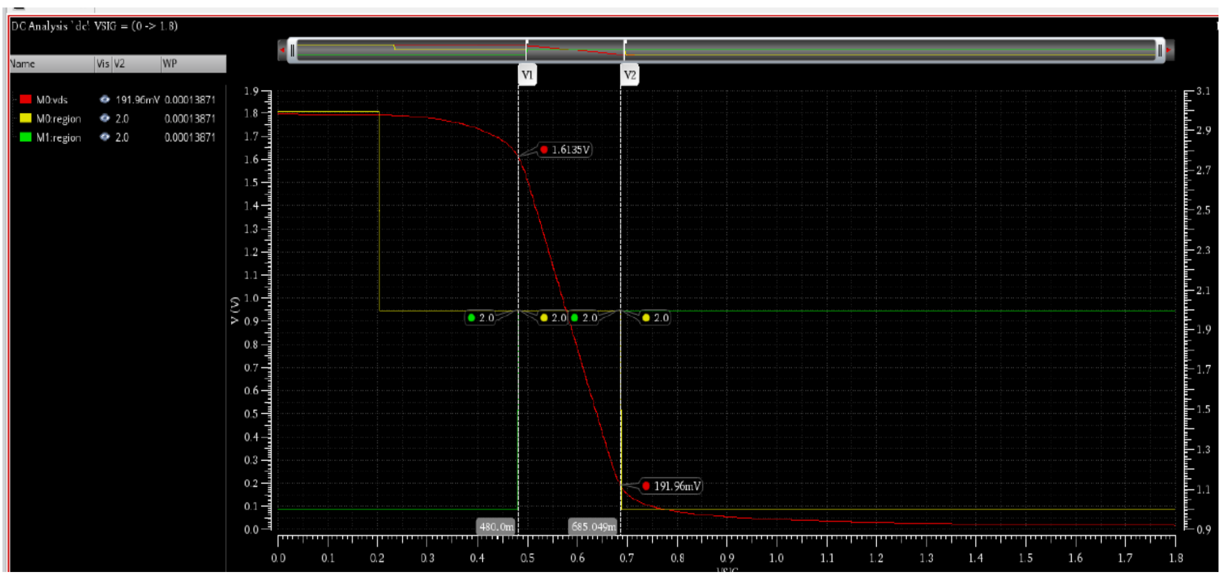
⇓

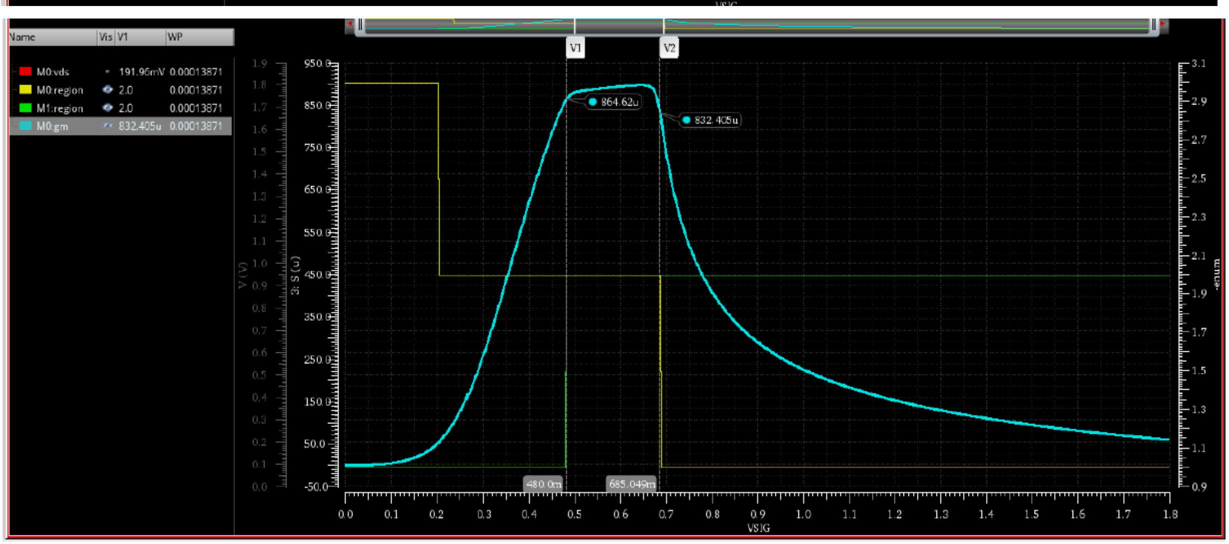
Linear gain

for as why the gain is linear too

because gm is nearly constant in that middle region too

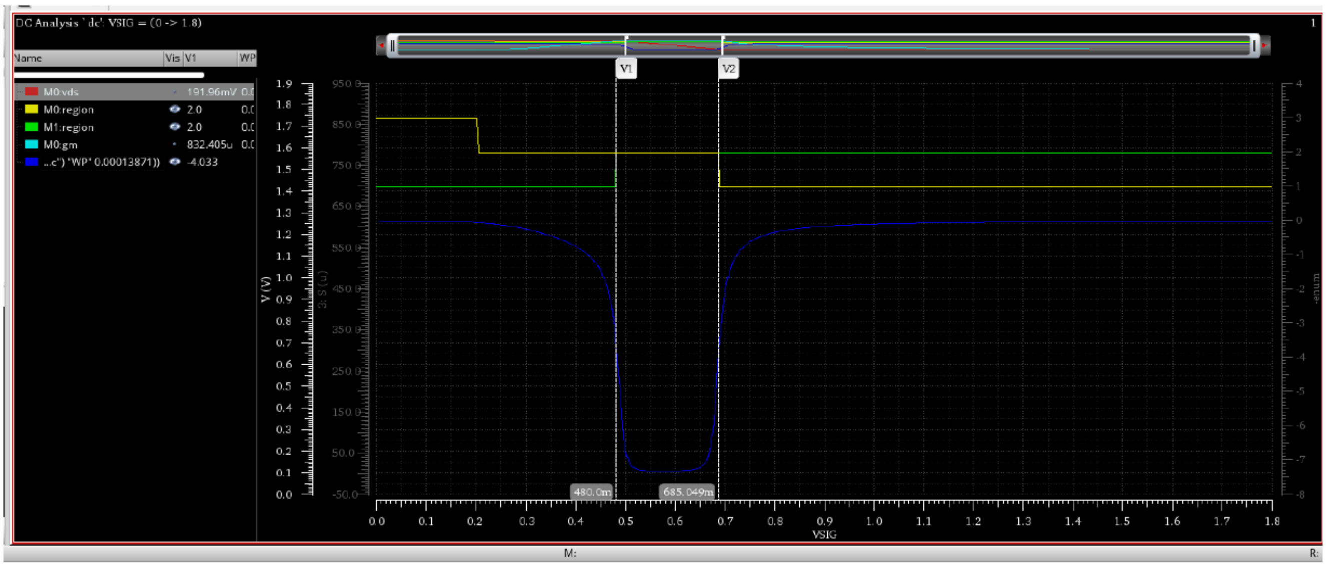
and Thus The gain linear





9) The derivative of δ Vout (small signal gain) is const in the Sat. region and Thus The gain is Linear.

1- feedback.
2- g_m Const.
3- No Variation with input swing.



10) from 480 mV to 685.049 mV
↳ where both are linear and Saturation

11) The amplification operation will fail if either device get out of saturation

$$V^* < V_{out} < V_{DD} - V^*$$

$$225\ mV < V_{out} < 1.575\ V \Rightarrow \text{Range} = V_{DD} - 2V^* = 1.29V$$

analytical

input Range will be $\frac{1.29}{8}$ = ~~190.9~~ mV ~~190.9~~

input Range in Simulation = 205 mV

161.25 mV → 180 mV

g_{m_0} = 898.1489 u

$r_{o_0} = \frac{1}{5.34877u}$ = 186.95 kΩ

$r_{o_1} = r_{o_0}$ = 186.95 kΩ

R_f = 8 MΩ

R_S = 1 MΩ

R_{out} = 9.04 kΩ

$G_m = -7.482 \times 10^{-4}$ S

Gain = −7.216 V/V

Vout

1.575 V

0.9278 m

647.2 m

422.2 m

225 mV

Vsig.

675.5 mV

58.775 m

618.8 mV

187.85 mV

128.87 m

487.9 mV

analytically

$\boxed{487.9\,mV < V_{in} < 675.5\,mV}$

nearly similar

THE END