An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier

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***Abstract*— This article presents an energy-efficient comparator design. The pre-amplifier adopts an inverter-based input pair powered by a floating reservoir capacitor; it realizes both current reuse and dynamic bias, thereby significantly boosting g_m/I_D and reducing noise. Moreover, it greatly reduces the influence of the process corner and the input common-mode voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180 nm achieves 46-μV input-referred noise while consuming only 1 pJ per comparison under a 1.2-V supply. This represents greater than seven-time energy efficiency boost compared with a strong-arm (SA) latch. It achieves the highest reported comparator energy efficiency to the best of our knowledge.**

***Index Terms*— Common-mode rejection, dynamic biasing, dynamic comparator, energy efficient, latch-type comparator, low-noise, strong-arm (SA).**

I. Introduction

COMPARATORS bridge the physical and digital worlds, as they perform the core operation of an analog-to-digital converter (ADC). In various applications, such as ubiquitous sensing and biomedical implants, a low-power and low-noise ADC is critical. As the technology scales down, the ADC power efficiency is significantly improved. Successive-approximation-register (SAR) ADCs especially benefit from its mostly digital architecture and achieve extremely low energy consumption [1]–[4]. The comparator becomes one of the major power contributors, since it is bounded by the thermal noise requirement. In addition to the power efficiency, another critical requirement raised for the comparator is input common-mode insensitivity. In the sensor-node applications, environmental interferences may cause a common-mode disturbance. In addition, advanced switching schemes in the SAR ADCs [5]–[7] also cause common-mode voltage variation. The performance of conventional dynamic comparators, including noise, offset, and speed, shows strong dependence on the input common-mode voltage, and thus, it limits the conversion resolution and degrades the system accuracy.

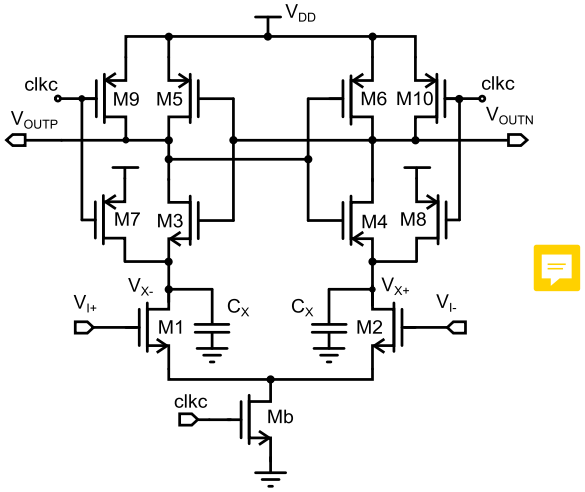

Fig. 1. Classic SA latch.

A comparator consists of a pre-amplifier followed by a latch. To save energy, dynamic comparators replace the conventional static pre-amplifiers by the dynamic integrator-based ones, which remove the static current. The strong-arm (SA) latch [8], [9], as shown in Fig. 1, is the first in this class and has been widely used over the years. The detailed operation and analysis are described in Section II-A. With the embedded dynamic pre-amplifier followed by a regenerative latch, the SA latch provides good energy efficiency and achieves fast comparison speed, thus suiting well for the energy-constraint applications. In a low-noise design, large integration capacitors C_X are required for good resolution. The complete discharge of C_X consumes the fixed energy $(2 \cdot C_X \cdot V_{DD}^2)$ and limits the comparator energy efficiency [10], [11].

Emerging efforts have been made to improve the power efficiency of dynamic comparators. To prevent the full discharge of the integration capacitors, dynamically biased (DB) integration is proposed in [12]. By providing a degeneration capacitor, V_{GS} of the input pair keeps decreasing, and eventually the input pair is cut off. It prevents fully discharging the load and boosts the g_m/I_D during the integration phase,

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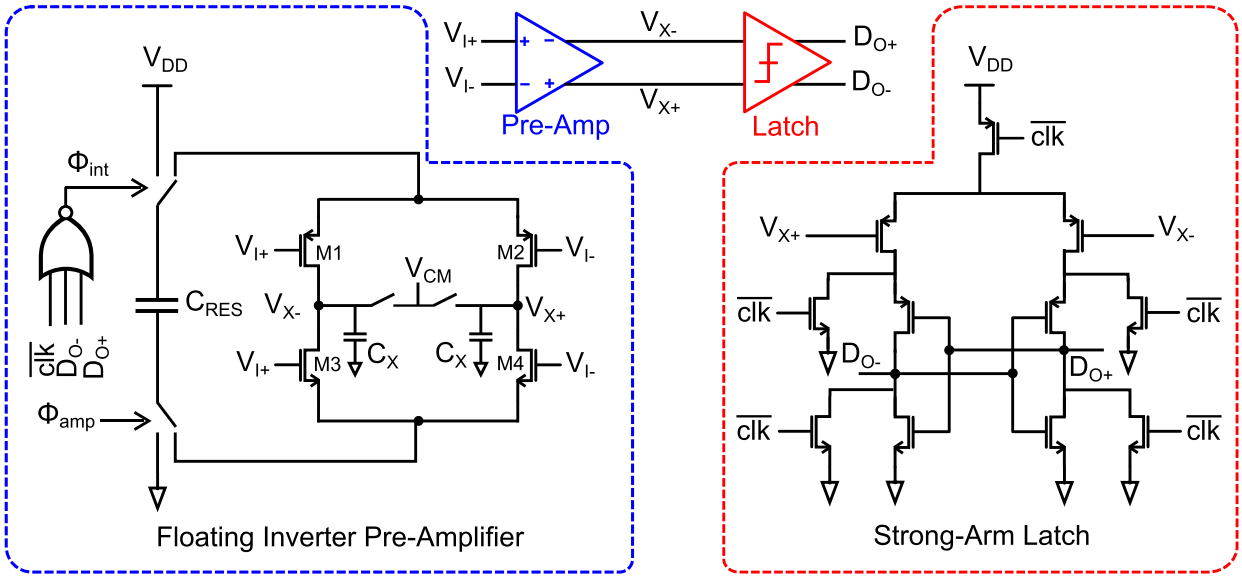

Fig. 2. Schematic of the proposed comparator with FIA.

thus resulting in a three-time energy efficiency improvement. A cascade-input comparator is proposed in [1]. It boosts integration gain by stacking the input pairs, and thus improves the energy efficiency by two times. Another way to improve the energy efficiency is explored in [13], where the bi-directional integration realizes current reuse. However, the extra circuit cost limits the efficiency improvement to 1.5 times compared with an SA latch. A gain-boosted comparator is proposed in [4], where its dynamic integrator includes a CMOS input pair followed by a pMOS common-gate stage. In addition to current reuse, it further improves energy efficiency by increasing the dynamic integrator gain. Yet, the efficiency is still limited by extra logic circuits. In addition to relatively limited efficiency boost, conventional dynamic comparators suffer from input common-mode voltage sensitivity. Since the tail transistor (Mb) works in the linear region, the integration current is heavily dependent on the input common-mode voltage, and thus, it results in variations in the comparator performance (e.g., offset, noise, and speed).

This article presents an energy-efficient dynamic comparator with a floating inverter amplifier (FIA)-based pre-amplifier, as shown in Fig. 2. The inverter-based input stage in the FIA naturally realizes current reuse. By powering the FIA with a floating reservoir capacitor, it provides an isolated power domain and makes the amplification independent of the input common-mode voltage. The FIA output common-mode voltage is kept constant, which elongates the integration time and increases the gain. In addition, the reservoir capacitor provides dynamic source degeneration that increases g_m/I_D and prevents the full discharge of the integration capacitors. Overall, the proposed comparator achieves over seven-time energy-efficiency improvement compared with the SA latch and provides input common-mode insensitivity.

This article is an extension of [14] and is organized as follows. Section II reviews the conventional SA latch and the dynamic bias technique. Section III presents the proposed FIA-based pre-amplifier design. Section IV describes the prototype comparator design. Section V shows the measured results. Finally, Section VI concludes this article.

II. Review of Prior Arts

A. SA Latch

The conventional SA latch is shown in Fig. 1. The operation can be divided into two phases, the integration phase and the latch regeneration phase, with the turn-on of the pMOS cross-coupled pair separating the two phases. During the integration phase, the comparator works as a dynamic integrator. The input signal is continuously integrated onto the integration capacitor C_X. $M3/M4$ is gradually turned on during the integration process. With the output nodes dropping below $(V_{DD}-V_{THP})$, where V_{THP} is the threshold voltage of $M5/M6$, the comparator enters the latch phase. The positive feedback provides the exponentially growing gain and dominates the behavior of the comparator during this phase. Fig. 3(a) shows a simplified model for a low-noise comparator, with large capacitors C_X placed at the integration nodes. The C_X integration process plays the dominant role in setting the comparator noise and power [10], [12], [15], [16]. Analyses in [15]–[18] show that the integration time is approximated as

$$T_{int} \approx \frac{C_X}{I_D} \cdot V_{THN} \tag{1}$$

where V_{THN} is the threshold voltage of $M3/M4$. The integration gain A_{int} depends on the input transistor g_m/I_D and the threshold voltage V_{THN}

$$A_{int} \approx \frac{g_m}{C_X} \cdot T_{int} \approx \frac{g_m}{I_D} \cdot V_{THN}. \tag{2}$$

Conventionally, the input transistors are biased in the strong-inversion region. The detailed analysis reveals that the input-referred comparator noise is dominated by the dynamic integrator, which is inversely proportional to g_m/I_D and the

loading capacitor C_X [15], [18], [19]

$$\sigma^2_{n,\text{int}} \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{\text{THN}} C_X}. \tag{3}$$

To reduce the thermal noise, we need a high g_m/I_D as well as a large loading capacitor C_X. The noise and offset contributed from the latch is attenuated by the integrator gain A_{int}

$$\sigma_{n(\text{os}),\text{in}} \approx \sqrt{\sigma^2_{n(\text{os}),\text{int}} + \frac{\sigma^2_{n(\text{os}),\text{latch}}}{A^2_{\text{int}}}}. \tag{4}$$

As can be seen, to design a low-noise comparator, it is desirable to have a large integration gain A_{int}. Overall, this SA latch saves energy by the elimination of static current and achieves high speed thanks to the positive feedback in the latch phase. However, this conventional nMOS dynamic integrator-based pre-amplifier suffers from several limitations: 1) the integration phase stops when V_{X+}/V_{X-} nodes reach $(V_{\text{DD}} - V_{\text{THN}})$, which means that only this initial discharge of the loading capacitors contributes to the noise reduction; since C_X is usually large, it is a waste of energy to fully discharge the capacitors; 2) the integration gain is limited by the bounded output common-mode drop, V_{THN}, resulting in a low dynamic integrator gain less than 10; and 3) the tail transistor works in the linear region, resulting in the strong correlated I_D with input common-mode voltage, and thus, the comparator performance (e.g., noise, offset, and speed) depends strongly on the input common-mode voltage.

B. DB Integration

The DB integration proposed in [12] increases the g_m/I_D of the input pair and prevents the full discharge of the integration capacitors C_X, thus improving the energy efficiency. A comparison between the conventional nMOS integration model and the DB integration model is presented in Fig. 3.

During the integration phase Φ_{int} of an SA latch, the overdrive voltage $(V_{\text{GS}} - V_{\text{TH}})$ of the input pair stays approximately constant, as shown in Fig. 3(c), which results in a constant g_m/I_D of 20 V^{-1} in this design. However, in a DB integrator, thanks to the tail capacitor C_{TAIL}, the source voltage V_S is charged up, which results in the reduced overdrive voltage of the input pair. It brings two benefits to this pre-amplifier design. First, as the voltage V_S increases, the V_{GS} of $M1/M2$ reduces until the source voltage reaches the cutoff point, $V_S = V_I - V_{\text{TH}}$, where V_{TH} is the threshold voltage of the transistors $M1/M2$. Then, the input pair turns off, and the dynamic integration stops, which prevents the full discharge of the loading capacitors, as can been seen from the common-mode voltage behavior of the integration nodes $V_{X,\text{CM}}$. Second, a reduced overdrive voltage results in an increased g_m/I_D during Φ_{int}. Fig. 3(c) shows that the average g_m/I_D of the DB integration is increased by 30% compared with the conventional nMOS integration. The higher g_m/I_D of the integrator directly reduces the input-referred noise of the dynamic integration phase, which is inversely proportional to g_m/I_D, as shown in (3). It also brings higher integration gain, thus reducing the noise contribution

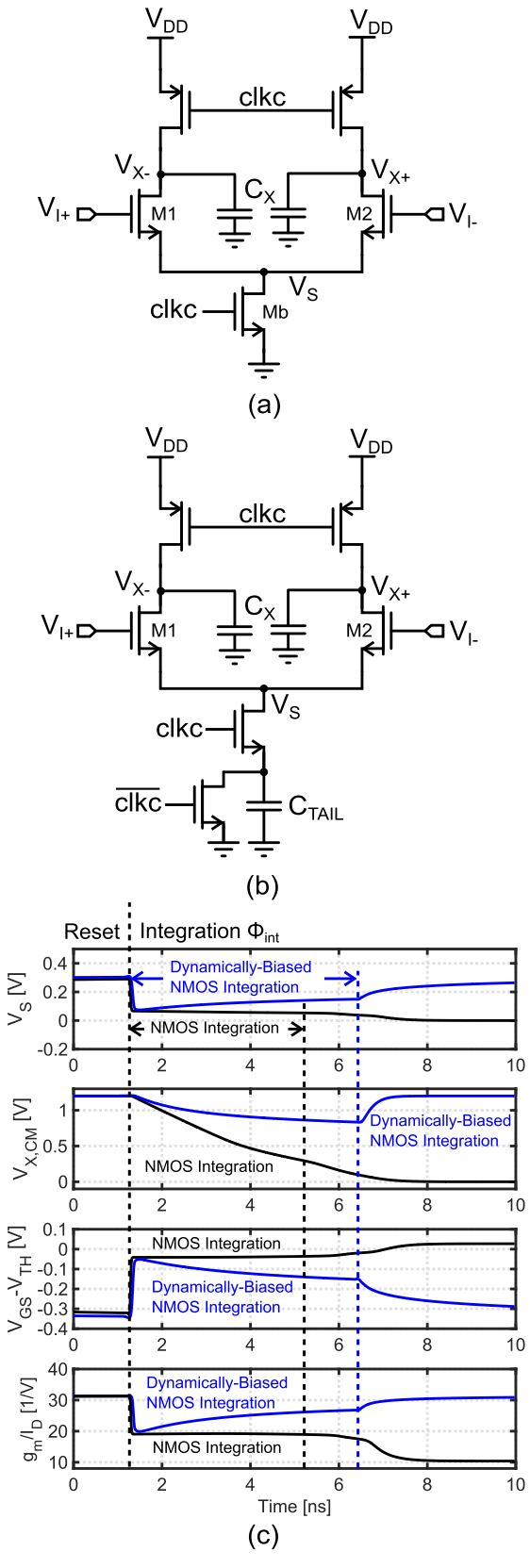

Fig. 3. (a) Conventional nMOS integration pre-amplifier model. (b) DB nMOS integration pre-amplifier model. (c) Simulated pre-amplifier behavior.

of the latch, as pointed out in (4). With the merits mentioned, the DB integration-based comparator in [12] achieves

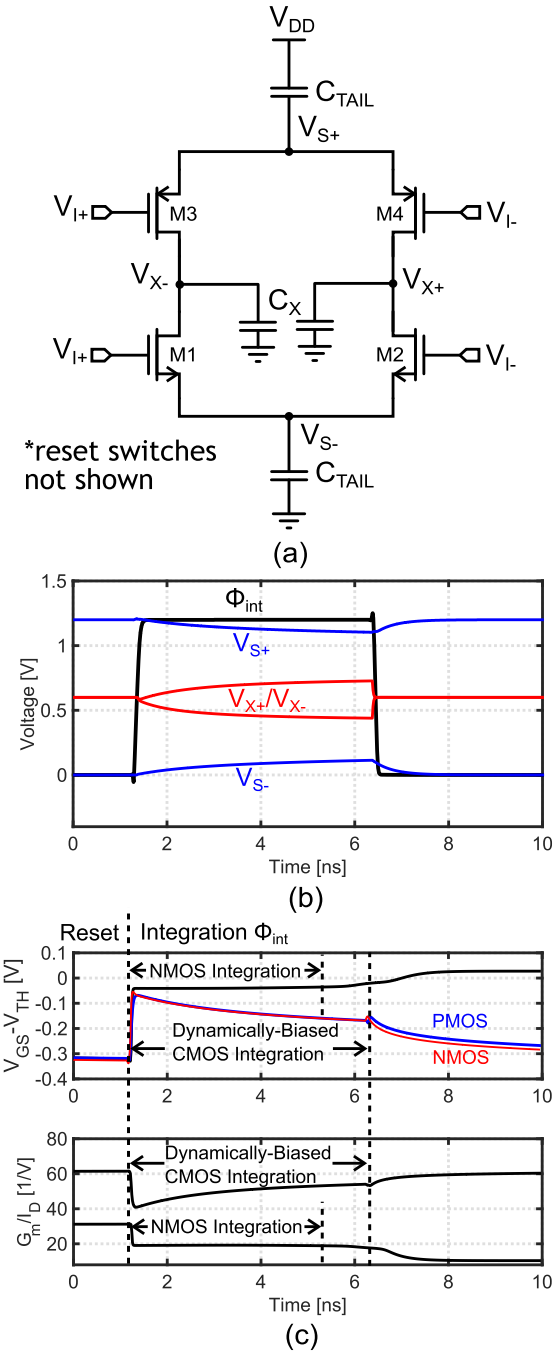

Fig. 4. (a) Proposed CMOS DB integration model. (b) Simulated pre-amplifier behavior. (c) Comparison with the SA latch.

three-time energy efficiency improvement compared with the conventional dynamic comparator.

III. Proposed Floating Inverter Pre-Amplifier

A. CMOS DB Integration Pre-Amplifier

To improve the energy efficiency of the pre-amplifier further, the CMOS DB integration is proposed in this article. A differential-mode integration model, including a CMOS input pair powered by two tail capacitors, is shown in Fig. 4(a). During the integration phase, the bottom source node V_{S-} increases, while the upper one V_{S+} decreases. It results in the decreased overdrive voltage of both nMOS and pMOS

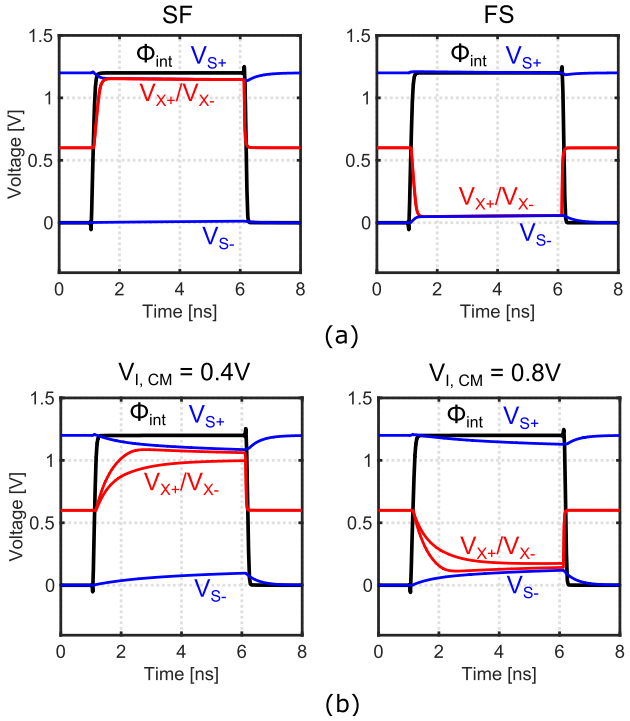

Fig. 5. Pre-amplifier behavior simulation with (a) process corner variation and (b) input common-mode voltage variation.

input pairs. Let $G_m \equiv g_{m,n} + g_{m,p}$ represent the overall transconductance of the pre-amplifier, where $g_{m,n}$ and $g_{m,p}$ are the transconductance of the nMOS and pMOS input pairs, respectively. As shown in Fig. 4(c), at the beginning of the dynamic integration phase Φ_{int}, the G_m/I_D of the pre-amplifier is twice the one in the SA latch thanks to the current reuse. Throughout the integration, it boosts the average G_m/I_D of the pre-amplifier by over 2.5 times, leading to a large improvement in the power efficiency.

In addition, during the integration phase, only the differential charge is integrated on the loading capacitors, and the common-mode voltage stays constant, which is 0.6 V with a 1.2-V supply. It prevents the full discharge of C_X and removes the bounded common-mode drop limitation for the pre-amplifier gain.

However, a caveat in this simple CMOS integration solution is the input common-mode and process corner sensitivity due to the lack of output common-mode feedback (CMFB). To ensure the CMOS integration functionality, the currents flowing through the pMOS and nMOS input pairs should be equal. In the nominal corner, as shown in Fig. 4(b), the pMOS and nMOS transistors are well balanced, so that the current reuse is achieved and the integration performs well. However, in the extreme corner like SF, as shown in Fig. 5(a), where nMOS is in the slow corner while pMOS is in the fast corner, the pMOS input transistor dominates the dynamic integration. The outputs are pulled to the supply, resulting in the failure of the integration. Similarly, in the FS corner, the nMOS side dominates the amplifier operation and pulls the output to the ground. The failure mechanism is similar for the input common-mode voltage variations, as shown in Fig. 5(b). With the lower input common-mode voltage, the pMOS input pair

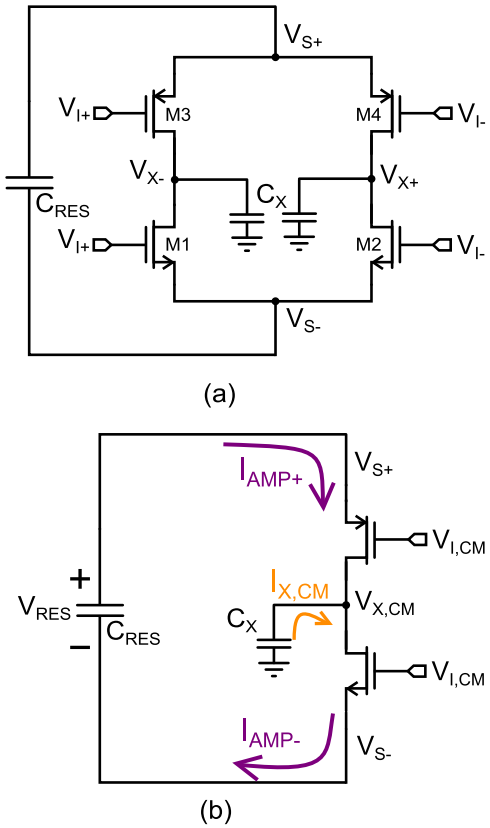

Fig. 6. (a) Proposed FIA powered by a floating reservoir capacitor. (b) Common-mode equivalent of FIA operation.

dominates the amplifier operation and vice versa. This drawback makes the simple CMOS DB integration pre-amplifier approach infeasible.

B. Floating Inverter Pre-Amplifier With Reservoir Capacitor

To solve this problem and build a robust dynamic integrator against process corner and input common-mode variations, the FIA architecture is proposed, as shown in Fig. 6(a). By merging the two tail capacitors C_{TAIL} into single floating reservoir capacitor C_{RES}, it not only reduces the total capacitance size by 75% since $C_{\text{RES}} = C_{\text{TAIL}}/2$ but also provides an isolated voltage domain for the pre-amplifier. A common-mode equivalent is shown in Fig. 6(b). Since the input and output currents from C_{RES} must be equal ($I_{\text{AMP}+} = I_{\text{AMP}-}$), the common-mode current flowing into the integration capacitor $I_{X,\text{CM}}$ is forced to be 0, thus achieving a constant output common-mode voltage without a dedicated CMFB circuit [20], [21].

A behavioral simulation result with different process corners is shown in Fig. 7(a). In the fast pMOS (SF) corner, with the reduced pMOS V_{TH}, both the initial V_{S+} and V_{S-} reduce at the beginning of the amplification phase. This downshift of the isolated voltage domain results in a decreased V_{GS} for pMOS and an increased V_{GS} for nMOS, thus forcing the currents to be the same and maintaining the correct operation. In the fast nMOS (FS) corner, both V_{S+} and V_{S-} are increased initially to maintain the correct integration.

The same mechanism also ensures the input common-mode insensitivity. The transistor strengths are balanced with

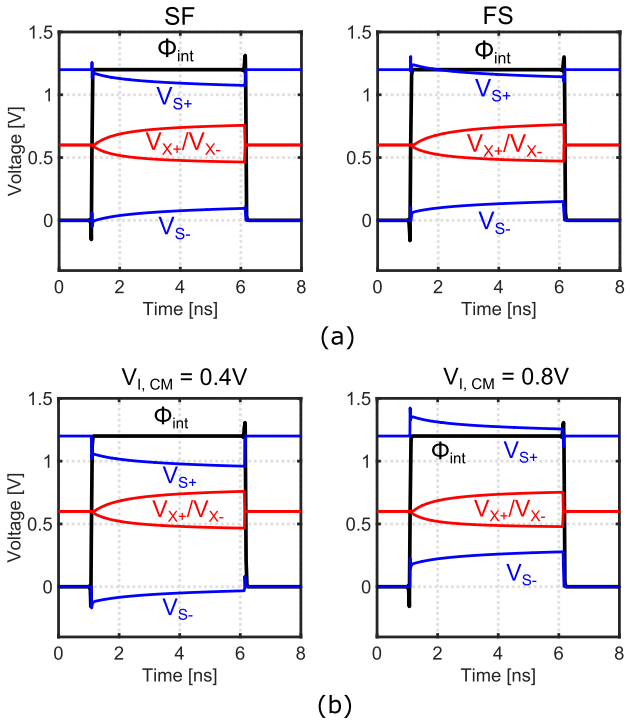

Fig. 7. FIA behavioral simulation with (a) process corner variation and (b) input common-mode voltage variation.

600-mV input common-mode voltage. If the input common-mode is decreased to 400 mV, to ensure the input–output current for C_{RES} to be the same, the isolated voltage domain will be automatically downshifted by approximately 200 mV to balance the nMOS and pMOS overdrive voltages. Similarly, with the 800-mV input common-mode voltage, the isolated voltage domain will be shifted up by about 200 mV, and as a result, the overall FIA operation is unaffected.

C. Pre-Amplifier Gain Analysis

In this design, with $V_{\text{DD}} = 1.2$ V and $V_{\text{TH}} \approx 0.55$ V in the typical corner, the input transistors $M1$–$M4$ are biased in the vicinity of the weak-inversion region when the comparison starts. With the decrease in V_{GS} during the operation, the transistors are further pushed into the deep-subthreshold region. For simplicity of analysis, we assume that the input transistors always work in the weak-inversion region. The transconductance is expressed as [22], [23]

$$G_m(t) \approx 2 \cdot \frac{I_D(t)}{n \cdot U_T} = \frac{I_{\text{AMP}}(t)}{n \cdot U_T} \tag{5}$$

where $I_D(t) \approx (1/2) \cdot I_{\text{AMP}}(t)$ is the instantaneous current of the transistor with a small differential input voltage, n is the weak-inversion slope factor, and $U_T = kT/q$ is the thermal voltage. By ignoring the output impedance of the input transistors, the differential pre-amplifier output voltage can be approximated as

$$\begin{aligned} \Delta V_{X,\text{DM}}(t) &= \frac{\int_0^t \Delta V_{I,\text{DM}} \cdot G_m(\tau) d\tau}{C_X} \\ &\approx \frac{\Delta V_{I,\text{DM}} \int_0^t I_{\text{AMP}}(\tau) d\tau}{n \cdot U_T \cdot C_X}. \end{aligned} \tag{6}$$

The tail current $I_{\text{AMP}}(t)$ can be calculated as follows:

$$I_{\text{AMP}}(t) = \frac{I_{\text{AMP}}(0^+)}{1 + \frac{I_{\text{AMP}}(0^+)}{n \cdot U_T \cdot C_{\text{TAIL}}} t} \tag{7}$$

where $I_{\text{AMP}}(0^+)$ is the tail current at the instant $(t = 0^+)$ when the comparator starts.

The source voltage V_{S+}/V_{S-} change $\Delta V_S(t)$ can be shown as follows:

$$\begin{aligned}\Delta V_S(t) &= \frac{\int_0^t I_{\text{AMP}}(\tau) d\tau}{2 \cdot C_{\text{RES}}} \\ &= n \cdot U_T \cdot \ln\left(1 + \frac{I_{\text{AMP}}(0^+)}{2 \cdot n \cdot U_T \cdot C_{\text{RES}}} t\right). \end{aligned} \tag{8}$$

This derived logarithmic behavior matches with the simulation results in Fig. 4(b). The integration gain is calculated as

$$\begin{aligned}A_V(T_{\text{INT}}) &= \frac{\Delta V_{X,\text{DM}}(T_{\text{INT}})}{\Delta V_{I,\text{DM}}} \\ &= \frac{2 \cdot C_{\text{RES}} \cdot \Delta V_S(T_{\text{INT}})}{n \cdot C_X \cdot U_T}. \end{aligned} \tag{9}$$

In this design, C_{RES} is chosen to be 2 pF and C_X is approximated as 250 fF including the parasitics. With 1-mV differential input V_I, $\Delta V_S(T_{\text{INT}})$ is approximately 125 mV according to the simulation. The calculated $A_V(T_{\text{INT}})$ is approximately 60. Due to the finite output impedance of the input transistors $M1$–$M4$, the simulated gain is around 30, which is still significantly higher than that of the SA latch.

D. Pre-Amplifier Noise Analysis

1) Conventional nMOS Integration Pre-Amplifier: The noise analysis for the conventional nMOS integration pre-amplifier is presented in this section. The following derivations are based on the weak inversion noise model. The general expression of the dynamic integrator's output noise can be described as a convolution of the power spectral density (PSD) $S_i(t)$ of the noise source and the magnitude squared impulse response from the noise source to the output voltage ($|h_n(t)|^2$) [12], [15], [18]

$$\sigma_o^2(t) = \frac{1}{2} \int_0^t S_i(t-\tau) \cdot |h_n(\tau)|^2 d\tau \tag{10}$$

where $S_i(t) = 4qI_D(t)$ is the input-referred single-sided white noise PSD contributing from $M1$ and $M2$ biased in the weak-inversion region [24]. Since $I_D(t)$ depends on the overdrive voltage $(V_{\text{GS}} - V_{\text{TH}})$, which is relatively constant during the dynamic integration, as shown in Fig. 3(c), $S_i(t)$ is assumed to be independent of time for simplicity. With the approximated impulse response $h_n(t) = (1/C_X) \cdot u(t)$, the mean square noise voltage at the pre-amplifier output can be derived as

$$\sigma_{o,\text{SA}}^2(t) = \frac{2nkT \cdot \Delta V_{X,\text{CM}}(t)}{C_X} \cdot \frac{g_m}{I_D}. \tag{11}$$

Recalling the integration gain from (2), the input-referred noise of the conventional nMOS integration pre-amplifier at the end of the integration phase T_{INT} can be expressed as

$$\sigma_{\text{in,SA}}^2(T_{\text{INT}}) = \frac{2nkT}{V_{\text{THN}} \cdot C_X} \cdot \frac{I_D}{g_m}. \tag{12}$$

2) DB Integration Pre-Amplifier: Similarly, in the DB comparator [12], the input-referred noise $\sigma_{o,\text{DB}}^2(t)$ is given as

$$\sigma_{o,\text{DB}}^2(t) = \frac{2q \cdot \Delta V_{X,\text{CM}}(t)}{C_p}. \tag{13}$$

The differential-mode signal gain can be calculated as

$$A_V(T_{\text{INT}}) = \frac{\Delta V_{X,\text{CM}}(T_{\text{INT}})}{n \cdot kT/q}. \tag{14}$$

The input-referred noise of the DB comparator at the end of the preamplification phase T_{INT} is derived as

$$\sigma_{\text{in,DB}}^2(T_{\text{INT}}) = \frac{2nkT}{C_p \cdot \Delta V_{X,\text{CM}}(T_{\text{INT}})} \cdot \frac{I_D}{g_m}. \tag{15}$$

3) Proposed FIA: In the proposed FIA design, $S_i(t) = 8qI_D(t)$ contributed from the differential CMOS input-pairs $M1$–$M4$. The mean-square noise voltage generated across the pre-amplifier output is derived as

$$\sigma_{o,\text{FIA}}^2(t) = \frac{4q \cdot C_{\text{RES}}}{C_X^2} \Delta V_S(t). \tag{16}$$

Given the voltage gain of the pre-amplifier in (9), the input-referred noise at the end of the preamplification time T_{INT} can be calculated as

$$\sigma_{in,\text{FIA}}^2(T_{\text{INT}}) = \frac{2nkT}{C_{\text{RES}} \cdot \Delta V_S(T_{\text{INT}})} \cdot \frac{I_D}{G_m}. \tag{17}$$

As can be seen, the input-referred noise of the proposed FIA is inversely proportional to G_m/I_D. In addition, the larger C_{RES} and $\Delta V_S(T_{\text{INT}})$ lead to a larger integration gain, which reduces the input-referred noise.

E. Energy Efficiency Analysis

Due to the fundamental tradeoff between energy consumption and thermal noise, a figure of merit (FoM) to represent the energy efficiency of a comparator is defined as the product of the comparator energy consumption and the input-referred noise power

$$\text{FoM} = \text{Energy} \cdot (\text{Noise Power}). \tag{18}$$

The lower the FoM, the higher the efficiency the comparator achieves. In a low-noise comparator, the pre-amplifier dominates the power consumption as well as noise contribution, and thus, the comparator's energy efficiency can be approximated by that of the pre-amplifier.

With the energy consumption per SA latch comparison as $(2 \cdot C_X \cdot V_{\text{DD}}{}^2)$ and input-referred noise derived in (12), the FoM of the pre-amplifier in the classic SA latch is expressed as

$$\text{FoM}_{\text{SA}} = \frac{4nkT \cdot V_{\text{DD}}{}^2}{V_{\text{THN}}} \cdot \frac{I_D}{g_m}. \tag{19}$$

Similarly, the energy consumption per DB pre-amplifier is $(2 \cdot C_X \cdot \Delta V_{X,\text{CM}} \cdot V_{\text{DD}})$, which results in an FoM as

$$\text{FoM}_{\text{DB}} = 4nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{g_m}. \tag{20}$$

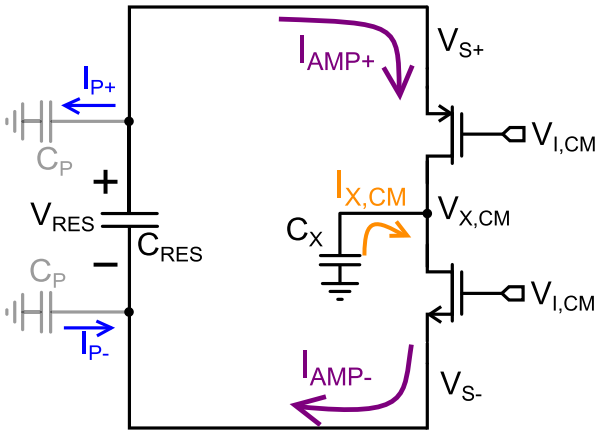

Fig. 8. Common-mode operation model with parasitic capacitance.

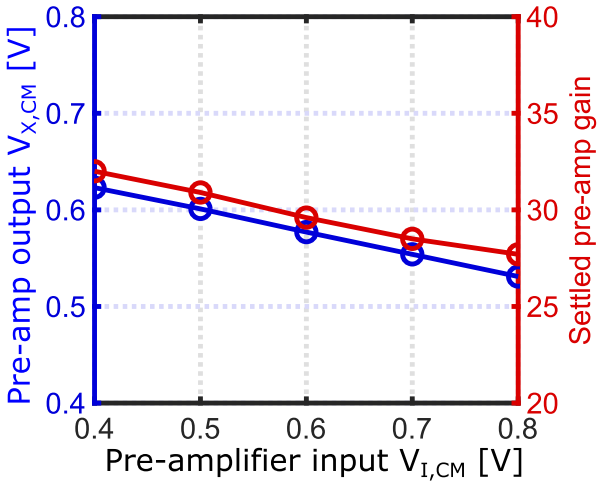

Fig. 9. Simulated pre-amplifier output common-mode voltage and gain as a function of the input common-mode voltage.

The energy consumption of the FIA operation is $(2 \cdot C_{\text{RES}} \cdot \Delta V_S \cdot V_{\text{DD}})$, leading to the energy efficiency representation as

$$\text{FoM}_{\text{FIA}} = 4nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{G_m}. \tag{21}$$

The energy efficiency improvement can be calculated as

$$\frac{\text{FoM}_{\text{SA}}}{\text{FoM}_{\text{FIA}}} = \frac{V_{\text{DD}}}{V_{\text{THN}}} \cdot \frac{(G_m/I_D)_{\text{FIA}}}{(g_m/I_D)_{\text{SA}}}. \tag{22}$$

Two major advantages of the proposed FIA are revealed in this equation when compared with the classic SA latch. The coefficient $(V_{\text{DD}}/V_{\text{THN}})$ comes from the avoidance of unnecessary full discharge of the integration capacitors C_X in the proposed FIA operation. In addition, the energy efficiency is proportional to G_m/I_D of the pre-amplifier, which is 2.5 times larger in the FIA, as shown in Fig. 4(c). With $V_{\text{DD}} = 1.2$ V and $V_{\text{TH}} \approx 0.55$ V in the typical corner, this theoretical analysis predicts a greater than five-time energy-efficiency improvement of the proposed FIA-based comparator over the conventional SA latch. Compared with the DB pre-amplifier [12], the proposed FIA doubles the energy-efficiency by realizing current reuse. In addition, given the higher integration gain provided in FIA, which attenuates the input-referred noise of the following latch, the proposed comparator can achieve an even larger overall energy efficiency improvement.

F. Parasitic Capacitance Impact

When C_{RES} is a perfect capacitor without any parasitic, the FIA works in an isolated voltage domain, and thus ensures the zero output common-mode change. In reality, with the parasitic capacitances, the output common-mode voltage can slightly change. To better analyze the parasitic effect, a model is shown in Fig. 8. In the prototype design, C_{RES} is implemented as a symmetric metal-on-metal (MoM) capacitor with equal parasitic capacitors on both plates.

The parasitic-induced common-mode rejection degradation can be derived through the current equation

$$I_{P+}(t) - I_{P-}(t) = I_{X,\text{CM}}(t). \tag{23}$$

It leads to a change in the output common-mode voltage

$$\Delta V_{X,\text{CM}}(t) = -(\Delta V_{S+}(t) + \Delta V_{S-}(t)) \cdot \frac{C_P}{C_X}. \tag{24}$$

Since the $\Delta V_{S+}/\Delta V_{S-}$ is proportional to the input common-mode voltage shift $\Delta V_{I,\text{CM}}$, the output common-mode voltage change can be approximated as

$$\Delta V_{X,\text{CM}} \approx -2 \cdot \Delta V_{I,\text{CM}} \cdot \frac{C_P}{C_X}. \tag{25}$$

With $C_P = 0$, there is no output common-mode voltage change, as pointed out in Section III-B. In this design, C_{RES} is implemented as a 2-pF MoM capacitor with the bottom layer of metal 2. The post-layout-extracted parasitics including routing is 1.5%. With $C_X \approx 250$ fF including the integration-node parasitics, the $\Delta V_{X,\text{CM}}$ is expected to be around 1/4 of the input common-mode voltage change. Comparing with the simple CMOS DB integration pre-amplifier presented in Section III-A, where the common-mode gain is around 20, the proposed FIA still achieves over 30-dB common-mode rejection ratio improvement.

To verify the output common-mode behavior with the parasitic impact, a post-layout simulation is shown in Fig. 9. With the input common-mode voltage varying from 0.4 to 0.8 V, the output common-mode has a variation below 100 mV, and the variation in the settled FIA gain is within 15%, which only has a limited impact on the comparator performance, as will be shown in the measurements.

IV. Proposed Comparator Design

As shown in Fig. 2, the proposed comparator consists of an FIA stage and a standard SA latch. During the reset phase (clk $= 0$), the reservoir capacitor C_{RES} is pre-charged to $V_{\text{DD}}/G_{\text{ND}}$, and the pre-amplifier output V_{X+}/V_{X-} is reset to $V_{\text{CM}} = V_{\text{DD}}/2$. When the comparison starts, the FIA performs dynamic integration ($\Phi_{\text{int}} = 1$). Once the SA latch resolves, the FIA is disabled to prevent the further discharge of C_{RES} to save energy ($\Phi_{\text{int}} = 0$).

The behavioral simulation is shown in Fig. 10. Unlike the SA latch, the integration nodes V_{X+}/V_{X-} are only partially discharged, which saves considerable energy. In addition, it also removes the bounded common-mode limitation and can provide a sufficiently large gain. With a pre-amplifier gain

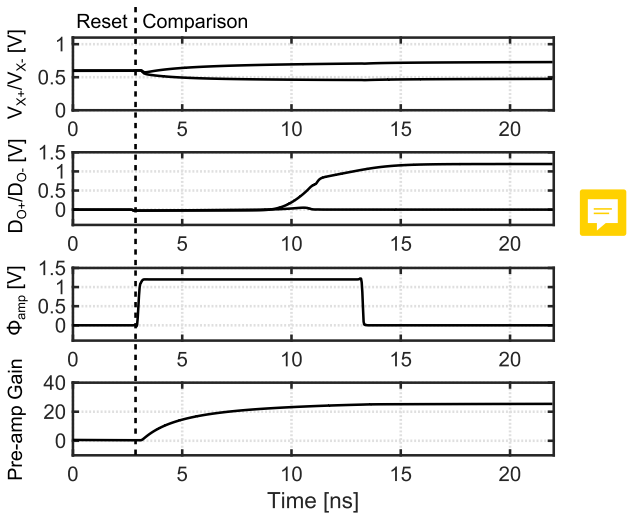

Fig. 10. Operation of the proposed comparator with FIA.

TABLE I
DEVICE SIZES

Transistor	Width [μm]	Length [μm]
M_1	44	0.18
M_2	44	0.18
M_3	22	0.18
M_4	22	0.18
Capacitor	**Size [pF]**	
C_X*	0.25	
C_{RES}	2	

*C_X includes the integration node parasitics

greater than 25, the noise contributed from the following latch is negligible.

Note that the V_{CM} only needs to replenish the charge loss caused by the output common-mode shift on the integration nodes during the reset phase. As indicated in (25), with the nominal input common-mode voltage input, there is no net charge consumption from the V_{CM}. Even with 200 mV in the input common-mode voltage shift, only 50-mV $\Delta V_{X,CM}$ is expected. In this case, the requirement of the V_{CM} buffer is relaxed. In this prototype design, V_{CM} is provided by an off-chip regulator for simple implementation.

There are several considerations in choosing the value of C_{RES}. The simulated CLK-Q delay in the comparator versus C_{RES} is shown in Fig. 11(a), and larger C_{RES} leads to faster preamplification, which increases the comparator speed. Although the theoretical energy efficiency (FoM) is independent of C_{RES}, as indicated by (21), in reality, they are still correlated, as shown in Fig. 11(b). If C_{RES} is too small, the preamplification gain is not large enough to suppress the latch stage noise, causing the degradation of comparator precision. While with larger C_{RES}, the dynamic bias effect is reduced, which diminishes the g_m/I_D boost. On the other hand, the larger C_{RES} will also bring area penalty. To better balance the tradeoffs among energy efficiency, comparison speed, and area consumption, a 2-pF C_{RES} is adopted in this design. Compared with an SA latch achieving the similar noise performance, the extra area overhead is around 30%. The device sizes in the prototype design are shown in Table I.

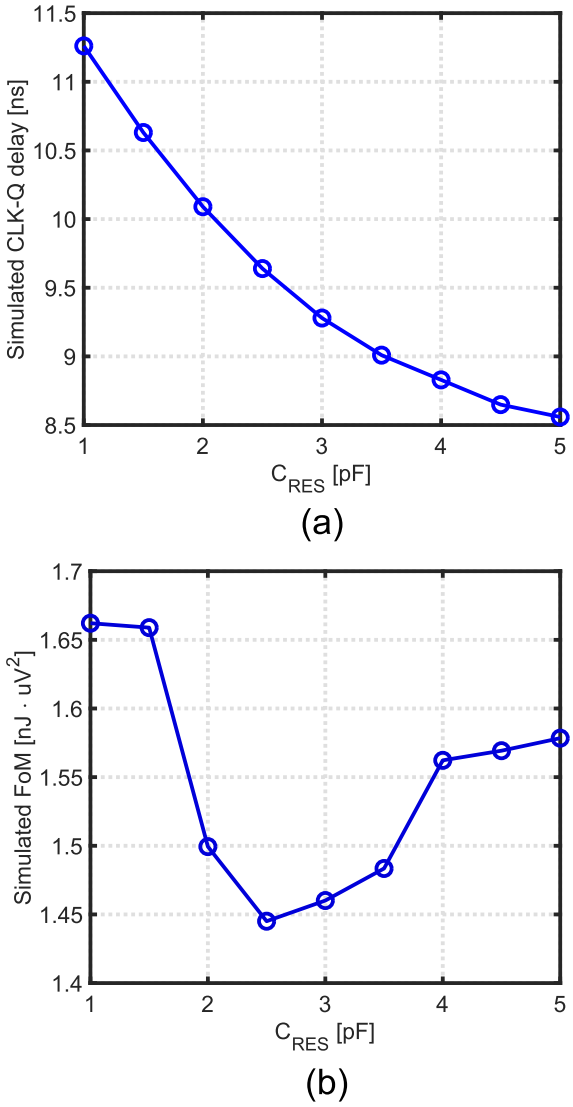

Fig. 11. Simulated (a) CLK-Q delay with 1-mV differential input and (b) energy efficiency of the proposed comparator versus C_{RES} value.

As our target application is mostly concerned with power efficiency instead of speed, the current sources in the comparators are scaled to achieve a low I_D while providing maximum G_m/I_D, at the cost of longer integration and regeneration times. The simulated CLK-Q delay versus the input common-mode voltage variation is shown in Fig. 12. With a low-input common-mode, the current in the SA latch, I_D, reduces greatly, thus significantly increasing the delay in the SA latch. For instance, with the input common-mode voltage decreases from 0.6 to 0.4 V, the simulated CLK-Q delay in the SA latch is increased by ten times. By contrast, the proposed comparator has only a small increase of 15%, which again attests its insensitivity to the input common-mode variation.

V. MEASUREMENT RESULTS

The prototype is fabricated in 180-nm CMOS, as shown in Fig. 13. To form a fair comparison, a stand-alone SA latch with two-time nMOS input pair size is also fabricated, which shares the same initial G_m as the FIA.

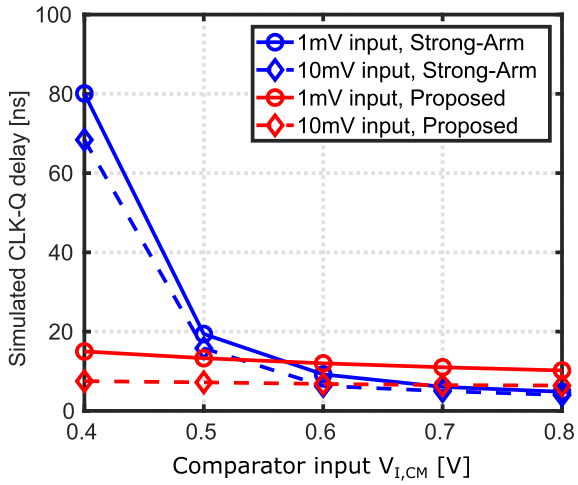

Fig. 12. Simulated CLK-Q delay versus input common-mode voltage.

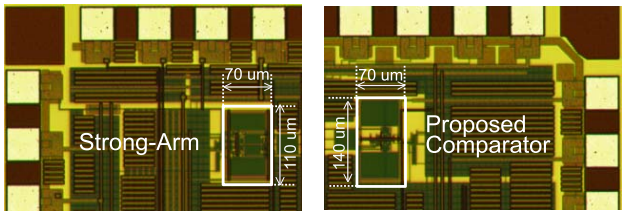

Fig. 13. Die micrograph of the SA latch and the proposed comparator.

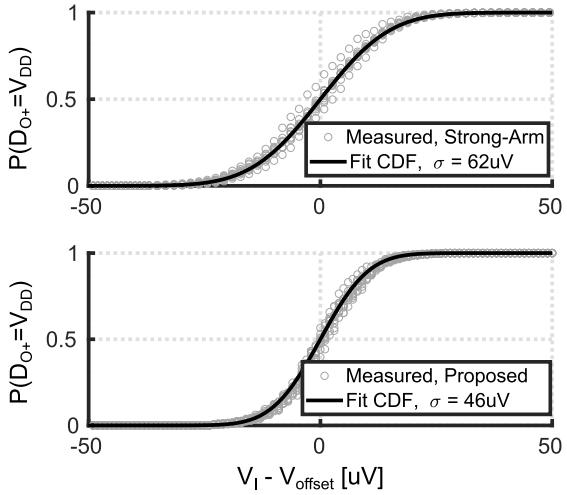

Fig. 14. Measured cumulative probability density distribution and fit to Gaussian distribution for proposed comparator and SA latch with 1.2-V supply and 0.6-V input common-mode voltage.

To measure the input-referred noise of both comparators, a dc input voltage V_I is applied. By firing the comparator with a large number of times (e.g., 10^5), the output probability can be calculated. This process is repeated for small increments (5 μV) in V_I to measure the accurate cumulative distribution functions (CDFs), as shown in Fig. 14. Fitting the measurement results to a Gaussian CDF, the comparator performance can be extracted. The measured rms input-referred noises are 62 μV for the SA latch and 46 μV for the proposed comparator with FIA.

Fig. 15 shows the measured comparator noise versus the input common-mode voltage. As for the SA latch, with higher input V_{CM}, larger $(V_{GS} - V_{TH})$ results in lower g_m/I_D for the nMOS input pair. Since the input-referred noise is inversely proportional to the g_m/I_D, as shown in (12), the noise is significantly larger with higher input common-mode voltage. By contrast, the input common-mode-insensitive operation of the FIA reduces the noise variation by four times. An input-referred offset measurement versus the input common-mode voltage is performed in Fig. 16, where the comparator inputs are supplied by two external DACs. By fine-tuning the DAC outputs until the comparator achieves 50% output probability, the aggregated system offset including the DACs and comparators is calibrated. In this measurement, all parts are calibrated at 0.6-V input common-mode voltage. The SA latch exhibits a 5.3-mV variation with ten parts measured, while the proposed work reduces the variation by greater than five times to 0.9 mV.

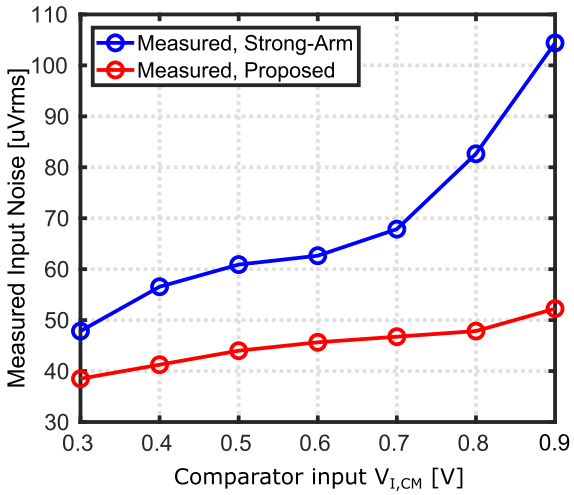

Fig. 15. Measured input-referred noise versus input common-mode voltage for the SA latch and proposed comparator.

Fig. 17 shows the energy consumption versus input differential voltage, highlighting the reduction in overall energy consumption for various input common-mode voltages. The energy consumption per comparison for the proposed comparator is approximately 0.98 pJ per comparison, whereas it is 4.1 pJ per comparison for the SA latch with 1-mV differential input at $V_{CM} = 0.6$ V. With the increase in the input common-mode voltage, the current I_D in the SA latch is raised, resulting in the increased energy consumption. Thanks to the input common-mode-insensitive operation, the proposed comparator consistently achieves greater than four-time energy reduction.

Table II summarizes the performance of the prototype design and compares it with the other state-of-the-art dynamic comparators. Noteworthy, to achieve the ten-time smaller noise performance than prior design in [11] and [12], the device sizes are much larger in the proposed work, resulting in larger area consumption. Compared with an SA latch that achieves similar noise performance, the proposed comparator has a 30% area overhead due to the C_{RES}. All these comparators are operated under 1.2-V supply voltage, which forms fair comparisons of energy efficiency. The proposed comparator with FIA achieves greater than seven-time improvement over

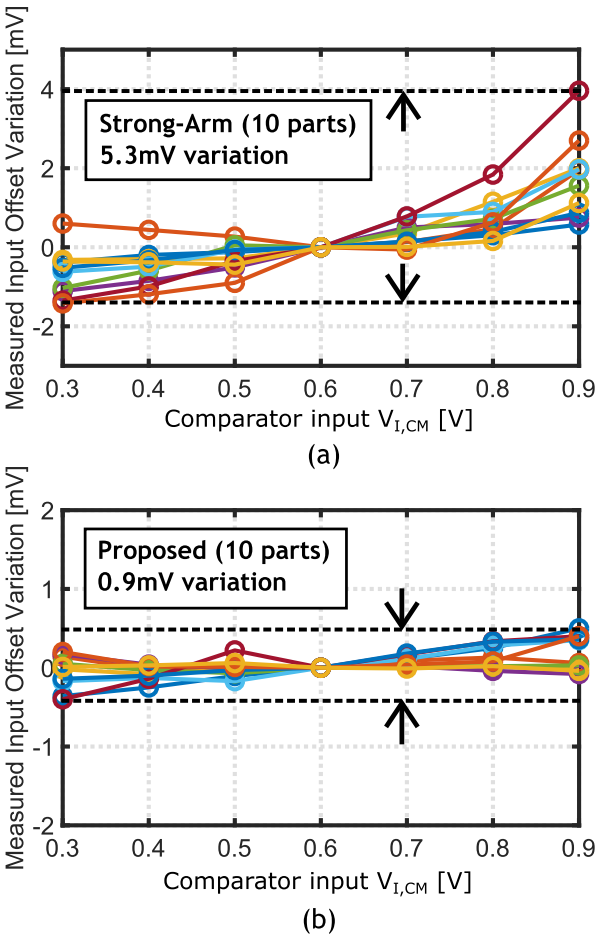

Fig. 16. Measured ten-part input-referred offset versus input CM voltage for (a) SA latch and (b) proposed comparator.

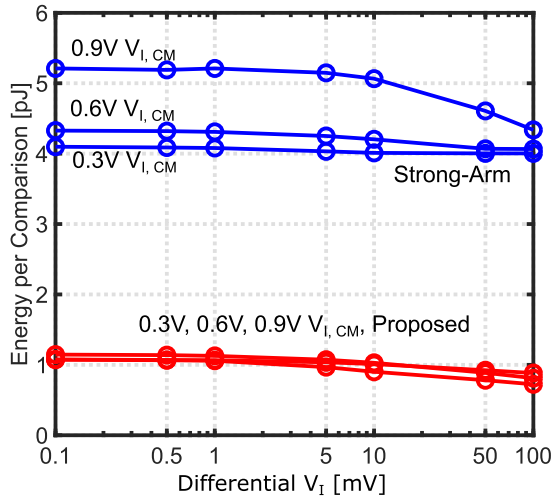

Fig. 17. Measured energy consumption versus input voltage for the SA latch and proposed comparator.

the classic SA latch and greater than 2.5-time improvement over the second best [12]. To the best of our knowledge, it is the most energy-efficient comparator reported to date. In addition, it has a reduced sensitivity to input common-mode voltage and process corner variations.

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART DYNAMIC COMPARATORS

	This Work		[12]		[11]
Featured Architecture	**Proposed FIA+SA**	Standard SA	Dynamic Bias	Double-Tail [10]	Double-Tail
Process [nm]	**180**	180	65	65	90
Supply [V]	**1.2**	1.2	1.2	1.2	1.2
Noise [μV]	**46**	62	400	450	1500
Energy [pJ]	**0.98**	4.1	0.034	0.088	0.113
Area [μm²]	**9800**	7700	125	90	82.5
FoM* [nJ·μV²]	**2.07**	15.8	5.44	17.8	254
Insensitive to Input CM voltage	**Yes**	No	No	No	No

*$FoM = Energy \cdot (NoisePower)$

VI. CONCLUSION

This article presents an energy-efficient dynamic comparator with a floating-inverter pre-amplifier. The proposed pre-amplifier realizes current reuse, boosts g_m/I_D, and prevents full discharge of the integration capacitors by the CMOS DB integration, thus significantly improving the energy efficiency. This pre-amplifier is powered by a floating reservoir capacitor, which provides an isolated voltage domain for the dynamic integration. With only differential input information sensed by the pre-amplifier, it achieves input common-mode and process corner robustness without a dedicated CMFB circuit. This article achieves the best energy efficiency, which represents more than 2.5-time improvement over the state of the art.

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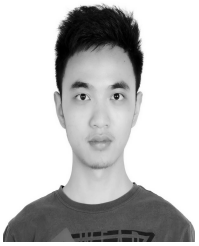

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