INTEGRATED CIRCUITS 1
LAB04

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Part 1: Sizing Chart

1) We can show that the intrinsic gain of a MOSFET is given by

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{V_A}{I_D} = \frac{2V_A}{V_{ov}}$$

Interestingly, the gain only depends on λ and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2V_A}{V^*}$$

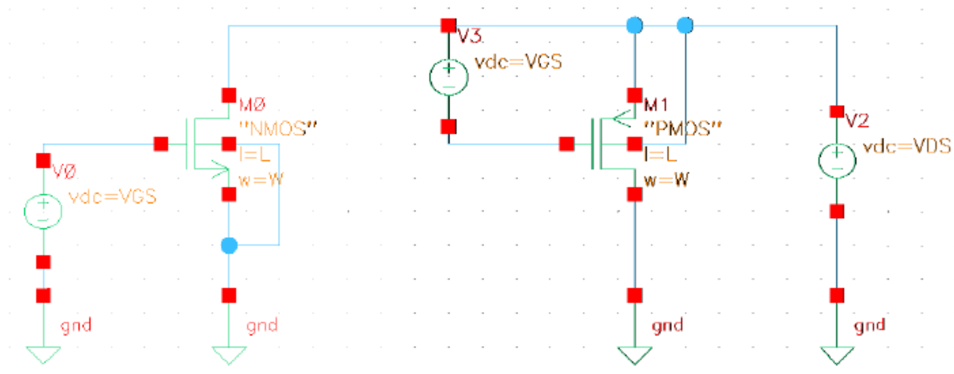
The lower the V^* the higher the gain, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) We want to design a CD amplifier with the parameters below.

Parameter	0.13um CMOS	0.18um CMOS
Input transistor	PMOS	PMOS
L	$1\mu m$	$1\mu m$
V^*	$200mV$	$200mV$
Supply	$1.2V$	$1.8V$
Current consumption	$10\mu A$	$10\mu A$

3) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation.

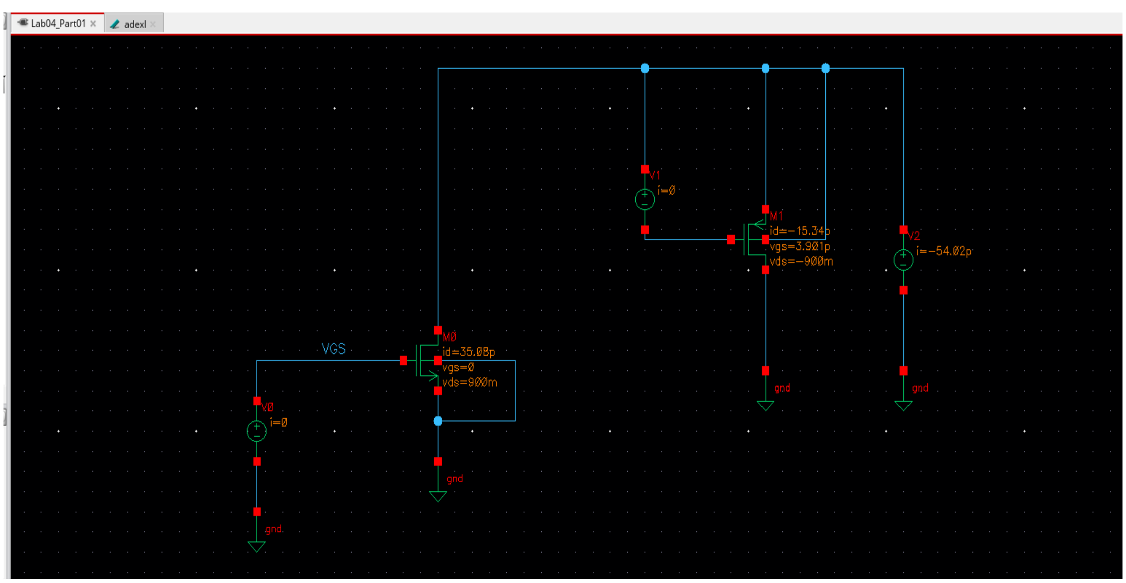
Create a testbench for PMOS transistor as shown below (we will use PMOS only in this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 1\mu m$ (the same L selected before).

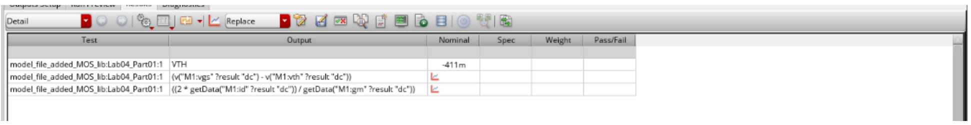


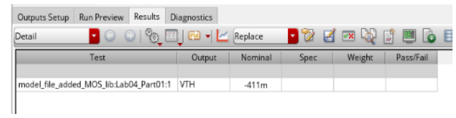
4) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
5) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. You can save the expressions to reuse them later.
6) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
7) An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$. On the V^* and V_{ov} chart locate the point at which $V^* = 200mV$. Find the corresponding V_{ovQ} and V_{GSQ}.
8) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
9) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 10\mu A$ as given in the specs. Calculate W as shown below.

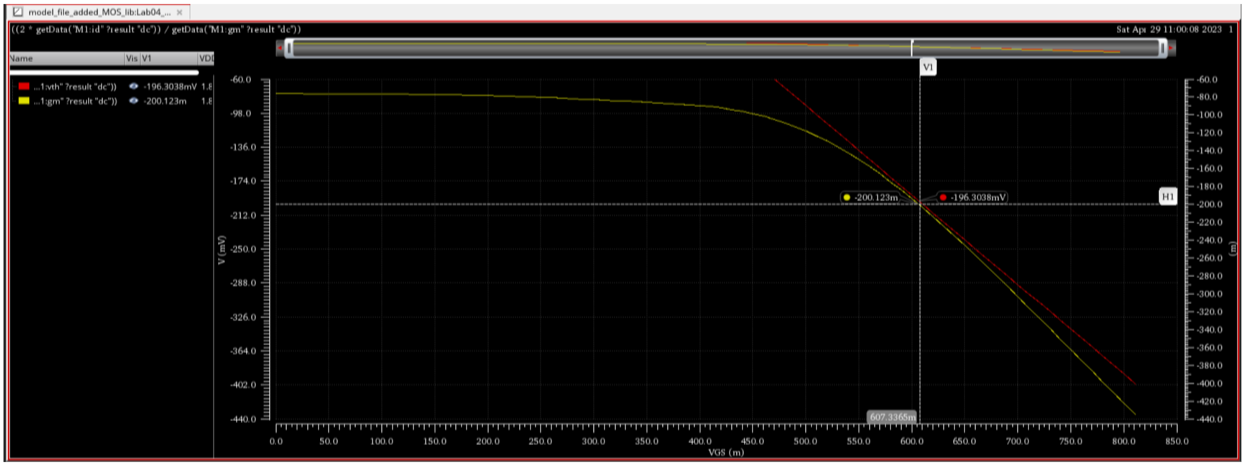
W	I_D
$10\mu m$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 10\mu A$ (from the specs)

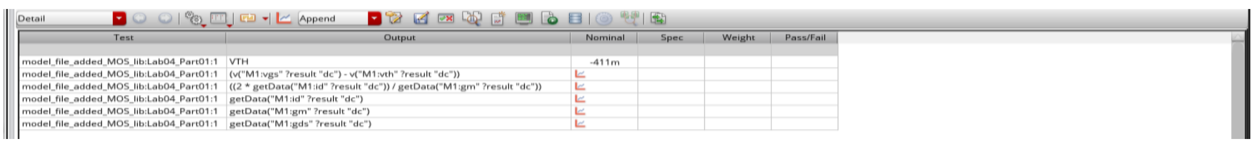
10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

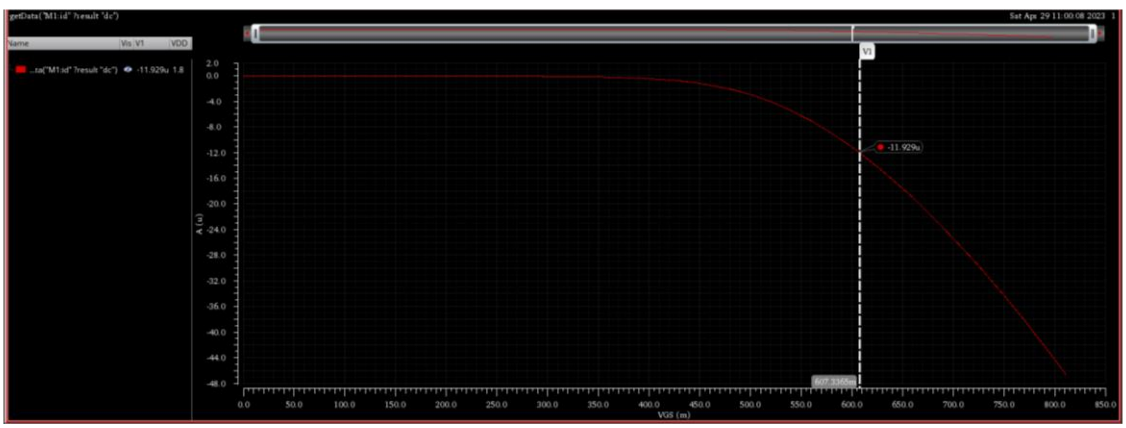


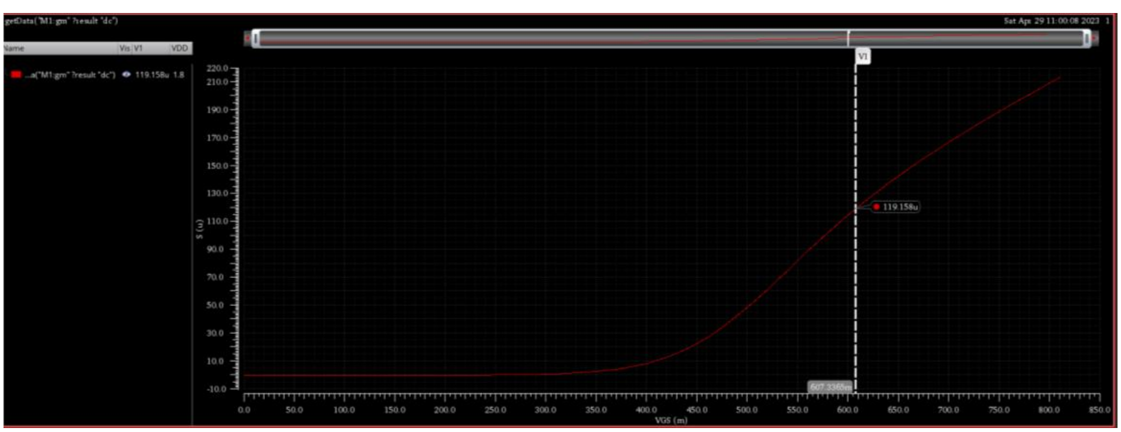

Detail
Replace
Test | Output | Nominal | Spec | Weight | Pass/Fail
model_file_added_MOS_lib:Lab04_Part01:1 | VTH | -411m
model_file_added_MOS_lib:Lab04_Part01:1 | (v("M1:vgs" ?result "dc") - v("M1:vth" ?result "dc"))
model_file_added_MOS_lib:Lab04_Part01:1 | ((2 * getData("M1:id" ?result "dc")) / getData("M1:gm" ?result "dc"))

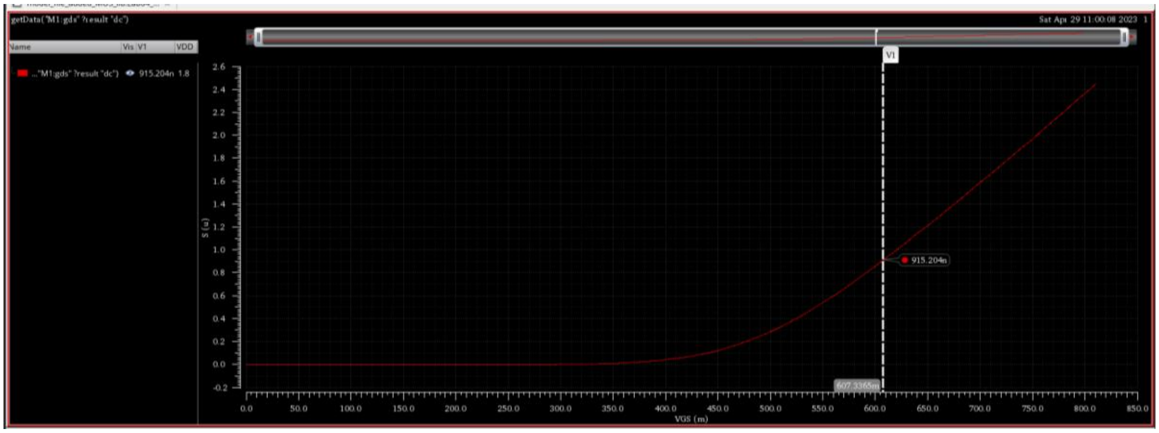

Outputs Setup
Run Preview
Results
Diagnostics
Detail
Replace
Test | Output | Nominal | Spec | Weight | Pass/Fail
model_file_added_MOS_lib:Lab04_Part01:1 | VTH | -411m


model_file_added_MOS_lib:Lab04_...
((2 * getData("M1:id" ?result "dc")) / getData("M1:gm" ?result "dc"))
Sat Apr 29 11:00:08 2023 1
Name | Vis | V1 | VDD
...1:vth" ?result "dc")) -196.3038mV 1.8
...1:gm" ?result "dc")) -200.123m 1.8
V1
H1
-200.123m
-196.3038mV
V (mV)
607.3365m
VGS (m)


Detail
Append
Test | Output | Nominal | Spec | Weight | Pass/Fail
model_file_added_MOS_lib:Lab04_Part01:1 | VTH | -411m
model_file_added_MOS_lib:Lab04_Part01:1 | (v("M1:vgs" ?result "dc") - v("M1:vth" ?result "dc"))
model_file_added_MOS_lib:Lab04_Part01:1 | ((2 * getData("M1:id" ?result "dc")) / getData("M1:gm" ?result "dc"))
model_file_added_MOS_lib:Lab04_Part01:1 | getData("M1:id" ?result "dc")
model_file_added_MOS_lib:Lab04_Part01:1 | getData("M1:gm" ?result "dc")
model_file_added_MOS_lib:Lab04_Part01:1 | getData("M1:gds" ?result "dc")


getData("M1:id" ?result "dc")
Sat Apr 29 11:00:08 2023 1
-11.929u
A (u)
607.3365m
VGS (m)


getData("M1:gm" ?result "dc")
Sat Apr 29 11:00:08 2023 1
119.158u
S (u)
607.3365m
VGS (m)



We will operate on The 0.18 um CMOS

	PMOS
L	1 μm
V^*	200 mV
Supply	1.8 V
Current Cons.	10 μA

from the Simulation $V_{tp} = -411$ mV

from the plot at $V^* = -200.123$ mV

$V_{GS_Q} = 607.3365$ mV

$V_{ov_Q} = -196.3038$ mV

$I_{D_X} = -11.929$ uA

$g_{m_X} = 119.158$ uS

$g_{ds_X} = 915.204$ uS

W	I_D
10 μm	11.929 uA
?	10 μA

$\therefore W = 8.3829$ μm

$g_m \propto W \qquad \frac{g_{m_1}}{g_{m_Q}} = \frac{W_1}{W}$

$$g_{m_Q} = \frac{119.158 \times 8.3829}{10} = 99.888\ \mu S$$

$$g_{ds} \propto W \quad \therefore g_{ds_Q} = \frac{g_{ds_1} \cdot W}{W_1} = \frac{915.204 \times 8.3829}{10} = 767.206\ \mu S$$

Parameters Resulting from the sizing chart

- $I_{DQ} = 10$ μA
- $g_{mQ} = 99.888$ μS
- $g_{dsQ} = 767.206$ μS
- $r_o = 1303.4\ \Omega$
- $W = 8.3829$ μm
- $L = 1$ μm
- Supply Voltage = 1.8 V
- $V^* = 200$ mV
- $|V_{ovQ}| = 196.3$ mV
- $* \ V_{GSQ} = 607.3365$ mV

PART 2: CD Amplifier

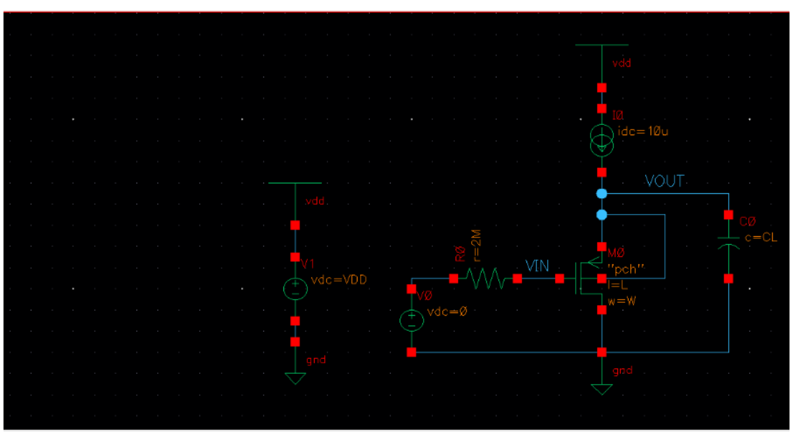
1. OP (Operating Point) Analysis

1) Create a new schematic for the CD amplifier (the schematic is not included in the lab document and is left for the student as an exercise). Use a PMOS and use a $10\mu A$ ideal current source for biasing (note that the current source will be connected to the source terminal). Connect the source to the bulk. Use $L = 1\mu m$ and W as determined in Part 1. Use $C_L = 2pF$, $R_{sig} = 2M\Omega$, and a DC input voltage = 0V.

2) Simulate the OP point. Report a snapshot clearly showing the following parameters (add a filter to your monitor).

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

3) Check that the transistor operates in saturation.



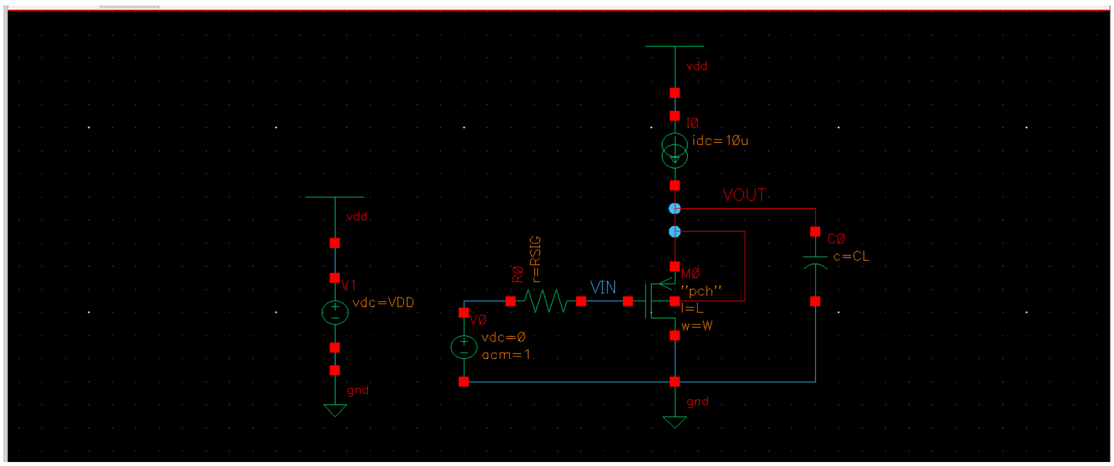
Test	Output	Nominal	Spec	Weight	Pass/Fail
model_file_added_MOS_lib:Lab04_Part02:1	ID	-10u			
model_file_added_MOS_lib:Lab04_Part02:1	VGS	-609.9m			
model_file_added_MOS_lib:Lab04_Part02:1	VDS	-609.9m			
model_file_added_MOS_lib:Lab04_Part02:1	VTH	-411m			
model_file_added_MOS_lib:Lab04_Part02:1	VDSAT	-166.1m			
model_file_added_MOS_lib:Lab04_Part02:1	GM	99.25u			
model_file_added_MOS_lib:Lab04_Part02:1	GDS	819.7n			
model_file_added_MOS_lib:Lab04_Part02:1	GMB	31.93u			
model_file_added_MOS_lib:Lab04_Part02:1	CDB	-6.687f			
model_file_added_MOS_lib:Lab04_Part02:1	CGD	-5.526f			
model_file_added_MOS_lib:Lab04_Part02:1	CGS	-56.73f			
model_file_added_MOS_lib:Lab04_Part02:1	CSB	-22.81f			
model_file_added_MOS_lib:Lab04_Part02:1	REGION	2			

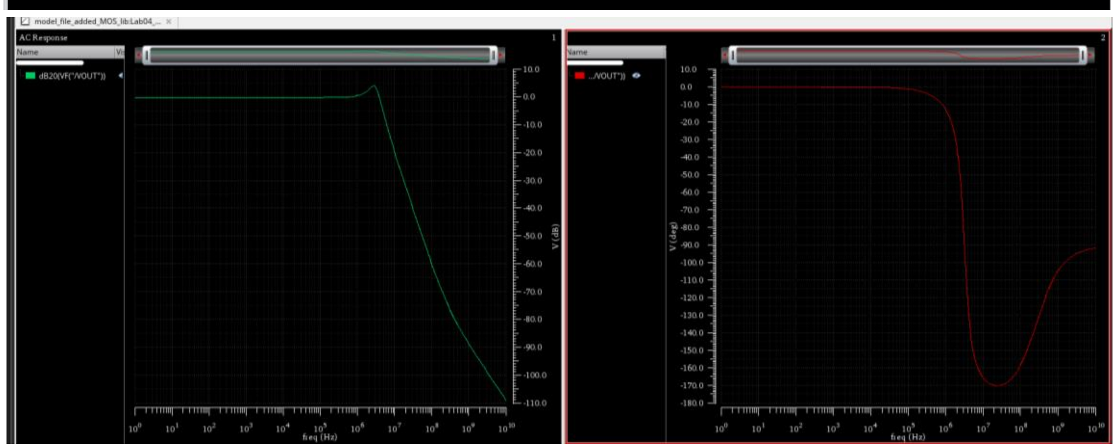
1- OP Analysis:

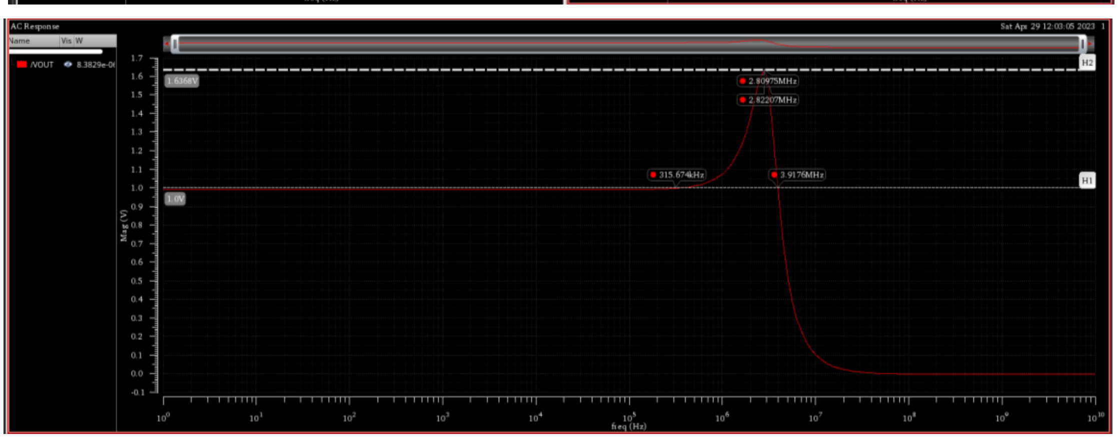
3- As we can see, the transistor is in Region 2 thus operates in saturation.

2. AC Analysis

1) Perform AC analysis (1Hz:10GHz, logarithmic, 20points/decade) to investigate the frequency domain peaking.
2) Report the Bode plot magnitude.
3) Do you notice frequency domain peaking?
   ➔ Cadence Hint: Use the following expression to calculate the peaking in dB: ymax(dB20(VF("/vout")))
4) Analytically calculate quality factor (use approximate expressions). Is the system underdamped or overdamped?
5) (Optional) Perform parametric sweep: CL = 2p, 4p, 8p.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs CL.
   - Comment.
6) (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs Rsig.
   - Comment.







2- AC Analysis

3) frequency isp peaking after it has settled in the mid band gain

peaking occurs from 315.674 KHz to 3.9176 MHz

The peak gain which is 1.638 v/v occurs at 2.815 MHz

Test	Output	Nominal	Spec	Weight	Pass/Fail
model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	4.287			
model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	1.638			

4)

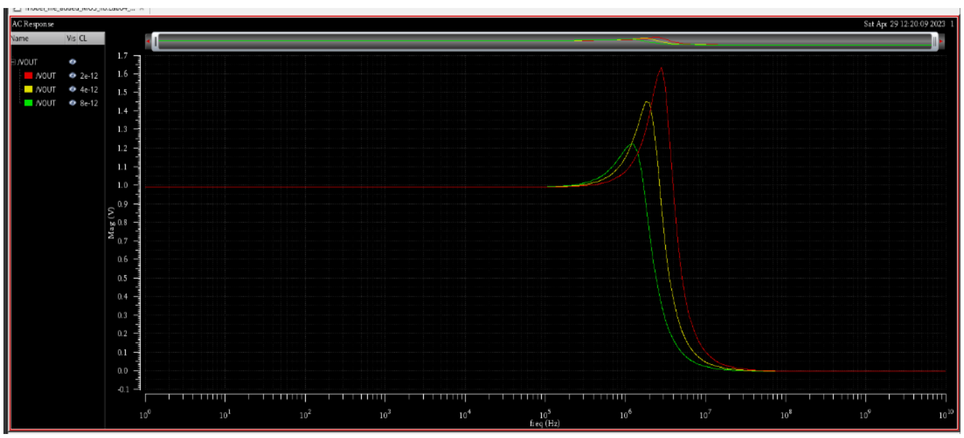
we can analitically calculate the Quality factor by

$$Q = \sqrt{\frac{g_m (C_{gs} + C_{gd}) R_{sig}}{C_L}}$$

$$Q = \sqrt{\frac{99.25 \times 10^{-6} [56.73 + 5.52] \times 10^{-15} \times 2 \times 10^{6}}{2 \times 10^{-12}}}$$

$Q = 2.485 > 0.5$ which means that the system is underdamped

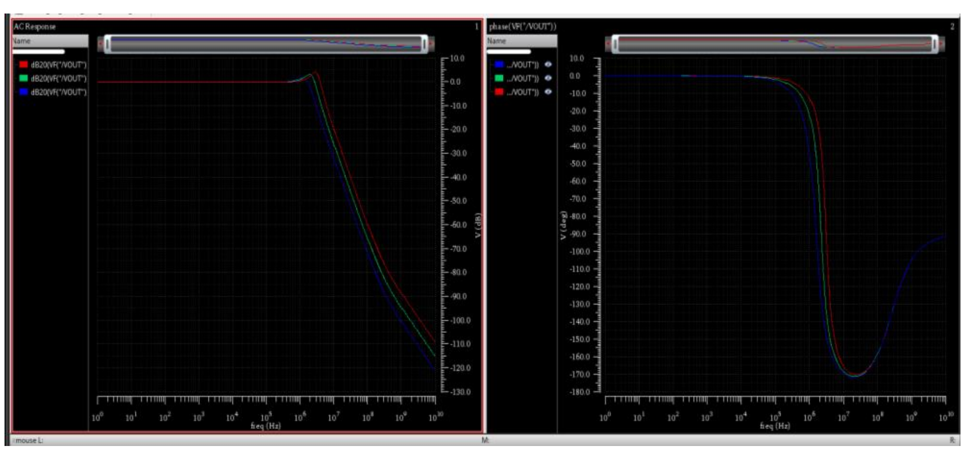
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: CL=2p						
1	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
1	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	4.287			
1	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	1.638			
Parameters: CL=4p						
2	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
2	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	3.235			
2	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	1.451			
Parameters: CL=8p						
3	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
3	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	1.75			
3	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	1.223			



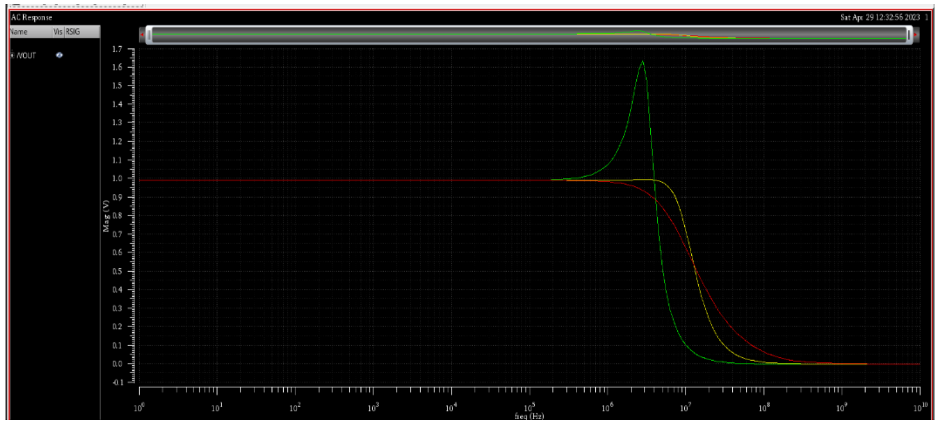
5) Comment; the as C_L increases the peak value decrease and the region or the Range where the Ringing occurs decreases

The Reason for the peaking is the Ringing effect there is a strong interaction between the input and output as they are close to each other

So by increasing C_L, the output pole decreases The distance between the two poles ↳ dominant Pole ~~decrease~~ increases thus Ringing effect decreases and the peaking decreases (value and Range)



Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
arameters: RSIG=20k						
1	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
1	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	-71.44m			
1	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	991.8m			
arameters: RSIG=200k						
2	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
2	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	-36.68m			
2	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	995.8m			
arameters: RSIG=2M						
3	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
3	model_file_added_MOS_lib:Lab04_Part02:1	ymax(dB20(VF("/VOUT")))	4.287			
3	model_file_added_MOS_lib:Lab04_Part02:1	ymax(mag(VF("/VOUT")))	1.638			

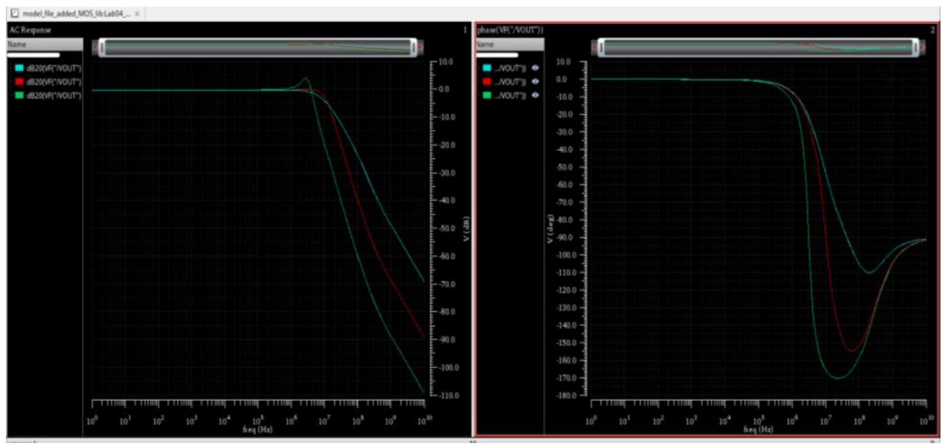


6) as Rsig increase, Peaking (Value and Range) increases, because the non-dominant pole at the input will decrease and thus approach the dominant pole at the output and this will increase the Ringing effect and thus peaking will increase

$\omega_{P_{out}}$ $\omega_{P_{in}}$

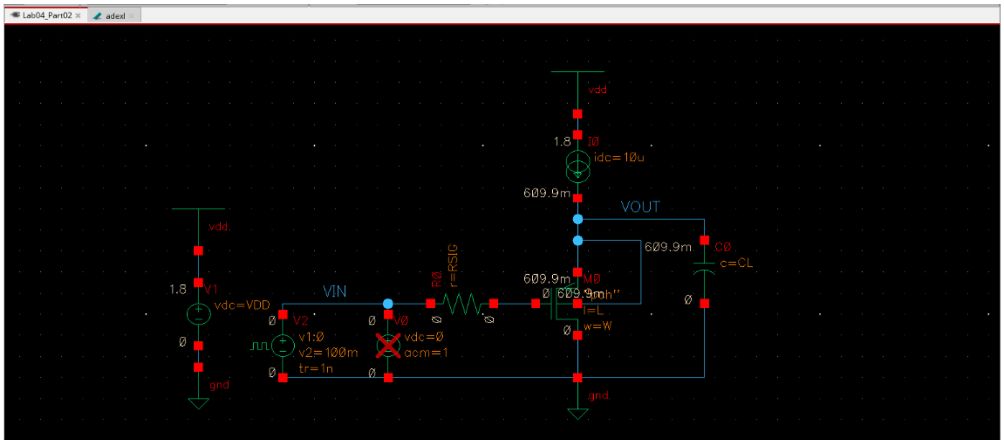
as CL increases

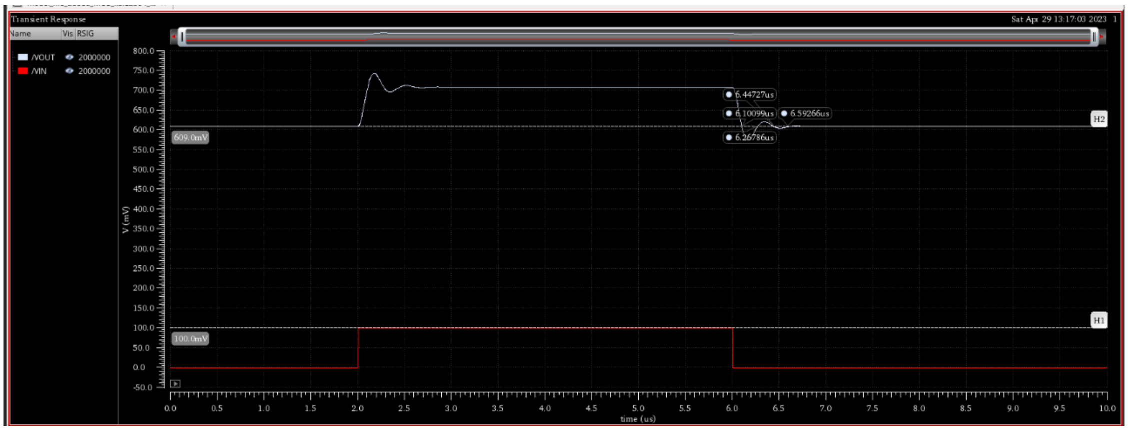
as Rsig increases



3. Transient Analysis

1) Use a pulse source (pulse_v_source) as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis (max step = 10n) for 10us to investigate the time domain ringing.
2) Report Vin and Vout overlaid vs time.
3) Calculate the DC voltage difference (DC shift) between Vin and Vout.
    - What is the relation between the DC shift and VGS?
    - How to shift the signal down instead of shifting it up?
4) Do you notice time domain ringing?
    ➔ Cadence Hint: Use the overshoot function to calculate the maximum overshoot as a percentage
5) (Optional) Perform parametric sweep: CL = 2p, 4p, 8p.
    - Report Vout vs time overlaid on same plot.
    - Report the overshoot vs CL.
    - Comment.
6) (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.
    - Report Vout vs time overlaid on same plot.
    - Report the overshoot vs Rsig.
    - Comment.





3) transient analysis :

3- The Dc shift between V_{in} and V_{out} Can be found from the Dc annotations to be 609.9 mV

→ The Dc shift is equal to V_{GS}

$V_{out_{DC}} = V_S \qquad V_{in_{DC}} = V_G$

$(V_{out} - V_{in})_{DC} = |V_{GS}|$

shift up ⇐ $\boxed{V_{out} = V_{SG} + V_{in}}$

→ to shift the Signal down instead of shifting it up

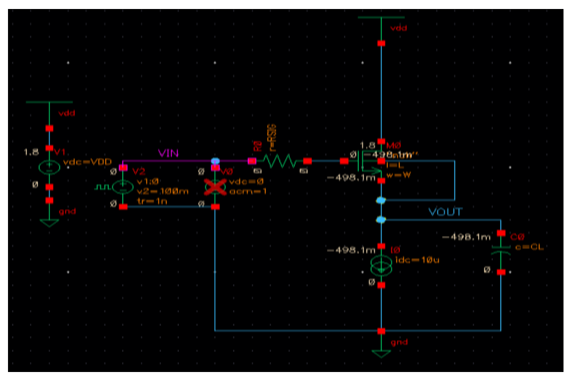
so we need:

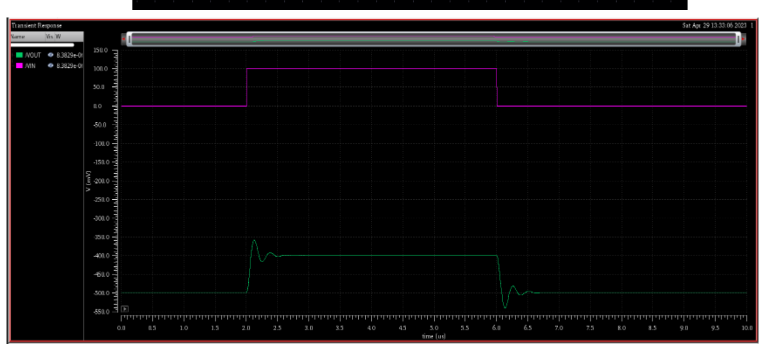
$\boxed{V_{in} = V_{GS} + V_{out}}$

Shift down ⇐ $V_{out} = V_{in} - V_{GS}$

Thus we need to use an NMOS with Current Source Conned to Source [Current sink]

→ I have also plotted the two signals together without the Dc shift





4) Yes, There is Ringing
overshoot percentage is 34.78 %

Test	Output	Nominal	Spec	Weight	Pass/Fail
model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609 nil 0.709 nil nil "time")	34.78			

5) Comment :

As cl increase peak overshoot decrease for the same reason that has stated earlier in AC analysis.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: CL=2p						
1	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
1	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
1	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	34.78			
Parameters: CL=4p						
2	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
2	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
2	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	28.85			
Parameters: CL=8p						
3	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
3	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
3	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	19.34			

6) Comment

As Rsig increase peak overshoot increase for the same reasons discussed earlier in AC analysis.

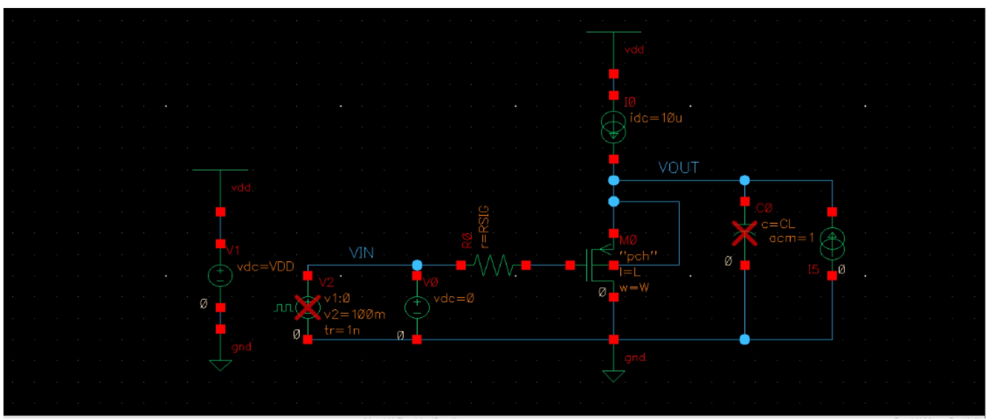
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: RSIG=20k						
1	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
1	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
1	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	34.65m			
Parameters: RSIG=200k						
2	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
2	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
2	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	5.418			
Parameters: RSIG=2M						
3	model_file_added_MOS_lib:Lab04_Part02:1	/VOUT				
3	model_file_added_MOS_lib:Lab04_Part02:1	/VIN				
3	model_file_added_MOS_lib:Lab04_Part02:1	overshoot(VT("/VOUT") 0.609...	34.78			

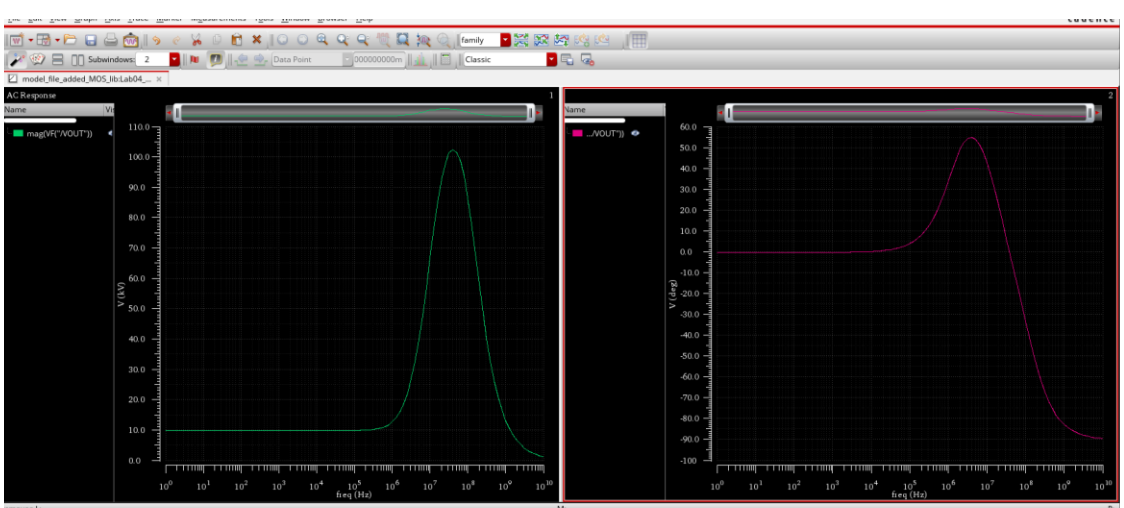
4. Z_{out} (Inductive Rise) (optional)

   1) We want to simulate the CD amplifier output impedance. Replace CL with an AC current source with magnitude = 1. Remove the AC input signal.
   2) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade). The voltage across the AC current source is itself the output impedance.
   3) Plot the output impedance (magnitude and phase) vs frequency. Do you notice an inductive rise? Why?
   4) Does Z_{out} fall at high frequency? Why?
      Hint: C_{gd} appears in parallel with R_{sig}.
   5) Analytically calculate the zeros, poles, and magnitude at low/high frequency for Z_{out}. Compare with simulation results in a table.

5. How to solve the peaking/ringing problem? (optional)

   1) Place the input/output poles away from each other (as we did when we swept CL and Rsig).
   2) (This part is optional) A compensation network can be used to compensate for the negative input impedance and prevent overshoots. Read [Johns and Martin, 2012] Section 4.4 and try to implement the compensation network.





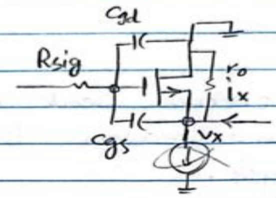
4)

Zout Inductive Rise:

3) Yes. There is an inductive rise

why ??

$$i_x = \frac{V_x}{R_{sig} + \frac{1}{sC_{gs}}} + g_m x$$



$$\frac{V_x}{R_{sig} + \frac{1}{sC_{gs}}} \times \frac{1}{sC_{gs}}$$

$g_{mb} V_x = i_x$

$\frac{V_x}{i_x} = \frac{1}{g_{mb}}$

$$\therefore \quad Z_{out} = \frac{1 + sR_{sig}C_{gs}}{1 + \frac{C_{gs}}{g_m}s} \cdot \frac{1}{g_m}$$

at low freq. $Z_{out} \simeq \frac{1}{g_m}$

at high freq. $Z_{out} \simeq R_{sig}$.

$(\frac{1}{g_{mb}})$ body resistance and r_o add to Zout in parallel

$$Z_{out} = \frac{1}{g_m}\left(\frac{1 + sR_{sig}C_{gs}}{1 + C_{gs}/g_m s}\right) // r_o // \frac{1}{g_{mb}}$$

Thus by increasing frequency There would be an inductive rise in Zout until it falls

4) Zout fall at very high frequencies

notice that C_{gd} is parallel to R_{sig}. $\simeq \frac{1}{R_{sig} \cdot C_{gd}}$ at high frequencies

$$R_{eq} = \frac{R_{sig} \cdot \frac{1}{sC_{gd}}}{R_{sig} + \frac{1}{sC_{gd}}} = \frac{R_{sig}}{sR_{sig}C_{gd} + 1}$$

at low freq. to moderate $\Rightarrow R_{eq} \simeq R_{sig}$.

at high freq. $R_{eq} \simeq \frac{R_{sig}}{sR_{sig}C_{gd} + 1} \rightsquigarrow \frac{\cancel{R_{sig}} \, 1}{R_{sig}C_{gd}}$

which Causes a drop in The output impedance $\frac{1}{sC_{gd}}$

Since C_{gd} is very small and Thus it takes over

5) $Z_{out} = \cancel{1 + S R_{sig}}$

$$= \frac{1 + S R_{eq} C_{gs}}{g_m + S C_{gs}} \parallel r_o \parallel \frac{1}{g_{mb}}$$

$$Z_{out} = \frac{1}{\frac{g_m + S C_{gs}}{1 + S R_{eq} C_{gs}} + \frac{1}{r_o} + g_{mb}}$$

$$Z_{out} = \frac{1 + S R_{eq} C_{gs}}{g_m + S C_{gs} + \frac{1}{r_o} + \frac{S R_{eq} C_{gs}}{r_o} + g_{mb} + g_{mb} S R_{eq} C_{gs}}$$

$$Z_{out} = \frac{1 + S R_{eq} C_{gs}}{S\left(C_{gs} + \frac{R_{eq} C_{gs}}{r_o} + g_{mb} R_{eq} C_{gs}\right) + \left(g_m + \frac{1}{r_o} + g_{mb}\right)}$$

$$R_{eq} = \frac{R_{sig}}{S R_{sig} C_{gd} + 1}$$

$$Z_{out} = \frac{1 + S C_{gs} \cdot \frac{R_{sig}}{S R_{sig} C_{gd} + 1}}{S C_{gs} + S\left(\frac{C_{gs}}{r_o} + g_{mb} C_{gs}\right) \cdot \frac{R_{sig}}{S R_{sig} C_{gd} + 1} + \left(g_m + \frac{1}{r_o} + g_{mb}\right)}$$

$$Z_{out} = \frac{S R_{sig} C_{gd} + 1 + S C_{gs} R_{sig}}{S^2 R_{sig} C_{gs} C_{gd} + S C_{gs} + S\left[\frac{C_{gs}}{r_o} + g_{mb} C_{gs}\right] R_{sig} + \left[g_m + g_{mb} + \frac{1}{r_o}\right] + S R_{sig} C_{gd}\left(g_m + g_{mb} + \frac{1}{r_o}\right)}$$

$$Z_{out} = \frac{S R_{sig}(C_{gd} + C_{gs}) + 1}{S^2 R_{sig} C_{gs} C_{gd} + S\left[C_{gs} + R_{sig} C_{gs}\left[\frac{1}{r_o} + g_{mb}\right] + R_{sig} C_{gd}\left(g_m + \frac{1}{r_o} + g_{mb}\right)\right] + \left(g_m + g_{mb} + \frac{1}{r_o}\right)} \Rightarrow$$

$$f_z = \frac{1}{2\pi} \times \frac{1}{R_{sig}(C_{gd}+C_{gs})} = \boxed{1.278 \text{ MHz}}$$

we will use dominant pole approx.

$$\omega_{Pd} = \frac{g_m + g_{mb} + 1/r_o}{C_{gs} + R_{sig}C_{gs}[1/r_o + g_{mb}] + R_{sig}C_{gd}[g_m + g_{mb} + 1/r_o]}$$

1.31979×10^{-4}

3.7713×10^{-17}

1.14586×10^{-12}

$R_{sig} = 2 \times 10^{6}\ \Omega$

$g_m = 99.24 \times 10^{-6}\ S$

$g_{mb} = 31.92 \times 10^{-6}\ S$

$g_{ds} = 819.5 \times 10^{-9}\ S$

$C_{gs} = 56.73 \times 10^{-15}\ F$

$C_{gd} = 5.526 \times 10^{-15}\ F$

$\therefore f_{Pd} = 4.0183$ MHz

Discussing the denominator of Zout:

$$s^2 \times (6.269 \times 10^{-22}) + s(5.2299 \times 10^{-12}) + 1.3197 \times 10^{-4} = 0$$

$$s^2 (6.269 \times 10^{-12}) + 5.2299\, s + 1.3197 \times 10^{8} = 0$$

$\omega_{P_1} = -25234515.38$ rad/sec $\quad \omega_{P_2} = -8.3422 \times 10^{11}$ rad/

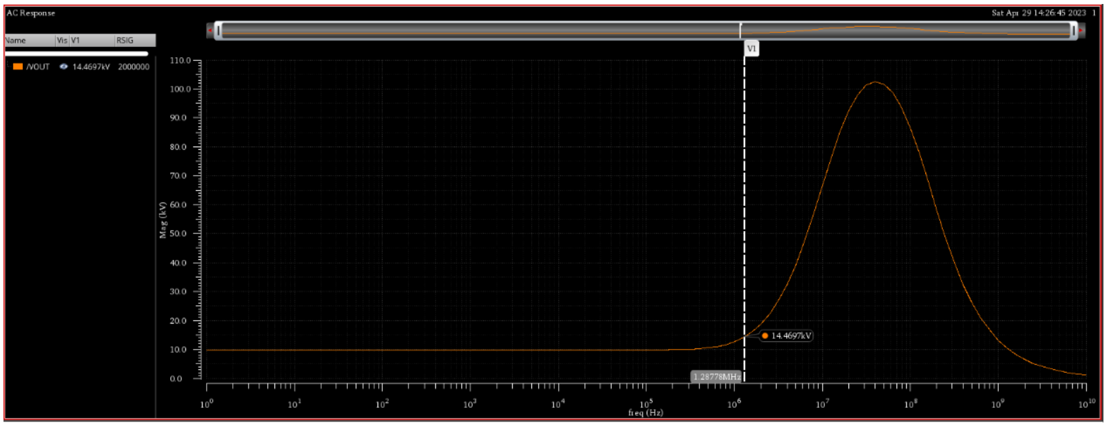
$\boxed{f_{Pd} = 4.01823 \text{ MHz}}$ $\quad \boxed{f_{Pnd} = 1.32837 \times 10^{11} \text{ Hz}}$

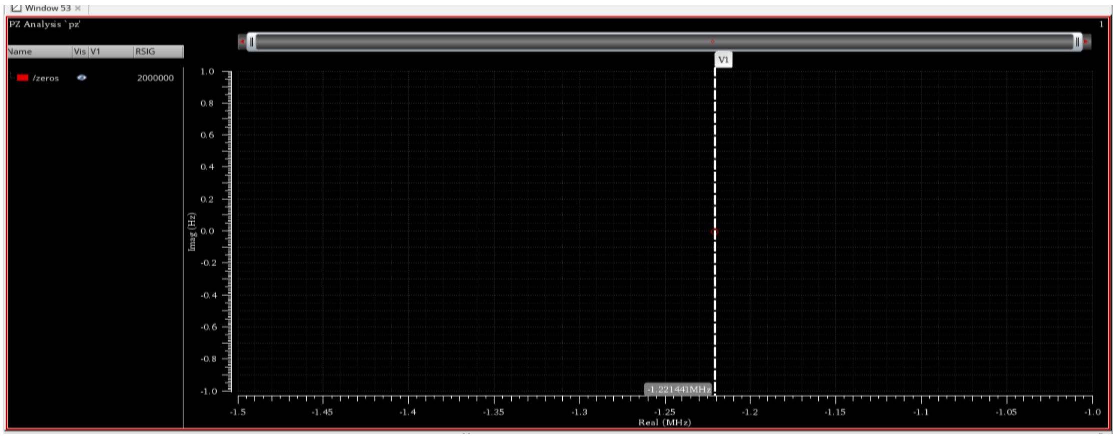
	Analytically	Simulation
Zeros	1.278 MHz	1.22144 MHz
Poles	4.0183 MHz – 1.328×10^{11} MHz	14.13 MHz – 117.99 MHz

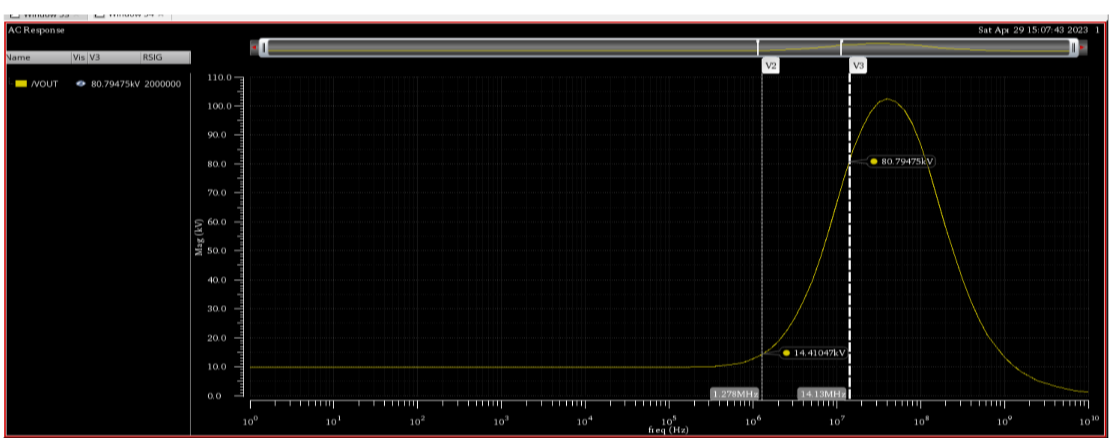
dominant

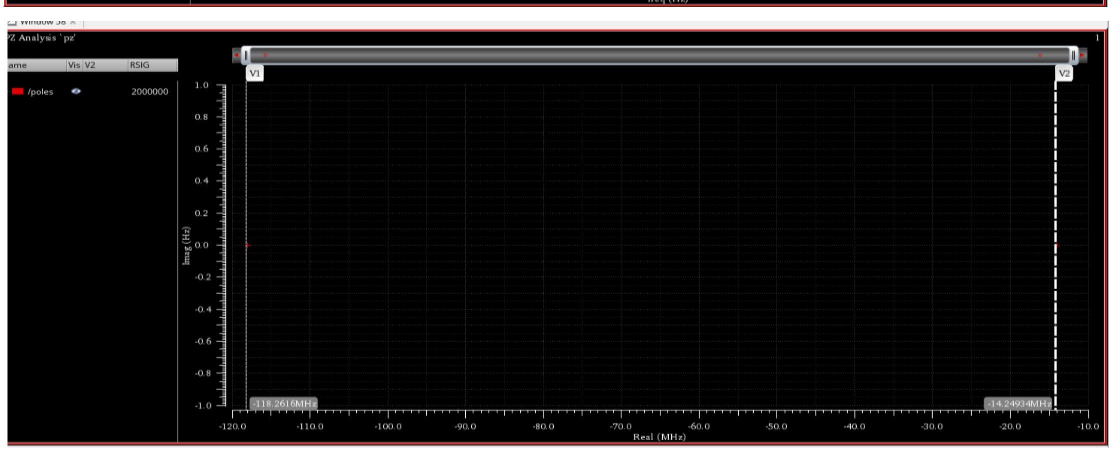
There is an error with my hand calculation

Could be a mistake in the numbers


AC Response
Sat Apr 29 14:26:45 2023
/VOUT 14.4697kV 2000000
V1
14.4697kV
1.28778MHz
Mag (kV)
freq (Hz)


PZ Analysis `pz'
/zeros 2000000
V1
-1.221441MHz
Imag (Hz)
Real (MHz)


AC Response
Sat Apr 29 15:07:43 2023
/VOUT 80.79475kV 2000000
V2
V3
80.79475kV
14.41047kV
1.278MHz
14.13MHz
Mag (kV)
freq (Hz)


PZ Analysis `pz'
/poles 2000000
V1
V2
-118.2616MHz
-14.24934MHz
Imag (Hz)
Real (MHz)

The End