

*Design a Common Source Amplifier meets the following specs use PMOS input trans.*

Spec.	
DC Gain	10 dB
BW	$\geq 3$ GHz
Power Consumption	$\leq 1.2$ mW
Cap Load	50 fF

No we will operate on The 65 nm PDK  
on Cadence

$$\text{DC gain} = 10 \text{ dB} \rightarrow 3.2 \text{ V/V}$$

$$\text{BW} \geq 3 \text{ GHz}$$

$$\text{Power Cons.} \leq 1.2 \text{ mW}$$

$$\text{Cap Load} = 50 \text{ fF}$$

$$\text{GBW} \geq 3.2 \times 3 \text{ GHz}$$

$$g_m \geq 3.2 \times 3 \text{ GHz}$$

$$2\pi \text{Cont}$$

$$g_m \geq 3 \text{ ms}$$

$$\text{take } V_{DD} = 1.2 \text{ V}$$

$$\text{and } V_{DS} = \frac{V_{DD}}{2} = 0.6 \text{ V}$$

$$P \leq 1.2 \text{ mW} \quad V_{DD} I_D \leq 1.2 \text{ mW} \quad \therefore I_D \leq 1 \text{ mA}$$

$$\therefore R_D = \frac{0.6}{1 \text{ mA}} = 600 \, \Omega$$

$$\frac{g_m}{I_D} = 3 \quad \text{for Margin let } g_m = 6 \text{ ms}$$

$$\therefore g_{\text{ain}} = g_m R_{\text{out}}$$

$$3.2 = 6 \times 10^{-3} R_{\text{out}} \quad \therefore R_{\text{out}} = 533.3 \, \Omega$$

$$\therefore \text{let } R_{\text{out}} = 540 \, \Omega$$

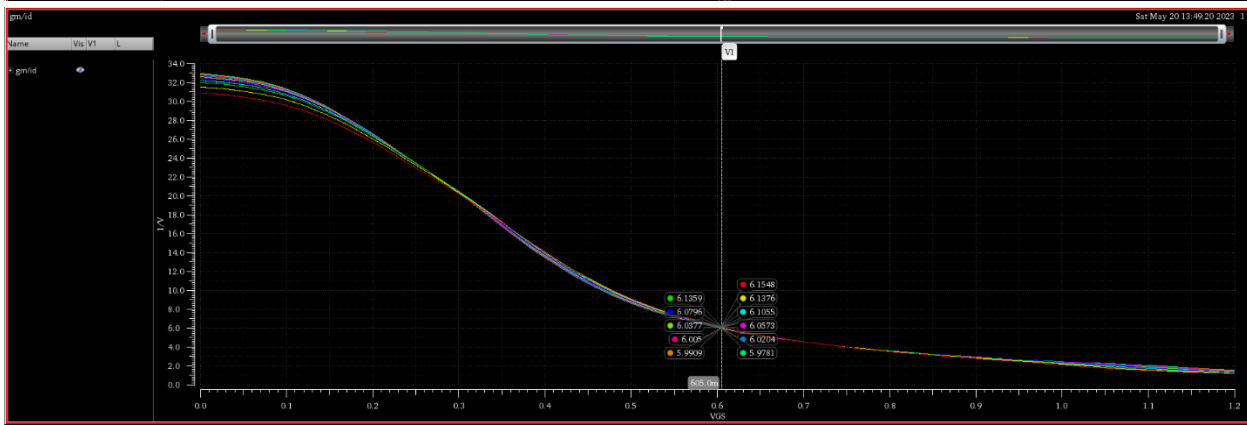
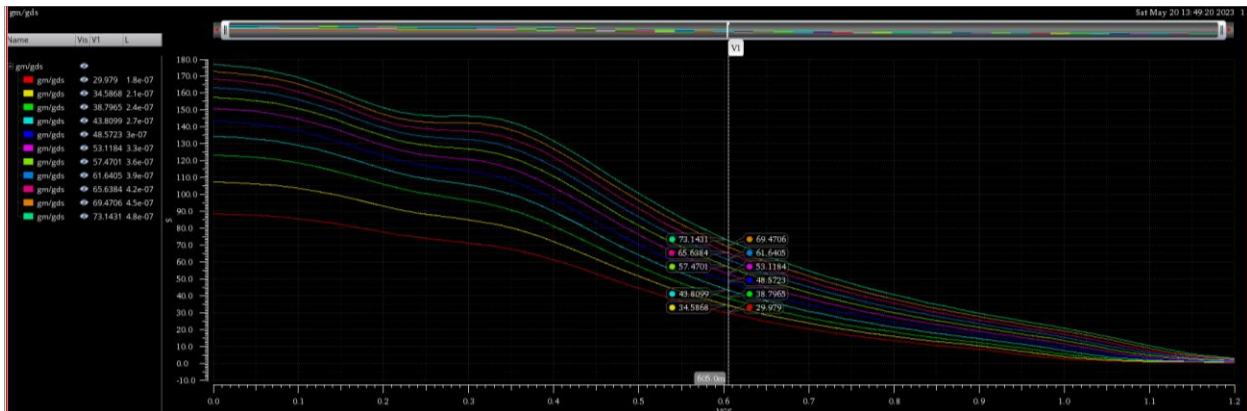
$$\therefore \frac{R_D r_o}{R_D + r_o} = 540 \quad \therefore r_o = 5400 \, \Omega$$

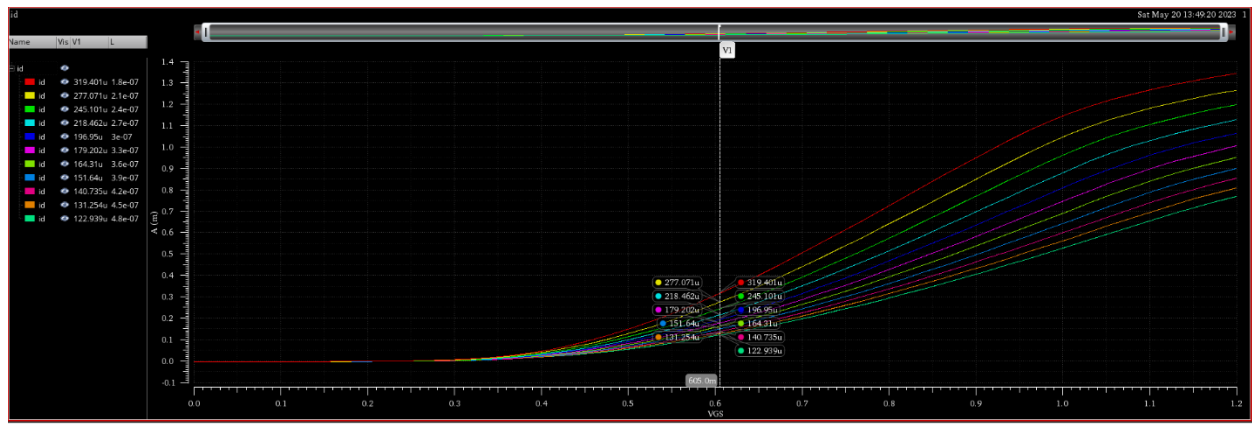
$$\therefore g_{ds} = \frac{1}{5400} \text{ S}$$

$$\therefore \frac{g_m}{g_{ds}} \geq 32.4$$

$$\frac{g_m}{I_D} = 6$$

$$V^* = \frac{2}{g_m / I_D} = 0.333 \text{ V}$$





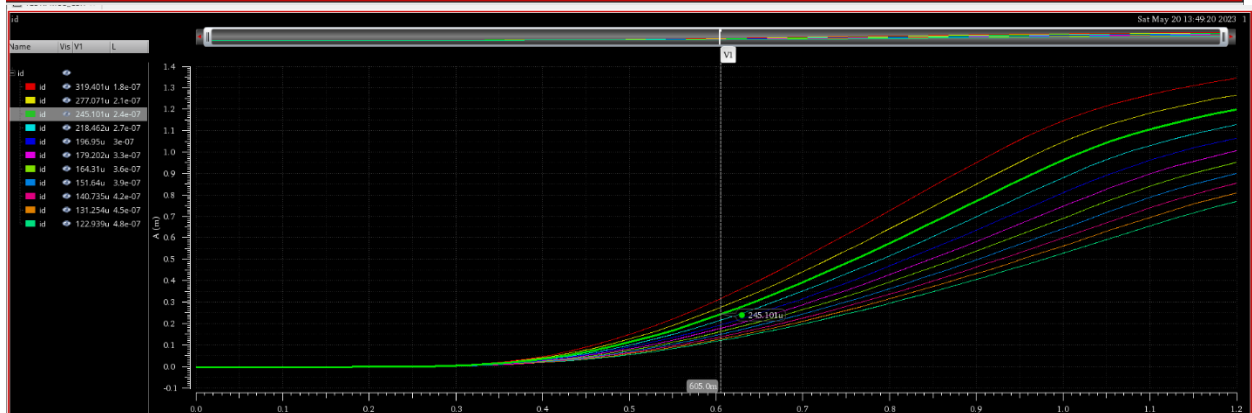
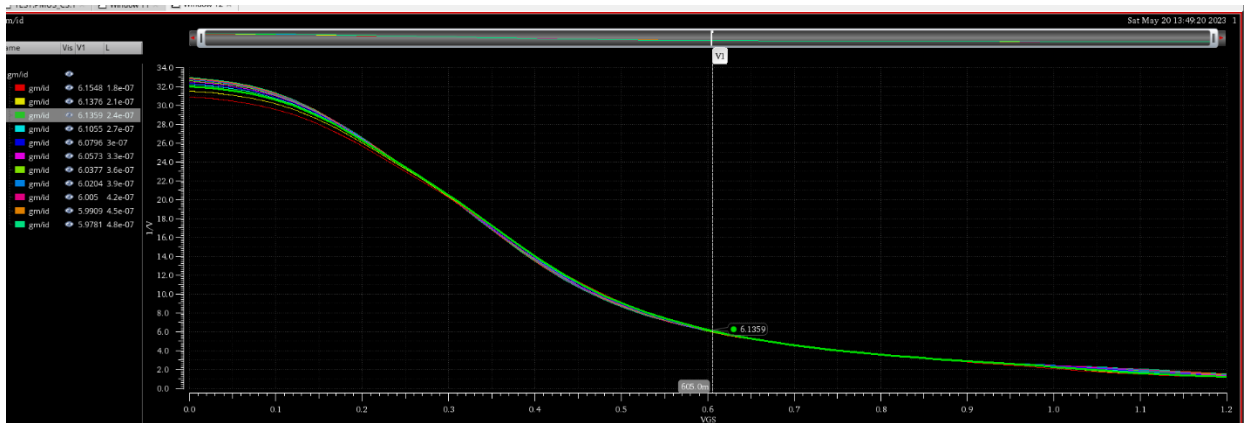
from the graphs we will take an average  $V_{GS}$  of 605 mV

from the  $\frac{g_m}{g_{ds}}$  graph the first ①

That satisfies the curve equation

and it gives  $g_{m1d} = 6.1359$

$g_m / g_{ds} = 38.7965$  uV





Thus we will take  $L = 240 \text{ nm}$

$$I_{Dx} = 245.101 \text{ u}$$

$$W = \frac{10 \times 1000}{245.101 \text{ u}} = 40.8 \text{ um}$$

we got gain = 2.954 v/v  
 $BW = 4.185 \text{ GHz}$

ine  $R_D$  to  $700 \Omega$

we obtained: gain = 10.3132 dB

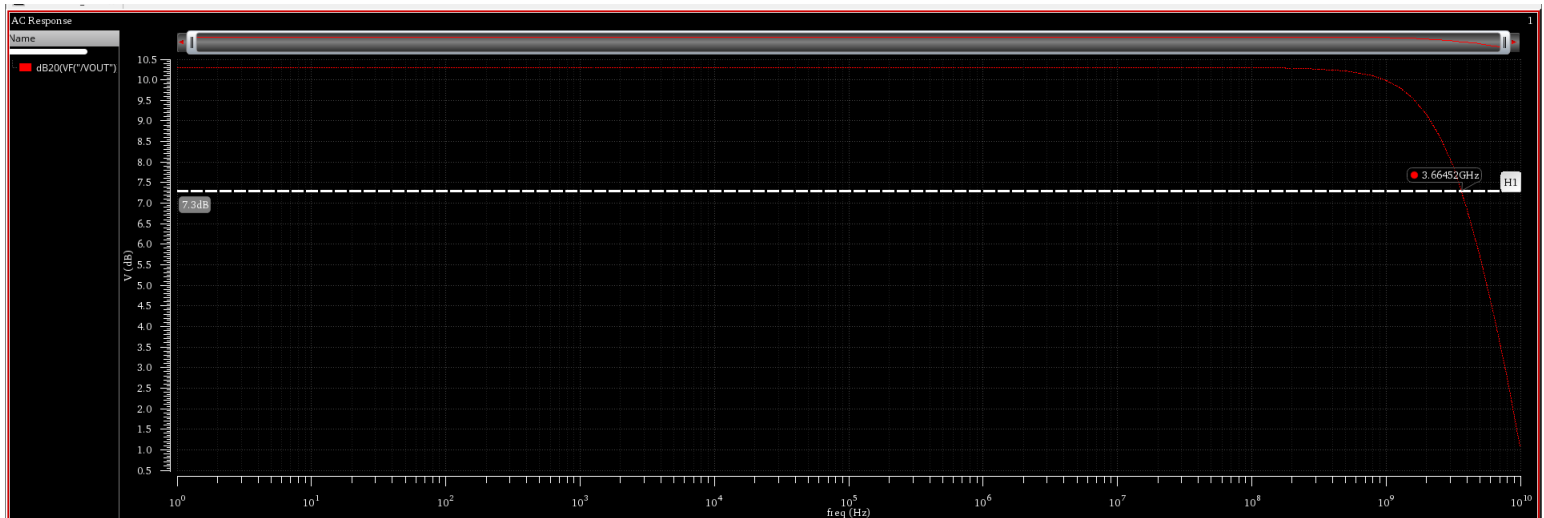
$$BW = 3.664 \text{ GHz}$$

$$I_d = 903.8 \text{ uA}$$

(a)

$$L = 240 \text{ um}$$

$$W = 40.8 \text{ um}$$



Specs Desired

obtained

gain  $\approx 10$  dB

10.3132 dB

Bw  $\approx 3$  GHz

3.664 GHz

Power  $\leq 1.2$  mW

1.084 mW

 $C_f = 50$  fF

Analyses

- ☒ ac 1 10G 10 Logarithmic Points Per D.
- ☒ dc t0 VAR("VDD") Automatic Start-St.

Click to add analysis

Design Variables

- ☐ A
- ☐ t
- ☐ VDD
- ☐ VGS
- ☐ W

Click to add variable

Click to add test

Global Variables

- ☒ L 240n
- ☐ W

Test	Output	Nominal	Spec	Weight	Pass/Fail
TEST-PMOS_CS1	gm				
TEST-PMOS_CS1	vth	-323.2m			
TEST-PMOS_CS1	id				
TEST-PMOS_CS1	v*				
TEST-PMOS_CS1	abs v*				
TEST-PMOS_CS1	gm/ids				
TEST-PMOS_CS1	gm/id				
TEST-PMOS_CS1	VR("VOUT")				
TEST-PMOS_CS1	bandwidth(VR("VOUT")) 3%...	3.664G			

