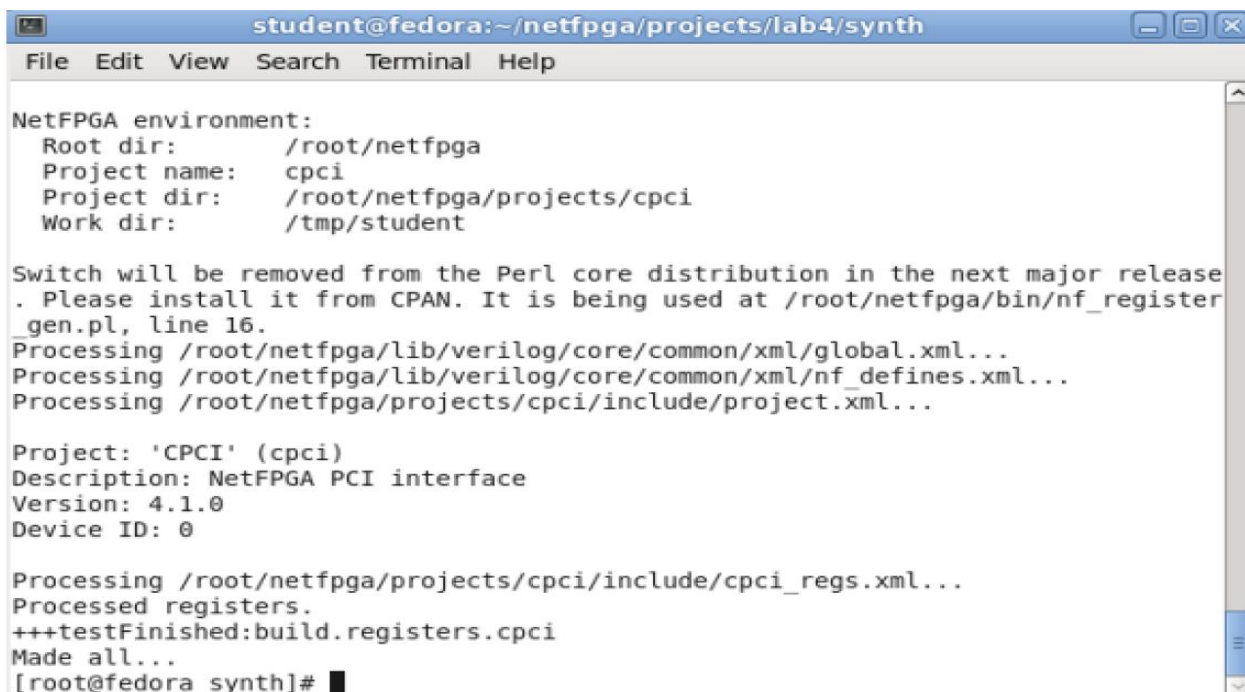
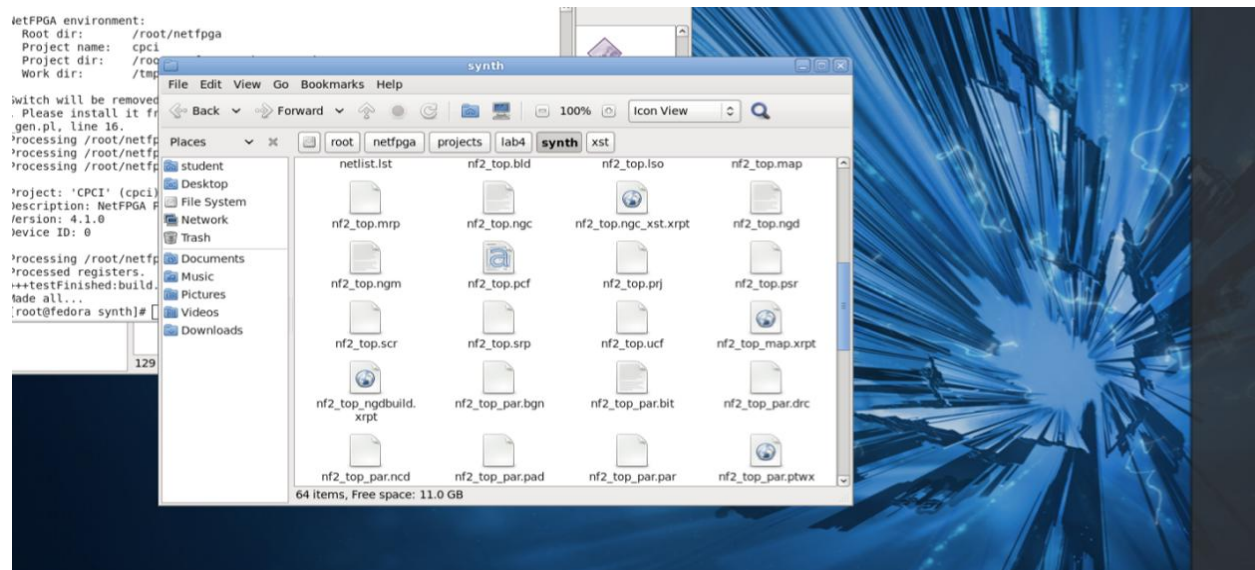


## Lab 4

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**Step 1:** Setting up NetFPGA tool and copying files to machines.



Running the reference project and generating the bit file

## Step2: Compile and generate a design bit file for NetFPGA.

```
student@fedora:~/netfpga/projects/lab4/synth
File Edit View Search Terminal Help
Module <pci2net_16x60> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/io_queues/add_rm_hdr/src/src_coregen/hdr_fifo.v" in library work
Module <syncfifo_512x32> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/syncfifo_512x36_fallthrough.v" in library work
Module <hdr_fifo> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/async_fifo_512x36_to_72_progfull_500.v" in library work
Module <syncfifo_512x36_fallthrough> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/syncfifo_512x36.v" in library work
Module <async_fifo_512x36_to_72_progfull_500> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/async_fifo_256x72_to_36.v" in library work
Module <syncfifo_512x36> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/async_fifo_512x36_progfull_500.v" in library work
Module <async_fifo_256x72_to_36> compiled
Compiling verilog file "/root/netfpga/lib/verilog/core/utls/src/src_coregen/syncfifo_512x72.v" in library work
Module <async_fifo_512x36_progfull_500> compiled
Module <syncfifo_512x72> compiled
No errors in compilation
Analysis of file <"nf2_top.prj"> succeeded.

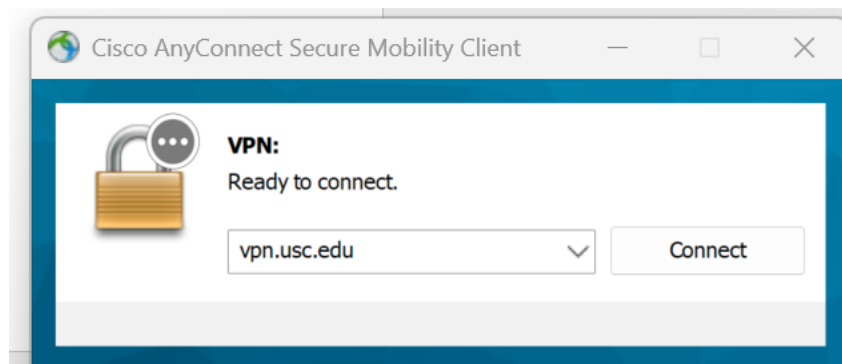
=====
*               Design Hierarchy Analysis               *
=====
ERROR:HDLCompilers:191 - "/root/netfpga/lib/verilog/core/utls/generic_regs/src/generic_sw_regs.v" line 69 Indices in part-select of vector wire 'reg_addr_in' are reverse
d
ERROR:HDLCompilers:185 - "/root/netfpga/lib/verilog/core/utls/generic_regs/src/generic_sw_regs.v" line 69 Illegal right hand side of continuous assign
ERROR:HDLCompilers:191 - "/root/netfpga/lib/verilog/core/utls/generic_regs/src/generic_hw_regs.v" line 70 Indices in part-select of vector wire 'reg_addr_in' are reverse
d
ERROR:HDLCompilers:185 - "/root/netfpga/lib/verilog/core/utls/generic_regs/src/generic_hw_regs.v" line 70 Illegal right hand side of continuous assign
-->

Total memory usage is 410676 kilobytes
Number of errors   :    4 ( 0 filtered)
Number of warnings :   74 ( 0 filtered)
Number of infos   :    0 ( 0 filtered)

Synthesis failed - see nf2_top.srp for details.
make: *** [nf2_top.ngc] Error 1
```

We are getting this error, and we tried solving it but it is taking time it seems. Will go through the error and try to solve it as soon as possible.

## Step 3: Setup VPN to USC



## Step 4: NetFPGA Environment.

```
node2@nf8:~  
Last login: Fri Feb  7 14:23:28 2025 from 10.23.213.39  
[team-7:n0 ~] echo $n0  
10.0.8.3  
[team-7:n0 ~] echo $n1  
10.0.9.3  
[team-7:n0 ~] echo $n2  
10.0.10.3  
[team-7:n0 ~] echo $n3  
10.0.11.3  
[team-7:n0 ~] █
```

IP address for the nodes 0 through 3.

## Step 5: NetFPGA- based Linux Kernel IP router

```
netfpga@nf7:~  
Built against CPCI version: 4 (rev 1)  
  
Virtex design compiled against active CPCI version  
[team-7:fpga ~] nf_download /home/netfpga/bitfiles/reference_nic.bit  
Found net device: nf2c0  
Bit file built from: nf2_top_par.ncd;HW_TIMEOUT=FALSE  
Part: 2vp50ff1152  
Date: 2011/11/17  
Time: 16:21:17  
Error Registers: 0  
Good, after resetting programming interface the FIFO is empty  
Download completed - 2377668 bytes. (expected 2377668).  
DONE went high - chip has been successfully programmed.  
CPCI Information  
-----  
Version: 4 (rev 1)  
  
Device (Virtex) Information  
-----  
Project directory: reference_nic  
Project name: Reference NIC  
Project description: Reference NIC  
  
Device ID: 1  
Version: 1.1.0  
Built against CPCI version: 4 (rev 1)  
  
Virtex design compiled against active CPCI version  
[team-7:fpga ~] █
```

Running the command and observing the output that was expected.

(b &c)

```
node2@nf6:~  
Last login: Fri Feb 7 13:56:54 2025 from 10.23.213.39  
[team-7:n3 ~] ping $n0  
PING 10.0.8.3 (10.0.8.3) 56(84) bytes of data.  
64 bytes from 10.0.8.3: icmp_seq=1 ttl=63 time=2.92 ms  
64 bytes from 10.0.8.3: icmp_seq=2 ttl=63 time=1.03 ms  
64 bytes from 10.0.8.3: icmp_seq=3 ttl=63 time=0.935 ms  
  
--- 10.0.8.3 ping statistics ---  
3 packets transmitted, 3 received, 0% packet loss, time 2001ms  
rtt min/avg/max/mdev = 0.935/1.632/2.924/0.914 ms  
[team-7:n3 ~] ping $n1  
PING 10.0.9.3 (10.0.9.3) 56(84) bytes of data.  
64 bytes from 10.0.9.3: icmp_seq=1 ttl=63 time=2.62 ms  
64 bytes from 10.0.9.3: icmp_seq=2 ttl=63 time=0.956 ms  
64 bytes from 10.0.9.3: icmp_seq=3 ttl=63 time=0.893 ms  
  
--- 10.0.9.3 ping statistics ---  
3 packets transmitted, 3 received, 0% packet loss, time 2000ms  
rtt min/avg/max/mdev = 0.893/1.491/2.626/0.803 ms  
[team-7:n3 ~] ping $n2  
PING 10.0.10.3 (10.0.10.3) 56(84) bytes of data.  
64 bytes from 10.0.10.3: icmp_seq=1 ttl=63 time=3.24 ms  
64 bytes from 10.0.10.3: icmp_seq=2 ttl=63 time=1.04 ms  
  
--- 10.0.10.3 ping statistics ---  
2 packets transmitted, 2 received, 0% packet loss, time 1000ms  
rtt min/avg/max/mdev = 1.044/2.146/3.248/1.102 ms  
[team-7:n3 ~]
```

e&g

```
node2@nf6:~  
4 bytes from 10.0.9.3: icmp_seq=2 ttl=63 time=0.956 ms  
4 bytes from 10.0.9.3: icmp_seq=3 ttl=63 time=0.893 ms  
  
-- 10.0.9.3 ping statistics --  
3 packets transmitted, 3 received, 0% packet loss, time 2000ms  
rtt min/avg/max/mdev = 0.893/1.491/2.626/0.803 ms  
[team-7:n3 ~] ping $n2  
PING 10.0.10.3 (10.0.10.3) 56(84) bytes of data.  
4 bytes from 10.0.10.3: icmp_seq=1 ttl=63 time=3.24 ms  
4 bytes from 10.0.10.3: icmp_seq=2 ttl=63 time=1.04 ms  
  
-- 10.0.10.3 ping statistics --  
2 packets transmitted, 2 received, 0% packet loss, time 1000ms  
rtt min/avg/max/mdev = 1.044/2.146/3.248/1.102 ms  
[team-7:n3 ~]  
[team-7:n3 ~] iperf -s -u  
-----  
server listening on UDP port 5001  
receiving 1470 byte datagrams  
UDP buffer size: 2.00 MByte (default)  
-----  
[3] local 10.0.11.3 port 5001 connected with 10.0.10.3 port 38379  
ID] Interval      Transfer      Bandwidth      Jitter    Lost/Total Datagrams  
[3]  0.0-10.2 sec   109 MBytes    88.9 Mbits/sec  9.657 ms  529117/606564 (87%)  
[4] local 10.0.11.3 port 5001 connected with 10.0.9.3 port 56265  
[4]  0.0-10.2 sec   102 MBytes    83.6 Mbits/sec  11.216 ms  532359/605169 (88%)  
[4]  0.0-10.2 sec   1 datagrams received out-of-order  
[3] local 10.0.11.3 port 5001 connected with 10.0.8.3 port 57281  
[3]  0.0-10.2 sec   110 MBytes    89.7 Mbits/sec  11.488 ms  553279/631434 (88%)  
[3]  0.0-10.2 sec   1 datagrams received out-of-order
```

h&i

N0 pinging to n3	Transfer-109MB	Bandwidth-88.9Mbps
N1 pinging to n3	Transfer-102MB	Bandwidth-83.6Mbps
N2 pinging to n3	Transfer-110MB	Bandwidth-89.7Mbps

## Step 6: NetFPGA Hardware IP Router

```
node2@nf6:~
[team-7:n3 ~] iperf -s -u
-----
Server listening on UDP port 5001
Receiving 1470 byte datagrams
UDP buffer size: 2.00 MByte (default)
-----
[3] local 10.0.11.3 port 5001 connected with 10.0.9.3 port 47275
ID] Interval      Transfer      Bandwidth      Jitter    Lost/Total Datagrams
[3] 0.0-10.2 sec   167 MBytes    138 Mbits/sec   14.202 ms 484176/603575 (80%)
[3] 0.0-10.2 sec   97 datagrams  received out-of-order
[4] local 10.0.11.3 port 5001 connected with 10.0.10.3 port 52968
[4] 0.0- 9.8 sec   215 MBytes    184 Mbits/sec   0.251 ms 453172/606565 (75%)
[4] 0.0- 9.8 sec   120 datagrams received out-of-order
[3] local 10.0.11.3 port 5001 connected with 10.0.8.3 port 54055
[3] 0.0-10.0 sec   298 MBytes    251 Mbits/sec   14.882 ms 345437/557718 (62%)
[3] 0.0-10.0 sec   49 datagrams  received out-of-order
```

e

N0 pinging to n3	Transfer-167MB	Bandwidth-139Mbps
N1 pinging to n3	Transfer-215MB	Bandwidth-184Mbps
N2 pinging to n3	Transfer-298MB	Bandwidth-251Mbps