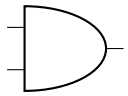
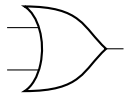
TABLE I
AND GATE



	F	*T*
F	F	F
T	F	T

Input1	Input2	Output
	1	
1		
1	1	1

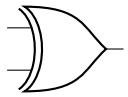
TABLE II
OR GATE



	F	*T*
F	F	T
T	T	T

Input1	Input2	Output
	1	1
1		1
1	1	1

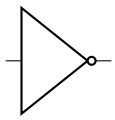
TABLE III
XOR GATE



	F	*T*
F	F	T
T	T	F

Input1	Input2	Output
	1	1
1		1
1	1	

TABLE IV
INVERTER OR NOT GATE



F	T
T	F

Input1	Output
1	
	1