Dr. Yuichi Nakamura, Executive Specialist, NEC Corporation

Dr. Yuichi Nakamura received his B.E. degree in information engineering and M.E. degree in electrical engineering from the Tokyo Institute of Technology in 1986 and 1988, respectively. He received his PhD degree from the Graduate School of Information, Production and Systems, Waseda University, in 2007. He joined NEC Corporation in 1988, and he led NEC's research about signal processing and embedded design as a general manager and a vice president of NEC research. Currently, he is an executive specialist at NEC Corporation. He is also a guest professor of the National Institute of Informatics, Hiroshima University, Waseda University, and Tokyo University. He has more than 30 years of professional experience in electronic design automation, signal processing, photonics, and quantum computing.

Dr. Yuichi Nakamura is an executive specialist in NEC. He contributed to manage and lead several innovative projects in signal processing and computing area. His main contribution is as follows.
1) He introduced a project of software and custom processor-based design methods, applied to media stream processing in set-top-box/digital TV/TV recorder LSI design. Since his design methods had rich flexibility and high performance, the design time was significantly reduced compared to all other hardware-based methods. According to his contribution, these chips were sold in the top share group on digital in 2006-2007.

2) He led a digital signal processing design method to optical fiber digital coherent LSI. In this case, one of the design difficulty was how to prepare the test bench for design. He managed a common test bench set for all design phases. Finally, the LSI could be developed without re-spin thanks to his clean test bench set.

3) He contributed the first commercial 4K HEVC based encoder development. Since this product should have been used to 4K board casting system at the 2014 FIFA World Cup, the development time was very short. He proposed all FPGA (Field Programmable Gate Array) based systems and led the FPGA design project. The system was released on time and success at 4K broadcasting during the FIFA World Cup games.

4) He started a novel quantum computing project from 2018. To start the project, he negotiated with the Japanese government and obtained a big grant (more than $27M USD/5 years) from the Japanese government. Until 2023, his team would develop the prototype of the novel quantum computing system to be specialized for solving combinational optimization problems.

Besides, Dr. Yuichi Nakamura has published more than 40 major international conference papers and more than 25 journal papers, which are related to the above contributions, and had delivered a number of keynote talks at major conferences such as ISCAS2019. In addition, currently, he is in charge of an advisory board member of the Japanese government quantum innovation meeting, a member of the evaluation committee of several Japanese government grant meetings. He is also a member of the technical committee of APSIPA SPS.

Title: Artificial Neural Networks and tools for Micro controllers

Speaker:

Danilo Pau
Technical Director, IEEE & ST Fellow
System Research and Applications
STMicroelectronics, Agrate Brianza

Abstract:

Is Artificial Intelligence a trendy technology or a singularity? With this key question in mind, the talk will review key milestones, discuss limitations of centralizing intelligence and review challenges and opportunities of having intelligence closer to sensors which produces data in real time. Next it will talk and demonstrate ST methodology and tools for automatic deployment of pre trained neural networks on company micro controllers (MCU): STM32 and Chorus. It will conclude with some considerations on ultra low power AI and about a more comprehensive AI ecosystem which the MCU mass market is looking at.

Danilo Pau, graduated at Politecnico di Milano, on 1992 in Electronic Engineering. He joined SGS-THOMSON (now STMicroelectronics) on 1991 and worked on mpeg2 video memory reduction, then video coding, transcoding, embedded graphics, computer vision, and currently on deep learning. During his career helped in transferring those developments into company products. Also funded and served as 1st Chairman of the STMicroelectronics Technical Staff Italian Community; he is currently Technical Director into System Research and Applications and a Fellow Member of ST. Since 2019 Danilo is an IEEE Fellow, serves as Industry Ambassador coordinator for IEEE Region 8 South Europe, is vice chair of the Task Force on “Intelligent Cyber-Physical Systems” within IEEE CIS and Member for the Machine learning, Deep learning and AI in CE (MDA) Technical Stream Committee IEEE Consumer Electronics Society (CESoc).

Contributed with 113 documents the development of Compact Descriptors for Visual Search (CDVS), CDVS successfully developed ISO-IEC 15938-13 MPEG standard. He was Funding Chair of MPEG Ad Hoc Group on Compact Descriptor for Video Analysis (CDVA), formerly Compact Descriptors for Video Search (CDViS). He also contributes (applications) to MPAI.community recently started by L. Chiariglione. His scientific production consists of 93 papers to date, 81 granted patents and 31 invited talks/seminars at various universities and conferences. He was also principal investigator into numerous funded projects at European and Italian level on embedded systems.

Danilo tutored lots of undergraduate students (till Msc graduation), Msc engineers and PhD students from various universities in Italy; France and India, one of the activities that he likes at most.