

Qubit Mapping and Routing tailored to Advanced Quantum ISAs: Not as Costly as You Think

Abstract

We propose CANOPUS (**C**anonical-**O**ptimized **P**lacement **U**tility **S**uite), a qubit mapping/routing framework tailored to advanced quantum ISAs adaptive to versatile hardware architectures.

1 Introduction

Advanced ISAs—Can [1], \sqrt{i} SWAP [2]

CANOPUS (**C**anonical-**O**ptimized **P**lacement **U**tility **S**uite) is a qubit mapping and routing framework that is tailored to advanced quantum ISAs, such as Can [1] and \sqrt{i} SWAP [2], which are adaptive to versatile hardware architectures. CANOPUS is designed to optimize the placement of qubits and the routing of quantum gates, taking into account the specific requirements of these advanced ISAs.

2 Background

2.1 Qubit mapping/routing

2.2 Quantum gates realization in diverse ISAs

3 Motivation

Two-fold motivations:

1. The scalable qubit routing effects (2x-4x) is still a critical challenge in practical quantum computing systems
2. How to utilize the emerging advanced ISAs (hardware breakthroughs); across all phases of compilation, routing is the bottleneck and is the most easily handled for co-optimization

[ZY: Use a “optimal routing benchmark” to illustrate the OVERHEAD of existing methods]

[ZY: There should be many takeaways]

- Previous routing overhead is not precise for hardware execution
- Previous routing is costly and also not precise for hardware execution
- SWAP can be implemented in low overhead (gate duration) with the recent breakthrough gate schemes for advanced ISAs
- How to efficiently capture the rich commutation relations when performing co-optimization during qubit routing and gate scheduling

4 CANOPUS framework

4.1 Overview

4.2 Routing in canonical form

- Unified and highly-effective qubit routing approach in canonical form, with properties of quantum ISAs tailored to the routing process

4.3 Gate commutation guided optimization

- Capture optimization opportunities exposed by gate commutation; while commutation relations can be uniformly described in canonical form

4.4 Qubit dependencies guided optimization

- Capture optimization opportunities exposed by qubit dependencies, which implies optimization in a more global scope

5 Implementation

5.1 Core functionalities

5.2 Extensions

5.3 Scalability

6 Case Studies

6.1 QFT kernel

6.2 Co-exploration of routing and ISA selection

6.3 Mapping on FTQC architecture

7 Evaluation

8 Related Works

9 Conclusion

References

- [1] Jianxin Chen, Dawei Ding, Weiyuan Gong, Cupjin Huang, and Qi Ye. 2024. One Gate Scheme to Rule Them All: Introducing a Complex Yet Reduced Instruction Set for Quantum Computing. In *Proceedings of the 29th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 2*. ACM, La Jolla, CA, USA, 779–796.
- [2] Cupjin Huang, Tenghui Wang, Feng Wu, Dawei Ding, Qi Ye, Linghang Kong, Fang Zhang, Xiaotong Ni, Zhijun Song, Yaoyun Shi, Hui-Hai Zhao, Chunqing Deng, and Jianxin Chen. 2023. Quantum Instruction Set Design for Performance. *Physical Review Letters* 130 (Feb 2023), 070601. Issue 7. doi:10.1103/PhysRevLett.130.070601

- A Canonical gate and 2Q circuit synthesis**
- B Optimal gate duration with Can ISA**