

# ZITENG YANG

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## EDUCATION

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**Georgia Institute of Technology (Georgia Tech)**, Atlanta, GA, USA Aug. 2021 – Present

*Ph.D. student* in Computer Science, School of Computer Science

- Advised by Vivek Sarkar
- Research Interests: program verification, formal methods, parallel program

**Shanghai Jiao Tong University (SJTU)**, Shanghai, China Sept. 2017 – Jul. 2021

*B.E.* in Computer Science and Technology, Department of Computer Science and Engineering

## PUBLICATIONS

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- **Z. Yang**, X. Yin and S. Li. “Maximally permissive supervisor control of timed discrete-event systems under partial observation,” in 21st IFAC World Congress, 2020

### Submitted

- [**\*Co-first author, dictionary order**] Verification-aided Compiler Optimization

## RESEARCH PROJECTS

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### Program Analysis for Parallel Program

Nov. 2021 – Now

*Research Assistant* Advisor: *Vivek Sarkar*, School of Computer Science, Georgia Tech.

- Implementing a new idea for May-happen-in-Parallel analysis problem on async/finish parallel model

### Verification-aided Compiler Optimization in the CompCert Compiler

Apr. 2020 – Jun. 2021

*Research Assistant* Advisor: *Qinxiang Cao*, John Hopcroft Center for Computer Science, SJTU.

An expedition to implement compiler optimization using verification code of a program:

- Designed a semantics framework based on small step semantics in CompCert Certified Compiler, aiming for verifying new compiler optimization methods for certified program using hints of Hoare Logic assertions
- Designed and proved the correctness of the verification routine of backward simulation relation as well as the preservation of annotation’s consistency between source and compiled program for the newly proposed optimization method

### Finite Model for Modal Logic’s Completeness Theory in Coq

Nov. 2019 – Apr. 2020

*Research Assistant* Advisor: *Qinxiang Cao*, John Hopcroft Center for Computer Science, SJTU.

- Formally proved Formalized Propositional Dynamic Logic (PDL)’s completeness theories in Coq using the method of finite canonical model which is distinctive from any previously formalized logics in this library

### Formal Control Theory of Timed Discrete-Event Systems

Aug. 2018 – Oct. 2019

*Research Assistant* Advisor: *Xiang Yin*, Department of Automation, SJTU.

Field: Formal methods in Automata & Control Theory

- Proposed a method for synthesizing a safe and maximally-permissive supervisor for Timed Discrete Event System, a finite-automata-style model which models time into automata, and formally proved the correctness;

## TEACHING EXPERIENCE

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[Incoming]**Teaching Assistant**, CS4510: Automata and Complexity, Georgia Tech, *Joseph Jaeger* Fall 2022

**Teaching Assistant**, MA208: Discrete Mathematics, SJTU, lectured *Qinxiang Cao* Fall 2020

**Teaching Assistant**, MA239: Discrete Mathematics (Honor), SJTU, lectured *Xiang Yin* Fall 2020

## COURSES AND PROJECTS

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### Graduate Courses:

2021 - Present, Georgia Tech

- **Compiler Design:**
  - Topics and assignments around middle/back-end optimization of modern compiler
  - One project in dynamic array bound checking and another project in loop dependence testing
- **Software Analysis and Testing:** Topics and paper review around classical and cutting edge program analysis researches, with a self-proposed project

### Selected Undergraduate Courses:

2017 - 2021, SJTU

- **Scored A:** Programming Languages (98/100), Computing Theory, Projects of Operating System (100/100), Linux Kernel, Cloud Computing, Database System Technology
- **Scored B:** Artificial Intelligence, Machine learning, Computer Network, Intro. to Information Security (89)

### Project: Interpreter for “SimPL” Programming Language

Spring 2020

- Implemented an interpreter in Java following given semantic specification of simplified dialect of ML
- Implemented type checking and evaluation

### Project: Naive Airdrop

Fall 2019

- Designed a file synchronizing application from Android phone to PC within local area network with encryption in transfer, auto connection, changes detecting etc.

### Project: Re-implementation of deque and map in STL

Fall 2018

- Re-implemented the *deque* and *map* template class in C++ Standard Template Library w.r.t. the interface

## SKILLS

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### Programming Experiences:

- **Coq:** long-term research projects on CompCert compiler
- **C/C++:** course projects (LLVM IR, Linux kernel, C++ STL implementation, algorithm design)
- **Java:** Android & PC applications
- **Python:** course projects (machine learning)

### Familiar Tools/Libraries:

- **LLVM IR**
- **VST:** Verified Software Tool-chain in Coq, a separation logic based tool to verify correctness of C programs

### Languages:

- Native: Standard Mandarin, Sichuanese Mandarin
- Fluent: English

## HONORS AND AWARDS

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- Rongchang Scholarship for Science and Technology Innovation, Finalist, 10,000 CNY (10 finalists winning 10,000, 10 winners winning 30,000, university-wide per year ) 2020
- Undergraduate Excellent Scholarship, 500 CNY Third-class 2018
- 1st Prize in National High School Mathematics League in Provinces 2016