# ZITENG YANG

**Z** ziteng.yang@gatech.edu · ♠ Youngzt998 · ♣ youngzt998.github.io/

#### **EDUCATION**

# Georgia Institute of Technology, Atlanta, GA, USA

Aug. 2021 – Present

Ph.D. student in Computer Science, School of Computer Science

- · Advised by Vivek Sarkar
- Research Interests: program verification, formal methods, parallel program

# Shanghai Jiao Tong University (SJTU), Shanghai, China

Sept. 2017 - Jul. 2021

B.E. in Computer Science and Technology, Department of Computer Science and Engineering

## **PUBLICATIONS**

• **Z. Yang**, X. Yin and S. Li. "Maximally permissive supervisor control of timed discrete-event systems under partial observation," in 21st IFAC World Congress, 2020

#### **Submitted**

• [\*Co-first author, dictionary order] Verification-aided Compiler Optimization

# RESEARCH PROJECTS

**Verification-aided Compiler Optimization in the CompCert Compiler** Apr. 2020 – Jun. 2021

Research Assistant Advisor: Qinxiang Cao, John Hopcroft Center for Computer Science, SJTU.

An expedition to implement compiler optimization using verification code of a program:

- Designed a semantics framework based on small step semantics in CompCert Certified Compiler, aiming for verifying new compiler optimization methods for certified program using hints of Hoare Logic assertions
- Designed and proved the correctness of the verification routine of backward simulation relation as well as
  the preservation of annotation's consistency between source and compiled program for the newly proposed
  optimization method

# Finite Canonical Model for Completeness Theory in Coq

Nov. 2019 – Apr. 2020

Research Assistant Advisor: Qinxiang Cao, John Hopcroft Center for Computer Science, SJTU.

A work for extension of a logic library in Coq from infinite method to finite method:

• Formally proved Formalized Propositional Dynamic Logic (PDL)'s completeness theories in Coq using the method of finite canonical model which is distinctive from any previously formalized logics in this library

# **Supervisor Control Theory of Timed Discrete-Event Systems**

Aug. 2018 – Oct. 2019

Research Assistant Advisor: Xiang Yin, Department of Automation, SJTU.

Field: Formal methods in Automata & Control Theory

- Proposed a method for synthesizing a safe and maximally-permissive supervisor for Timed Discrete Event System (TDES, a finite-automata-style model) which models time into conventional automata;
- Formally proved the correctness of such method, i.e. the closed-loop language which depicts the behavior of the system under the synthesized supervisor is within a safe specification language

## TEACHING EXPERIENCE

**Teaching Assistant**, MA208: Discrete Mathematics, SJTU, lectured by *Qinxiang Cao* **Teaching Assistant**, MA239: Discrete Mathematics (Honor), SJTU, lectured by *Xiang Yin*Fall 2020

# **COURSES AND PROJECTS**

#### **Graduate Courses:**

2021 - Present, Georgia Tech

- Compiler Design: topics around middle-end optimization of modern compiler with projects in dynamic array bound checking
- · Software Analysis and Testing

# **Selected Undergraduate Courses:**

2017 - 2021, SJTU

• Programming Languages (98), Computing Theory (91), Project Workshop of Operating System (100), Linux Kernel (91)

## Project: Interpreter for "SimPL" Programming Language

Spring 2020

- Implemented an interpreter in Java following given semantic specification of simplified dialect of ML
- Implemented type checking and evaluation

## **Project: Naive Airdrop**

Fall 2019

• Designed a file synchronizing application from Android phone to PC within local area network with encryption in transfer, auto connection, changes detecting etc.

## Project: Re-implementation of deque and map in STL

Fall 2018

• Re-implemented the *deque* and *map* template class in C++ Standard Template Library w.r.t. the interface

# SKILLS

## **Programming Experiences:**

- Coq: long-term research projects on CompCert compiler
- C/C++: course projects (LLVM IR, Linux kernel, C++ STL implementation, algorithm design)
- Java: Android & Windows applications
- **Python**: course projects (machine learning)

#### Familiar Tools/Libraries:

- LLVM IR
- VST: Verified Software Tool-chian in Coq, a separation logic based tool to verify correctness of C programs

#### Languages:

- Native: Standard Mandarin, Sichuanese Mandarin
- Fluent: English

#### Honors and Awards

- Rongchang Scholarship for Science and Technology Innovation, Finalist, 10,000 CNY (10 finalists wining 10,000, 10 winners winning 30,000, university-wide per year)
- Undergraduate Excellent Scholarship, 500 CNY Third-class

2018

• 1st Prize in National High School Mathematics League in Provinces

2016