ZITENG YANG

EDUCATION

Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA

2021 - 2026 (expected)

Ph.D. student in Computer Science, Advised by Vivek Sarkar, GPA: 3.6 / 4.0

• Research Area: Program Logic & Certified Compilation, Formal Methods, Parallelism & Concurrency

Minor in Mathematics

Shanghai Jiao Tong University (SJTU), Shanghai, China

2017 - 2021

B.E. in Computer Science and Technology, GPA: 3.6 / 4.0

PUBLICATIONS

- Z. Yang, J. Shirako, V. Sarkar, Fully Verified Instruction Scheduling, OOPSLA'24 [Compiler Verification]
- **Z. Yang**, X. Yin and S. Li, Maximally permissive supervisor control of timed discrete-event systems under partial observation, in 21st IFAC World Congress, 2020 [Control Theory]

RESEARCH PROJECTS

Verified Linear Scan Register Allocation

2024-now

Advisor: Vivek Sarkar, School of Computer Science, Georgia Tech.

• Incorporating and formally proving linear scan register allocation algorithm in CompCert addressing the problem that verified graph coloring register allocation requires either heavy work on proof of code or heavy compile time during validation.

Verified Instruction Scheduling

2023 - 2024

Advisor: Vivek Sarkar, School of Computer Science, Georgia Tech.

- Formally build the foundation to verify instruction scheduling passes in the CompCert Certified Compiler which addresses the problem that existing approaches only implemented unverified schedulers with verified validators instead of direct verification
- Implemented a case study to prove the correctness of list scheduling based on the framework
- Achieved the first ever fully verified instruction scheduling pass in a formally verified compiler

Program Analysis of Parallel Programming Model via CFL Reachability

2022-now

Advisor: Vivek Sarkar, School of Computer Science, Georgia Tech.

- Proposed, proved, and implemented O(V+E)-worst-case algorithm (previously $O(V^3)$) for MHP analysis of parallel programs with async, finish, and atomic structures based on sub-problems of CFL-reachability
- Investigating applications on data-race detection/prediction

Compiler Correctness of Annotation Verifier

2020 - 2021

Advisor: Qinxiang Cao, John Hopcroft Center for Computer Science, SJTU.

- Designed an extended semantics & correctness framework for CompCert Certified Compiler to verify optimizations that use Hoare/Separation Logic assertions annotated in C program as a hint
- Formalized (in Coq) the correctness of the framework, i.e. any optimization that preserved the validity of assertions inside programs preserved the semantics simulation (program equivalence) relation.

2018 - 2019

Advisor: Xiang Yin, Department of Automation, SJTU.

Field: Formal methods in Automata & Control Theory

• Designed an algorithm for synthesizing a safe and maximally-permissive supervisor for Timed Discrete Event System and formally proved its correctness, i.e. the language generated by the automata under such synthesized supervisor is safe yet maximal.

TEACHING EXPERIENCE

Teaching Assistant, CS6390 Programming Languages, Georgia Tech, taught by *Vivek Sarkar* Spring 2023

• The foundational principles of programming languages

Teaching Assistant, CS4510 Automata and Complexity, Georgia Tech, taught by *Joseph Jaeger* Fall 2022

• Introduction to Computability: regular language & DFA/NFA, context-free language & PDA, Turning Machine, complexity theory (P/NP/co-NP., L/NL, co-NL)

Teaching Assistant, Discrete Mathematics (IEEE Honor Class), SJTU, taught by *Qinxiang Cao* Fall 2020

• First-order Logic (proof, semantics, and soundness), Set Theory as foundation of mathematics

Teaching Assistant, Discrete Mathematics (Zhiyuan Honor Class), SJTU, taught by *Xiang Yin* Fall 2020

• Logic and deduction, Graph Theory, Set Theory

SELECTED COURSES AND PROJECTS

Graduate Courses:

2021 - Present, Georgia Tech

- **Software Development Process** Object-oriented software engineering, unit test, UML, android/java development, group development, software refactoring
- Parallelizing Compilers, techniques for loop-level & instruction-level parallelism
- **High-Performance Computer Architecture**, with labs simulating CPU with bypassing, branch-prediction, super-scalar, out-of-order-execution, multi-level caches, DRAM, multi-processor, cache way-partition etc.
- Compiler Design, LLVM IR optimization techniques with labs and projects on compiler optimization
- Software Analysis and Testing, program analysis techniques, paper reviews and projects on static analysis
- [Minor in math] Measure Theory(= Real Analysis I), Algebra I (ongoing)

Selected Undergraduate Courses:

2017 - 2021, SJTU

• Programming Languages, Computing Theory, Artificial Intelligence, Machine Learning, Operating System, Linux Kernel, Database System, Information Security, Computer Network, Game Design, etc.

Undergraduate Project: Interpreter for "SimPL" Programming Language

Spring 2020

• Implemented an interpreter (type inference/checking and evaluation) in Java for a simplified dialect of ML following given semantic specification

Undergraduate Project: Naive Airdrop

Fall 2019

• Designed & implemented a file synchronizing application from Android phone to Windows PC within local area network with encryption in transfer, auto connection, changes detecting etc.

SKILLS

Programming Experiences:

- Coq: long-term research projects on certified compiler and program logic
- C/C++: course and research projects (LLVM IR, Linux kernel, STL implementation, algorithm design)
- Java, Python: course projects (machine learning, small apps, etc.)

Tools/Libraries:

- LLVM IR
- CompCert Certified Compiler (an end-to-end formally verified C compiler)
- VST (Verified Software Tool-chian in Coq, a separation logic based verification tool for C programs)

HONORS AND SCHOLARSHIPS

•	Conference Travel & Registration Grant by PLMW@PLDI'22, San Diego	2022
•	Rongchang Scholarship for Science and Technology Innovation, Finalist, 10,000 CNY (10 finalists	and 10
	winners per year, university-wide)	2020
•	Undergraduate Excellence Scholarship, 500 CNY Third-class	2018