Ziteng Yang

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Education

Georgia Institute of Technology (Georgia Tech), Atlanta, GA, USA Aug. 2021 – Present

Ph.D. student in Computer Science, PLSE Lab at School of Computer Science

- Advised by *Vivek Sarkar*
- Research Interests: Program Logic & Certified Compilation, Formal Methods, Parallelism & Concurrency

Shanghai Jiao Tong University (SJTU), Shanghai, China Sept. 2017 – Jul. 2021

B.E. in Computer Science and Technology, Department of Computer Science and Engineering

Publications

- **Z. Yang**, X. Yin and S. Li. "Maximally permissive supervisor control of timed discrete-event systems under partial observation," in 21st IFAC World Congress, 2020 **[Formal Control Theory]**

In submission

- **[*Co-first author, dictionary order]** Verification-aided Compiler Optimization **[Compiler Verification]**

Research Projects

Directly Verified Instruction Scheduler in Compilers Dec. 2022 - Now

First Author Advisor: *Vivek Sarkar*, School of Computer Science, Georgia Tech.

- Existing certified instruction scheduling only implemented indirectly unverified scheduler, i.e. verified validator and cannot reason whether it will falsely reject a valid program due to scheduler's bug that triggers validator's error alarm
- We are working on directly proving the correctness of schedulers formally based on building and reasoning on properties of the dependence graph and reducing the verification work as possible.

May-happen-in-parallel (MHP) Analysis for parallel program Jan. 2022 - Now

First Author Advisor: *Vivek Sarkar*, School of Computer Science, Georgia Tech.

- Proposed, proved, and implemented $O(V+E)$-worst-case algorithm (previously $O(V^3)$) for MHP analysis of parallel programs with async, finish, and atomic structures based on sub-problems of CFL-reachability

Verification-aided Compiler Optimization in the CompCert Compiler Apr. 2020 – Jun. 2021

First Author Advisor: *Qinxiang Cao*, John Hopcroft Center for Computer Science, SJTU.

- Designed an extended semantics & correctness framework for CompCert Certified Compiler to verify optimizations that use Hoare/Separation Logic assertions annotated in C program as a hint
- Formalized (in Coq) the correctness of the framework, i.e. any optimization that preserved the validity of assertions inside programs preserved the semantics simulation (program equivalence) relation.

Modal Logic's Completeness Theory in Coq Nov. 2019 – Apr. 2020

Research Assistant Advisor: *Qinxiang Cao*, John Hopcroft Center for Computer Science, SJTU.

- Formally proved Propositional Dynamic Logic(a derivation from general modal logic)'s completeness theorem in Coq via finite canonical model

Formal Control Theory of Timed Discrete-Event Systems Aug. 2018 – Oct. 2019

First Author Advisor: *Xiang Yin*, Department of Automation, SJTU.

Field: Formal methods in Automata & Control Theory

- Designed an algorithm for synthesizing a safe and maximally-permissive supervisor for Timed Discrete Event System and formally proved its correctness, i.e. the language generated by the automata under such synthesized supervisor is safe yet maximal.

Teaching Experience

Teaching Assistant, CS4510 Automata and Complexity, Georgia Tech, lectured by *Joseph Jaeger* Fall 2022

- Intro to Compatibility: regular language & DFA/NFA, context-free language & PDA, Turning Machine, P/NP/co-NP., L/NL, co-NL

Teaching Assistant, MA208 Discrete Mathematics, SJTU, lectured by *Qinxiang Cao* Fall 2020

- First-order Logic (proof, semantics and soundness), Set Theory and Foundation of Mathematics

Teaching Assistant, MA239 Discrete Mathematics (Honor), SJTU, lectured by *Xiang Yin* Fall 2020

- Logic and deduction, Graph Theory, Set Theory

Selected Courses and Projects

Graduate Courses: 2021 - Present, Georgia Tech

- **[Ongoing] Parallelizing Compilers**, techniques on task level parallelism (loop transformation, etc.), and instruction level parallelism (instruction scheduling, etc.) in compilers
- **High Performance Computer Architecture**, with labs simulating CPU with bypassing, branch-prediction, super-scalar, out-of-order-execution, multi-level caches, DRAM, multi-processor, cache way-partition etc.
- **Compiler Design**, IR and optimization of compiler (LLVM) with labs on dynamic array bound checking and project on loop dependence testing
- **Software Analysis and Testing**
- **[Minor in math] Measure Theory**

Selected Undergraduate Courses (All Scored A): 2017 - 2021, SJTU

- Programming Languages (98/100), Computing Theory, Projects of Operating System (100/100), Linux Kernel, Cloud Computing, Database System etc. Technology

Undergraduate Project: Interpreter for "SimPL" Programming Language Spring 2020

- Implemented an interpreter (type inference/checking and evaluation) of a simplified dialect of ML following given semantic specification (using Java)

Skills

Programming Experiences:

- **Coq**: long-term research projects on Mathematical Logic and CompCert Certified compiler
- **C/C++**: course and research projects (LLVM IR, Linux kernel, STL implementation, algorithm design)
- **Java**: Android & PC applications
- **Python**: course projects (machine learning)

Familiar Tools/Libraries:

- **LLVM IR**
- **CompCert Certified Compiler** (the end-to-end formally verified C compiler)
- **VST** (Verified Software Tool-chian in Coq, a separation logic based verification tool for C programs)

Languages: Standard Mandarin (Native), Sichuanese Mandarin (Fluent), English (Fluent)

Honors and Awards

- Rongchang Scholarship for Science and Technology Innovation, Finalist, 10,000 CNY (10 finalists and 10 winners, university-wide per year) 2020
- Undergraduate Excellent Scholarship, 500 CNY Third-class 2018
- 1st Prize in National High School Mathematics League in Provinces 2016