وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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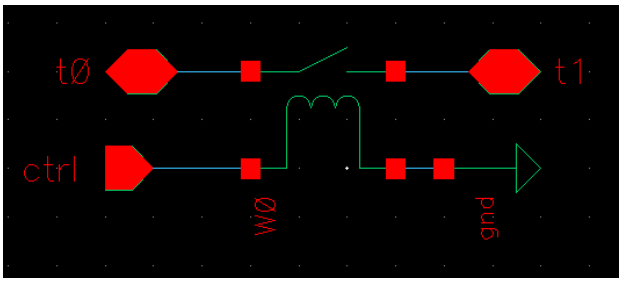
# Analog Integrated System Design – Cadence Tools
# Lab 09 (Mini-Project 02)
Oversampling ΣΔ Modulator

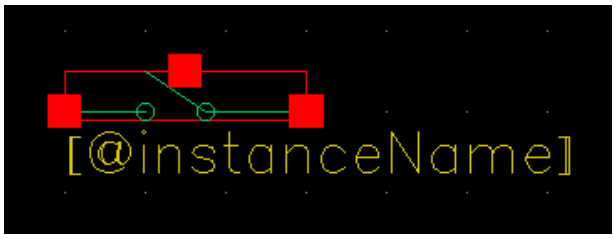
## Intended Learning Objectives

1) To be familiar with the design and simulation of fully-differential ΣΔ modulator.

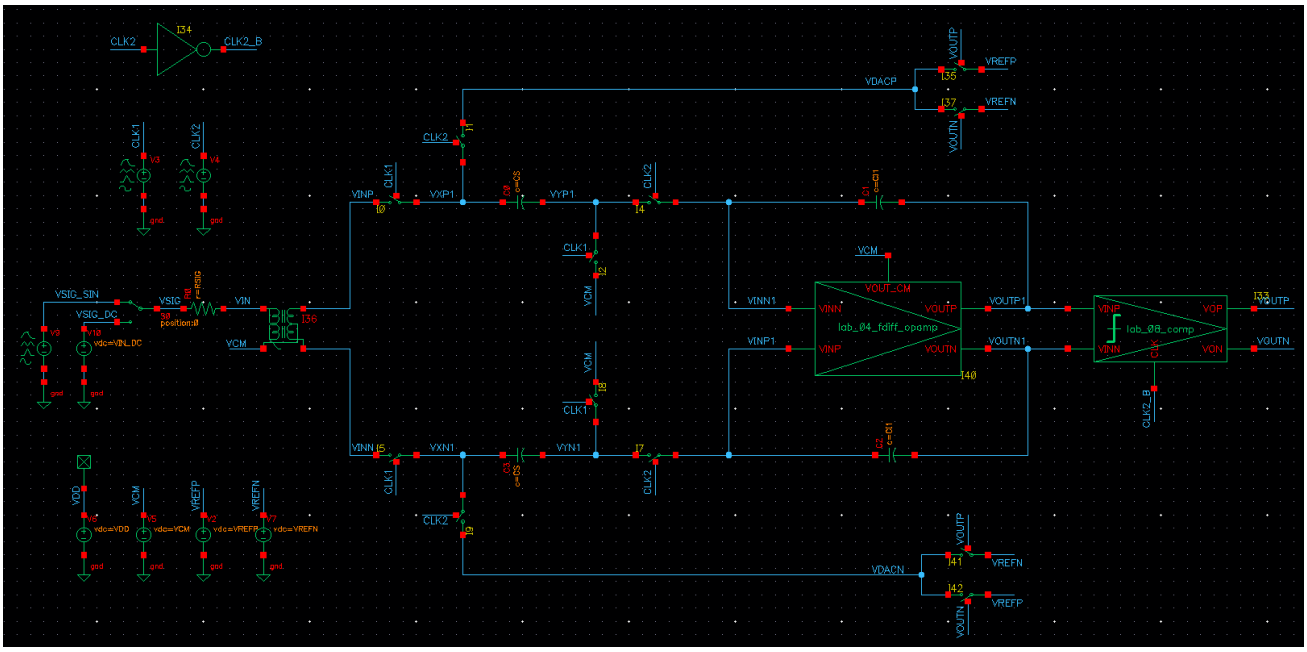
## PART 1: First-Order ΣΔ Modulator

1) Create a schematic and a compact symbol for an analog switch. Make the symbol as compact as possible because we will use the switch frequently.



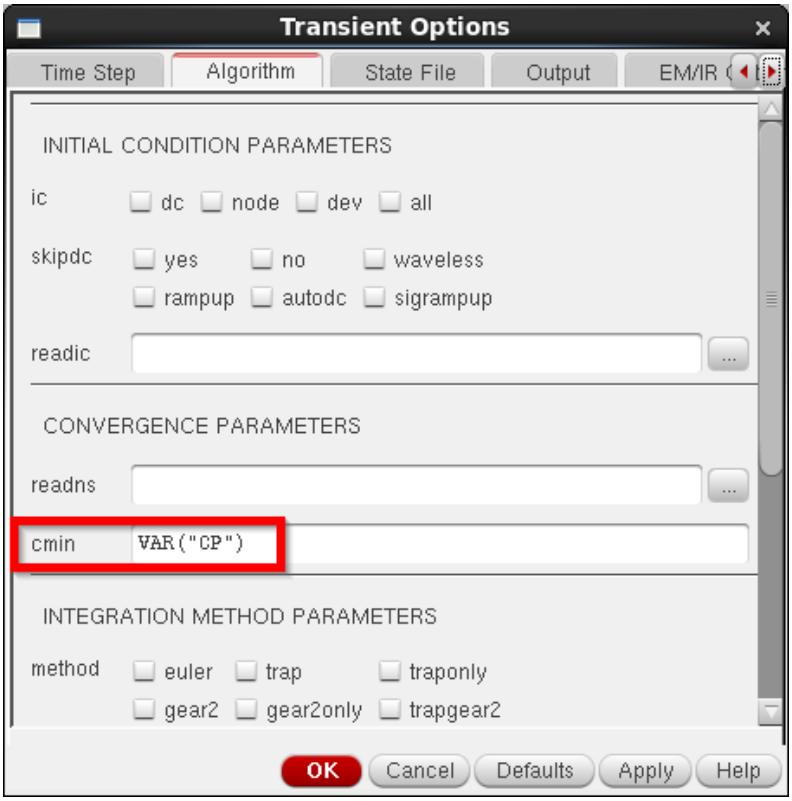




2) Create a testbench for first-order Sigma-Delta modulator (SDM) as shown below. Use a fully differential OTA similar to Lab 04 and a behavioral comparator similar to Lab 07.




3) Create adexl view.

4) In the transient analysis settings, set output start and stop time to TDROP and TSTOP variables as usual. Set the min capacitance at each node to be CP as shown below. This will help avoid convergence problems and sharp voltage transients.



# PART 2: First-Order SDM DC Functional Test

1) Set CLK1 and CLK2 as two non-overlapping clocks as shown below.

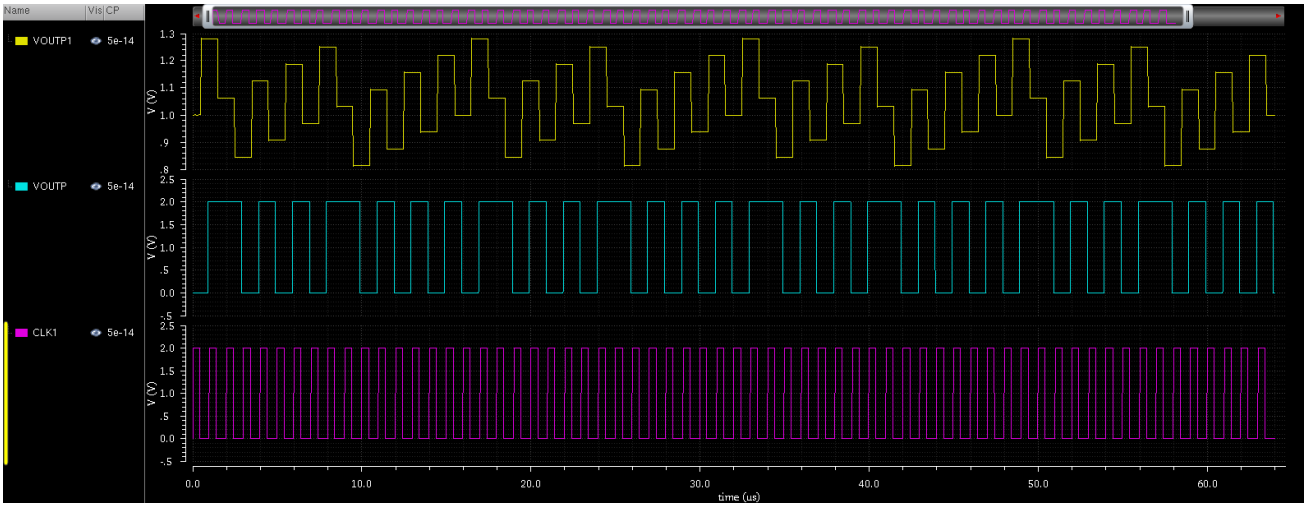
| | CLK1 | CLK2 |
|---|---|---|
| **Type** | Pulse | Pulse |
| **Zero value** | 0 | 0 |
| **One value** | VDD | VDD |
| **Period** | TS | TS |
| **Pulse width** | TON | TON |
| **Delay** | 0 | TS/2 |
| **Rise/fall time** | TRF | TRF |

2) Set global variables as shown below.

| | |
|---|---|
| **CI1** | 2p |
| **CS** | 1p |
| **RSIG** | 1k |
| **TRF** | 1n |
| **TS** | 1u |
| **TON** | 0.4*TS |
| **VDD** | 2 |
| **VCM** | 0.5*(VREFP + VREFN) |
| **VREFP** | 0.75*VDD |
| **VREFN** | 0.25*VDD |
| **CP** | 50f |
| **NFFT** | (2**5)*OSR |
| **NCYC** | 5 |
| **FIN** | (NCYC/NFFT)/TS |
| **OSR** | 2**5 |
| **FNYQ** | 0.5/TS |
| **FMAX** | FNYQ/OSR |
| **VPK** | A*(VREFP - VREFN) |
| **A** | 0.5 |
| **VIN_DC** | 0.125*(VREFP – VREFN) |
| **TDROP** | 0 |
| **TSTOP** | 2*OSR*TS |
| **SW_POS** | 2 |

3) Run transient simulation.
4) Report the waveforms of CLK1, the integrator output (VOUTP1) and the comparator output (VOUTP). Comment on the waveforms.

a. Do you notice any periodicity? Why?
b. What do you expect to see if you plot the output spectrum?
c. Find the value that the integrator increments each clock cycle. Justify this value.



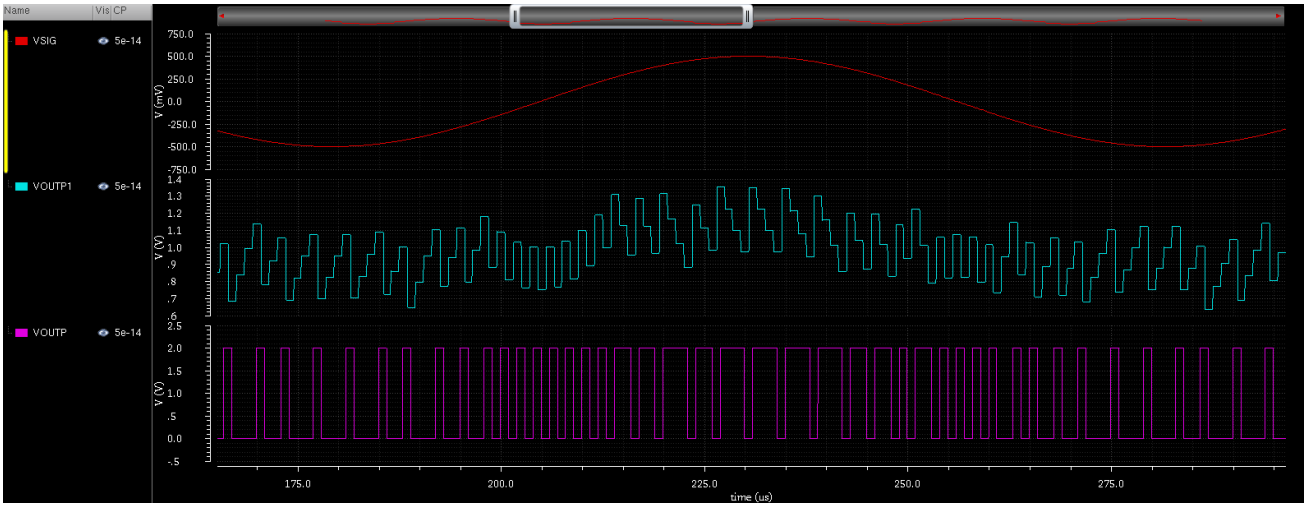

5) Calculate the average value of the comparator output (VOUTP). Justify the value you calculated.

# PART 3: First-Order SDM Sine Wave Test

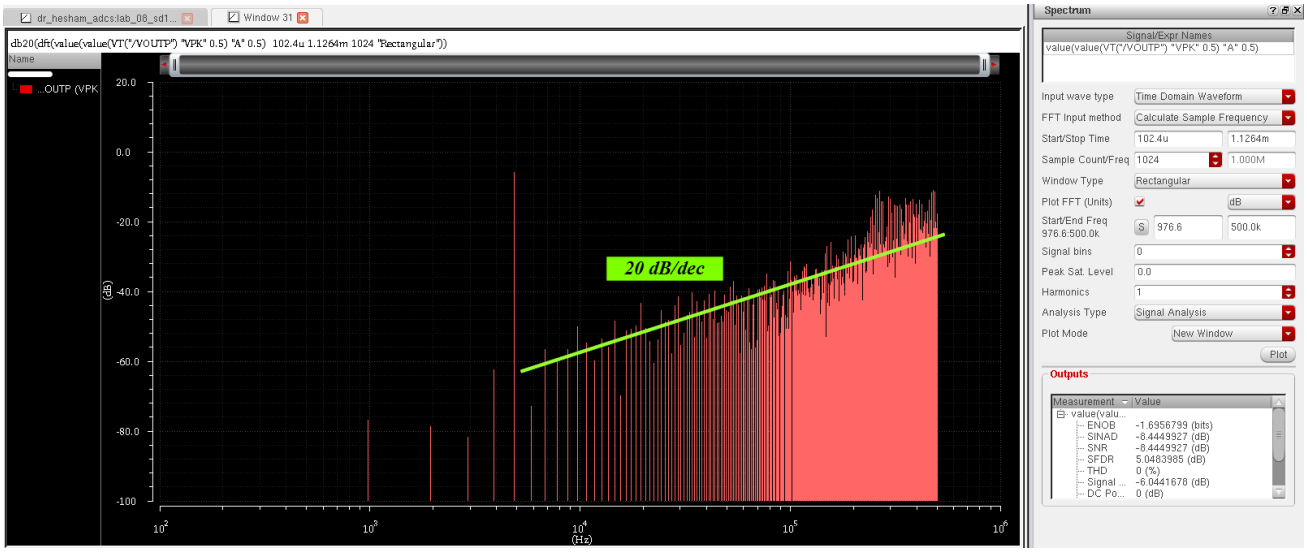
1) Save the simulation state of the previous part as “dc_test”. Modify the global variables as below.

| | |
|---|---|
| **CI1** | 2p |
| **CS** | 1p |
| **RSIG** | 1k |
| **TRF** | 1n |
| **TS** | 1u |
| **TON** | 0.4*TS |
| **VDD** | 2 |
| **VCM** | 0.5*(VREFP + VREFN) |
| **VREFP** | 0.75*VDD |
| **VREFN** | 0.25*VDD |
| **CP** | 50f |
| **NFFT** | (2**5)*OSR |
| **NCYC** | 5 |
| **FIN** | (NCYC/NFFT)/TS |
| **OSR** | 2**5 |
| **FNYQ** | 0.5/TS |
| **FMAX** | FNYQ/OSR |
| **VPK** | A*(VREFP - VREFN) |
| **A** | 0.5 |
| **VIN_DC** | 0.125*(VREFP – VREFN) |
| **TDROP** | 0.5/FIN |
| **TSTOP** | NCYC/FIN + TDROP |
| **SW_POS** | 1 |

2) Run transient simulation.
3) Zoom-x on one cycle of VSIG and report the waveforms of VSIG, the integrator output (VOUTP1) and the comparator output (VOUTP). Comment on the waveforms.



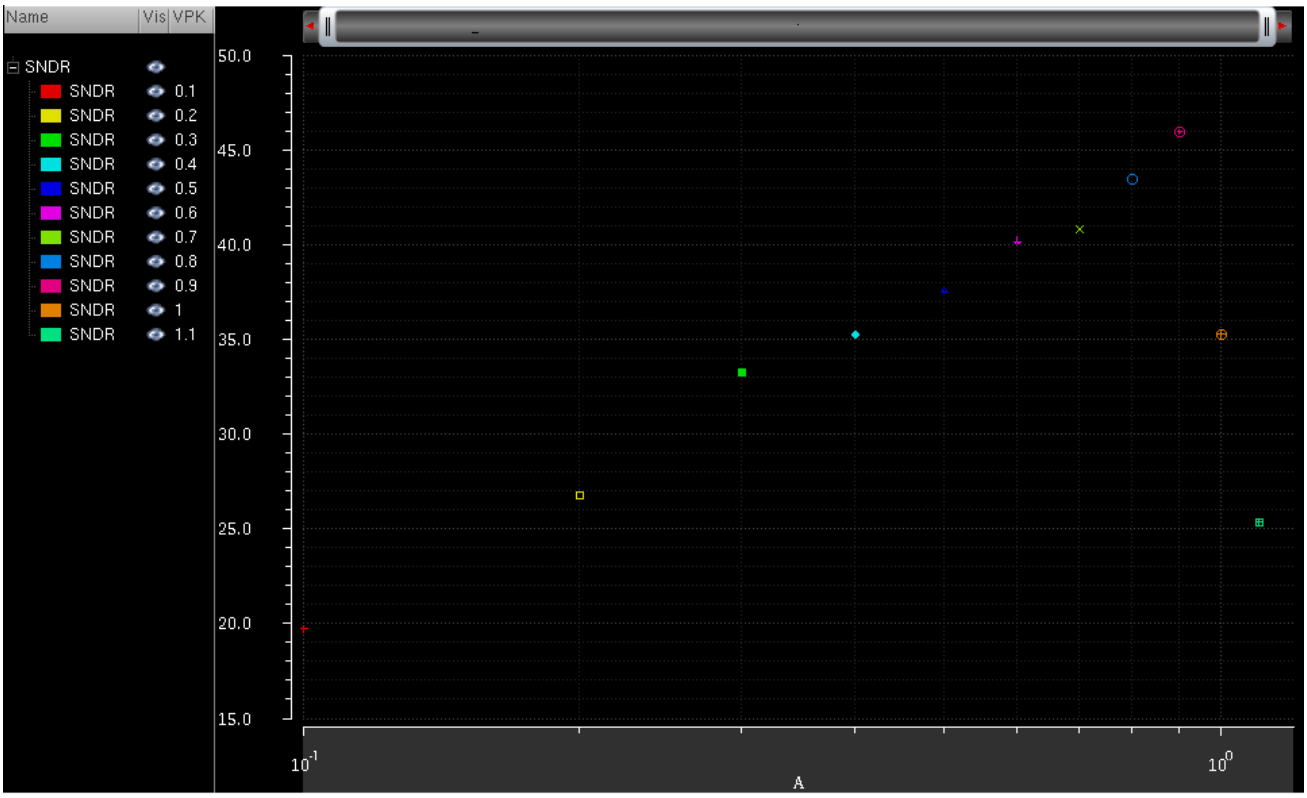

4) Use the spectrum tool to plot the output spectrum. Right click on the frequency axis and choose log scale. Comment on the results.



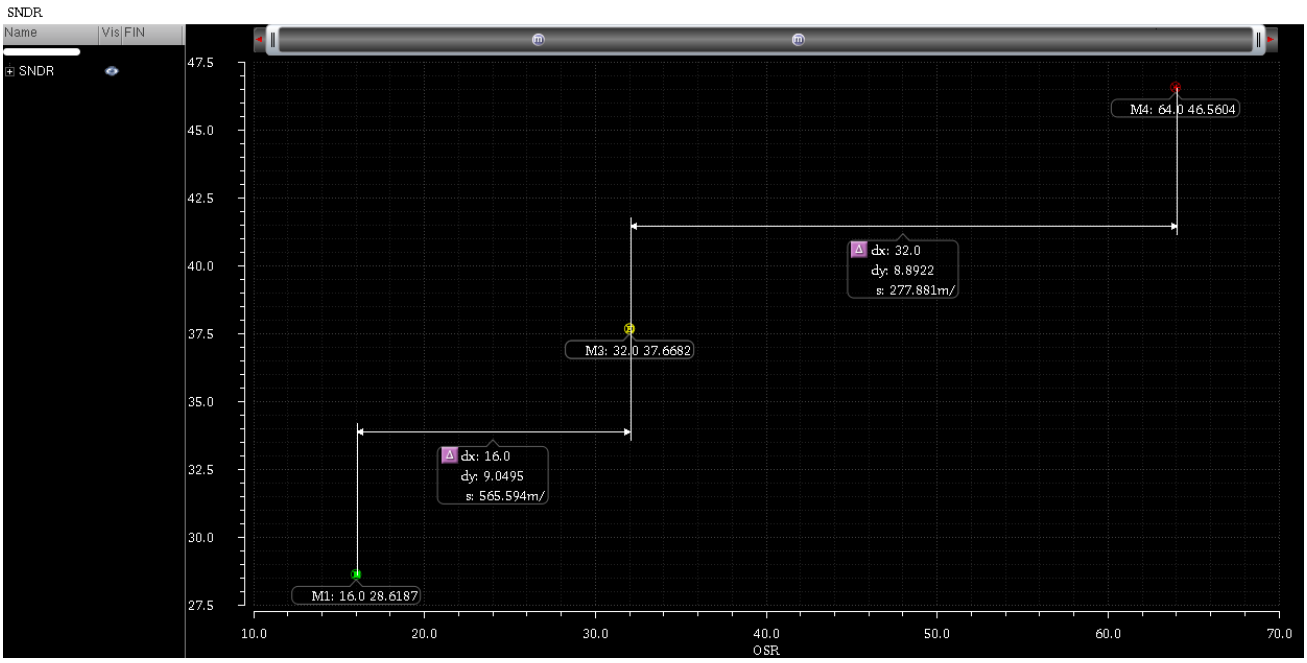

5) Use the following expression in adexl to calculate the ENOB and SNDR.

```
spectrumMeasurement(getData("/VOUTP" ?result "tran") t VAR("TDROP") VAR("TSTOP")
VAR("NFFT") VAR("FIN") VAR("FMAX") 0 "Rectangular" 0 0 7 "enob")
spectrumMeasurement(getData("/VOUTP" ?result "tran") t VAR("TDROP") VAR("TSTOP")
VAR("NFFT") VAR("FIN") VAR("FMAX") 0 "Rectangular" 0 0 7 "sinad")
```

6) Run parametric sweep with A = 0.1:0.1:1.1
   a. Plot SNDR vs A on log scale. Comment on the results.
   b. Find the peak SNDR and ENOB and compare them with the theoretically expected values.




7) Run parametric sweep with OSR = 2**4, 2**5, 2**6
   a. Plot SNDR vs OSR. Comment on the results.
   b. Find the improvement in SNDR vs OSR and compare it with the theoretically expected values.




# PART 4: Second-Order SDM

1) Create a new testbench for a second-order SDM. Repeat what you did in Part 3.