Analog Integrated Systems Design

Lecture 16
ADCs Comparison

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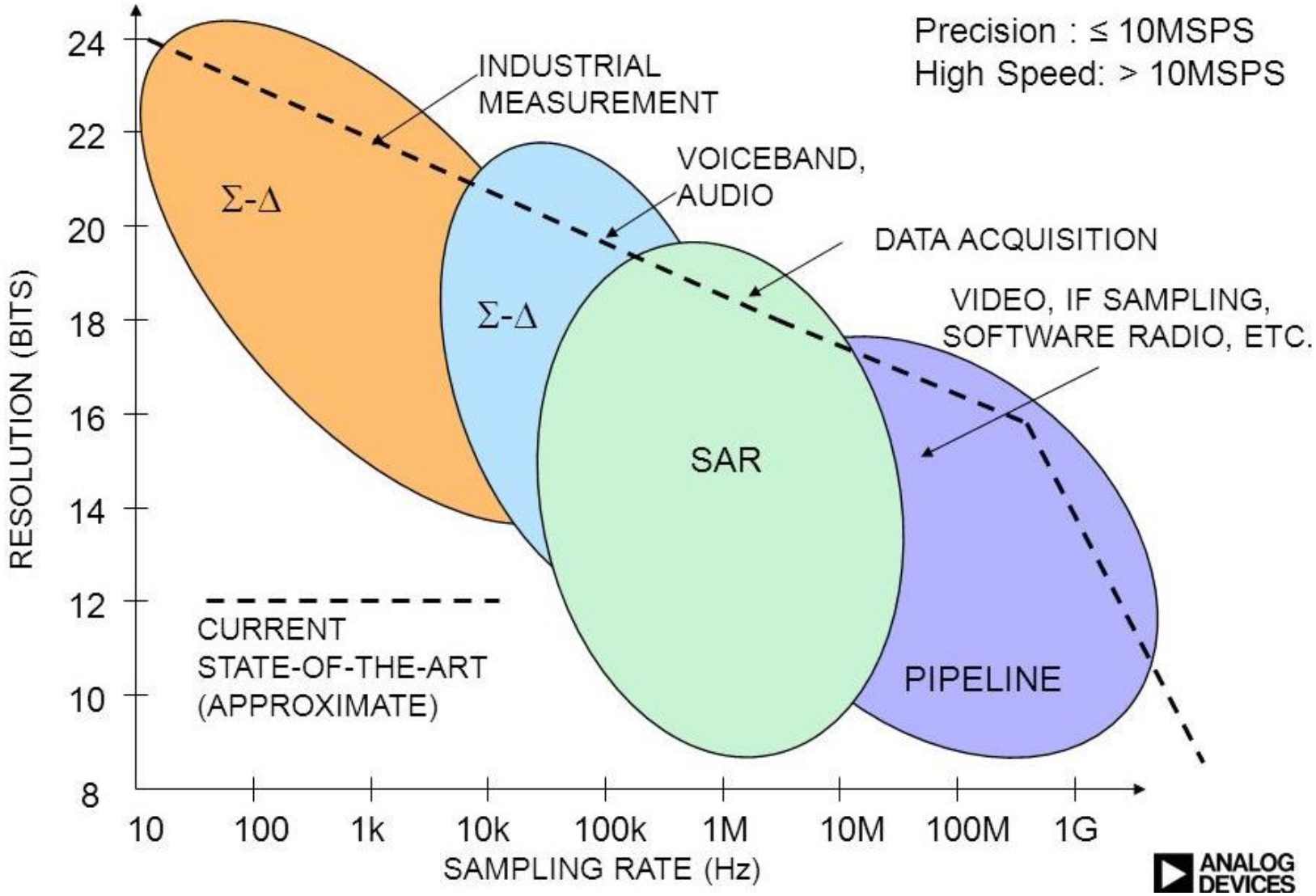
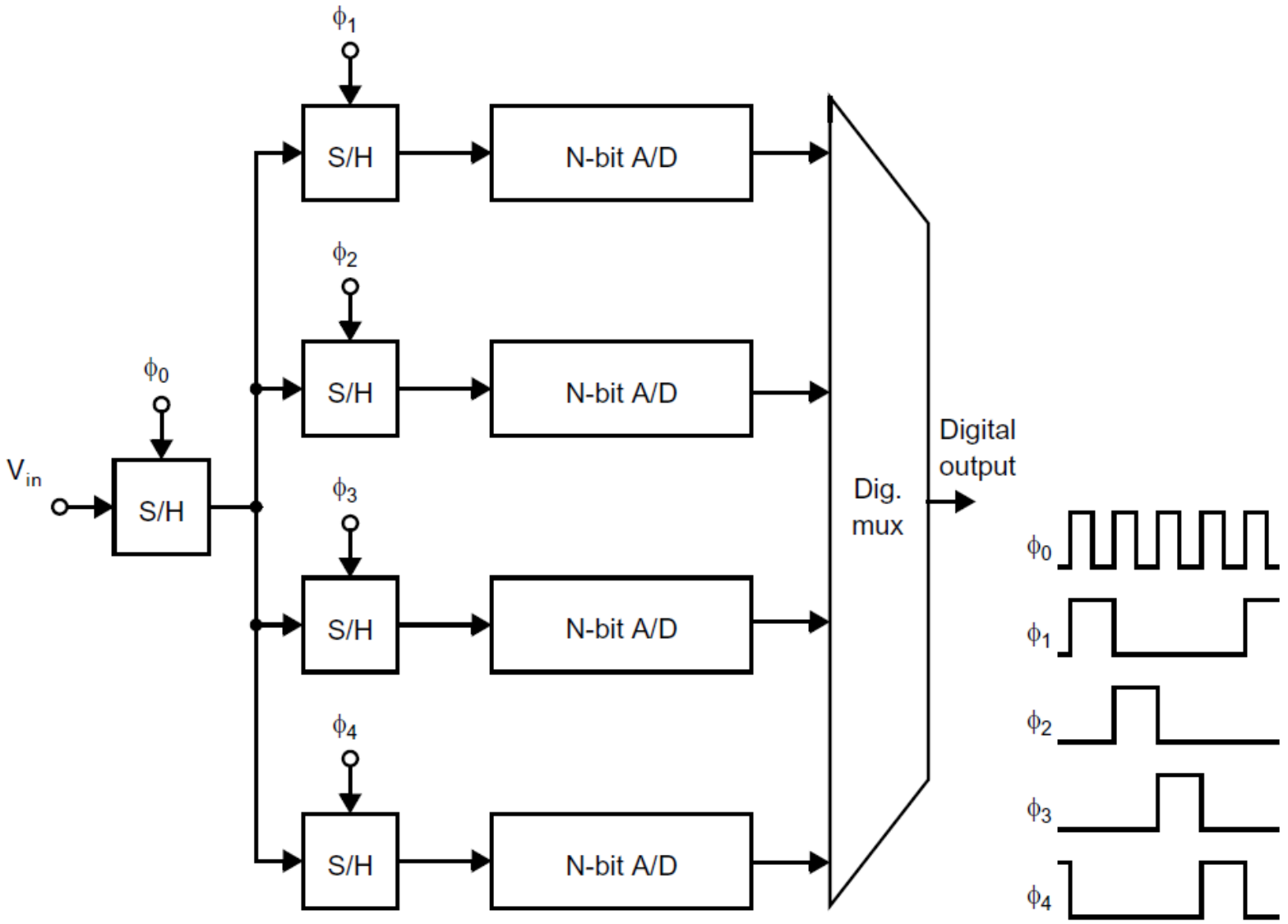
ADCs Comparison



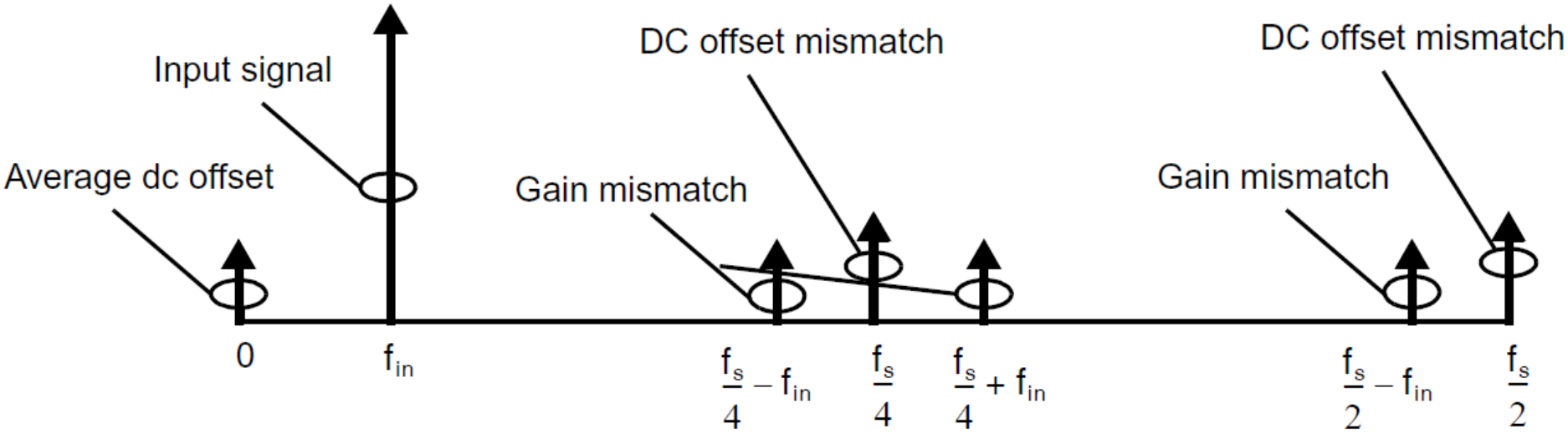
Time-Interleaved ADC



[Johns & Martin, 2012]

Time-Interleaved ADC

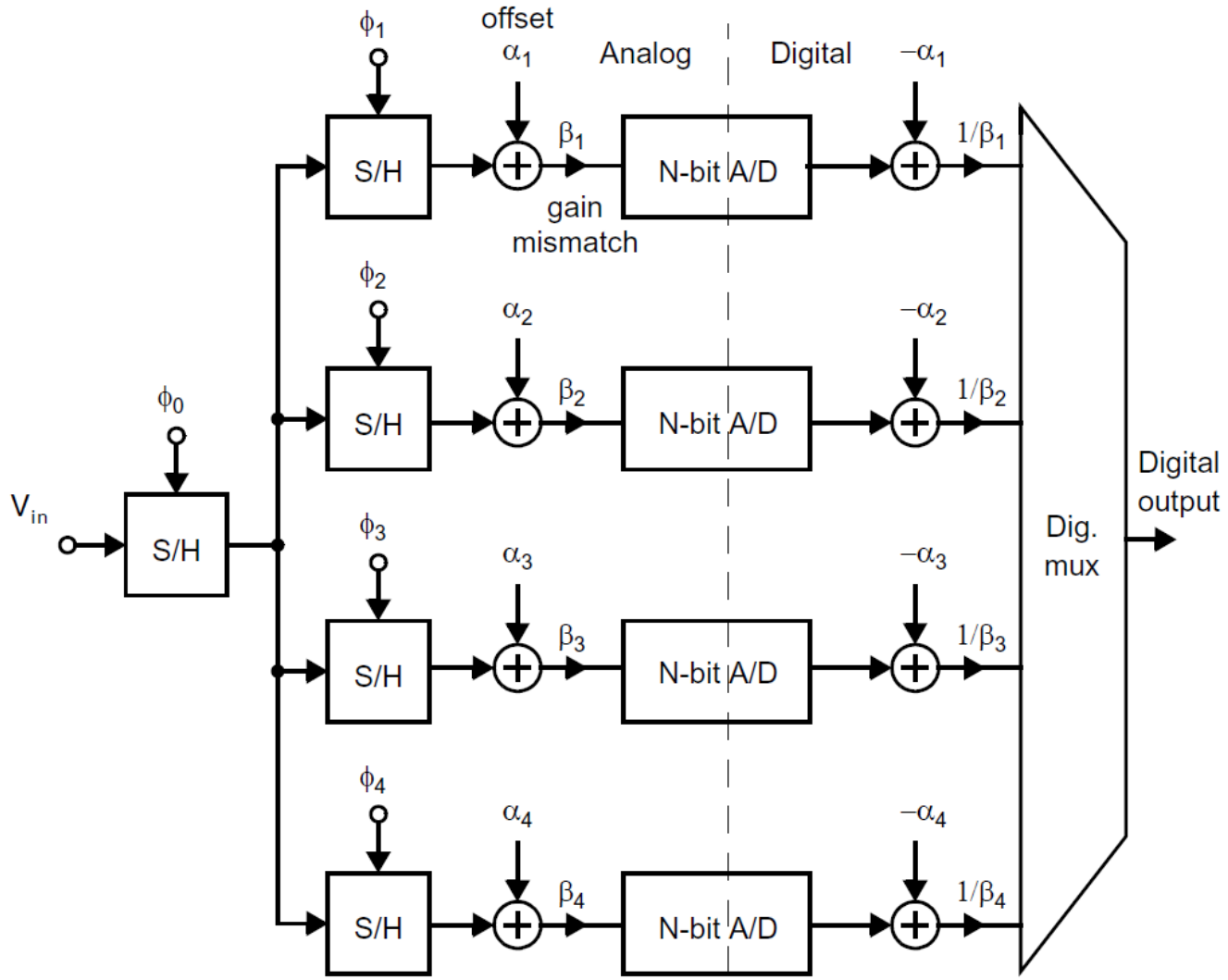
- A major limitation on the performance of time-interleaved converters is mismatch through the parallel signal paths in either their dc offset, gain, or sampling time.
  - dc offset that appears every 4 cycles will show as spur at fs/4
  - Gain errors mean that fin is multiplied (modulated) by a periodic signal



[Johns & Martin, 2012]

Time-Interleaved ADC

- If offset/gain errors can be accurately quantified, such errors can be cancelled digitally



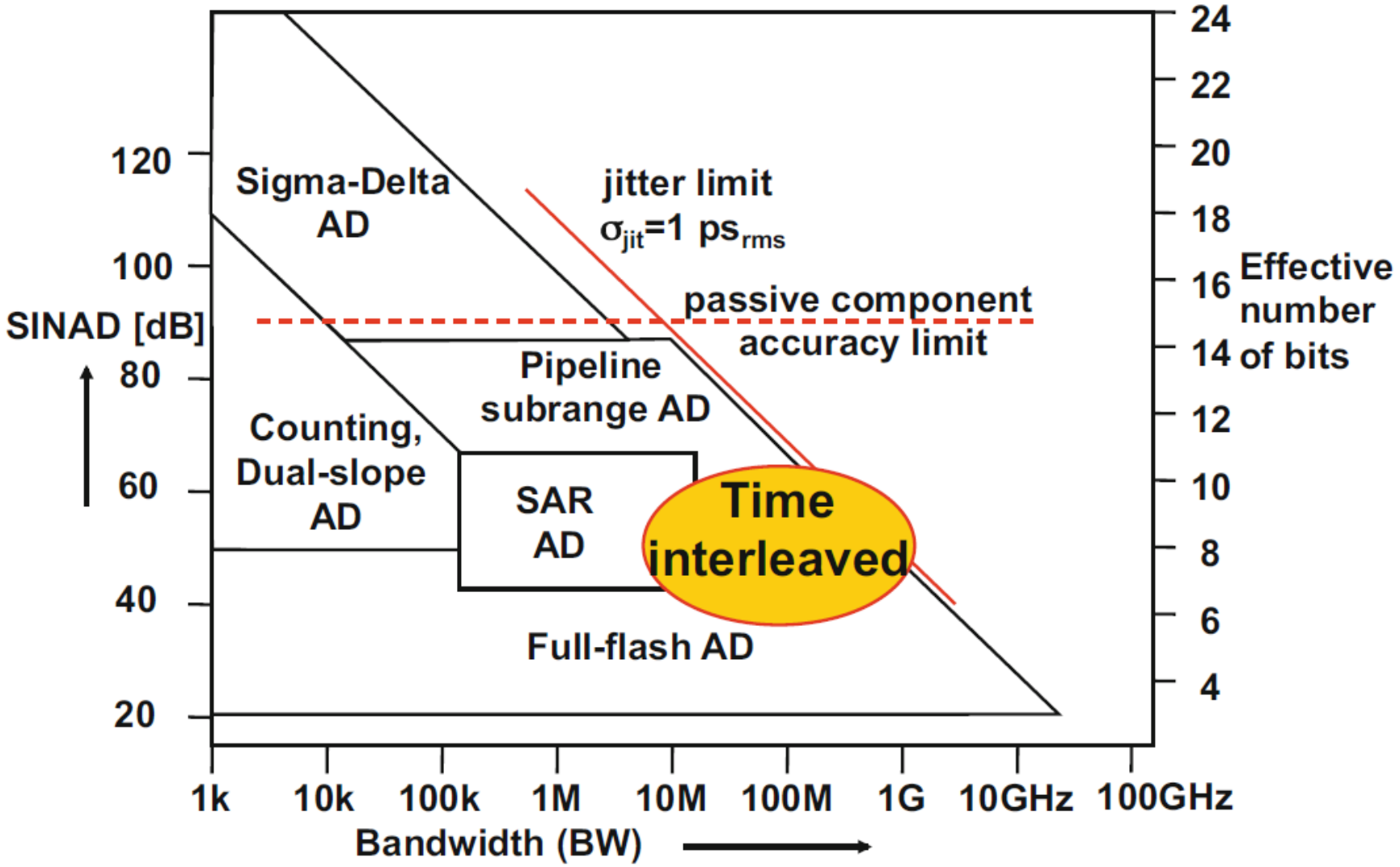
[Johns & Martin, 2012]

ADCs Comparison

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

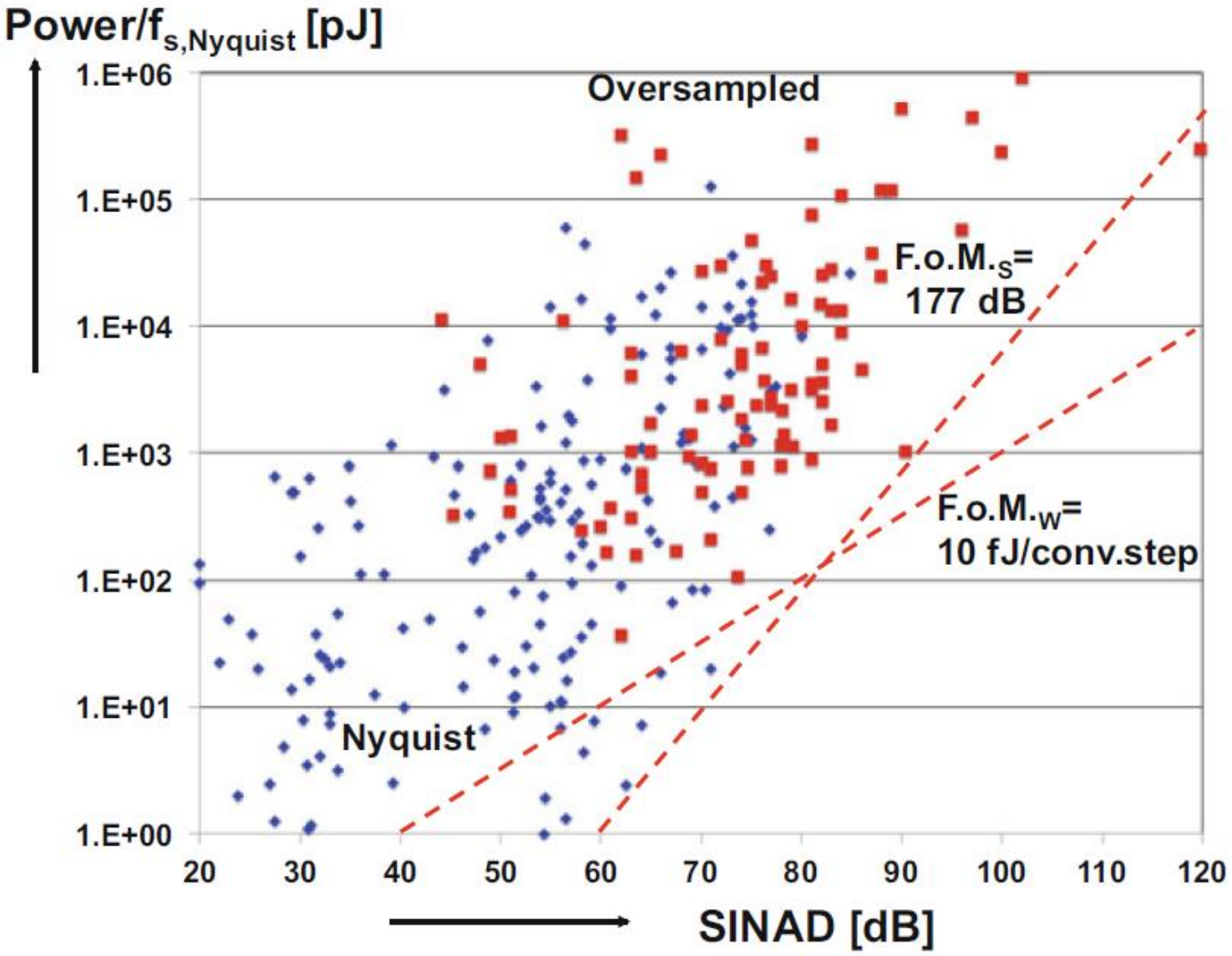
[Johns & Martin, 2012]

ADCs Comparison



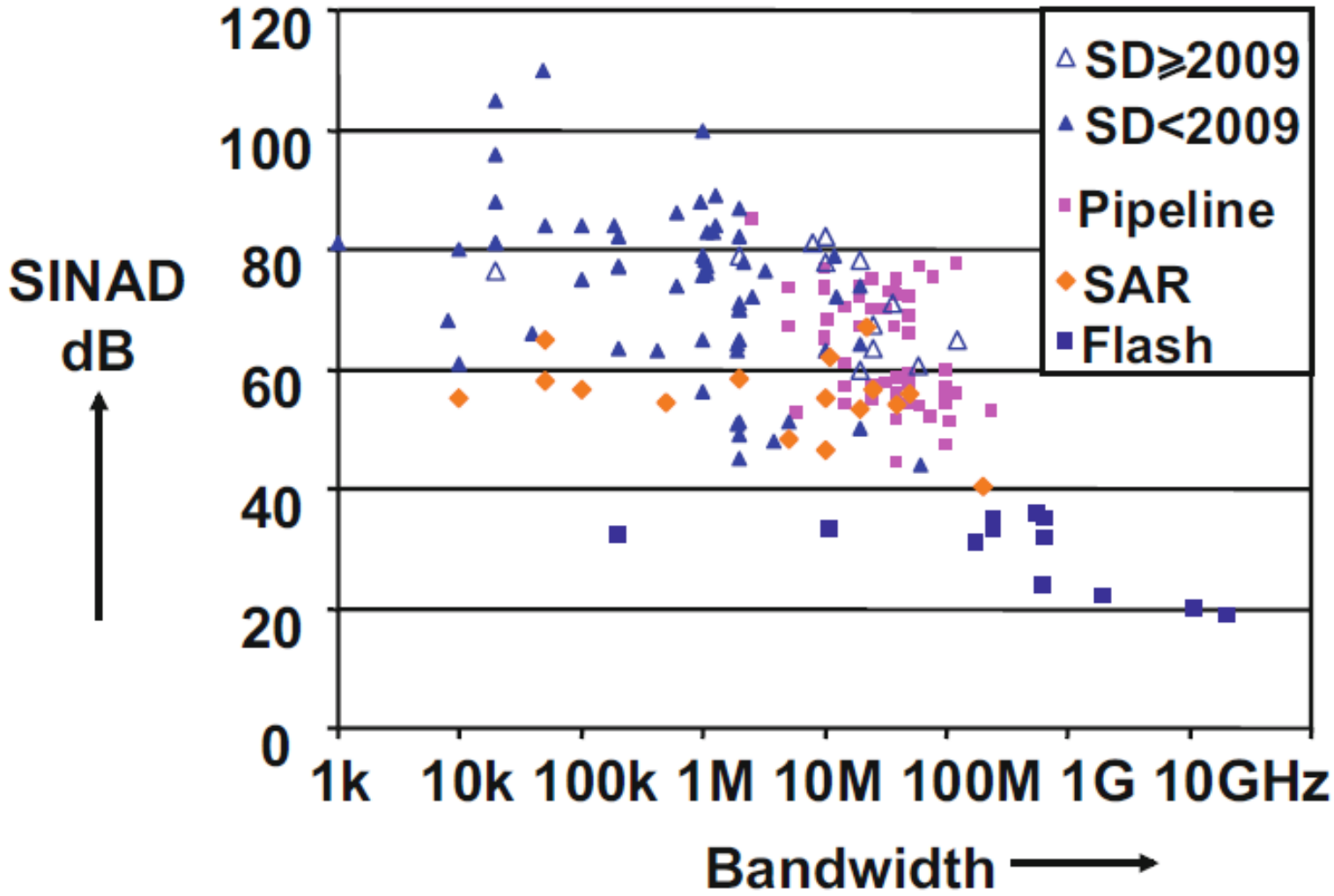
[M. Pelgrom, 2017]

ADCs Comparison



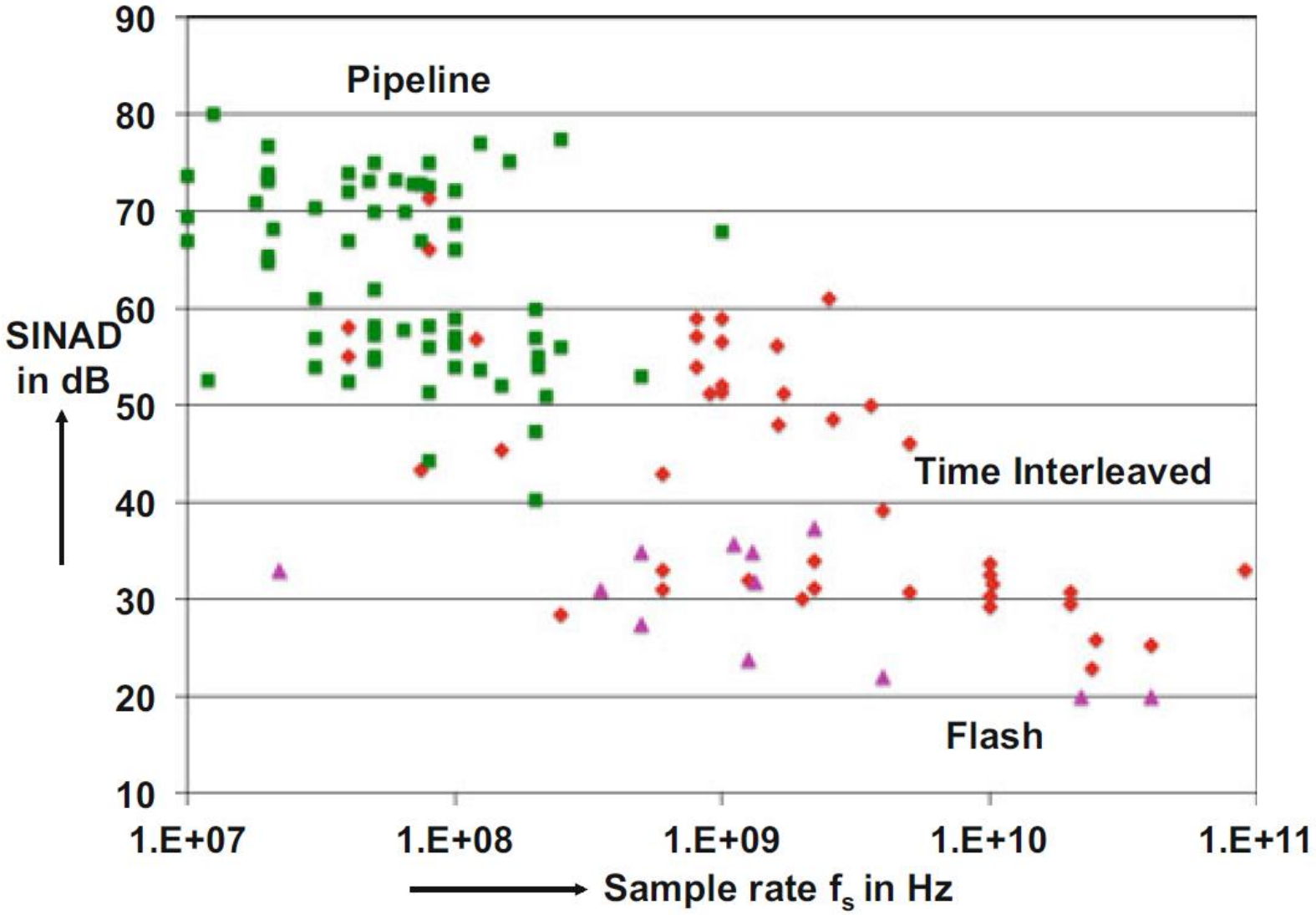
[M. Pelgrom, 2017]

ADCs Comparison



[M. Pelgrom, 2017]

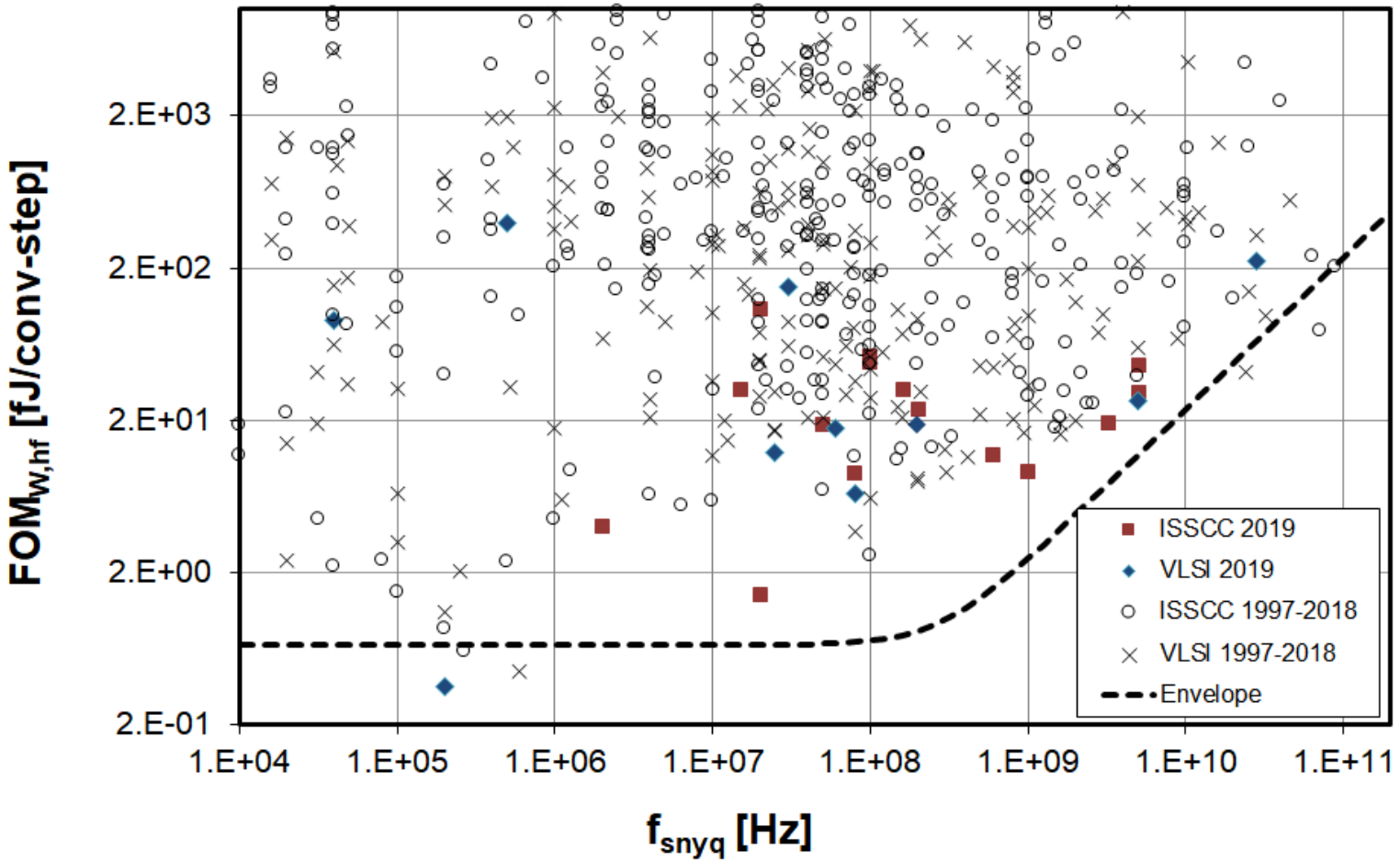
ADCs Comparison



[M. Pelgrom, 2017]

Walden FOM vs. Speed

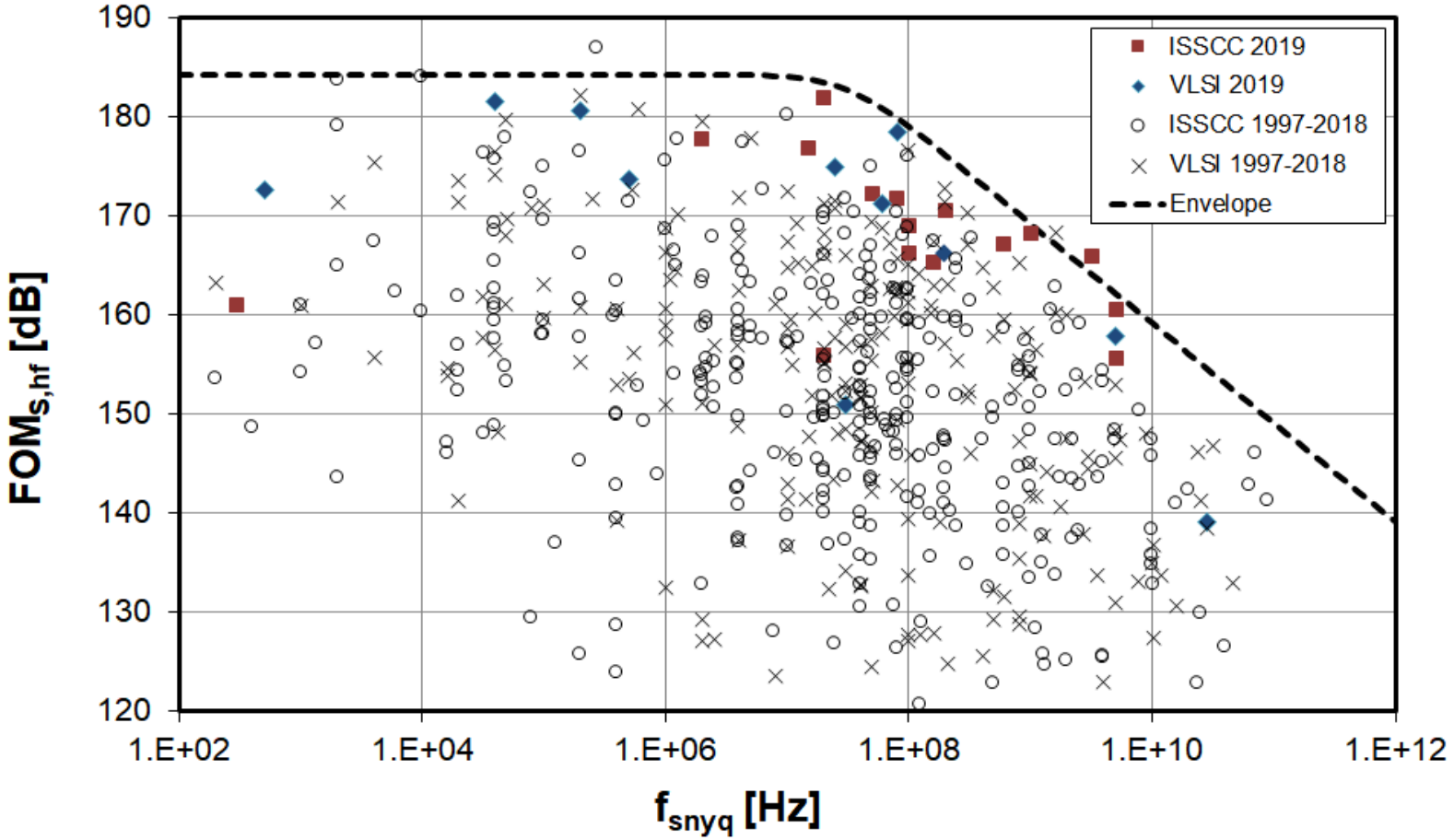
- Slower architectures (e.g., SAR) have better energy efficiency (better FoM)
  - Time interleaving extends good efficiency to higher speeds



[Murmann's Survey]

Schreier FOM vs. Speed

- Slower architectures (e.g., SAR) have better energy efficiency (better FoM)
  - Time interleaving extends good efficiency to higher speeds



ADCs Comparison

	FLASH (Parallel)	SAR	DUAL SLOPE (Integrating ADC)	PIPELINE	SIGMA DELTA
Pick This Architecture if you want:	Ultra-High Speed when power consumption not primary concern?	Medium to high resolution (8 to 20 bits), 5Msps and under, low power, small size.	Monitoring DC signals, high resolution, low power consumption, good noise performance ICL7106.	High speeds, few Msps to 100+ Msps, 8 bits to 16 bits, lower power consumption than flash.	High resolution, low to medium speed, no precision external components, simultaneous 50Hz/60Hz rejection, digital filter reduces anti-aliasing requirements.
Conversion Method	N bits - 2^{N-1} Comparators Caps increase by a factor of 2 for each bit.	Binary search algorithm, internal circuitry runs higher speed.	Unknown input voltage is integrated and value compared against known reference value.	Small parallel structure, each stage works on one to a few bits.	Oversampling ADC, 5Hz to 60Hz rejection programmable data output.
Encoding Method	Thermometer Code Encoding	Successive Approximation	Analog Integration	Digital Correction Logic	Over-Sampling Modulator, Digital Decimation Filter
Disadvantages	Sparkle codes/metastability, high power consumption, large size, expensive.	Speed limited to ~5Msps. May require anti-aliasing filter.	Slow Conversion rate. High precision external components required to achieve accuracy.	Parallelism increases throughput at the expense of power and latency.	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC.
Conversion Time	Conversion Time does not change with increased resolution.	Increases linearly with increased resolution.	Conversion time doubles with every bit increase in resolution.	Increases linearly with increased resolution.	Tradeoff between data output rate and noise free resolution.
Resolution	Component matching typically limits resolution to 8 bits.	Component matching requirements double with every bit increase in resolution.	Component matching does not increase with increase in resolution.	Component matching requirements double with every bit increase in resolution.	Component matching requirements double with every bit increase in resolution.
Size	2^{N-1} comparators, Die size and power increases exponentially with resolution.	Die increases linearly with increase in resolution.	Core die size will not materially change with increase in resolution.	Die increases linearly with increase in resolution.	Core die size will not materially change with increase in resolution.

[https://www.maximintegrated.com/en/app-notes/index.mvp/id/2094]

References

- B. Murmann, “ADC Performance Survey 1997–20xx,” Online: http://web.stanford.edu/~murmann/adcsurvey.html
- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.
- Y. Chiu, EECT 7327, UTD.

Thank you!