AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics & Comm. Eng. Dept.

Examination Date: 14-Nov-2018 ***Allowed Time: 90 minutes***

CHEP: ECE 486: Analog Integrated Systems Design
Midterm Exam

The exam consists of 3 questions in 3 pages ***Total Marks: 25 Marks***

Question (1) [8 points]

The figures below show some performance characteristics for a state-of-the-art ADC from ADI. The ADC sampling rate is 3 GS/s and the full-scale differential input is 1.7 Vpp.

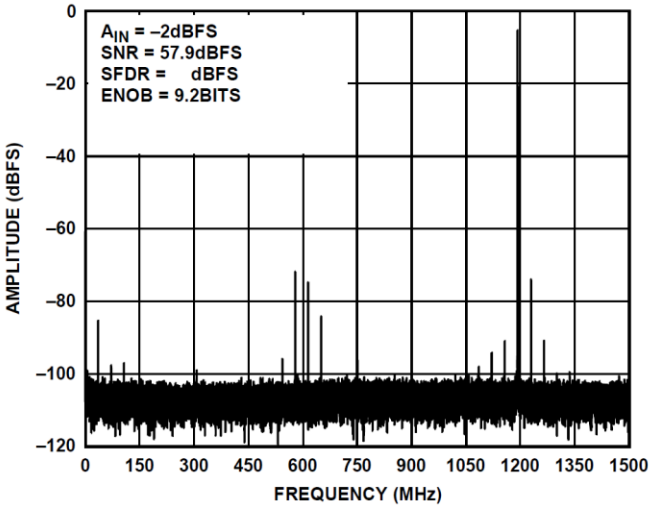

Figure 1.1

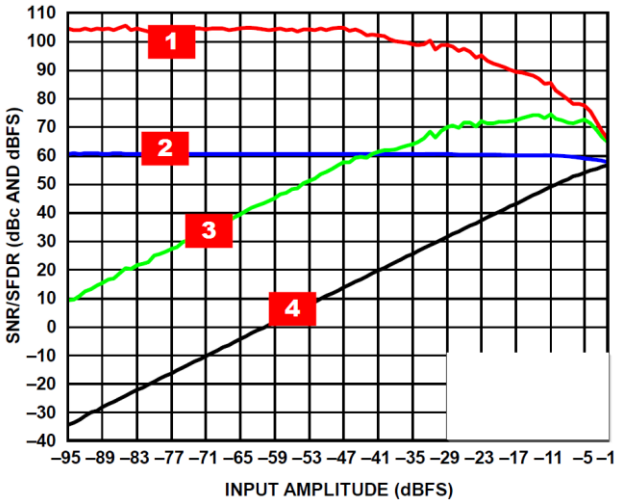

Figure 1.2

a) [1 point] Calculate the test frequency used for Figure 1.1 given that it is located in the 2nd Nyquist zone (fs/2 to fs).
b) [1 point] From Figure 1.1, calculate the SFDR in dBFS.
c) [1 point] Calculate the number of points used for the FFT in Figure 1.1.
d) [1 point] Choose the best answer: The resolution of this ADC is (10, 14, 18) bits.
e) [4 points] Figure 3.2 shows four curves for the SNR and SFDR in dBc and dBFS. Determine which is which (justify your answer).

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Question (2) [9 points]

A 3-bit ADC is tested using code density (histogram) test with a linear ramp as an input signal. The sampling frequency is 1 MHz. The table below shows the test results.

Code	0	1	2	3	4	5	6	7
# of hits	330	72	61	89	112	139	129	270

f) [2 points] Plot the DNL vs code (annotate the DNL values on the plot).
g) [2 points] Plot the INL vs code (annotate the INL values on the plot).
h) [2 points] Assume a ~1.2 MHz input test tone is applied to this ADC, and the output is plotted by FFT. What is the frequency at which the highest distortion component will appear? (Hint: You can determine the type of distortion from the INL plot.)
i) [1 point] Can we measure DNL/INL with 0.05 LSB resolution using the given test results? What is the best DNL/INL resolution that can be obtained from this test?
j) [1 point] Calculate the total time that was required by this code density test.
k) [1 point] Can you deduce if this ADC is monotonic or not? Why?

Question (3) [8 points]

Figure 3.1 and Figure 3.2 show two switched capacitor circuits. Answer the following questions **<u>for each circuit</u>**:

Hint: The analysis can be simplified by using the half circuit principle.

a) [2 points] Find the transfer function Vout/Vsig (in z-domain). What is the function of this circuit?
b) [2 points] Assume the input is a ramp that goes from 0 to 100mV in five clock cycles, $C_S = 2pF$ and $C_F = 1pF$. Plot the input and output waveforms.
c) [2 points] Find the transfer function Vout/Vos (in z-domain), where Vos is the offset voltage. Use half circuit principle and assume Vos is applied to the OTA non-inverting terminal.
d) [2 points] Compare the two circuits by stating one advantage and one disadvantage for each circuit.

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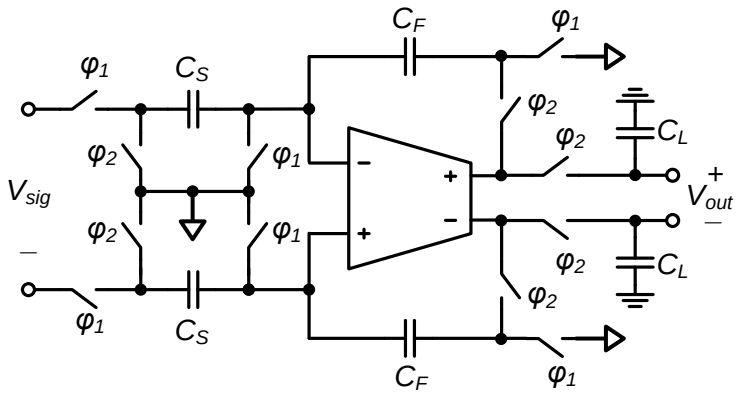

Figure 3.1

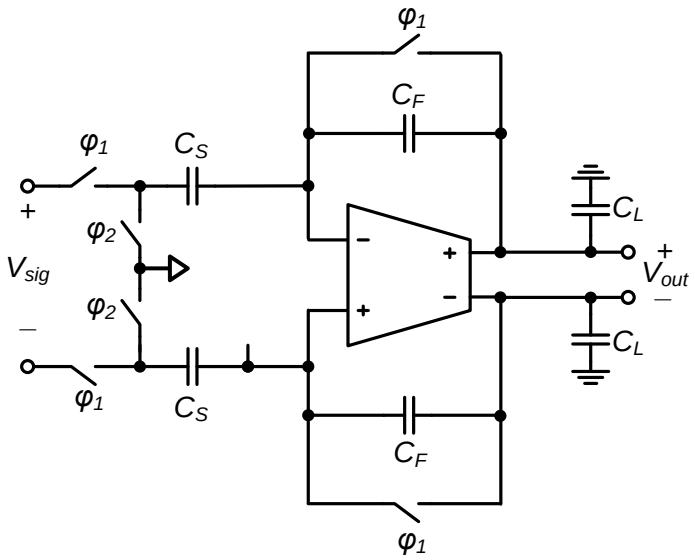

Figure 3.2