Analog Integrated Systems Design

Lecture 08
Basics of Switched Capacitor Circuits

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Switched Capacitor Circuits

- Switched cap circuits is the most popular approach for realizing analog signal processing in CMOS ICs
- Analog signals are sampled and stored on capacitors
  - Charge is transferred from one capacitor to another
  - Discrete time (DT) analog signals (z-transform)
  - Require anti-aliasing and smoothing filters when combined with continuous time (CT) circuits
- Most important applications:
  - Data converters
  - Precision gain stages (amplifiers)
  - DT analog filters

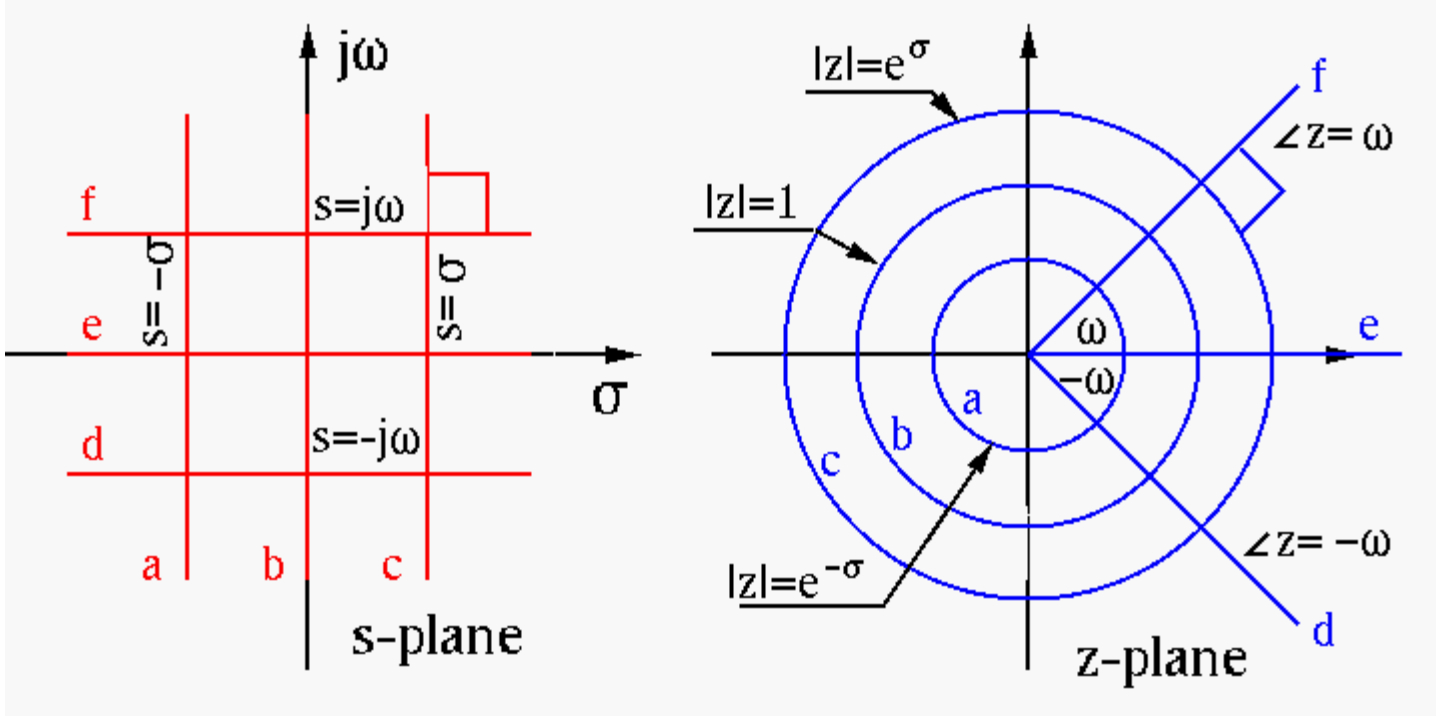
S-Plane vs Z-Plane

$$z = e^{sT_s} = e^{(\sigma + j\omega)/f_s}$$

- Assume $f_s = 1$ (normalized)

$$|z| = e^{\sigma}$$
$$\angle z = \omega$$

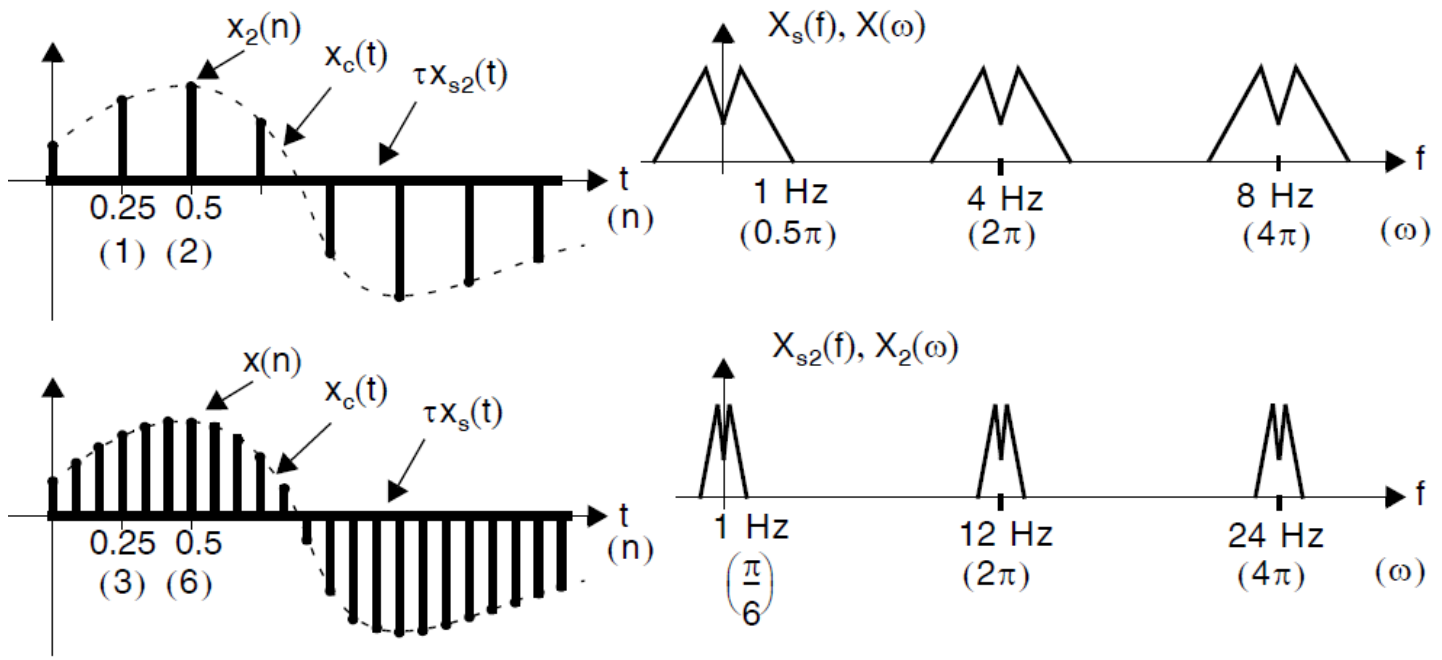
- RHP in s-domain maps to outside unit circle in z-domain



[http://fourier.eng.hmc.edu/e102/lectures/Z_Transform/node2.html]

DT Frequency Spectrum

- Z-transform is periodic with period = 2π
  - 2π is the normalized representation of $\omega_s = 2\pi f_s$
- Ex: spectrum of a signal with $BW = 1Hz$ sampled at
  - $f_s = 4Hz$
  - $f_s = 12Hz$



Switched Cap Circuit Building Blocks

- Op-amps (OTAs)
- Capacitors
- Switches
- Non-overlapping clocks

Op-amps (OTAs)

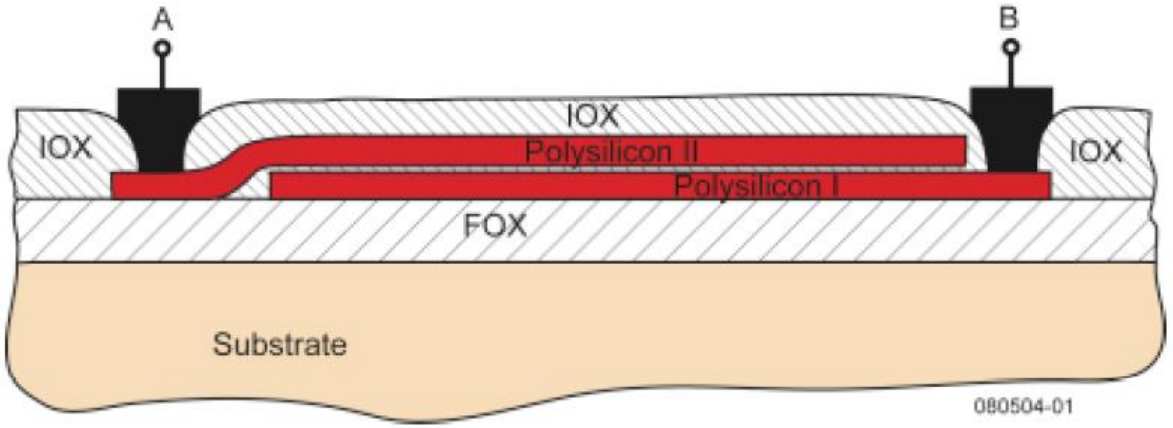
- OTA imperfections impact switched cap circuits performance
  - DC gain (typically require 40 dB to 80 dB)
  - GBW (UGF) (typically GBW > 10*fs)
  - PM (typically > 70deg)
  - Slew rate (SR)
  - Offset
  - Noise

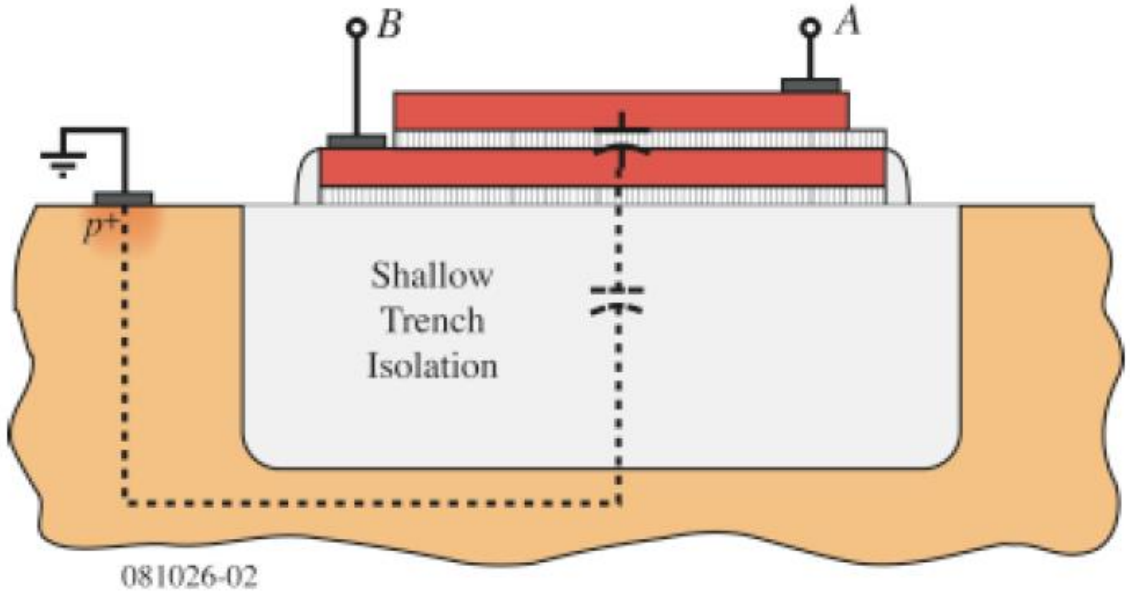
Capacitors

- Very well matched capacitors can be fabricated on-chip (mismatch < 0.1%)
- The absolute variation of capacitors is much less than the absolute variation of resistors
- Capacitors voltage and temperature dependence is much better than resistors dependence
- Unit capacitors can range from sub-fF to few pF
- Types of capacitors:
  - Poly-insulator-poly (PIP): Not used beyond $0.18\mu m$ node
  - Metal-insulator-metal (MIM): Vertical field
  - Metal-oxide-metal (MOM): Lateral and vertical field
  - MOSCAP: highest density, but highly non-linear

PIP Capacitor

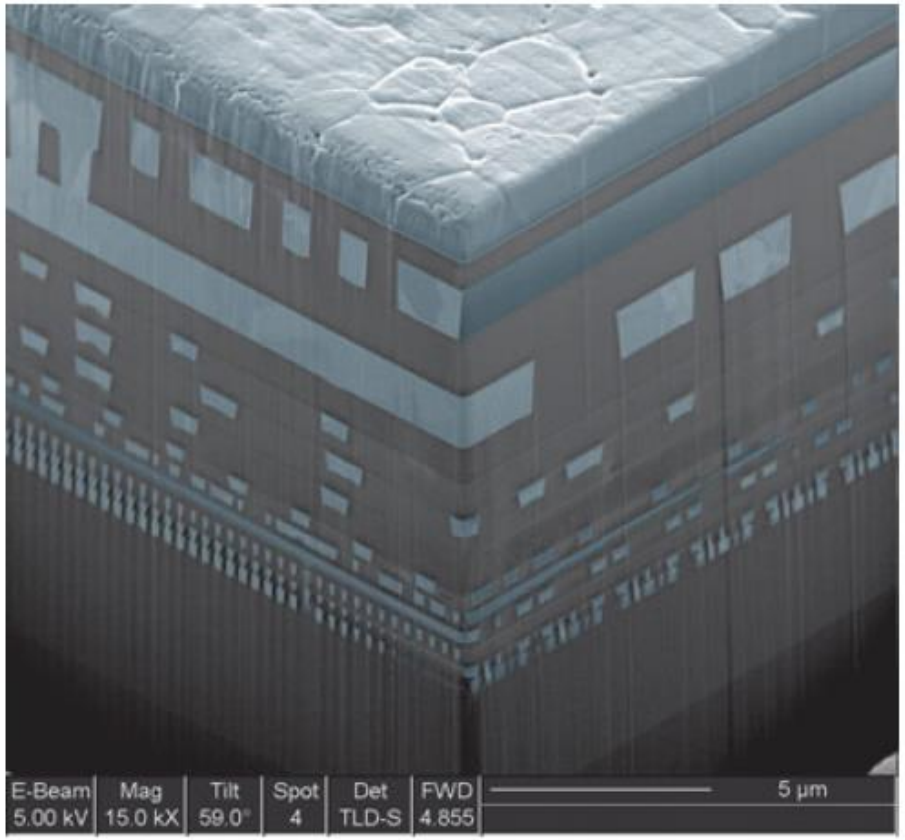
- Poly-insulator-poly (PIP)

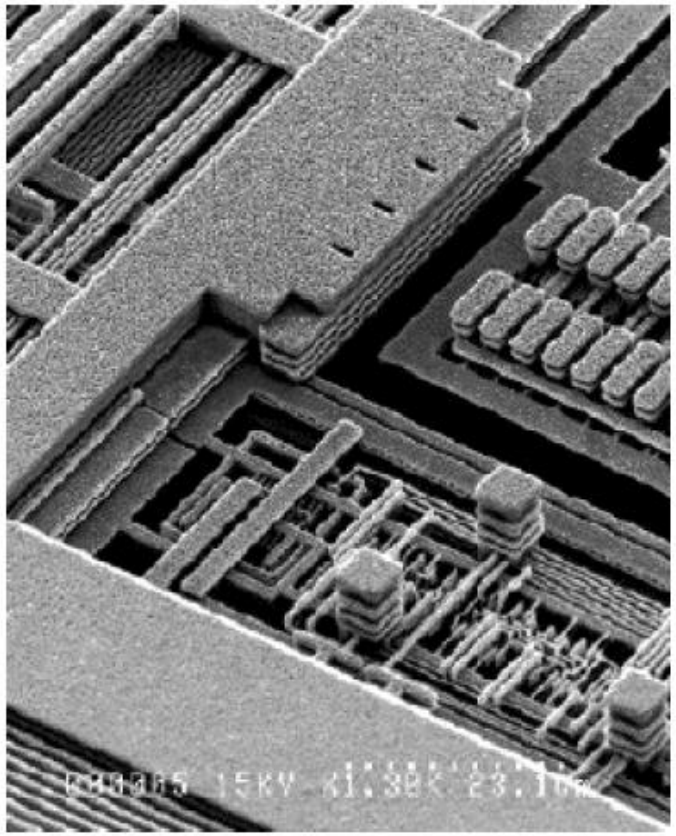




Metallization

- Old processes used Aluminum (Al)
- New technologies use Copper (Cu) for its lower resistivity
- Top metal layers are usually thicker for global interconnects

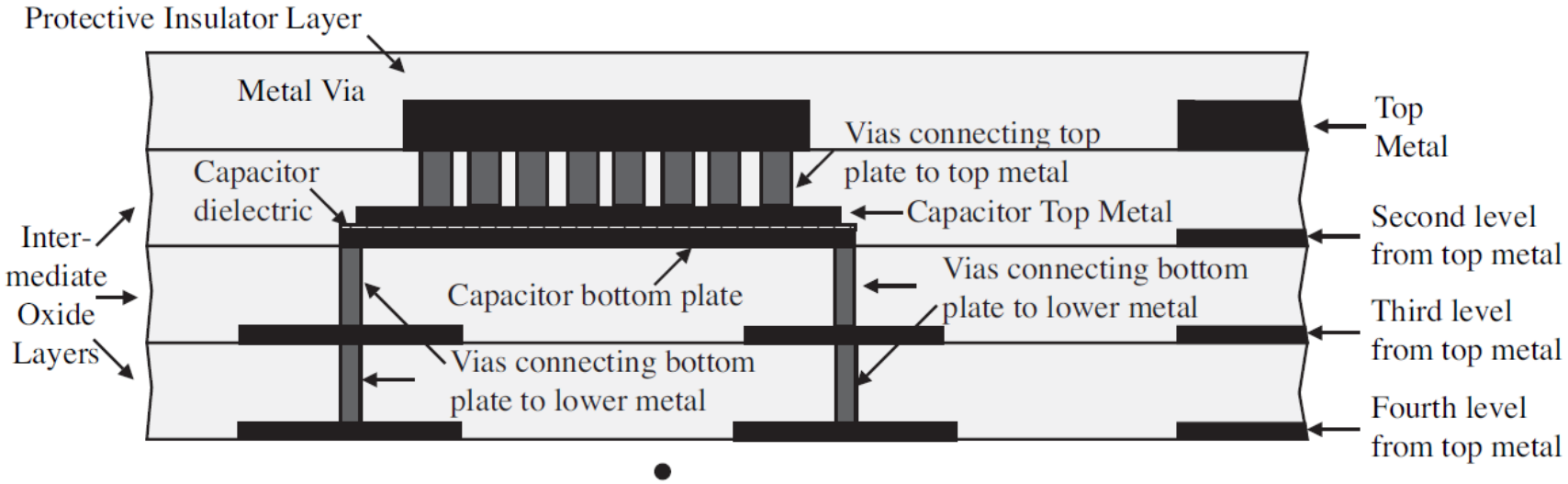




[Harris, 2010]

MIM Capacitor

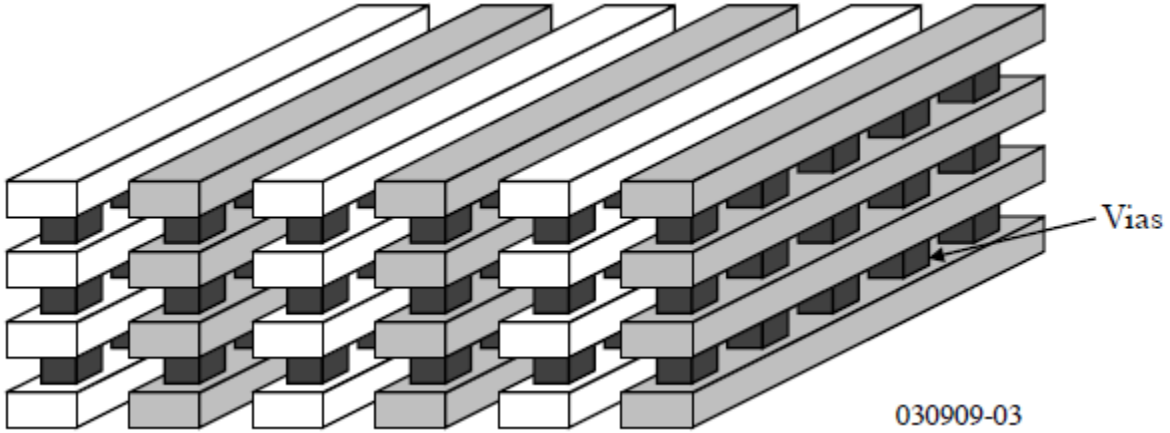
- Metal-insulator-metal (MIM)

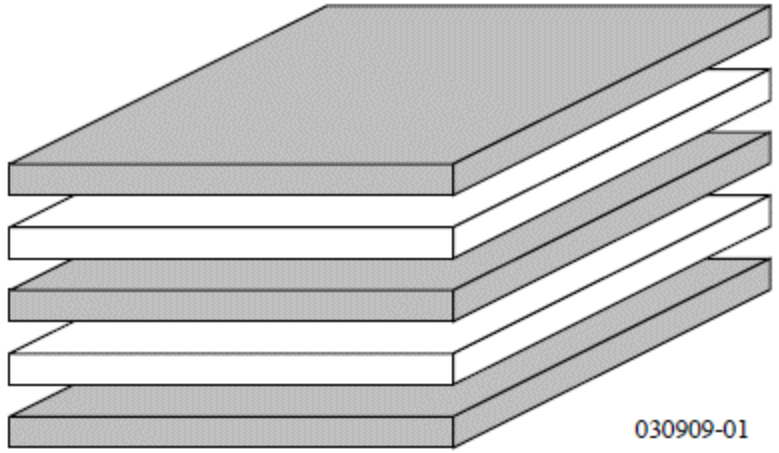


[P. E. Allen, 2010]

MOM Capacitor

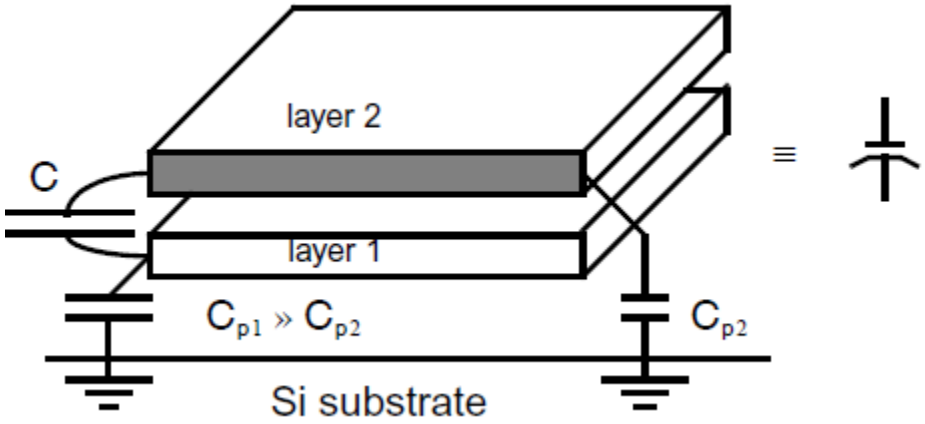
- Metal-oxide-metal (MOM): Lateral and vertical flux

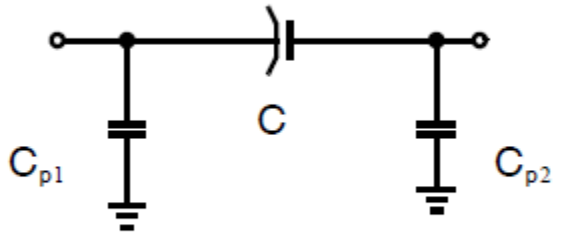




Capacitor Specs

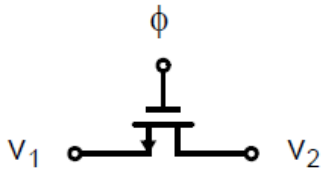
- Highly linear capacitance is required → Low voltage coefficient
  - PIP, MIM, and MOM have very good linearity
    - Voltage coefficient less than -100 ppm/V (usually negligible)
    - Good up to 16-bit
  - MOSCAP is highly non-linear (may be OK for less than 8-bit)
- Small parasitics are required:
  - For PIP and MIM: bottom plate cap be 20% of the desired cap
  - For lateral field MOM parasitics are balanced

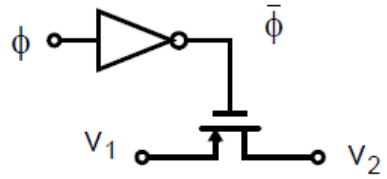


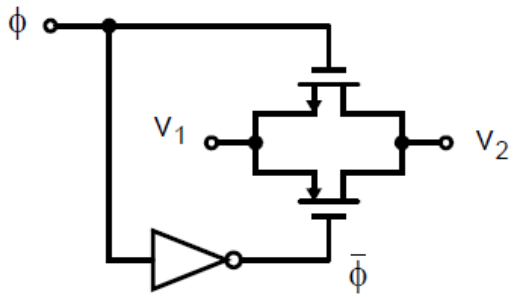


Switches

- Switches imperfections:
  - Input dependent resistance
    - Mitigated by using CMOS switch and/or bootstrapping
  - Channel charge injection
    - Mitigated by using bottom plate sampling and dummies
  - Clock feedthrough: Capacitive coupling from the clock
    - Mitigated by using fully differential architecture
  - Nonlinear junction capacitance on each side of the switch
    - Mitigated by using parasitic insensitive structures



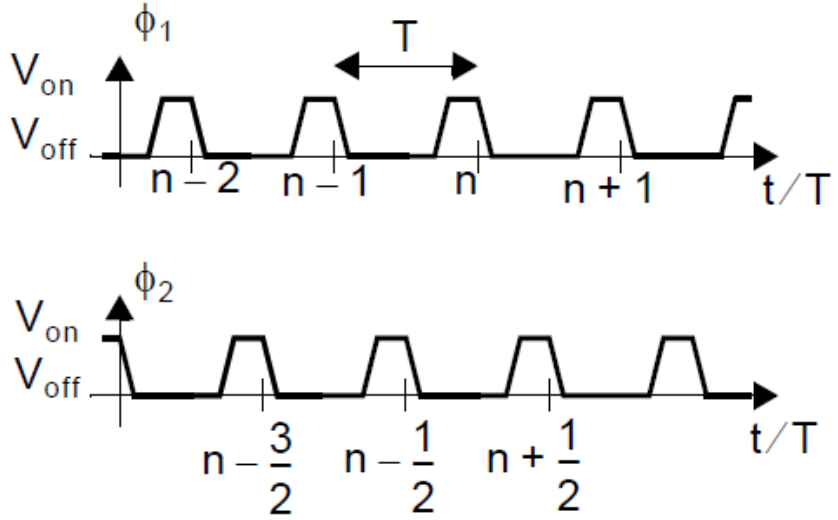




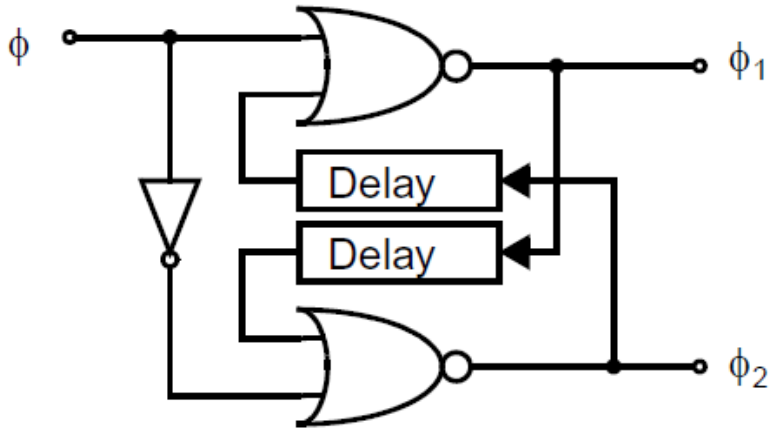
[Johns & Martin, 2012]

Non-overlapping Clocks

- Non-overlapping clocks: Φ_1 and Φ_2
  - Running at the same frequency BUT not simultaneously high
- Pulse width of Φ = T/2
  - Pulse width of Φ_1 and Φ_2 = T/2 - t_{delay}
- Non-overlapping time determined by inverter delays or RC network
  - Sensitive to process, voltage, and temperature (PVT) variations
  - High speed designs use delay locked loops (DLLs)



$$f_s \equiv \frac{1}{T}$$



Why not Continuous Time (CT)?

- Ex: CT integrator
  - Time constant: $\tau = R_1 C_1$
  - Absolute R and C are highly variable

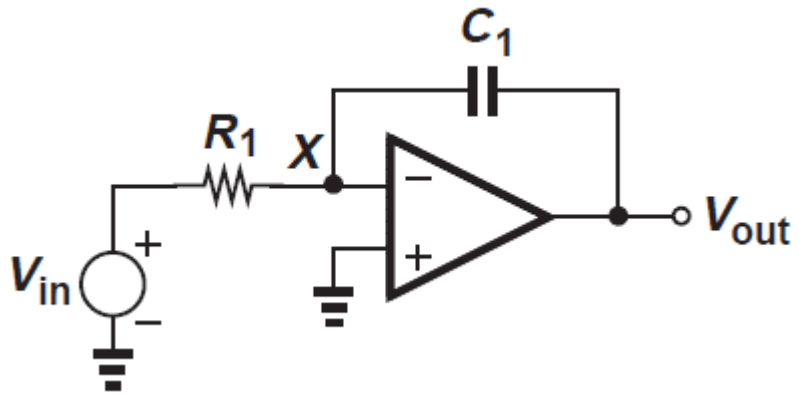
S-domain

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_1 s}}{R_1} = -\frac{1}{R_1 C_1 s}$$

Time-domain

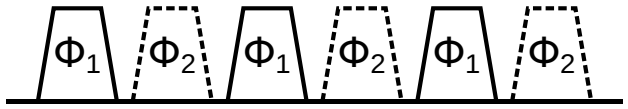
$$\frac{V_{in}}{R_1} = -C_1 \frac{dV_{out}}{dt}$$

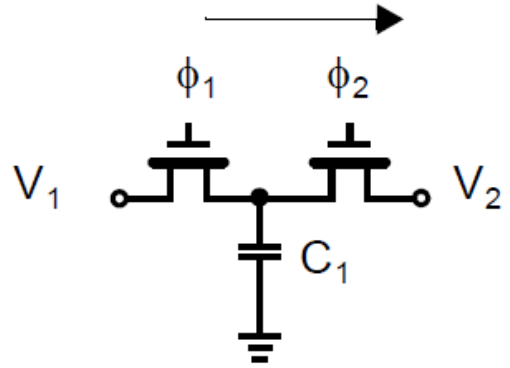
$$V_{out} = -\frac{1}{R_1 C_1} \int V_{in}\, dt$$



[Razavi, 2014]

Switched Capacitor Resistor Equivalence





$\Delta Q = C_1(V_1 - V_2)$ every clock period

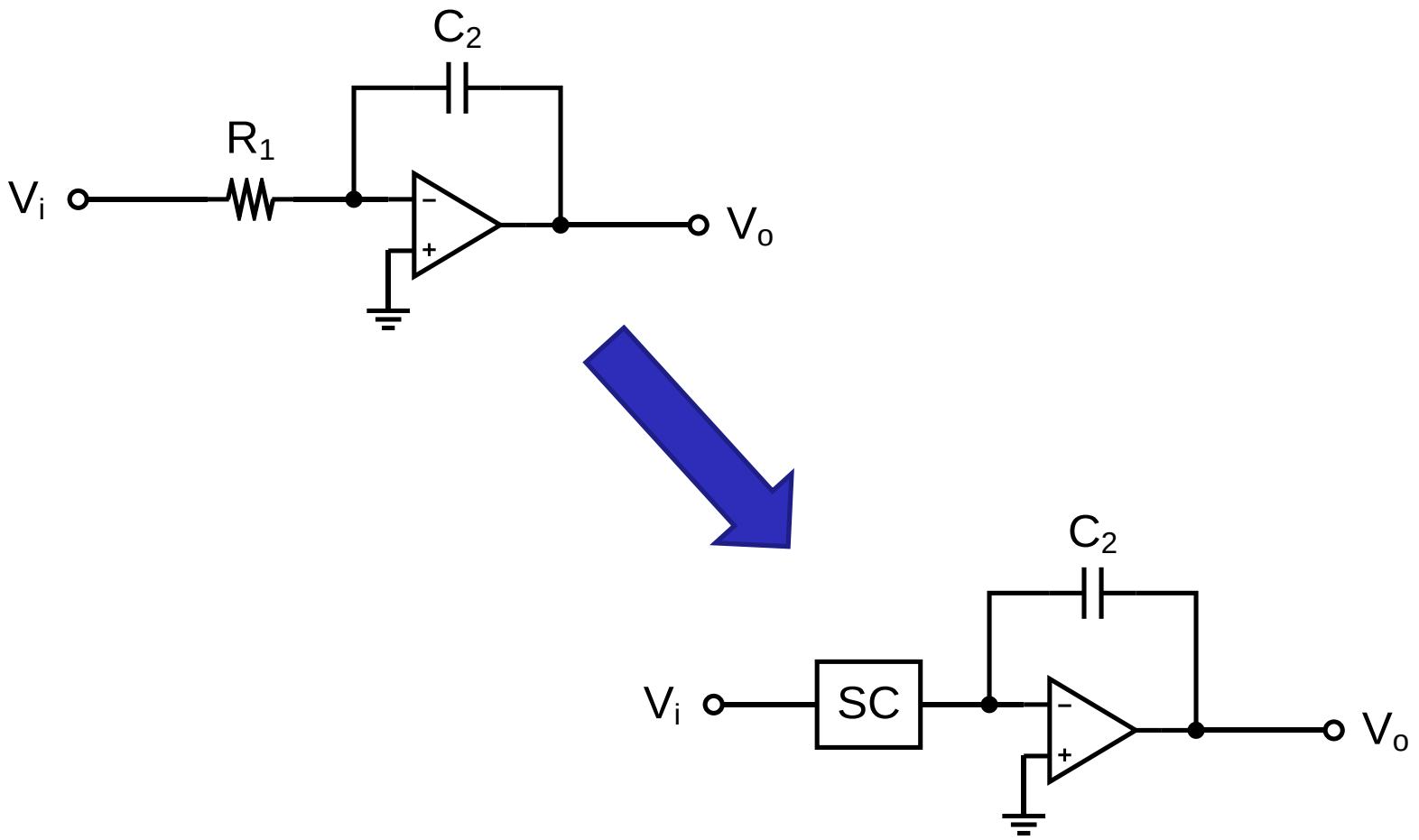
$$R_{eq} = \frac{T}{C_1}$$

$$I_{avg} = \frac{\Delta Q}{T} = \frac{C_1(V_1 - V_2)}{T} = \frac{V_1 - V_2}{R}$$

$$R = \frac{T}{C_1} = \frac{1}{f_s C_1}$$

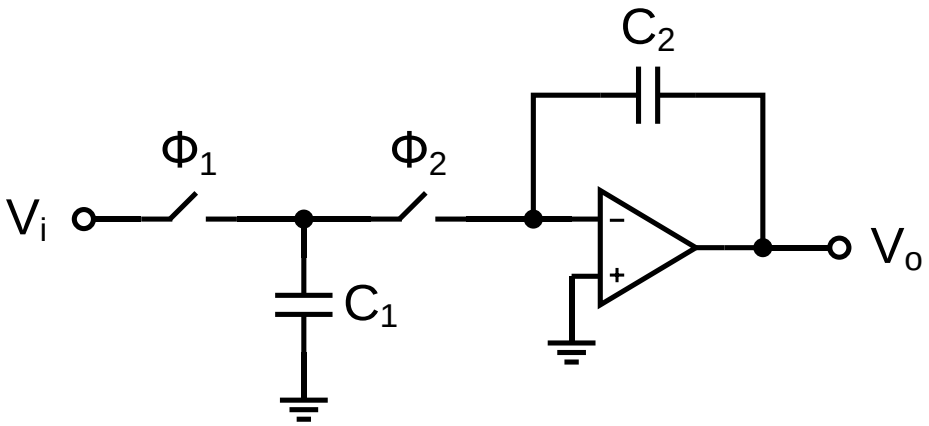
CT to Switched-Cap

- Replace resistors with switched capacitors

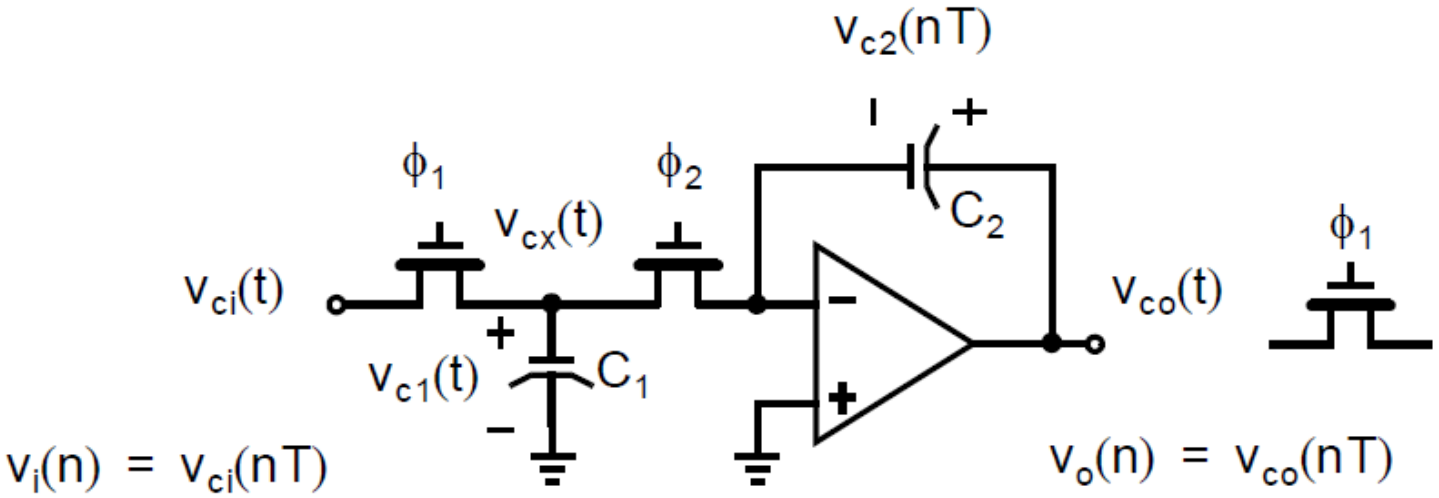


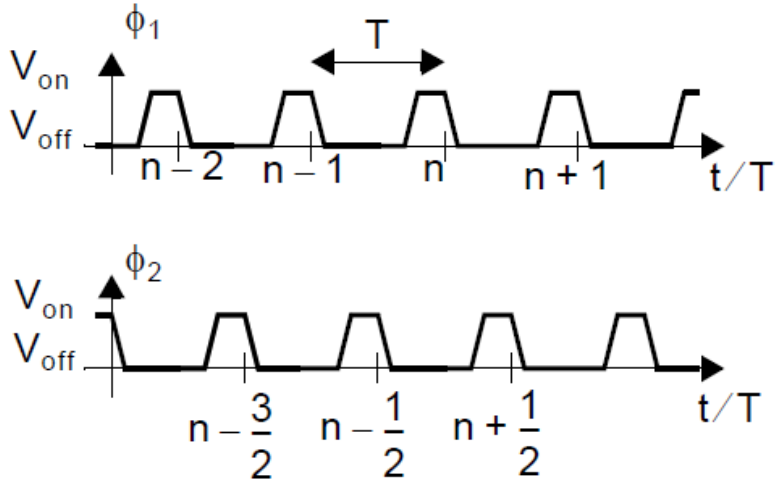
Switched-Cap DT Integrator

- Time constant: $\tau = R_1 C_2 = \frac{C_2}{f_s C_1}$
- τ determined by:
  1. Ratio of capacitors → matched caps → very precise
  2. f_s → crystal oscillator (and PLL) → very precise (and flexible)

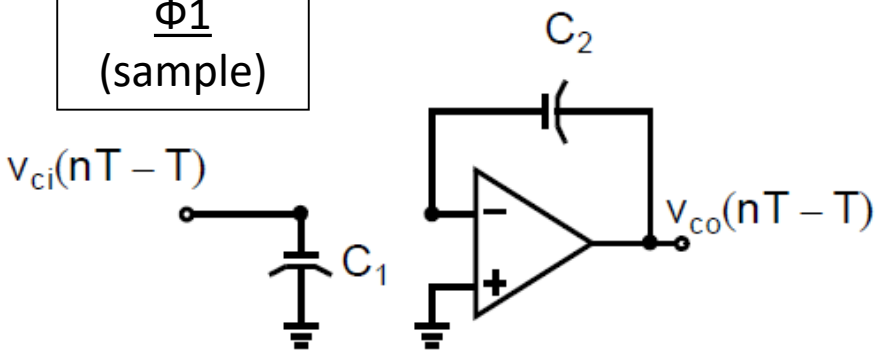


Switched-Cap Integrator

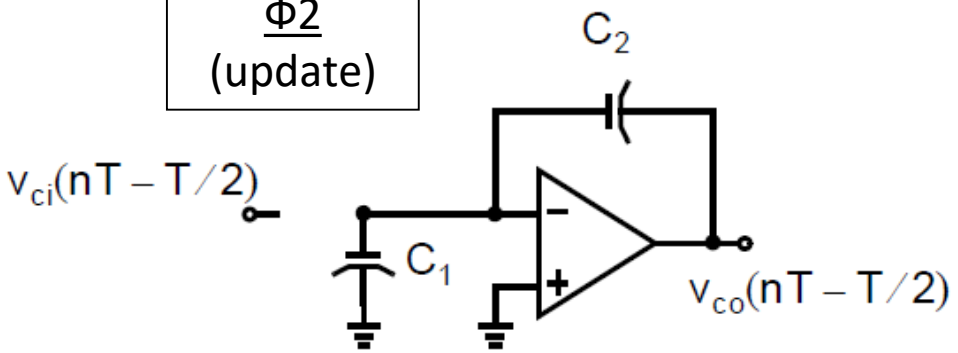




Φ1 (sample)



Φ2 (update)



Analysis in Charge Domain

- Apply charge conservation
  - But take care of charge polarity!

$$Total\ charge\ in\ \Phi_2 = Total\ charge\ in\ \Phi_1$$

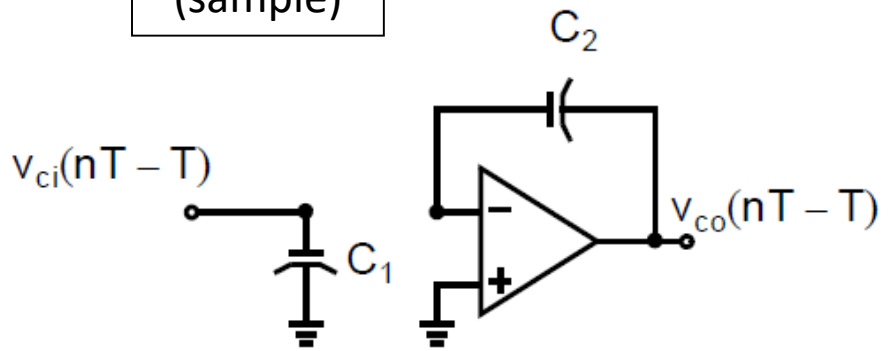
$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T)$$

$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n-1)$$

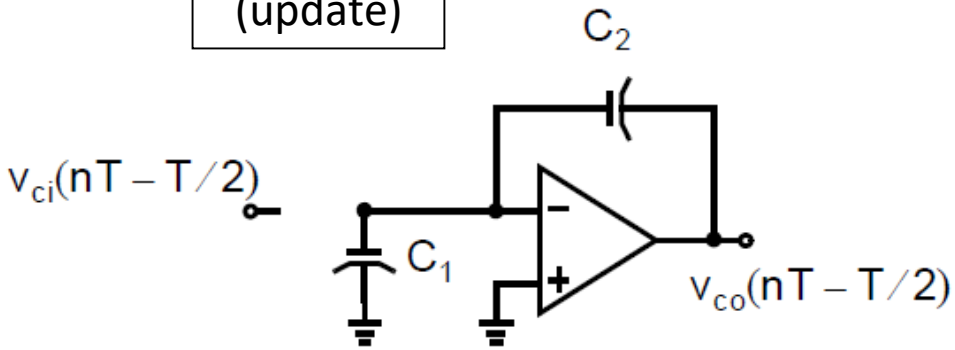
$$V_o(z) = z^{-1} V_o(z) - \frac{C_1}{C_2} z^{-1} V_i(z)$$

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{z^{-1}}{1 - z^{-1}} = -\left(\frac{C_1}{C_2}\right) \frac{1}{z - 1}$$

Φ1 (sample)

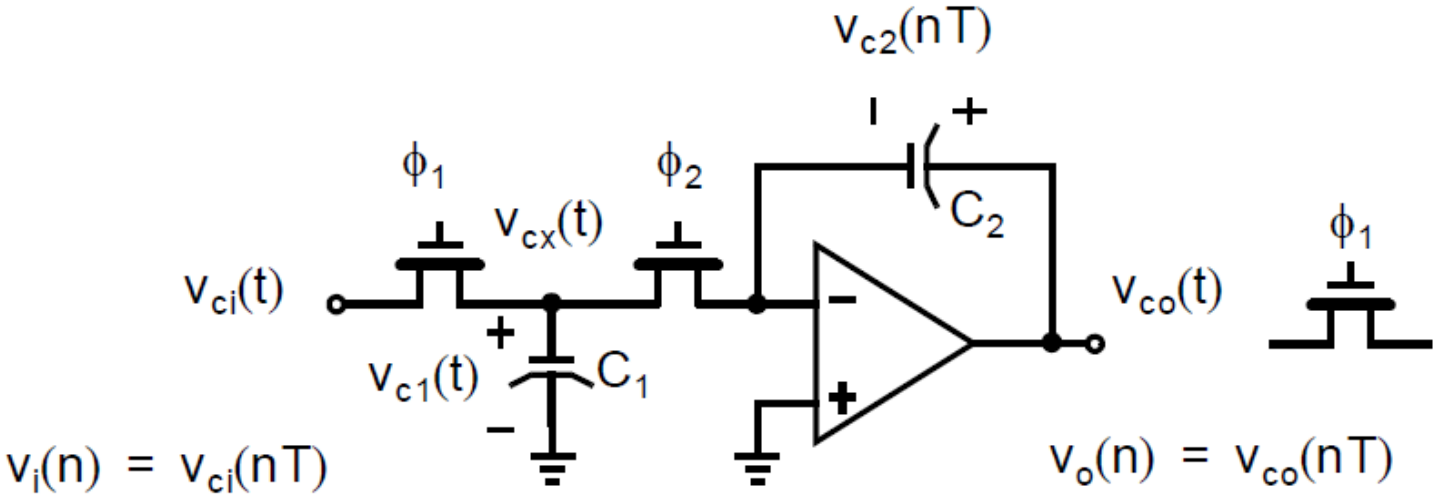


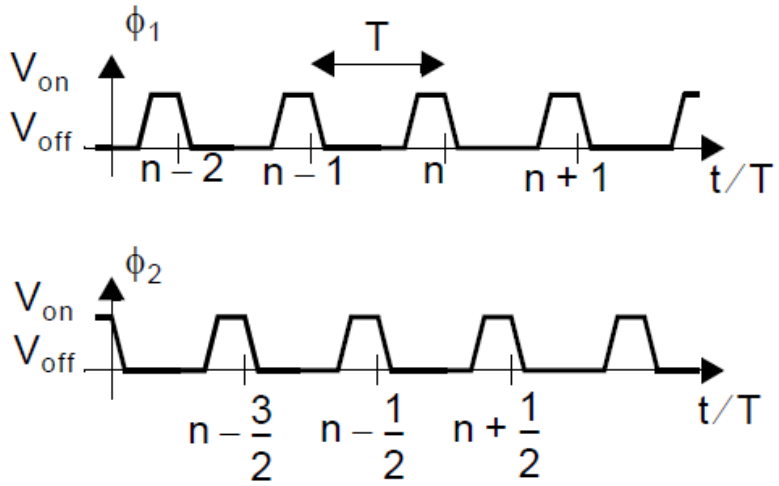
Φ2 (update)



Analysis in Voltage Domain

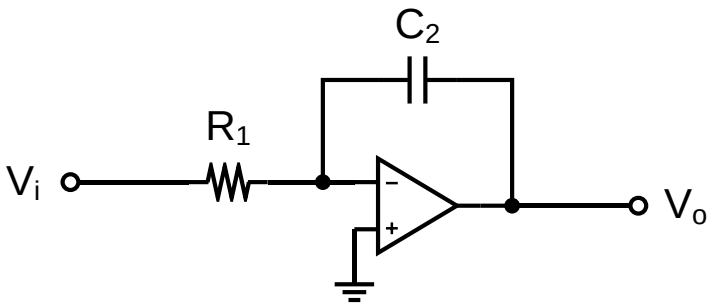
- Replace every charged cap with an uncharged cap in series with a voltage source
  - Apply circuit analysis laws (KVL and voltage divider) as usual

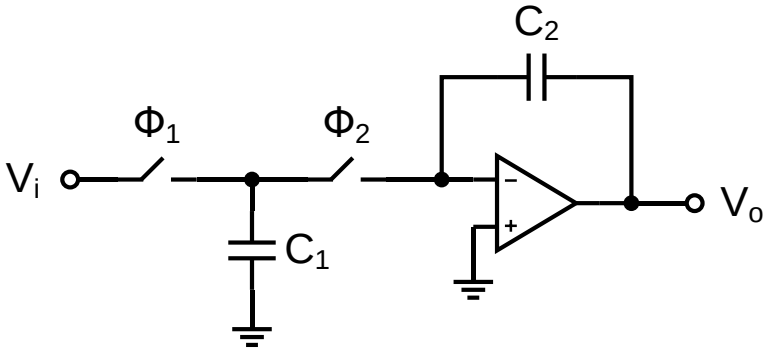




CT vs DT Integrator Step Response

- Assume $\tau = 1$ and $f_s = 1$ (normalized)
- Plot step response of CT and DT integrators

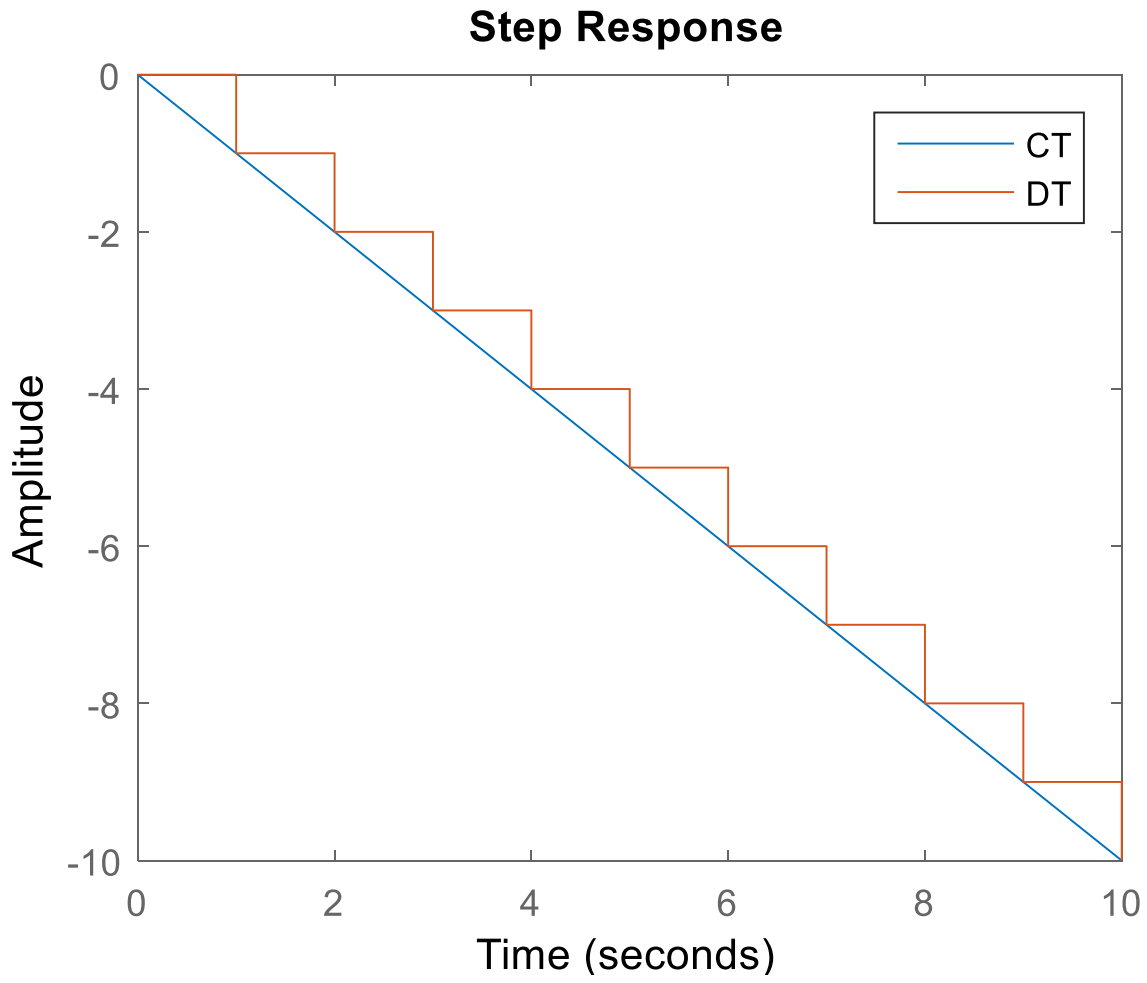




$$V_{out} = -\frac{1}{R_1 C_2}\int V_{in} dt$$

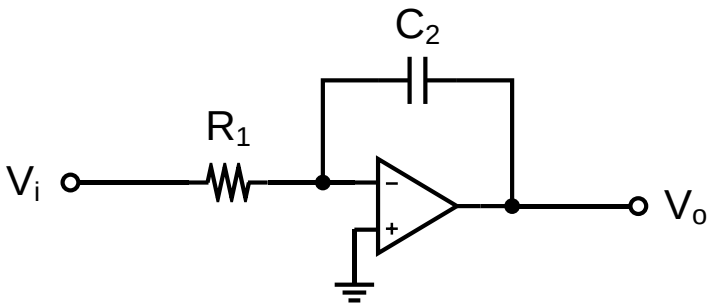
$$V_{out}[n] = -\frac{C_1}{C_2} V_{in}[n-1] + V_{out}[n-1]$$

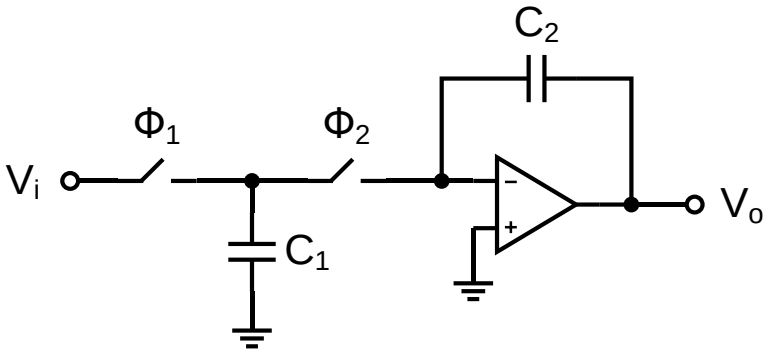
CT vs DT Integrator Step Response



CT vs DT Integrator Frequency Response

- Assume $\tau = 1$ and $f_s = 1$ (normalized)
- Plot pole-zero plot and frequency response of CT and DT integrators





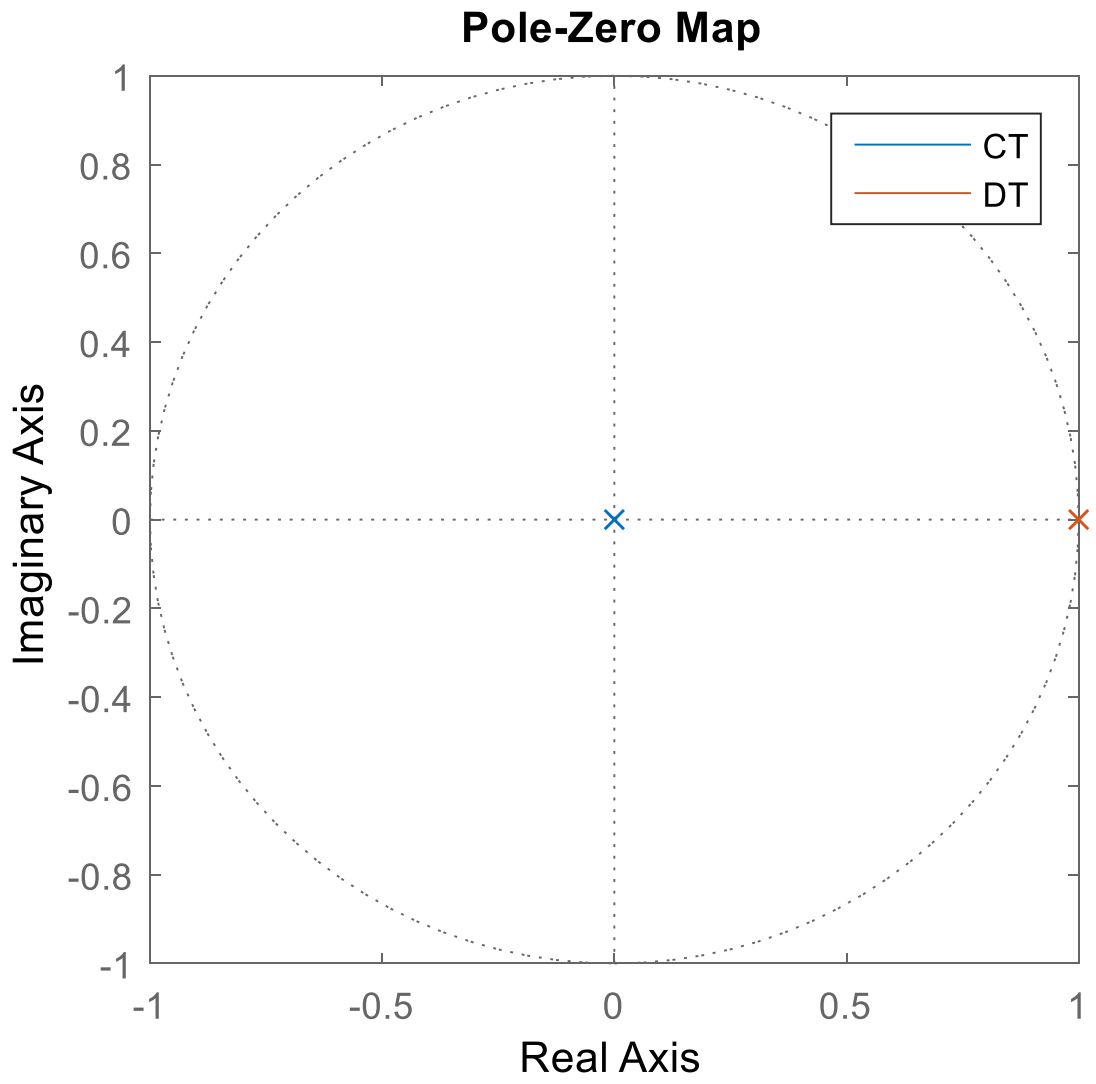
$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sR_1C_2}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{1}{z-1}$$

CT vs DT Integrator PZ Plot

$$H(s) = -\frac{1}{sR_1C_2}$$

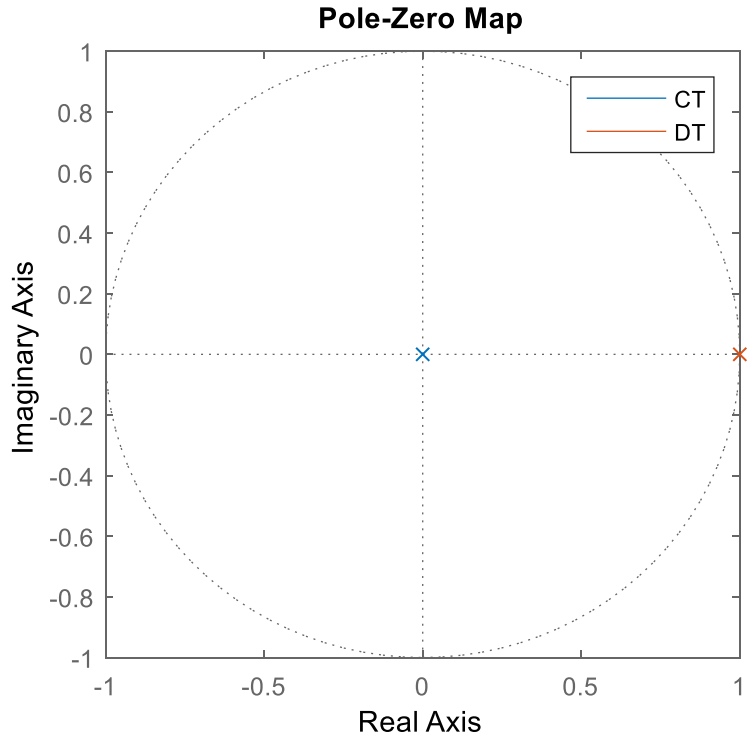
$$H(z) = -\frac{C_1}{C_2}\frac{1}{z-1}$$

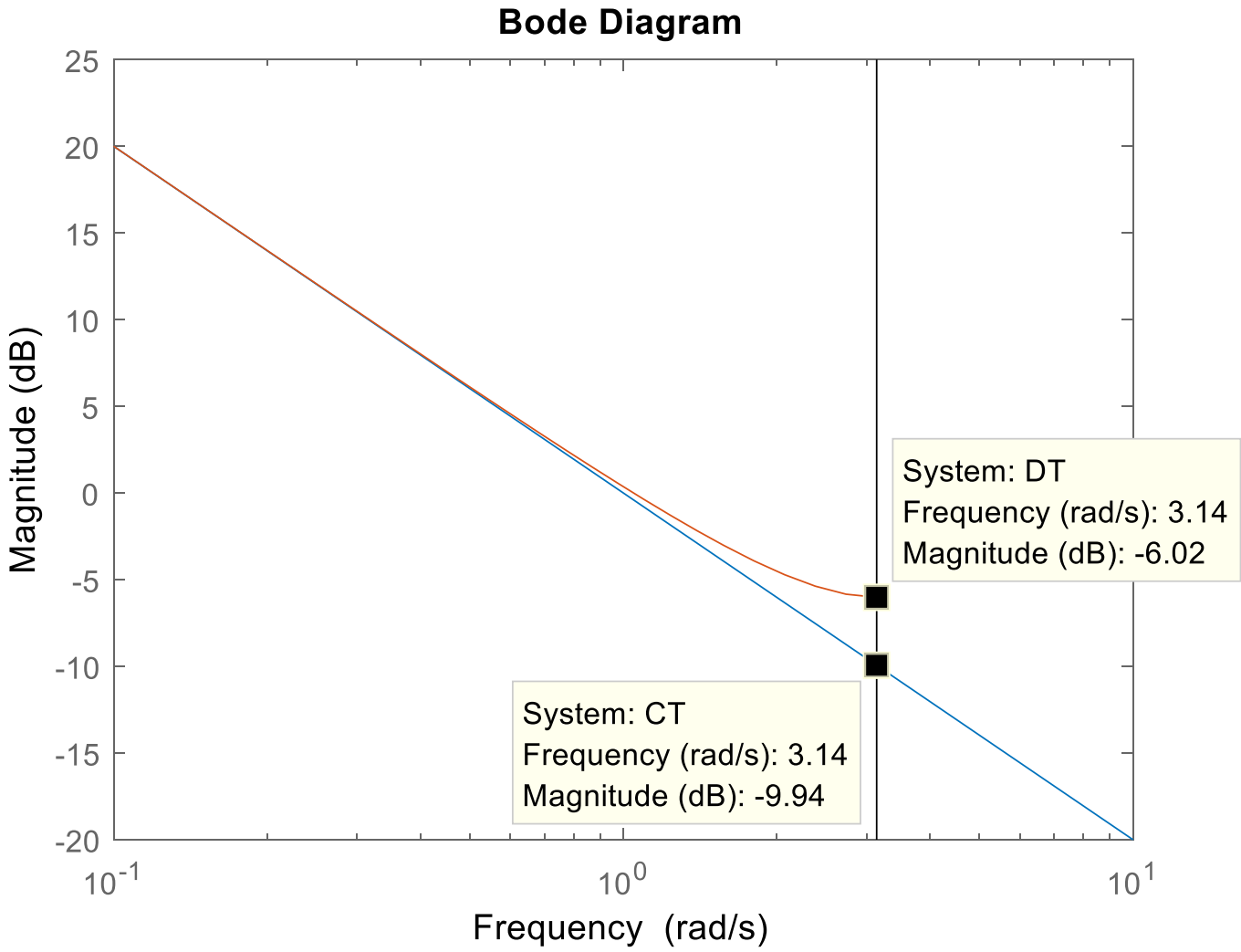


CT vs DT Integrator Frequency Response

$$|H(s=j\omega)| = \frac{1}{\|\vec{s}-\vec{p}\|} = \frac{1}{\|\overrightarrow{ps}\|}$$

$$\left|H\left(z=e^{j\omega}\right)\right| = \frac{1}{\|\vec{z}-\vec{p}\|} = \frac{1}{\|\overrightarrow{pz}\|}$$





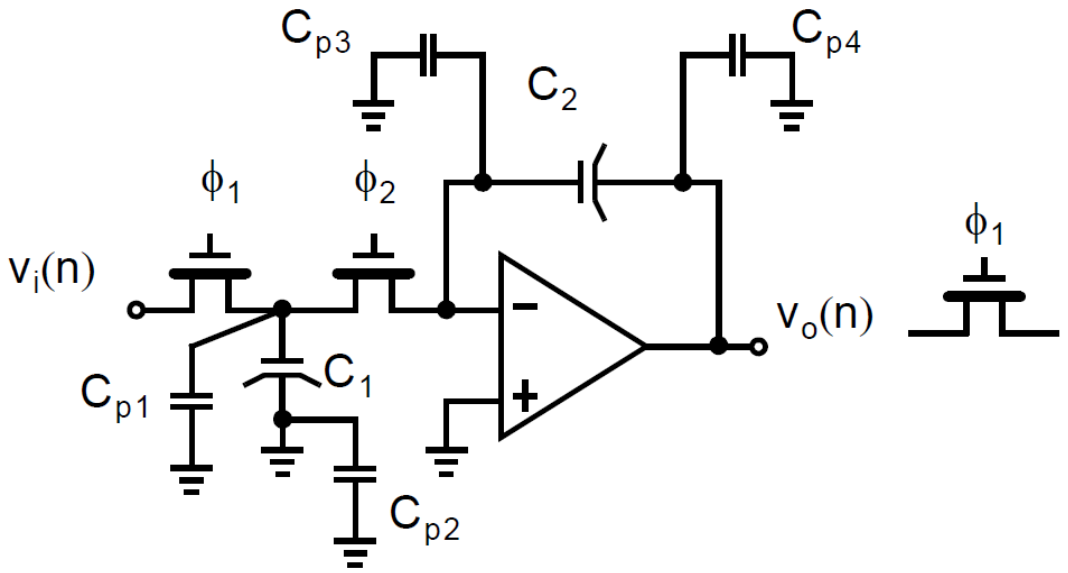
MATLAB Code

```
%% Compare CT and DT integrators
close all; clear all;
% tau = R*C2 = C2/(FS*C1)
tau = 1;
TS = 1; FS = 1/TS;
s = tf('s');
z = tf('z',TS);
cti = -1/(s*tau);
dti = -tau/FS*1/(z-1);
figure;
bode(cti,dti);
legend('CT','DT')
figure;
step(cti,dti,0:10);
legend('CT','DT')
figure;
pzmap(cti,dti);
legend('CT','DT');
```

Parasitic (Stray) Sensitivity

- The parasitic (stray) caps can be problematic if they contribute to charge sharing
  - Not well controlled (top plate and wiring parasitics)
  - Partially nonlinear due to the D/S junction capacitances of the switches

$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1}$$

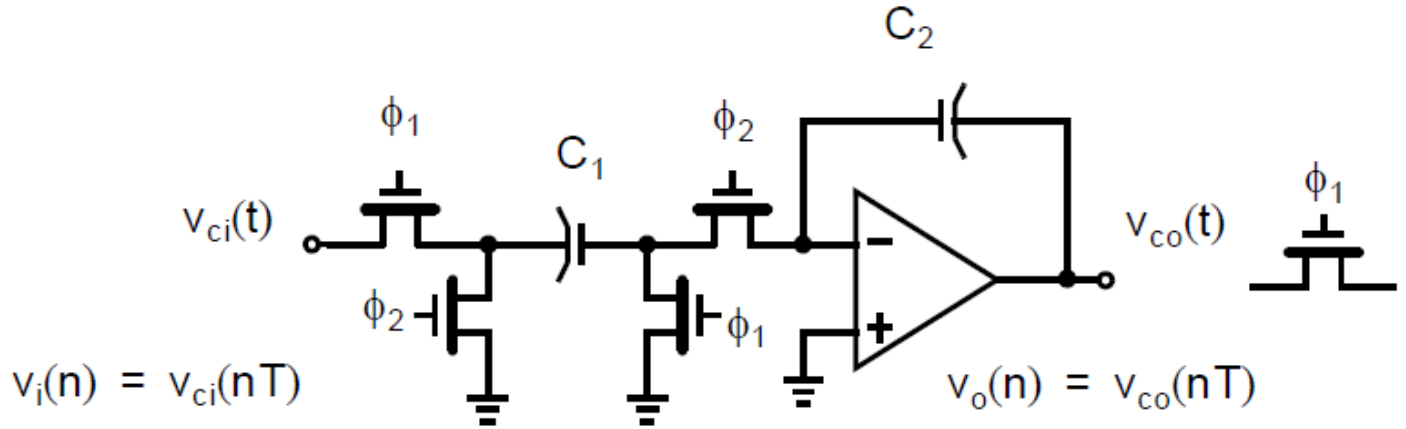


[Johns & Martin, 2012]

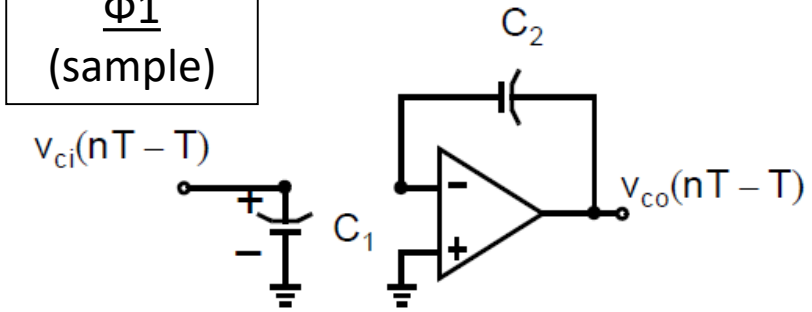
Non-Inverting Parasitic-Insensitive

- Parasitic caps dump their charge to ground or do not charge at all

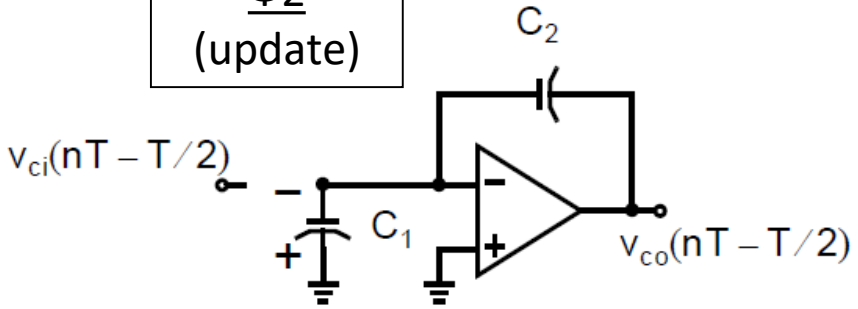
$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1-z^{-1}} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$



Φ1 (sample)

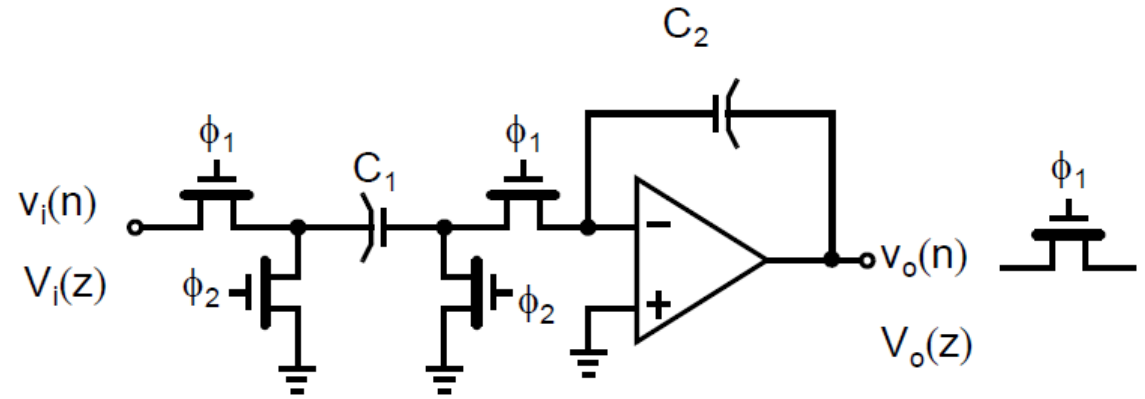


Φ2 (update)

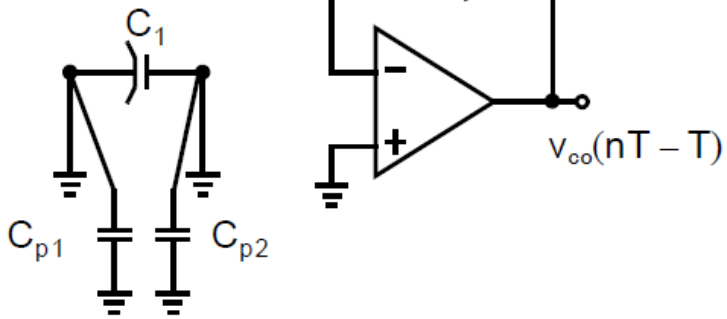


Delay-Free Inverting Parasitic-Insensitive

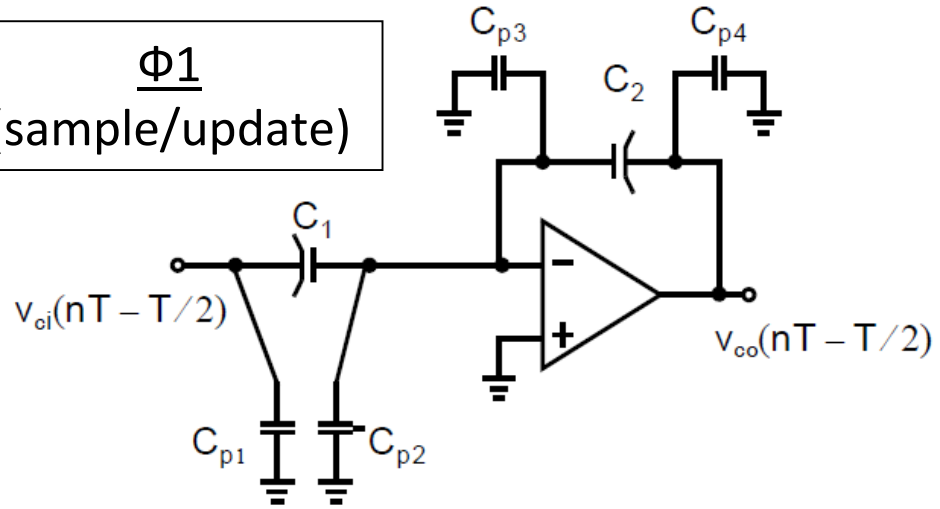
$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n) \qquad H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right) \frac{1}{1 - z^{-1}}$$



Φ2
(reset)



Φ1
(sample/update)

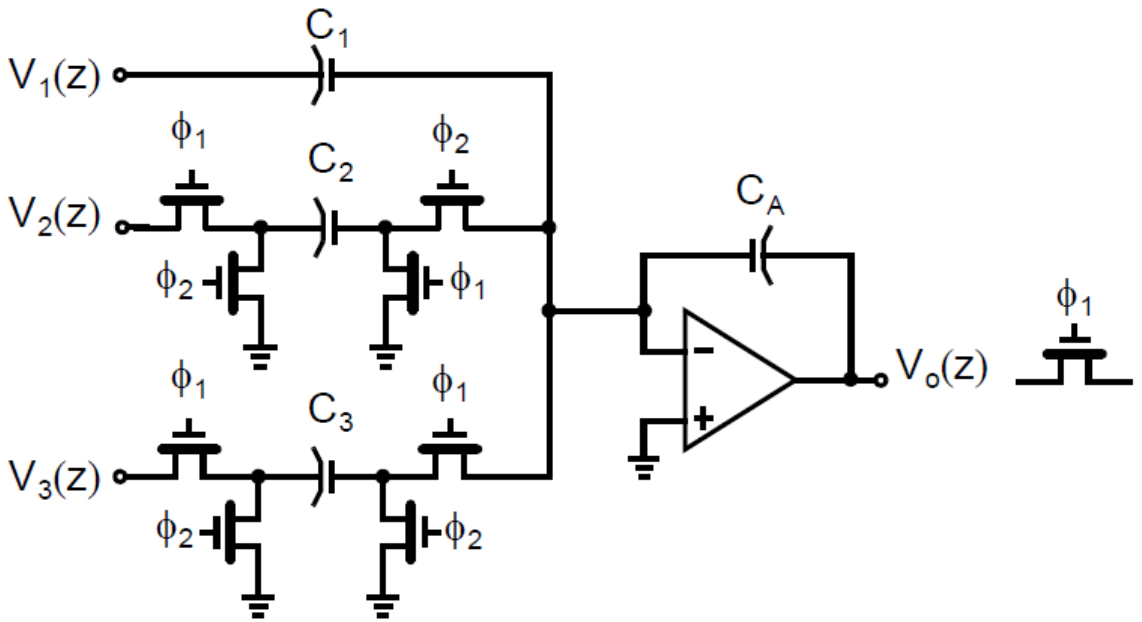


[Johns & Martin, 2012]

Summing Integrator

- V_1: CT amplification
- V_2: DT non-inverting integrator
- V_3: DT delay-free inverting integrator

$$V_o(z) = -\left(\frac{C_1}{C_A}\right) V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right) V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{1}{1-z^{-1}}\right) V_3(z)$$

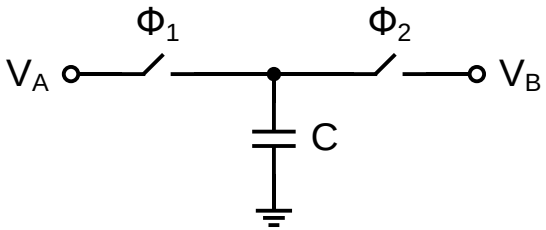


[Johns & Martin, 2012]

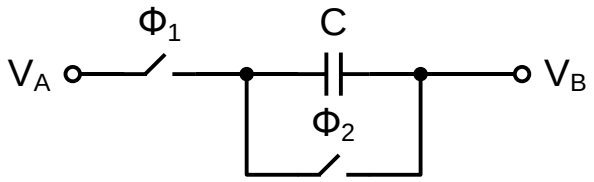
Types of Switched Capacitors

- Shunt- and series-type SCs are simple and cheap to implement
- Stray-insensitive SC requires 2 more switches

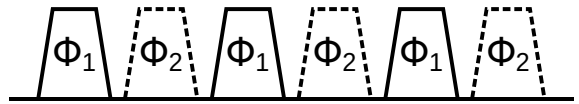
Shunt-type



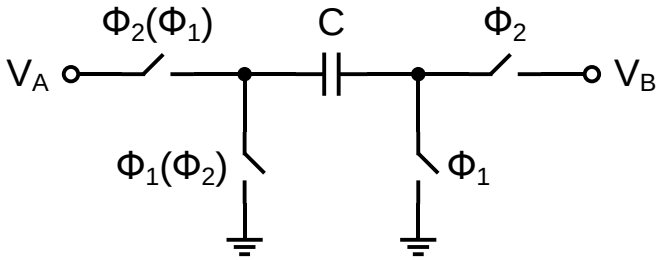
Series-type



2-phase clock



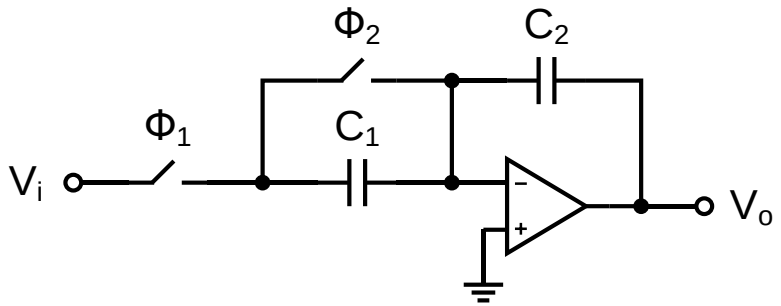
Stray-insensitive



Series Type DT Integrator

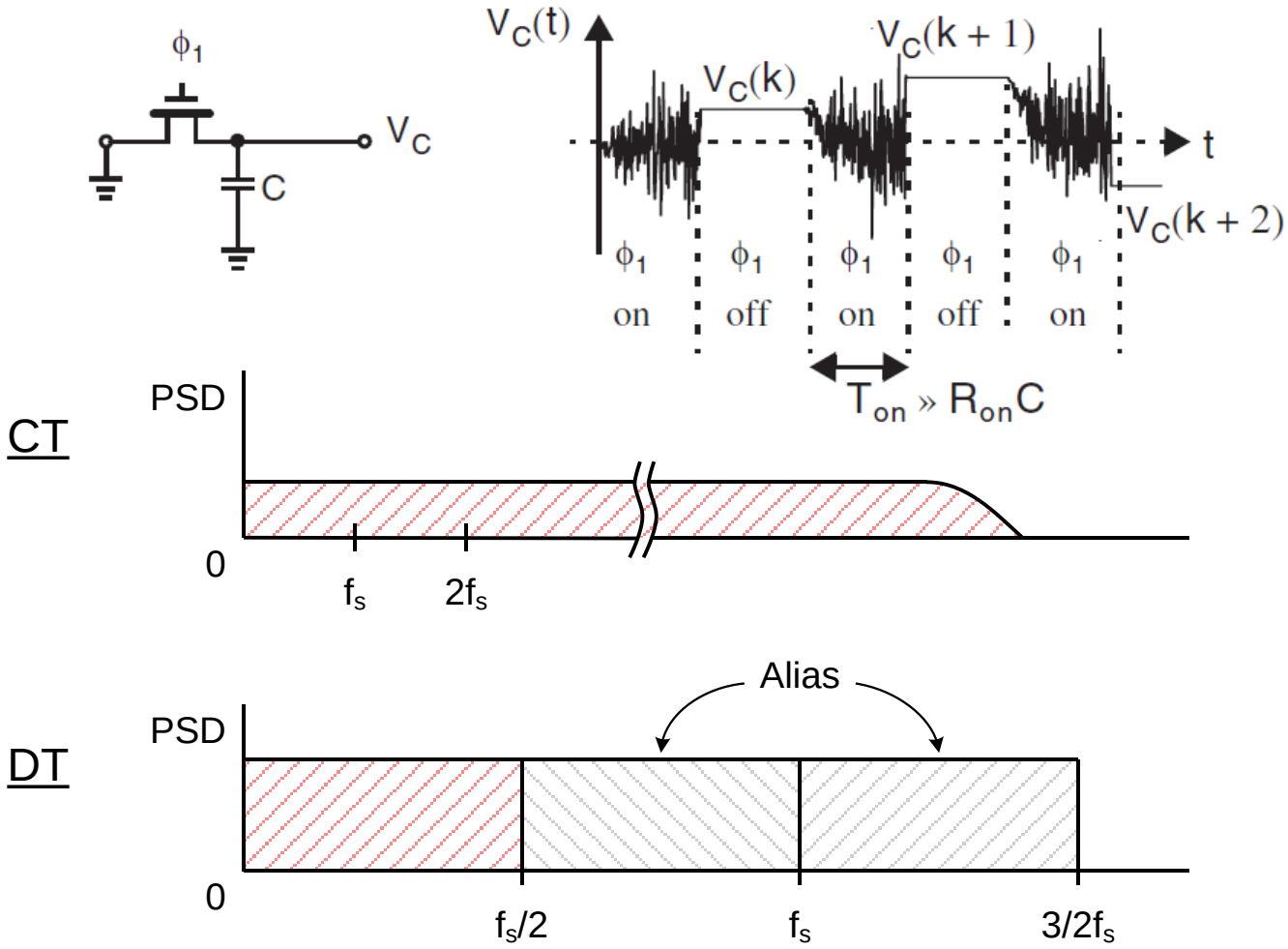
$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2}\frac{1}{1 - z^{-1}}$$

Φ1 (sample/update)	⇨	Φ2 (reset C_1)



Sampled Noise

- Noise density increases (noise folding)
  - But total integrated noise power remains constant

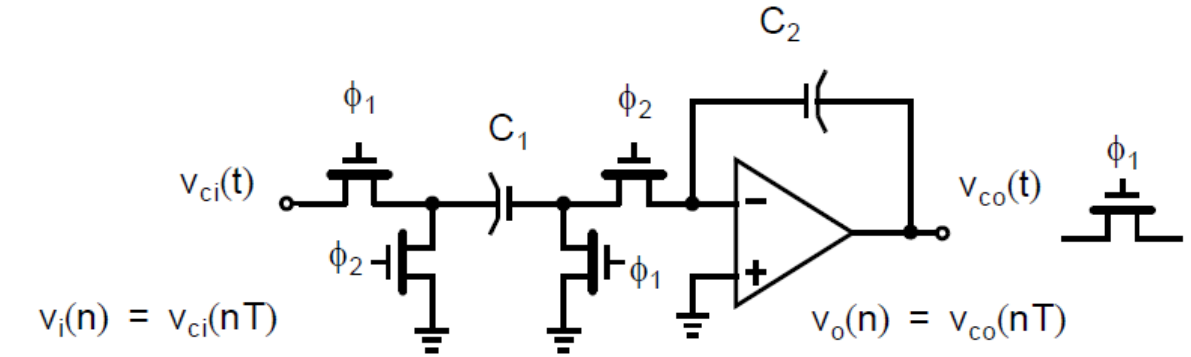


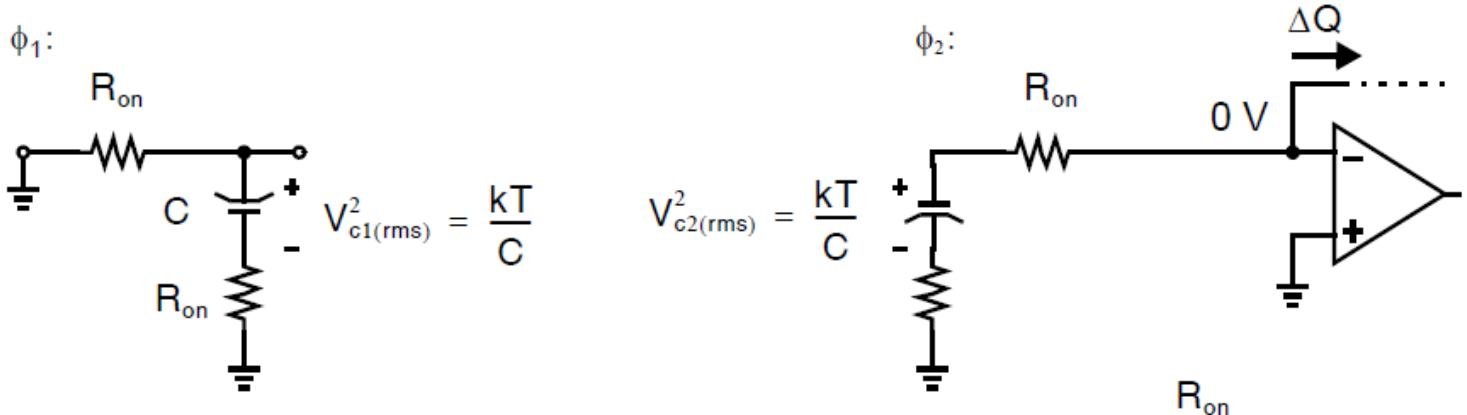
Noise in SC Circuits

- Two noise components (sampled in Φ_1 and CT in Φ_2)
- SC noise cannot be simulated using AC noise simulation
  - Use transient noise or pnoise analysis

$$\Delta Q_{(rms)}^2 = \Delta Q_{1(rms)}^2 + \Delta Q_{2(rms)}^2 = 2kTC$$

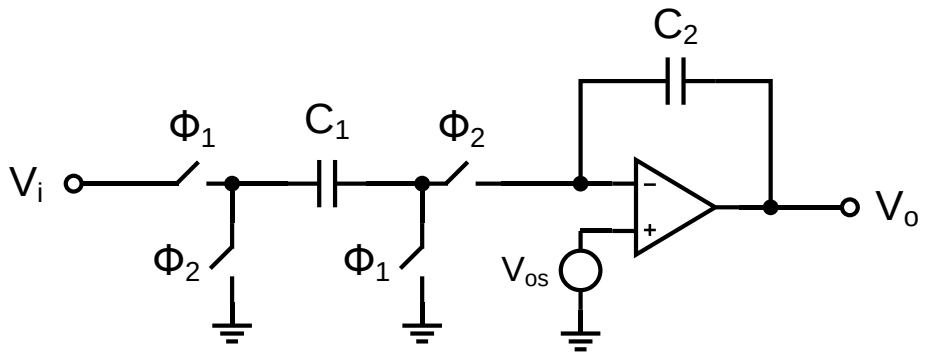
$$V_{in(rms)} = \sqrt{\frac{2kT}{C}}$$

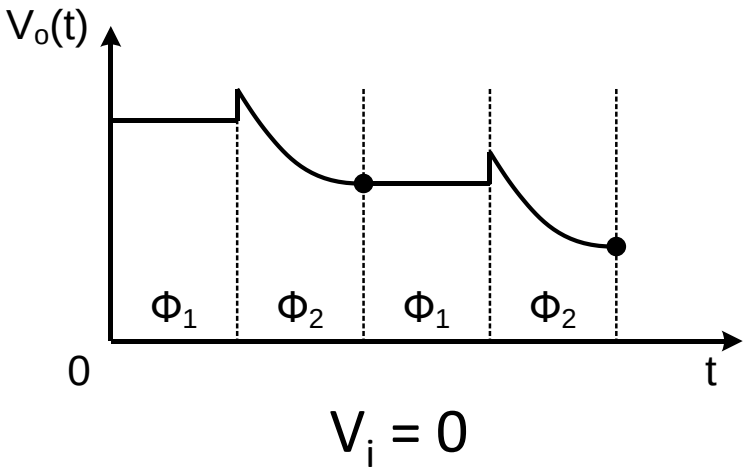




[Johns & Martin, 2012]

OTA Offset Voltage





$V_i = 0$

$$\sum Q(\varphi_1) = V_i(n)C_1 + [V_o(n) - V_{os}]C_2$$

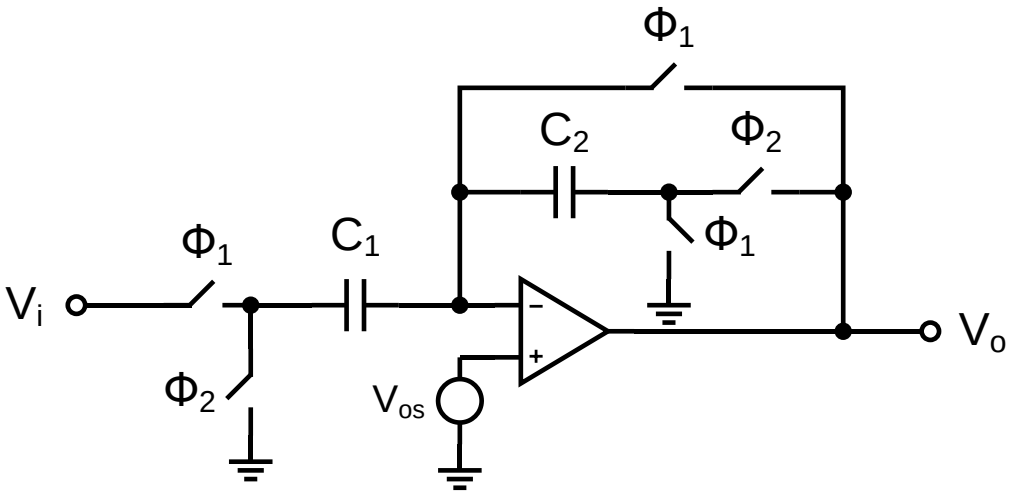
$$\sum Q(\varphi_2) = -V_{os}C_1 + [V_o(n+1) - V_{os}]C_2$$

$$V_i = 0 \quad \Rightarrow \quad V_o(n+1) - V_o(n) = \left(\frac{C_1}{C_2}\right)V_{os}$$

$$V_o(z) = \frac{C_1}{C_2}\frac{1}{z-1}V_{os}$$

Autozeroing

- Auto-zeroing (AZ) eliminates offset voltage and reduces 1/f noise
  - A.k.a. correlated double sampling (CDS)



$$\sum Q(\varphi_1) = [V_i(n) - V_{os}]C_1 - V_{os}C_2$$

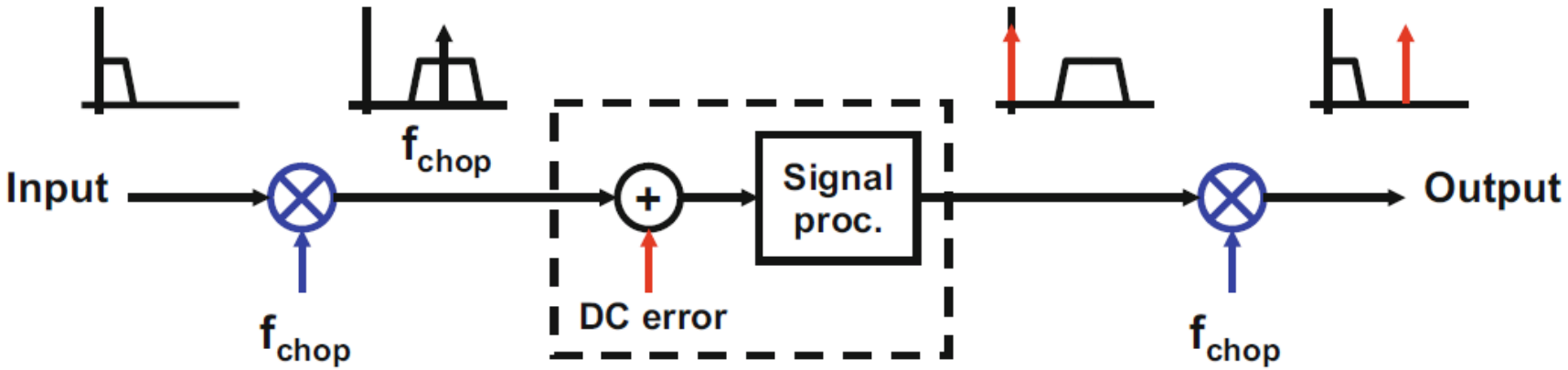
$$\sum Q(\varphi_2) = -V_{os}C_1 + [V_o(n) - V_{os}]C_2$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}$$

Find the mistake!

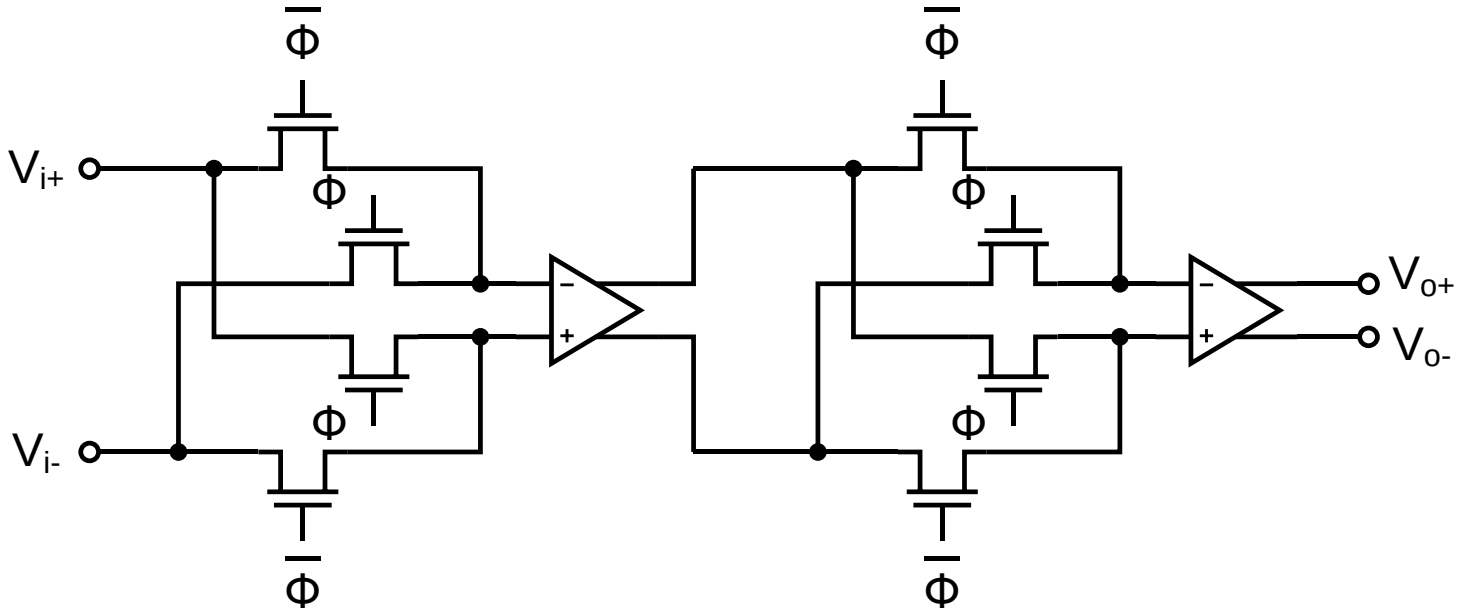
Chopping

- Chopping is a technique used for improving accuracy.
  - Sensitive signals are modulated to frequency bands where the signal processing is free of errors.
  - Mitigates the effect of DC offsets, flicker noise, etc.



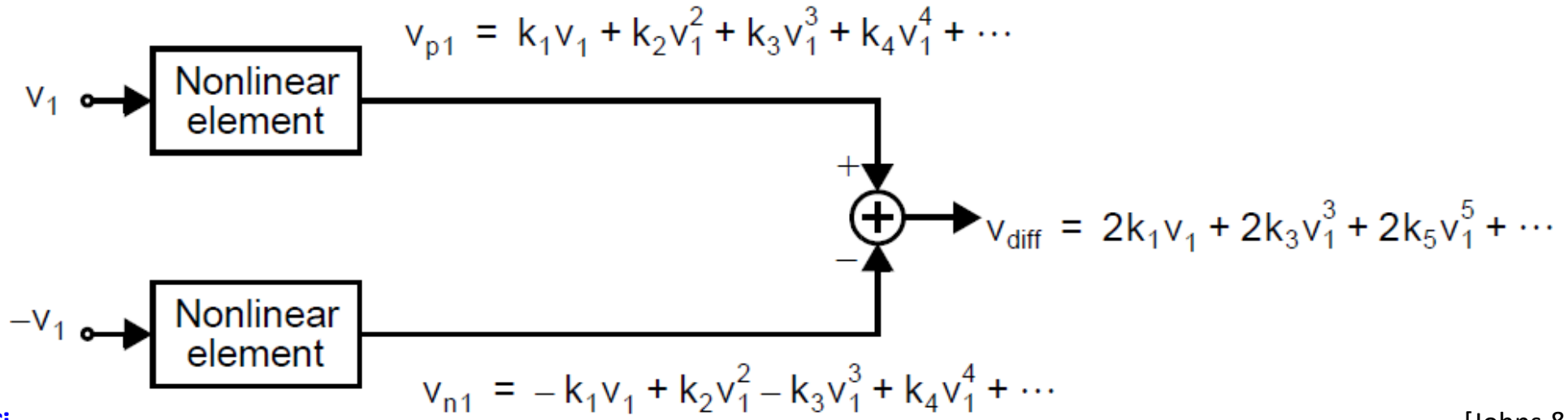
Chopper-Stabilized Fully Diff OTA

- In differential circuits, chopping is implemented easily by alternating between the differential branches.



Fully Differential Operation

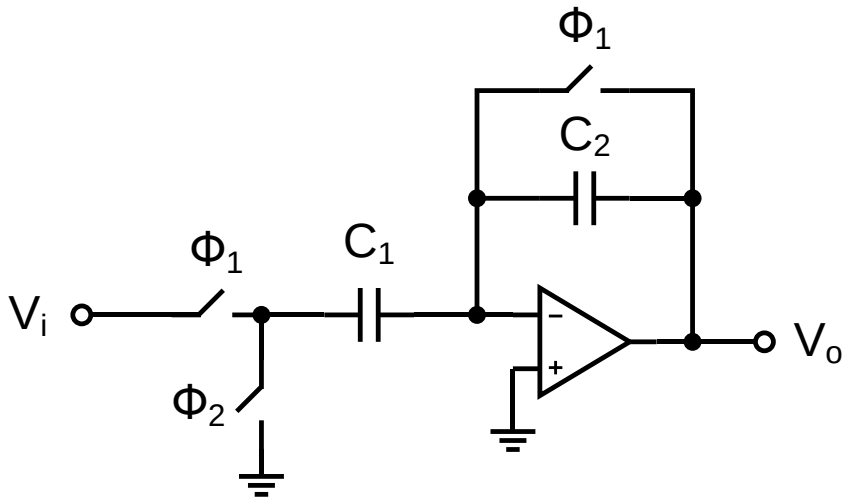
- Pros
  - CM errors rejection
  - Even-order distortion rejection
  - Double signal swing
  - Simple sign inversion (useful in chopping)
- Cons
  - More power, more area, and CMFB circuit required



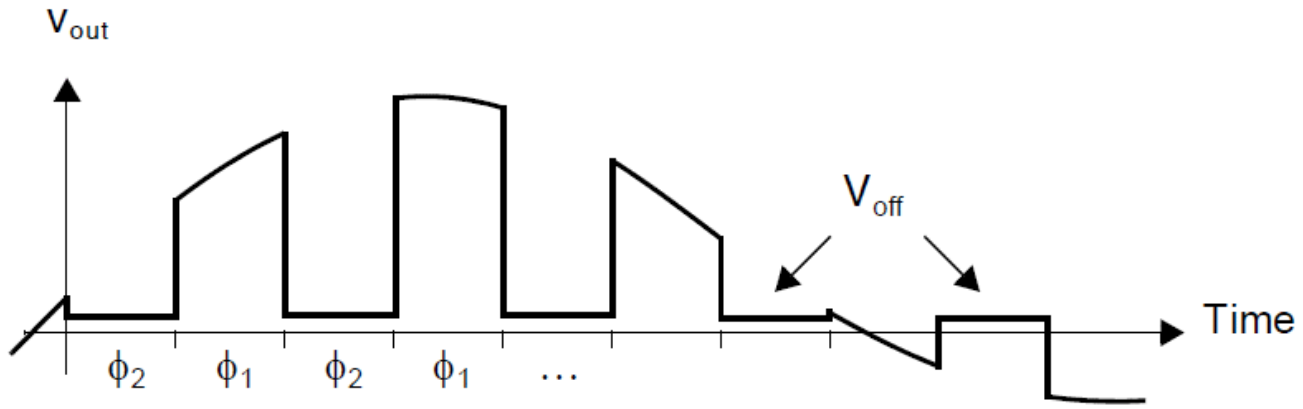
[Johns & Martin, 2012]

Resettable SC Amplifier

- The output is reset every cycle (resettable gain stage)
  - The OTA must have high slew rate



$$H(z) = +\frac{C_1}{C_2} \cdot z^{-1}$$

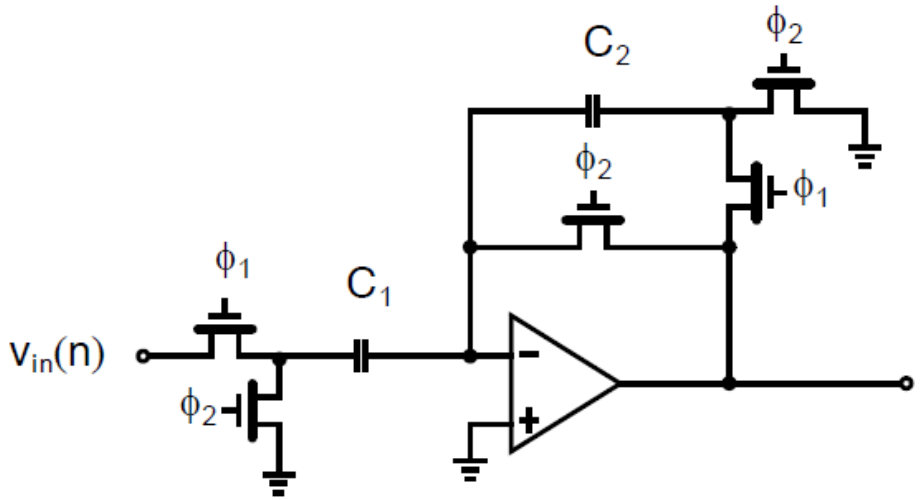


Find the mistake!

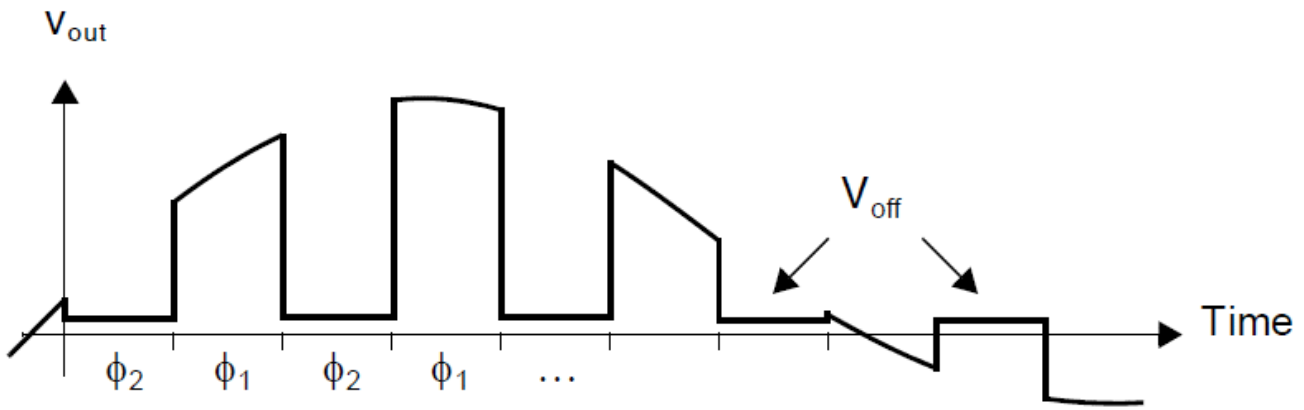
[Y. Chiu, EECT 7327, UTD] [Johns & Martin, 2012]

SC Amplifier with Offset Cancellation

- Auto-zeroing (AZ) eliminates offset voltage and reduces 1/f noise
  - A.k.a. correlated double sampling (CDS)



$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$



[Johns & Martin, 2012]

SC Amplifier with Offset Cancellation

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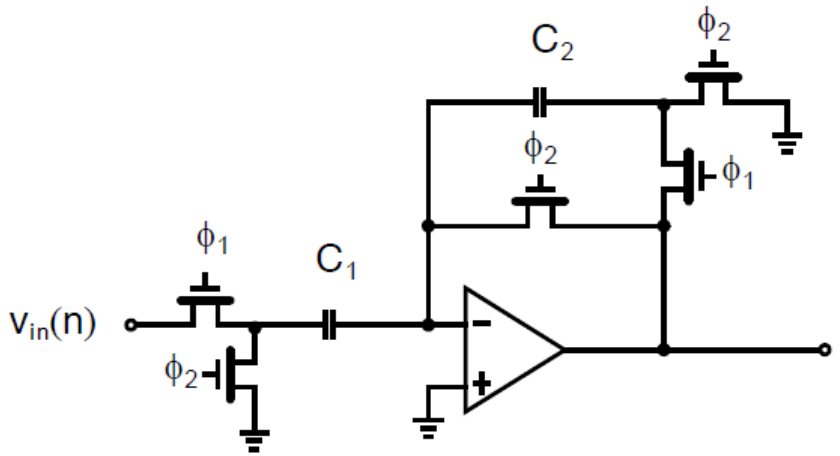
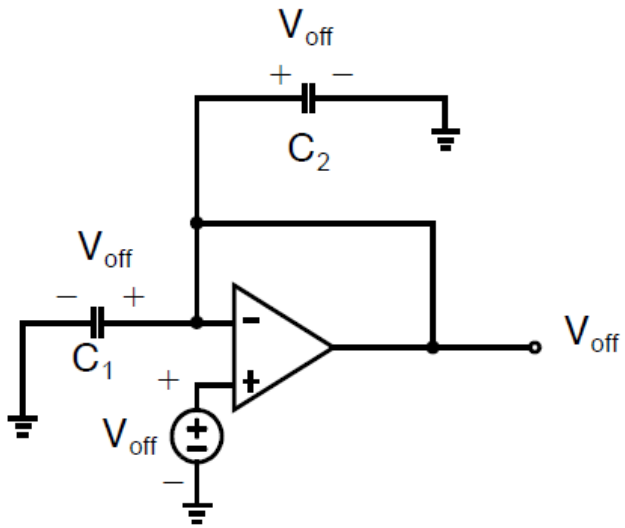
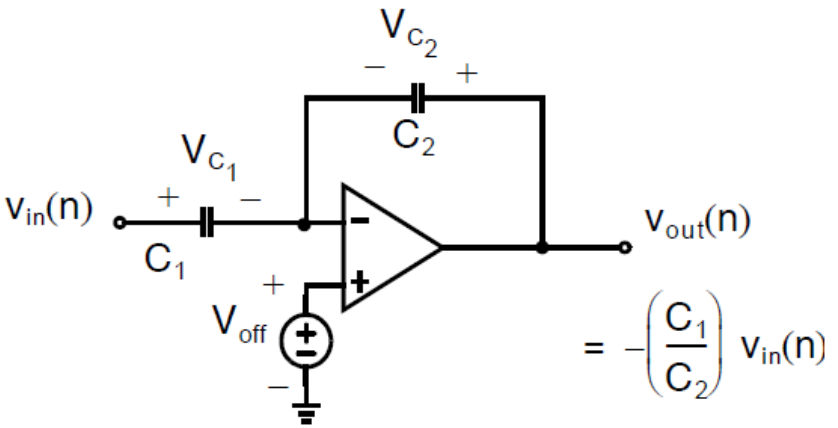


$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$



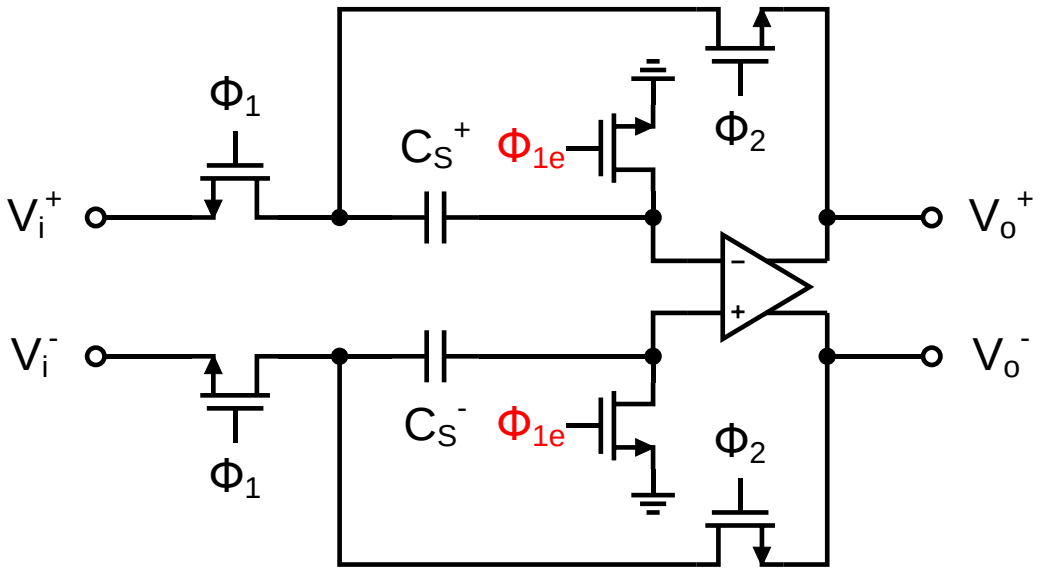


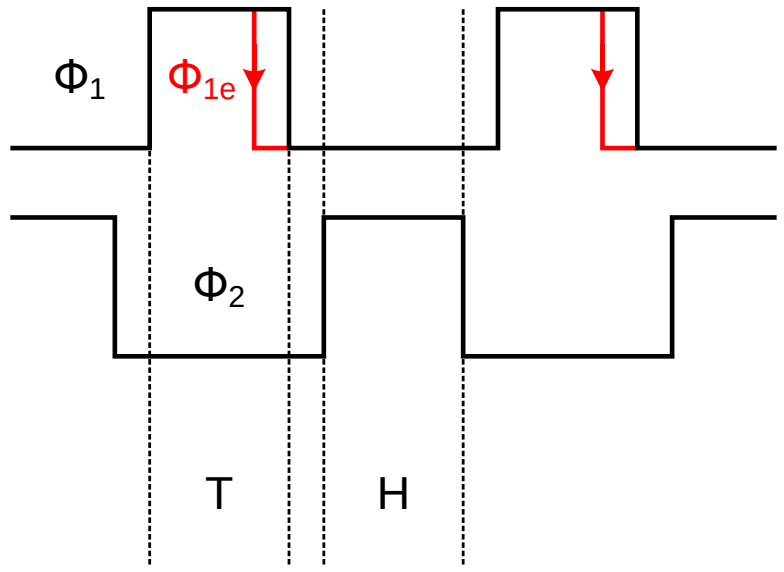
$$= -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$

[Johns & Martin, 2012]

Flip-Around S/H Amplifier (SHA)

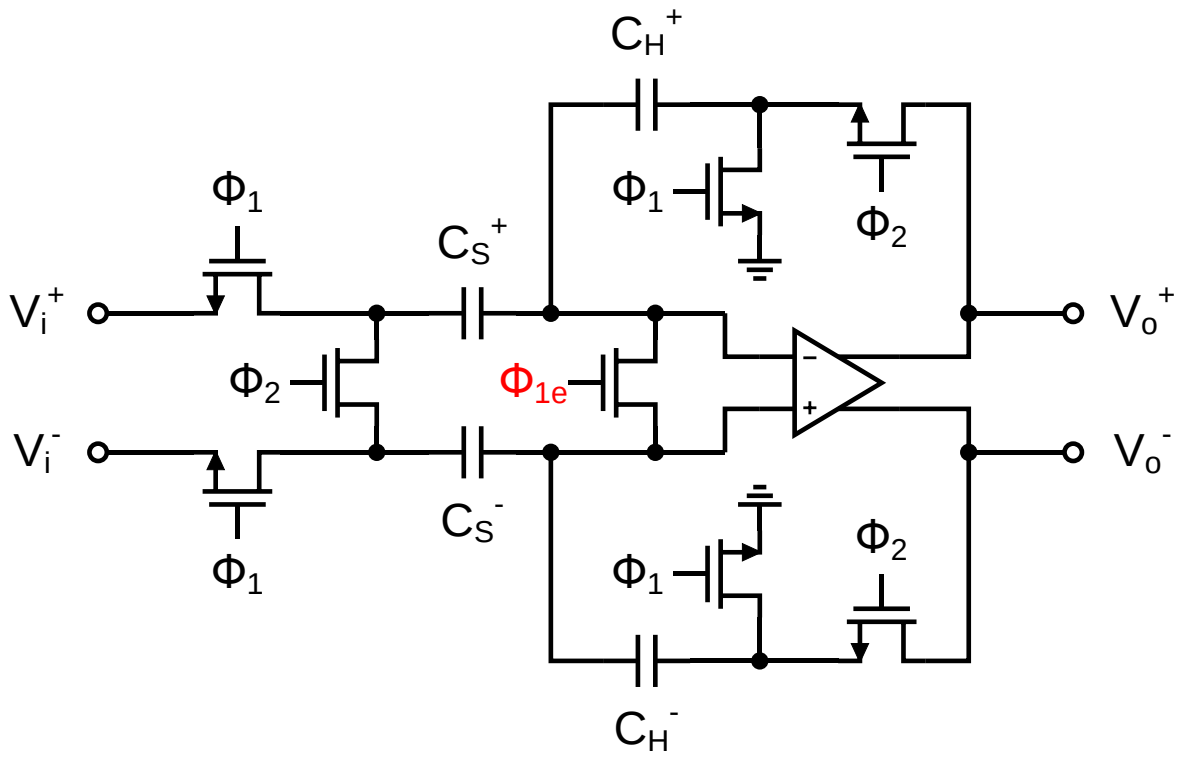
- Non-inverting, 1X closed-loop gain
- Close-to-unity feedback factor in hold mode
- CF/CI independent of Vin and cancelled differentially





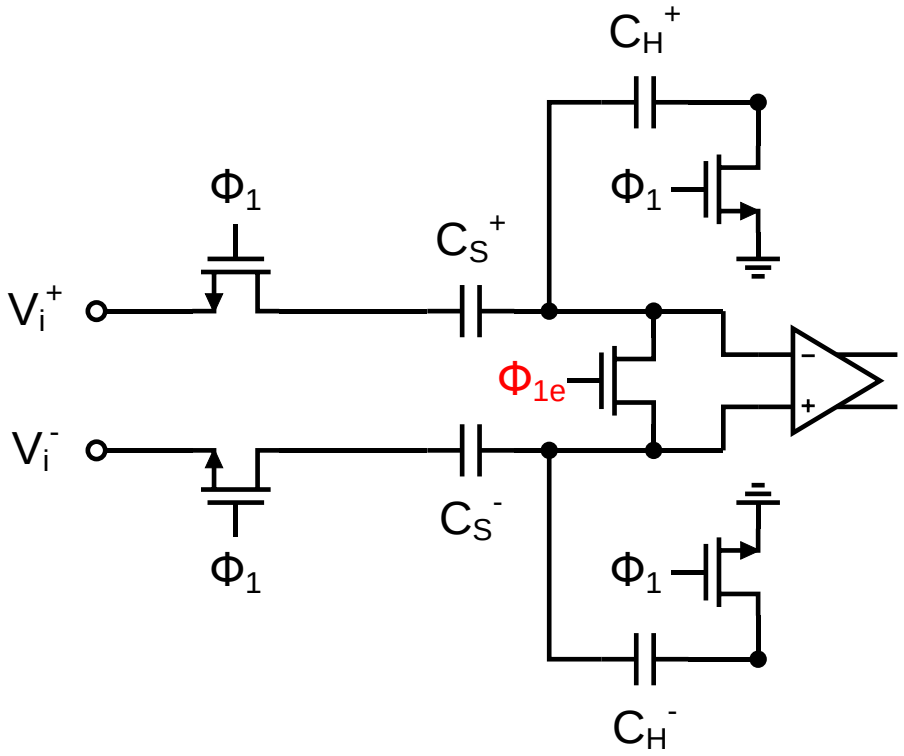
Inverting S/H Amplifier (SHA)

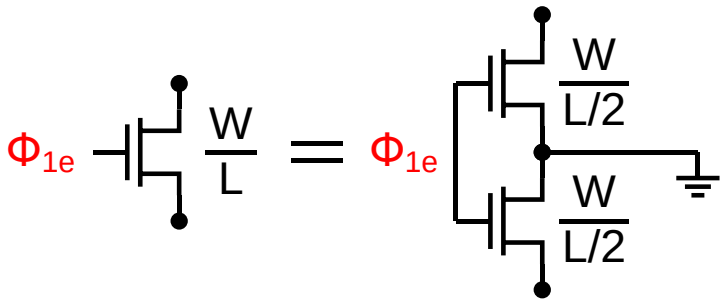
- Inverting amplifier
- Closed-loop gain determined by the ratio CS/CH
- CMOS (TG) or bootstrapped switches are required when passing signals with large swing

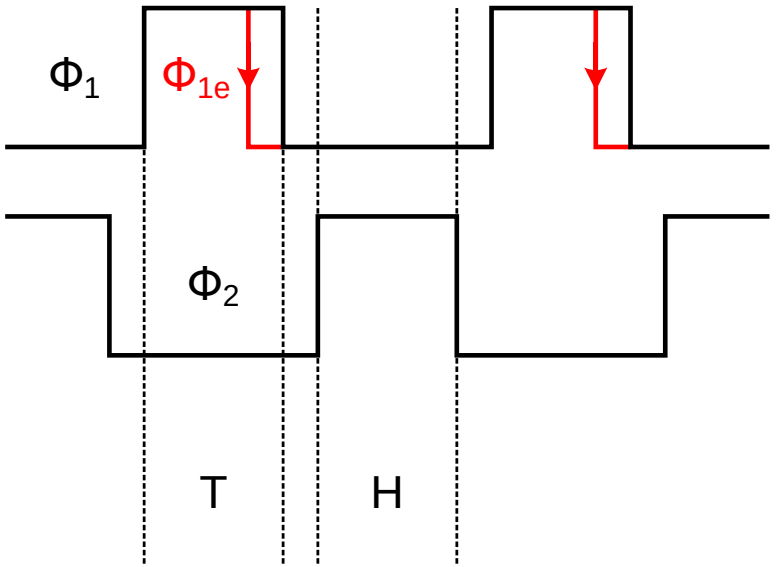


Inverting SHA (Track Mode)

- CF and CI are independent of Vin and cancelled differentially

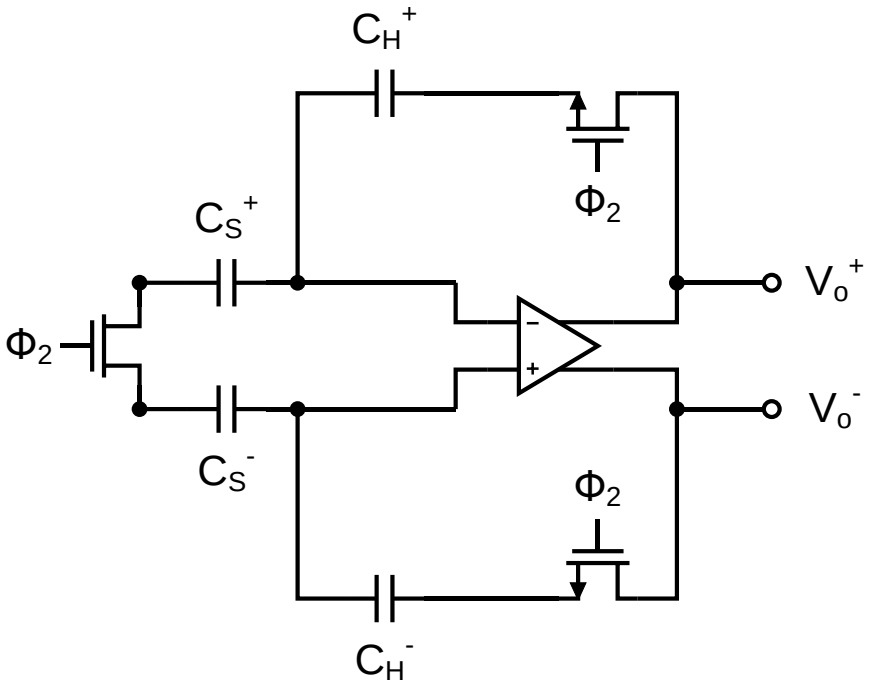




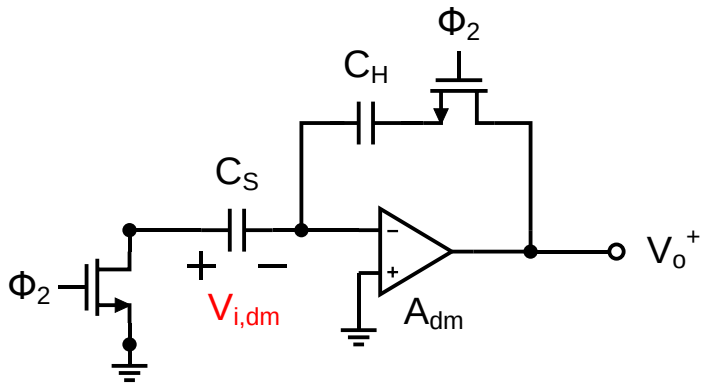


Inverting SHA (Hold Mode)

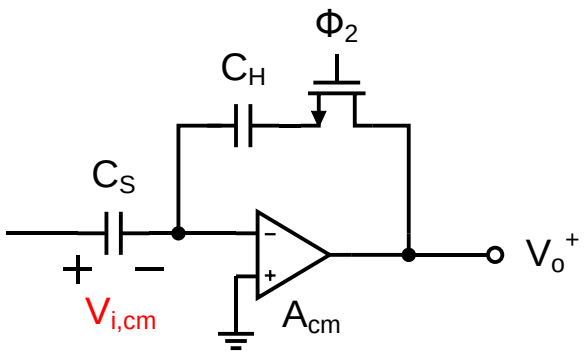
- For 1X gain: $C_S = C_H$
- DM charge is transferred but CM charge is not transferred!

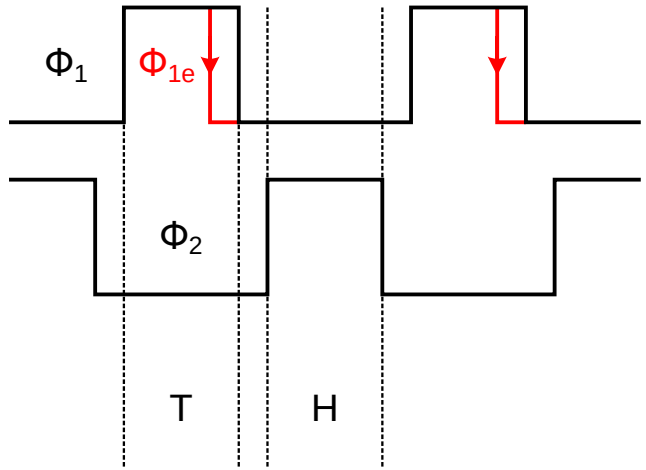


DM half circuit



CM half circuit





Switch Sizing

- To minimize switch-induced error voltages, small transistor size, slow turn-off, low source impedance should be used.
  - Always use minimum channel length for switches as long as leakage allows.
  - Caution: slow turn-off is more sensitive to jitter
- For fast settling (high-speed design), large W/L should be used, and errors will be inevitably large as well.
  - Usually $(R_{on}C_S)^{-1} \geq (3\text{-}5)\cdot\omega_{-3dB}$ of closed-loop op-amp for settling purpose
- For a given speed, switch sizes can be optimized w/ simulation.
- Be aware of the limitations of simulators (SPICE etc.) using lumped device models.

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- W. Kester, The Data Conversion Handbook, ADI, Newnes, 2005.
- B. Boser and H. Khorramabadi, EECS 247 (previously EECS 240), Berkeley.
- B. Murmann, EE 315, Stanford.
- Y. Chiu, EECT 7327, UTD.

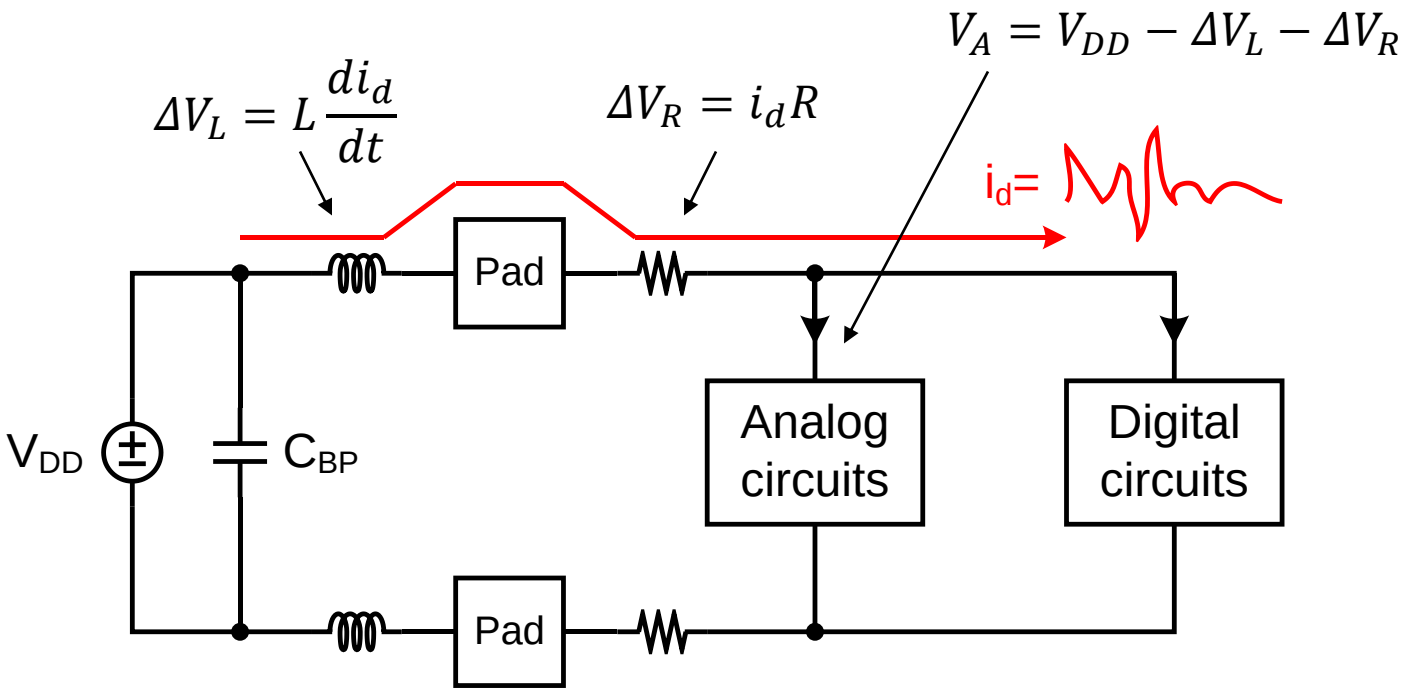
Course Resources

Lectures	Labs	YouTube Channel

Thank you!

Analog vs Digital Supply Lines (1)

- Sharing sensitive analog supplies with digital ones is a very bad idea.



Analog vs Digital Supply Lines (2)

- Dedicated pads for analog and digital supplies
- On-chip bypass capacitors help (watch ringing)
- Off-chip chokes (large inductors) can stop noise propagation at board level