AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Department of Electronics and Communications Engineering
Credit Hours Engineering Program (CHEP)

1st Semester, 2020/2021	**Course Code: *ECE486***	***Time allowed: 2 Hrs.***

Analog Integrated Systems Design

The Exam Consists of **Four** Questions in **Three** Pages. ***Maximum Marks: 40 Marks*** **1 / 3**

تعليمات هامة

- حيازة التيلفون المحمول داخل لجنة الامتحان تعتبر حالة غش تستوجب العقاب، وإذا كان الدخول بالمحمول ضروريا فيلزم وضعه مغلقا فى الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- **يسمح لكل طالب باصطحاب ورقة واحدة فقط A4 يدون عليها الطالب ما يشاء (على الوجهين)، ويكتب عليها اسمه بالقلم الجاف.**
- لايسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة **زيادة على ما ذكر** والمخالفة تعتبر حالة غش.

Question (1): [15 marks]

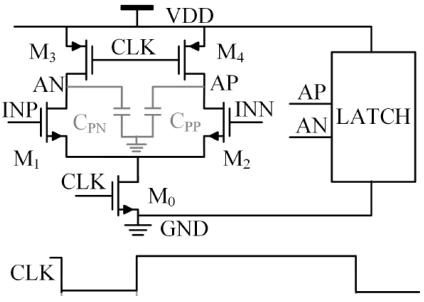
Choose the best answer and complete the missing dots:

a) For a SAR ADC, the digital logic power consumption is **(linear, quadratic, exponential)** with the number of bits, while the capacitive DAC power consumption is **(linear, quadratic, exponential)** with the number of bits if the unit element is kept unchanged.
b) For a SAR ADC, the area is usually limited by the **(digital logic, capacitive DAC, comparator)**, and the linearity is usually dominated by the **(digital logic, capacitive DAC, comparator)**.
c) In order to increase the speed of a S/H circuit, you may **(increase, decrease)** W/L and use **(bottom plate sampling, bootstrapping)**.
d) In order to improve the linearity of a S/H circuit, you may **(increase, decrease)** W/L and use **(bottom plate sampling, bootstrapping)**.
e) Complete with "True" or "False":
   For a SAR ADC, if we design the capacitive DAC to achieve matching requirements:
   - The thermal noise will be dominant. (…..)
   - The capacitive DAC power and area will be very large. (…..)
f) For medium resolution and speed, the best ADC architecture is …..
g) For high resolution, the best ADC architecture is …..
h) For high speed applications, the best ADC architectures are ….. and …..
i) Each stage of a pipelined ADC contains a low-resolution ADC and DAC. Digital error correction can be used to correct **(ADC errors, DAC errors, both ADC and DAC errors)**.
j) Clock-feed through errors in mixed-signal circuits can be reduced by using …..
k) The offset errors in analog circuits can be fixed using ….., ….. and …..
l) The metastability problem of a comparator can be mitigated by ….. and …..
m) For under-sampling, the antialiasing filter is a …..-pass filter.
n) It is more difficult to get a low Walden FoM at ….. sampling frequency.
o) Increasing the resolution by one bit means that the power of the quantization error is reduced by a factor of **(2, 4, 6, 8)**.
p) If a high resolution DAC is required, it is necessary to use special techniques to overcome mismatch limits, such as ….., ….., and …..
q) The rms noise in a S/H with 1pF capacitance is around …..
r) [1 mark] For VFS = 1V, the thermal noise in a S/H with 1pF capacitance will become dominant (higher than the quantization noise) if the number of ADC bits is higher than ….. bit.

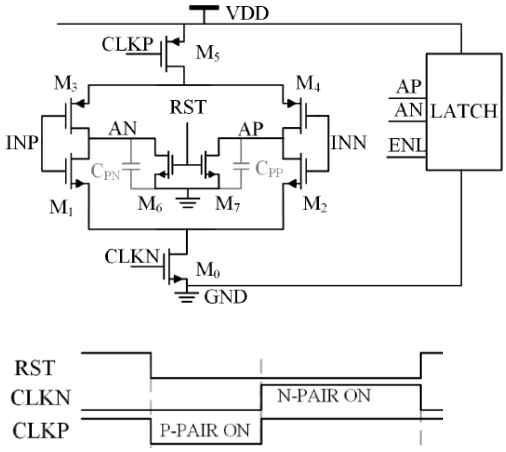
Question (2): [7 marks]

The figure below shows two comparator implementations (A) and (B).

(A)



(B)



a) [4 marks] For each comparator, copy the given timing diagram and add to each diagram the waveforms at nodes AN and AP. Assume INP is slightly higher than INN.
b) [1 mark] Which of the two comparators (A) and (B) will be more energy efficient? Why?
Hint: Think about the energy consumed in charging the capacitance CPN and CPP.
c) [2 marks] Draw the schematic of a latch that can be used with the comparator in (A). Add the waveforms at the output of the latch to the timing diagram.

Comparator schematics used in this problem are from 10.1109/JSSC.2016.2587688.

Question (3): [10 marks]

It is required to design a 3-bit pipelined ADC with 1.5-bit/stage. Assume the full-scale reference levels are $V_{RFFP} = 1V$ and $V_{REFN} = -1V$, and assume the comparator thresholds are at $V_{REFP}/4$ and $V_{REFN}/4$.

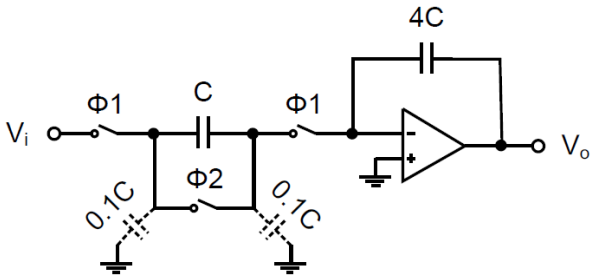
a) [4 marks] Draw the complete schematic of the ADC.
b) [6 marks] Assume an input voltage $V_{in} = 0.22V$. Copy the following table to your answer sheet and fill all missing items.

Stage input voltage	MDAC operation	Stage decision (0 or 1 or P)	B2	B1	B0
Final ADC output					

Question (4): [8 marks]

The diagram below shows a switched-capacitor (SC) circuit using a standard non-overlapping two-phase clock. Two stray capacitors of value 0.1C are also shown in the diagram. Assume an ideal op-amp and that Vi and Vo update when $\phi 1 = 1$.

a) [1 mark] Is this circuit an amplifier or an integrator?
b) [4 marks] Derive the z-domain voltage transfer function Vo(z)/Vi(z) when all stray capacitors are ignored.
c) [3 marks] Re-derive the transfer function with stray capacitors taken into account.



This question is courtesy of Prof. Yun Chiu, UTD.

End of Exam

دعواتي لكم بالتوفيق

Dr. Hesham Omran ***Exam Date: 23-Feb-2021***