Analog Integrated Systems Design

Lecture 12
Nyquist ADCs (1)

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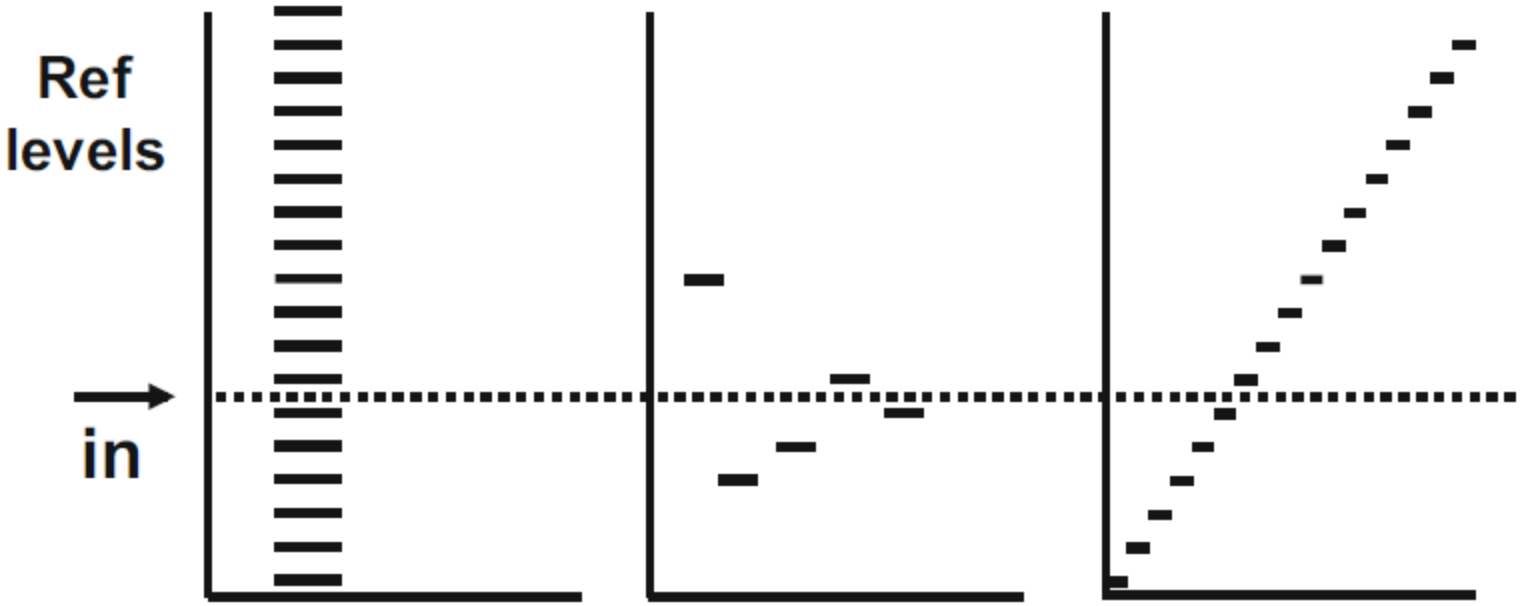
ADCs Classification

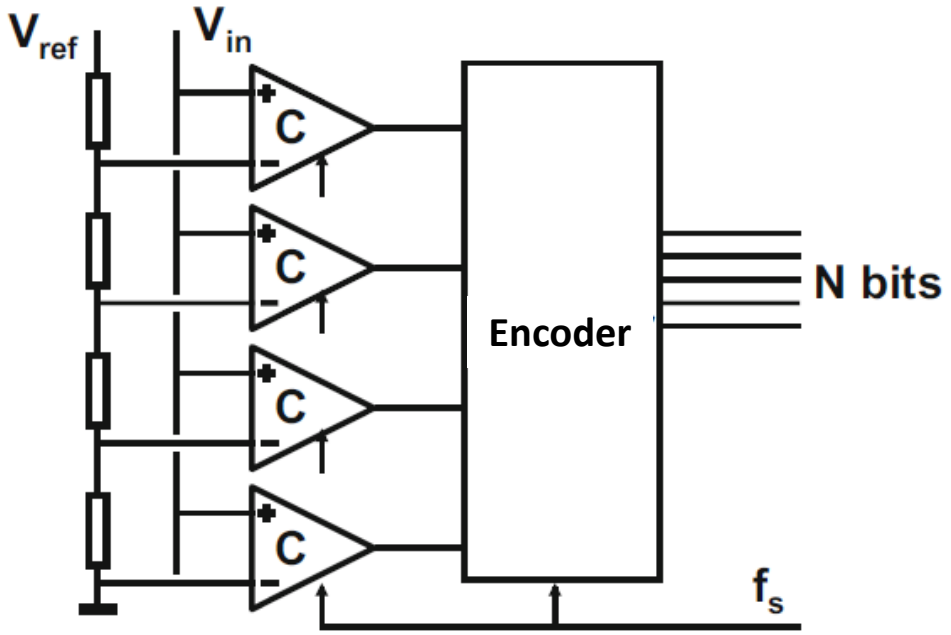
- Nyquist ADCs: signal BW close to Nyquist limit ($f_s/2$)
  1. Parallel search (e.g., flash ADC): $T_{conv} \sim T_{clk}$
  2. Sequential search (e.g., SAR ADC): $T_{conv} \sim N \times T_{clk}$
  3. Linear search (e.g., dual-slope ADC): $T_{conv} \sim 2^N \times T_{clk}$



[M. Pelgrom, 2017]

Flash ADC

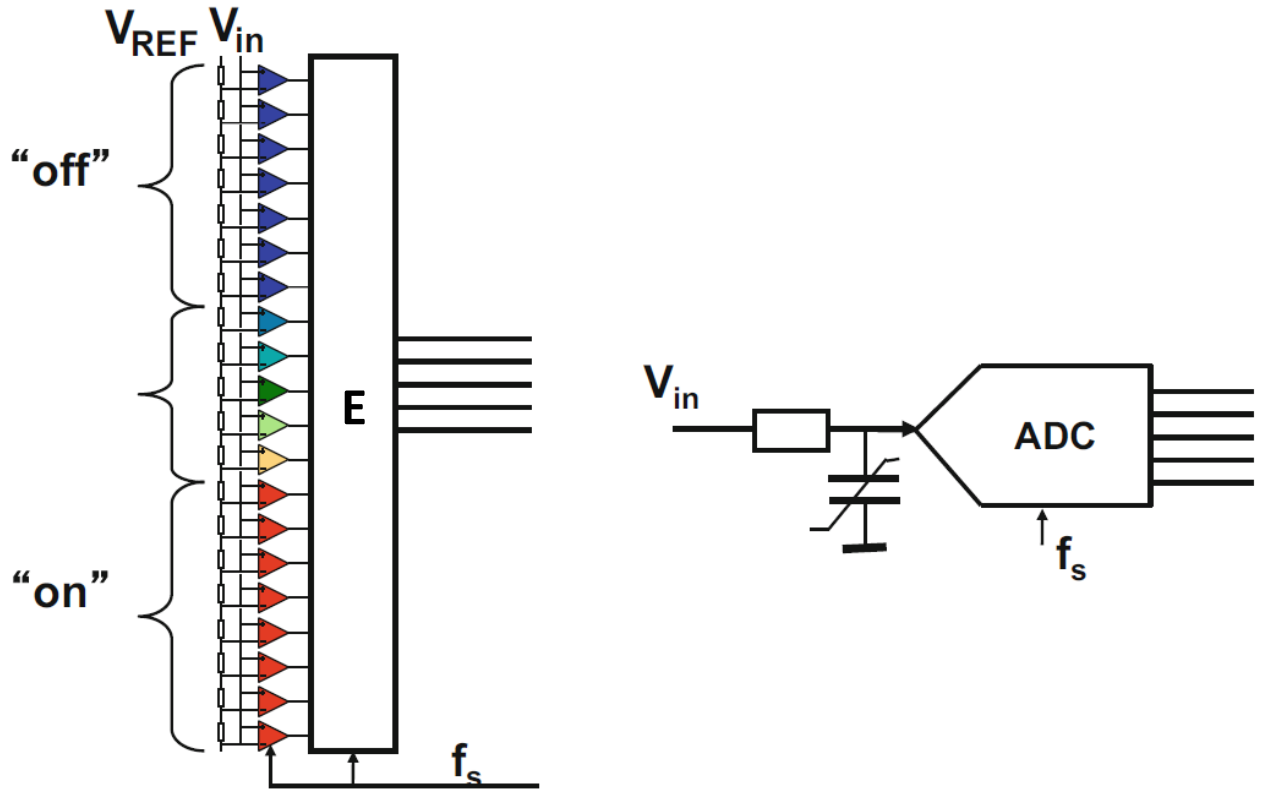
- Resistor ladder DAC
- $(2^N - 1)$ comparators ➔ complexity, power, area, and input capacitance grow exponentially with no. of bits
- Parallel search ➔ very fast
  - Encoder converts thermometer code to straight binary code
- S/H inherent in the digital latches of the comparators



[M. Pelgrom, 2017]

Nonlinear Input Impedance

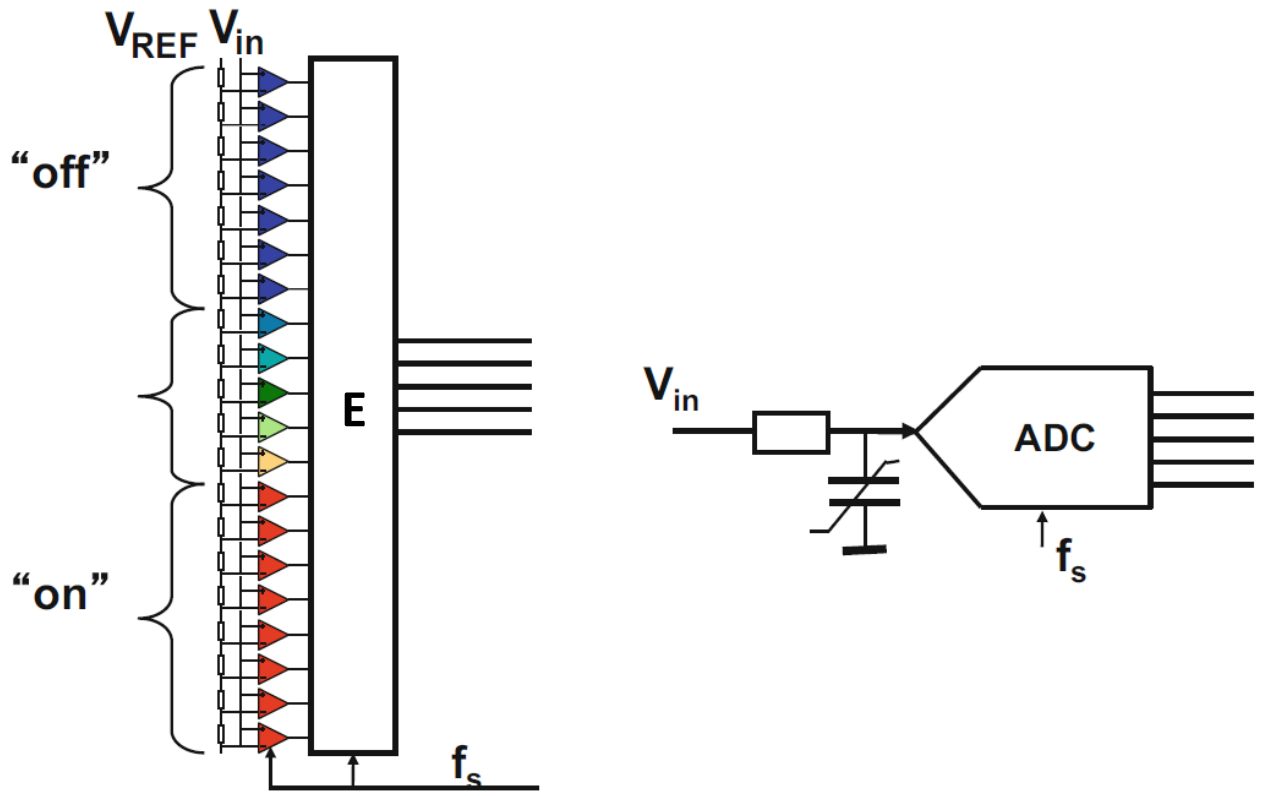
- Input cap of comparator is the input cap of a diff pair
- Comparators below the decision level create a high capacitance
- Comparators above the decision level will show a low capacitance
- Non-linear input capacitance creates distortion



[M. Pelgrom, 2017]

Nonlinear Input Impedance

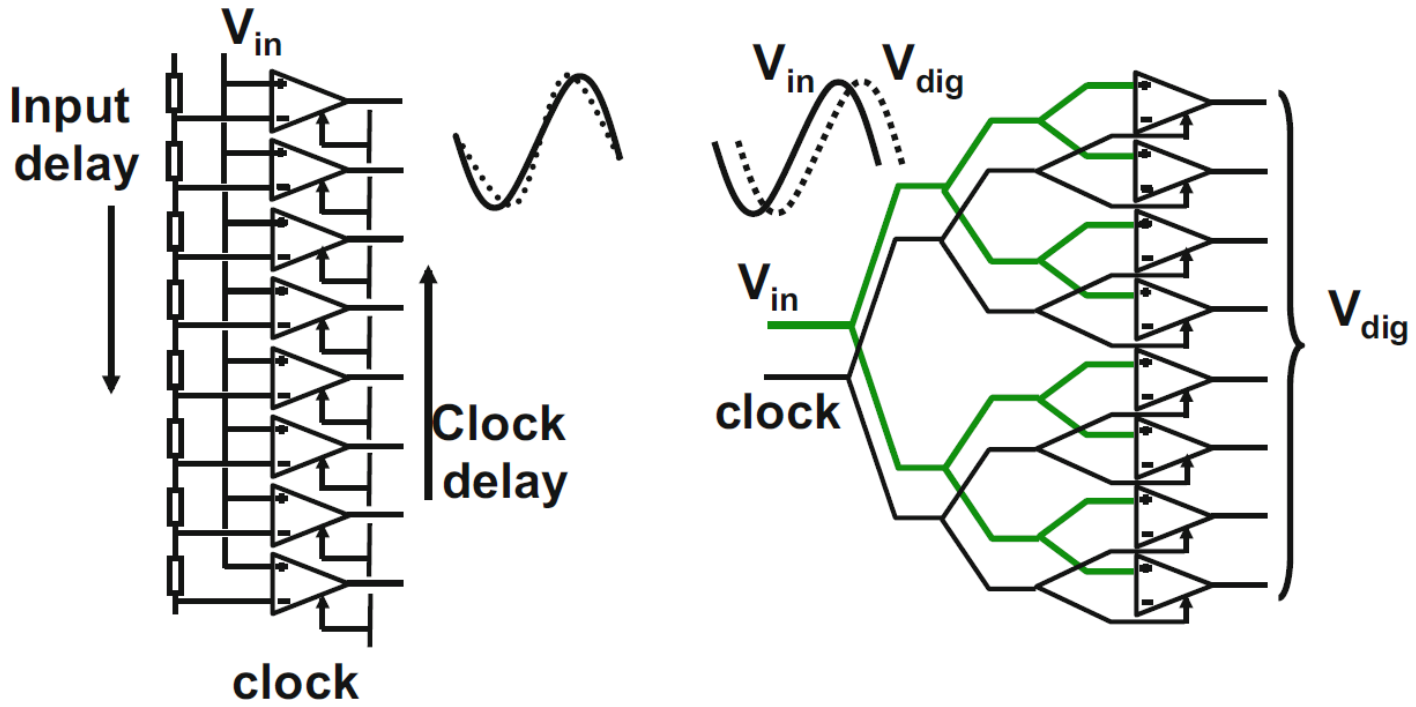
- Analysis shows: $HD2 = 20\log\frac{\omega_{sig}R_{sig}(C_{max}-C_{\min})}{4}$
- Differential architecture cancels 2nd order distortion
  - But more current and area



[M. Pelgrom, 2017]

Tree Layout

- The impedance of the wiring in combination with a string of load elements (e.g., inputs to the comparators) can easily lead to delay differences between individual comparators
  - Timing error translated to 2nd order distortion $\sim 0.5\omega_{sig}\Delta T$
- Tree-like layout is necessary to avoid delay differences



[M. Pelgrom, 2017]

Flash ADC Example

- Given:
  - $V_{REF} = 1V, R_{tap} = 1\Omega, C_{tap} = 100fF, and\ N = 7$

- Time constant for resistor ladder

$$\tau = \frac{R_{tot}C_{tot}}{\pi^2} = \frac{R_{tap}C_{tap}2^{2N}}{\pi^2} = 0.16ns$$

  - R_{tot} is total resistance and C_{tot} is total capacitance
- For 0.5LSB error

$$f_s = \frac{1}{0.69(N+1)\tau} \approx 1.1GHz$$

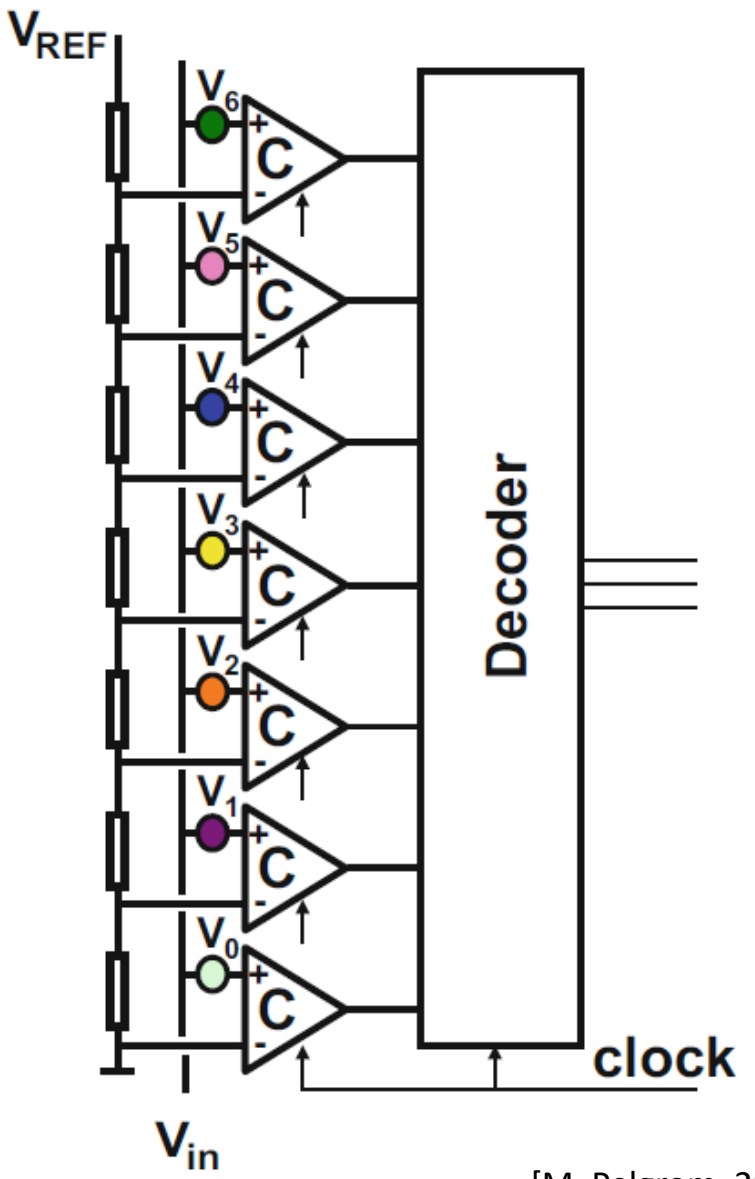
- $R_{tot} = 128\Omega \rightarrow I = \frac{V_{REF}}{R_{tot}} = 8mA$
- Low-ohmic ladder is required: Often constructed from metal layers

Flash Comparator

- Requirements:
  - Low capacitive load
  - No DC input current
  - Low kick-back noise
  - High switching speed (large bandwidth)
  - Low power
  - Low random offset
- All requirements need small devices except the offset requirement
  - 0.5 LSB must be > 3-sigma-offset
  - BJT has 10x lower offset compared to MOSFET
    - But it draws DC current ➔ Use Darlington pair

Comparator Offset

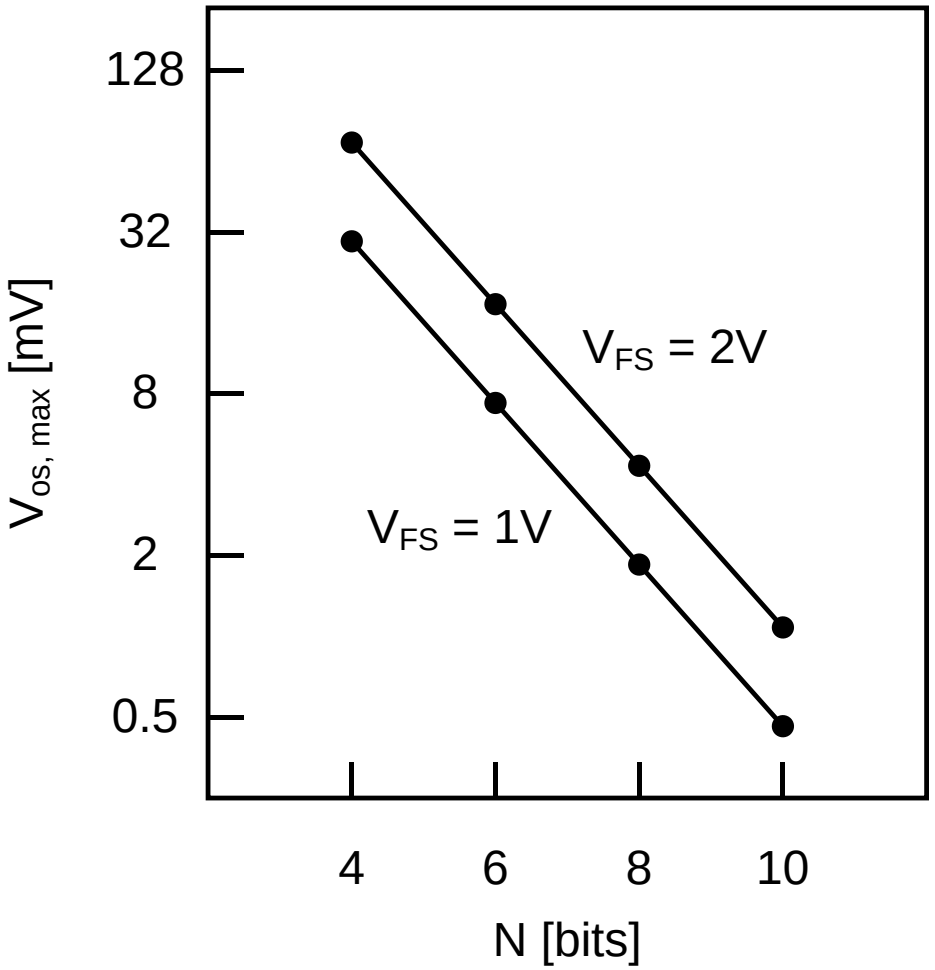
- Flash resolution limited by the input referred mismatch of the comparators
- For BJT $\sigma_{in,os} \approx 0.3mV$
- For MOSFET $\sigma_{in,os}$ is much higher
  - Ex: $\sigma_{in,os} \approx 5mV$
    - 0.5LSB > $3\sigma_{in,os}$
    - LSB = 30mV
    - Let VFS = 1V
    - N = $\log_2$(VFS/LSB) = 5-bit
- Input CM difference creates systematic mismatch between comparators



[M. Pelgrom, 2017]

Offset-Limited Resolution

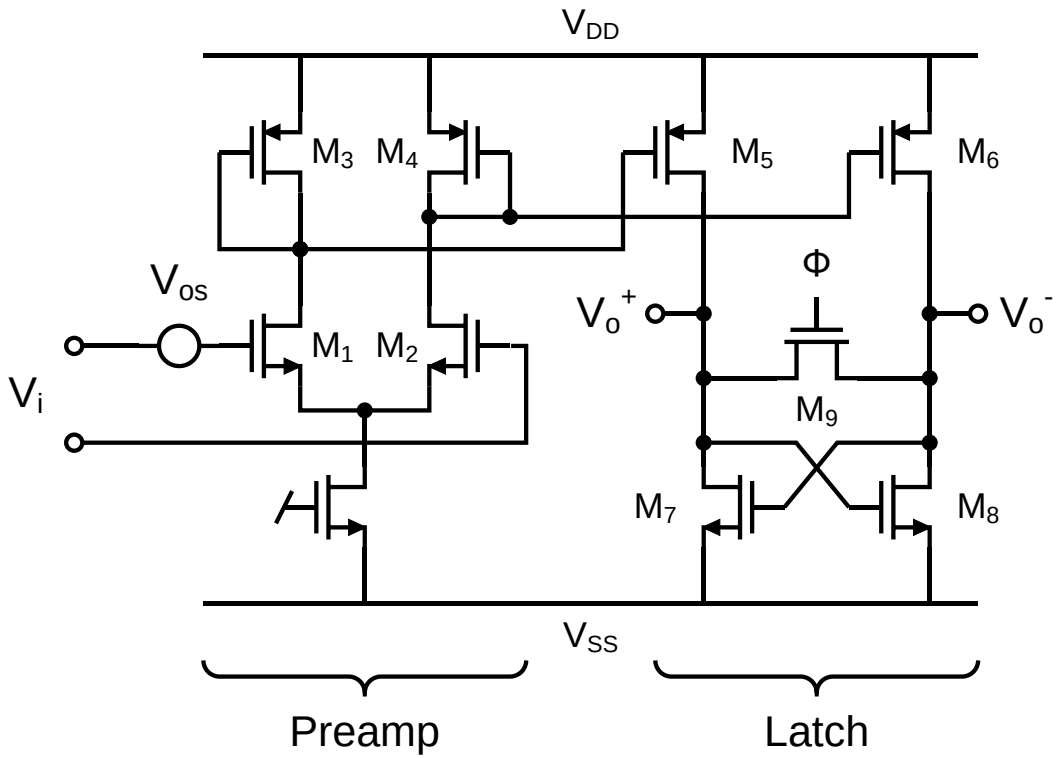
- Practically limited to resolutions of 4-8 bits



Comparator Offset Sources Revisited

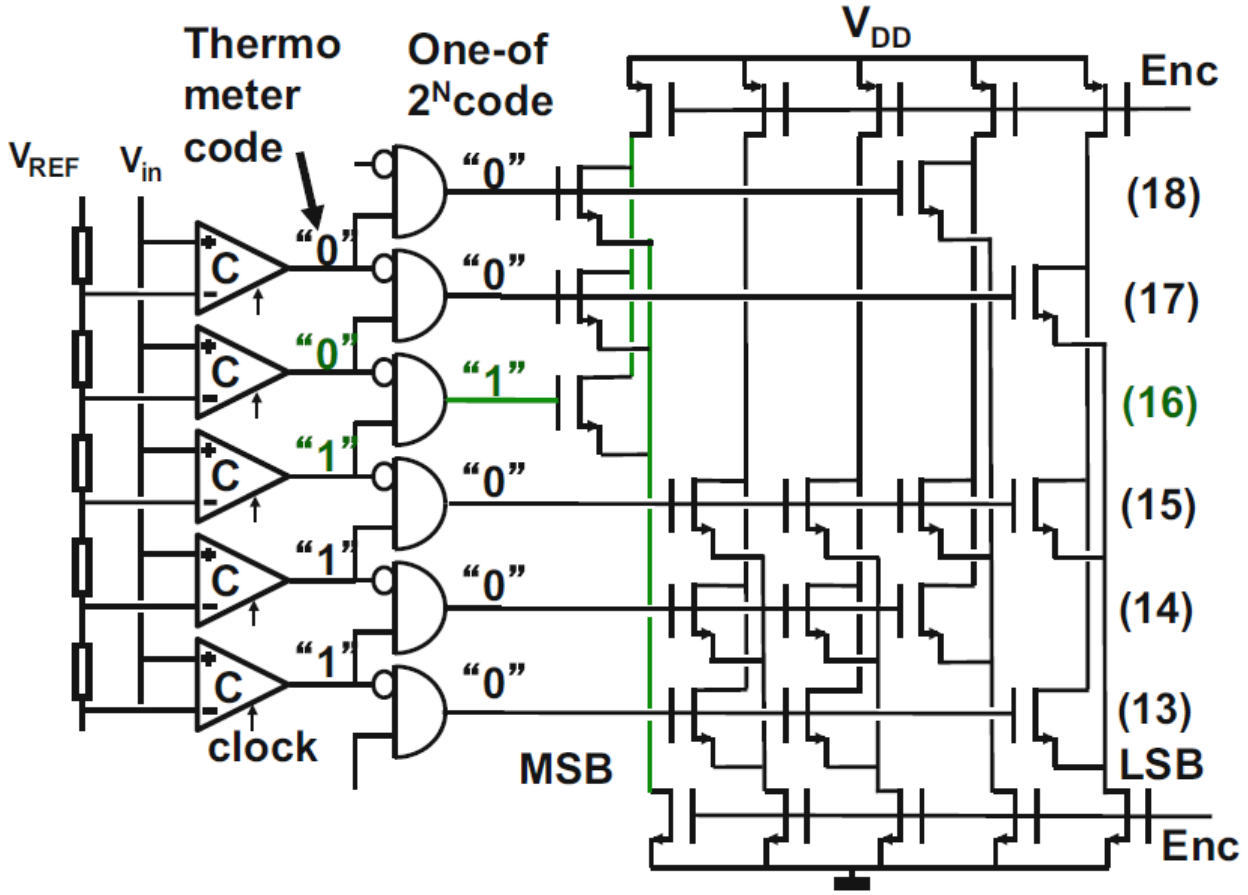
- Preamp input pair mismatch (V_{th},W,L)
- PMOS loads mismatch
- Latch mismatch
- CI / CF imbalance of reset switch (M_9)
- Clock routing
- Parasitics

- Typical flash comparator may use multiple preamplifiers



Thermometer Encoder

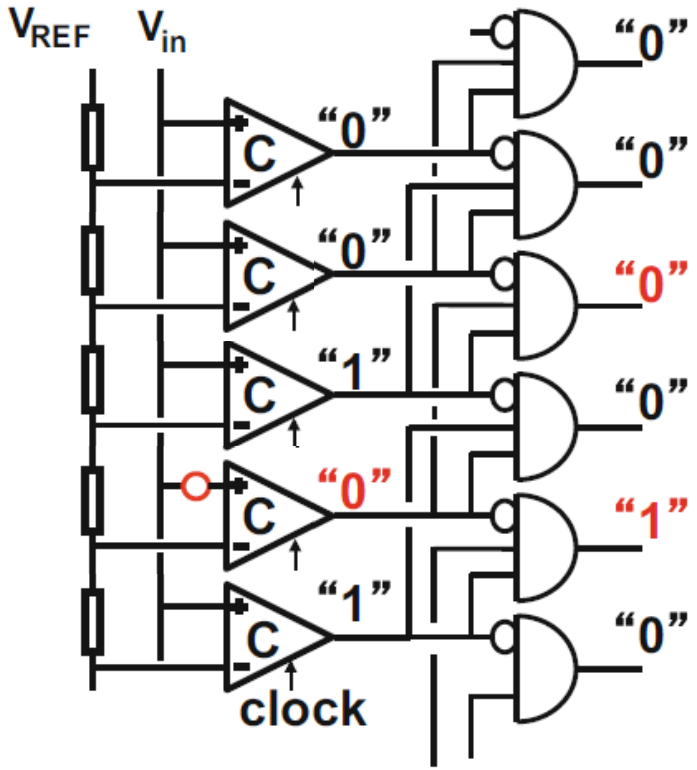
- Thermometer code converted to 1-of-2^N code
- Encoder to straight binary similar to dynamic NOR gate (wired-NOR) ➔ Matrix of transistors as a straight binary code



[M. Pelgrom, 2017]

Sparkle Codes

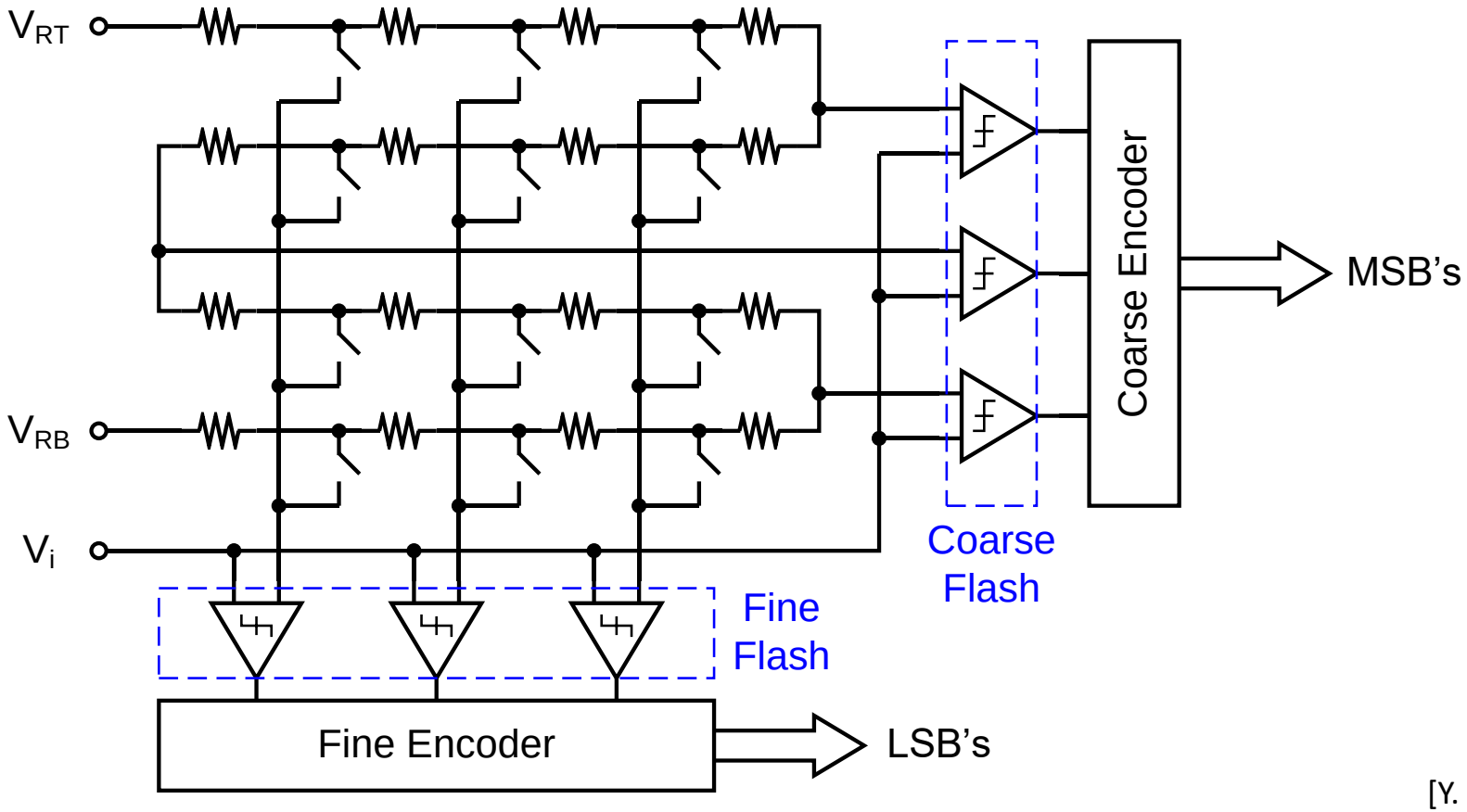
- Mismatch, metastability, noise may make more than one Wired-NOR input active ➔ Sparkle codes (a.k.a. bubble errors)
- Many bubble correction schemes were proposed (may provide “biased correction”)
  - Trade-off between robustness and speed



[M. Pelgrom, 2017]

Subranging/Coarse-Fine ADC

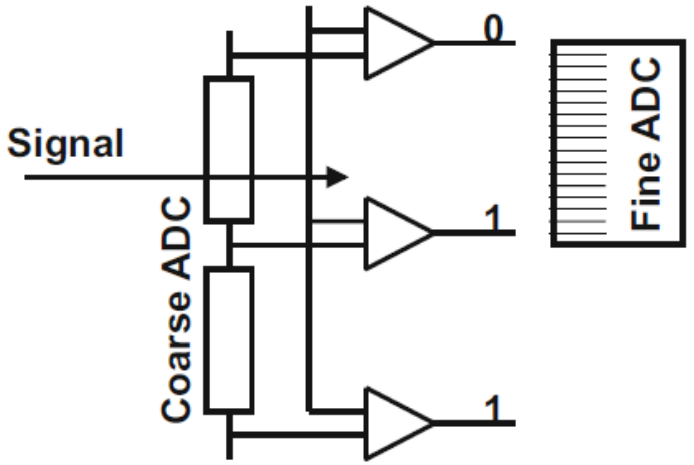
- Ruler analogy: coarse step gets “cm” and fine step gets “mm”
- Reduced complexity (relative to flash): $N = N_1 + N_2$ ➔ $(2^{N_1} + 2^{N_2} - 2)$ comparators
- Reduced C_{in}, area, and power consumption



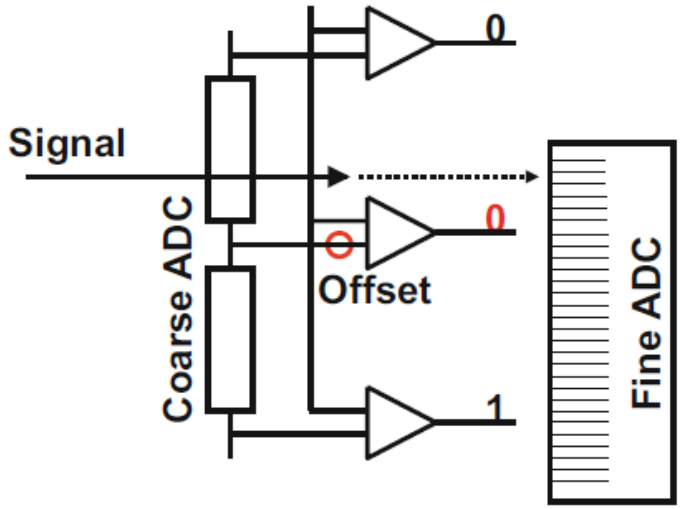
Over-range

- By adding additional levels on both sides of the fine ADC range, errors from the coarse ADC can be corrected
- One form of using redundancy to recover errors

The coarse flash converter takes a correct decision and the fine-converter receives a signal within its range



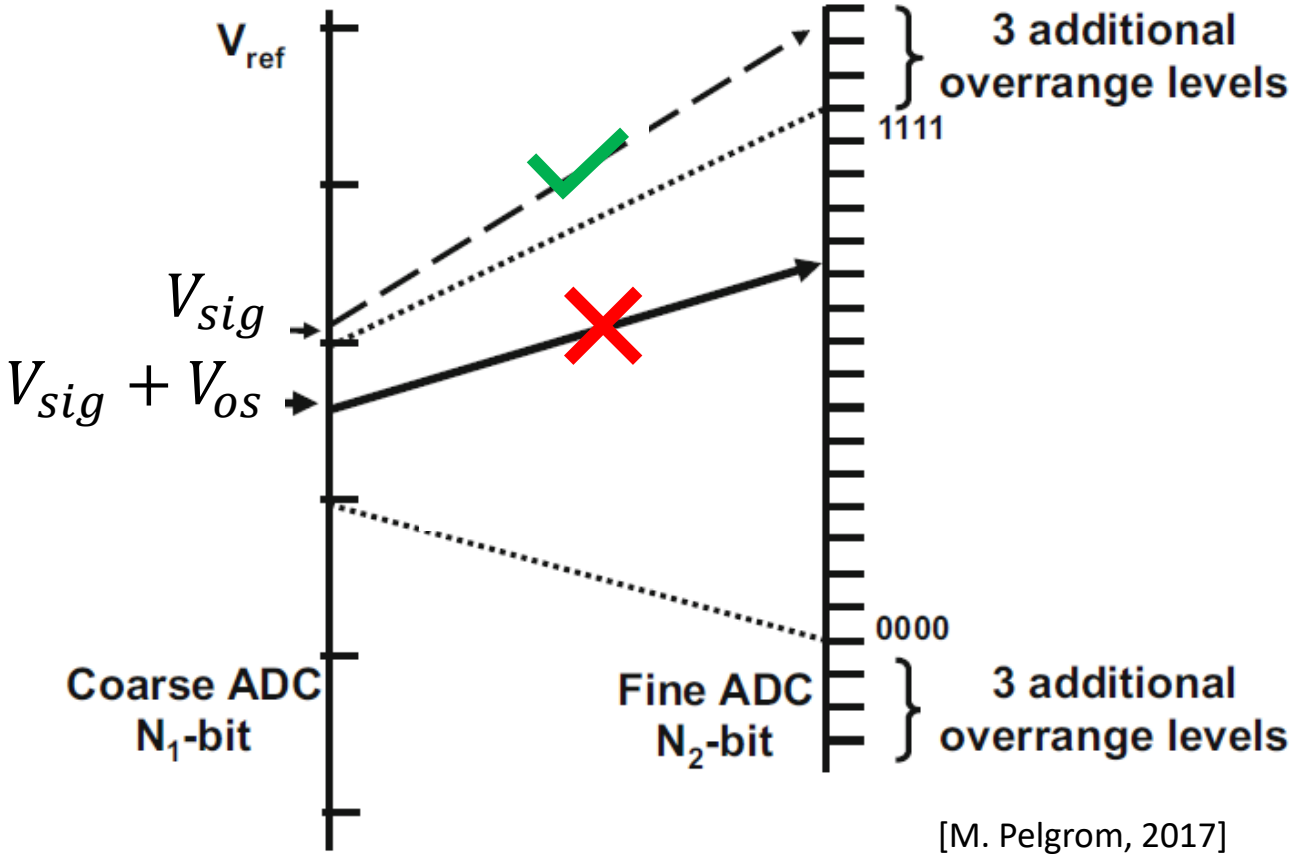
One comparator has offset and the coarse converter indicates the wrong range for the fine converter



[M. Pelgrom, 2017]

Over-range

- Correct coarse decision (dashed line)
- Wrong coarse decision (bold line): Over-range in the fine converter corrects this wrong decision
  - We added 6 more levels to fine
  - $N_{fine} = \log_2(16 + 6) = 4.46\ bit$



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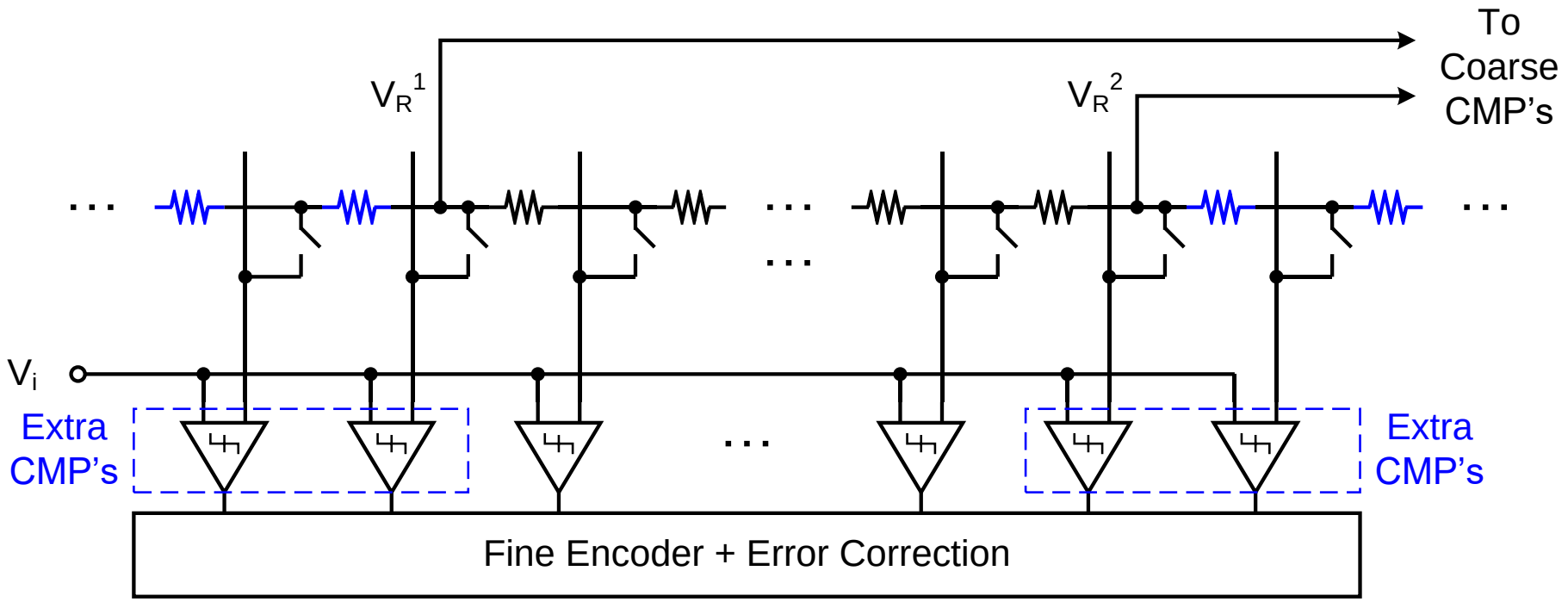
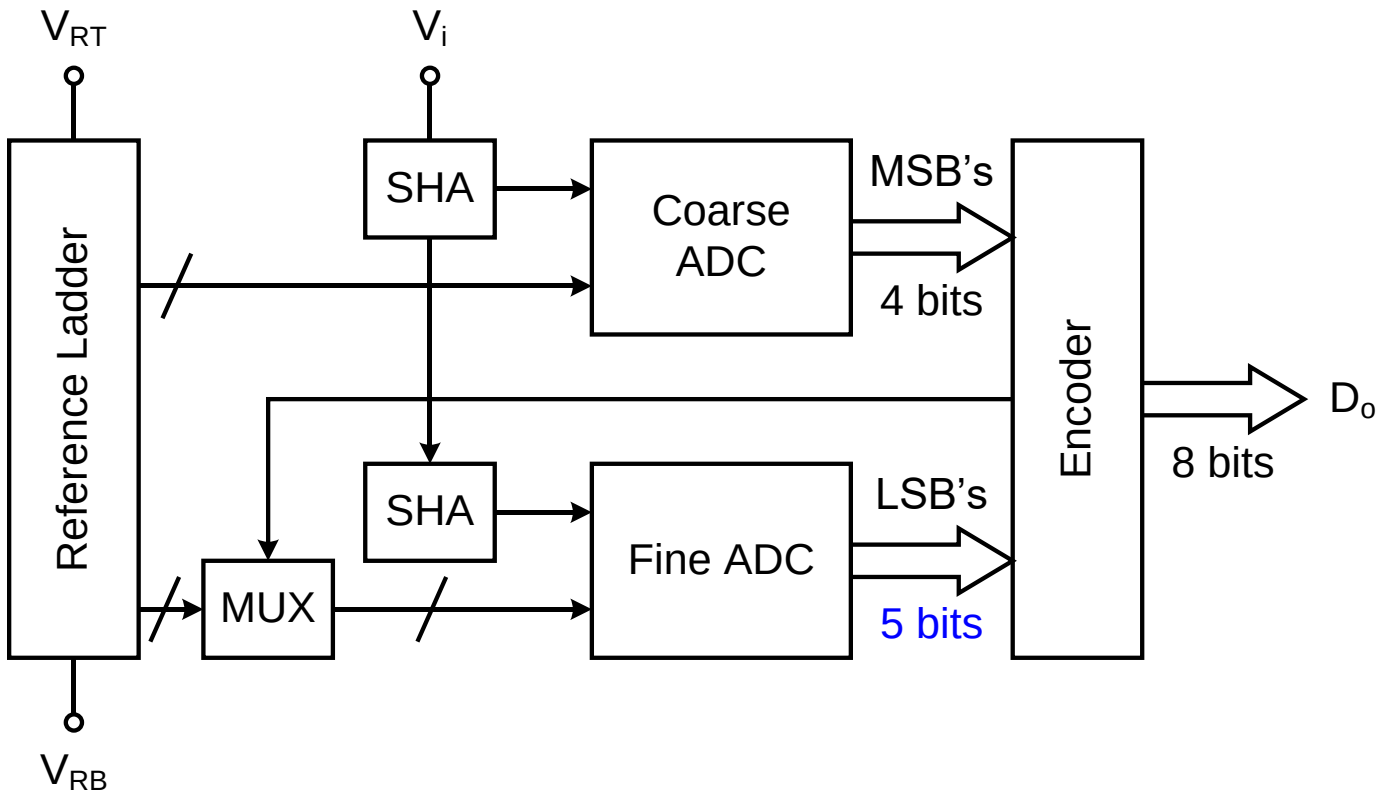
Digital Redundancy in Fine ADC

- The range of fine ADC search extended on both sides
- Offset tolerance on coarse comparators can be relaxed
- Fine comparator offset still must be controlled to N-bit level



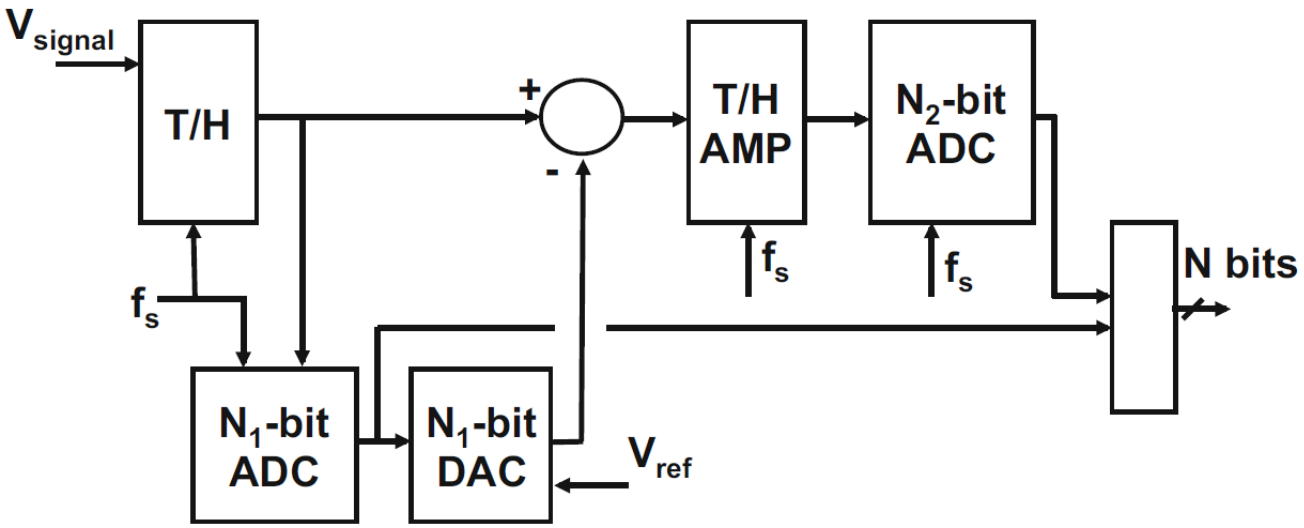
Subranging/Coarse-Fine ADC Block Diagram

- Typically two SHAs are required for the coarse and fine ADCs
- Typically 3 clock phases per conversion
  - Sample + Coarse comparison + Fine comparison
- No residue amplifier required (compare to next slide)



Two-Step Subranging/Pipelined ADC

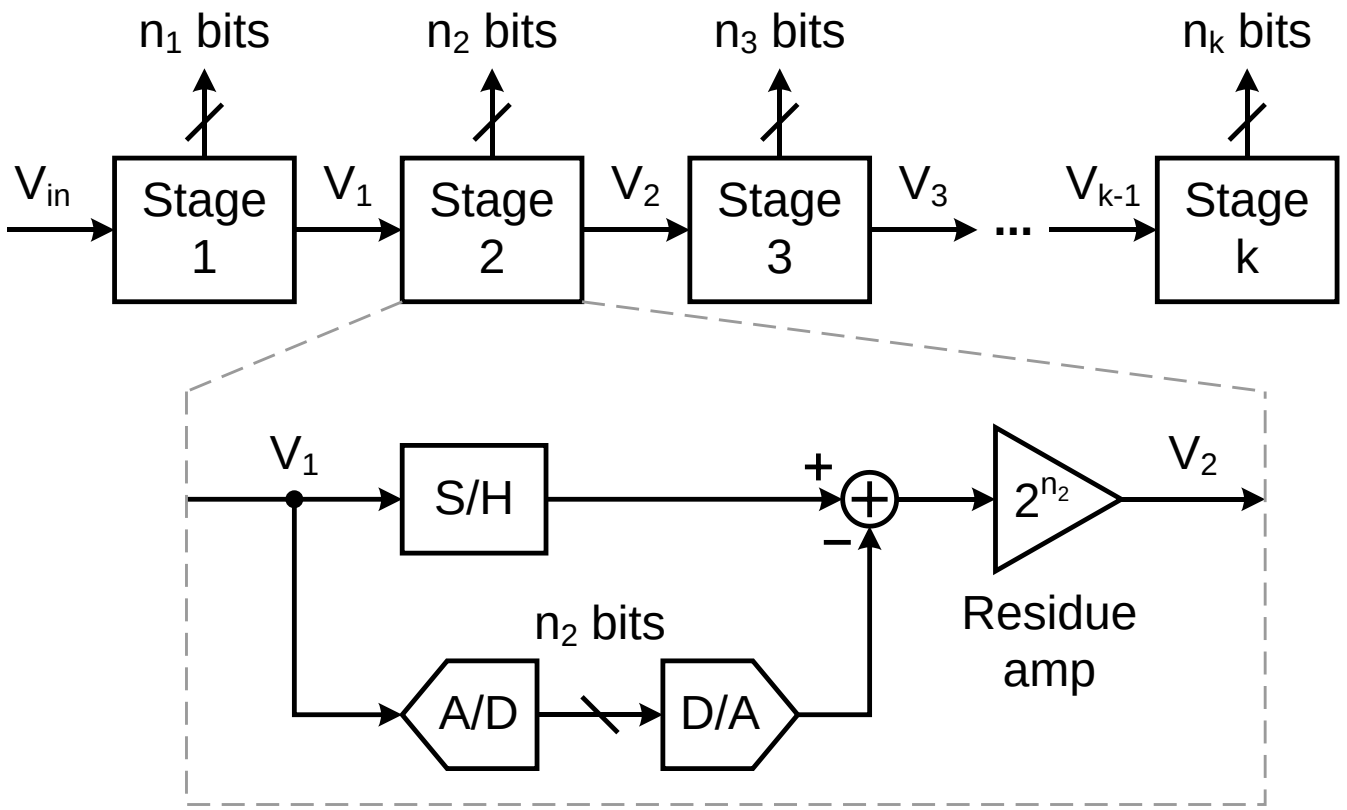
- A coarse ADC estimates the input signal
  - Result fed to a DAC ➔ Subtraction generates residue signal
- A fine ADC converts the residue signal
- Amplification may precede the fine ADC (residue amplifier)
  - Limited speed (GBW = const)
  - 2nd T/H allows pipelining → pipelined ADC
- $N = N_1 + N_2$ ➔ $(2^{N_1} + 2^{N_2} - 2)$ comparators



[M. Pelgrom, 2017]

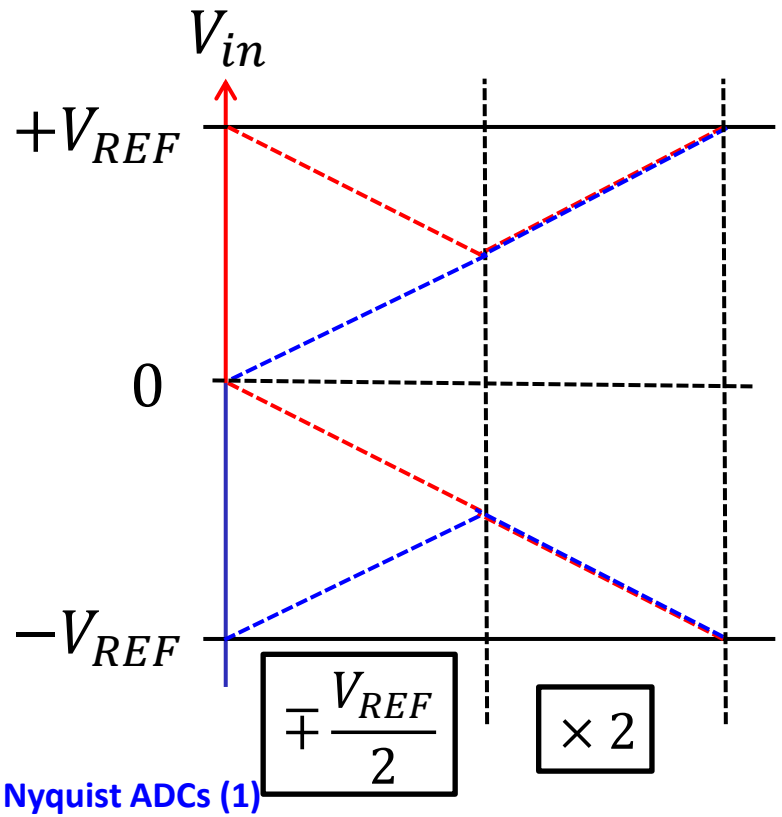
Pipelined ADC

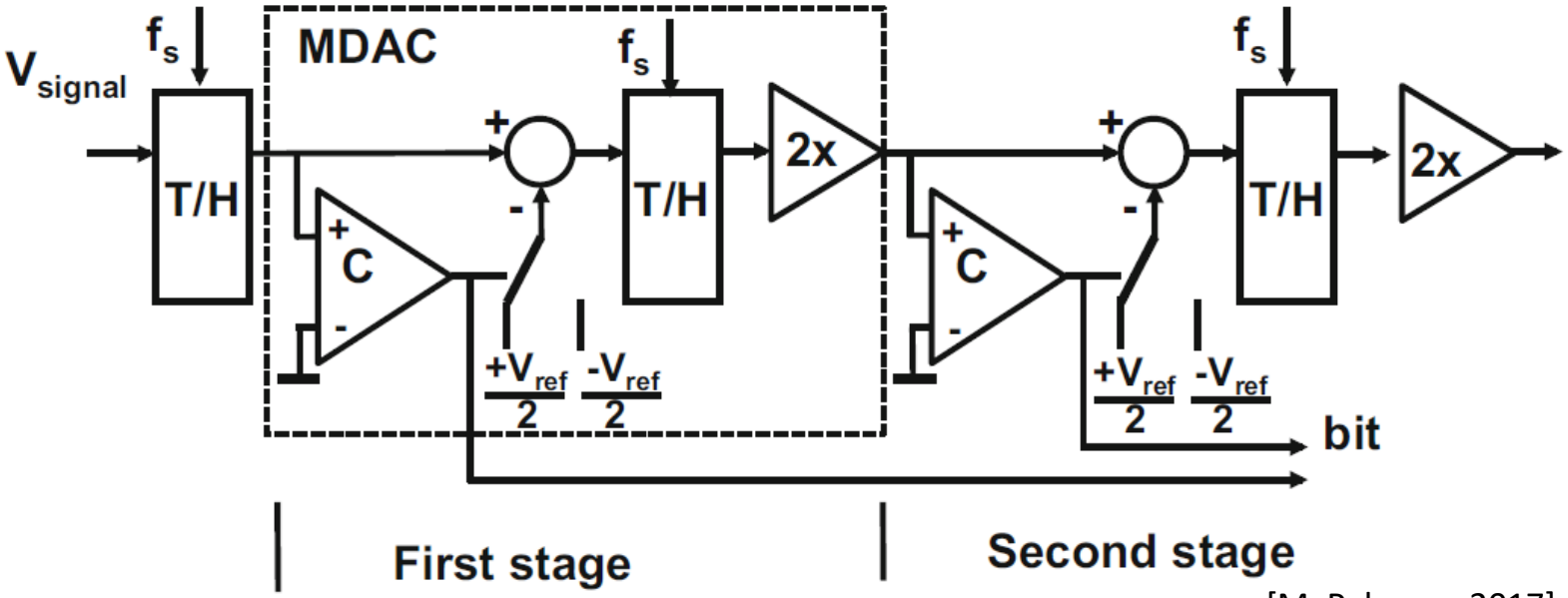
- A generalization of subranging ADC: Cascade of k-bit stages
  - $N = n_1 + n_2 + \cdots + n_k$
- Sample rate is high, but large latency (not suitable for FB loops)



1-bit/stage Pipelined ADC

- The ADC is 1-bit: comparator
- The DAC is also 1-bit ➔ perfectly linear by definition
- Low inter-stage gain (x2): high speed (GBW = const)
- No. of pipelined stages (a.k.a. MDACs) = no. of bits

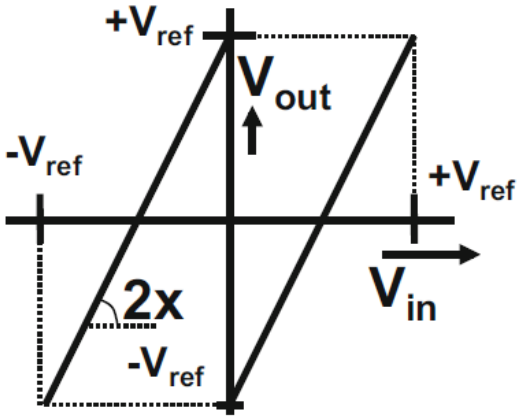




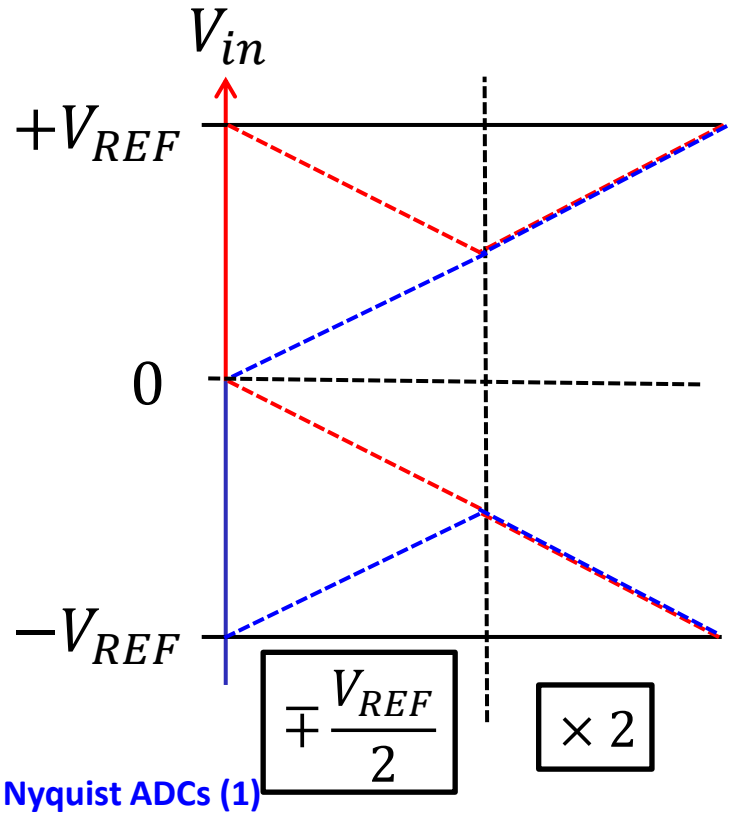
[M. Pelgrom, 2017]

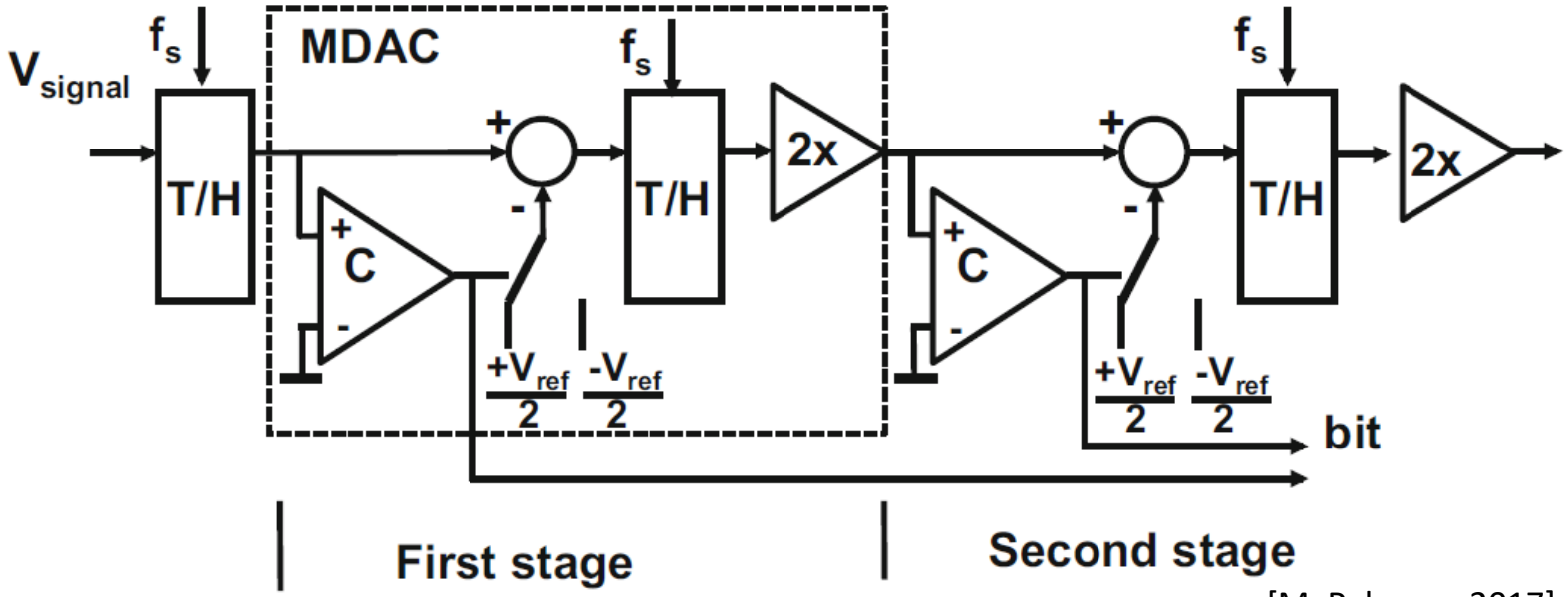
MDAC Characteristics

$$V_{out} = 2\left(V_{in} \mp \frac{V_{ref}}{2}\right)$$



- Comparator threshold defines breakpoint
- DAC output (multiplied by $\frac{DAC\ gain}{V_{in}\ gain} = \frac{2}{2}$) defines x-intercept



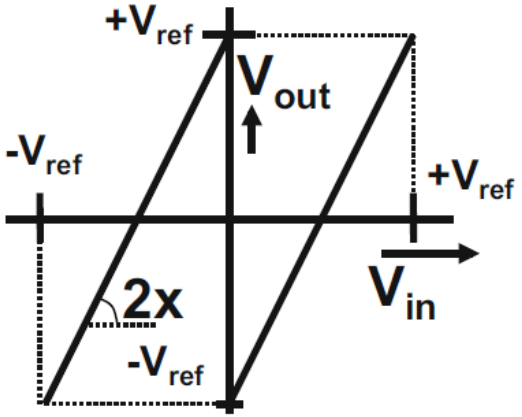


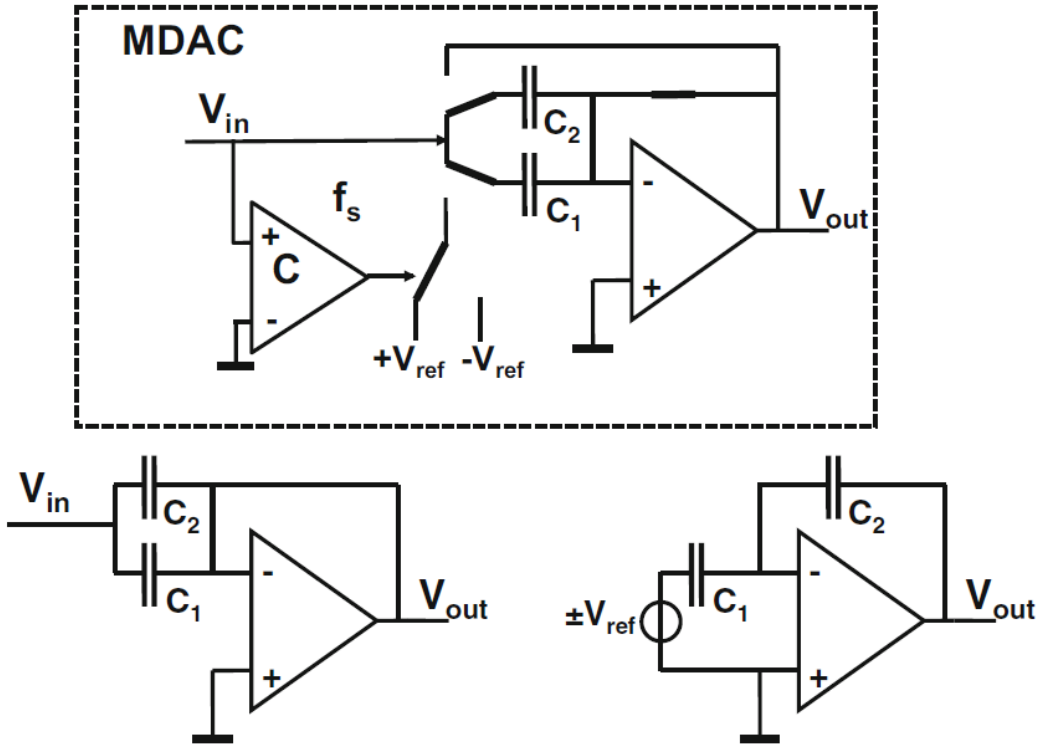
[M. Pelgrom, 2017]

MDAC Implementation

$$V_{out} = \frac{C_1 + C_2}{C_2} V_{in} \mp \frac{C_1}{C_2} V_{ref} = 2\left(V_{in} \mp \frac{V_{ref}}{2}\right)$$

- Comparator threshold defines breakpoint
- DAC output (multiplied by $\frac{DAC\ gain}{V_{in}\ gain} = \frac{1}{2}$) defines x-intercept

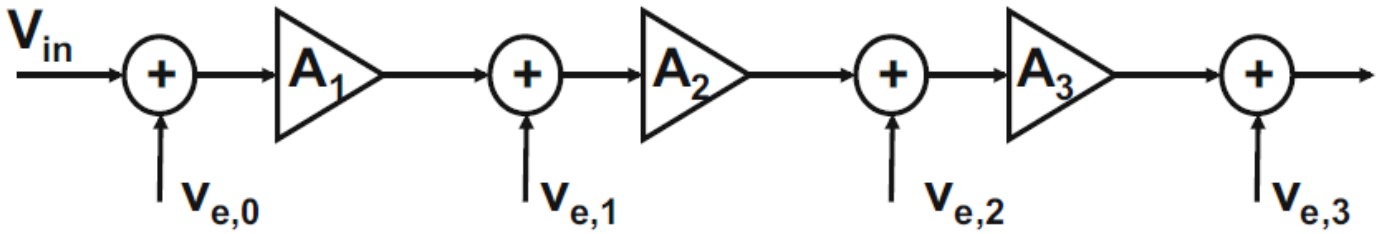




[M. Pelgrom, 2017]

Pipelined ADC Error Sources

- Comparator offset, residue amplifier offset, exact 2x amplification
- The offset and gain errors must together remain under 0.5LSB to obtain a correct transfer curve
  - With some offset compensation this condition can be reached for 10–12 bit accuracies
- Errors in early stages are more critical (later errors divided by gain)



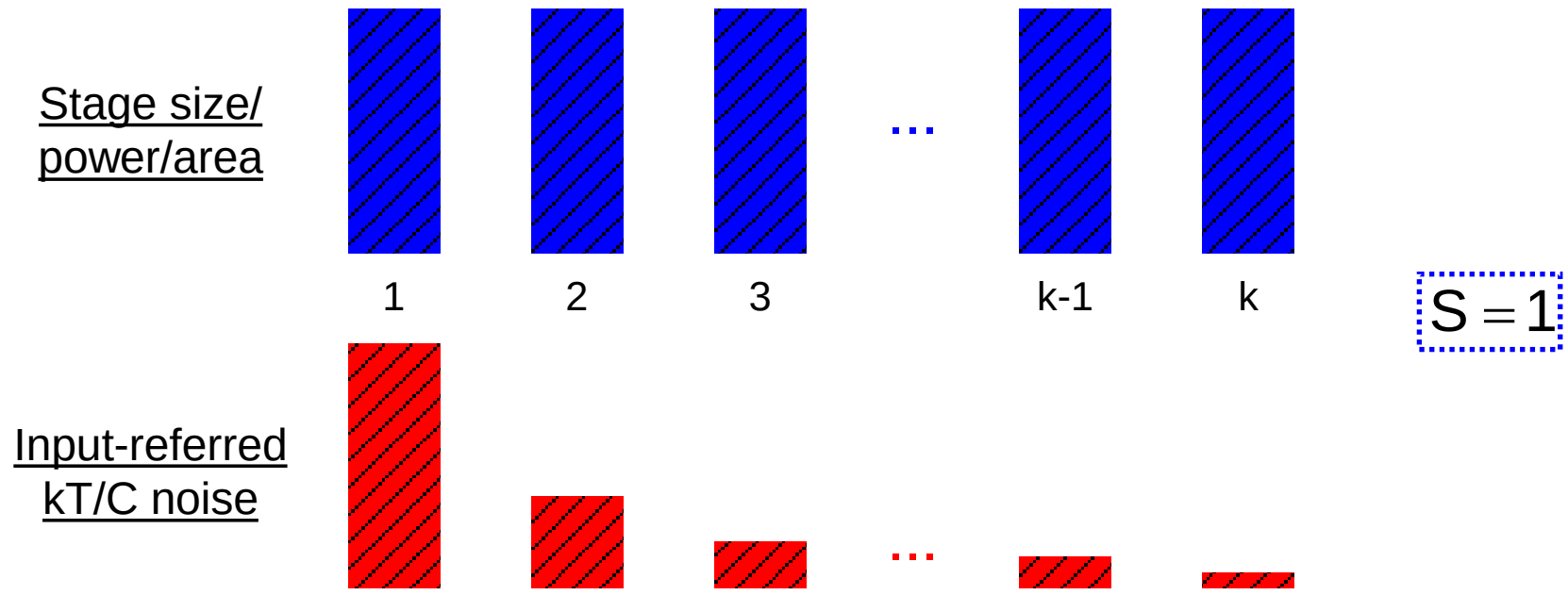
$$v_{in,det} = v_{e,0} + \frac{v_{e,1}}{A_1} + \frac{v_{e,2}}{A_1 A_2} + \frac{v_{e,3}}{A_1 A_2 A_3} + \dots$$

$$v_{in,random} = \sqrt{v_{e,0}^2 + \frac{v_{e,1}^2}{A_1^2} + \frac{v_{e,2}^2}{A_1^2 A_2^2} + \frac{v_{e,3}^2}{A_1^2 A_2^2 A_3^2} + \dots}$$

[M. Pelgrom, 2017]

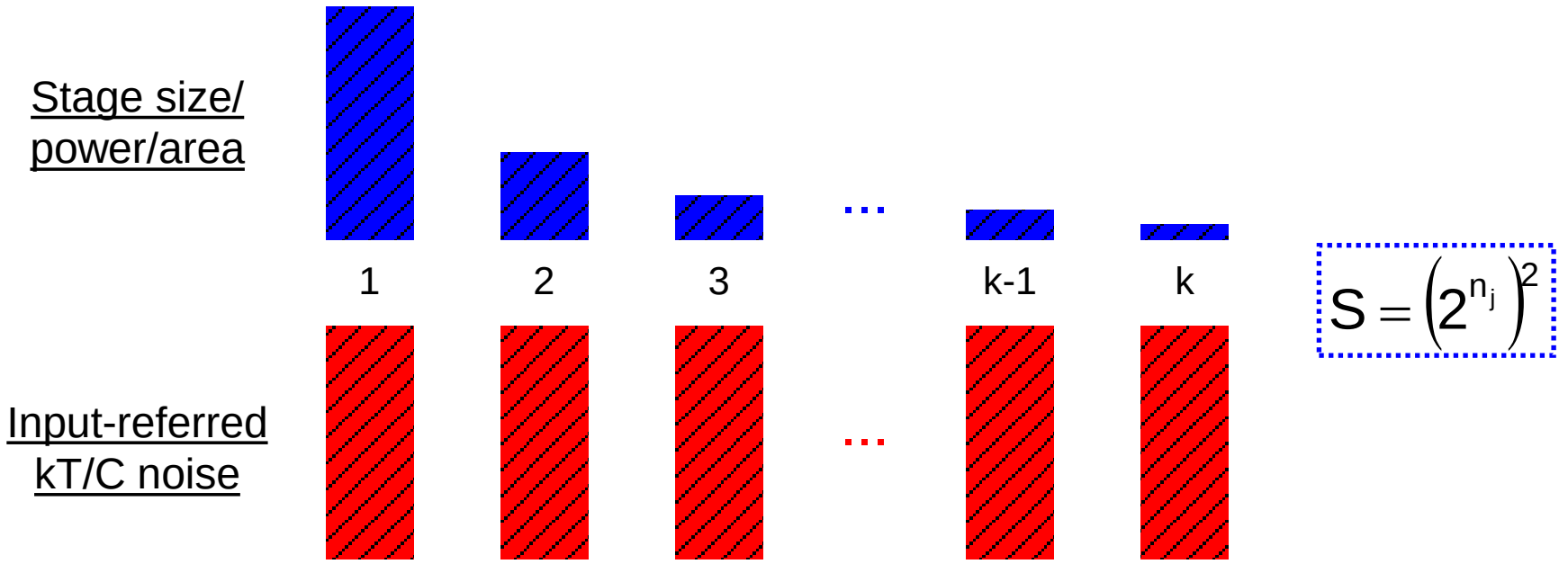
Scaling Pipelined Stages

- No Stage Scaling
  - All stages identically sized – same capacitors, op-amps, comparators → S = 1
  - Later stages are clearly oversized due to inter-stage gains
- We can save a lot of power/area in later stages with minimal increase in noise



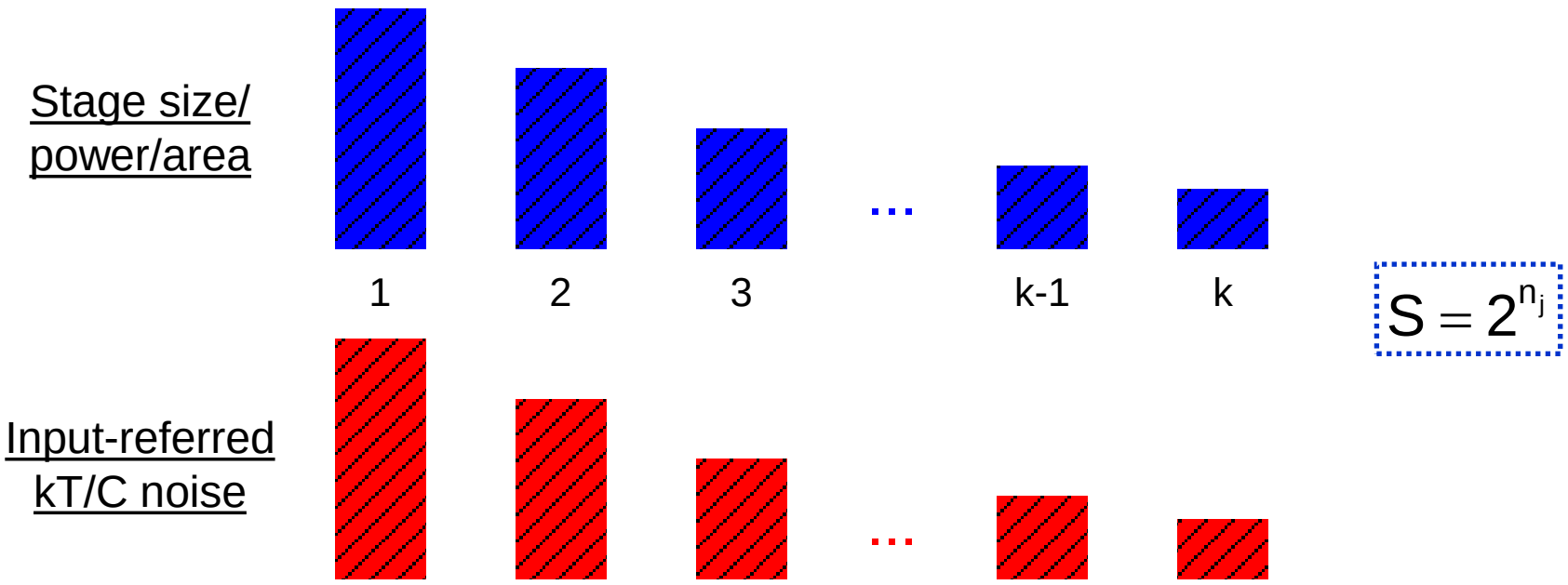
Scaling Pipelined Stages

- Aggressive Stage Scaling
  - Stages sized such that the input-referred noises are identical → $S \approx (2^{n_j})^2$
  - Later stages are clearly downsized too aggressively
- We can save a lot of noise in later stages with minimal increase in power/area



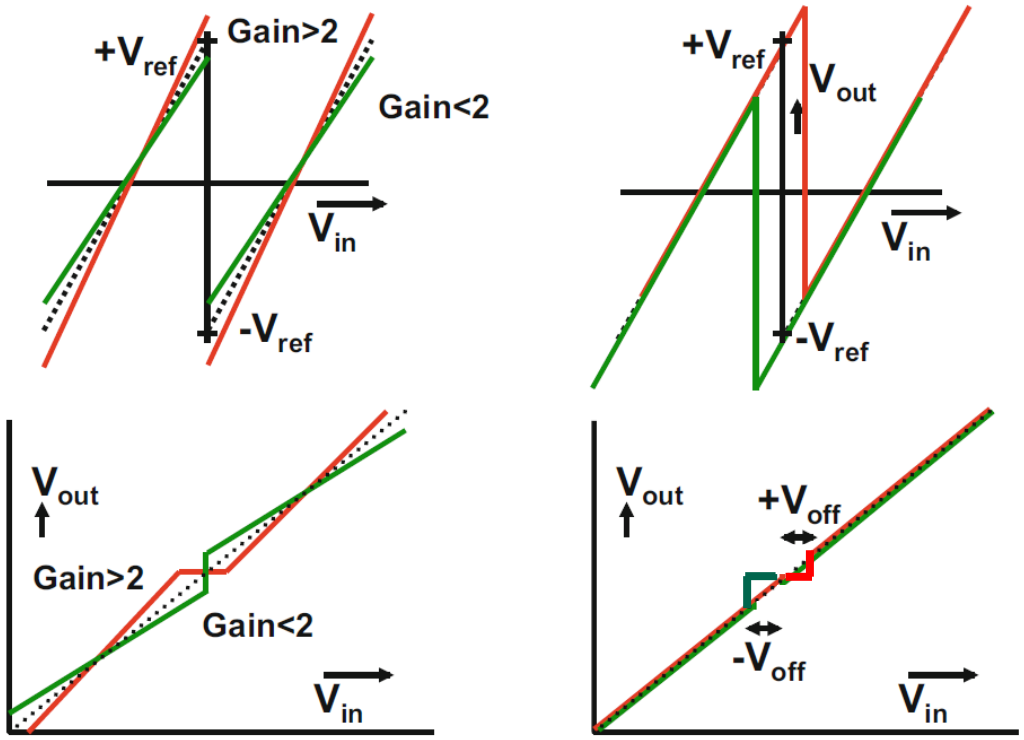
Scaling Pipelined Stages

- Optimum Stage Scaling
  - Optimum scaling lies in between the two extremes → $S \approx 2^{nj}$
- Area/power vs noise trade-off is balanced (gain vs loss is roughly the same)



Pipelined ADC Errors

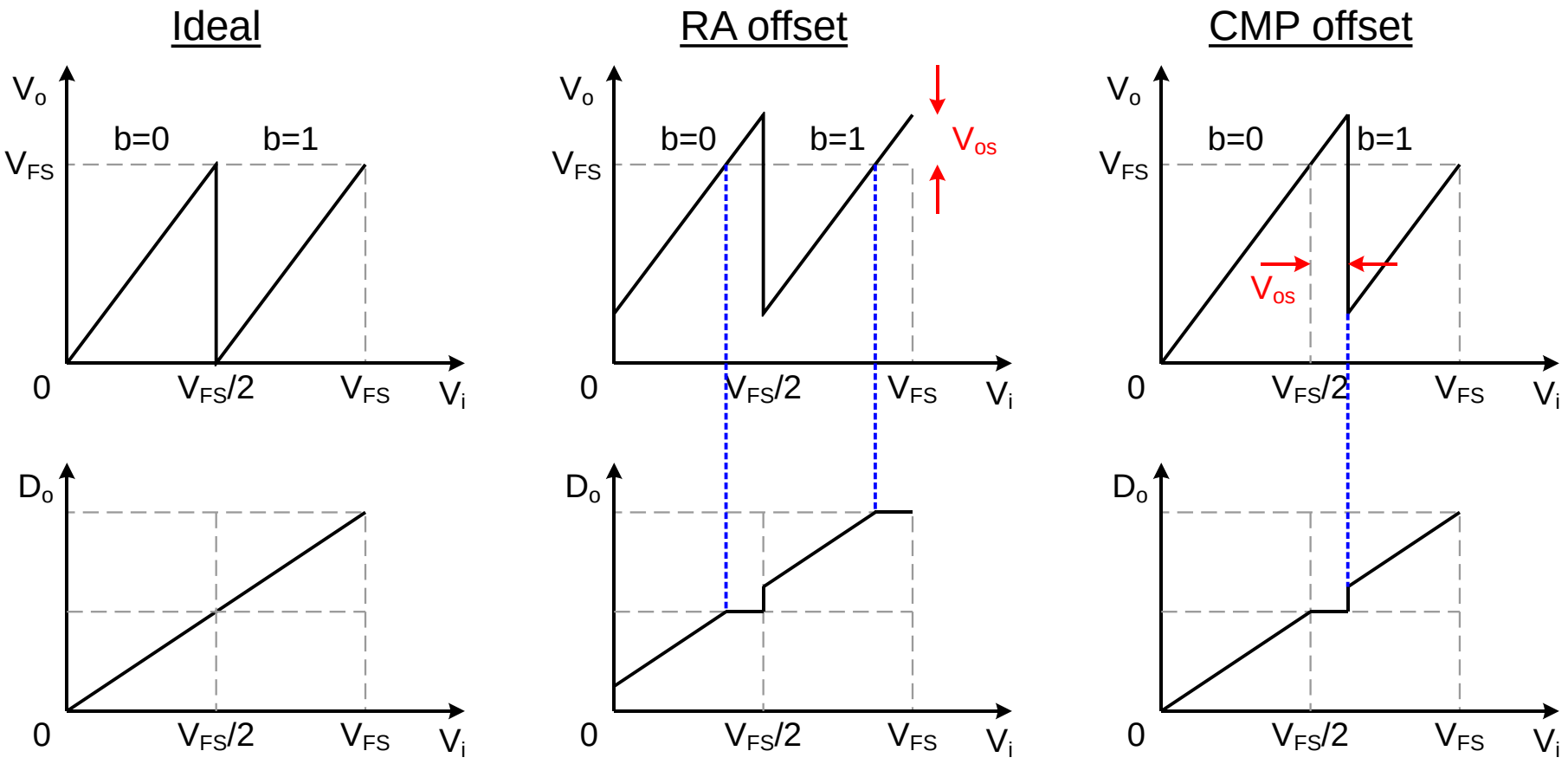
- Comparator threshold defines the breakpoint of MDAC transfer characteristics
- Offset/gain errors
  - Non-linearity in the overall transfer function
  - Offset errors can be solved by using 1.5-bit architecture



[M. Pelgrom, 2017]

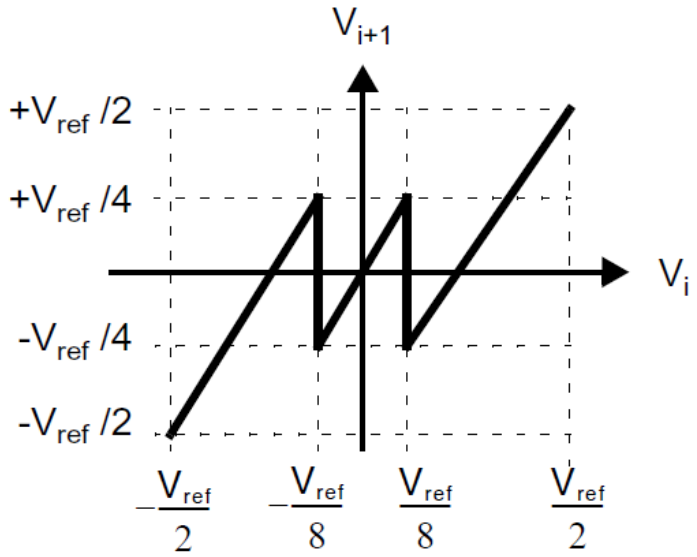
Offset Errors

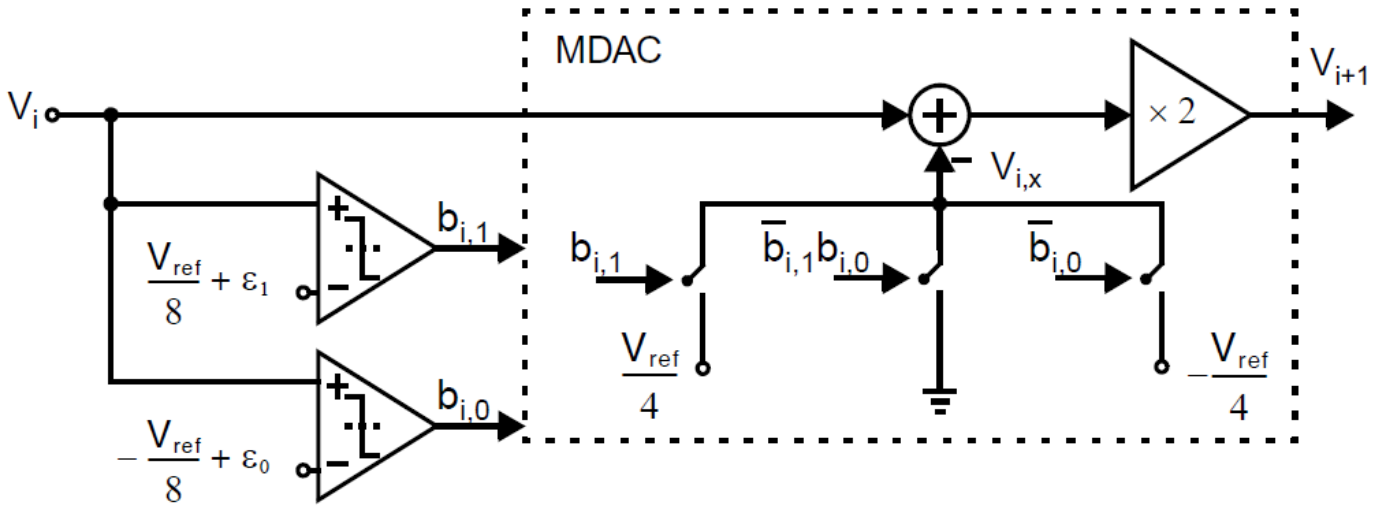
- Reduce offset sensitivity by using 1.5-bit topology



1.5-bit Concept

- 1-bit ADC: 2-levels, one threshold
- 2-bit ADC: 4-levels, three thresholds
- The use of two thresholds (three levels) is referred to as 1.5-bit ADC ($\log_2 3 \approx 1.58$)
  - Comparator and residue amplifier (RA) offsets can be corrected

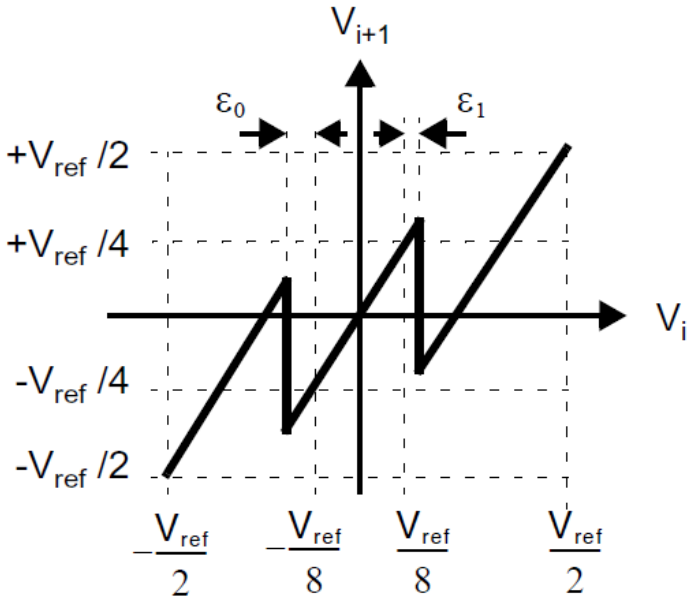


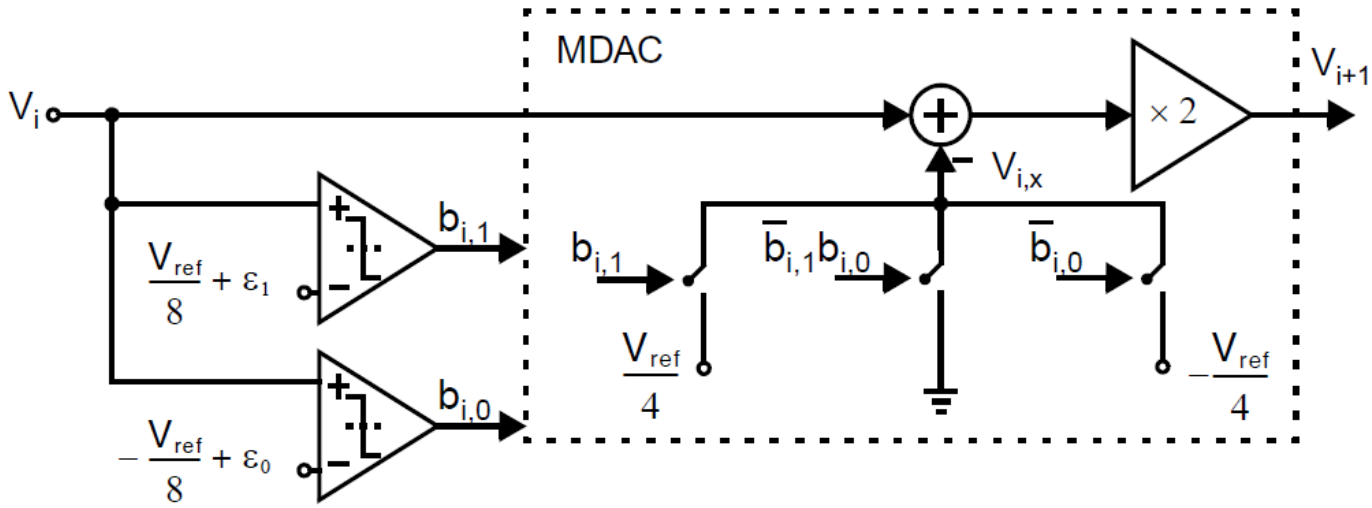


[Johns and Martin, 2012]

Digital Correction

- 1.5-bit digital outputs: 00 (left), 01 (middle), 11 (encoded as 10) (right)
- Left region -> certain 0. Right region -> certain 1,
- Middle region -> o/p postponed (P) to next stage
  - Output is amplified (x2) to be better resolved by next stage
- Errors in comparator thresholds are corrected by next stage

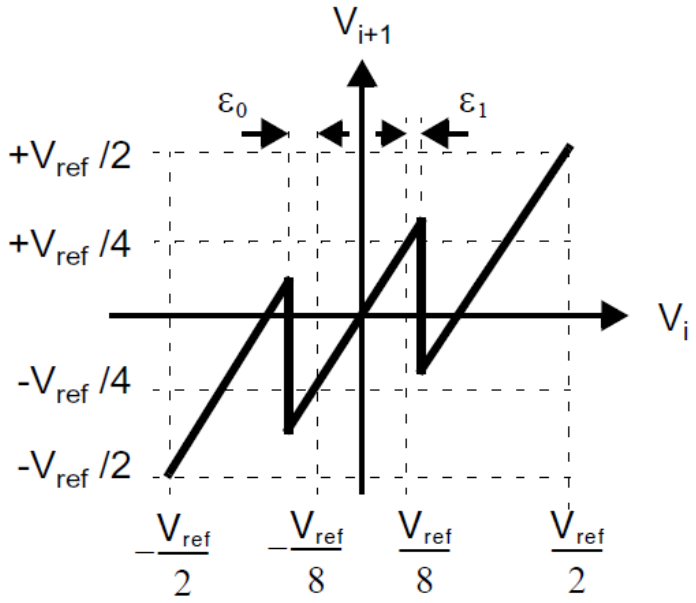


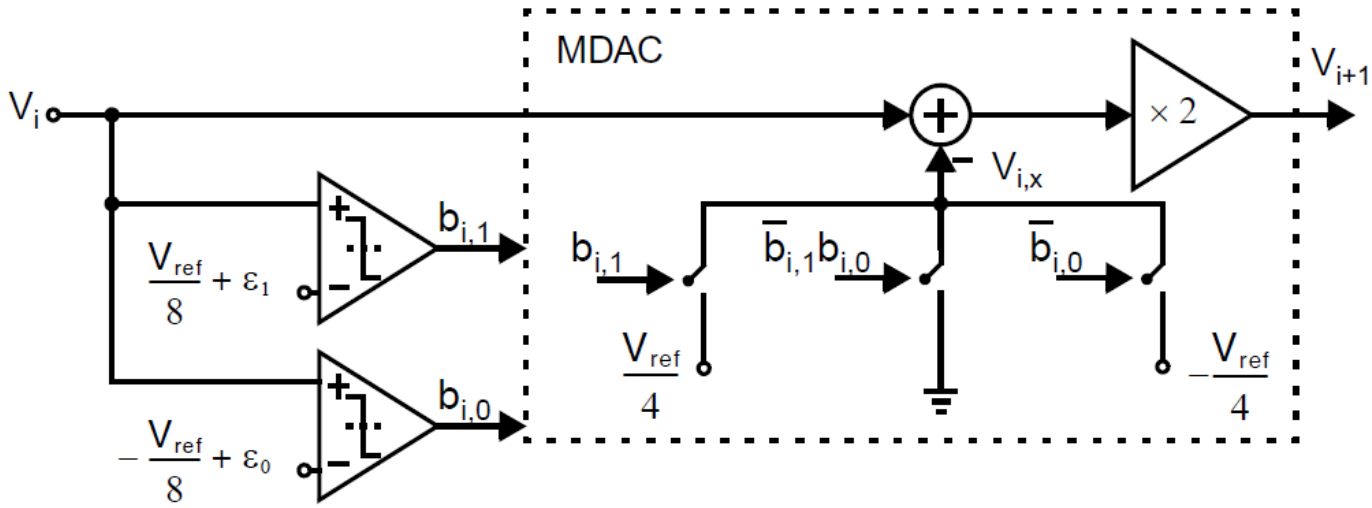


[Johns and Martin, 2012]

Digital Correction

- As long as the error is stored in the residue it can be corrected
  - The information is not yet lost
- Digital Correction corrects comparator and RA offset errors
  - It does not correct DAC or residue generator errors
- Digital adder required to combine digital output

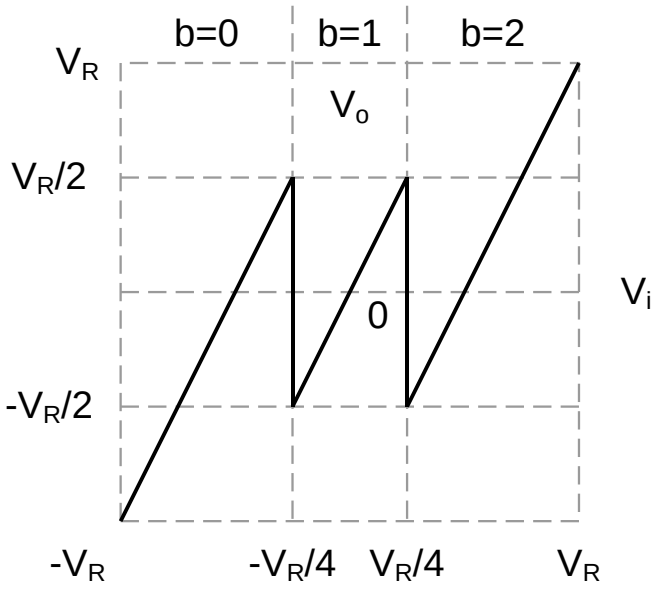




[Johns and Martin, 2012]

1.5-bit Example

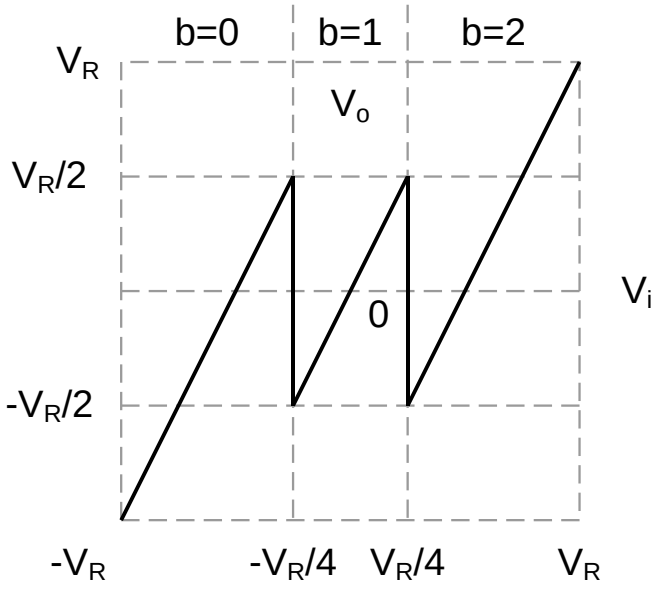
- Assume 6-bit pipelined ADC with 1.5-bit/stage
- Let $V_R = +1V$ and $V_{in} = -0.21$
- Note that $dec2bin\left(\frac{V_{in}-(V_{REF,LOW})}{\Delta V_{REF}} \times 2^N\right) = dec2bin(25.3) = 011001$

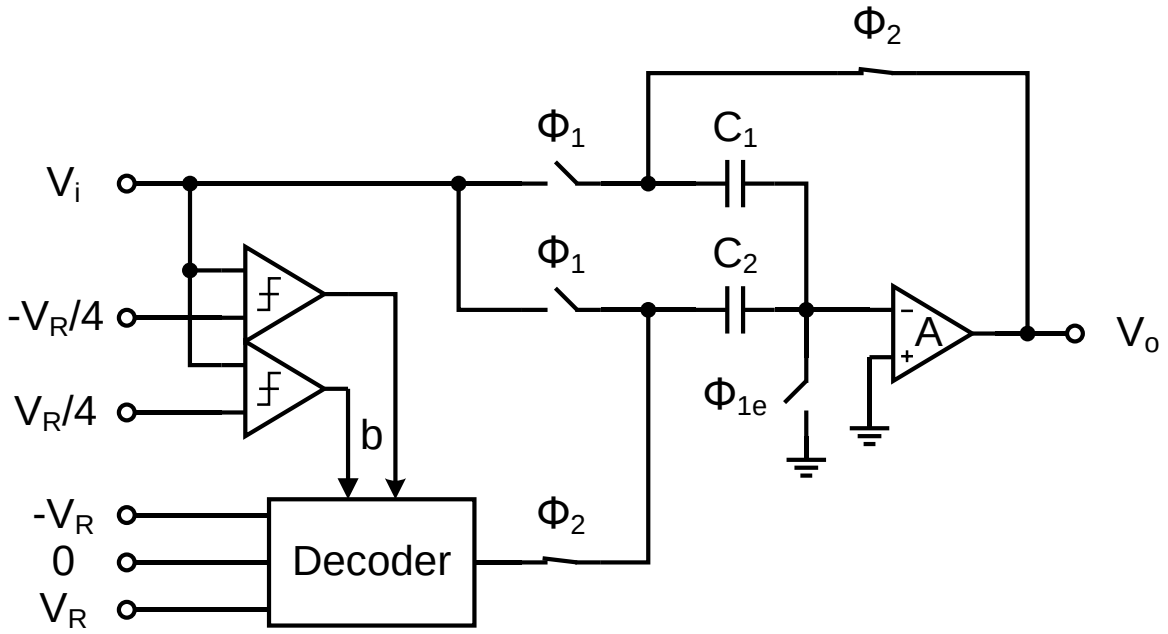


Stage Input (V)	MDAC operation	Decision	B5	B4	B3	B2	B1	B0
$V_{in} = -0.21$	$V_x \times 2$	P	0	1				
-0.42	$\left(V_x + \frac{V_{REF}}{2}\right) \times 2$	0		0	0			
0.16	$V_x \times 2$	P			0	1		
0.32	$\left(V_x - \frac{V_{REF}}{2}\right) \times 2$	1				1	0	
-0.36	$\left(V_x + \frac{V_{REF}}{2}\right) \times 2$	0					0	0
0.28	$-$	1						1
			0	1	1	0	0	1

1.5-bit Stage

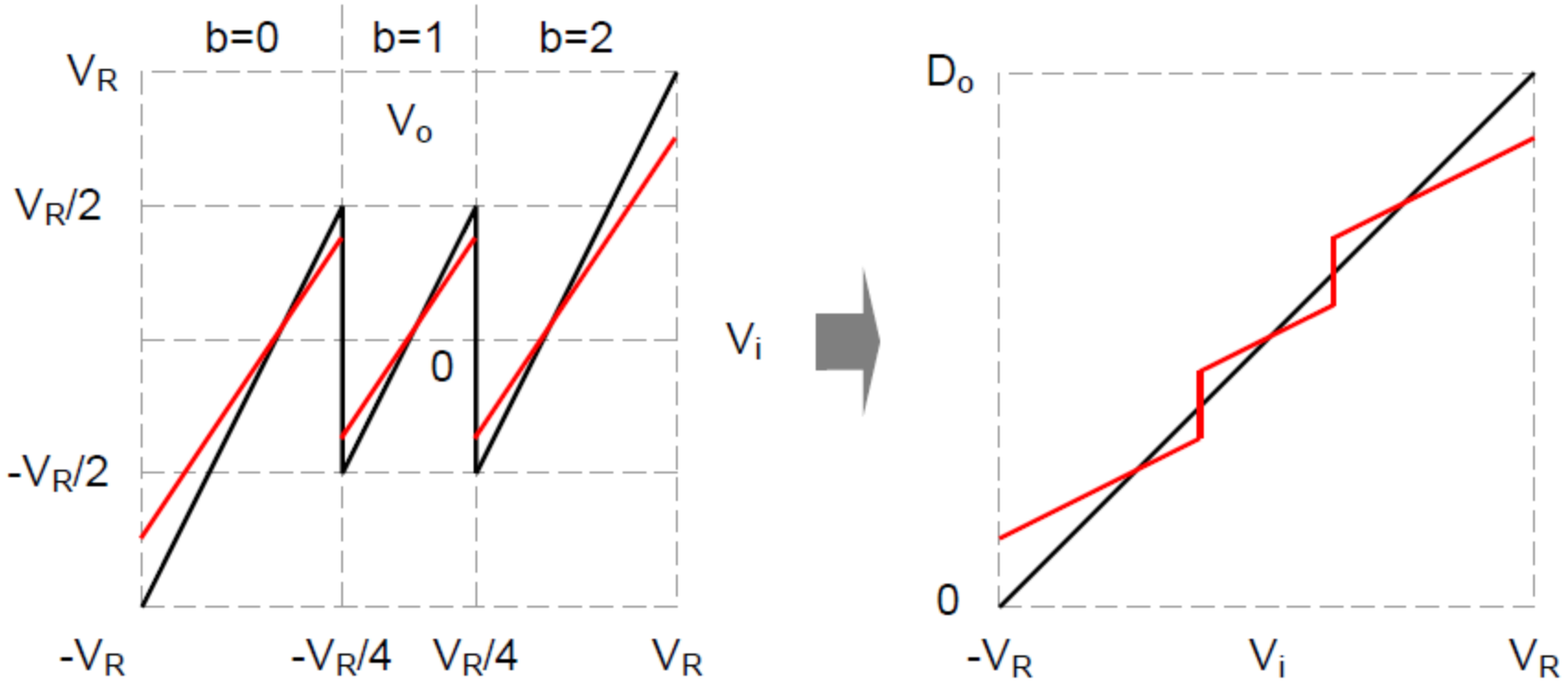
- 2X gain + 3-level DAC + subtraction all integrated
- Digital redundancy relaxes the tolerance on CMP/RA offsets





RA Gain Error and Non-linearity

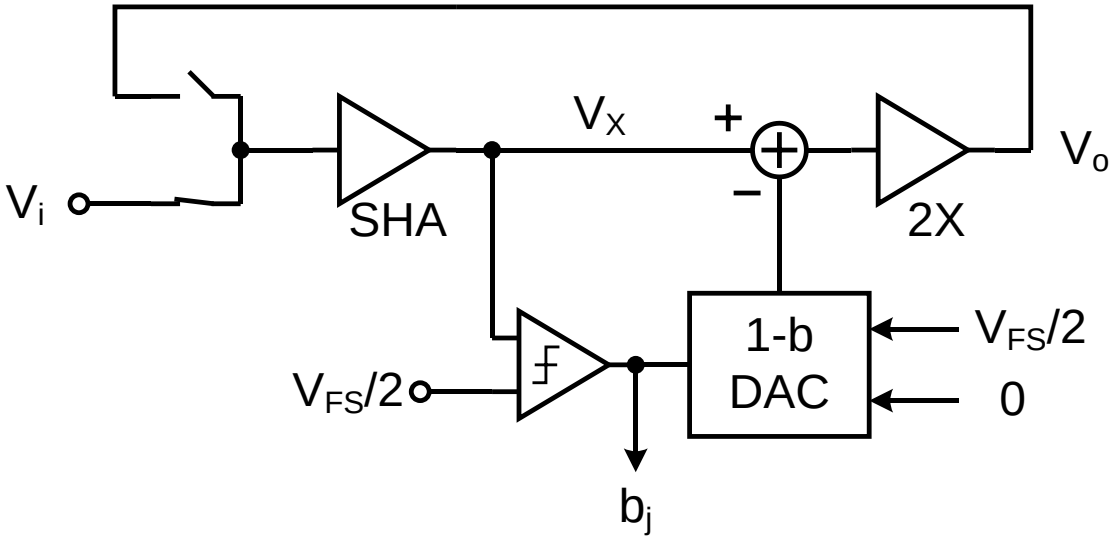
- RA gain error and non-linearity are not solved by 1.5-bit MDAC.
- More complex digital calibration techniques are required for more than 10-12 bit resolution.

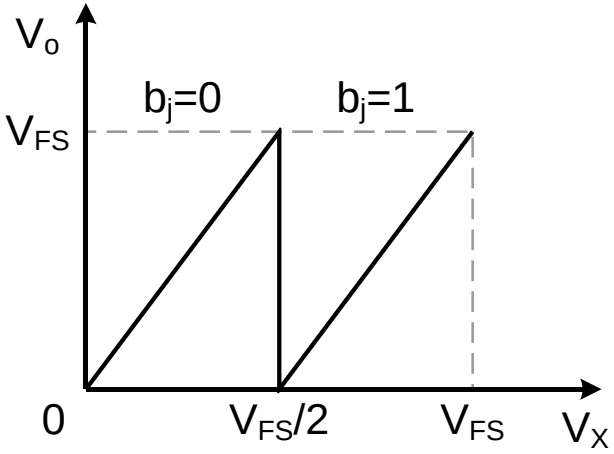


[Y. Chiu, EECT 7327, UTD]

Algorithmic (Cyclic) ADC

- Similar to pipelined, but the hardware is reused for every bit
- The signal is compared to reference to generate the MSB bit
  - Based on this bit the signal is shifted (residue is calculated) and multiplied by 2
  - This residue is fed back to the sample and hold for the next run





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Thank you!