Analog Integrated Systems Design

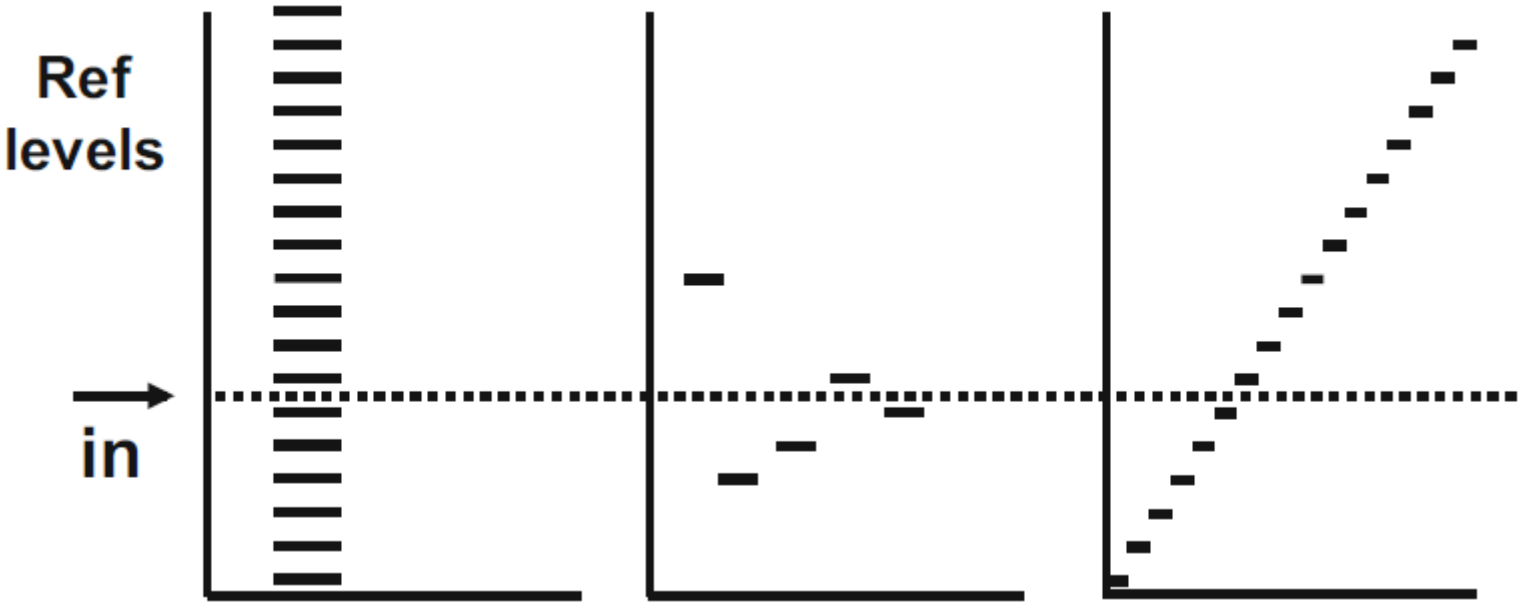
Lecture 13
Nyquist ADCs (2)

Dr. Hesham A. Omran

Integrated Circuits Laboratory (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

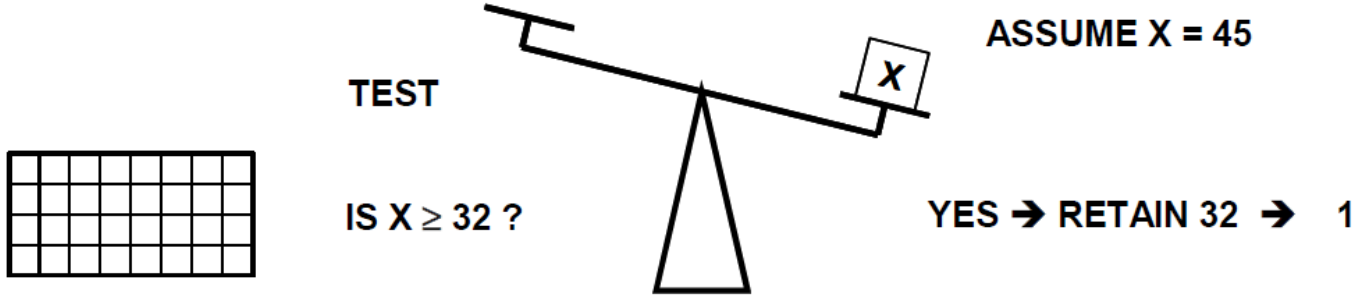
ADCs Classification

- Nyquist ADCs: signal BW close to Nyquist limit ($f_s/2$)
  1. Parallel search (e.g., flash ADC): $T_{conv} \sim T_{clk}$
  2. Sequential search (e.g., SAR ADC): $T_{conv} \sim N \times T_{clk}$
  3. Linear search (e.g., dual-slope ADC): $T_{conv} \sim 2^N \times T_{clk}$



[M. Pelgrom, 2017]

Successive Approximation Algorithm

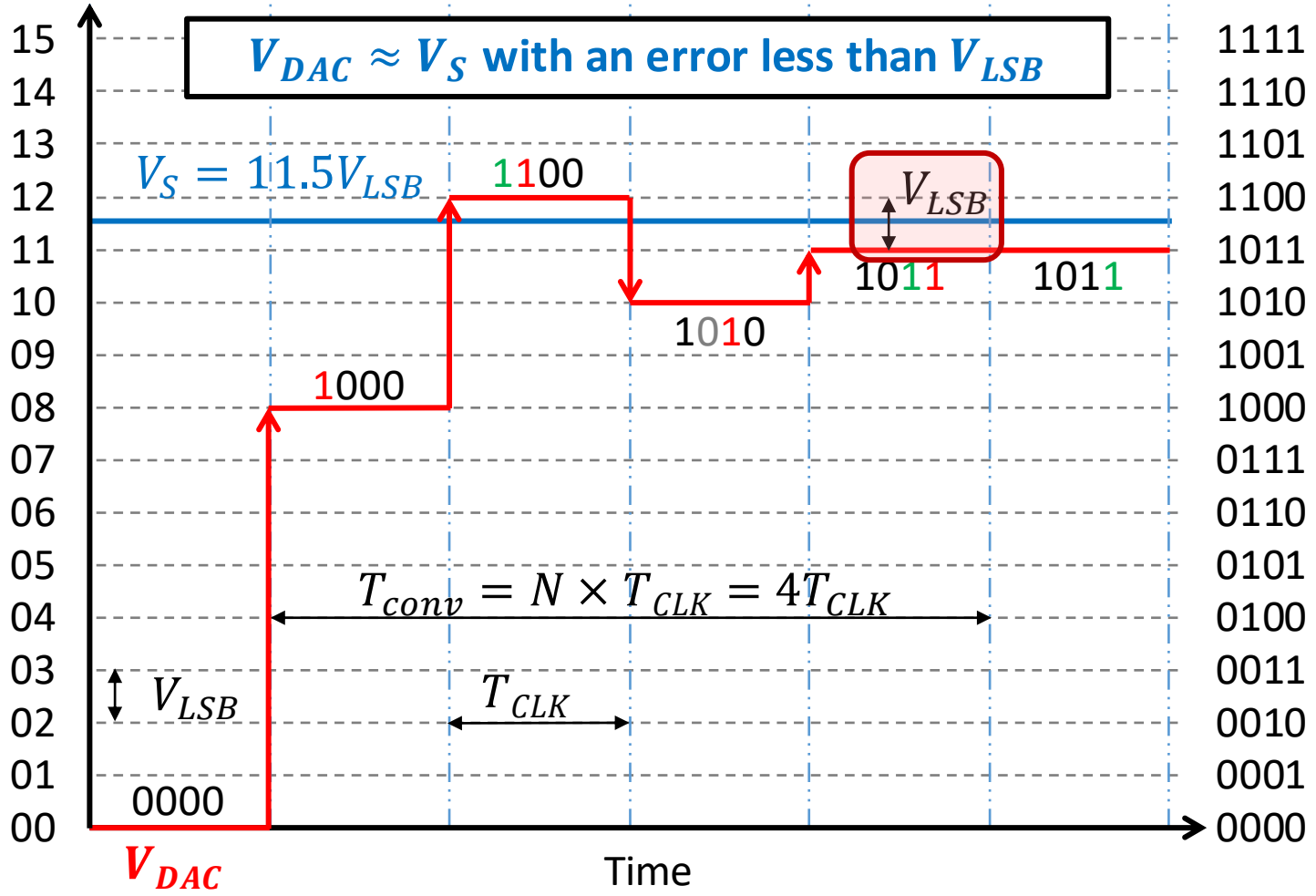


TEST	ASSUME X = 45	
IS X ≥ 32 ?	YES → RETAIN 32 →	1
IS X ≥ (32 +16) ?	NO → REJECT 16 →	0
IS X ≥ (32 +8) ?	YES → RETAIN 8 →	1
IS X ≥ (32 +8 + 4) ?	YES → RETAIN 4 →	1
IS X ≥ (32 +8 + 4 + 2) ?	NO → REJECT 2 →	0
IS X ≥ (32 +8 + 4 + 2 + 1) ?	YES → RETAIN 1 →	1

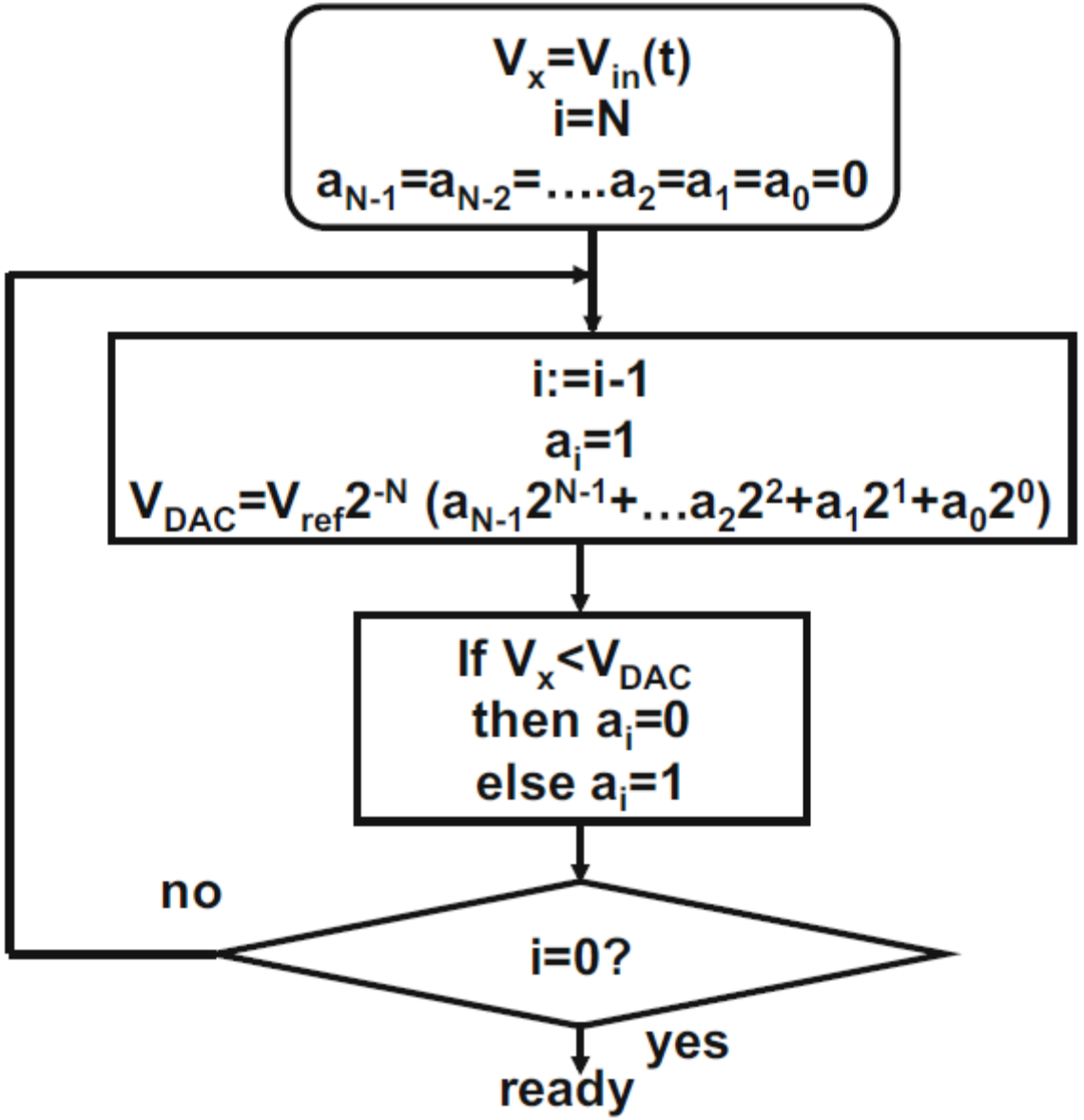
TOTALS: $X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2$

[Kester, 2005]

Successive Approximation Example



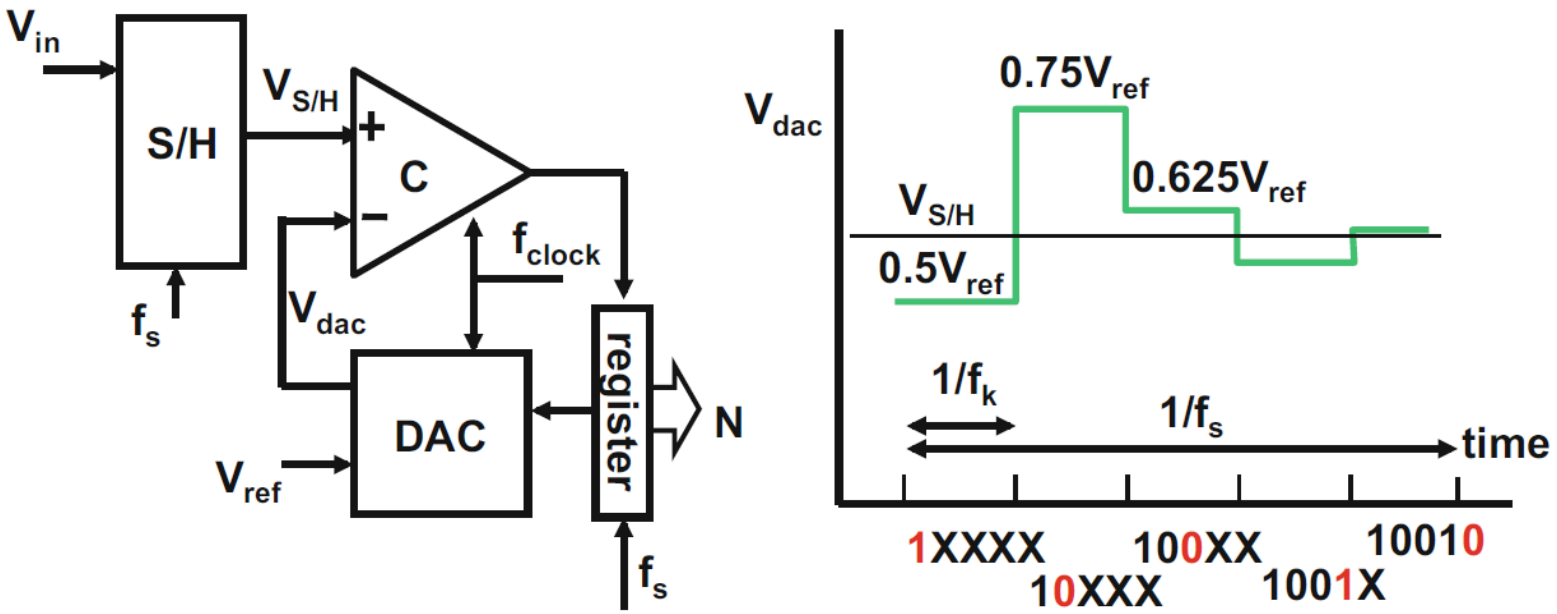
Successive Approximation Flowchart



[M. Pelgrom, 2017]

SAR ADC Example

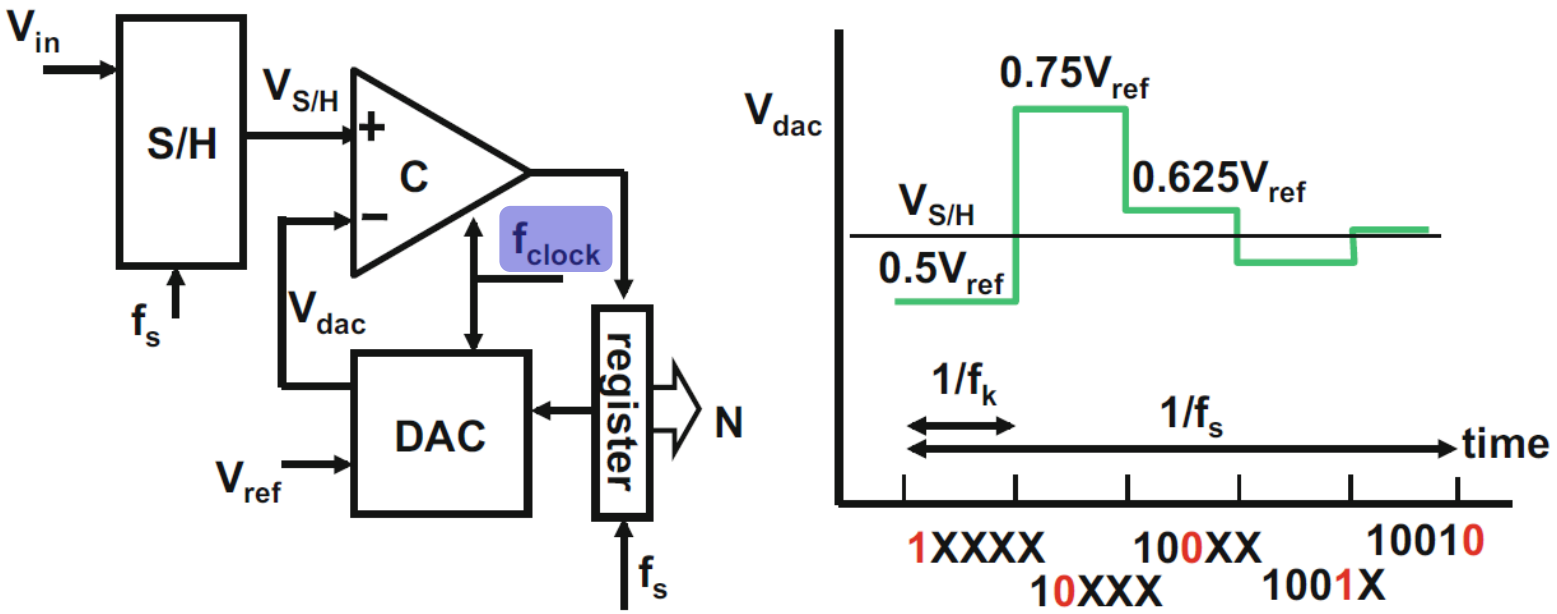
- SAR stands for successive approximation register
- Offsets in the sample-and-hold circuit or the comparator will generate a shift of the conversion range
  - But this shift is identical for every code ➔ ADC offset error (no non-linearity)
- Comparator differential input gradually approaches zero
  - Negative feedback loop action



[M. Pelgrom, 2017]

Asynchronous SAR ADC

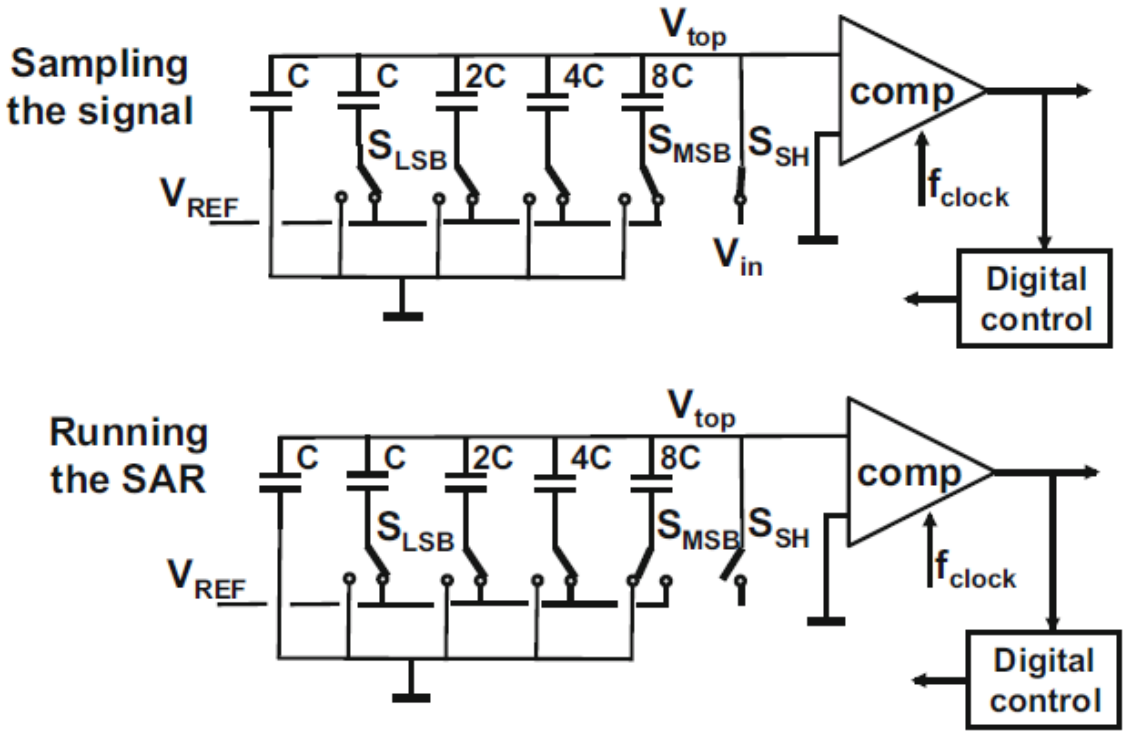
- Usually, half T_{clk} is allocated for the DAC and half for the comparison + digital logic
- The synchronous logic can be replaced by asynchronous logic
  - Event-driven: Each decision triggers next comparison
  - Self-clocked: No high speed external clock is required
  - Example: P. J. A. Harpe *et al.*, *IEEE JSSC*, July 2011.



[M. Pelgrom, 2017]

Charge-Redistribution SAR ADC

- SAR ADC can be built with any DAC architecture
  - But most attention is focused on capacitive DAC structures
    - Low-power and low-voltage operation
  - The properties of CMOS technology are optimally utilized
    - Good switches and capacitors



[M. Pelgrom, 2017]

Charge-Redistribution SAR ADC

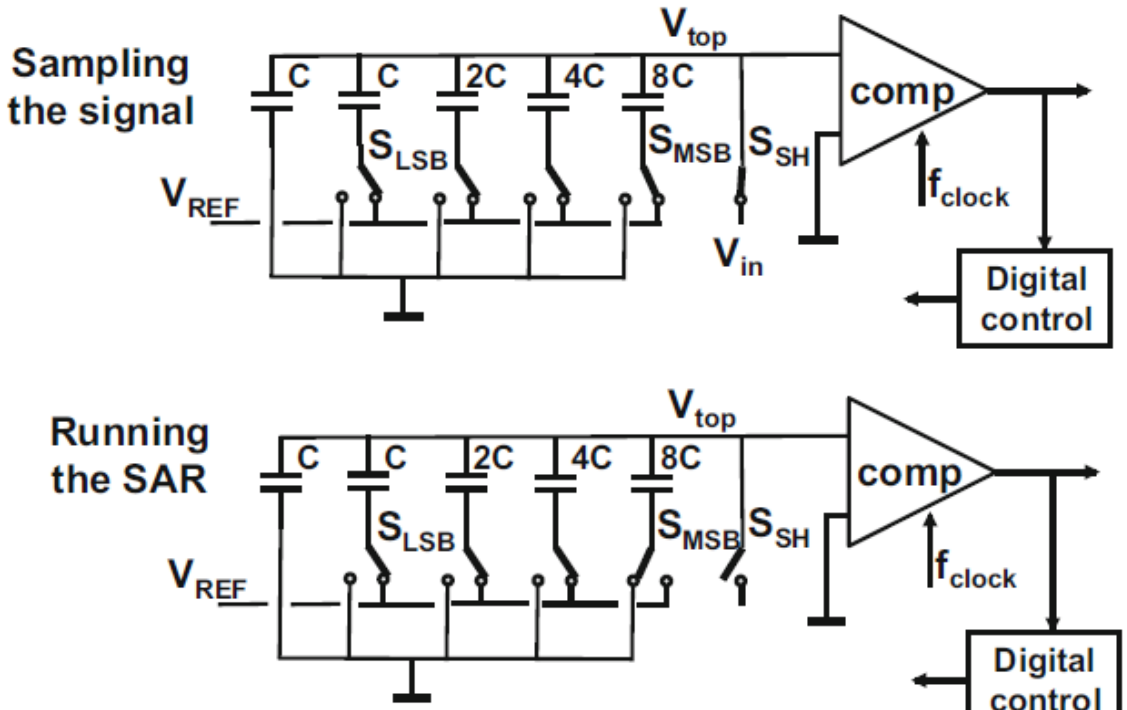
- Sampling: $Q = (C_{FS} - C)(V_{in} - V_{REF}) + CV_{in}$
- Conversion: $Q = (C_{on} + C)V_{top} + C_{off}(V_{top} - V_{REF})$

$$C_{FS}V_{in} - (C_{FS} - C)V_{REF} = C_{FS}V_{top} - C_{off}V_{REF}$$

$$V_{top} = V_{in} - \frac{C_{on}}{C_{FS}}V_{ref}$$

$$C_{FS} = 16C$$

$$C_{FS} = C_{on} + C_{off} + C$$



[M. Pelgrom, 2017]

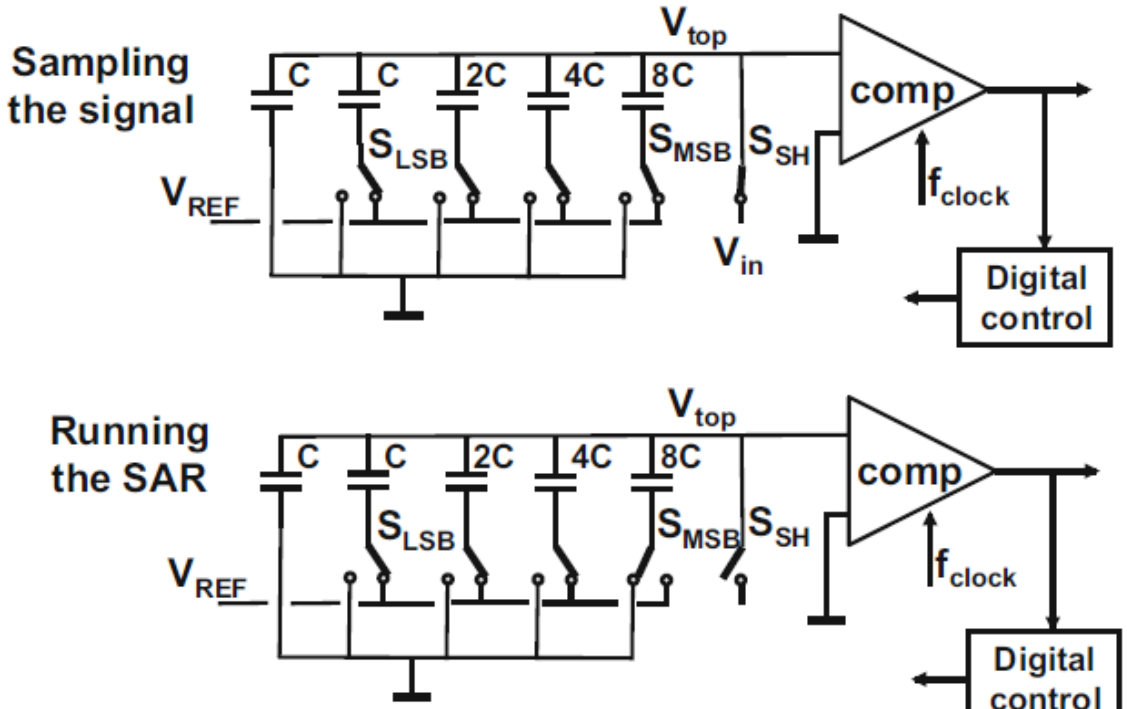
Parasitic Capacitor Effect

- The parasitic capacitor at the top plate attenuates V_{REF}
- Sampling: $Q = (C_{FS} - C)(V_{in} - V_{REF}) + (C + \boldsymbol{C_p})V_{in}$
- Conversion: $(C_{on} + C + \boldsymbol{C_p})V_{top} + C_{off}(V_{top} - V_{REF})$

$$V_{top} = V_{in} - \frac{C_{on}}{C_{FS} + C_p} V_{REF} = V_{in} - \frac{C_{on}}{C_{FS}} V'_{REF}$$

$$V'_{REF} = \frac{C_{FS}}{C_{FS} + C_p} V_{REF}$$

$$V'_{REF} < V_{REF}$$

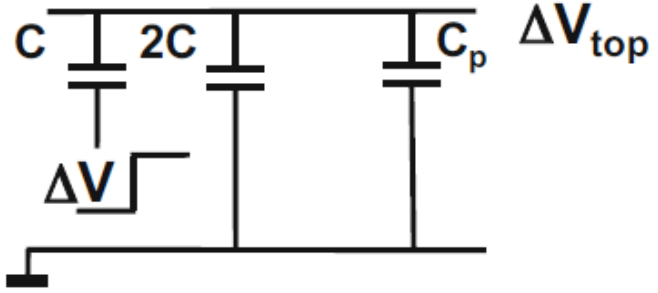


[M. Pelgrom, 2017]

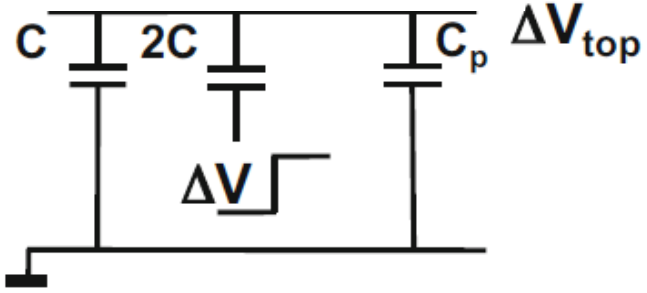
Parasitic Capacitor Effect

- The voltage step on a capacitor 2C gives exactly two times amplitude change on the top plate compared to the same step on a capacitor C
  - Irrespective of the parasitic capacitance.
  - The effect of additional capacitive load on the top plate is just attenuation.
  - But non-linear comparator input capacitance may yield a non-linear error.

$$\Delta V_{top} = \frac{C}{3C + C_p}\Delta V$$



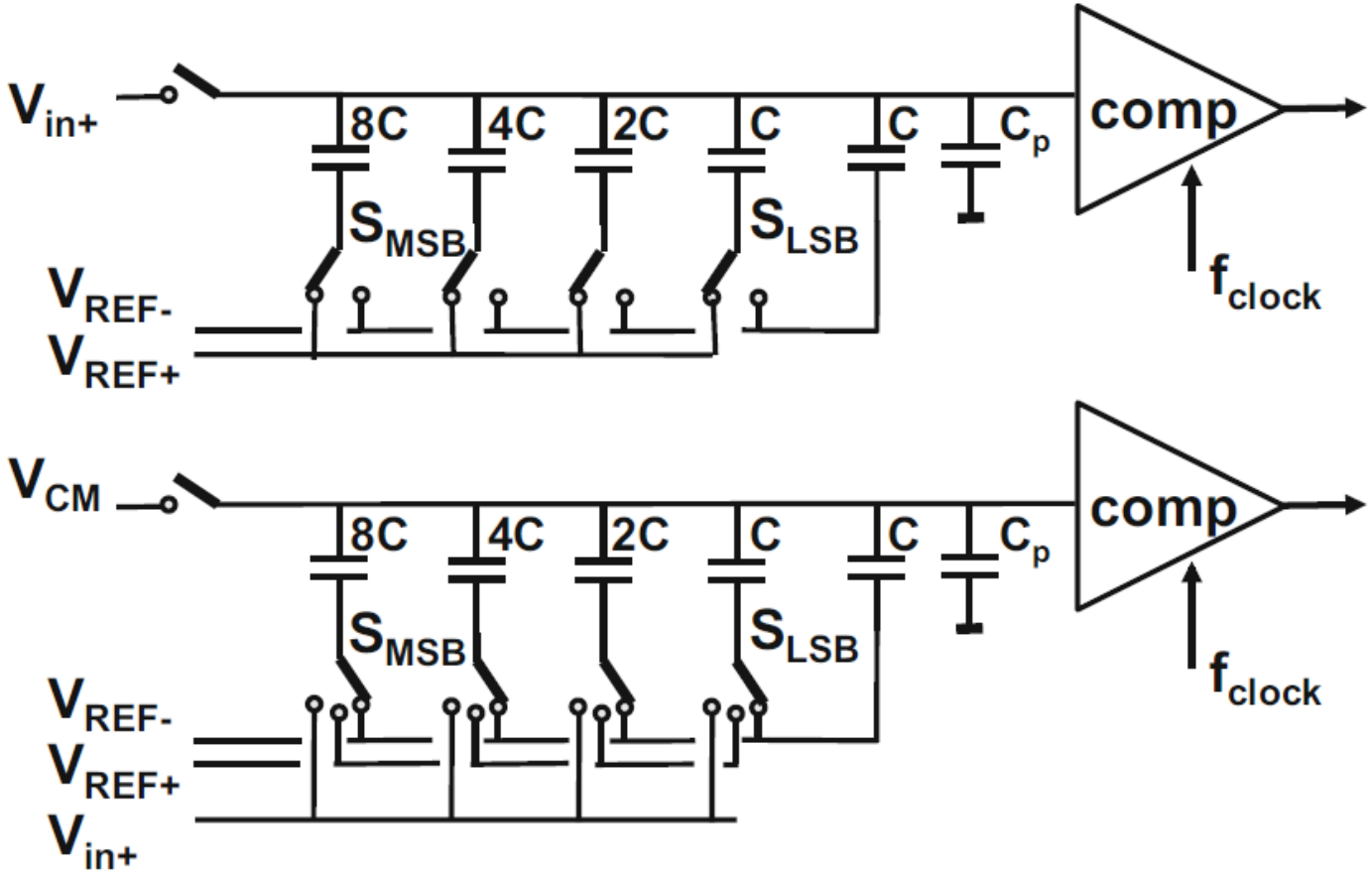
$$\Delta V_{top} = \frac{2C}{3C + C_p}\Delta V$$



[M. Pelgrom, 2017]

Top vs Bottom Plate Sampling

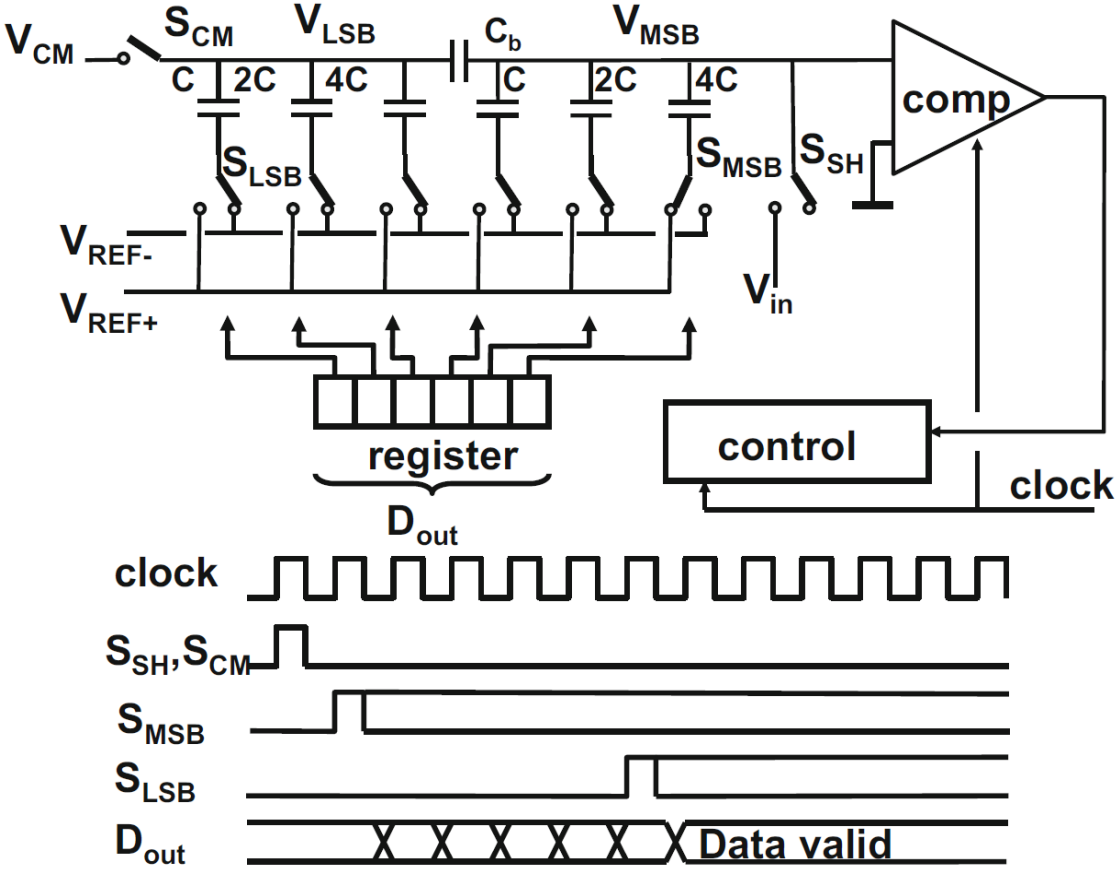
- Top: V_{in} does not utilize the full reference range because V_{REF} gets attenuated + input-dependent switching errors (distortion)
- Bottom: Same path for V_{in} and V_{REF}, but additional V_{CM} is required



[M. Pelgrom, 2017]

SAR ADC with Bridge Capacitor

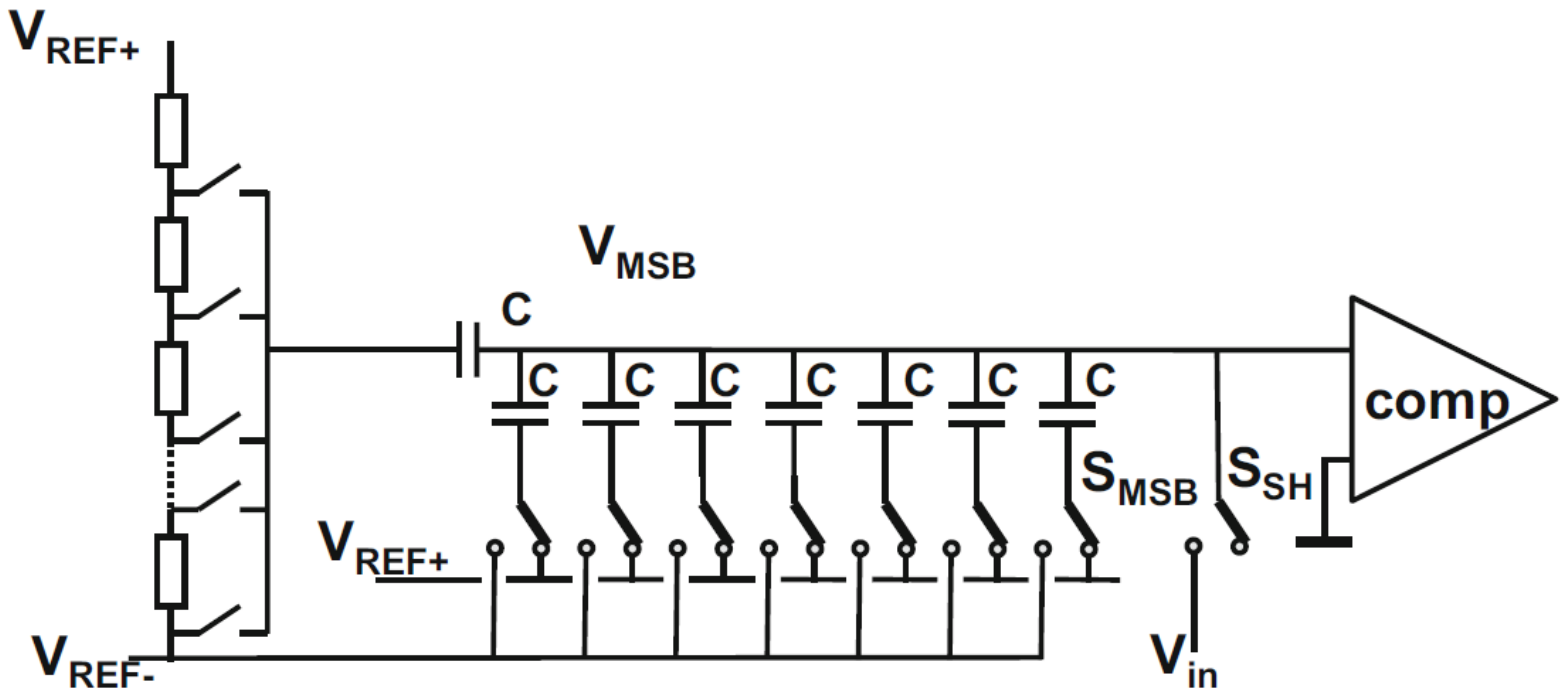
- The LSB section generates a voltage division on the left side of the bridge capacitor
  - But the top node is not a virtual ground node (compare with the DAC lecture)
  - An example of a coarse-fine structure



[M. Pelgrom, 2017]

SAR ADC with Resistor Ladder

- Better coarse-fine operation
  - But the ladder consumes static current



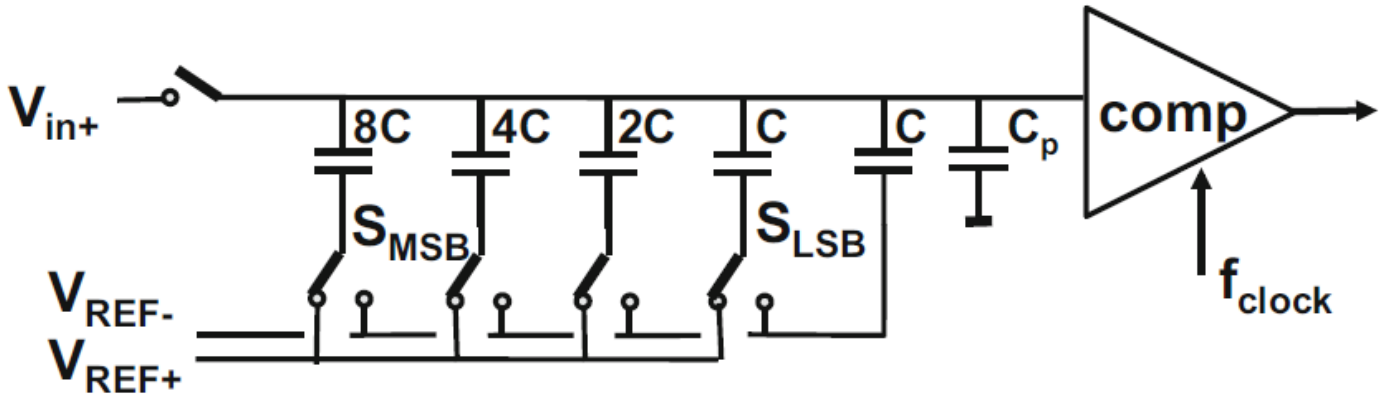
[M. Pelgrom, 2017]

SAR ADC Speed

- Capacitive DAC has to settle to 0.5 LSB accuracy

$$t_{settle} > 0.69(N+1)\tau_{DAC}$$

  - Switch resistance and output impedance of V_{REF} have to be low
  - Switches are scaled for the cap they drive to make τ of each cap nearly constant
- Comparator speed depends on topology, power consumption, and technology node

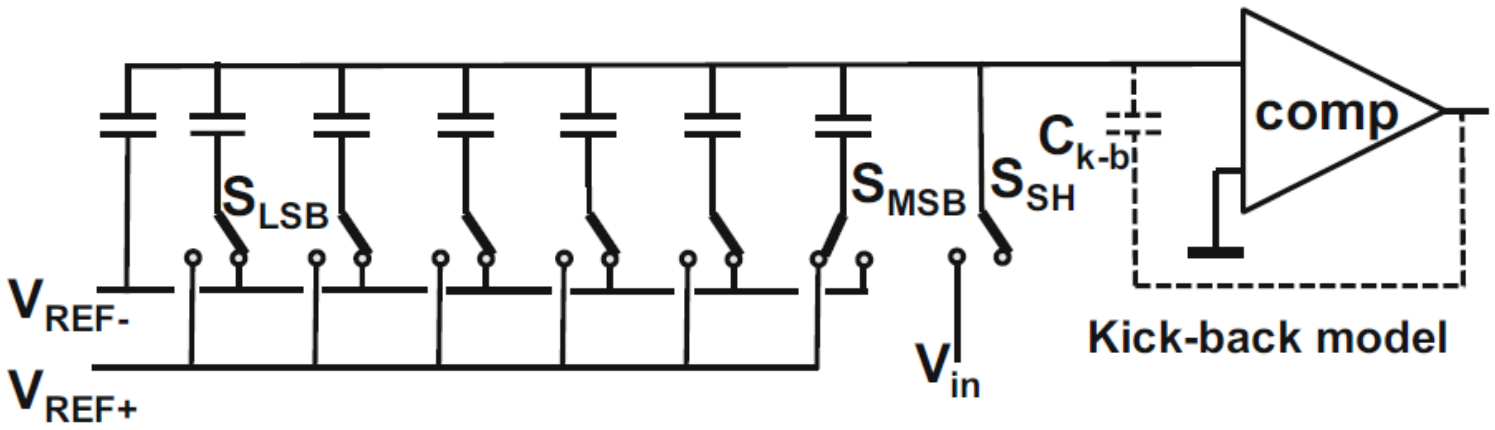


SAR ADC Error Sources

- Thermal noise of the sampling cap array: kT/C_{FS}
  - Usually small for practical values of C_{FS}
- Comparator input referred noise
  - Can be reduced by majority voting
- Sampling clock jitter SNR: $1/\left(\omega_{in}\sigma_{jitter}\right)^2$
  - High-speed clock buffers consume significant power
- Quantization error: $V_{LSB}^2/12$
- Cap array mismatch: Random ($A_p/\sqrt{Area}$) and systematic (layout) errors
- Voltage reference errors
  - A good V_{REF} circuit may consume more power than the SAR ADC!
- Comparator metastability
  - Happens at most once during each conversion
- Kickback noise (next slide)

Kickback Noise

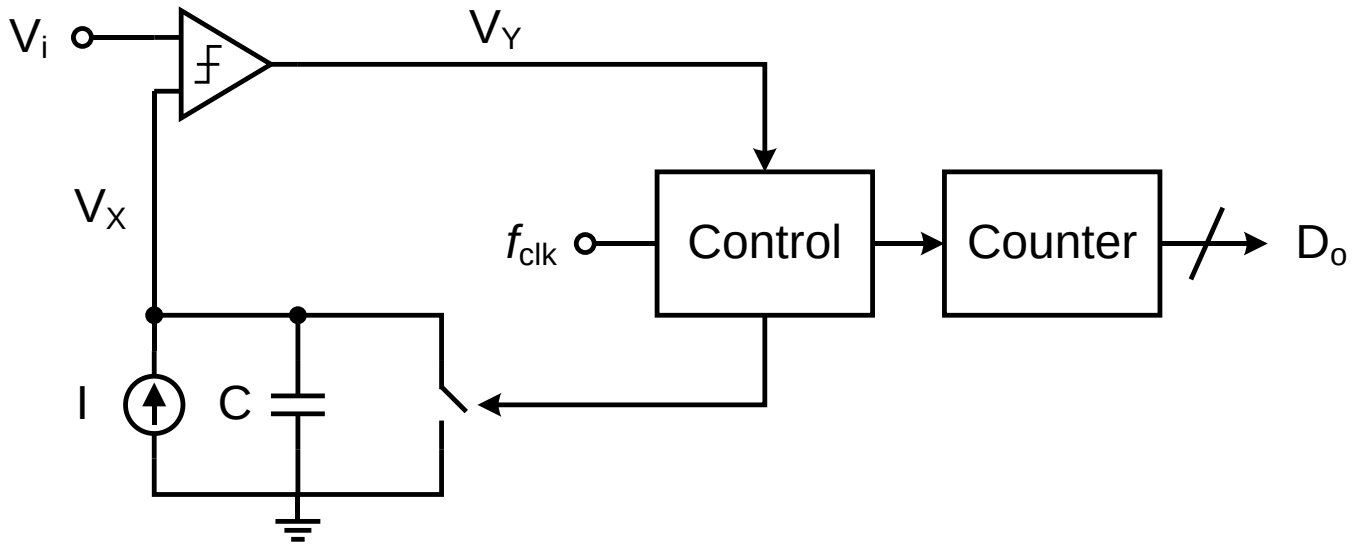
- Fixed comparator offsets in the SAR ADC show up as a tolerable signal offset that do not affect linearity
- But the use of dynamic comparators leads to strong kick-back
- The comparator decision will induce charge on the top plate that can affect the decision that is being processed or the next decision
  - Many designers avoid simple comparators (e.g., StrongArm)
    - Robust designs use preamplifiers
- In differential designs common-mode kick-back is cancelled



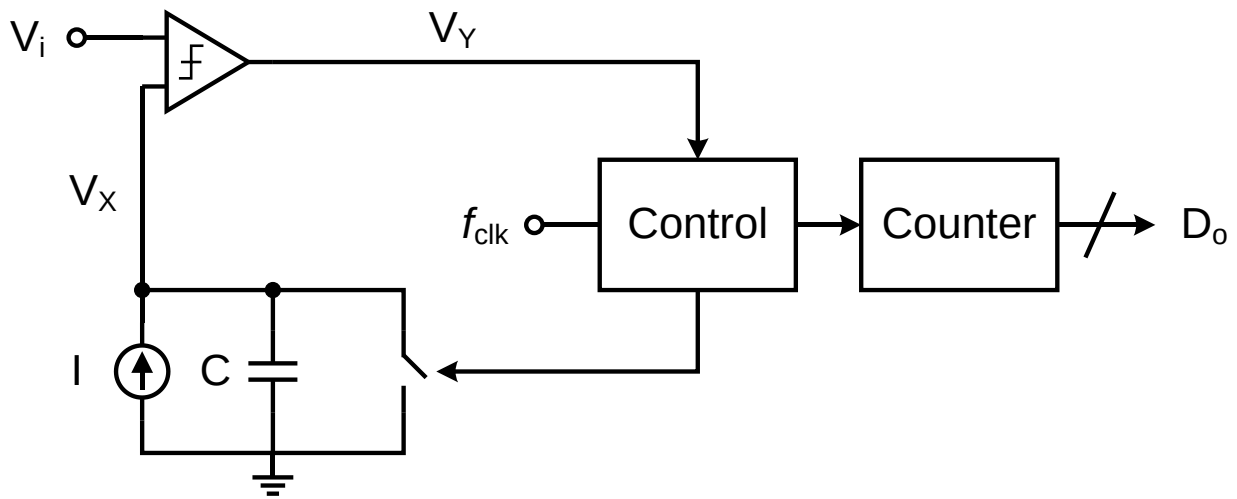
[M. Pelgrom, 2017]

Single-Slope Integrating / Counting ADC

- Sampled-and-held input (Vi), linear search for output
- Counter keeps counting until comparator output toggles
  - Ramp signal generated by charging/discharging a capacitor with a constant current
    - Ramp linearity determines INL
- Simple, inherently monotonic, but very slow: $T_{conv} \sim 2^N \times T_{clk}$



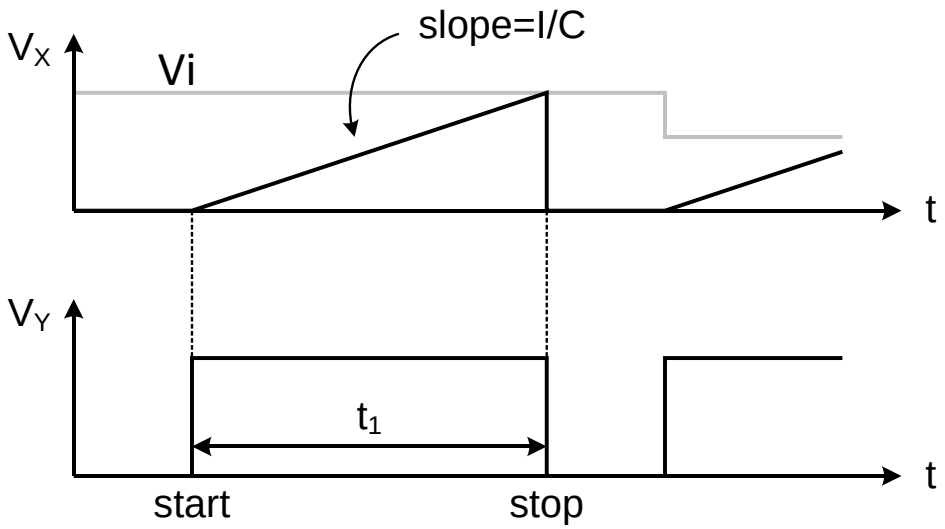
Single-Slope Integrating / Counting ADC



$$V_i = \frac{I}{C} \cdot t_1, \; D_o = \left\lfloor \frac{t_1}{T_{clk}} \right\rfloor$$

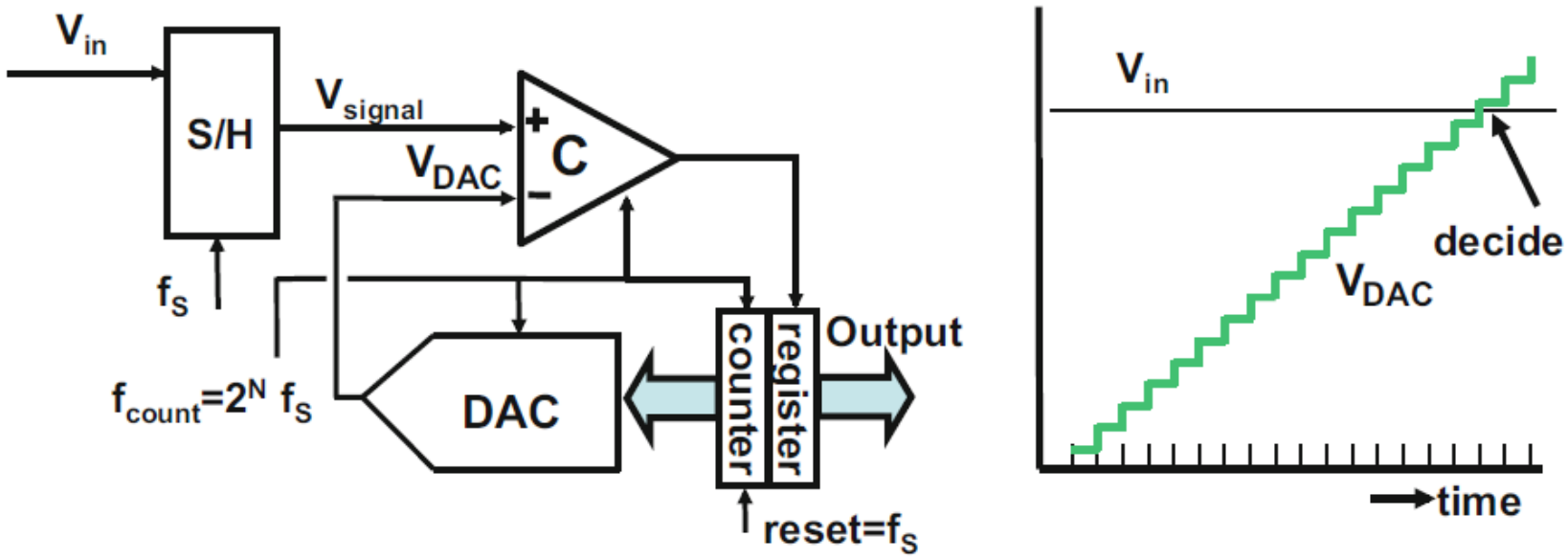
$$\Rightarrow D_o = \left\lfloor \frac{V_i}{\left(\frac{I \cdot T_{clk}}{C} \right)} \right\rfloor,$$

$$LSB = \frac{I \cdot T_{clk}}{C}$$



Single-Slope Integrating / Counting ADC

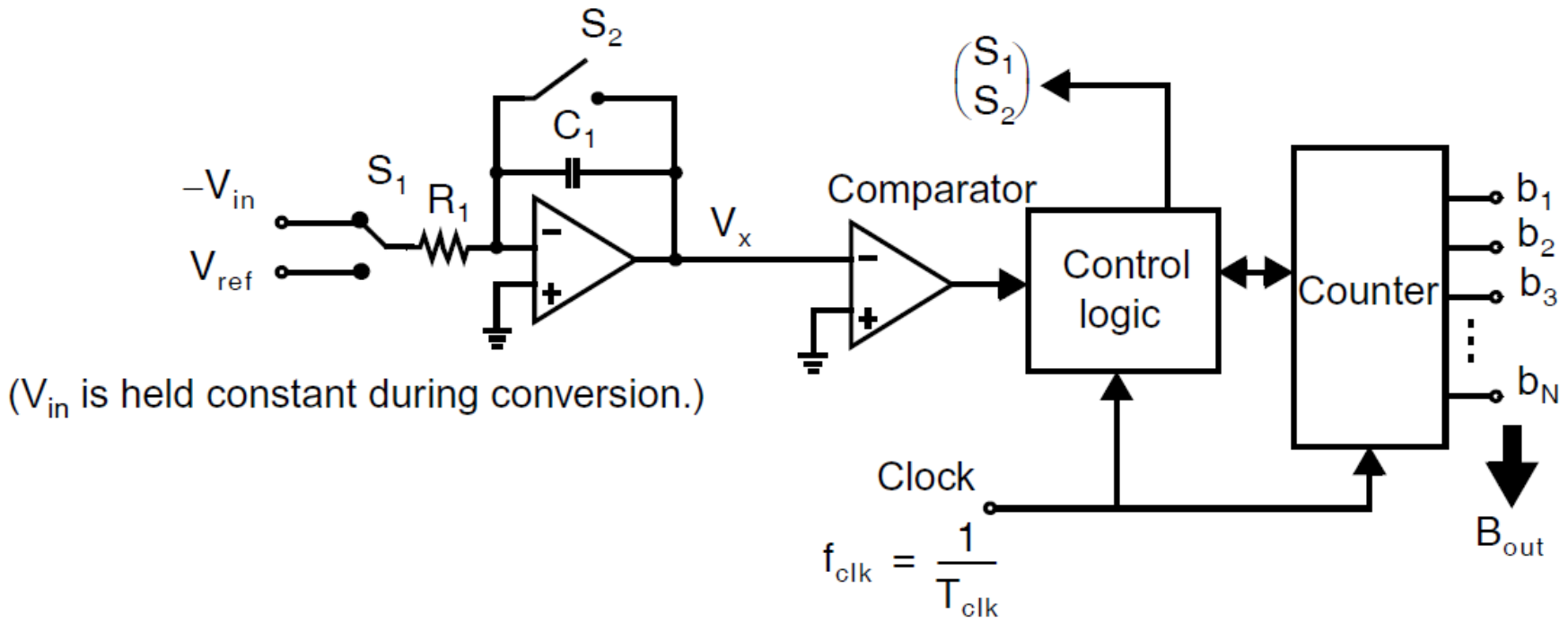
- For analog ramp
  - Need precision capacitor (C), current source (I), and clock (T_{clk})
- The ramp can be digitally generated using a DAC
  - Need precision DAC: DNL and INL depend on DAC ccs



[M. Pelgrom, 2017]

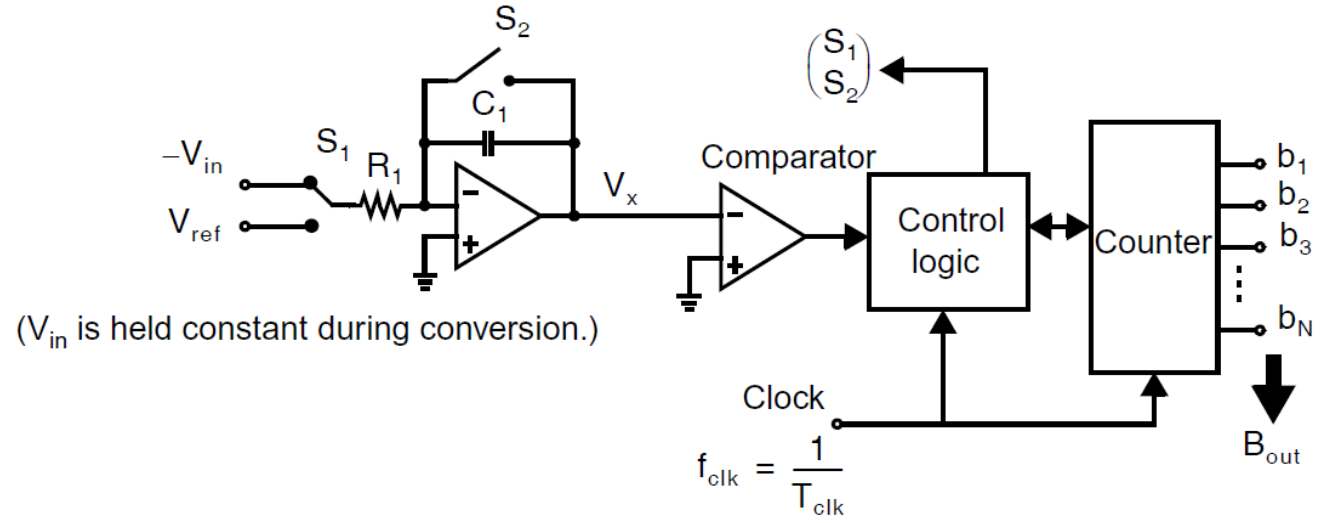
Dual-Slope Integrating ADC

- Op-amp converts V to I
  - Constant current is charging/discharging feedback capacitor
- Popular in multimeters and harsh industrial environments



[Johns & Martin, 2012]

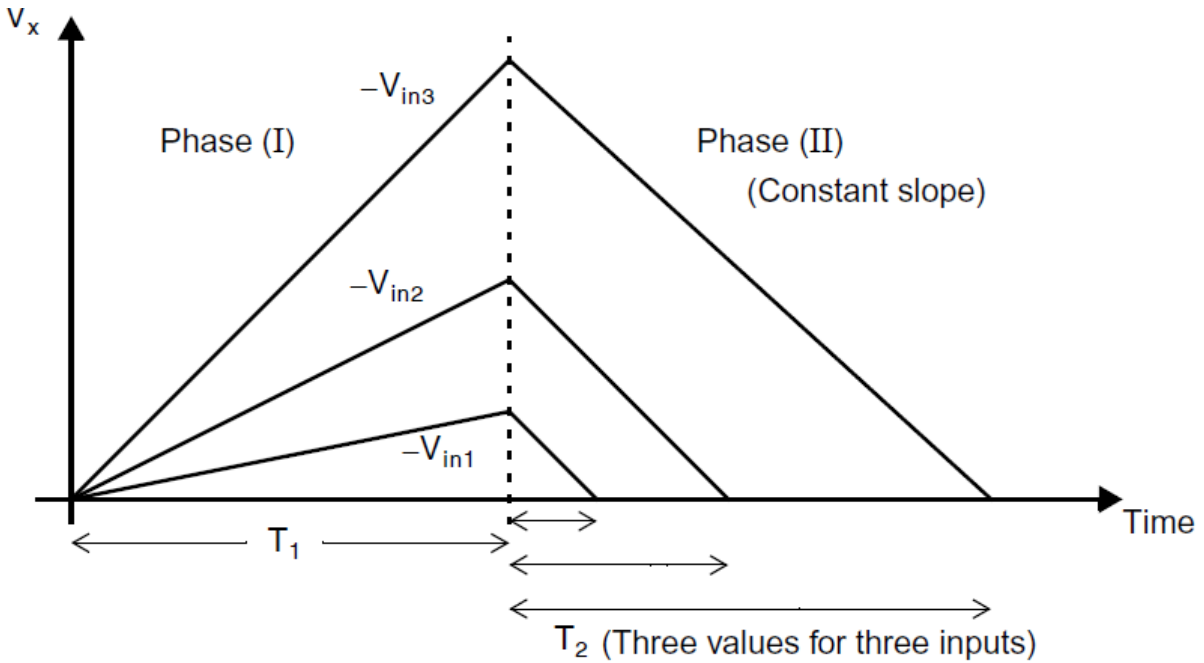
Dual-Slope ADC



$$V_m = \frac{V_i}{RC} \cdot t_1 = \frac{V_R}{RC} \cdot t_2$$

$$\Rightarrow \quad D_o = \left|\frac{V_i}{V_R}\right| = \left|\frac{t_2}{t_1}\right| = \frac{N_2}{N_1}$$

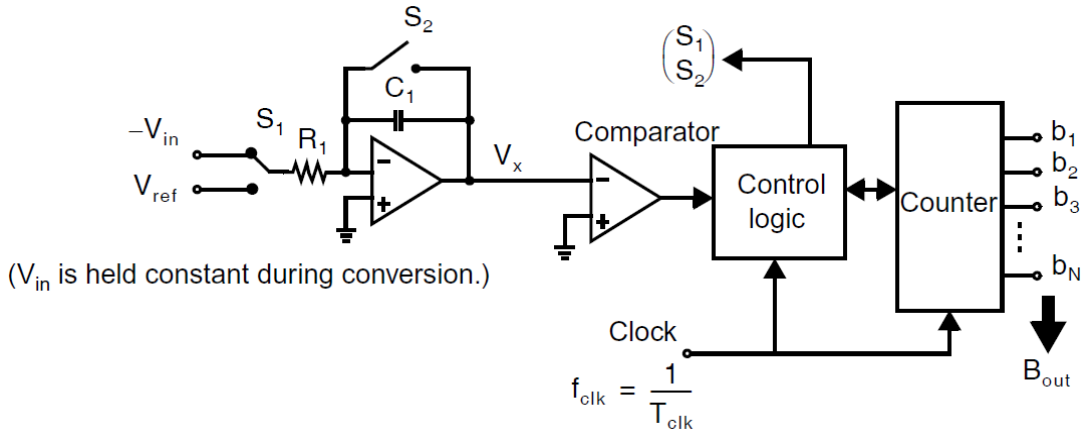
$$or \quad D_o = N_2 \ \ for\ fixed \ \ N_1$$



[Johns & Martin, 2012]

Dual-Slope ADC

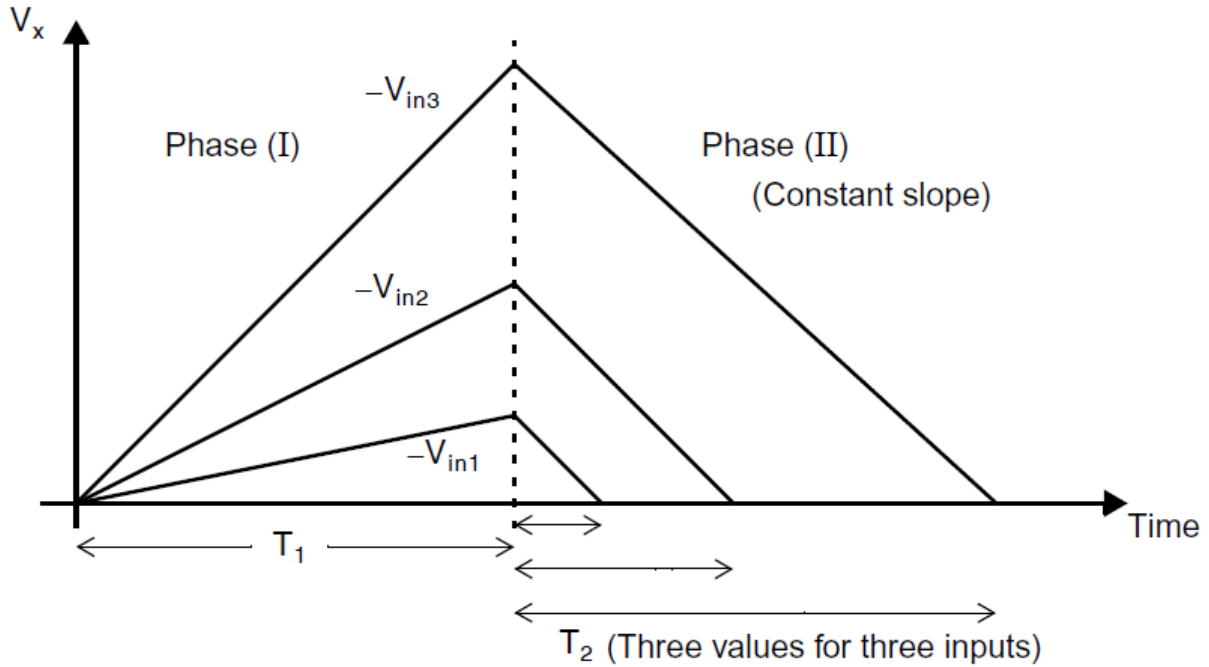
- Exact values of R, C, and T_{clk} are not required
- Comparator offset doesn't matter
- Op-amp offset introduces gain and offset error
- Op-amp nonlinearity introduces INL error



$$V_m = \frac{V_i}{RC} \cdot t_1 = \frac{V_R}{RC} \cdot t_2$$

$$\Rightarrow \quad D_o = \left|\frac{V_i}{V_R}\right| = \left|\frac{t_2}{t_1}\right| = \frac{N_2}{N_1}$$

$$or \quad D_o = N_2 \ \ for \ fixed \ \ N_1$$



[Johns & Martin, 2012]

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed, 2017.
- W. Kester, The Data Conversion Handbook, ADI, Newnes, 2005.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” Wiley, 2nd ed., 2012.
- B. Boser and H. Khorramabadi, EECS 247 (previously EECS 240), Berkeley.
- B. Murmann, EE 315, Stanford.
- Y. Chiu, EECT 7327, UTD.
- F. Maloberti, Data Converters, Springer, 2007.
- Low-Power SAR ADCs by Pieter Harpe: https://youtu.be/BE9onmrGZhY

Thank you!