Analog Integrated Systems Design

Lecture 15
Oversampling Data Converters (2)

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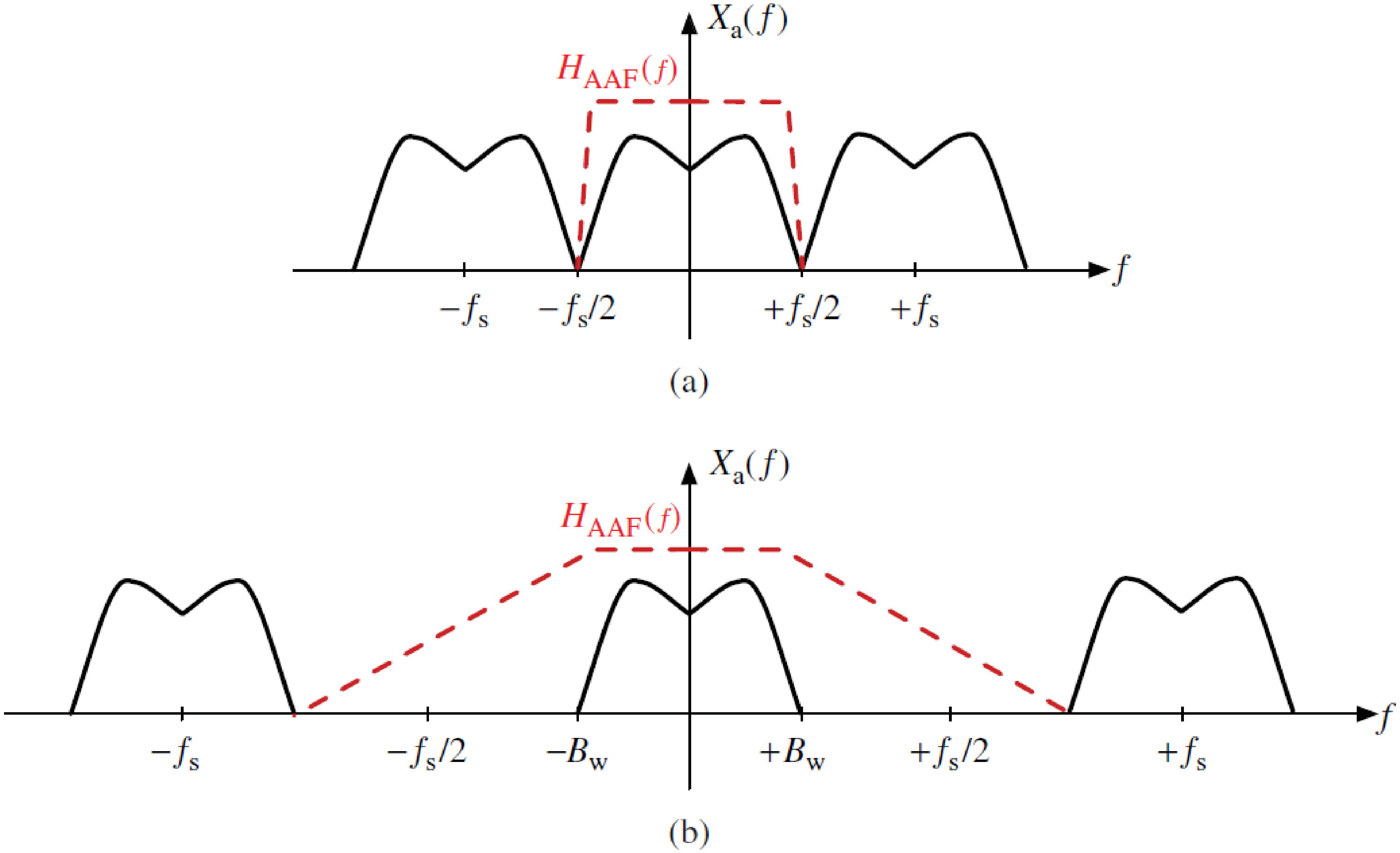
Why Oversampling?

- Technology scaling enable very fast MOS transistors
  - GHz sampling and processing is possible
  - We can build faster ADCs for broadband signals
- But signals in many applications have limited bandwidth
  - Ex: sensors (baseband) and communication systems (passband)
- Oversampling: $f_s \gg f_N = 2BW$
  - Make use of the high sample rate to improve the resolution
    - Oversampling Ratio (OSR)

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2BW}$$

  - Also simpler antialiasing filter
  - But higher digital power consumption

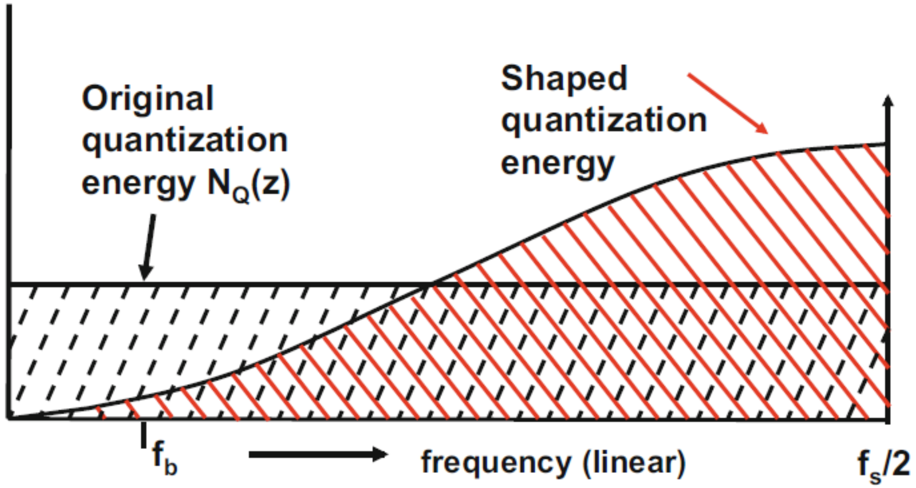
Nyquist vs Oversampling ADC



[J. M. de la Rosa and R. del Rio, 2013]

Noise Shaping

- ❑ Noise transfer function (NTF) is a HPF (differentiator)

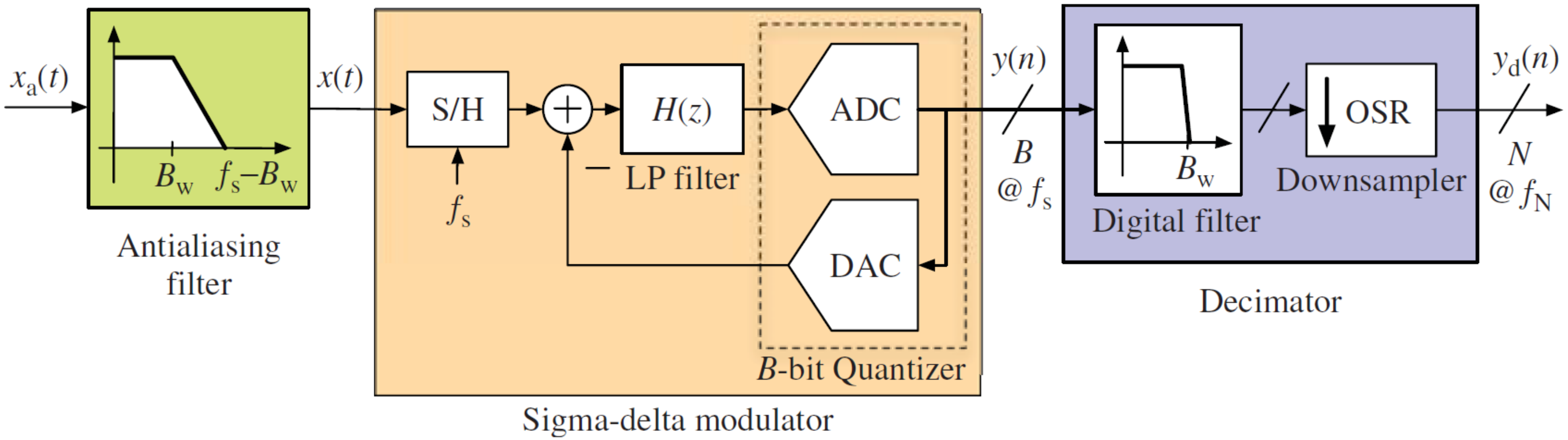


- ❑ For 1st order NTF: The shaped noise has twice the noise power
  - But IBN is significantly reduced

[M. Pelgrom, 2017]

Sigma-Delta (ΣΔ) ADC

- Closed loop negative feedback system
- $H(z)$ is the loop filter
- The B-bit quantizer is typically $1 - 5$ bit
  - Single bit: One bit DAC is inherently linear
    - We care more about DAC linearity (we will know why later)
  - Multibit: Each bit in the ADC/DAC adds 6dB to the SNR



[J. M. de la Rosa and R. del Rio, 2013]

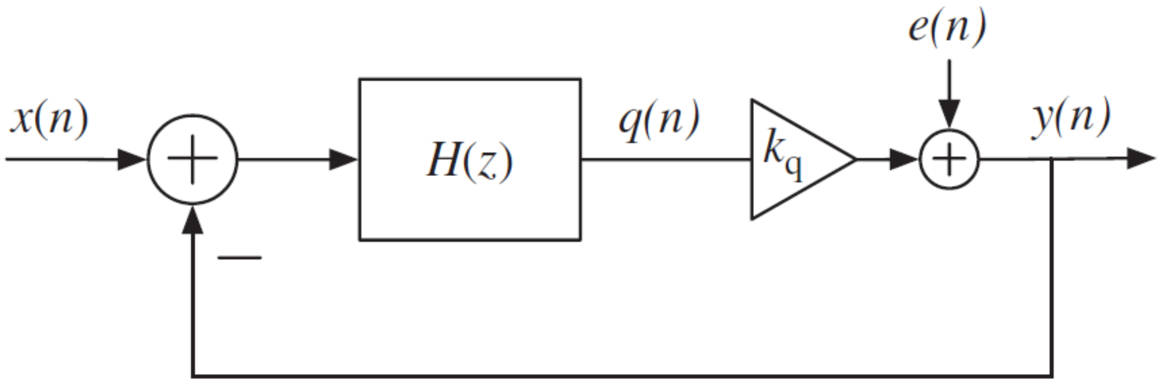
First-Order ΣΔM

Let $H(z) = \frac{z^{-1}}{1-z^{-1}}$ and $k_q = 1$

$$STF(z) = \frac{H(z)}{1+H(z)} = z^{-1} \quad \rightarrow \quad \text{Delay}$$

$$NTF(z) = \frac{1}{1+H(z)} = 1 - z^{-1} \quad \rightarrow \quad \text{Noise shaping}$$

$$Y = STF \cdot X + NTF \cdot E = z^{-1} \cdot X + (1 - z^{-1}) \cdot E$$



[J. M. de la Rosa and R. del Rio, 2013]

Higher-Order ΣΔM

Let $H(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right)^L$ and $k_q = 1$

$$STF(z) = \frac{H(z)}{1+H(z)} = z^{-L}$$ ➔ Delay

$$NTF(z) = \frac{1}{1+H(z)} = (1 - z^{-1})^L$$ ➔ Noise shaping

$$Y = STF \cdot X + NTF \cdot E = z^{-L} \cdot X + (1 - z^{-1})^L \cdot E$$

$$SQNR = 10 \log\left(\frac{P_{sig}}{IBN}\right)$$

$$\approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2\boldsymbol{L}+1}{\boldsymbol{\pi}^{2\boldsymbol{L}}}\right)} + \mathbf{(2\boldsymbol{L}+1)10\log(\boldsymbol{OSR})}$$

Noise Shaping Gain

$$SQNR \approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2L+1}{\pi^{2L}}\right)} + \mathbf{(2L+1)10\log(OSR)}$$

$$ENOB\ Gain = \frac{\mathbf{(2L+1)10\log(OSR)}}{6} \approx \mathbf{(2L+1)} \times 0.5\log_2(OSR)$$

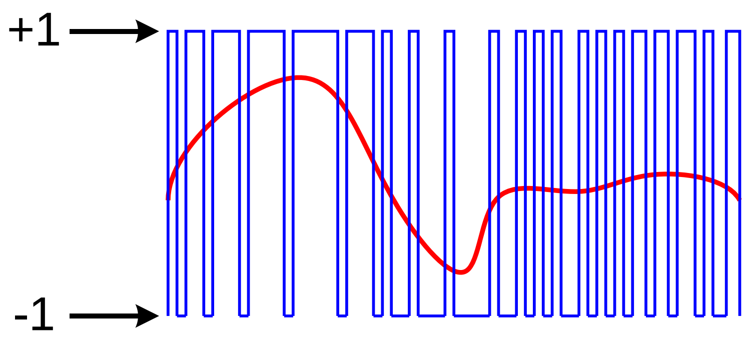
- SNQR increases with OSR by $3(2L+1)$ dB/octave
- ENOB increases with OSR by $(L+0.5)$ bit/octave
- Need OSR > 4 (more than two octaves) to reap **ΣΔM** benefits

Order (L)	Static SNR loss	SNR gain	Static ENOB loss	ENOB gain
0	0	3 dB/octave	0	0.5 bit/octave
1	-5.2 dB	9 dB/octave	-0.86 bit	1.5 bit/octave
2	-12.9 dB	15 dB/octave	-2.14 bit	2.5 bit/octave
3	-21.4 dB	21 dB/octave	-3.55 bit	3.5 bit/octave
4	-30.2 dB	27 dB/octave	-5.02 bit	4.5 bit/octave

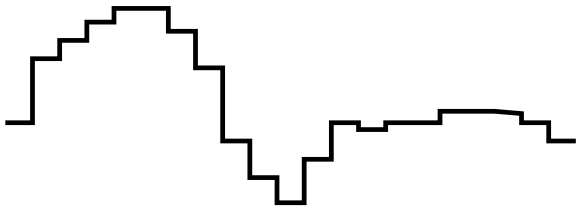
ΣΔ vs Nyquist ADC

- ΣΔ ADC behaves quite differently from Nyquist converters
- Digital codes only display an “average” impression of the input
- INL, DNL, monotonicity, missing code, etc. do not directly apply in ΣΔ converters
- Usually only dynamic ccs are important (SNR, SNDR, SFDR, etc.)

ΣΔ ADC output (1-bit)



Nyquist ADC output



$\boldsymbol{\Sigma\Delta M}$s Classification

- Single-Bit vs Multibit $\boldsymbol{\Sigma\Delta M}$s
- First-order vs Higher-order $\boldsymbol{\Sigma\Delta M}$s
  - Order of the loop filter
- Single-Loop vs Cascade or MASH $\boldsymbol{\Sigma\Delta M}$s
  - Single-loop: uses only one quantizer
  - Cascade or MASH: uses several quantizers

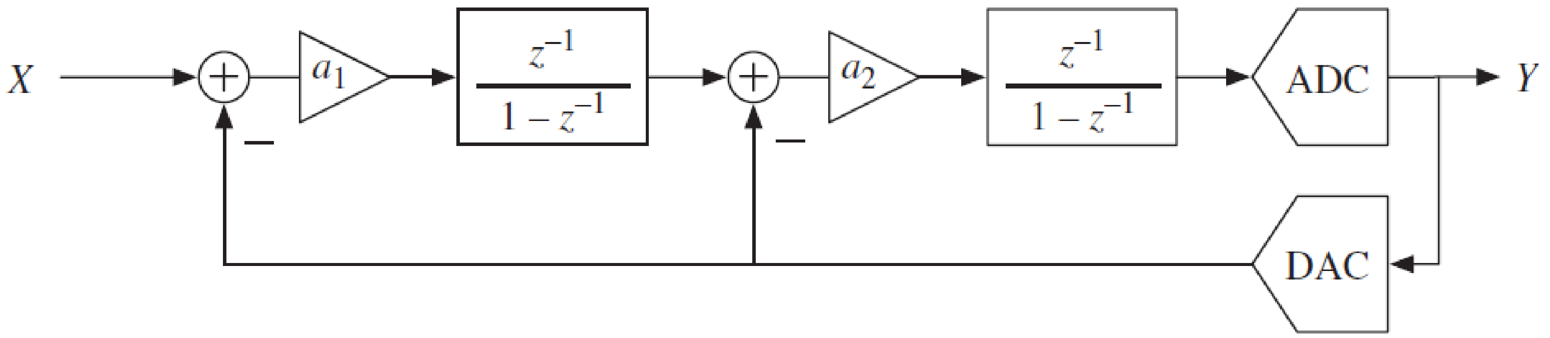
Second-order ΣΔM

- Two DT integrators are cascaded
  - Each integrator receives a weighted feedback path

$$Y(z)=\frac{k_q a_1 a_2 \frac{z^{-2}}{(1-z^{-1})^2}X(z)+E(z)}{1+k_q a_1 a_2 \frac{z^{-2}}{(1-z^{-1})^2}+k_q a_2 \frac{z^{-1}}{(1-z^{-1})}}$$

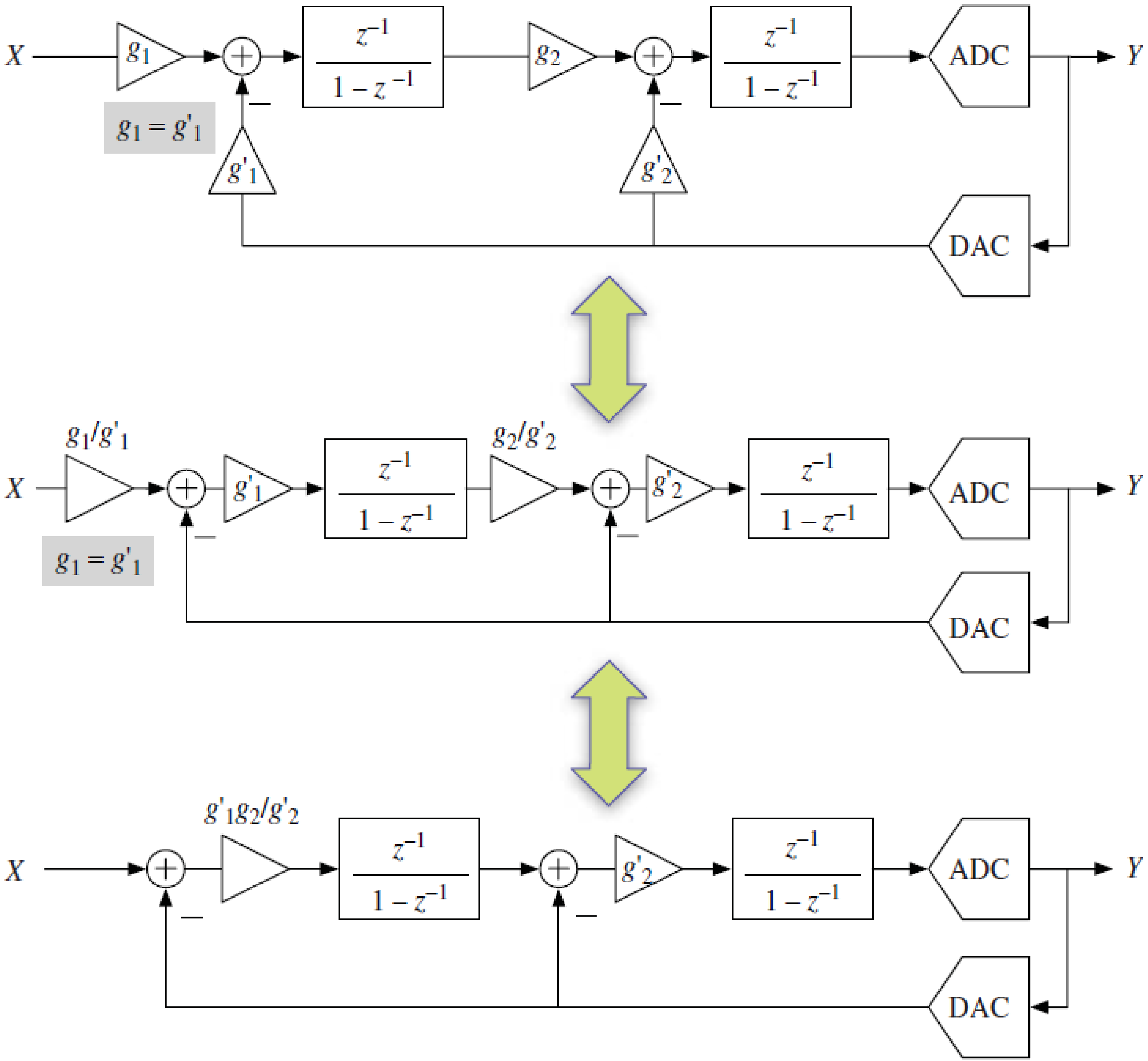
$$Y(z)=z^{-2}X(z)+(1-z^{-1})^2E(z)$$

$$k_q a_1 a_2 = 1$$
$$k_q a_2 = 2$$



[J. M. de la Rosa and R. del Rio, 2013]

Second-order ΣΔM



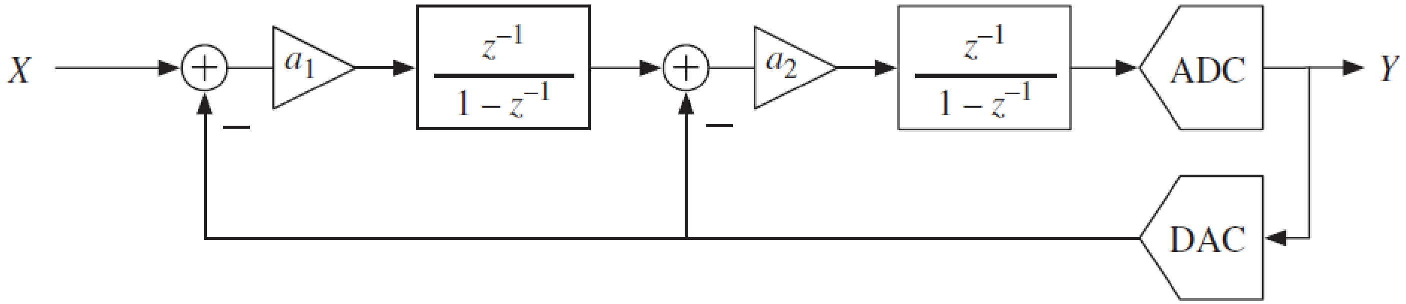
$$a_1 = \frac{g_1' g_2}{g_2'}$$
$$a_2 = g_2'$$

[J. M. de la Rosa and R. del Rio, 2013]

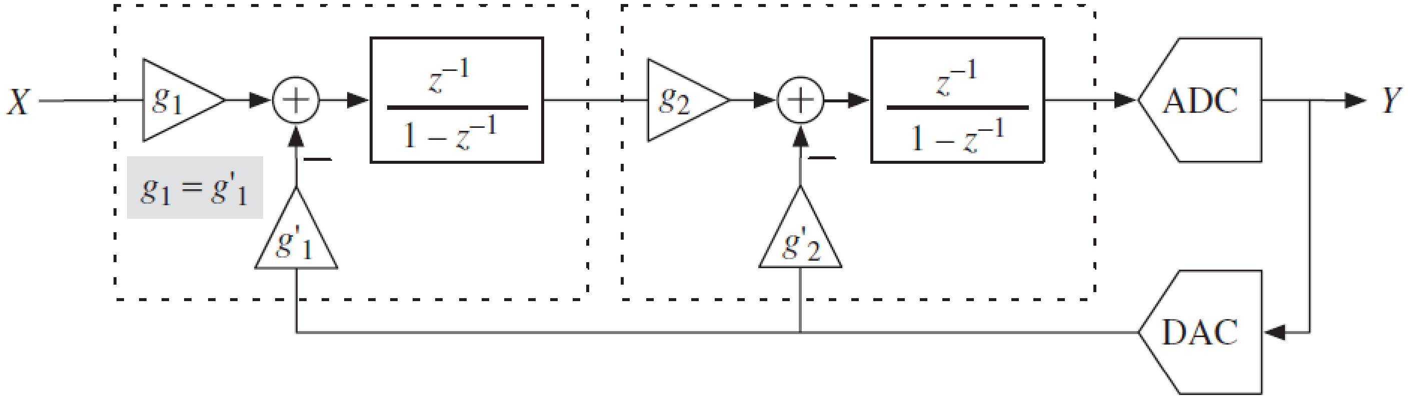
Second-order ΣΔM

- Two alternative representations are possible
  - (a) suits system level
  - (b) suits circuit level

$$a_1 = \frac{g'_1 g_2}{g'_2}$$
$$a_2 = g'_2$$



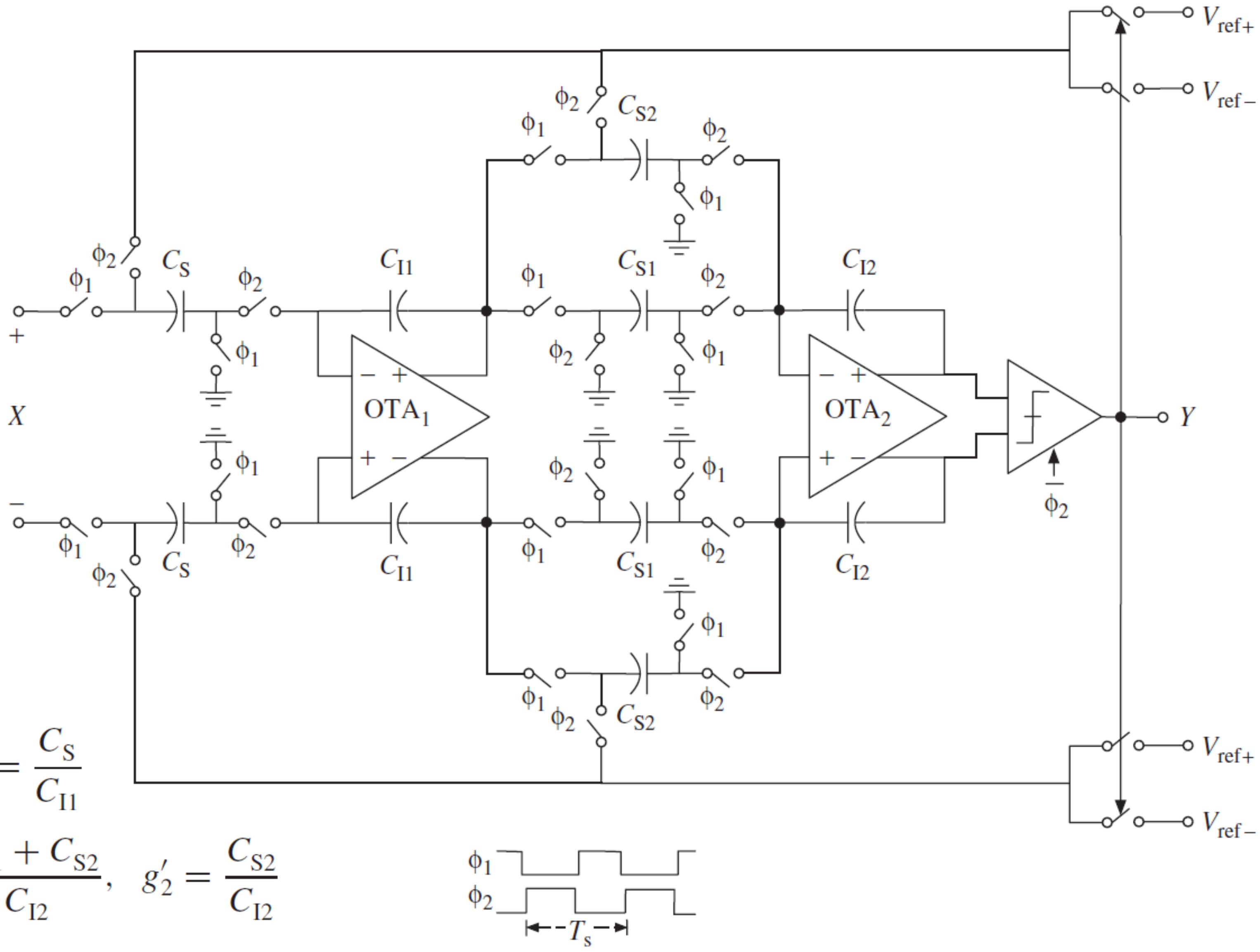
(a)



(b)

[J. M. de la Rosa and R. del Rio, 2013]

Second-order $\Sigma\Delta\mathbf{M}$: SC Implementation

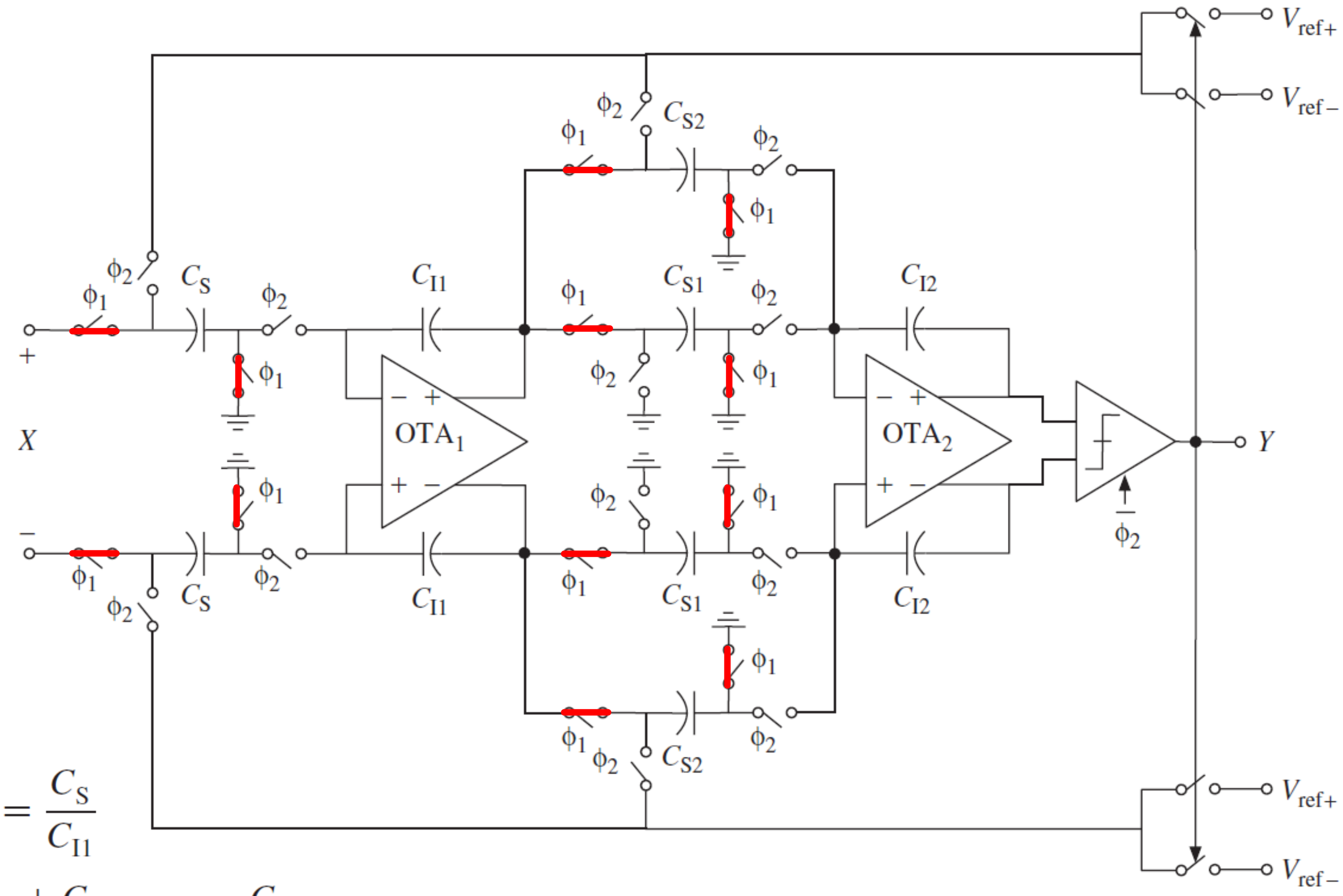


$$g_1 = g_1' = \frac{C_S}{C_{I1}}$$

$$g_2 = \frac{C_{S1} + C_{S2}}{C_{I2}}, \quad g_2' = \frac{C_{S2}}{C_{I2}}$$

[J. M. de la Rosa and R. del Rio, 2013]

Second-order $\Sigma\Delta\mathbf{M}$: SC Implementation



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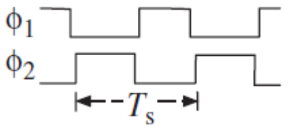
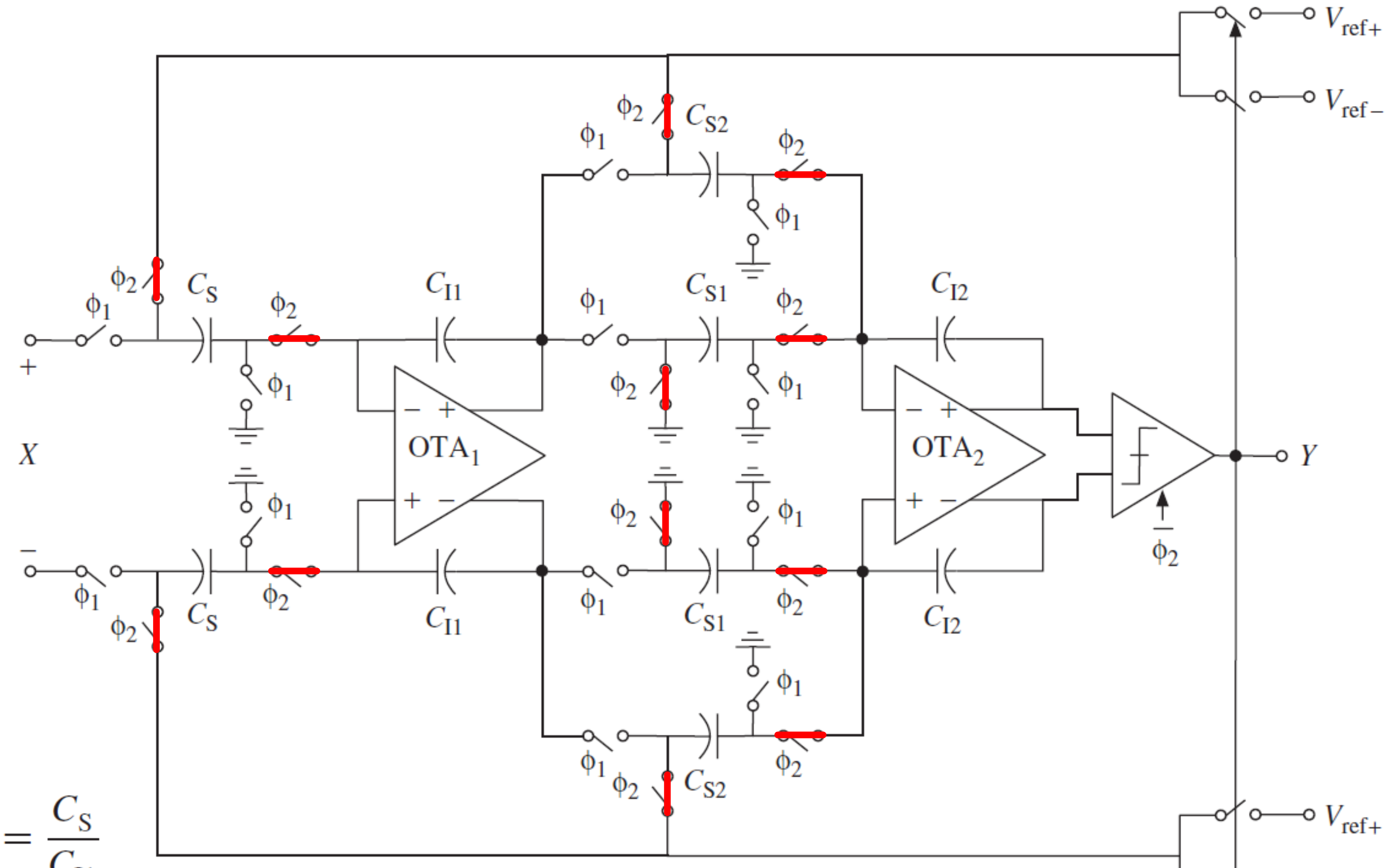


[J. M. de la Rosa and R. del Rio, 2013]

Second-order $\Sigma\Delta M$: SC Implementation



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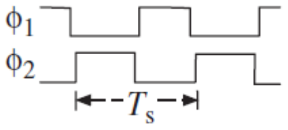


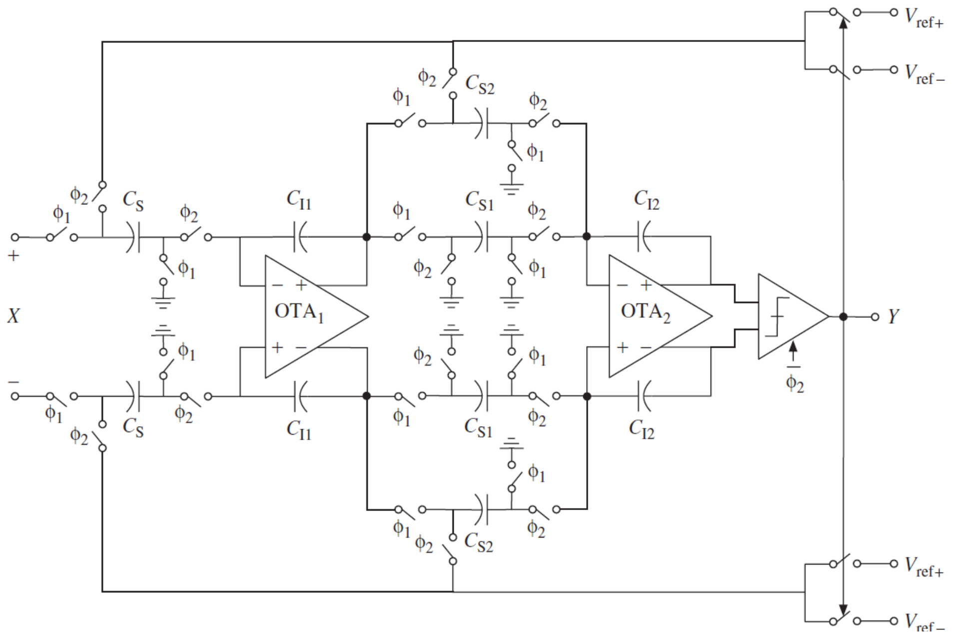
[J. M. de la Rosa and R. del Rio, 2013]

Second-order ΣΔM: Design Examples

$$k_q a_1 a_2 = 1$$
$$k_q a_2 = 2$$

$$g_1 = g_1' = \frac{C_S}{C_{I1}}$$

$$g_2 = \frac{C_{S1} + C_{S2}}{C_{I2}}, \quad g_2' = \frac{C_{S2}}{C_{I2}}$$



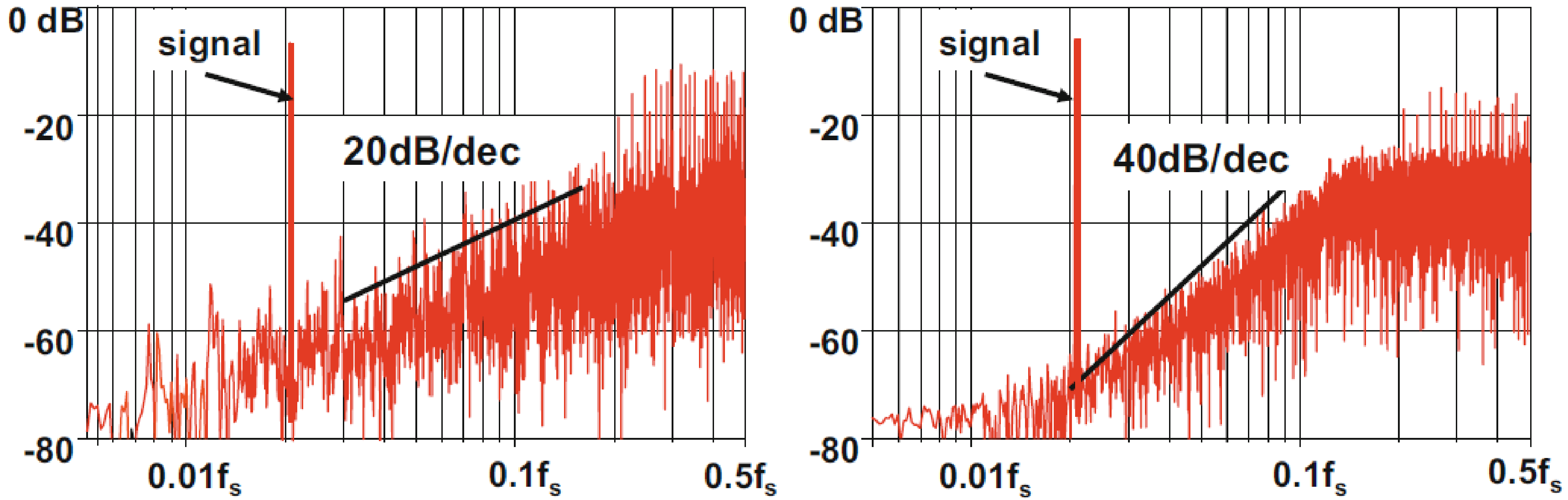
$$\boxed{\begin{aligned} a_1 &= \frac{g_1' g_2}{g_2'} \\ a_2 &= g_2' \end{aligned}}$$

g_1, g_1'	1/2, 1/2	1/4, 1/4	1/2, 1/2	1/3, 1/3
g_2, g_2'	1/2, 1/2	1/2, 1/4	1, 1/2	3/5, 2/5
a_1, a_2	0.5, 0.5	0.5, 0.25	0.5, 0.5	0.5, 0.4
Overload level	−4 dBFS	−4 dBFS	−4 dBFS	−4 dBFS
Integrator output swing	$\pm 1.5 V_{ref}$	$\pm 0.75 V_{ref}$	$\pm 1.25 V_{ref}$	$\pm 1.0 V_{ref}$
Unit capacitors (2× in fully diff)	6(= 3 + 3)	11(= 5 + 6)	9(= 5 + 4)	12(= 4 + 8)

[J. M. de la Rosa and R. del Rio, 2013]

First- vs Second-order SDM

- The dual integration of the signal and the two feedback paths from the quantizer create a much more complex pattern
  - Less correlated products ➔ Less idle tones
- Higher-order converters scramble the pattern even more due to the extra integration stages in the filters
  - Third and fourth order show hardly any idle tones



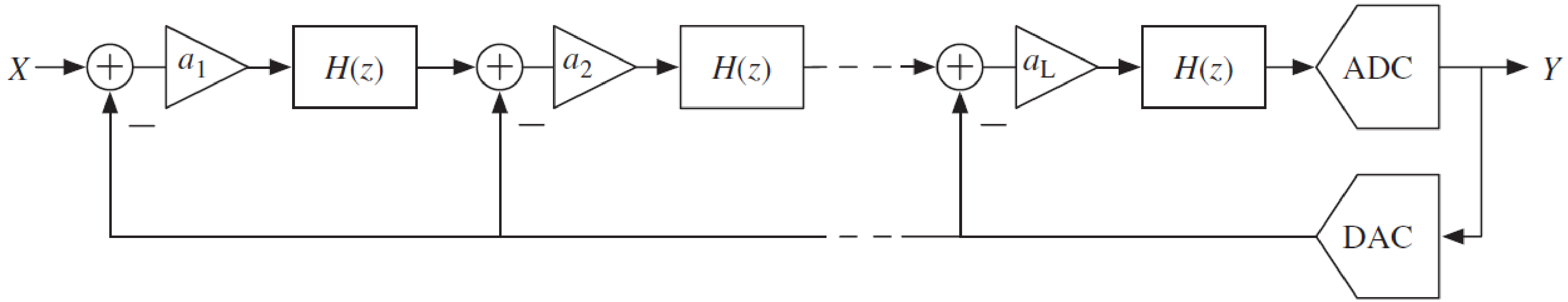
[M. Pelgrom, 2017]

Higher-order $\Sigma\Delta\mathbf{M}$ with Distributed FB

- Simply include L integrators before the quantizer
- Derive a set of relations between the integrator scaling coefficients to fulfill pure differentiator noise shaping

$$Y = z^{-L} \cdot X + (1 - z^{-1})^{L} \cdot E$$

- But pure-differentiator NTFs are prone to instability if $L > 2$
  - Instability appears at the modulator output as a large-amplitude and low-frequency oscillation
    - Long bitstreams of alternating +1s and −1s



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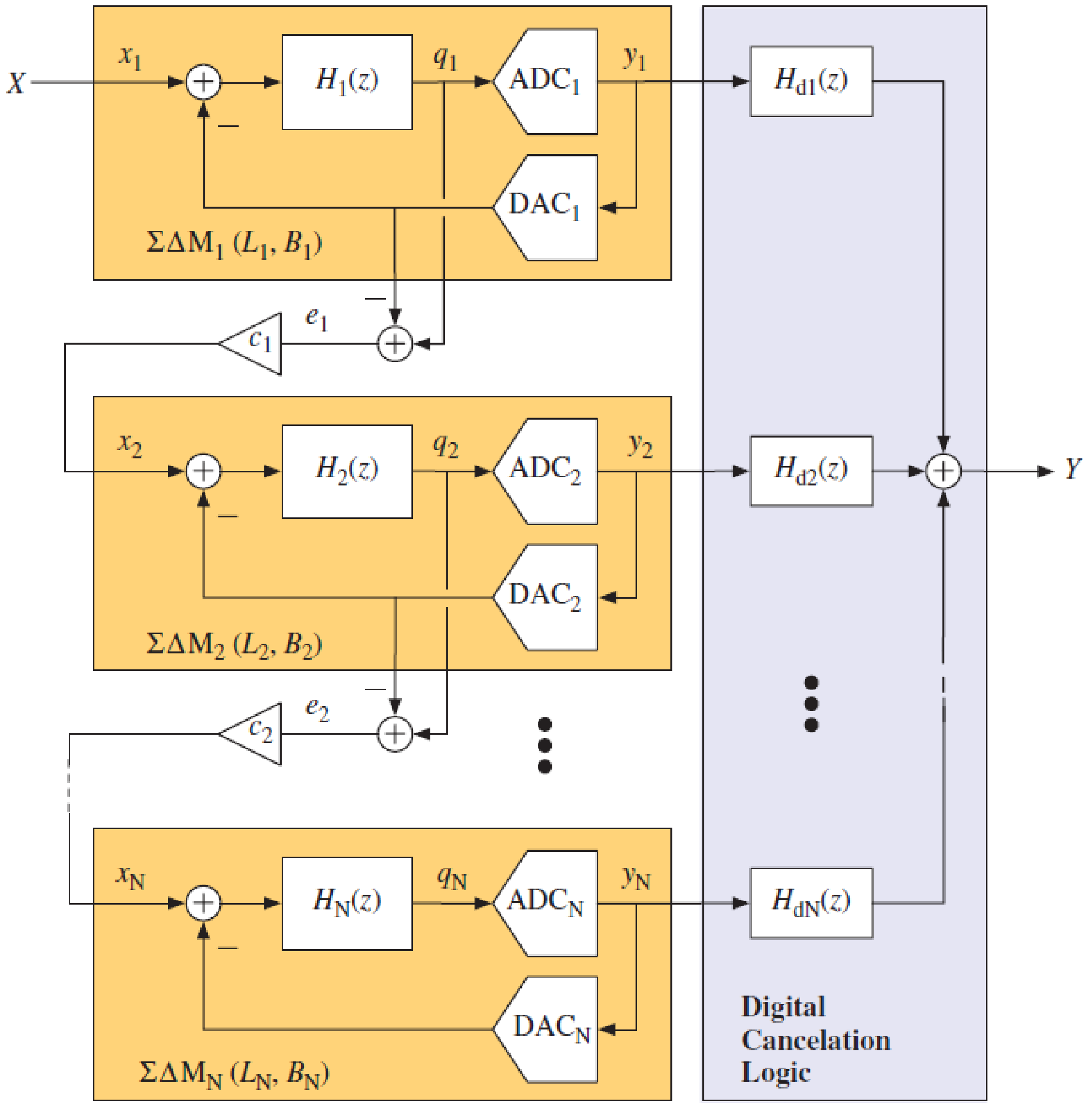
Cascade ΣΔMs

- A.k.a. multiloop **ΣΔM** or multistage noise shaping (**MASH**) **ΣΔM**
- An alternative approach to obtain a high-order noise shaping while avoiding instabilities
- $L = \Sigma L_i$
- Unconditionally stable if $L_i \leq 2$
- No inter-stage feedback
- Digital cancelation logic (DCL) combines outputs such that only e_3 appears at output (shaped by $L = \Sigma L_i$)
- L limited by circuit non-idealities (noise leakage)
  - Practically e_1 (shaped by L_1) and e_2 (shaped by $L_1 + L_2$) will leak to output



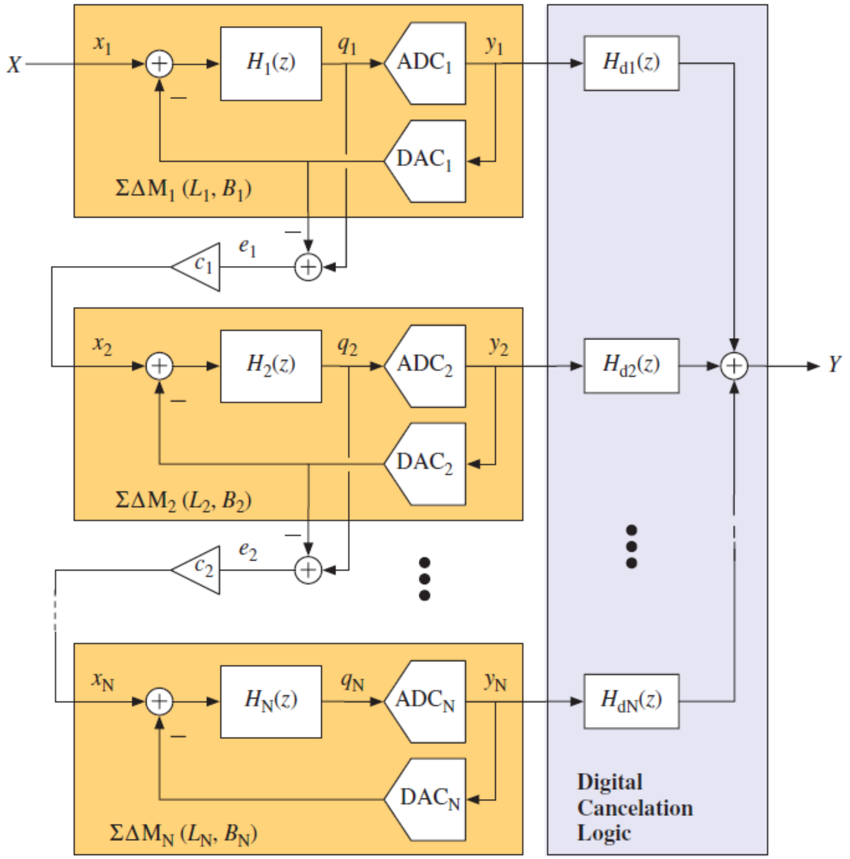
[J. M. de la Rosa and R. del Rio, 2013]

MASH $\mathbf{\Sigma\Delta M}$s Topologies

- The first stage is usually 2nd order SDM
  - Reduce noise leakage
  - Avoid idle tones
- Example MASH toplogies
  - 2-1 ➔ 3rd order
  - 2-2 ➔ 4th order
  - 2-1-1 ➔ …
  - 2-2-1
  - 2-1-1-1
  - 2-2-2
  - etc.

Two-Stage Cascade ΣΔMs Example

- $X_1(z) = X(z)$
- $X_2(z) = -c_1 E_1(z)$
- The digital transfer function should track the analog transfer function
  - Imperfect tracking means E_1 will leak to output (not completely canceled)



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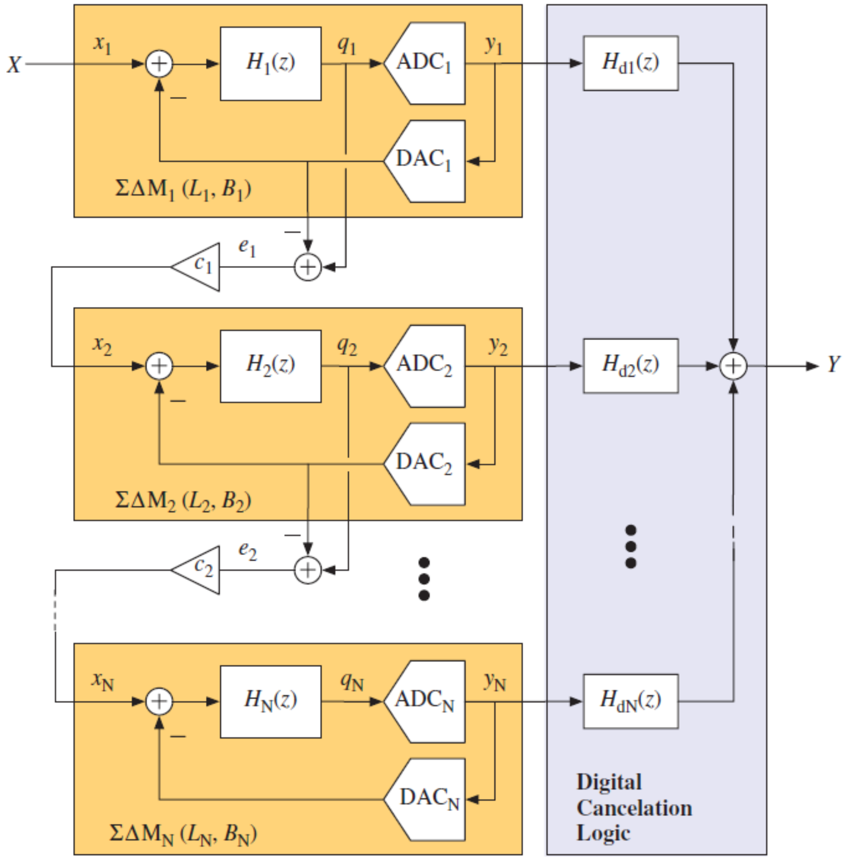


$$
\boxed{\begin{aligned}
Y_1(z) &= \text{STF}_1(z)X_1(z) + \text{NTF}_1(z)E_1(z) \\
Y_2(z) &= \text{STF}_2(z)X_2(z) + \text{NTF}_2(z)E_2(z)
\end{aligned}}
$$

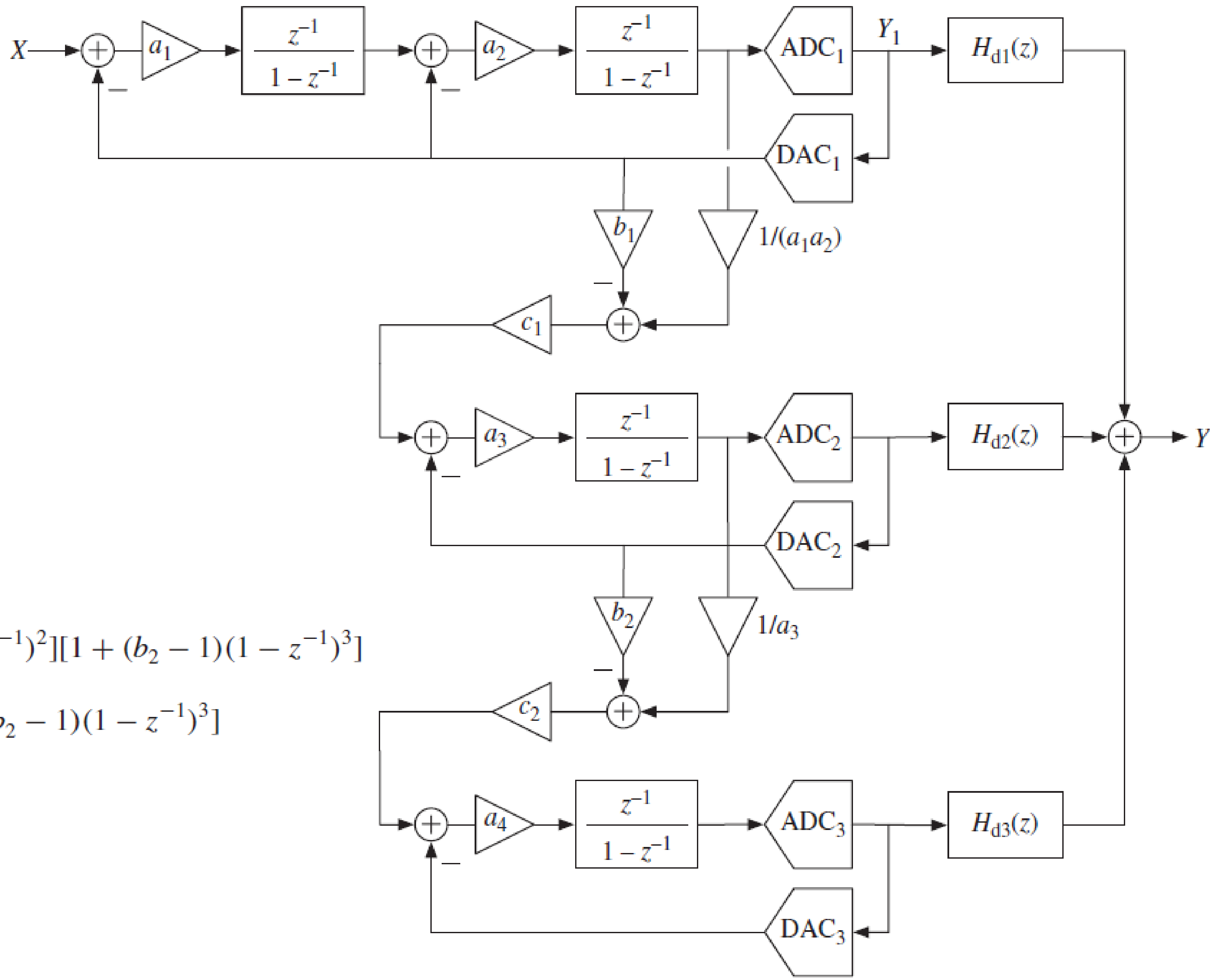
$$
\boxed{\begin{aligned}
Y(z) &= H_{d1}(z)Y_1(z) + H_{d2}(z)Y_2(z) \\
&= \text{STF}_{\text{casc}}(z)X(z) + \text{NTF}_{1,\text{casc}}(z)E_1(z) + \text{NTF}_{2,\text{casc}}(z)E_2(z)
\end{aligned}}
$$

$$
\boxed{\begin{aligned}
\text{STF}_{\text{casc}}(z) &= H_{d1}(z)\text{STF}_1(z) \\
\text{NTF}_{1,\text{casc}}(z) &= H_{d1}(z)\text{NTF}_1(z) - c_1 H_{d2}(z)\text{STF}_2(z) \\
\text{NTF}_{2,\text{casc}}(z) &= H_{d2}(z)\text{NTF}_2(z)
\end{aligned}}
$$

$$
\boxed{\left.\begin{aligned}
H_{d1}(z) &= \text{STF}_2(z) \\
H_{d2}(z) &= \frac{1}{c_1}\text{NTF}_1(z)
\end{aligned}\right\} \Rightarrow \left\{\begin{aligned}
\text{STF}_{\text{casc}}(z) &= \text{STF}_1(z)\text{STF}_2(z) \\
\text{NTF}_{1,\text{casc}}(z) &= 0 \\
\text{NTF}_{2,\text{casc}}(z) &= \frac{1}{c_1}\text{NTF}_1(z)\text{NTF}_2(z)
\end{aligned}\right.}
$$

[J. M. de la Rosa and R. del Rio, 2013]

Example: MASH 2-1-1 SDM



$$k_{q1}a_1a_2 = 1,\ k_{q1}a_2 = 2$$

$$k_{q2}a_3 = 1$$

$$k_{q3}a_4 = 1$$

$$H_{d1}(z) = z^{-2}[1 + (b_1 - 1)(1 - z^{-1})^2][1 + (b_2 - 1)(1 - z^{-1})^3]$$

$$H_{d2}(z) = \frac{1}{c_1}z^{-1}(1 - z^{-1})^2[1 + (b_2 - 1)(1 - z^{-1})^3]$$

$$H_{d3}(z) = \frac{1}{c_1c_2}(1 - z^{-1})^3$$

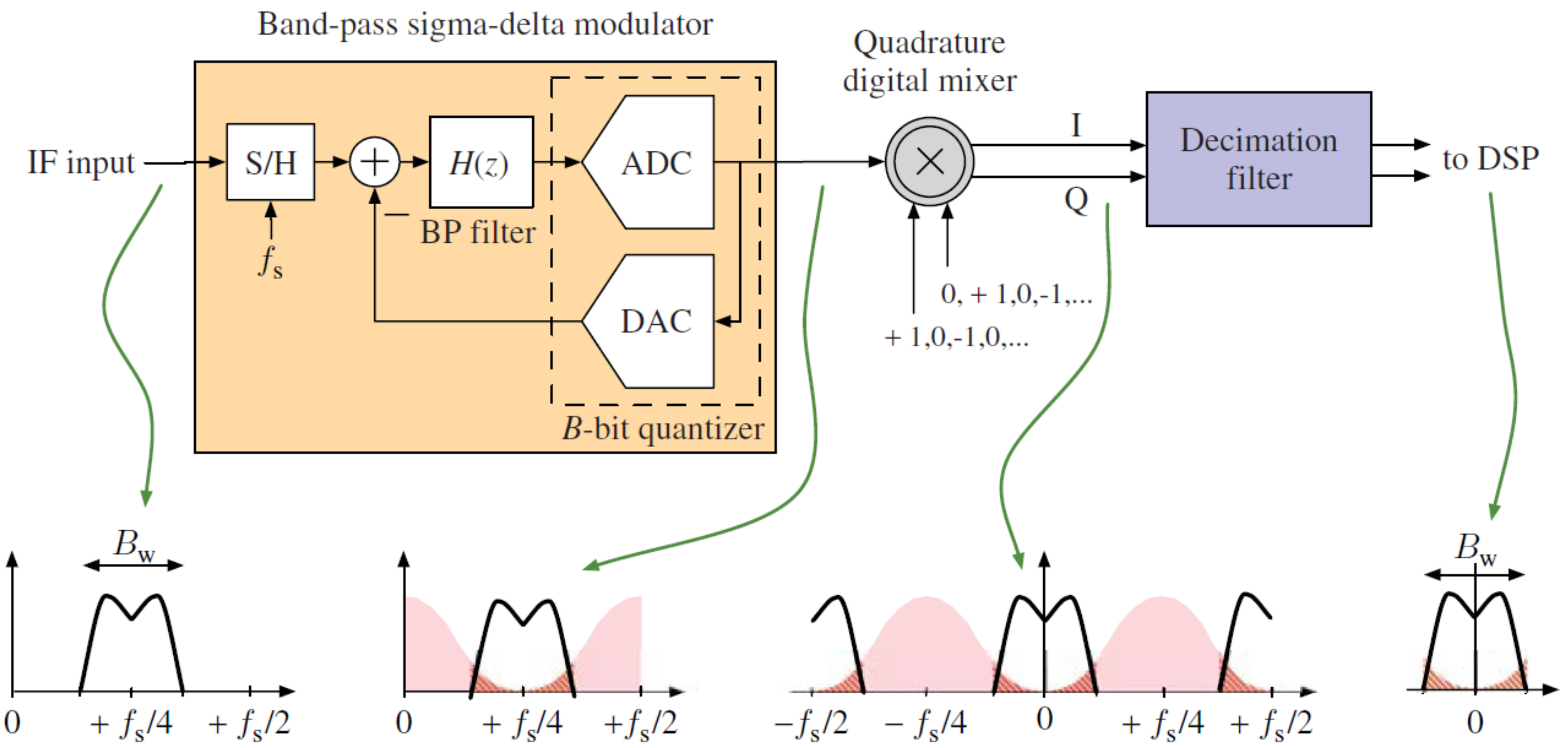
[J. M. de la Rosa and R. del Rio, 2013]

More $\mathbf{\Sigma\Delta M}$s Classification

- Low-Pass vs Band-Pass $\mathbf{\Sigma\Delta M}$s
- Discrete-Time vs Continuous-Time $\mathbf{\Sigma\Delta M}$s
  - Discrete-time: uses DT filter (switched capacitor filter)
  - Continuous-time: uses CT filter (e.g., Gm-C filter)

Band-pass SDM

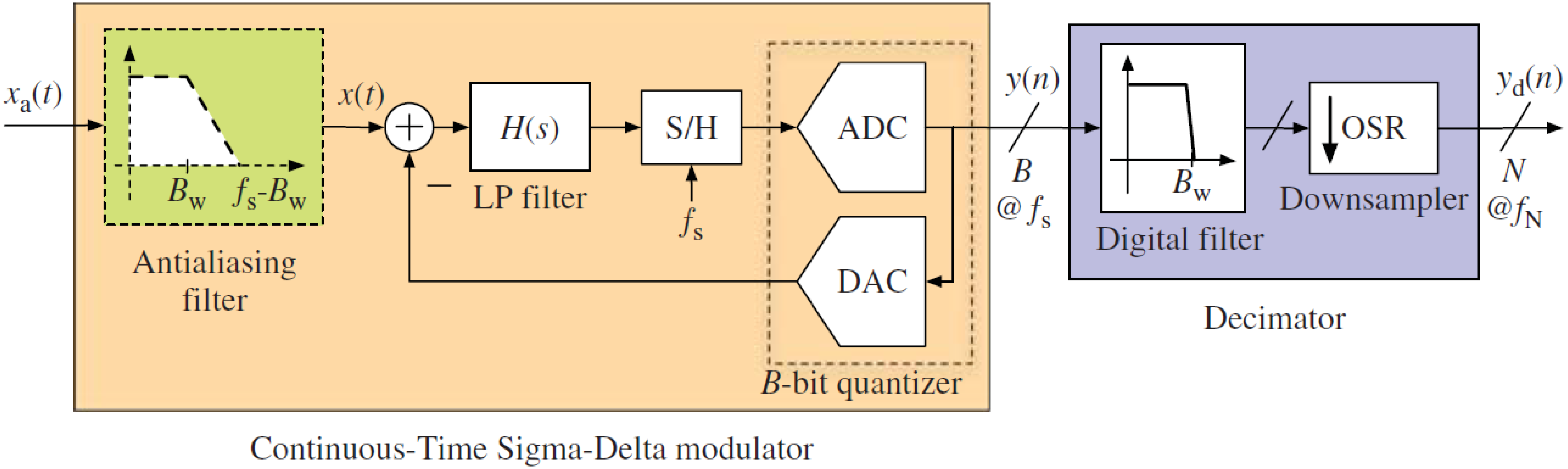
- In low-pass SDM, the NTF is HPF
- In band-pass SDM, the NTF is band-stop filter
- BP-SDM is used for digitizing IF signals in wireless receivers



[J. M. de la Rosa and R. del Rio, 2013]

Continuous-Time (CT) SDMs

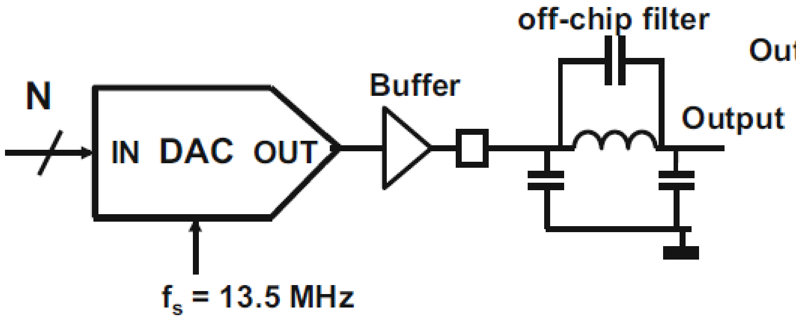
- The majority of SDMs are implemented using SC DT circuits
- CT SDMs can operate at higher sampling rates with lower power consumption
- The sampling operation is moved just before the quantizer

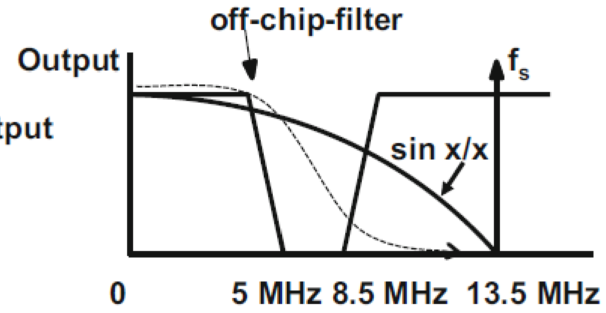


[J. M. de la Rosa and R. del Rio, 2013]

Nyquist vs Oversampling DAC

- DAC with BW close to Nyquist limit
  - Requirements on the filter (sharpness) and the buffer (SR) become hard to meet





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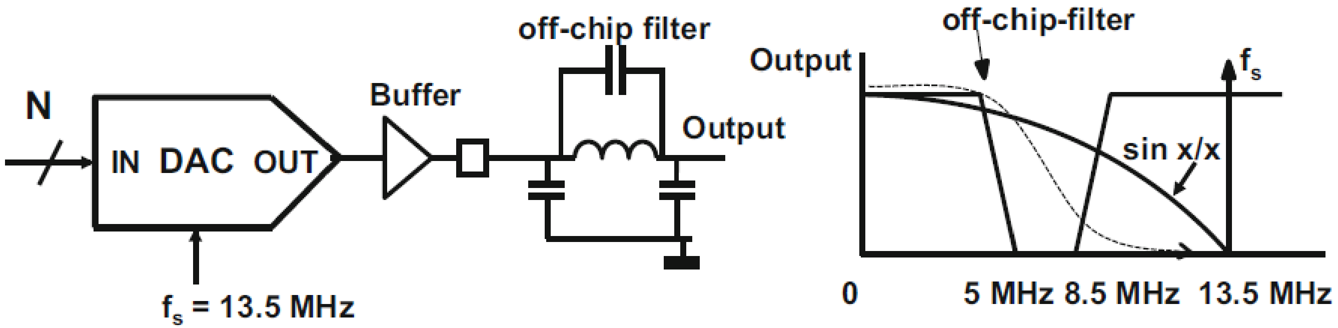
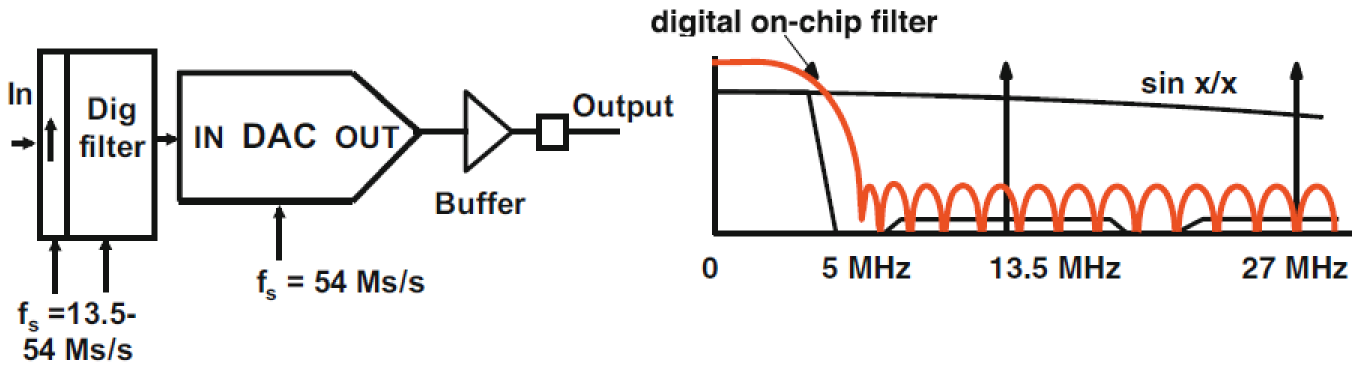


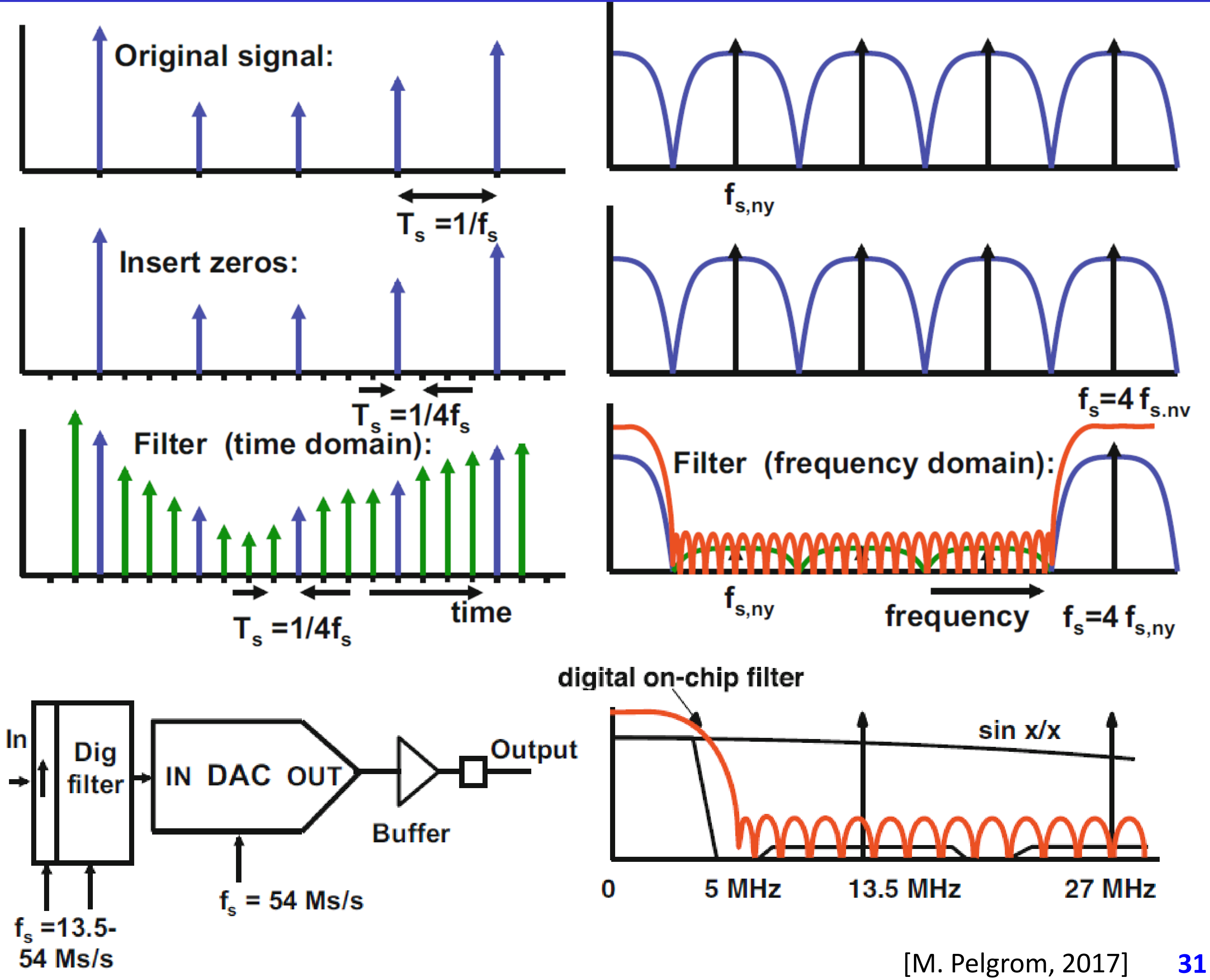
- Oversampling DAC
  - Simpler filter and buffer → but digital filtering required
  - sinc(x) distortion reduced → no sinc(x) compensation required



[M. Pelgrom, 2017]

Oversampling DAC

- ❑ Up-sampling by zero stuffing
- ❑ Digital filter is required after up-sampling to suppress alias bands
  - Performs interpolation in digital domain
- ❑ Smaller transient steps at output
  - Buffer SR and distortion specs are relaxed



[M. Pelgrom, 2017]

Nyquist vs Oversampling DAC

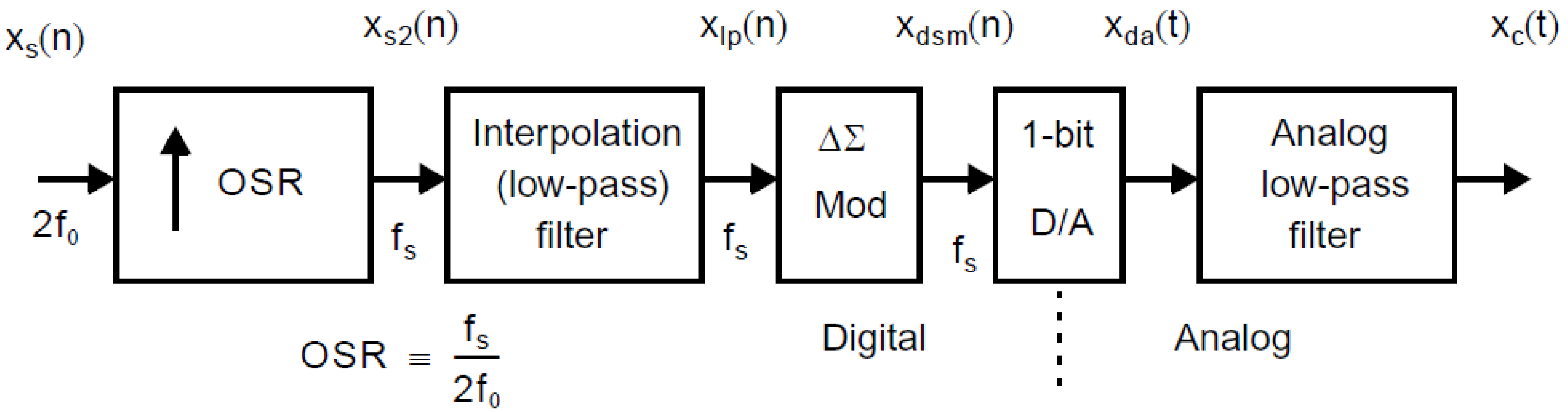
- Trade-off between analog buffer and filter power/complexity and digital filter power/area
  - Modern CMOS technologies favors the oversampling solution
  - Area and power of the digital filter shrinks and the switching speed of the short channel transistors allows high oversampling frequencies
- Comparison for OSR = 4:

Nyquist rate solution	Oversampling solution
External multi-pole filter needed	Internal digital CMOS filter
High slew current in driver	Medium current in driver power for digital filter
sin(x)/x loss of 2 dB	sin(x)/x loss $= 0.3$ dB
Standard sample rate	$4\times$ sample rate needed

[M. Pelgrom, 2017]

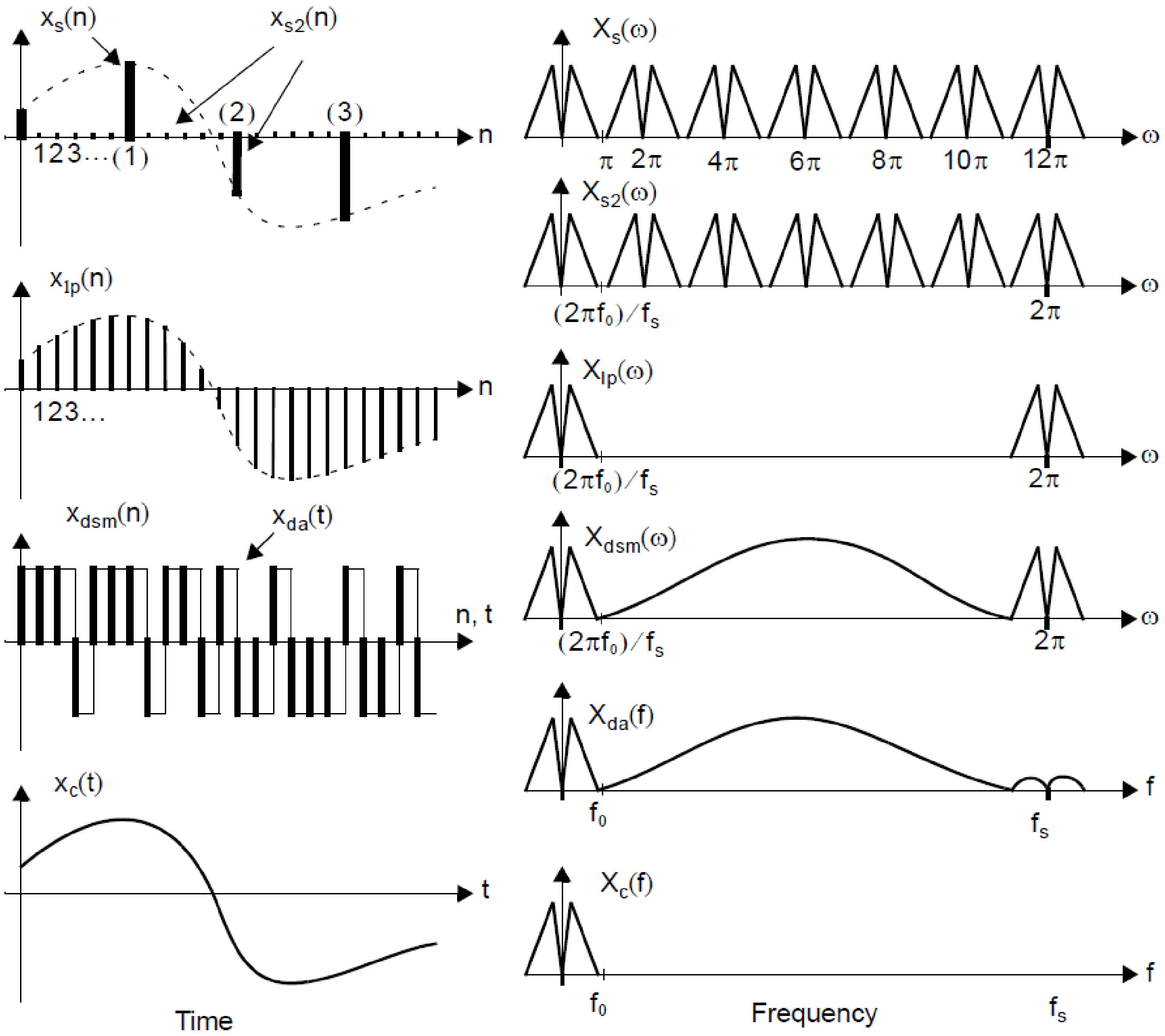
Sigma-Delta DAC

- The order of the analog low pass filter should be at least one order higher than that of the modulator.
  - If the analog filter's order is equal to that of the modulator, the slope of the rising quantization noise will match the filter's falling attenuation
- Oversampling is often used with multi-bit D/A converters to reduce this analog-smoothing filter's complexity



[Johns & Martin, 2012]

Sigma-Delta DAC



[Johns & Martin, 2012]

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- J. M. de la Rosa and R. del Rio, CMOS Sigma-Delta Converters: Practical Design Guide, Wiley, 2013.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.
- Y. Chiu, EECT 7327, UTD.

Thank you!