Analog Integrated Systems Design

Lecture 06
Data Converters Testing

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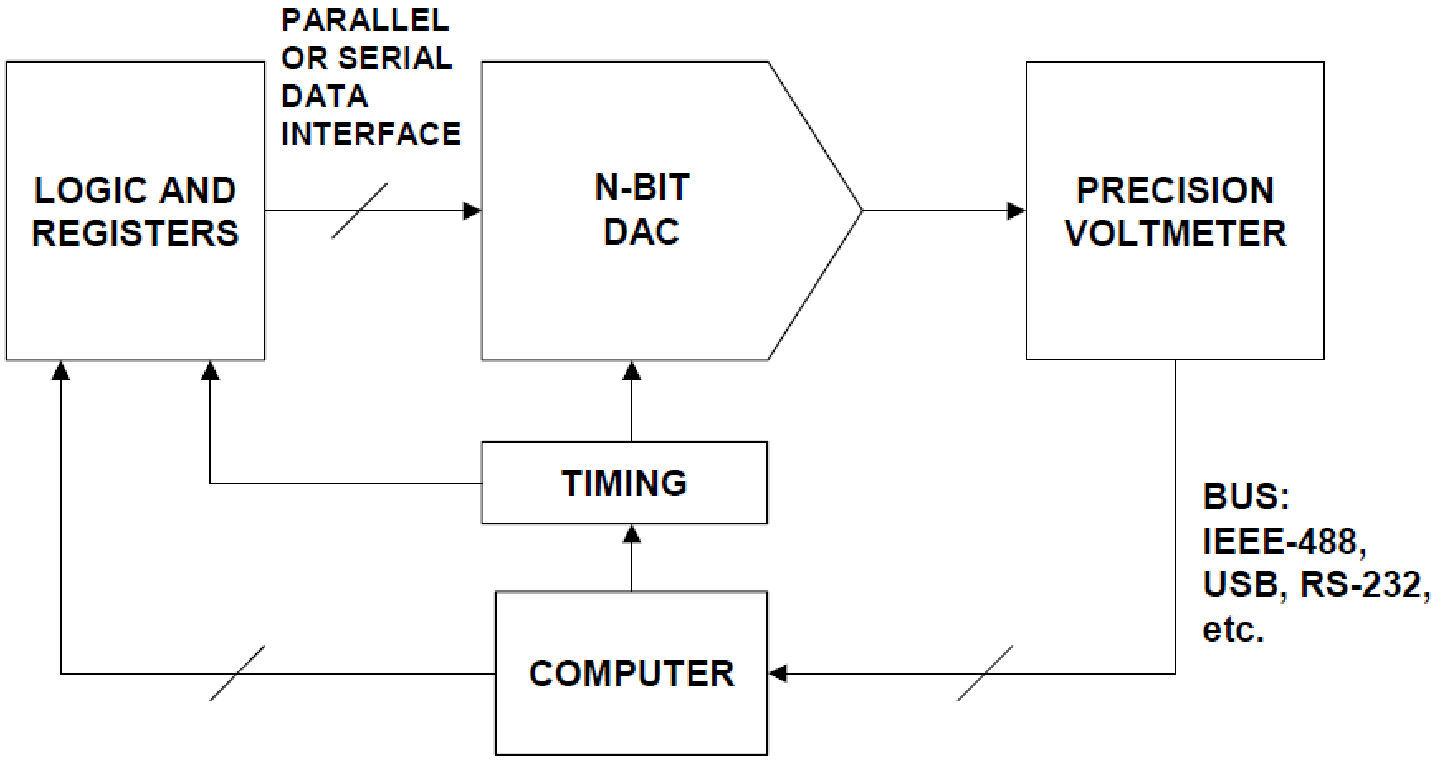
DAC Static Testing

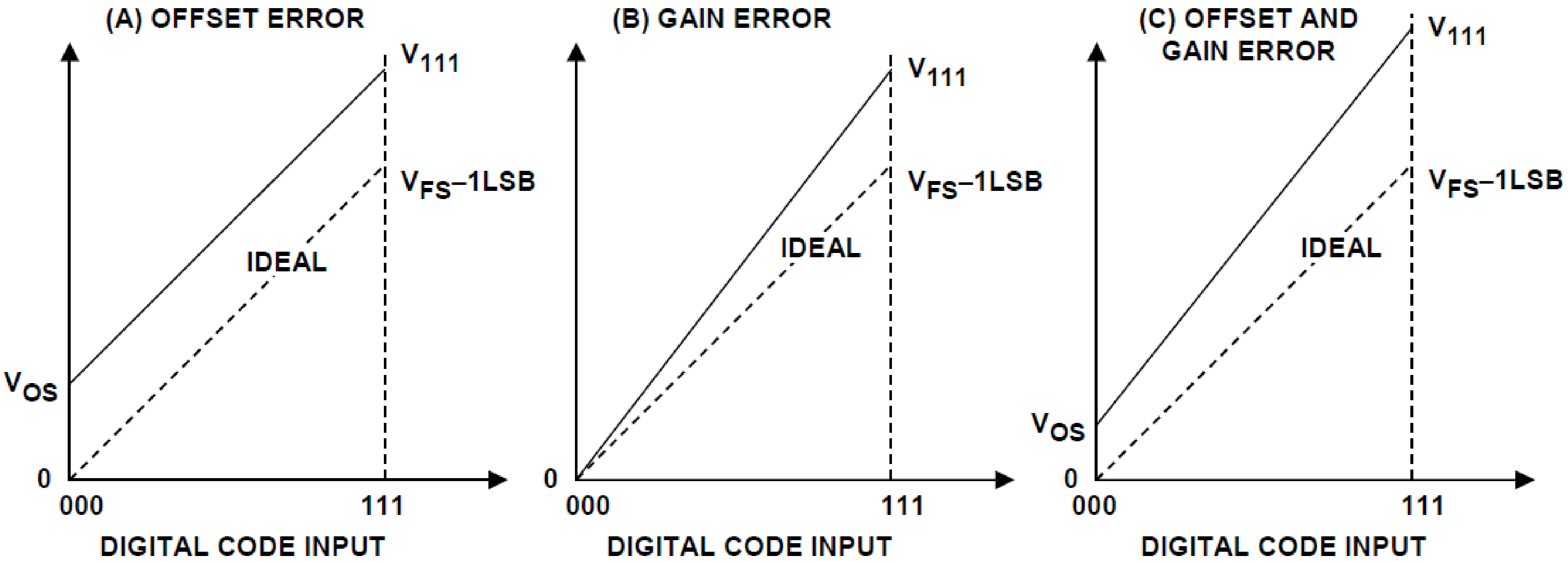
- Many points to test!
- Use automated computer-based test setup (LabVIEW, MATLAB, etc.)
- Most equipment can be computer-controlled (GPIB, USB, etc.)



[W. Kester, ADI, 2005]

DAC Offset and Gain Errors

- Measure offset error first then measure gain error



OFFSET ERROR = V_{000} = V_{OS}

GAIN ERROR = 0

OFFSET ERROR = 0

GAIN ERROR (%) =

$$100\left[\frac{V_{111}}{V_{FS}-1LSB}-1\right]$$

OFFSET ERROR = V_{000} = V_{OS}

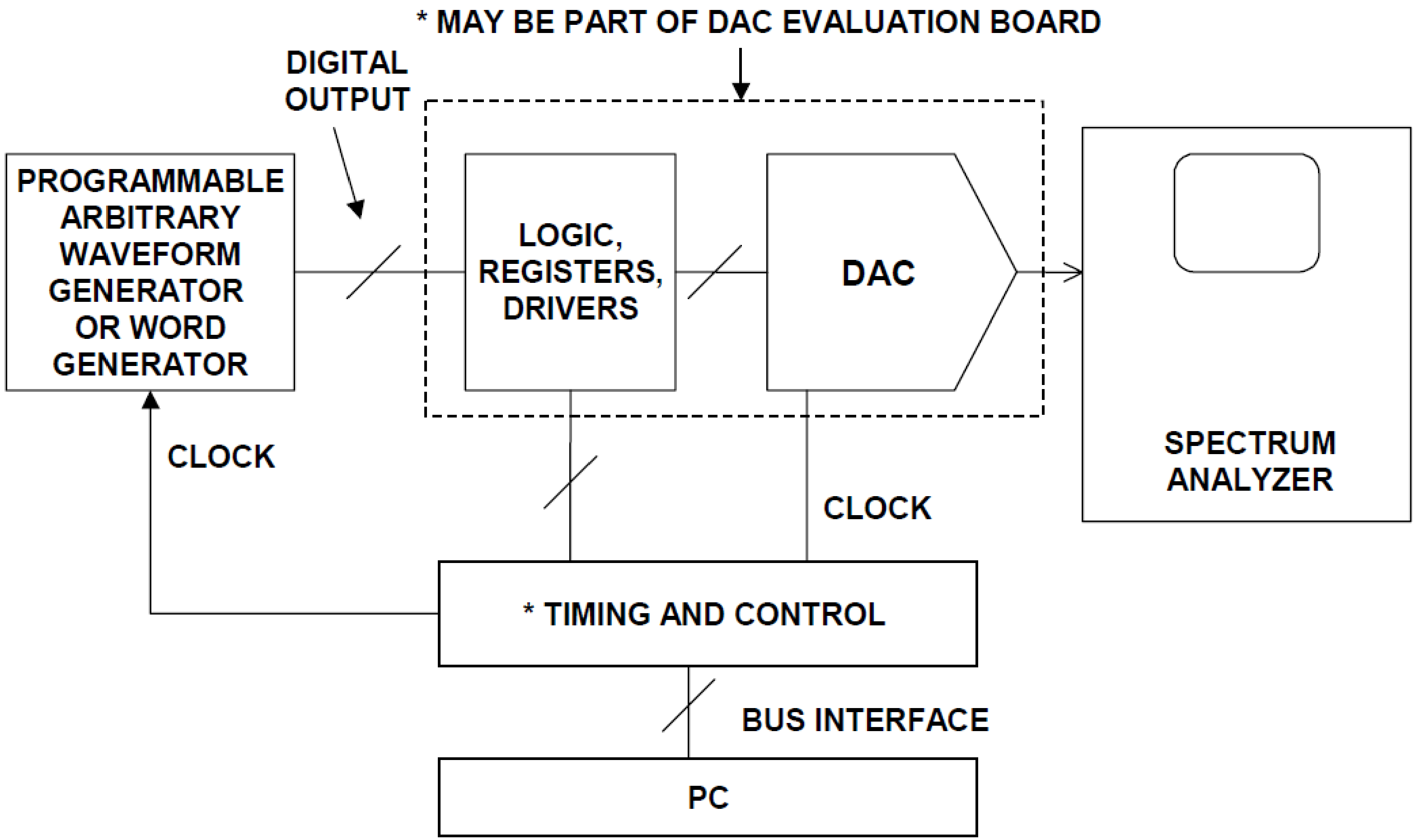
GAIN ERROR (%) =

$$100\left[\frac{V_{111}-V_{OS}}{V_{FS}-1LSB}-1\right]$$

[W. Kester, ADI, 2005]

DAC Dynamic Testing

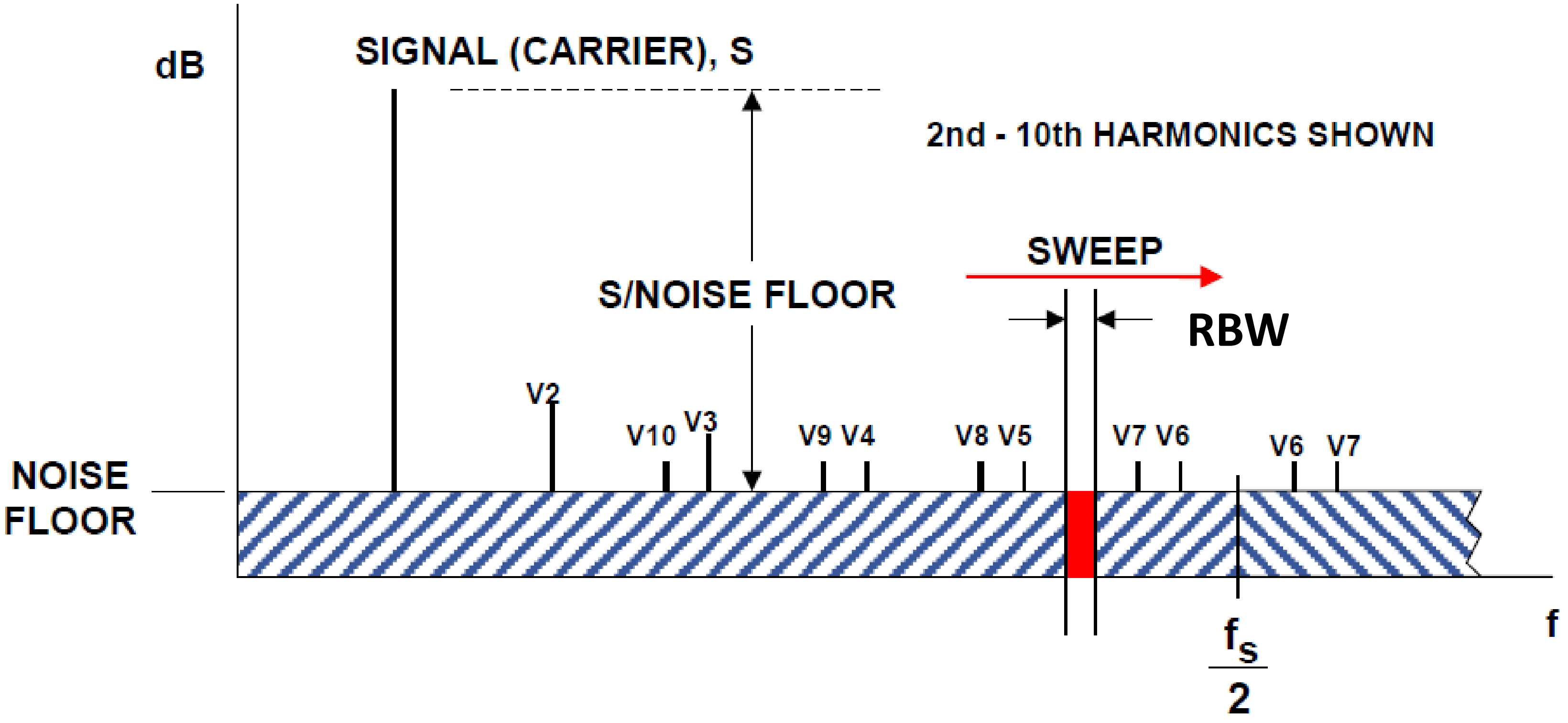
- Drive DAC by digital sine wave
- Plot analog output using spectrum analyzer



[W. Kester, ADI, 2005]

DAC Dynamic Testing

- Spectrum analyzer resolution bandwidth (RBW) is equivalent to FFT bin size



- RBW = ANALYZER RESOLUTION BANDWIDTH
- $\text{SNR} = \text{S/NOISE FLOOR} - 10\log_{10}\left[\frac{f_s/2}{\text{RBW}}\right]$

[W. Kester, ADI, 2005]

DAC Dynamic Testing

- $$\text{SNR} = \text{S/NOISE FLOOR} - 10\log_{10}\left[\frac{f_s/2}{\text{RBW}}\right]$$

- $$\text{THD} = 20\log_{10}\sqrt{\left[10^{-V2/20}\right]^2 + \left[10^{-V3/20}\right]^2 + \cdots + \left[10^{-V6/20}\right]^2}$$

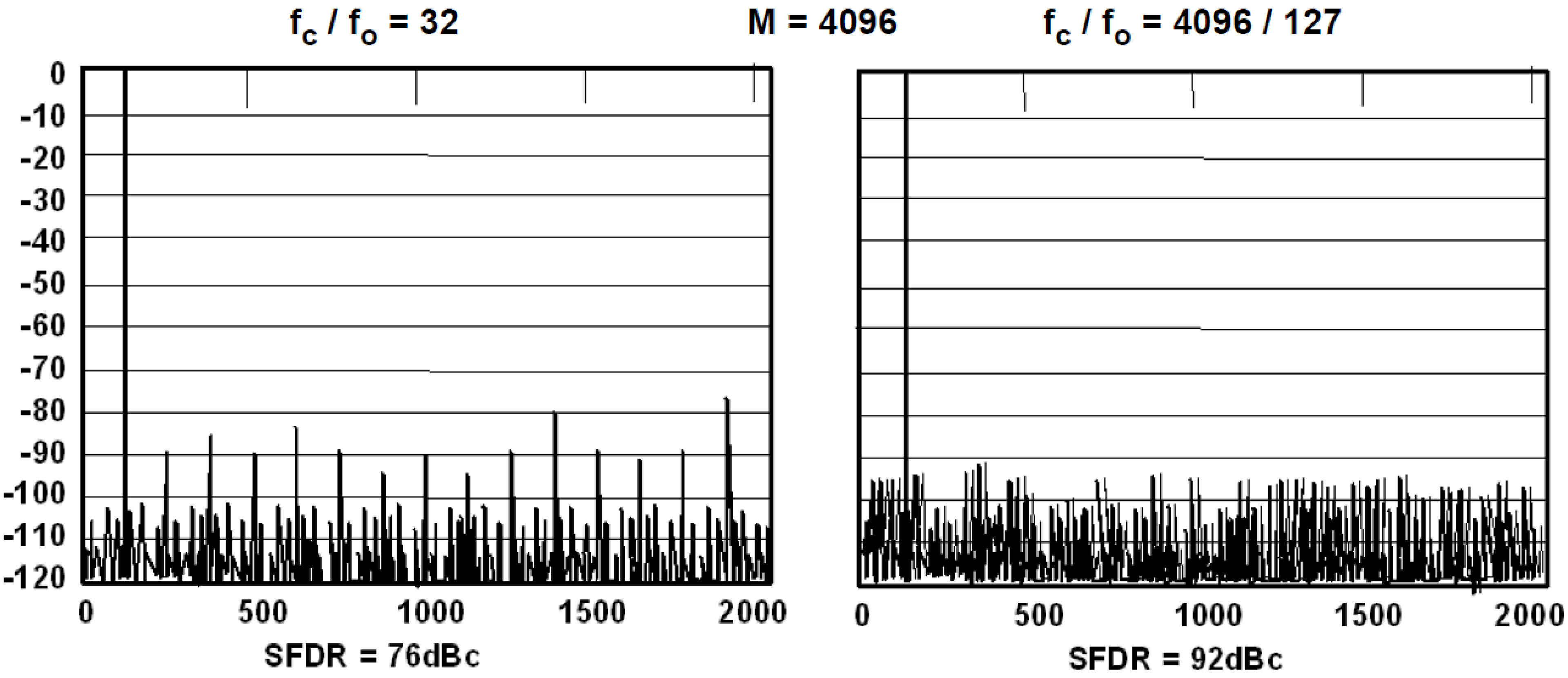
- $$\text{SINAD} = 20\log_{10}\sqrt{\left[10^{-\text{SNR}/20}\right]^2 + \left[10^{-\text{THD}/20}\right]^2}$$

NOTE: NOISE FLOOR, SNR, THD, SINAD, V2, V3, … , V6 in units of dBc

[W. Kester, ADI, 2005]

DAC Dynamic Testing

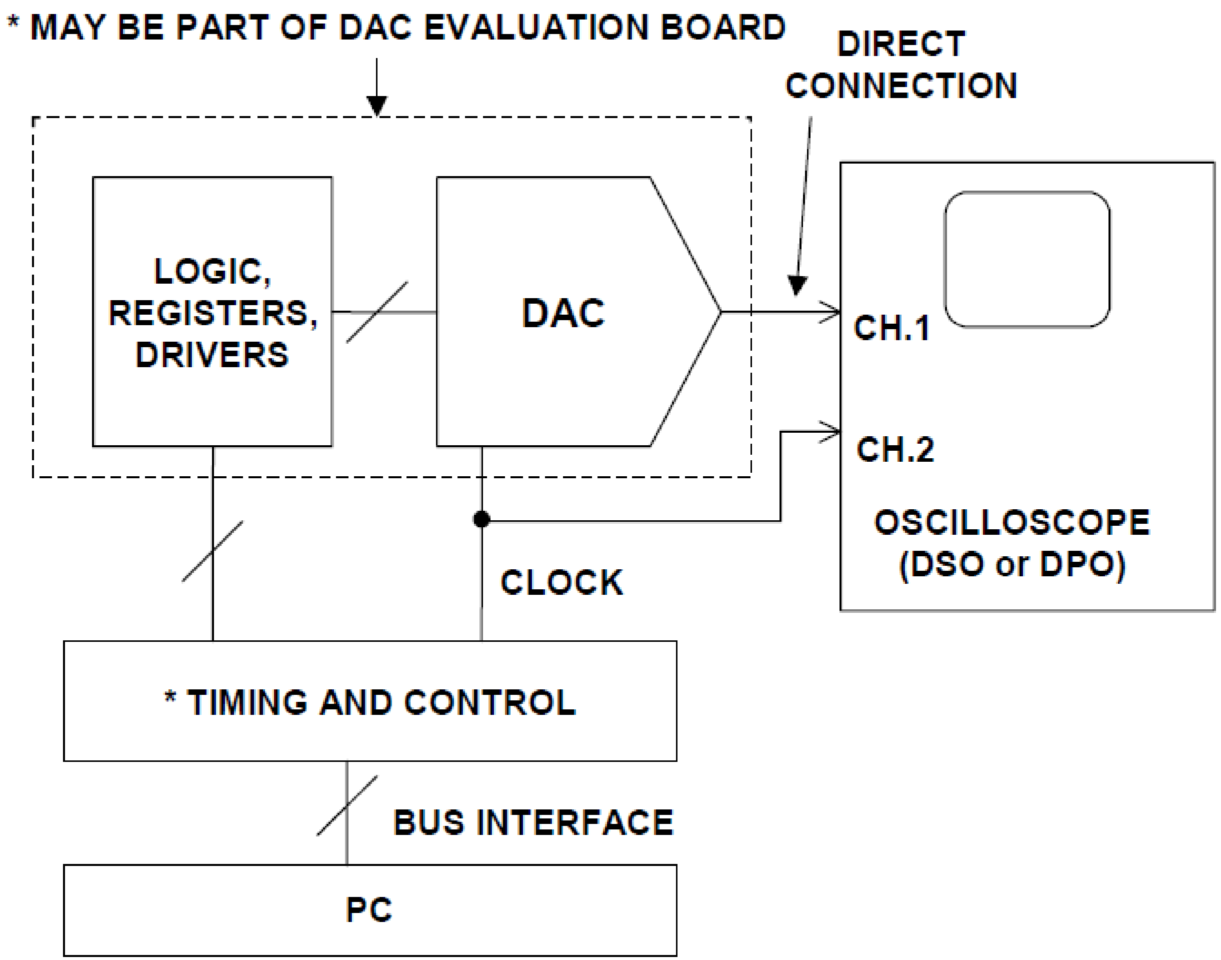
- The ratio of update rate to test tone frequency must be non-integer
  - Otherwise quantization noise will appear as distortion



[W. Kester, ADI, 2005]

DAC Settling Time Testing

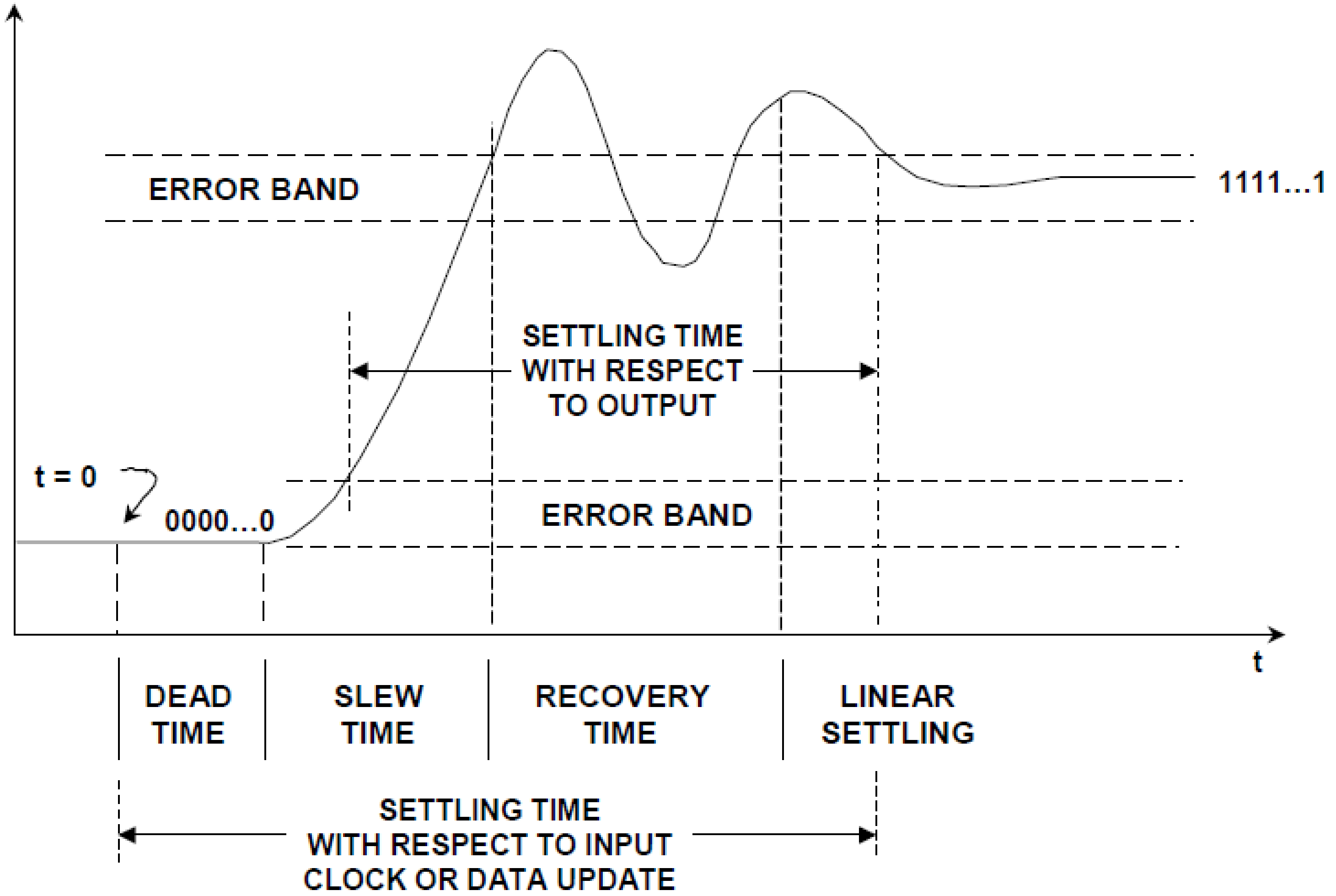
- Drive DAC by digital step
- Plot clock and output on oscilloscope



[W. Kester, ADI, 2005]

DAC Full-Scale Settling Time Testing

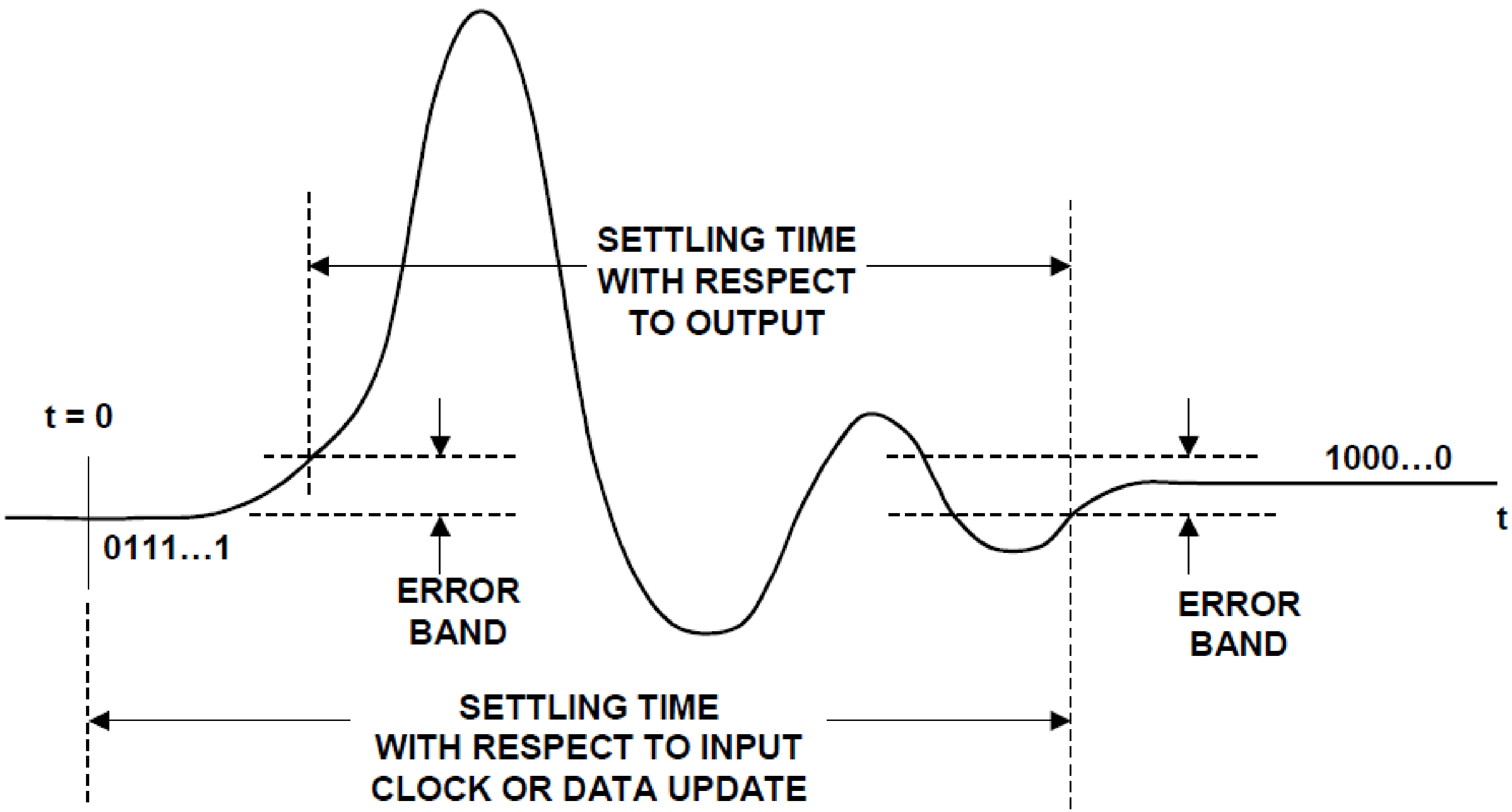
- Digital step from all 0s to all 1s



[W. Kester, ADI, 2005]

DAC Mid-Scale Settling Time Testing

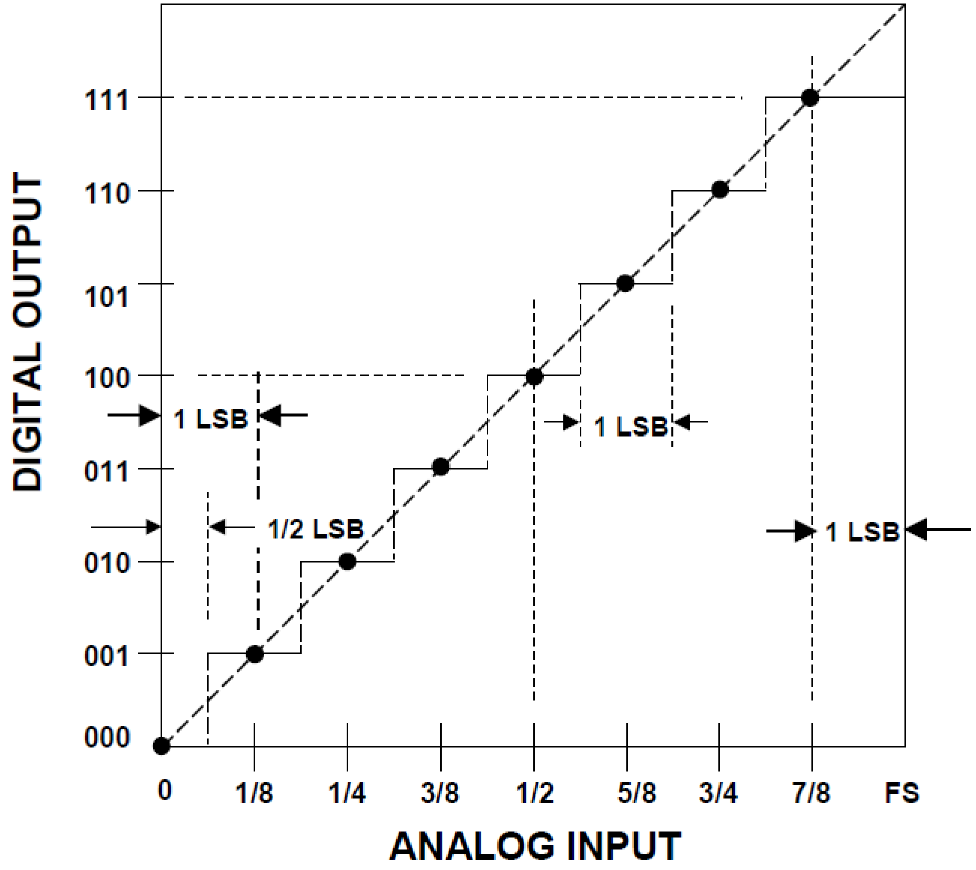
- In midscale transition all bits are switched, but may not switch simultaneously

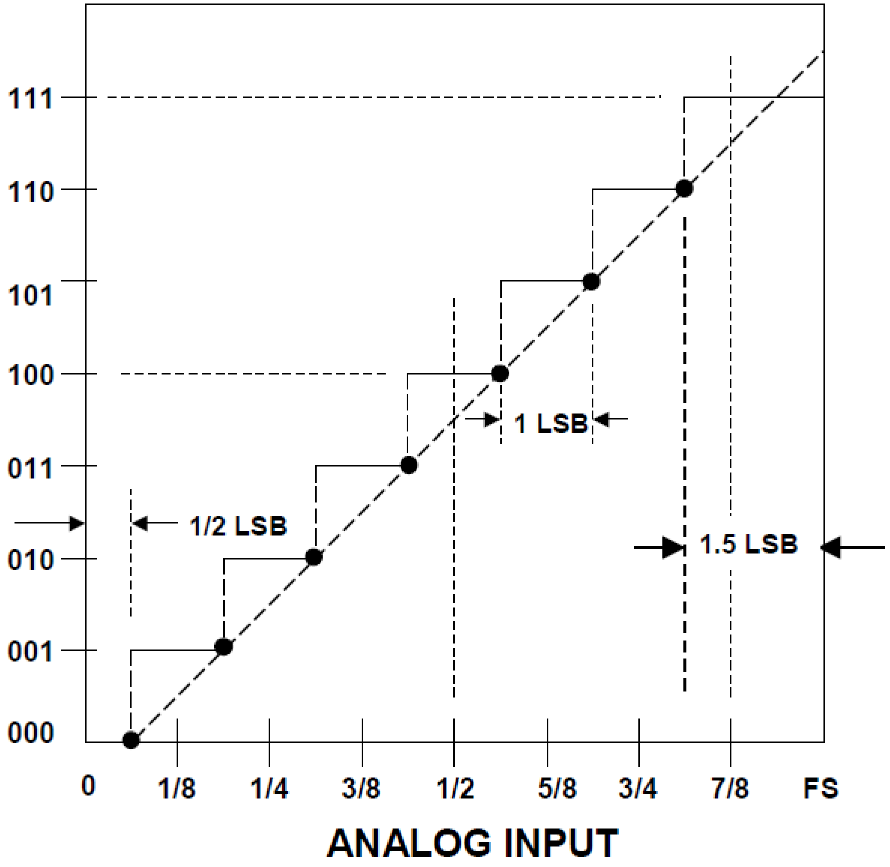


[W. Kester, ADI, 2005]

ADC Static Testing

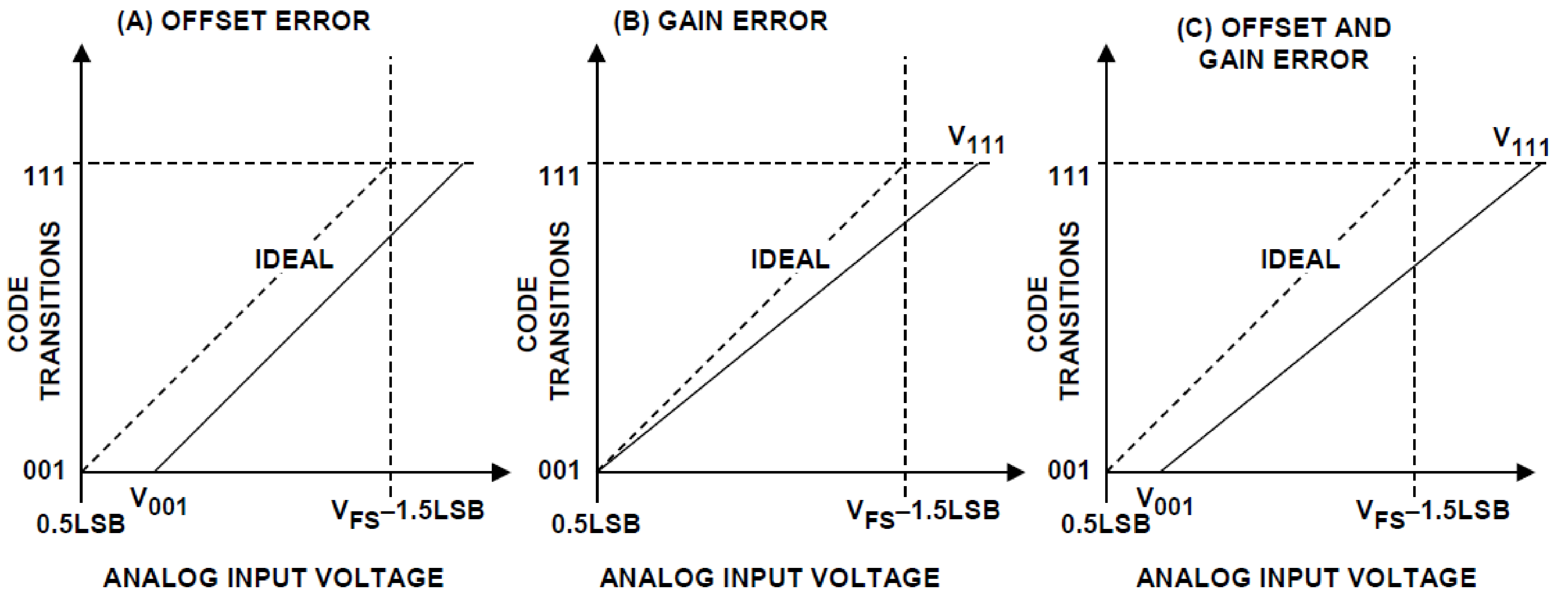
- Code centers are difficult to measure → use code transitions
  - First point in the ccs (first code transition) at $V_{LSB}/2$
  - Last point in the ccs (last code transition) at $V_{FS} - 1.5V_{LSB}$





[W. Kester, ADI, 2005]

ADC Offset and Gain Errors



(A)

OFFSET ERROR = V_{001} – 0.5LSB

GAIN ERROR = 0

NOTE: V_{001} = CODE TRANSITION BETWEEN 000 AND 001

(B)

OFFSET ERROR = 0

GAIN ERROR (%) =

$$100\left[\frac{V_{111} - 0.5\text{LSB}}{V_{FS} - 2\text{LSB}} - 1\right]$$

(C)

OFFSET ERROR = V_{001} – 0.5LSB

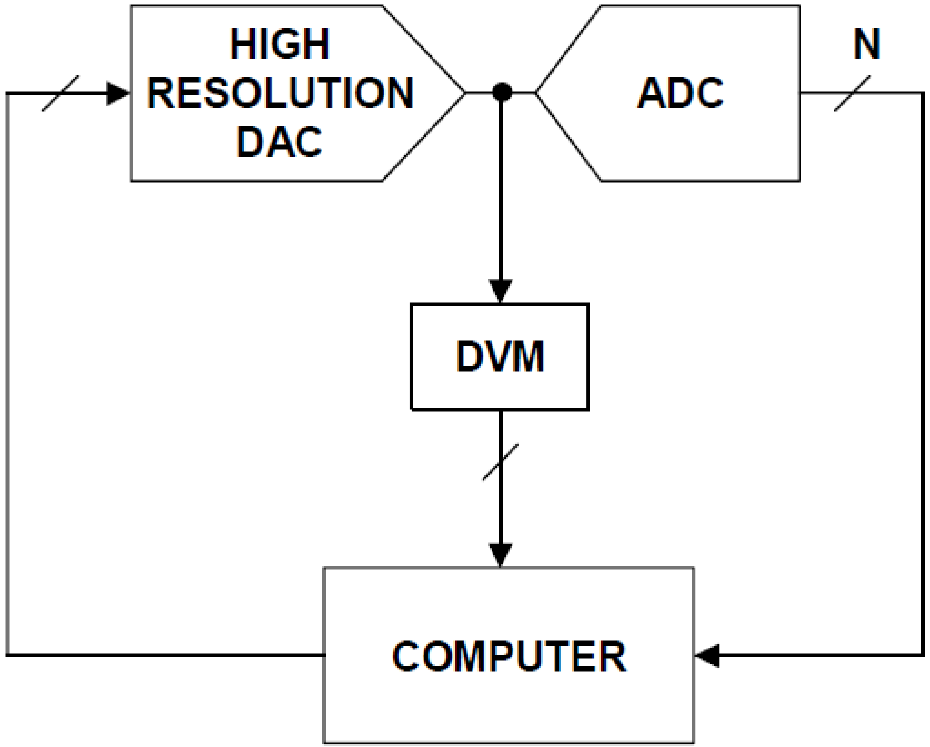
GAIN ERROR (%) =

$$100\left[\frac{V_{111} - V_{001}}{V_{FS} - 2\text{LSB}} - 1\right]$$

[W. Kester, ADI, 2005]

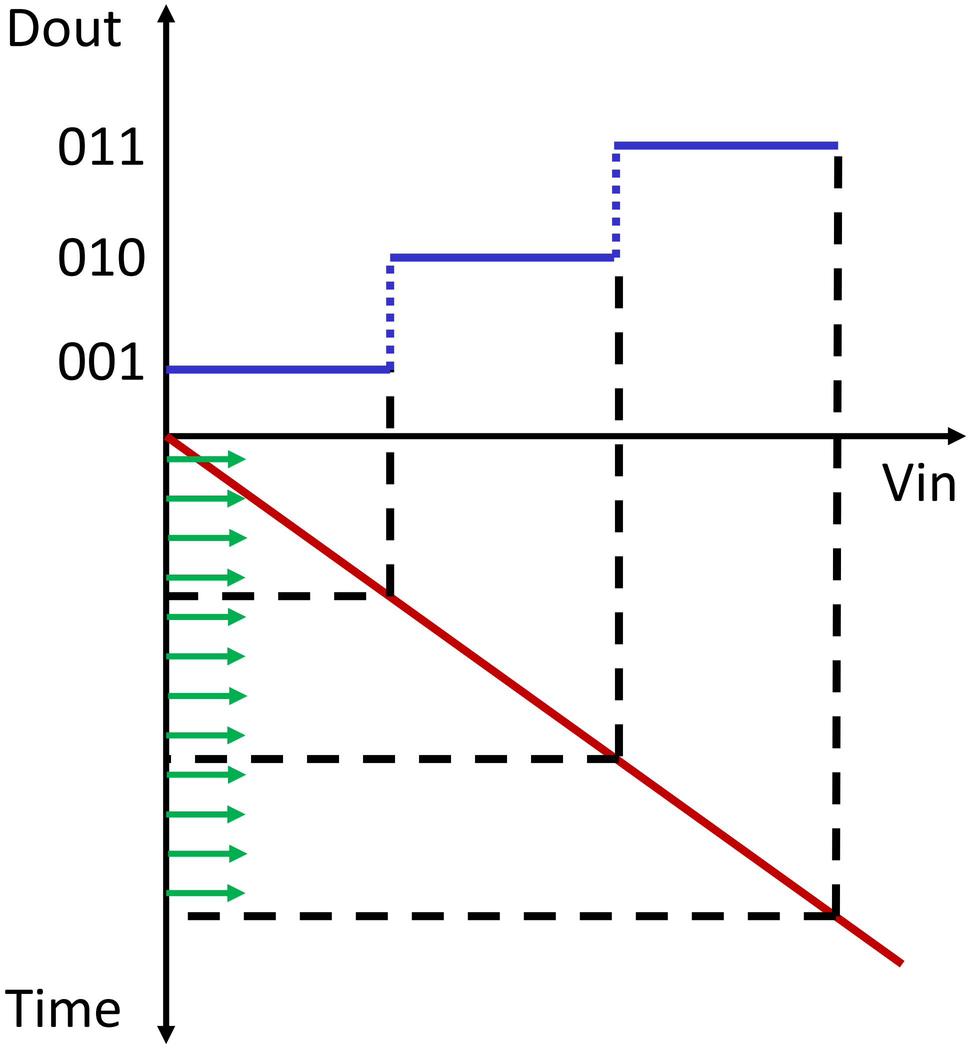
Servo-Loop Code Transition Test

- ❑ Detect when ADC output code flips
  - Record DVM output → code transition
  - Use averaging to cancel ADC input-referred noise
- ❑ DAC resolution must be ≥ ADC resolution + 2-bit

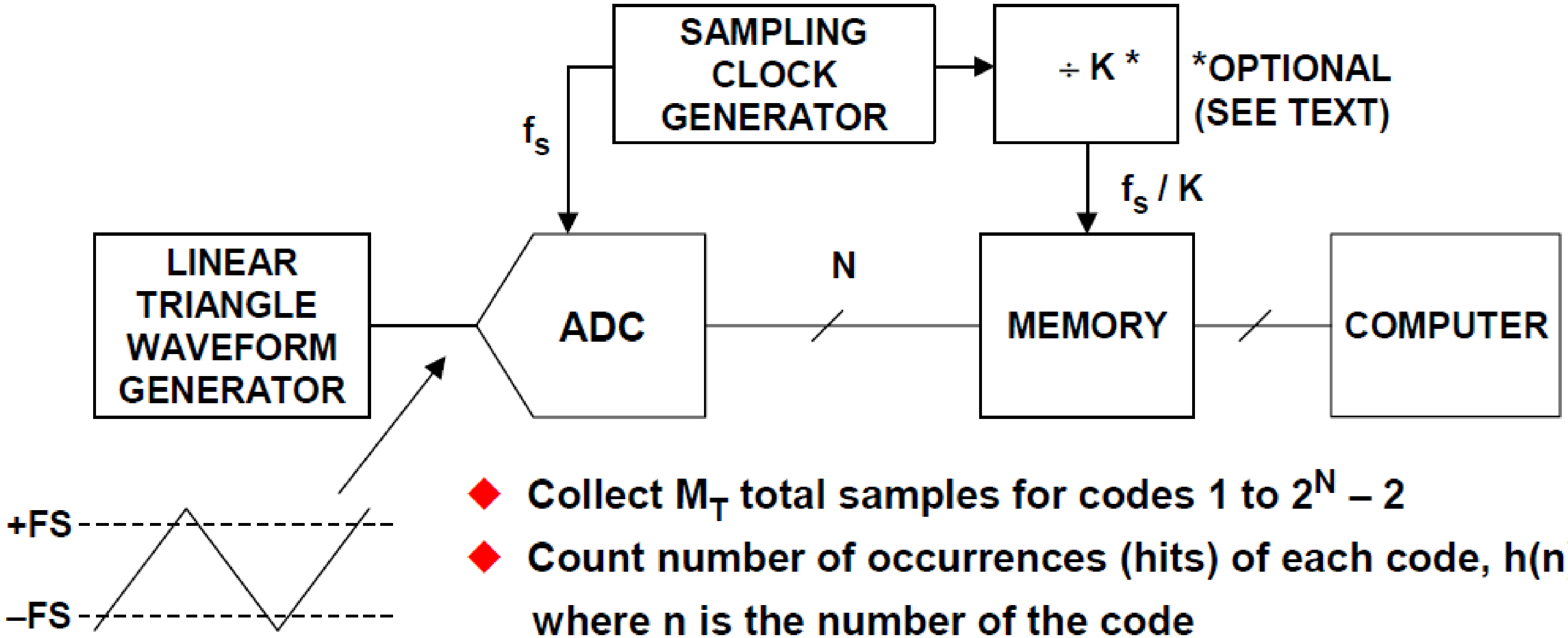


[W. Kester, ADI, 2005]

Histogram (Code Density) Test



Histogram (Code Density) Test



- Collect M_T total samples for codes 1 to $2^N - 2$
- Count number of occurrences (hits) of each code, $h(n)_{ACTUAL}$, where n is the number of the code
- For FS triangle input, theoretical number of hits is:
  $h(n)_{THEORETICAL} = M_T / (2^N - 2)$
- Calculate DNL of each code for n = 1 to n = $2^N - 2$:

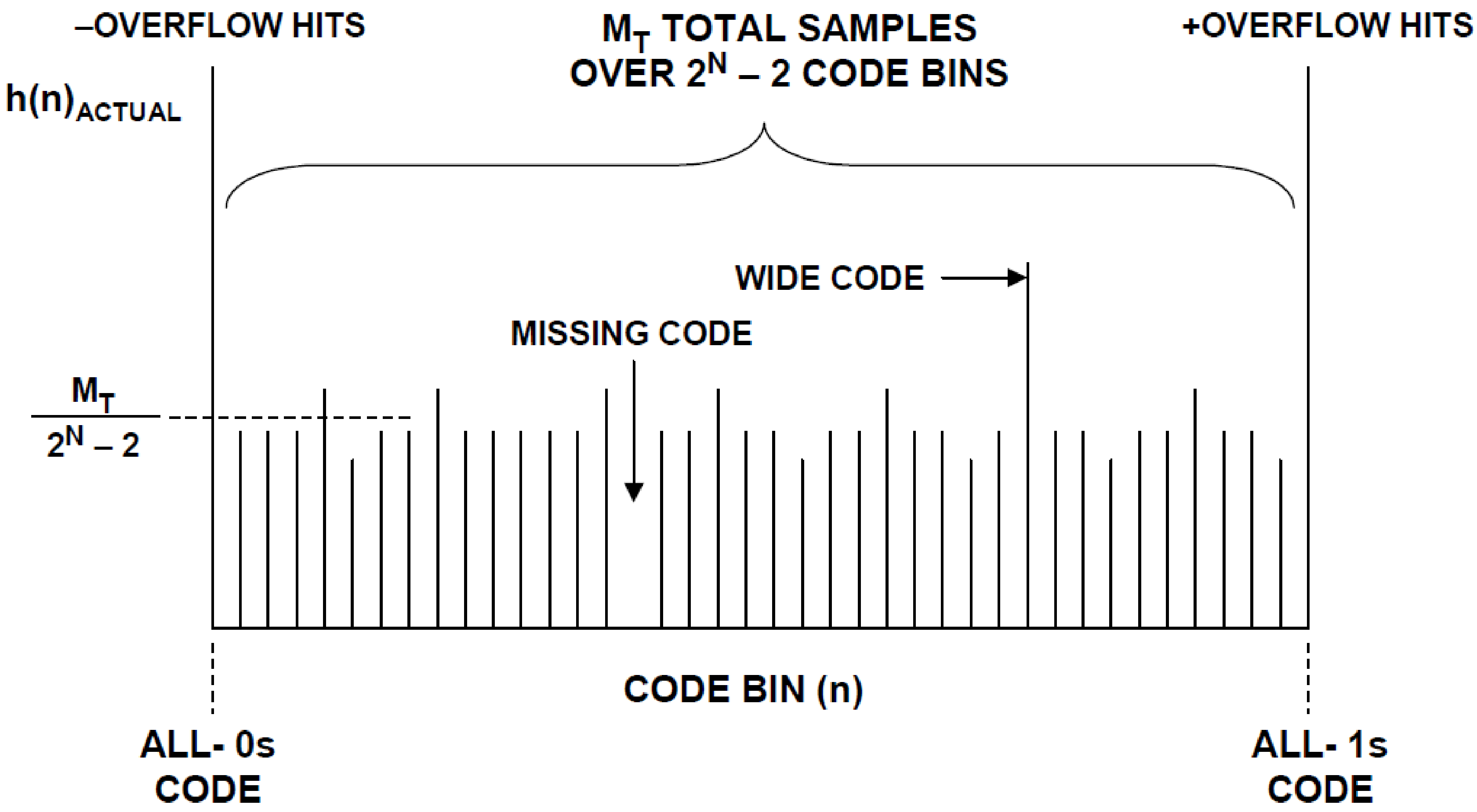
$$DNL(n) = \frac{h(n)_{ACTUAL}}{h(n)_{THEORETICAL}} - 1$$

- Integrate DNL to obtain INL

[W. Kester, ADI, 2005]

Histogram (Code Density) Test

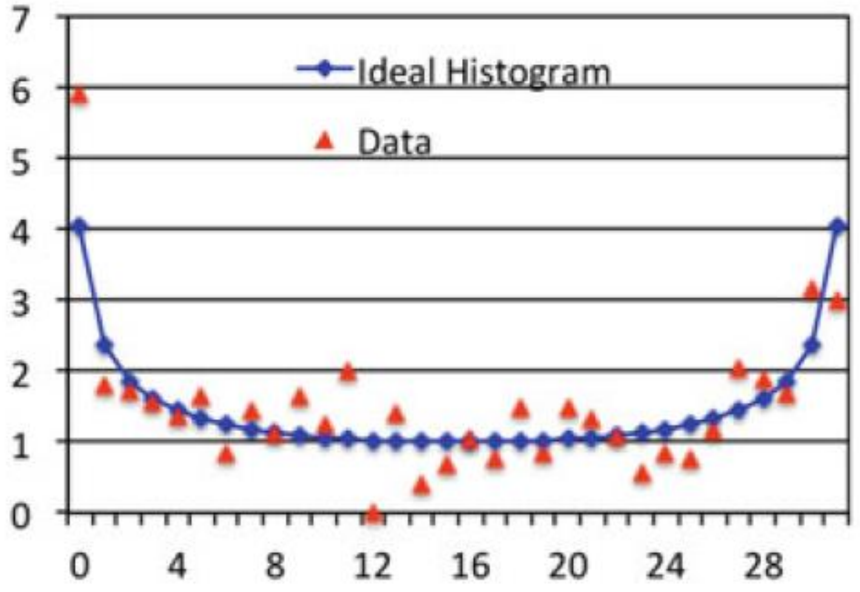
- Overflow hits in all 0s and all 1s bins are discarded

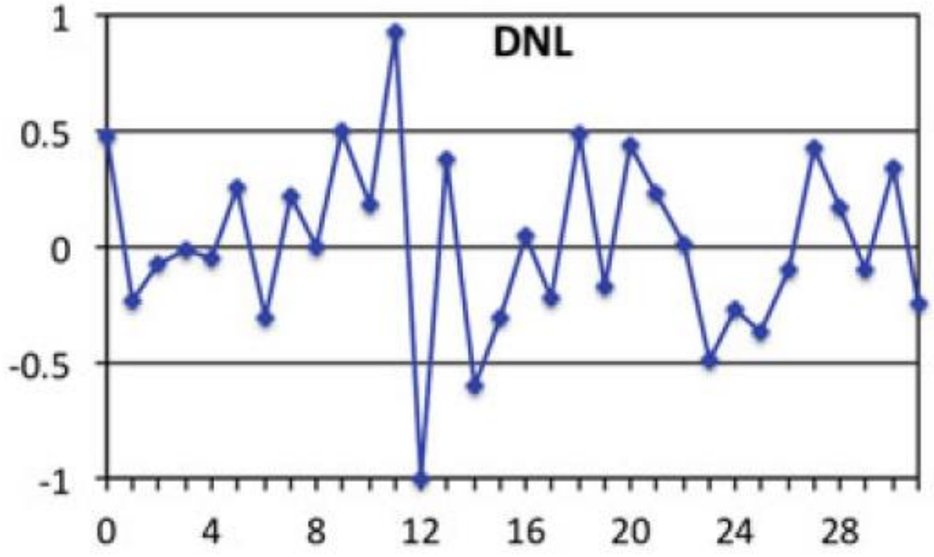


[W. Kester, ADI, 2005]

Sine Wave Histogram Test

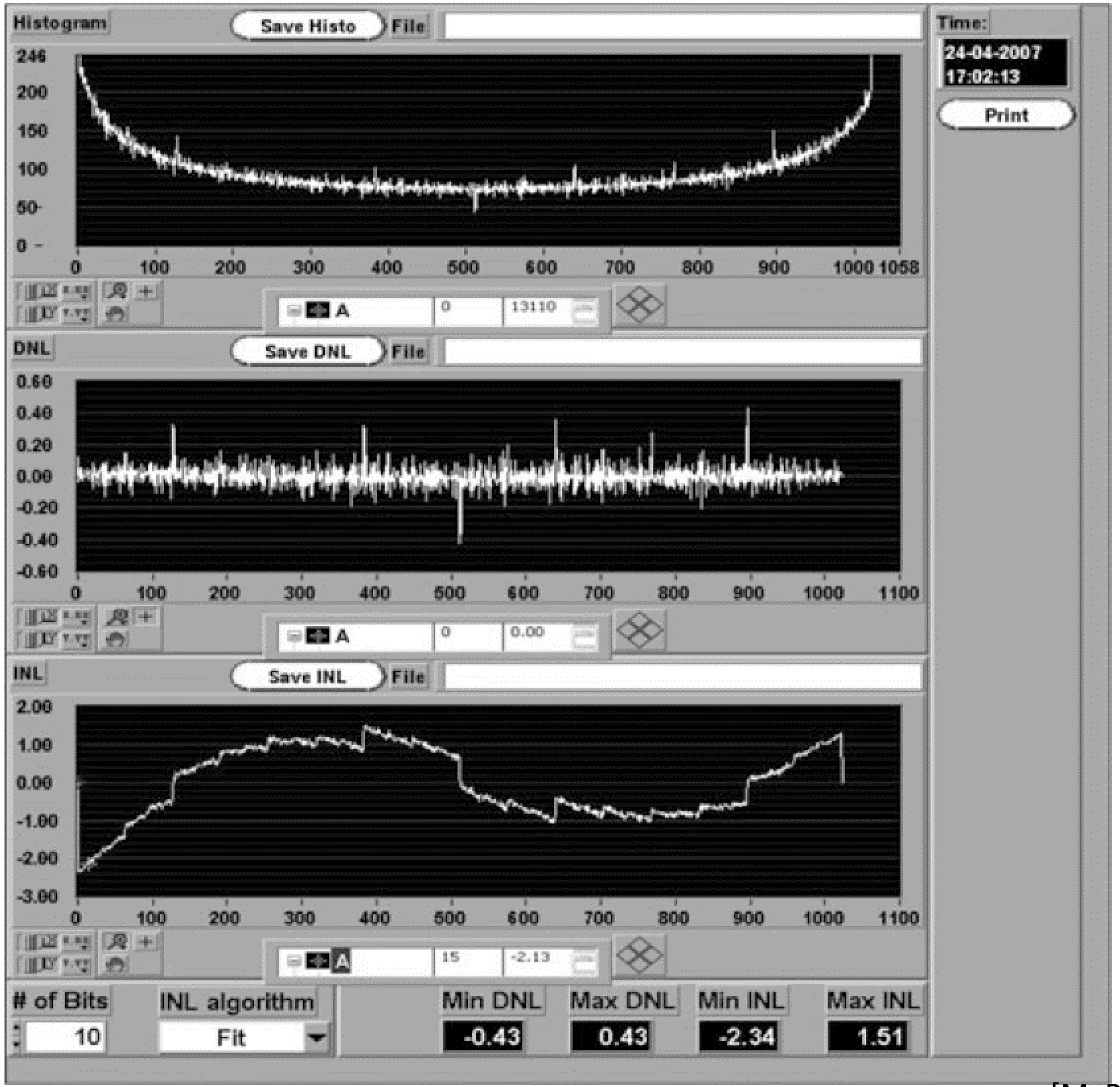
- Sinewaves can be generated with extremely high linearity and low noise with appropriate filtering
- Currently, the standard and most popular method to measure ADC static characteristics





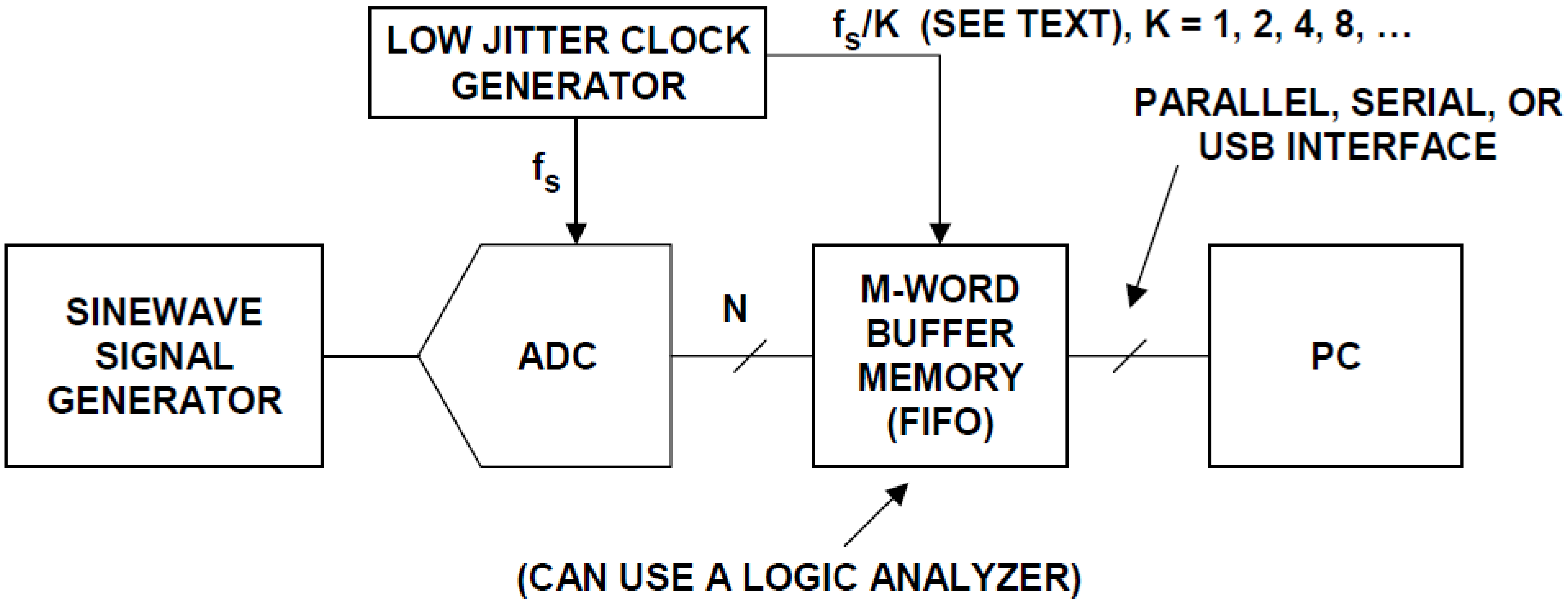
[M. Pelgrom, 2017]

Sine Wave Histogram Test Example



[M. Pelgrom, 2017]

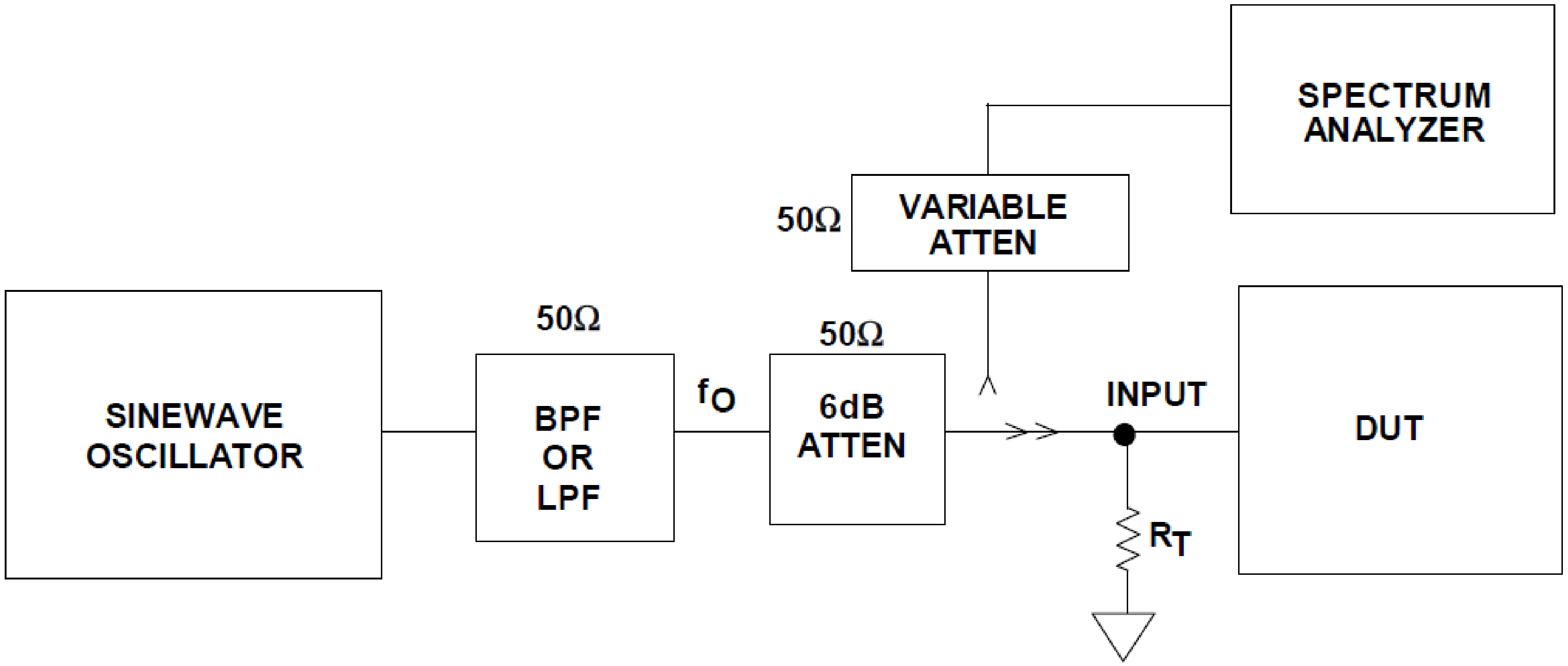
ADC Dynamic Testing



[W. Kester, ADI, 2005]

Generating Low Distortion Single Tone

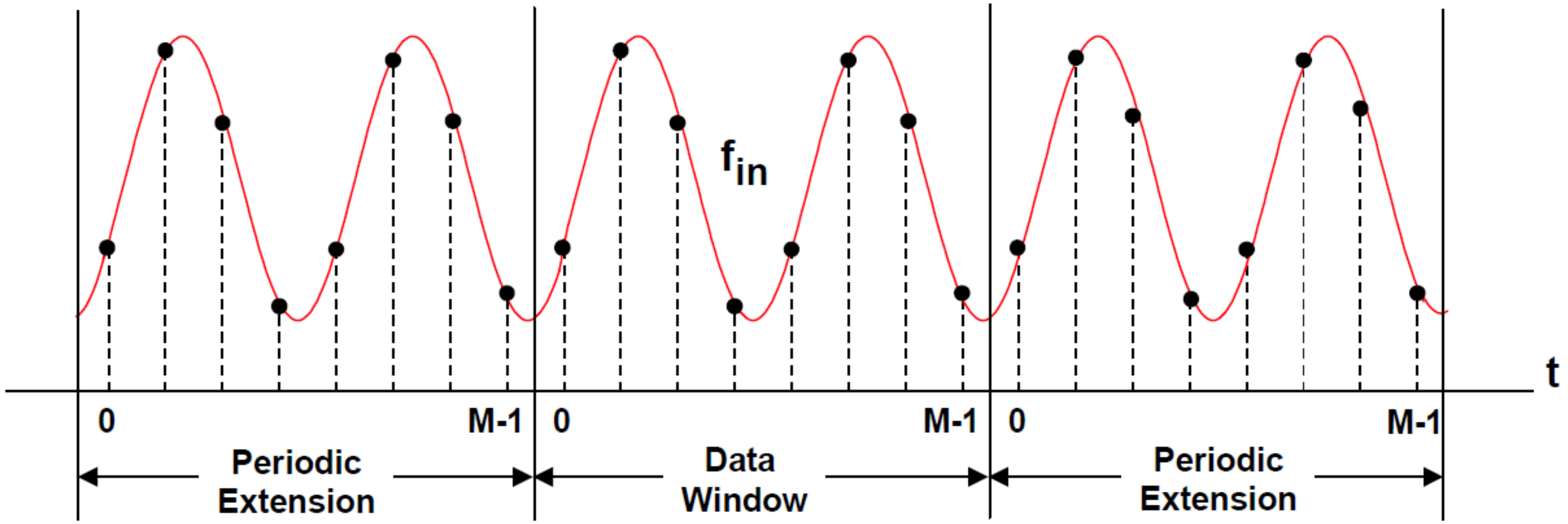
- BPF or LPF is necessary to remove harmonics (Ex: tte.com)
- The input tone distortion should be 10 dB lower than the desired accuracy of the measurement
- R_T is selected so that the parallel combination of RT and the input impedance of the DUT is $50\ \Omega$



[W. Kester, ADI, 2005]

DTFS (DTFT) and FFT

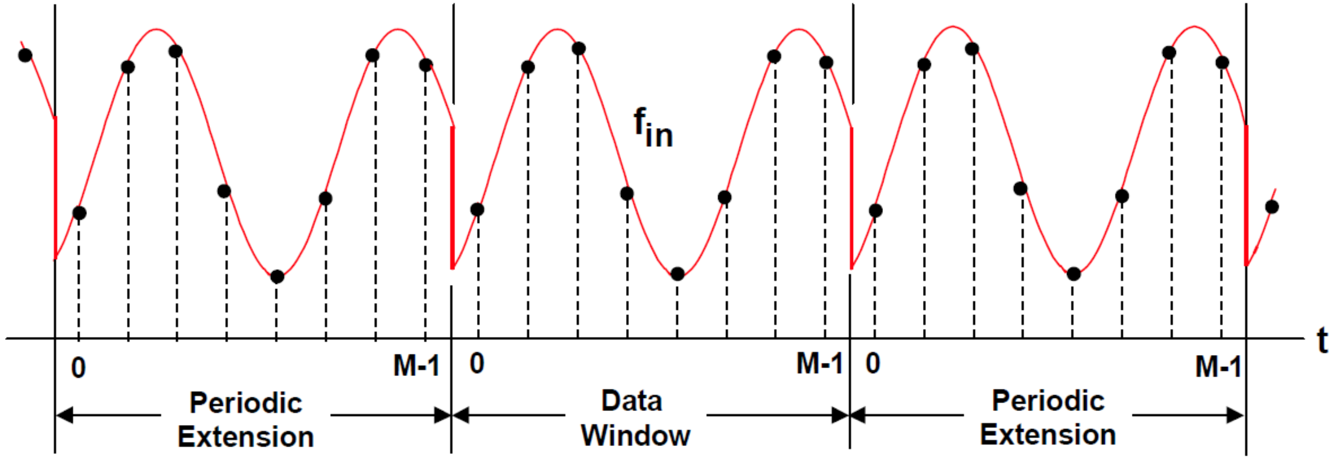
- The DFT Operates on a Finite Number (M) of Digitized Time Samples
- When These Samples are Repeated and Placed “End-to-End”, they Appear Periodic to the Transform
- Practically, Fast Fourier Transform (FFT) is used to compute DFT
- The FFT is simply an algorithm that reduces the required number of mathematical computations

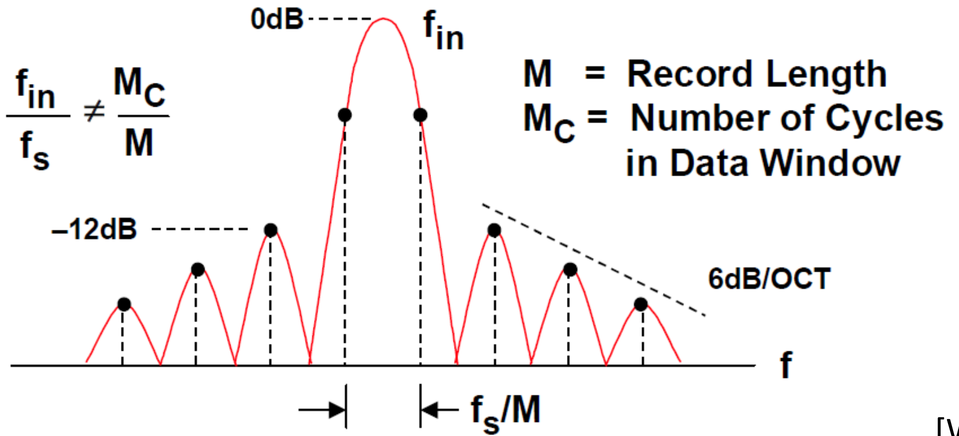


[W. Kester, ADI, 2005]

Spectral Leakage

- The discontinuities at endpoints result in "spectral leakage"
- Equivalent to multiplying the input sinewave by a rectangular window pulse which has the familiar sin(x)/x frequency response



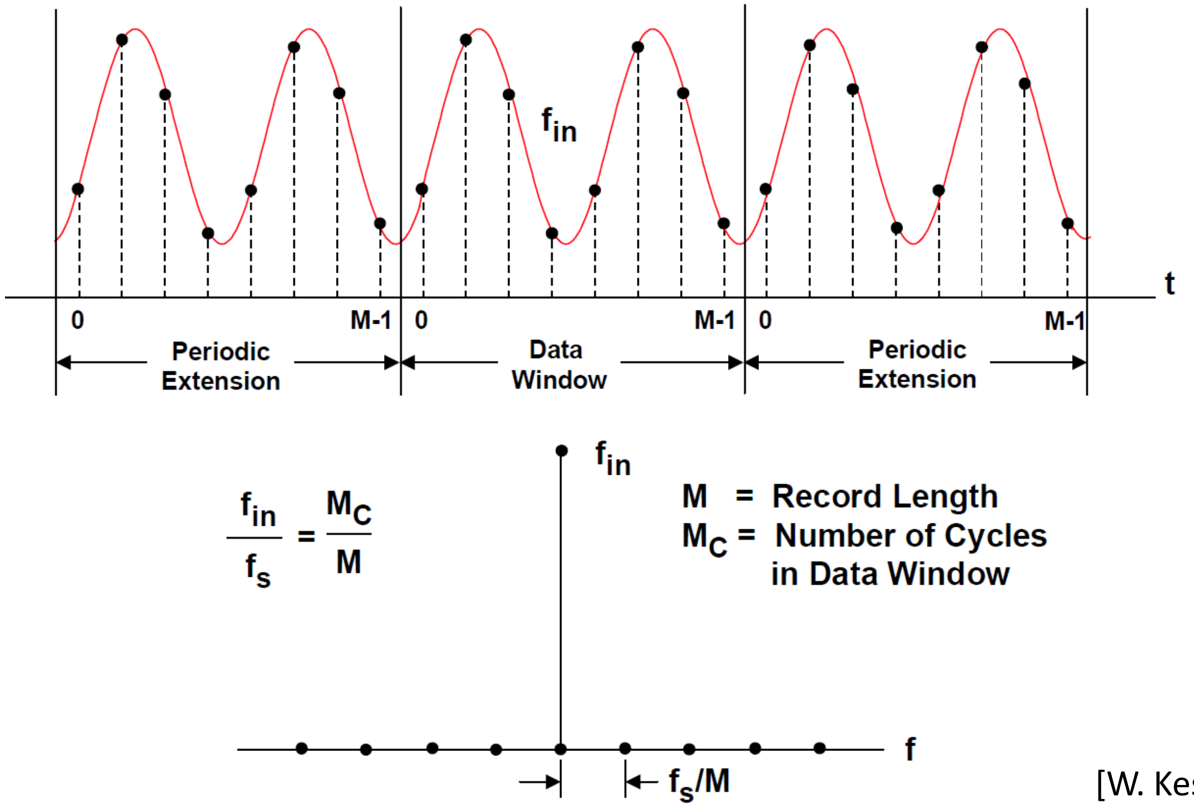


[W. Kester, ADI, 2005]

Coherent Testing Condition

$$T_{measure} = M \times T_s = M_C \times T_{in} \rightarrow \frac{f_s}{f_{in}} = \frac{M}{M_C}$$

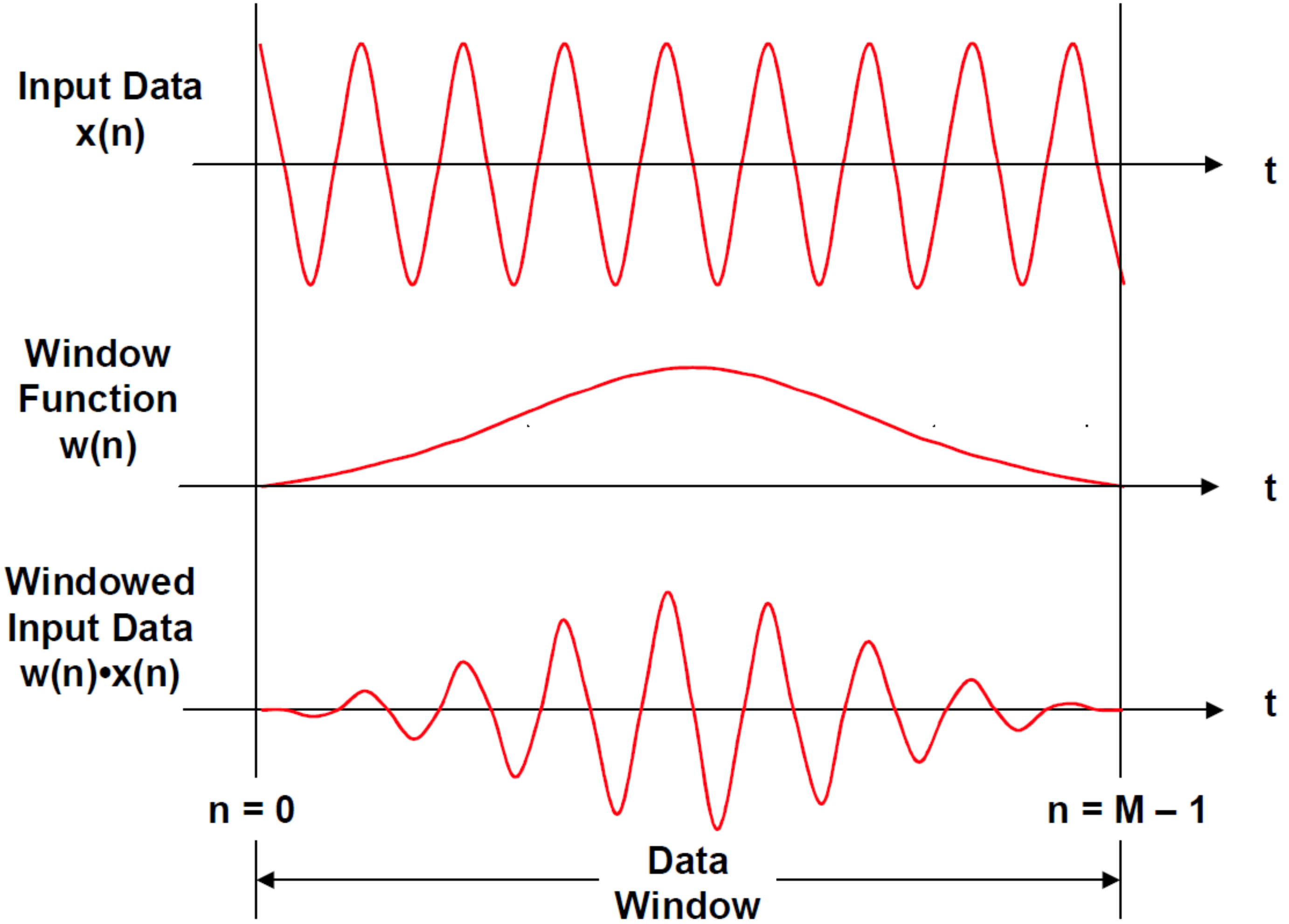
- M should be a power of 2 (to speed up FFT computation)
- M_C must be integer to avoid spectral leakage
- M and M_C must be mutually prime: gcd(M, M_C) = 1 ➔ Make M_C odd



[W. Kester, ADI, 2005]

Windowing for Non-Coherent Testing

- Windowing mitigates spectral leakage for arbitrary input tone
  - Coherent testing condition does not have to be strictly satisfied

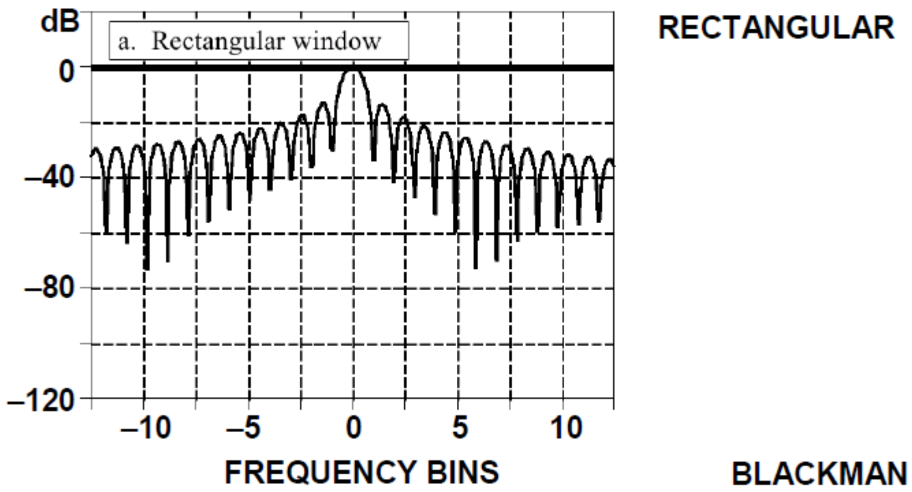


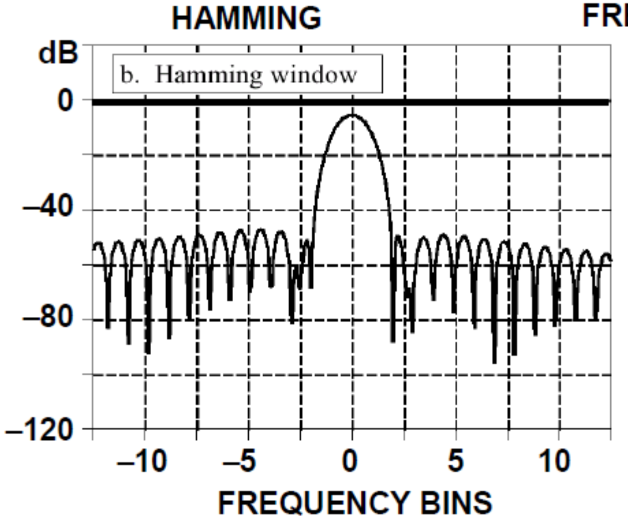
[W. Kester, ADI, 2005]

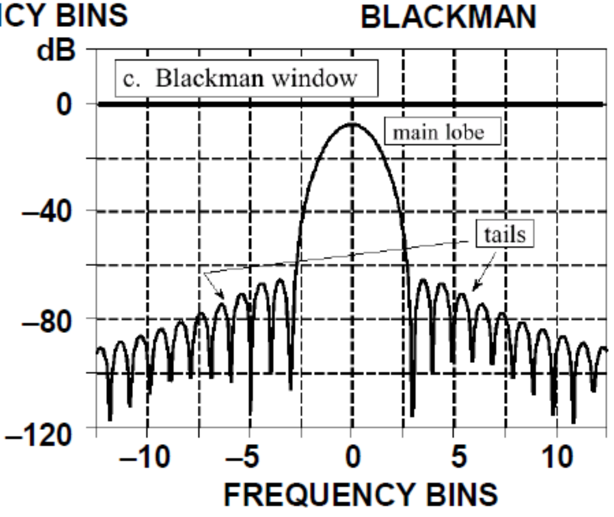
Window Functions Example (M=256)

- Multiplication in time domain = Convolution in frequency domain
  - The window is modulated by the tone (frequency shifting)

$$\text{BIN WIDTH} = \frac{f_s}{M}$$







[W. Kester, ADI, 2005]

Window Functions Comparison

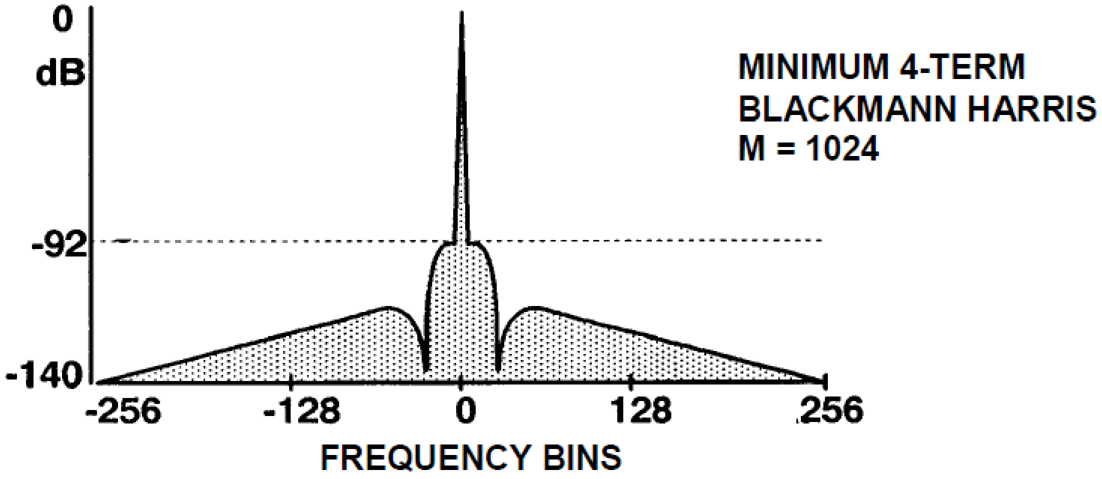
- Tradeoff between main-lobe spreading and side-lobe rejection

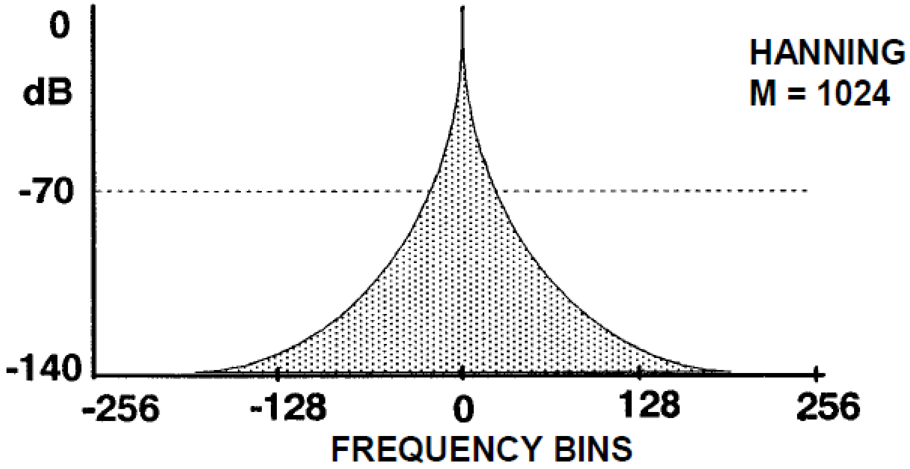
WINDOW FUNCTION	3dB BW (Bins)	6dB BW (Bins)	HIGHEST SIDELOBE (dB)	SIDELOBE ROLLOFF (dB/Octave)
Rectangle	0.89	1.21	–12	6
Hamming	1.3	1.81	– 43	6
Blackman	1.68	2.35	–58	18
Hanning	1.44	2.00	–32	18
Minimum 4-Term Blackman-Harris	1.90	2.72	–92	6

[W. Kester, ADI, 2005]

Popular Window Functions

- Tradeoff between main-lobe spreading and side-lobe rejection

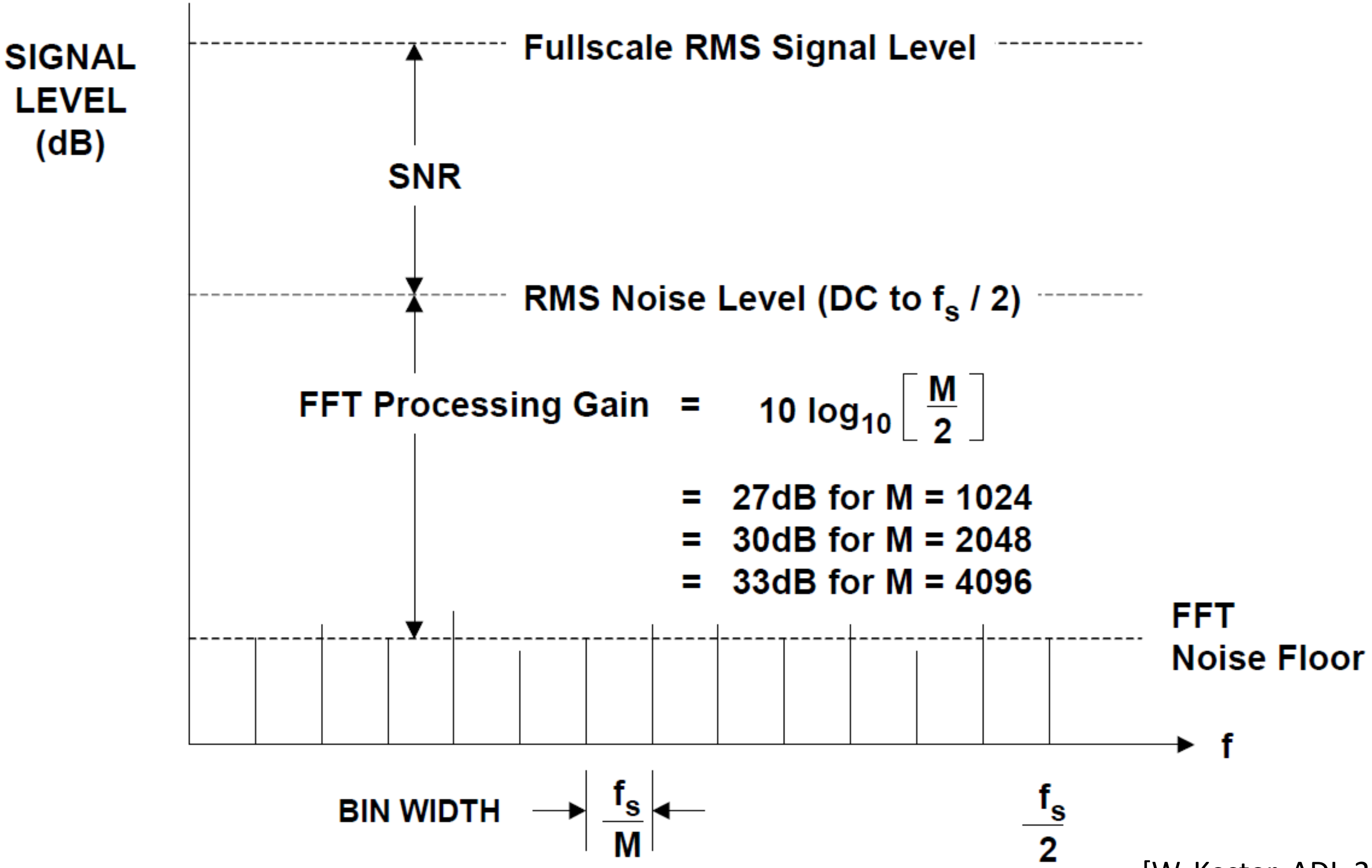




[W. Kester, ADI, 2005]

FFT Processing Gain

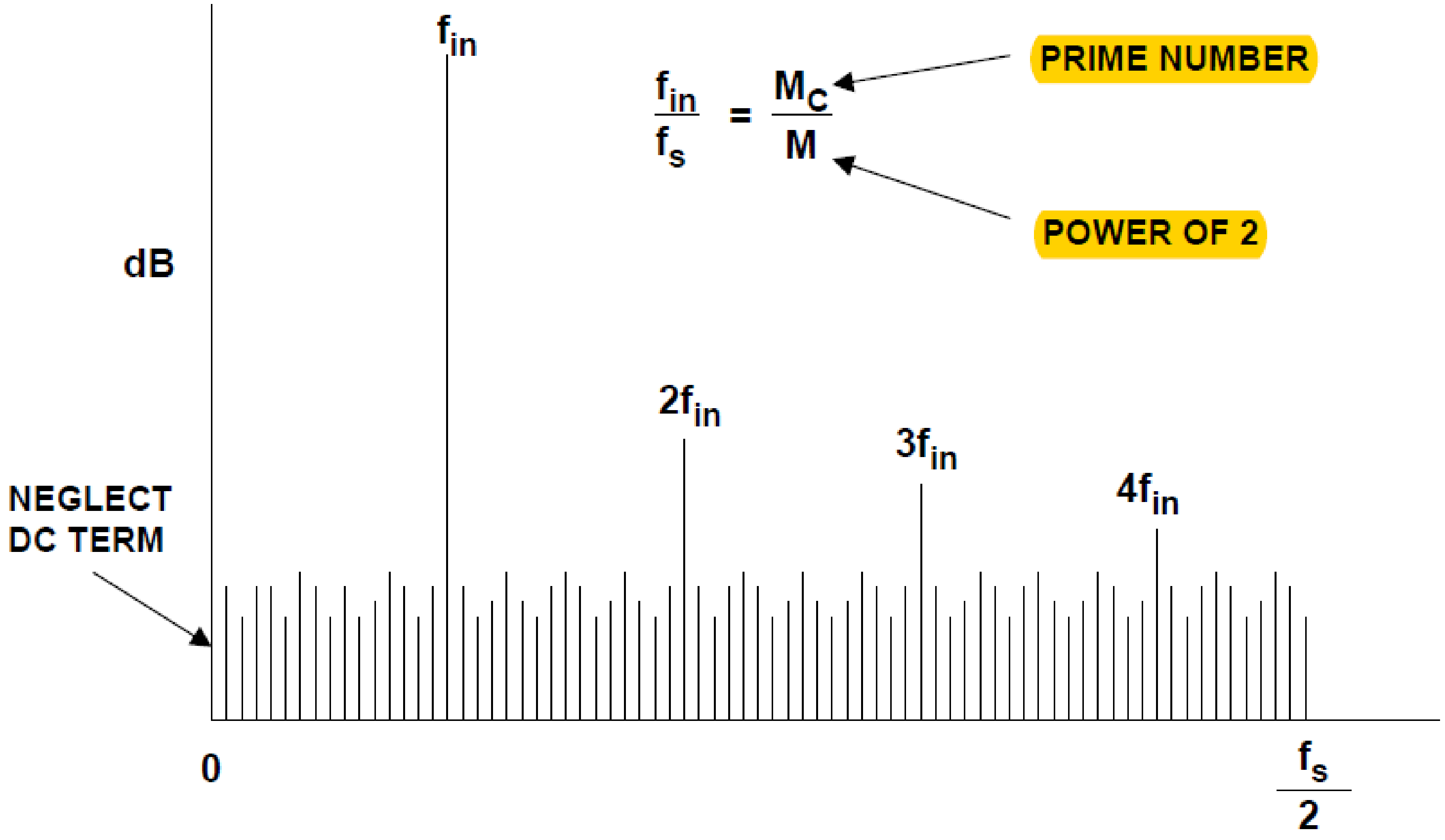
- Increasing no. of bins (FFT points) reduces noise floor
  - Area = noise power = $M/2 \times Noise\ Floor$ = constant



[W. Kester, ADI, 2005]

FFT Output for Coherent Testing

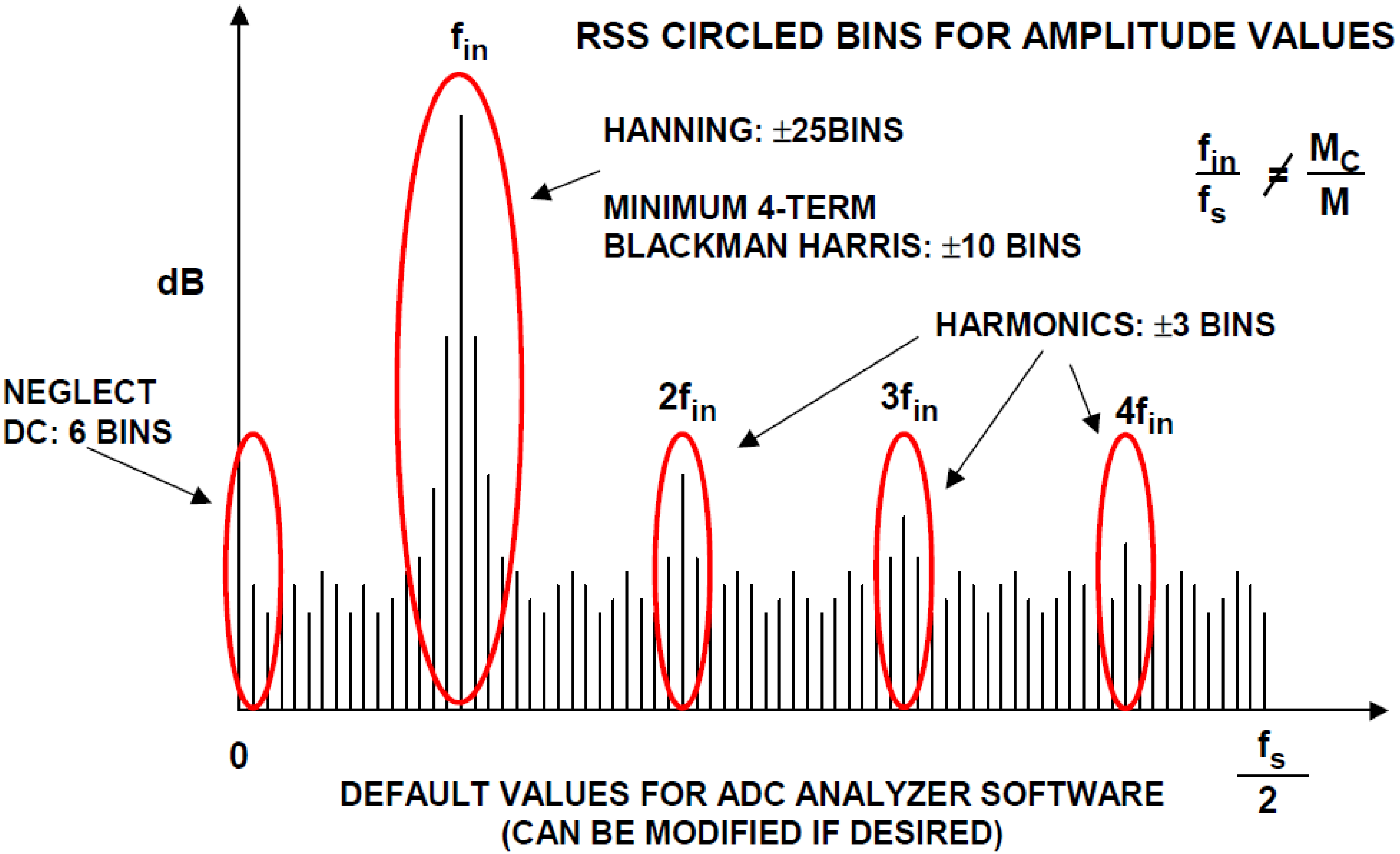
- The fundamental and the harmonics fall in single bins
- f_s and f_{in} should be generated from locked frequency synthesizers in order to maintain the exact relationship



[W. Kester, ADI, 2005]

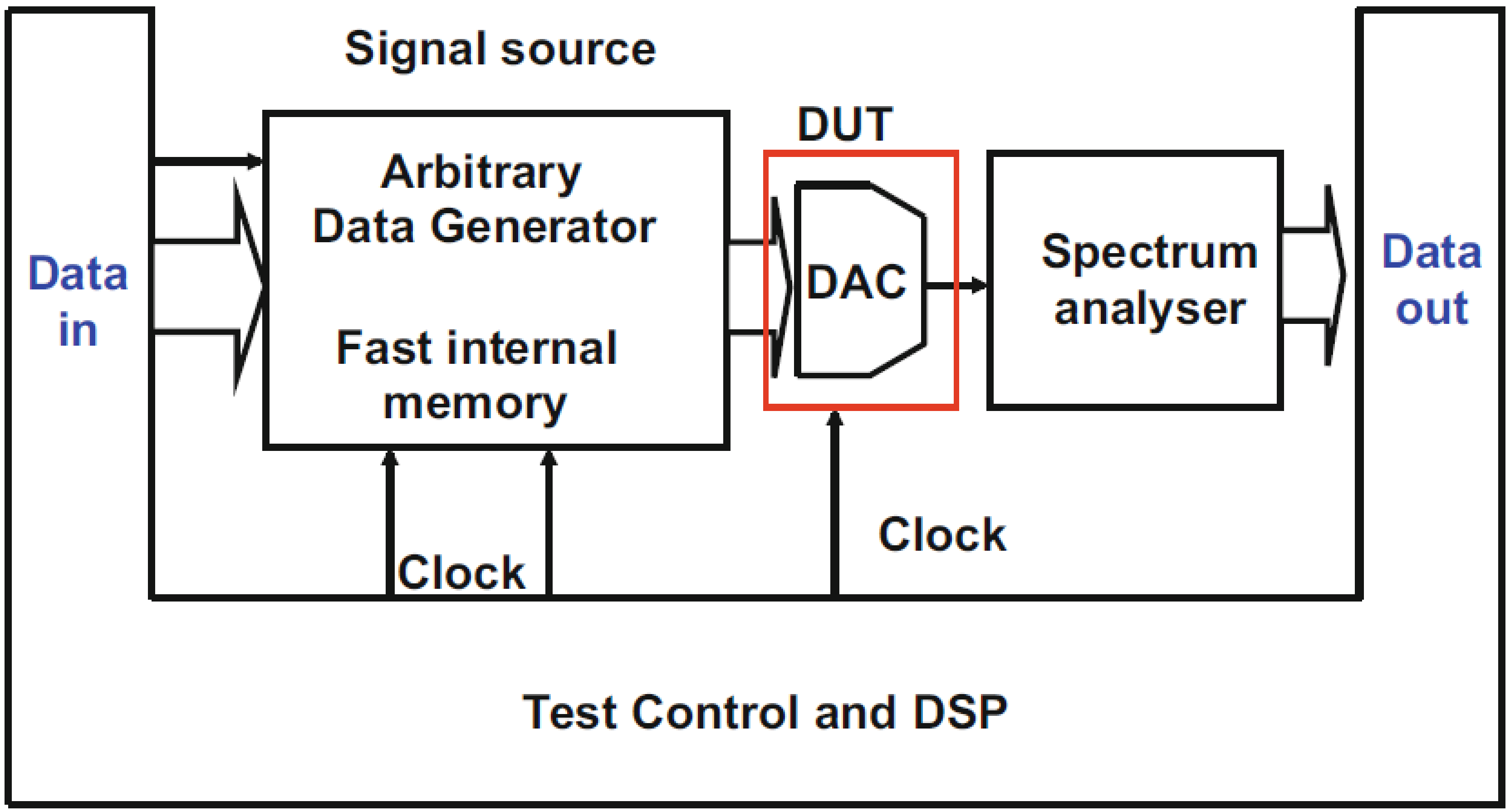
FFT Output for Non-Coherent Testing

- Fundamentals and harmonics leak according to the window used
- Do NOT count leakage bins as noise!



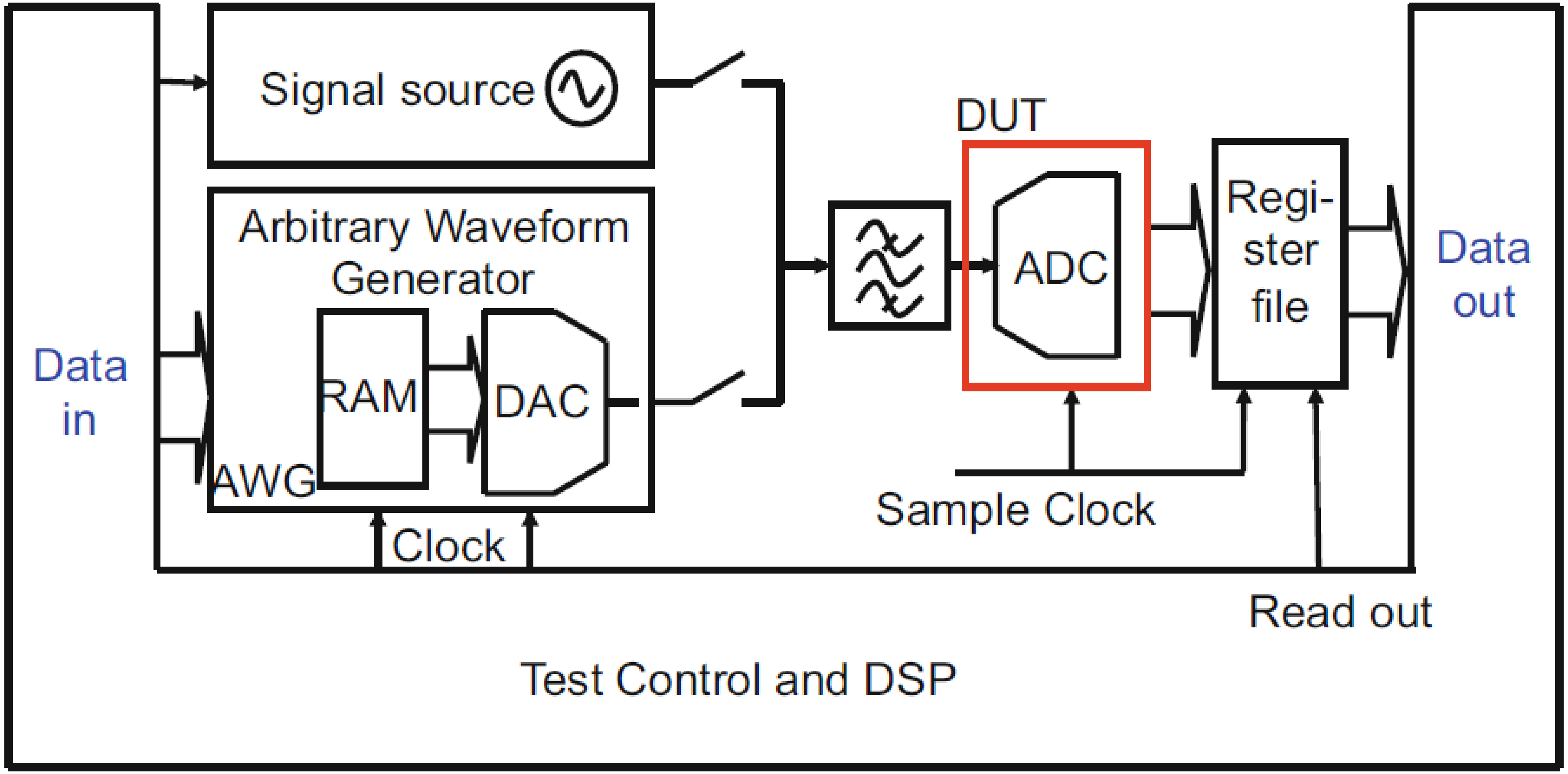
[W. Kester, ADI, 2005]

DAC Test Setup



[M. Pelgrom, 2017]

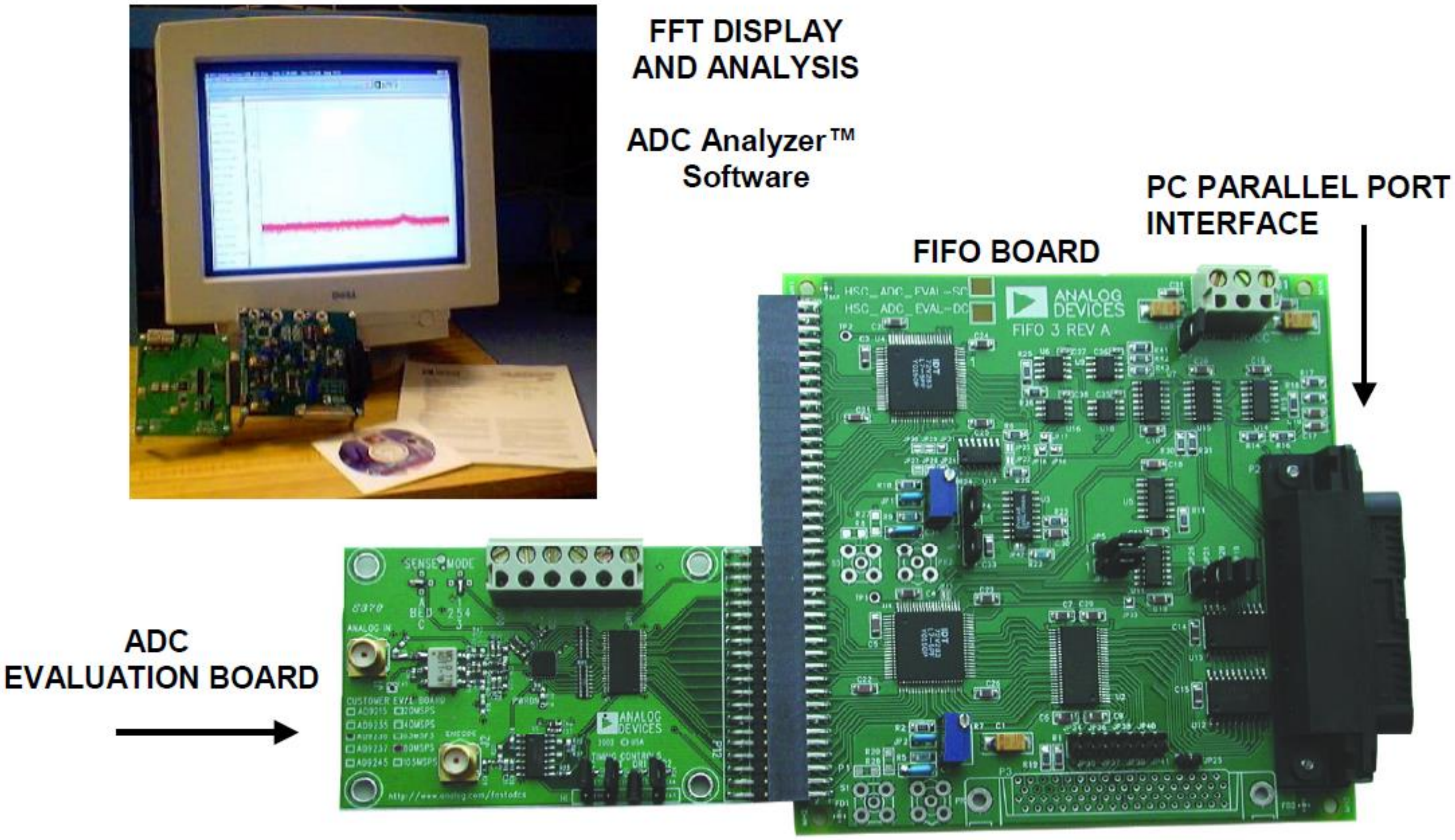
ADC Test Setup Example



[M. Pelgrom, 2017]

Evaluation Boards

- Evaluation boards and software from manufacturers are very valuable resources.



[W. Kester, ADI, 2005]

Test PCB Design Hints

- **Use (and learn from) manufacturers evaluation boards.**
- Analog and digital supplies should be separated except at a single node
- Add decoupling caps at different ranges (Ex: $10\ \mu F\ and\ 100\ nF$)
- Add $100\ nF$ cap as close as possible to every supply pin
- Proper grounding
- Proper termination of signal with fast rise/fall time
- For signals with fast rise/fall time every wire is a transmission line

References

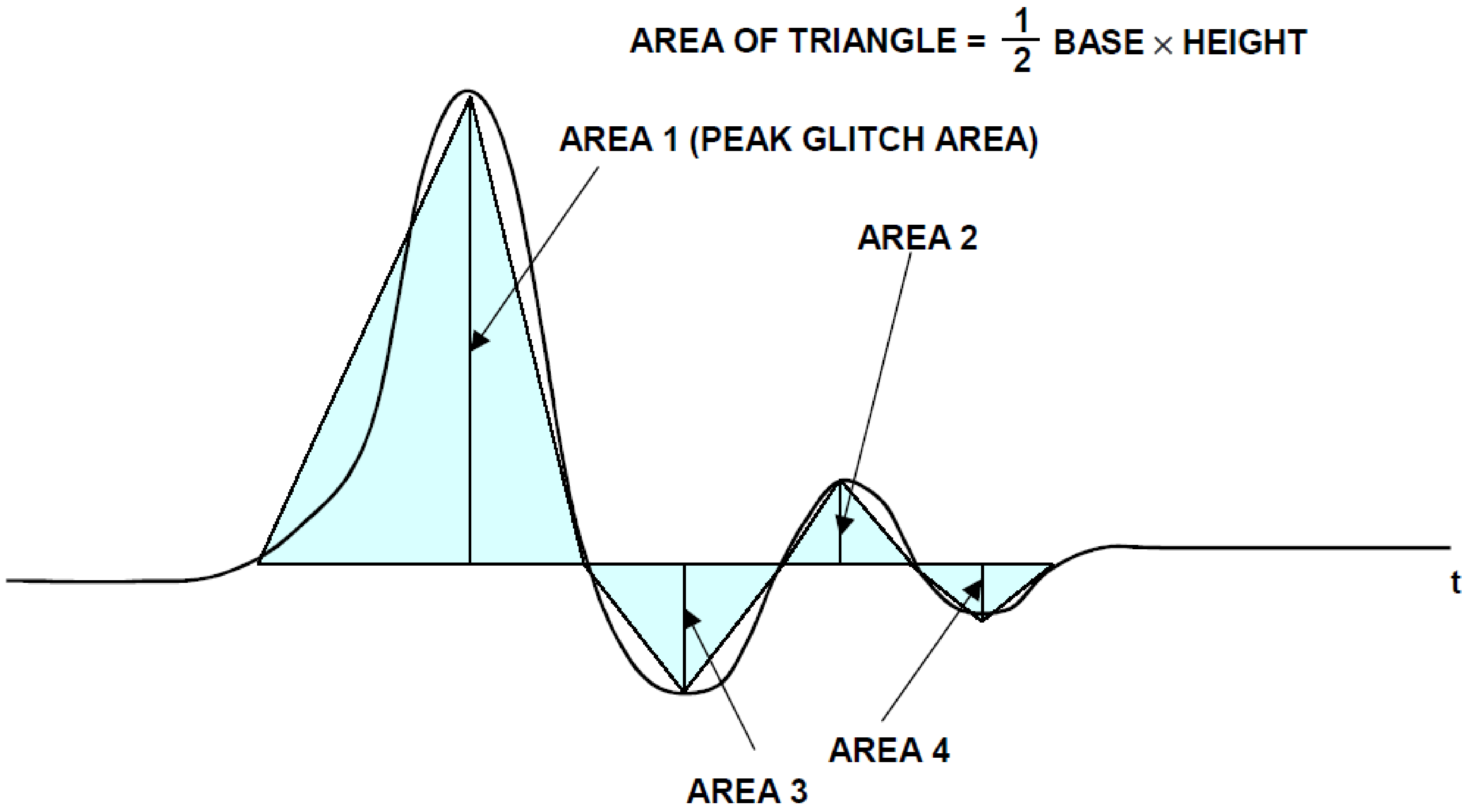
- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- W. Kester, The Data Conversion Handbook, ADI, Newnes, 2005.
- B. Boser and H. Khorramabadi, EECS 247 (previously EECS 240), Berkeley.
- B. Murmann, EE 315, Stanford.
- Y. Chiu, EECT 7327, UTD.

Course Resources

Lectures	Labs	YouTube Channel

Thank you!

DAC Glitch Impulse Area

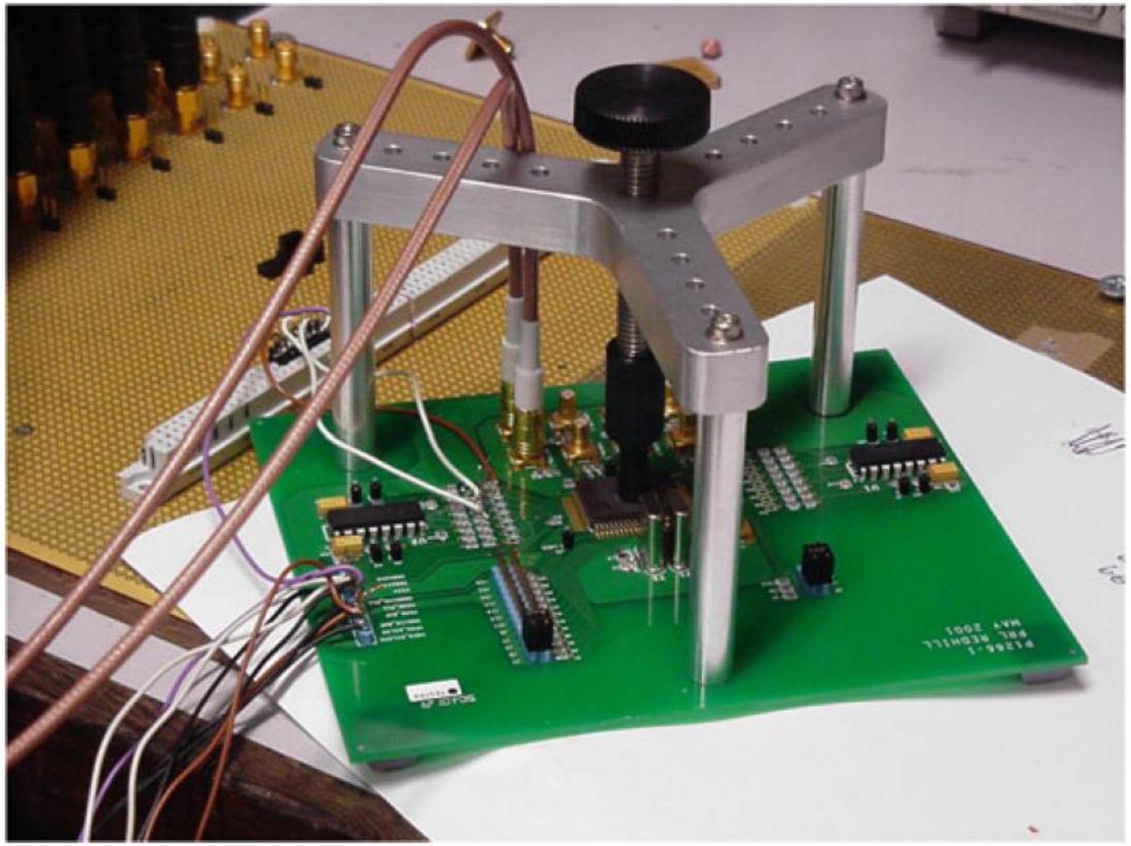


$$\text{NET GLITCH IMPULSE AREA} \approx \text{AREA 1} + \text{AREA 2} - \text{AREA 3} - \text{AREA 4}$$

[W. Kester, ADI, 2005]

Test Setup Example

- The tool below allows to exchange the samples easily
- The chip is pushed onto the connection electrodes of the printed-circuit card without socket parasitics



[M. Pelgrom, 2017]