وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – EECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

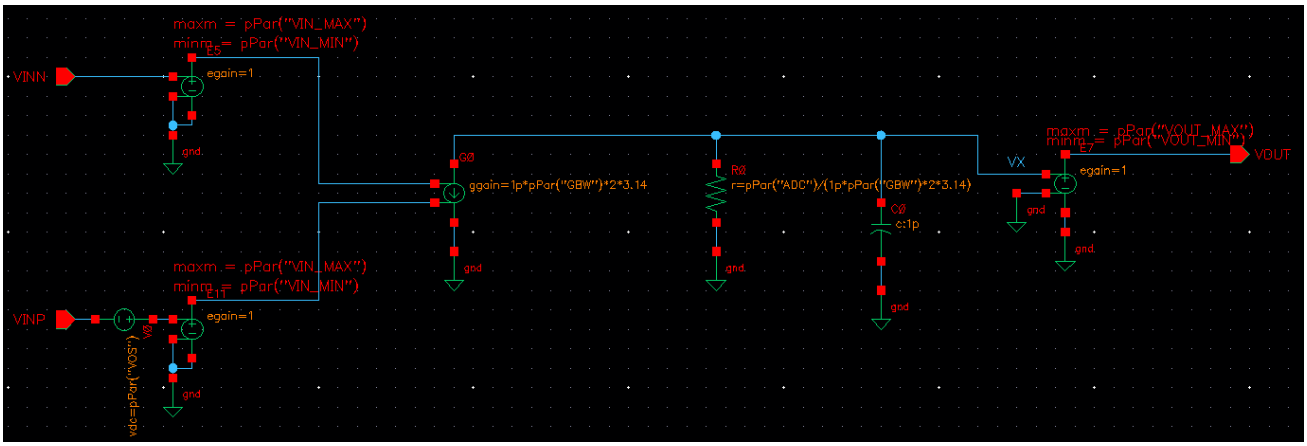
Analog Integrated System Design – Cadence Tools
Lab 06
Capacitive Digital-to-Analog Converter

Intended Learning Objectives

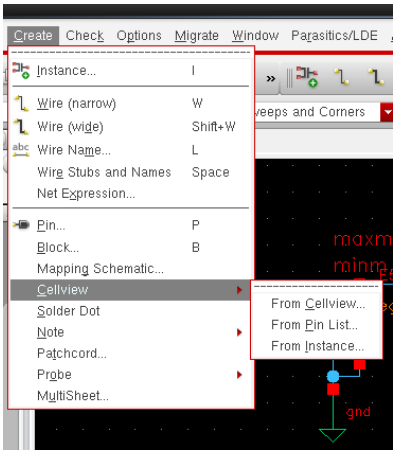
1) To be able to model an op-amp with different types of imperfection.
2) To be familiar with the simulation and characterization of digital-to-analog converters.
3) To be familiar with the operation of capacitive DACs.

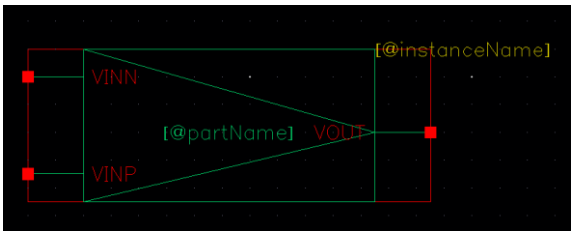
PART 1: Single-ended Output Op-amp Behavioral Model

1) Create the schematic shown below to model a single-ended output op-amp with finite gain, finite input range, finite output range, and finite GBW. Use vccs and vcvs from analogLib.

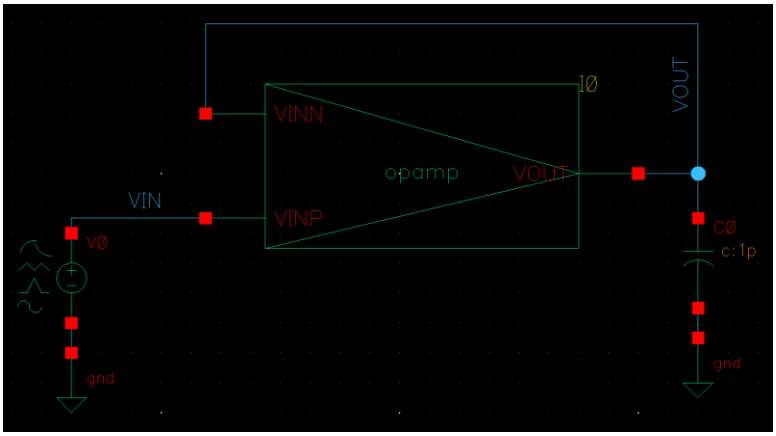


2) Create a new symbol.





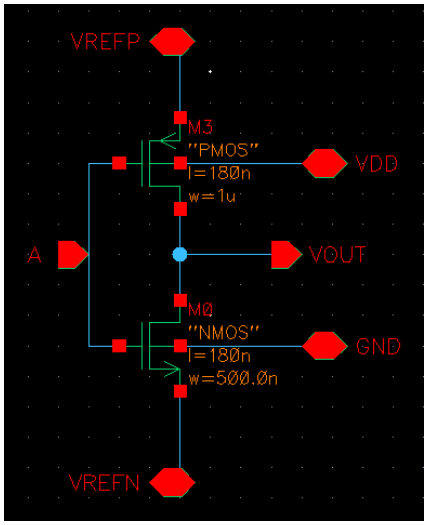
3) Create a simple testbench to verify your op-amp. An example testbench is shown below. Set the input as a sinusoidal signal (FIN, VDC, VPK). Run transient analysis for 4/VAR("FIN") conservative (four input cycles). You may develop more testbenches to verify input/output limiting, offset voltage, etc.

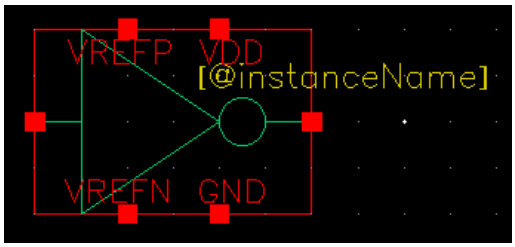


Parameter	Value	Comments
VDD	2	Use VDD = 1.2 for 130nm tech
FIN	1k, GBW	Parametric sweep (list)
VDC	VDD/2	
VPK	VDD/4	
VIN_MAX	VDD-0.2	
VIN_MIN	0.2	
VOUT_MAX	VDD-0.2	
VOUT_MIN	0.2	
ADC	1e5	DC gain
GBW	10M	
VOS	0	Offset voltage

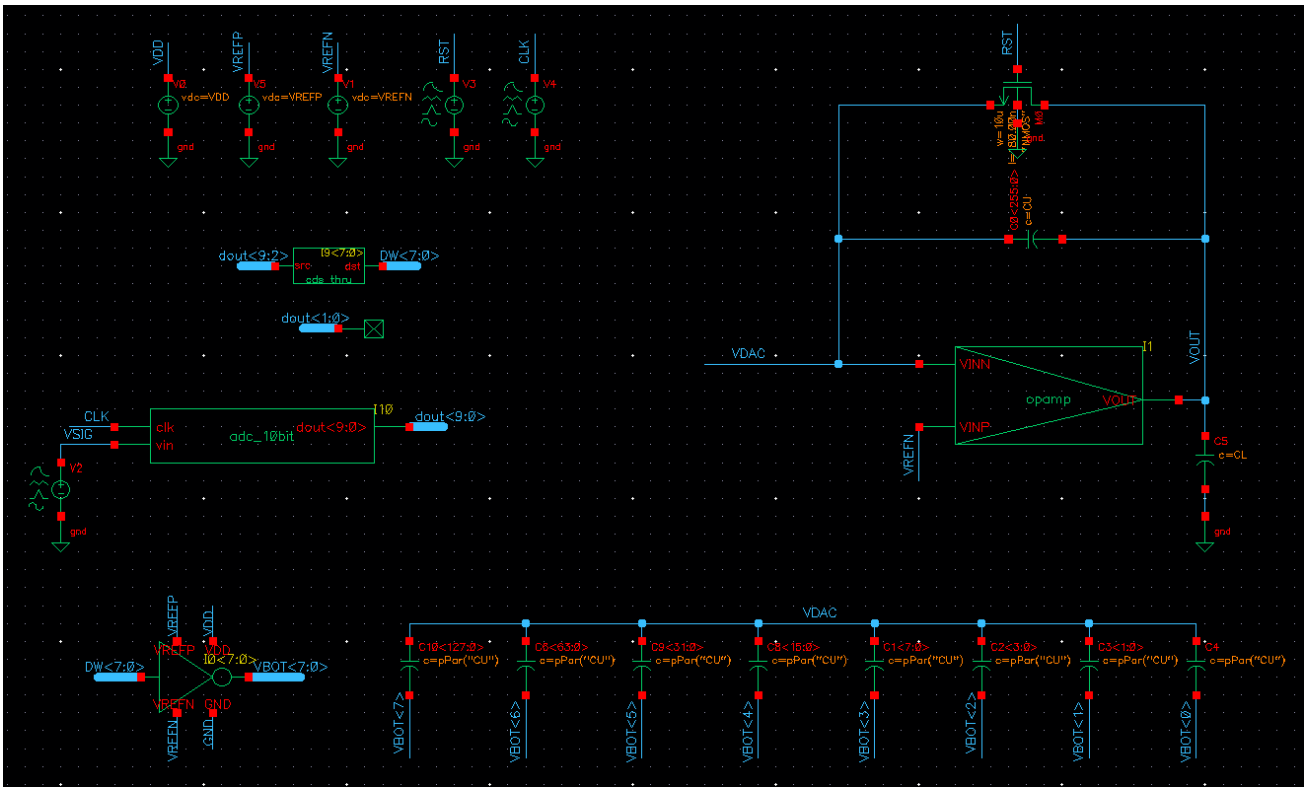
PART 2: Capacitive DAC (Ramp Test)

1) Create a schematic for a bottom plate switch. It is similar to a digital inverter, but the bottom and top rails are defined by VREFN and VREFP instead of GND and VDD.





2) Create the schematic of the capacitive DAC shown below. Use cds_thru from basic library as a jumper to connect nets with different names. Use the Verilog-A ADC that you designed in Lab 02. Note that several elements of the schematic (including basic -> noConn) are defined as an array of elements. The feedback capacitance is also defined as an array of 2^N elements.

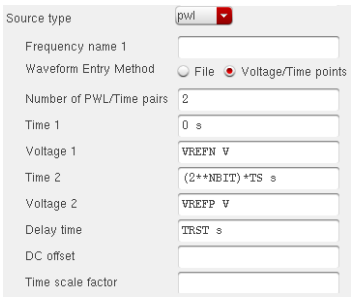


3) Set sources (RST and CLK) as shown below.

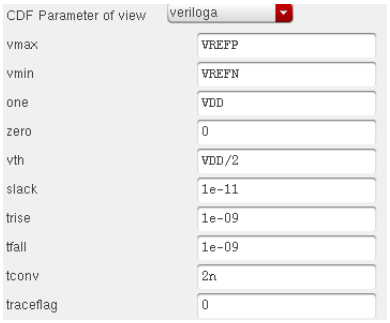
	RST	CLK
Type	Pulse	Pulse

Initial value	0	0
Pulse value	VDD	VDD
Period	1	TS
Pulse width	TRST/2	TS/2
Delay	TRST/2	1.1*TS
Rise/fall time	TRF	TRF

4) Set VIN to perform a simple code ramp test as below.



5) Set ADC parameters as below. The ADC is used as a pattern generator, i.e., stimulus generator.

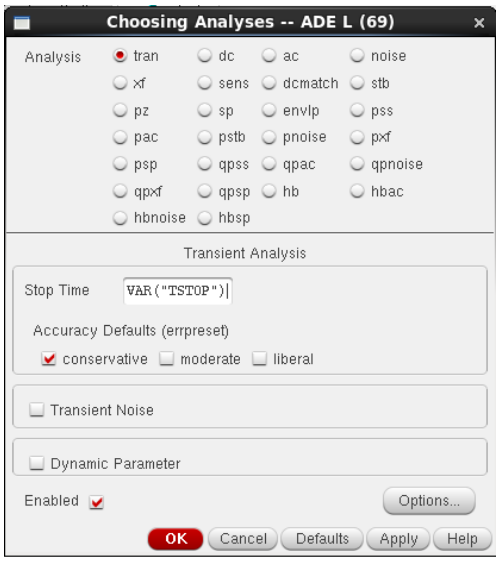


6) Set global variables as below.

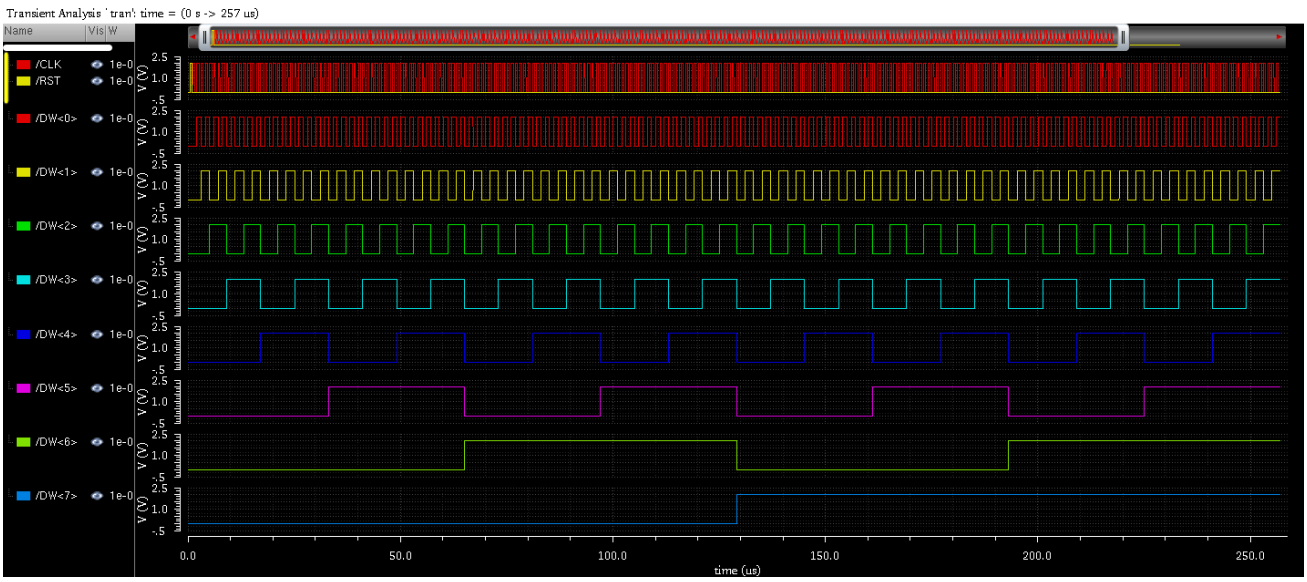
Parameter	Value
VDD	2
VIN_MAX	VDD-0.2
VIN_MIN	0.2
VOUT_MAX	VDD-0.2
VOUT_MIN	0.2
ADC	1e5
GBW	10M
VOS	0
CU	100f

TS	1u
TRF	1n
VREFN	0.25*VDD
VREFP	0.75*VDD
CP	CU
CL	1p
TRST	TS
NBIT	8
TSTOP	(2**NBIT + 1)*TS

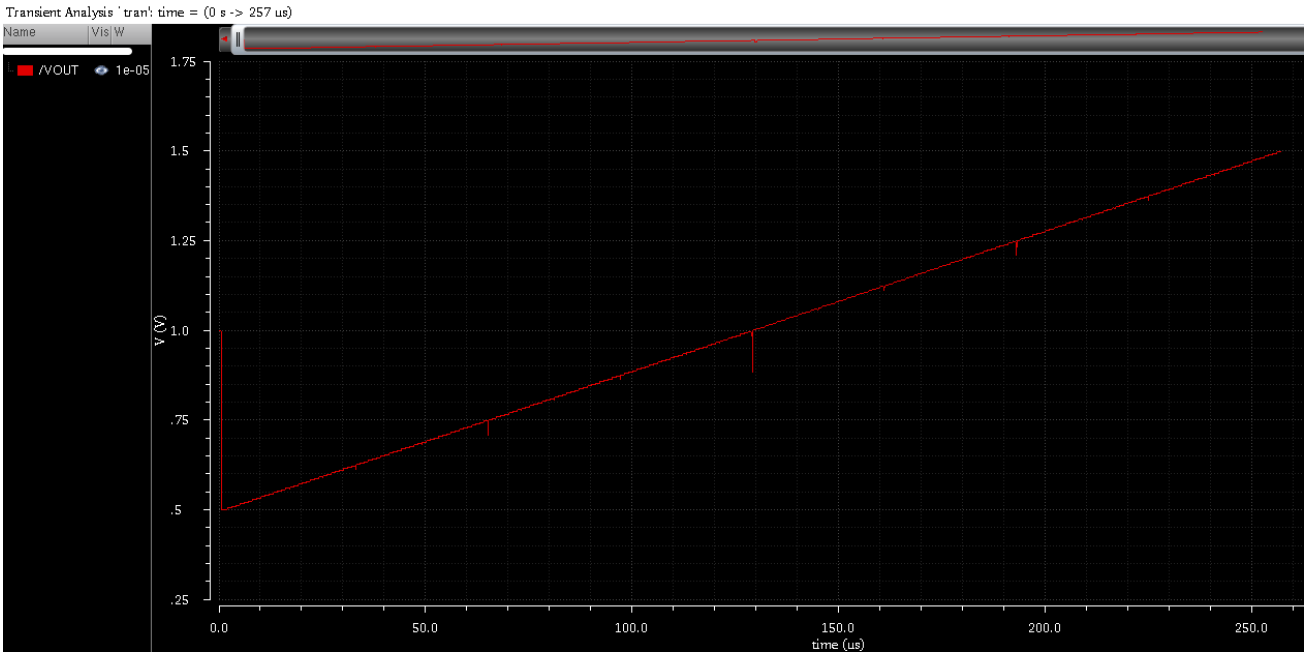
7) Set transient analysis as below.



8) Plot the transient waveforms and verify correct input stimulus.

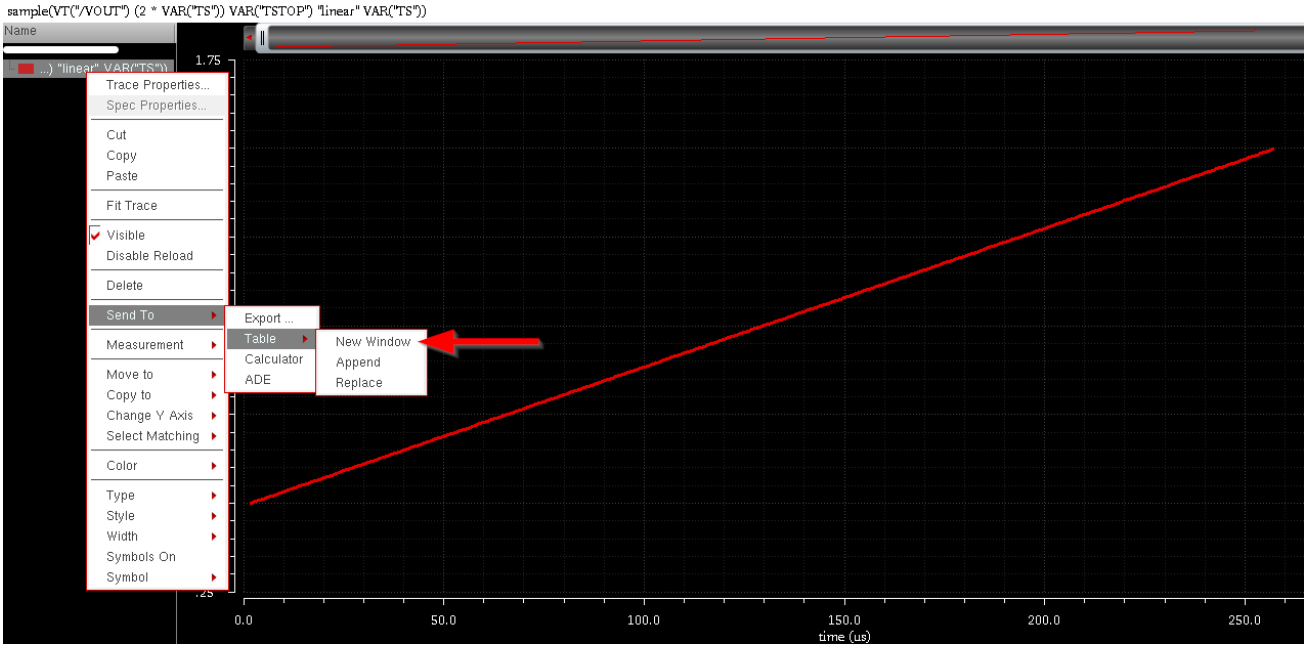


9) Plot DAC output and verify correct DAC operation. Observe the glitches in the DAC output.

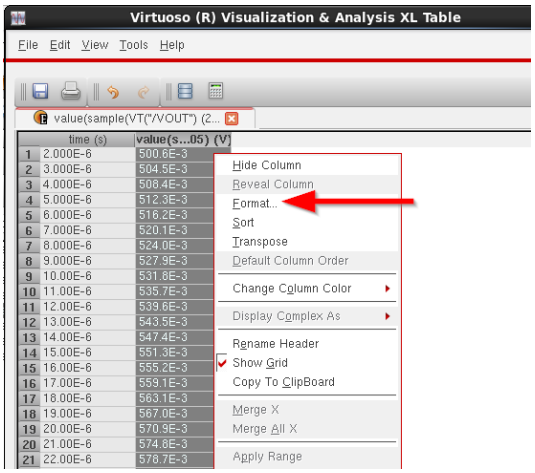


10) Sample the DAC output using the “sample” function in the calculator.
`sample(VT("/VOUT") (2 * VAR("TS")) VAR("TSTOP") "linear" VAR("TS"))`

11) Export the transfer function to a table.



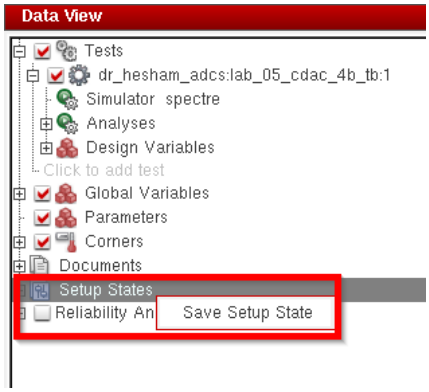
12) Change the precision of the numbers to 6 digits as shown below.



13) Copy the data to Excel or Matlab. Plot the DNL and the INL. An example Matlab code is shown below.

```
dvout = vout(2:end)-vout(1:end-1);
lsb = mean(dvout)
dnl = dvout/lsb - 1;
inl = cumsum(dnl)
subplot(211); plot(dnl); axis tight; ylabel('DNL (LSB)');
subplot(212); plot(inl); axis tight; ylabel('INL (LSB)');
```

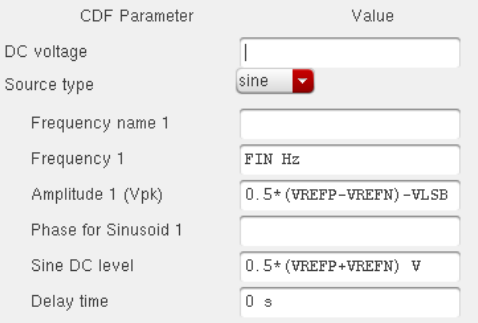
14) Save your setup state to “rampTest” before going to the next part.



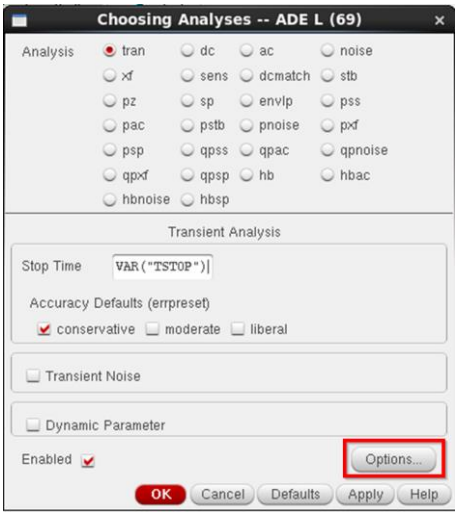
15) We want to intentionally add mismatch to see how it affects the DNL and INL. Add a capacitor = 0.2*CU parallel to the capacitors of bit7 and a capacitor = 0.1*CU parallel to the capacitors of bit6. Repeat the analysis and plot the DNL and INL. Explain the results.

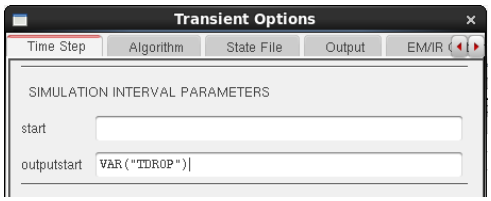
PART 3: Capacitive DAC (Sine Wave Test)

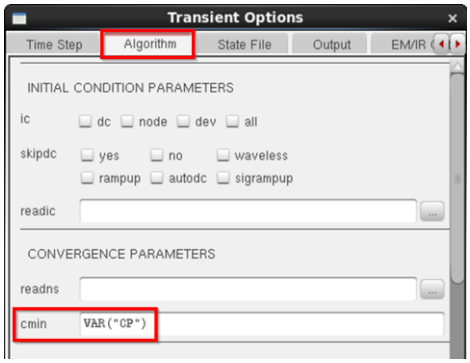
1) Modify the input signal source as below.



2) Modify the transient analysis settings as below. The “cmin” option install a minimum capacitance at every node to avoid convergence issues.





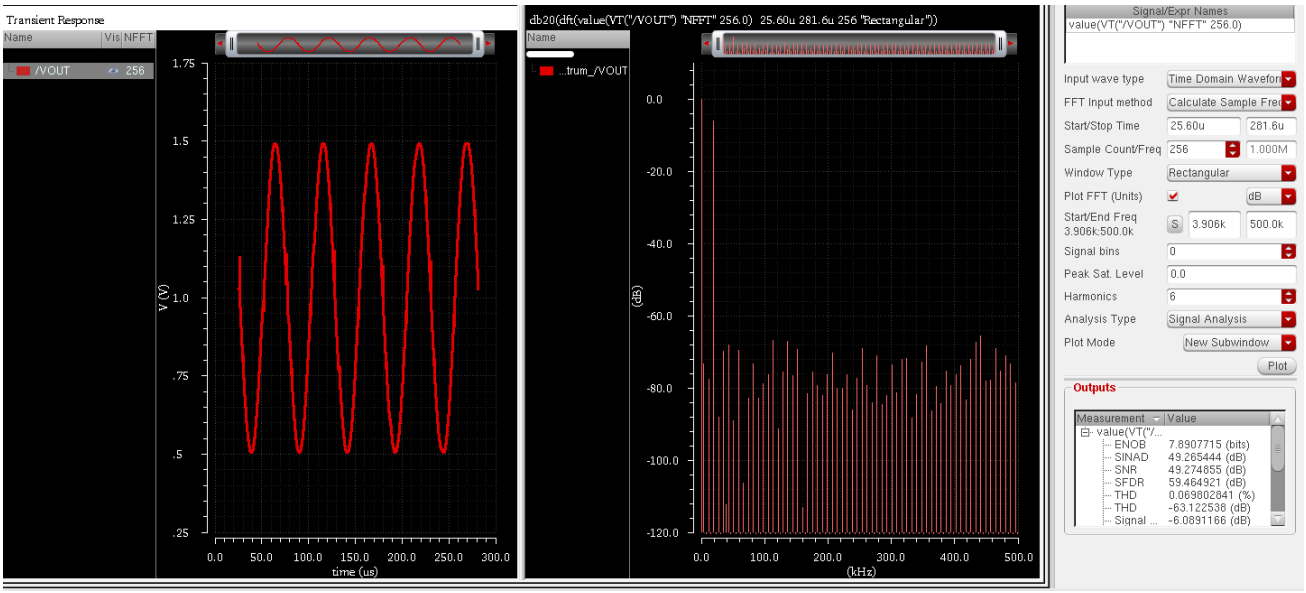


3) Set global variables as below.

Parameter	Value
VDD	2
VIN_MAX	VDD-0.2
VIN_MIN	0.2

VOUT_MAX	VDD-0.2
VOUT_MIN	0.2
ADC	1e5
GBW	10M
VOS	0
CU	100f
TS	1u
TRF	1n
VREFN	0.25*VDD
VREFP	0.75*VDD
CP	CU
CL	1p
TRST	TS
NBIT	8
NFFT	2**8
NCYC	5
FIN	(NCYC/NFFT)/TS
VPK	VDD/8
TDROP	0.5/FIN
TSTOP	NCYC/FIN + TDROP
VLSB	(VREFP-VREFN)/2**NBIT

4) Plot transient waveforms. Plot the FFT of the DAC output to measure the ENOB and other performance parameters.


Transient Response
Name
Vis
NFFT
/VOUT
256
1.75
1.5
1.25
1.0
.75
.5
.25
V (V)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time (us)
db20(dft(value(VT("/VOUT") "NFFT" 256.0) 25.60u 281.6u 256 "Rectangular"))
Name
...trum_/VOUT
0.0
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0
(dB)
0.0
100.0
200.0
300.0
400.0
500.0
(kHz)
Signal/Expr Names
value(VT("/VOUT") "NFFT" 256.0)
Input wave type
Time Domain Waveform
FFT Input method
Calculate Sample Freq
Start/Stop Time
25.60u
281.6u
Sample Count/Freq
256
1.000M
Window Type
Rectangular
Plot FFT (Units)
dB
Start/End Freq
3.906k:500.0k
S
3.906k
500.0k
Signal bins
0
Peak Sat. Level
0.0
Harmonics
6
Analysis Type
Signal Analysis
Plot Mode
New Subwindow
Plot
Outputs
Measurement
Value
value(VT("/...
ENOB
7.8907715 (bits)
SINAD
49.265444 (dB)
SNR
49.274855 (dB)
SFDR
59.464921 (dB)
THD
0.069802841 (%)
THD
-63.122538 (dB)
Signal ...
-6.0891166 (dB)