AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Department of Electronics and Electrical Comm. Eng.
Credit Hours Engineering Program (CHEP)

1st Semester, 2018/2019	**Course Code: *ECE486***	***Time allowed: 3 Hrs.***

Analog Integrated Systems Design

The Exam Consists of **Four** Questions in **Three** Pages. ***Maximum Marks: 40 Marks*** **1 / 3**

تعليمات هامة

- حيازة التيلفون المحمول داخل لجنة الامتحان تعتبر حالة غش تستوجب العقاب، وإذا كان الدخول بالمحمول ضروريا فيلزم وضعه مغلقا فى الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- **يسمح لكل طالب باصطحاب ورقة واحدة فقط A4 يدون عليها الطالب ما يشاء (على الوجهين)، ويكتب عليها اسمه بالقلم الجاف.**
- لايسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة **زيادة على ما ذكر** والمخالفة تعتبر حالة غش.

Question (1): [10 marks]

Complete the missing items with appropriate words or sentences:

a) If we plot the FFT of an ADC spectral analysis test, the …… depends on the number of FFT points used in the test.
b) If a simple NMOS switch is used in a S/H circuit, the non-linearity of charge injection errors is mainly due to ……
c) Comparator metastability cannot be completely eliminated, but the probability of metastability can be reduced by …… and ……
d) For high gain amplifier …… offset cancellation is more appropriate, while for low gain amplifier …… offset cancellation is more appropriate.
e) An all-pass filter can be used for ……
f) One of the important filter specifications is the ……/pole and ……/pole.
g) A biquad section is a …… order filter. It is called biquad because in its general form it is a ……
h) For a second order passive LPF, the distance of the poles from the origin is equal to ……, and the poles go towards the $j\omega$ axis as the …… increases, causing …… in the frequency response and …… in the transient response.
i) The filter type that has the best phase response is the …… filter, while the filter type that has the worst phase response is the …… filter.
j) The filter type that has the steepest roll-off is the …… filter, but it uses …… in the stopband to compensate the high-Q poles.
k) If two single-opamp Sallen-Key sections are cascaded, the resulting filter is of …… order.

Question (2): [10 marks]

It is required to design a 4-bit pipelined ADC with 1.5-bit/stage. Assume the full-scale reference levels are $V_{RFFP} = 1V$ and $V_{REFN} = -1V$, and assume the comparator thresholds are at $V_{REFP}/4$ and $V_{REFN}/4$.

a) [3 marks] Draw the complete schematic of the ADC.
b) [6 marks] Assume an input voltage $V_{in} = 0.15V$. Copy the following table to your answer sheet and fill all missing items.

Stage input voltage	MDAC operation	Stage decision (0 or 1 or P)	B3	B2	B1	B0

Final ADC output						

c) [1 mark] If the capacitors of the 1st stage are $1pF$, select the capacitors of the remaining stages for optimum power/noise/area trade-off.

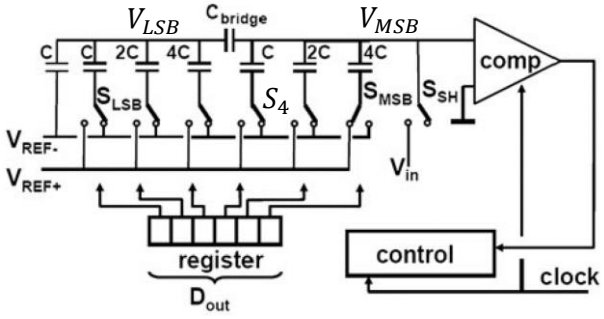
Question (3): [11 marks]

It is required to design a DT single-ended 1st order oversampling sigma-delta ADC. Assume $V_{DD} = 2V$, $V_{CM} = 1V$, $V_{REFP} = 1.5V$, $V_{REFN} = 0.5V$. Assume the sampling capacitor is $1pF$. The ADC will process signals in the audio frequency range with $f_{max} = 20kHz$.

a) [3 marks] Draw the complete schematic of the ADC.
b) [1 mark] If the integrator closed-loop gain is 0.5, find the value of the integrator feedback capacitor.
c) [4 marks] Assume the input is a DC voltage $V_{in} = 1.3V$. Assume the initial op-amp output is $0V$. Sketch the waveforms of the following signals for 15 clock cycles (indicate the voltage levels):
   i. Clock (ϕ_1 and ϕ_2).
   ii. Integrator output.
   iii. Comparator output.
   iv. DAC output
d) [1 mark] What is the average value of the DAC output and the comparator output?
e) [1 mark] If you plot the ADC output spectrum, what do you expect to see? Why?
f) [1 mark] If 12-bit resolution is required, calculate the clock frequency.

Question (4): [9 marks]

The figure below shows an implementation of a 6-bit SAR ADC with bridge capacitor. The capacitive DAC is divided into 3-bit coarse DAC (MSB array) and 3-bit fine DAC (LSB array) that controls the voltage at the left plate of C_{bridge}.



a) [2 marks] The equivalent capacitance of the bridge capacitor together with the LSB array to the left of it should sum up to a unit capacitor (C). Show that to achieve this the bridge capacitor must be given by $C_{bridge} = \frac{2^k}{2^k-1}C$, where k is the resolution of the fine capacitive DAC.
b) [1 mark] If S_4 is switched (i.e., a voltage change of ΔV_{REF} at the bottom plate of the capacitor C in the MSB array), show that it will result in voltage change $= \frac{1}{2^3}\Delta V_{REF}$ at V_{MSB}.

Hint: Group parallel/series capacitors together and apply simple voltage divider.

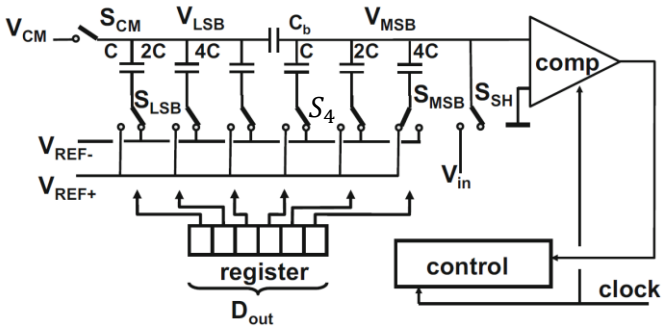
c) [2 marks] If S_{LSB} is switched (i.e., a voltage change of ΔV_{REF} at the bottom plate of the capacitor C in the LSB array), show that it will result in voltage change $= \frac{57}{512}\Delta V_{REF}$ at V_{LSB} and a voltage change $= \frac{1}{2^6}\Delta V_{REF}$ at V_{MSB}.
Hint: Group parallel/series capacitors together and apply simple voltage divider.

Since the previous SAR design requires C_{bridge} to be a fraction of C, it may lead to layout and matching difficulties. Another implementation that resolves this problem is shown in the figure below. It can be easily shown that if S_4 is switched, the change in V_{MSB} is

$$\Delta V_{MSB} = \frac{C}{C_{MSB} + \frac{C_b C_{LSB}}{C_b + C_{LSB}}}(V_{REF+} - V_{REF-})$$

Where C_{MSB} and C_{LSB} are the capacitances of the MSB and LSB arrays (both equal $7C$ for this example). If S_{LSB} is switched, the change in V_{MSB} is

$$\Delta V_{MSB,LSB} = \frac{C_b}{C_b + C_{MSB}}\Delta V_{LSB} = \frac{C_b}{C_b + C_{MSB}} \frac{C}{C_{LSB} + \frac{C_b C_{MSB}}{C_b + C_{MSB}}}(V_{REF+} - V_{REF-})$$



d) [2 marks] For proper ADC operation, the following relation should be satisfied between the previous two equations: $\Delta V_{MSB,LSB} = \frac{1}{2^3}\Delta V_{MSB}$. Show that to satisfy this condition the value of C_b should be equal to C, which resolves layout and matching issues.

e) [2 marks] If S_{LSB} is switched (i.e., a voltage change of ΔV_{REF} at the bottom plate of the capacitor C in the LSB array), show that it will not result in a voltage change $= \frac{1}{2^6}\Delta V_{REF}$ at V_{MSB}. Calculate the actual change at V_{MSB}. Does this means a non-linearity error?

End of Exam

دعواتي لكم بالتوفيق

Dr. Hesham Omran ***Exam Date: 06-Jan-2018***