AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Credit Hours Engineering Program - CHEP
Electronics & Comm. Eng. Dept.

Fall 2017	***Examination Date : 1-Jan-2018***	***Allowed Time: 3 Hours***

CHEP: ECE 486: Analog Integrated Systems Design

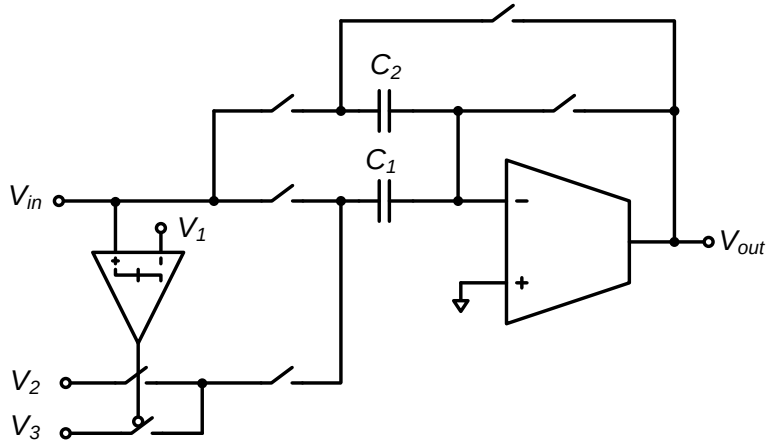
The exam consists of 5 questions in 4 pages	***Total Marks: 40 Marks***	**Page: 1/4**

NOTE: The Exam will be graded out of 80 Marks, then the total will be divided by 2.

Question (1) [16 Marks]

The figure below shows the first stage of a pipelined ADC, where $-V_{REF} < V_{in} < V_{REF}$. The switches are controlled by two non-overlapping clocks ϕ_1 and ϕ_2.

a) Redraw the schematic in your answer booklet showing which switches are controlled by ϕ_1, and which switches are controlled by ϕ_2.
b) Choose appropriate values for $V_1, V_2, and\ V_3$.
c) Find the equation that describes V_{out} in terms of V_{in} and V_{REF} if the comparator output is 0 or 1.
d) Plot V_{out} vs V_{in} showing the coordinates of breakpoints if $C_1 = C_2$.
e) If, due to an error, V_1 has a negative shift of $0.25V_{REF}$, repeat (d).
f) If, due to an error, $C_1 = 0.5C_2$, repeat (d).



Question (2) [18 Marks]

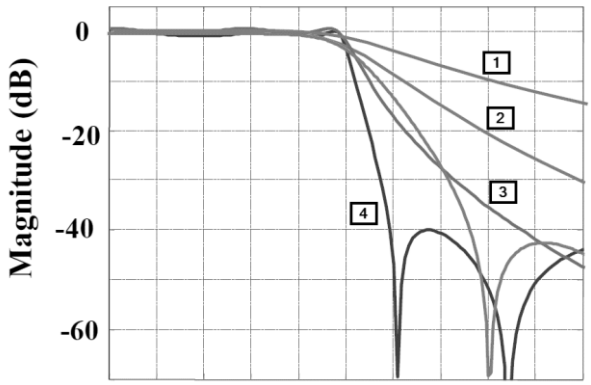
a) Three sinusoidal signals at frequencies 1kHz, 2kHz, and 3kHz are applied to a 5kHz LPF. The time delay for the three signals was measured to be equal to 2ms.
   i. What is the most likely type of the filter (e.g. Chebychev, Butterworth, etc.)?
   ii. Plot the phase vs frequency within the passband.
b) Among the filter topologies we studied, which one is more suited for operation at higher frequencies?
c) Among the continuous-time filter topologies we studied, which one has the potential for highest linearity performance?

d) Briefly list the major advantages and disadvantages of switched capacitor filters compared to continuous time filters.

e) If we add an integrator in the feedback path of a low pass filter:
   i. What will be added in the filter transfer function (a pole or a zero)?
   ii. Sketch the magnitude of the filter's new transfer function.

f) Assume it is required to implement a 5th order LPF:
   i. If it is implemented using biquads, how many biquads are needed?
   ii. Other than biquads, what additional block is required?
   iii. If the biquads are implemented using Sallen-Key topology, how many op-amps are required for the whole filter? Why? If a topology other than Sallen-Key is used for the biquad, will the number of op-amps remain the same?
   iv. If the filter is implemented as an integrator based ladder filter, how many integrators are required?

g) The figure below shows the magnitude response vs frequency for a 5th order LPF using different filter types. What are the filter types for the numbered responses (1 to 4)?



Question (3) [12 Marks]

Compute the required sampling frequency for an oversampling ADC converter built to handle in-band signal ranging from DC to 20kHz with 18-bit resolution (HiFi audio applications).

Consider these three cases:

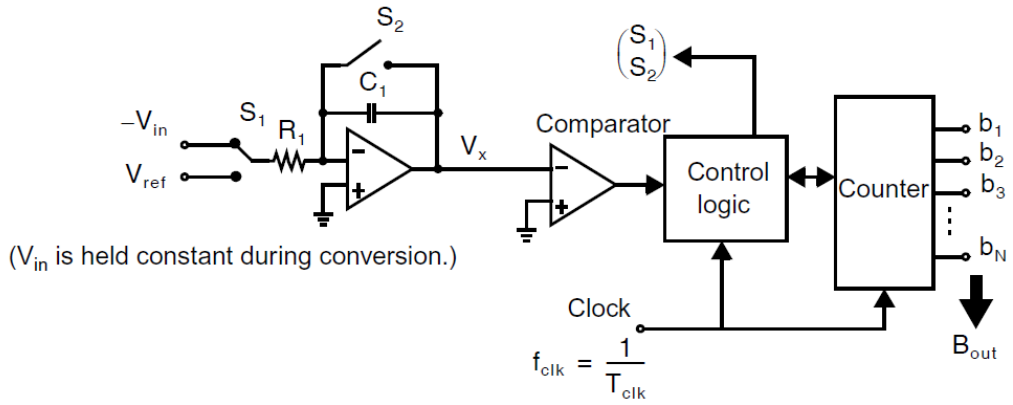
a) No noise-shaping, just pure oversampling, 1-bit quantization.
b) 1st order SDM.
c) 2nd order SDM.
d) 2-2-1 MASH SDM.

Hint: $SQNR = 10\,log\left(\frac{P_{sig}}{IBN}\right) \approx 1.76 + 6.02N + 10\,log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\,log(OSR)$

Question (4) [16 Marks]

The ADC depicted below operates in two phases: In phase I the switch S1 is connected to $-V_{in}$ for a fixed time T_1, then in phase II S1 is connected to V_{ref} for a variable time T_2 till the comparator toggles. Assume $T_1 = 10ms$, $V_{ref} = 2V$, $R_1 = 20k\Omega$ and $C_1 = 250nF$.

a) What is the type and name of this ADC?
b) Plot the waveforms at V_x vs time for $V_{in} = 1$V and $V_{in} = 1.5$V overlaid on the same plot. On the plot clearly indicate the peak voltage and the value of T_2.
c) If 12-bit resolution is required, calculate f_{clk}.
d) What is the maximum conversion time of this ADC? What is the sample rate?
e) Assume there is a 50Hz noise signal coupled to V_{in} from the power lines. Choose a suitable T_1 such that the 50Hz noise signal does not affect the conversion result.
f) Does this ADC suffer from gain error due to circuit imperfections/variations? Why?



Question (5) [18 Marks]

It is required to design an integer-N charge pump PLL that has $f_{in} = 100MHz$ and $f_{out} = 400MHz$. Assume the VCO output frequency is given by $f_{out}(MHz) = 300MHz + K_{VCO}V_{ctrl}$, where $K_{VCO} = 200MHz/V$. Assume $V_{DD} = 1V$ and the loop filter is implemented as shown in the figure below.

a) Draw the block diagram of the PLL indicating the frequency divider ratio.
b) Draw a simplified schematic for the PFD+CHP using two D-FFs, one AND gate, and two ideal current sources.
c) Sketch the transfer function of the VCO (f_{out} vs V_{ctrl}).
d) What is the type and order of this PLL?
e) Does this PLL suffer from static phase error? Why?
f) What is the function of R_z *and* C_p in the loop filter?

g) If it is required to integrate the loop filter on-chip, a reasonable choice for the loop damping factor is (0.2, 1.2, 2.2).

h) A reasonable choice for the loop bandwidth is (10MHz, 25MHz, 50MHz).

i) Assume the PLL was initially in lock, then an abrupt phase step caused the input reference to lead by 4ns. For simplicity, assume the PLL will achieve lock again in 50ns. In this 50ns time span, sketch the waveforms of (1) the input reference, (2) the divider output, (3) the PFD digital output (UP and DN), (4) the loop filter output (V_{ctrl}), (5) the output frequency, and (6) the PLL output. In the sketch, indicate the value of V_{ctrl} at steady state.

j) The output phase noise components of the PLL are shown in the figure below. Indicate what each numbered curve represents (1 to 4).

k) In the phase noise example below, what is the major phase noise contributor? From phase noise perspective, is increasing the loop bandwidth good or bad?