وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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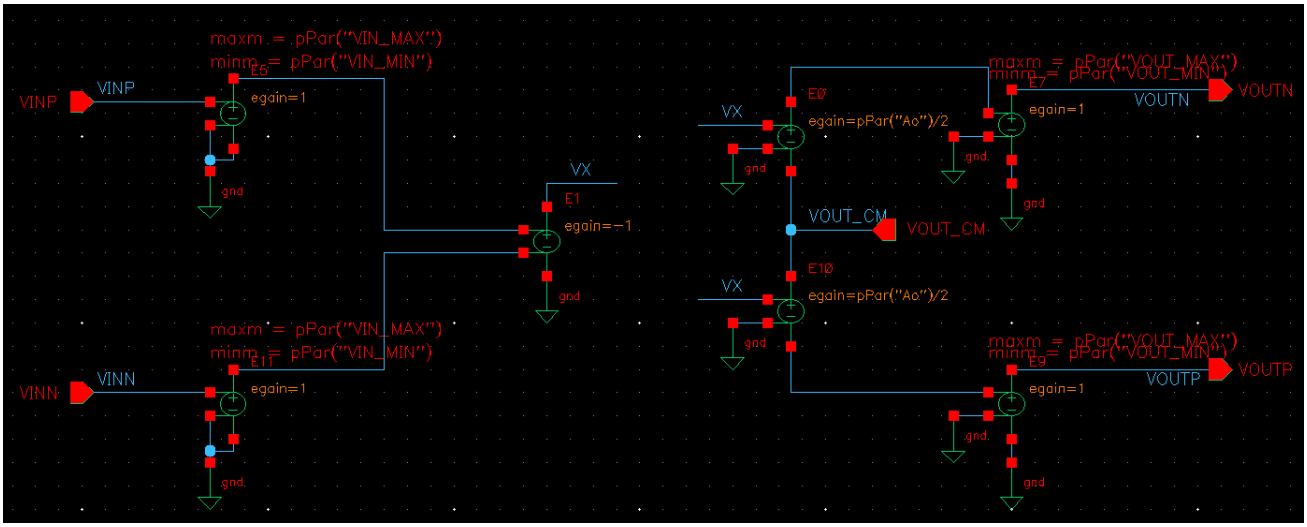
Analog Integrated System Design – Cadence Tools
Lab 05
Switched Capacitor Circuits

Lab Objective

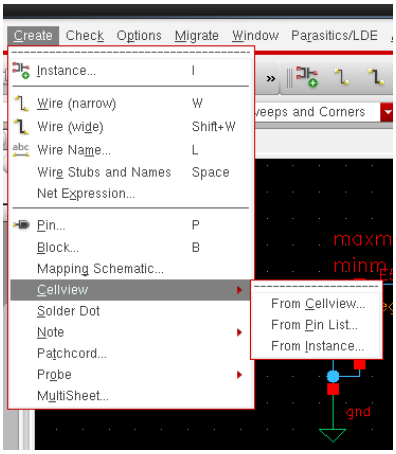
1) To be able to model a fully differential amplifier.
2) To be familiar with the operation of a fully differential switched cap amplifier.
3) To be familiar wit the operation of a fully differential switched cap integrator.
4) To be familiar with Periodic Steady State (PSS) and Periodic AC (PAC) analyses.

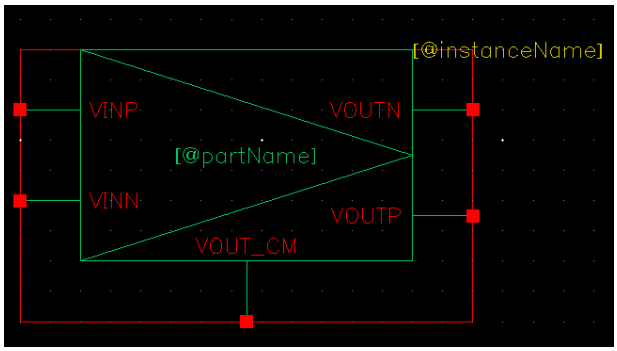
PART 1: Fully Differential Op-amp Behavioral Model

1) Create the schematic shown below to model a fully differential op-amp with finite gain, finite input range, and finite output range. Use vcvs from analogLib.

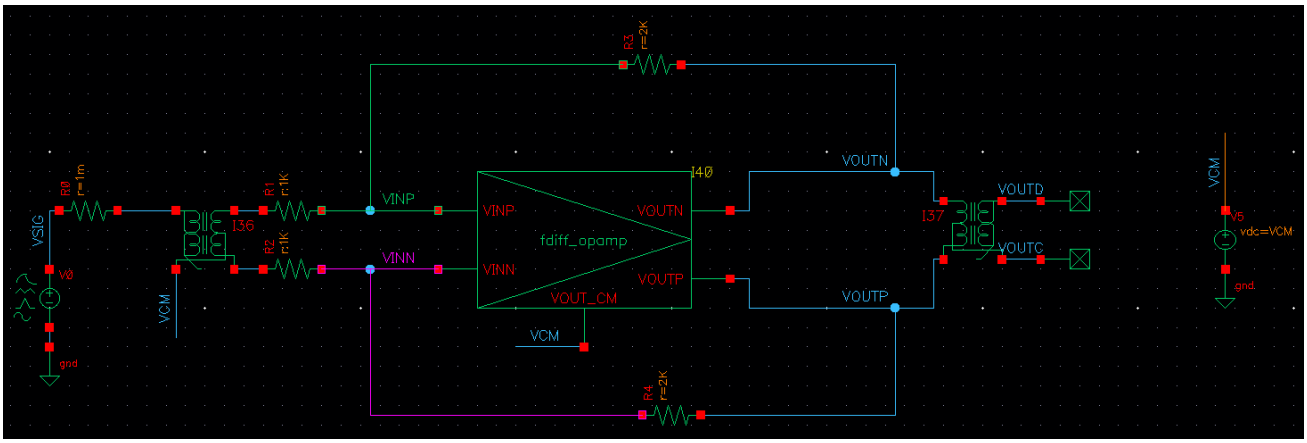


2) Create a new symbol.





3) Create a simple testbench to verify your fully differential op-amp. An example testbench is shown below.

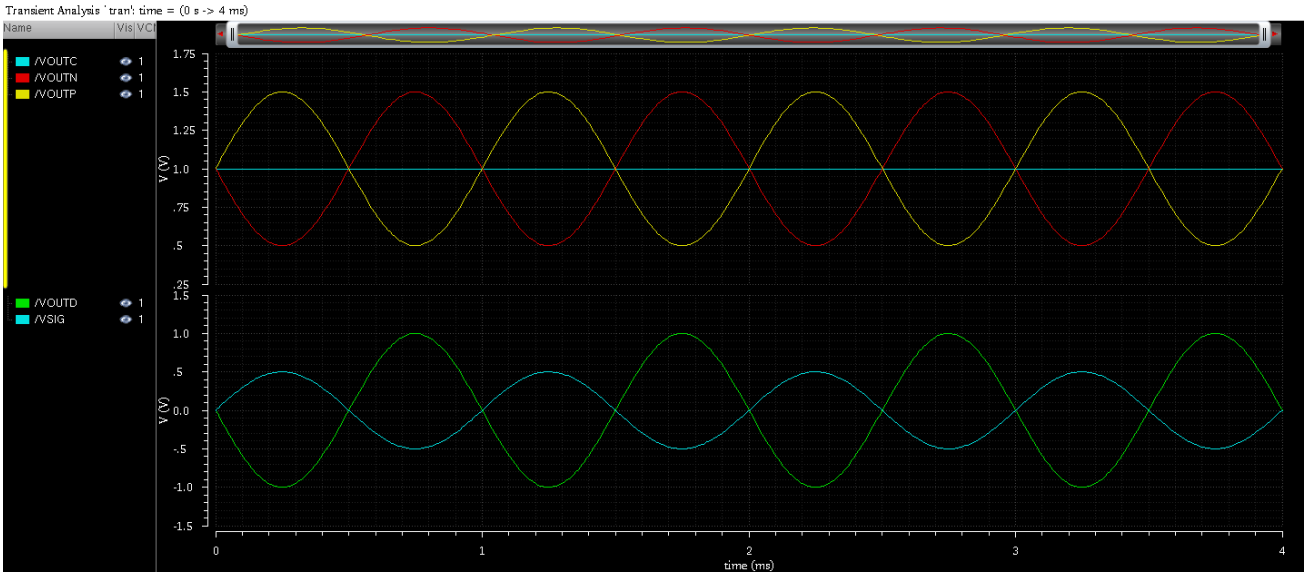


CDF Parameter	Value	Display
Ao	1e5	off
VOUT_MAX	VDD - 0.2	off
VOUT_MIN	0.2	off
VIN_MAX	VDD - 0.2	off
VIN_MIN	0.2	off

4) Set the input signal as below. The differential operation doubles the signal swing (one extra bit).

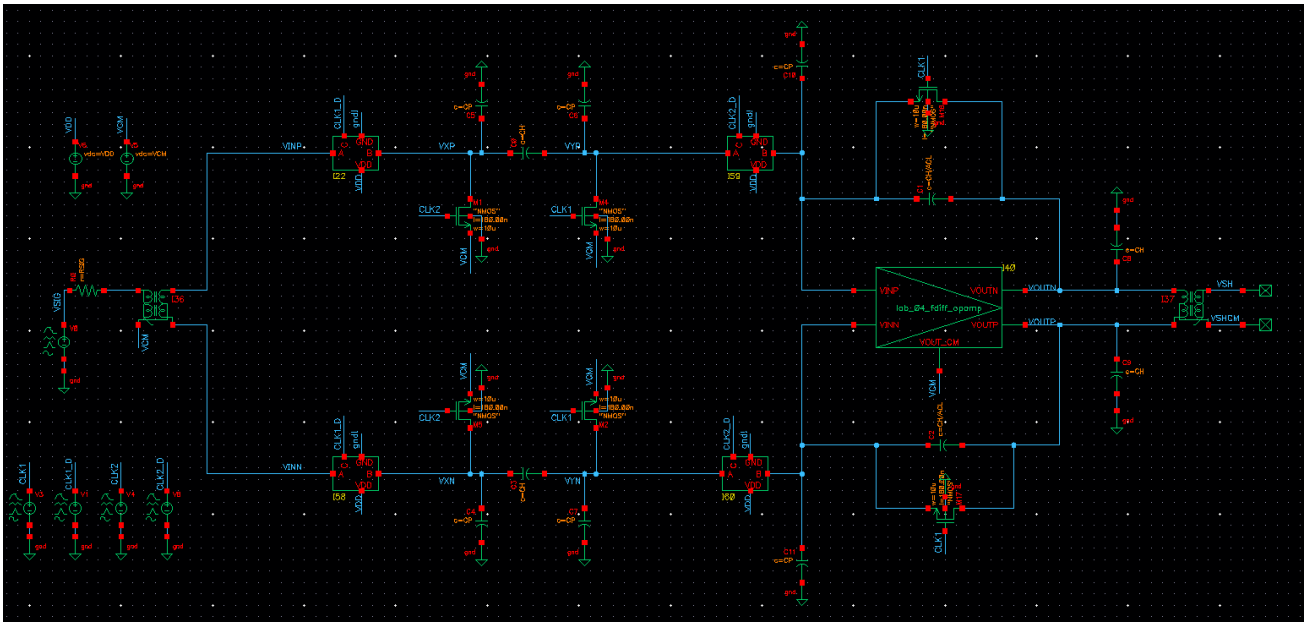
Type	Sin
Frequency	FIN
Amplitude	2*VPK
Offset (DC level)	0

5) Import design variables. Set FIN = 1k, VPK = 0.25, and VCM = 1. Set transient analysis stop time to 4/VAR("FIN"), i.e., four input cycles and accuracy to conservative.


Transient Analysis `tran': time = (0 s -> 4 ms)
Name
Vis
/VOUTC
/VOUTN
/VOUTP
/VOUTD
/VSIG
V (V)
time (ms)

PART 2: Fully Differential Switched Capacitor Amplifier

1) Create a testbench for a fully differential switched cap amplifier as shown below. This is an example of a sample and hold amplifier (it samples the signal and multiplies it by 2).



2) Set the input signal as below. The differential operation doubles the signal swing (one extra bit).

Type	Sin
Frequency	FIN
Amplitude	2*VPK
Offset (DC level)	0

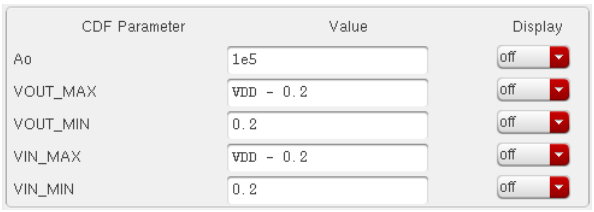
3) Set the clock signals as below.

	CLK1	CLK1_D	CLK2	CLK2_D
Type	Pulse	Pulse	Pulse	Pulse
Initial value	0	0	0	0
Pulse value	VDD	VDD	VDD	VDD
Period	TS	TS	TS	TS
Pulse width	TON	TON	TON	TON
Delay	0	0.1*TON	0.5*TS	0.5*TS+0.1*TON
Rise/fall time	TRF	TRF	TRF	TRF

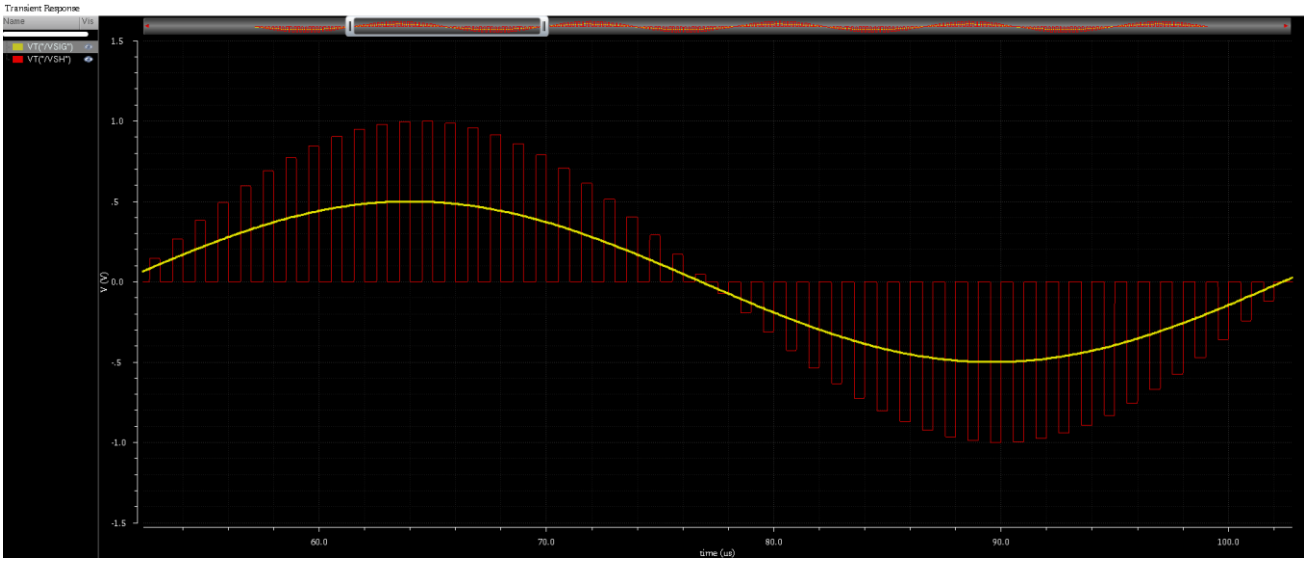
4) Import variables from schematic. Set the global variables as below. NCYC is the number of input signal cycles. NFFT is the number of FFT points. TS is the sampling period. TON is the T&H ON time

(transparent window). TSTOP is extended by a half period (TDROP). This half period is dropped before doing the FFT to avoid simulator artifacts when simulation starts (and to avoid start-up artifacts in a real circuit). Note that NCYC, NFFT, and FIN are selected to satisfy the coherent sampling condition.

CH	1p
CP	0.1*CH
RSIG	1k
TS	1u
TON	0.4*TS
TRF	1n
NFFT	2**8
NCYC	5
FIN	(NCYC/NFFT)/TS
VDD	2
VCM	VDD/2
VPK	VDD/8
TDROP	0.5/FIN
TSTOP	NCYC/FIN + TDROP
ACL	2

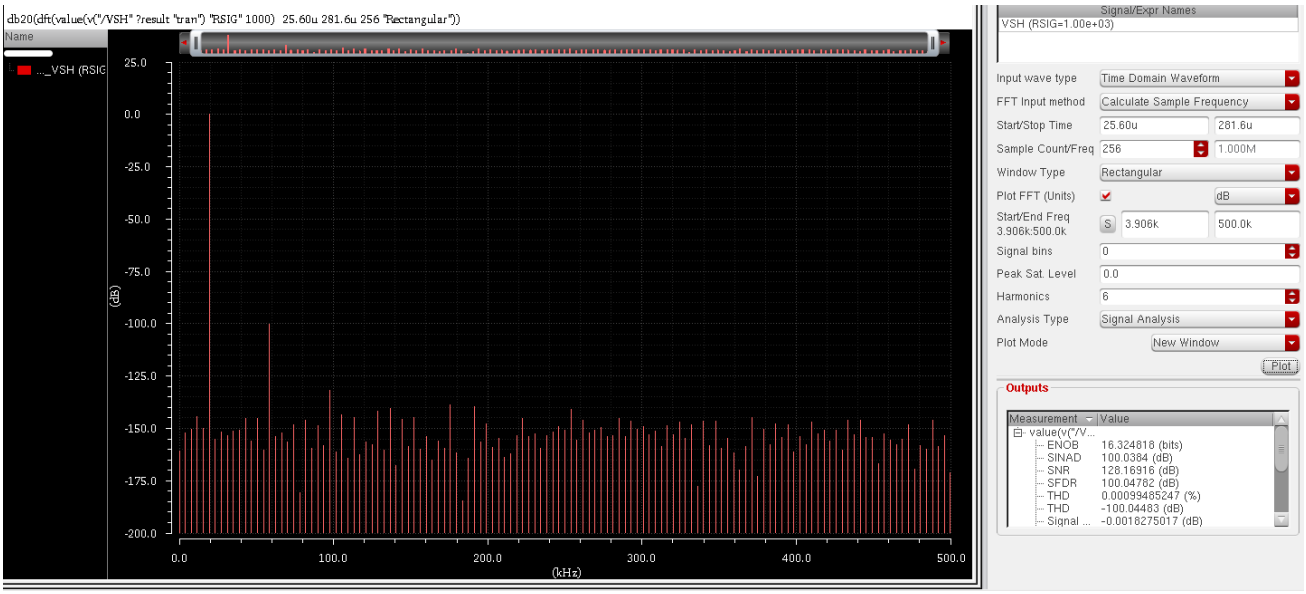


5) Run transient analysis. Examine the transient waveforms at different points. Note that this architecture requires an OTA with very high slew rate (resettable gain stage).



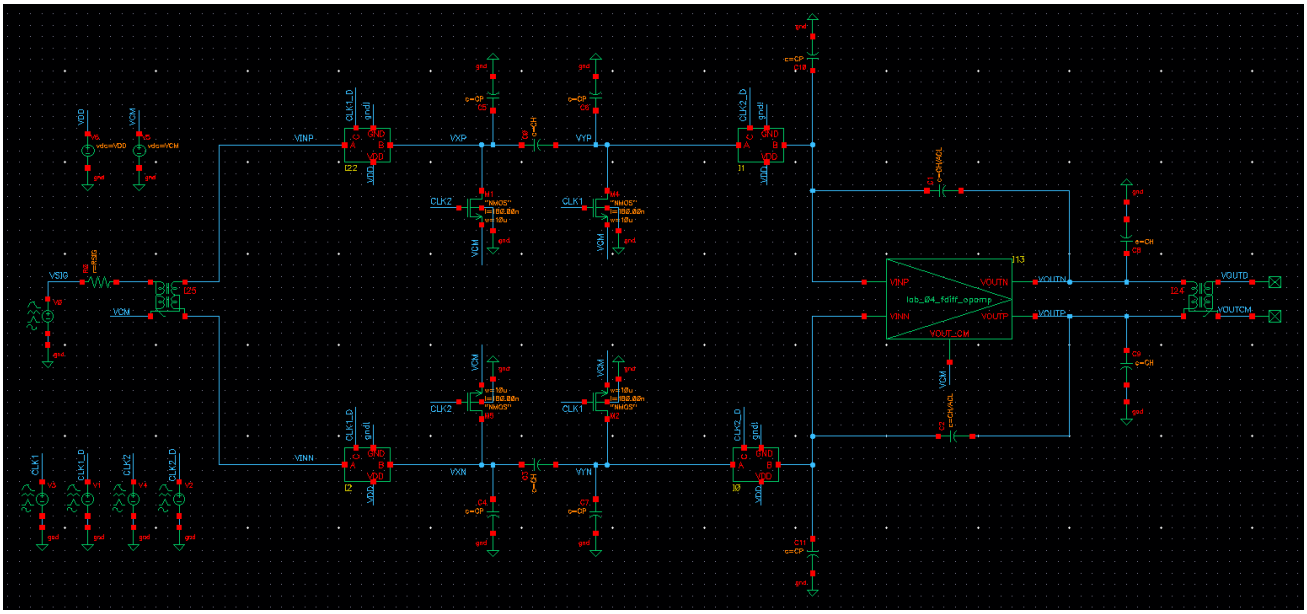
6) Use the Spectrum Assistant to plot FFT for the differential output. Report the following results.

- ENOB
- SINAD
- SNR
- SFDR
- THD (in dB)
- Signal power
- DC power



PART 3: Fully Differential Switched Capacitor Integrator

1) Copy the previous cell to a new cell “lab_04_sw_cap_int_tb”. Remove the reset switch that was used across the feedback capacitors. The circuit now acts as a switched capacitor integrator. The modified circuit schematic is shown below.



2) Modify the input signal to a be a pulse source with the properties shown below.

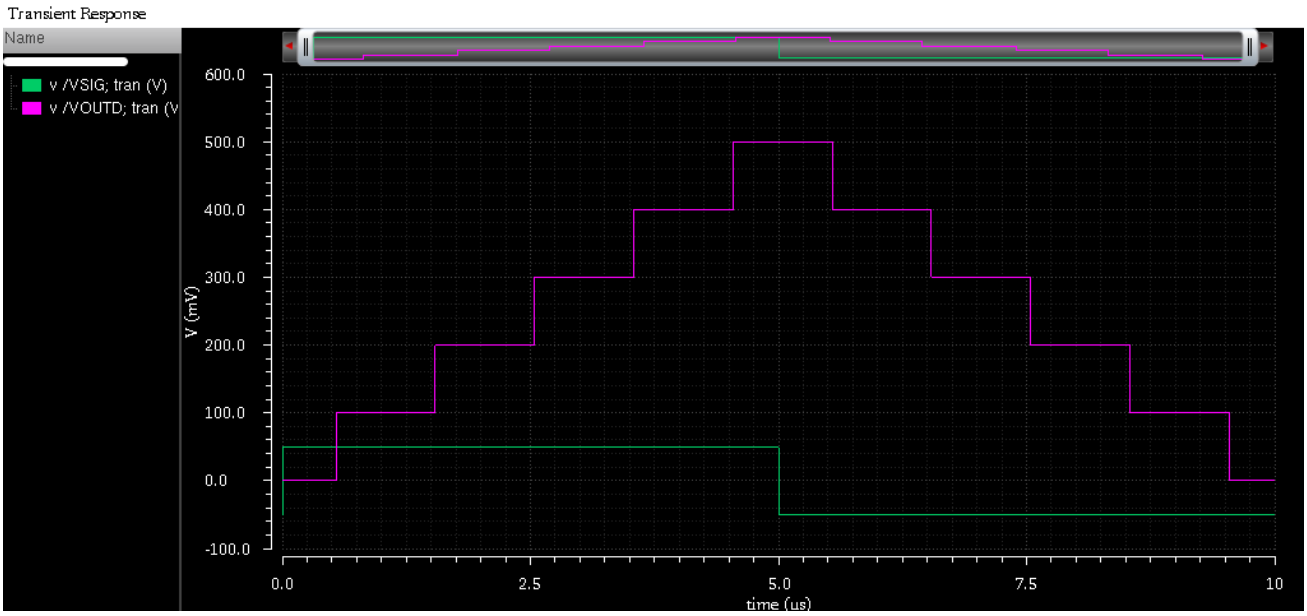
Type	Pulse
Initial (one) value	VPK
Pulse (zero) value	-VPK
Period	2*NP*TS
Pulse width	NP*TS
Delay	0
Rise/fall time	TRF

3) Set global variables as shown below.

CH	1p
CP	0.1*CH
RSIG	1k
TS	1u
TON	0.4*TS
TRF	1n
VDD	2
VCM	VDD/2
VPK	50m
TSTOP	2*NP*TS

NP	5
ACL	2

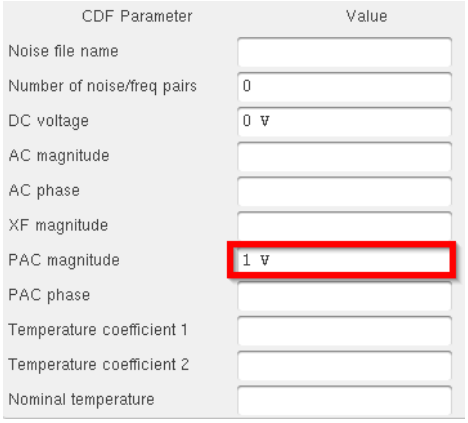
4) Run transient analysis for VAR("TSTOP"). Plot VSIG and VOUTD.
    a. What is the relation between input and output waveforms?
    b. What is the value of each voltage step in the output waveform? Why?



PART 4: Periodic Steady State (PSS) and Periodic AC (PAC) Analyses

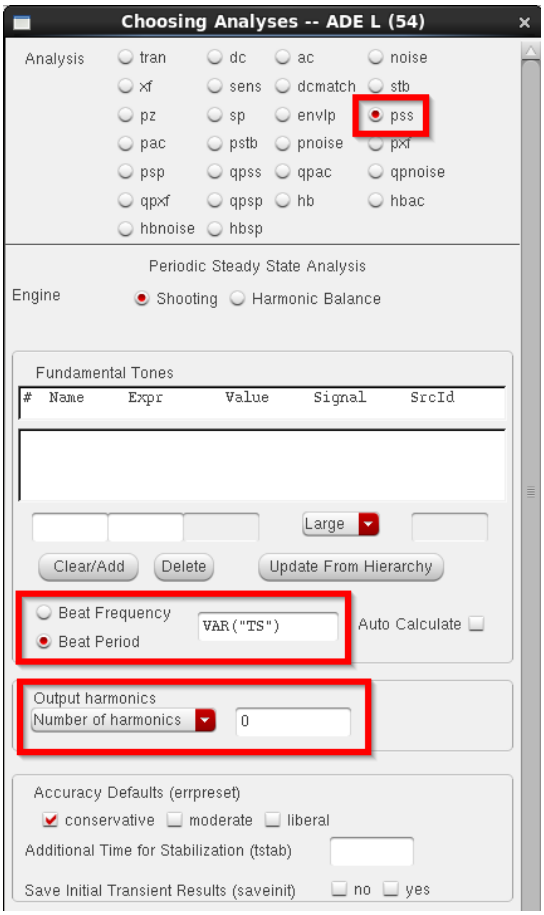
In this part we would like to plot the frequency response of the switched capacitor integrator. Note that a switched cap circuit is a linear circuits (doubling the input doubles the output), but it is time variant (not an LTI system). Since the behavior of the circuit changes with time according to the clock signal, it is not possible to use normal ac analysis. The circuit doesn't have an operating point (dc steady state), but the clock signal which changes the circuit state is periodic (periodic steady state). A specialized type of analysis name periodic steady state (PSS) is used to analyze such type of circuits. PSS can be followed by other types of analysis such as PAC (periodic equivalent of ac analysis) and pnoise (periodic equivalent of noise analysis)[1].

1) Replace the transient signal source with a DC source and set its properties as shown below (set PAC magnitude to unity).

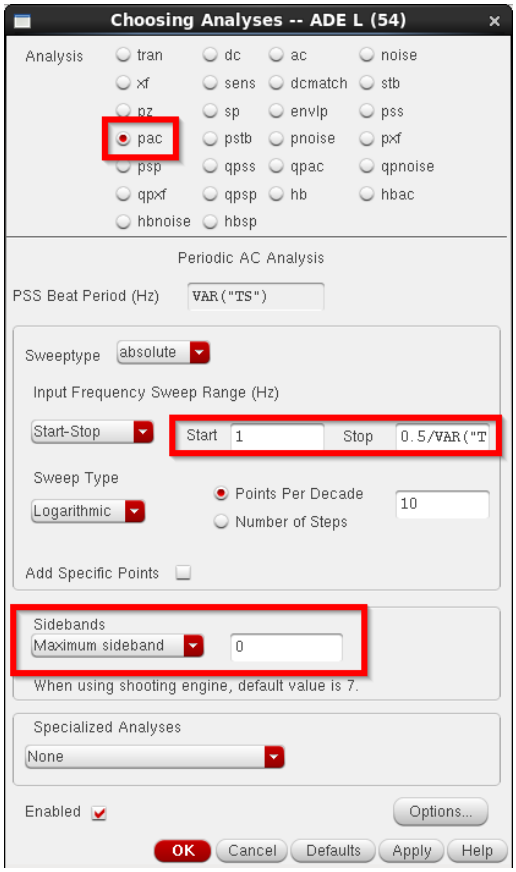


2) Define the DC gain of the fully differential op-amp as a parameter "ADC". In global variables set ADC = 1e4, 1e5.
3) Disable the transient analysis. Set PSS analysis as shown below.

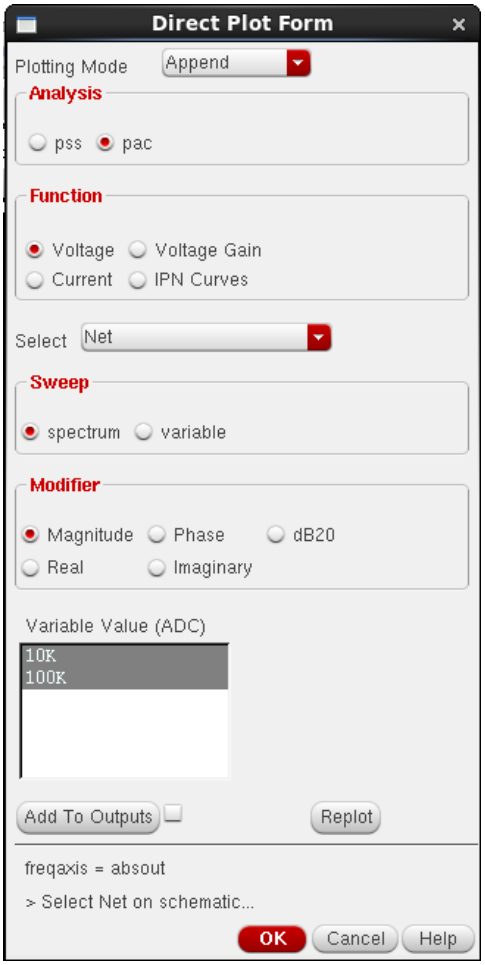
[1] For more information on pss, pac, and pnoise analyses, see "B. Murmann, Thermal Noise in Track-and-Hold Circuits: Analysis and Simulation Techniques, IEEE Solid-State Circuits Magazine, 2012, 4, 46-54" and "K. Kundert, Simulating switched-capacitor filters with spectreRF, Available: http://www.designers-guide.org/Analysis/sc-filters.pdf".

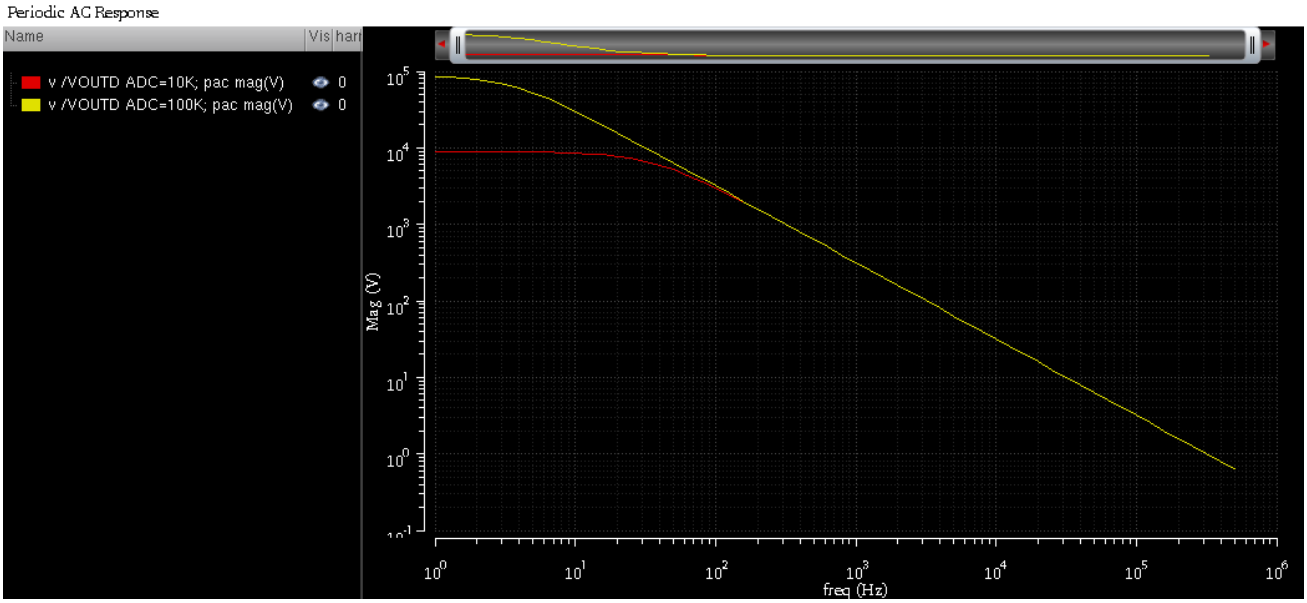


4) Setup PAC analysis as shown below. Set stop frequency to 0.5/VAR("TS").



5) Run the simulation. Use the Direct Plot Form to plot the integrator ac response (VOUTD vs frequency). Use log-scale for both x and y axes.
   a. What is the type of the frequency response (LPF, HPF, BPF)? Why?
   b. Does the gain of the transfer function saturate? At what value? Why?[2]





[2] Note that the continuous time equivalent output is $v_{out}(t) = \frac{A_{CL}}{T_S}\int v_{in}(t)dt$. Convert to s-domain and take the magnitude: $|v_{out}(f)| = \left|\frac{A_{CL}}{T_S \cdot 2\pi f}\right|$.