Analog Integrated Systems Design

Lecture 07
Basics of Sample & Hold Circuits

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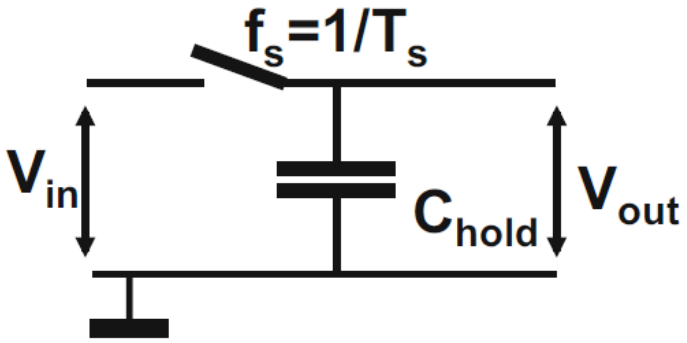
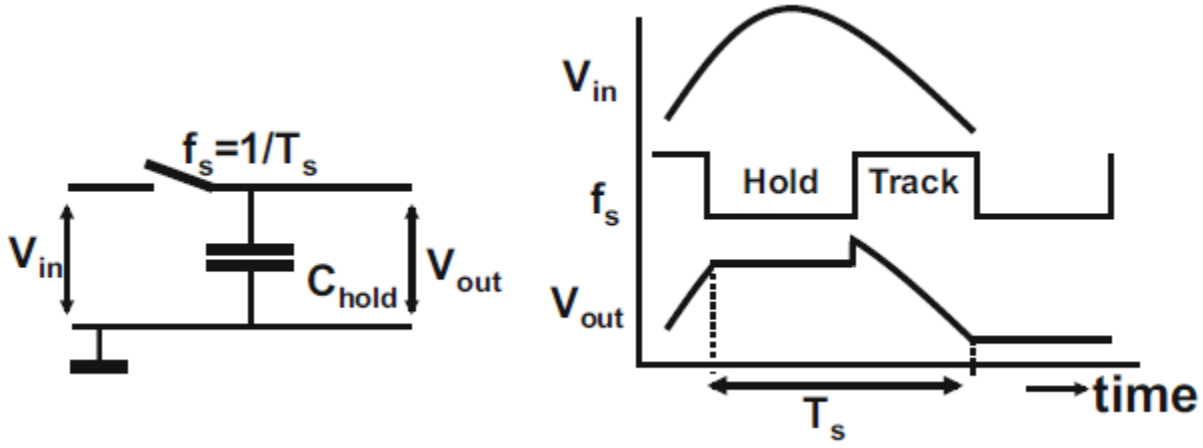
Sampling

- Converts a continuous time (CT) signal to a discrete time (DT) signal
  - The result is a sequence of samples
- The sampling instants are defined by a clock signal
- The clock signal controls an electronic switch (e.g., MOS transistor)
- The sampled signal is stored as a voltage on a capacitor



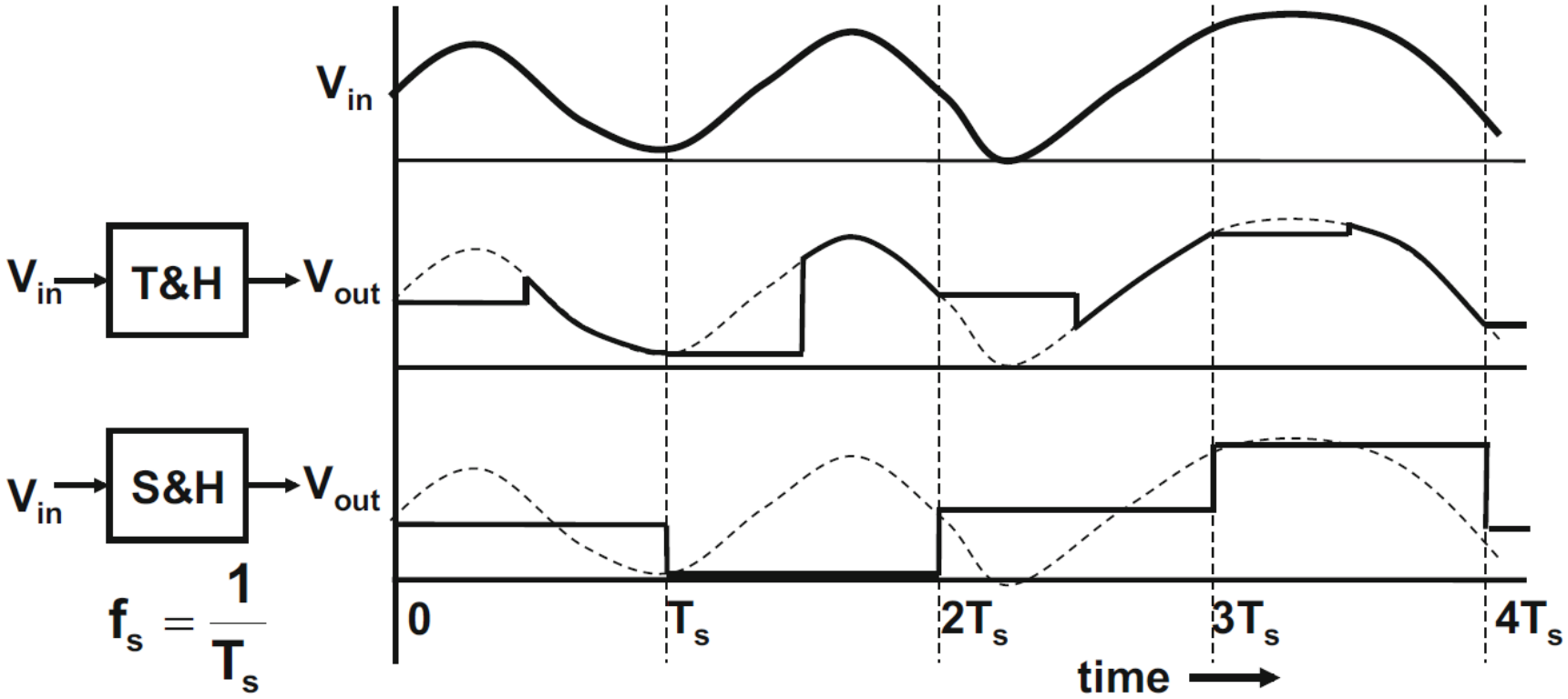
Track & Hold (T/H)

- What we implement practically is a T/H not a S/H
  - Switch closed (ON): Track mode
  - Switch open (OFF): Hold mode
- But we sometimes refer to it as S/H



[M. Pelgrom, 2017]

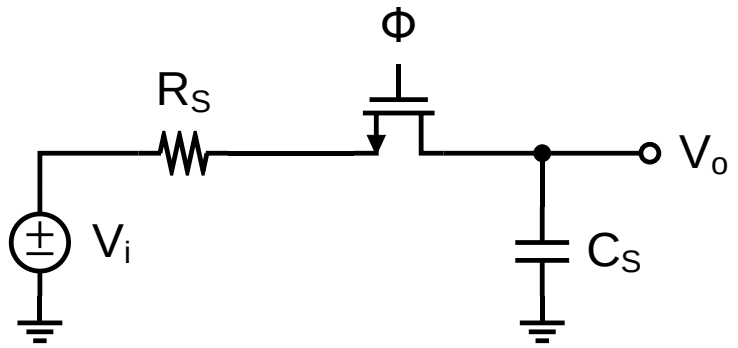
T/H vs S/H



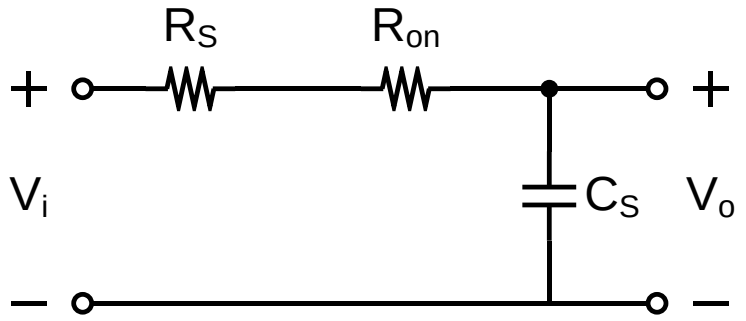
[M. Pelgrom, 2017]

Tracking Bandwidth (TBW)

- MOS technology is naturally suitable for implementing T/H
- The lowpass network determines the tracking bandwidth
- Tracking bandwidth determines how promptly Vo can follow Vi
- Signal-dependent R_{on} → signal-dependent TBW → distortion
  - Not a concern if TBW is sufficiently large
    - TBW >> f_{in}, depending on the target accuracy



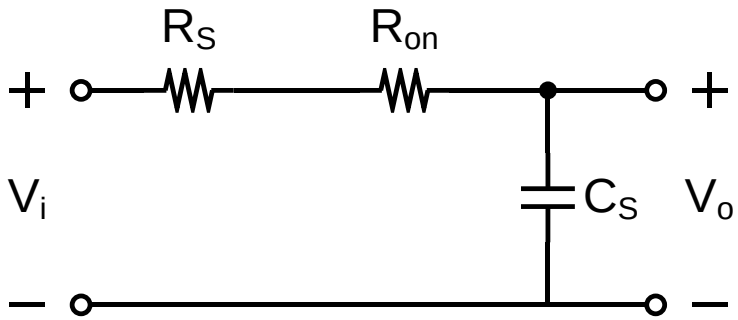
$$R_{on}^{-1} = \mu C_{ox} \frac{W}{L}(V_{DD} - V_{th} - V_i)$$



$$TBW = 1/(R_S + R_{on})C_S$$

T/H Speed-Accuracy Trade-off

- Short L, large W, large V_{ov}, and small V_i help reduce R_{on} → More speed
- But large W and V_{ov} (large Q_{ch}) increase T/H errors → Less accuracy



$$\tau = \frac{1}{\text{TBW}} = (R_S + R_{on})C_S$$

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu C_{ox} WL(V_{DD} - V_{th} - V_i)} = \frac{L^2}{\mu Q_{ch}}$$

Acquisition Time (t_{acq})

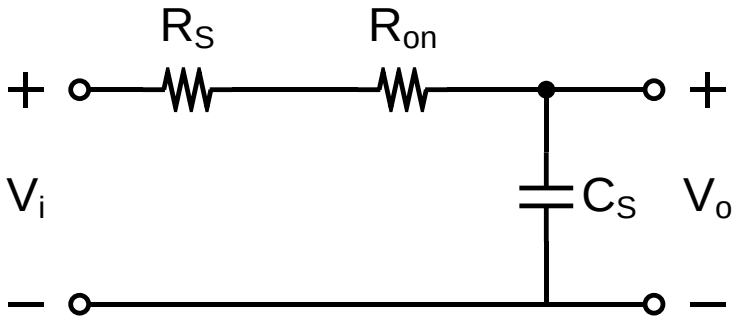
- Assume linear settling of first order system

$$V(t) = V_i + (V_f - V_i)(1 - e^{-\frac{t}{\tau}})$$

$$T = \tau \ln\left(\frac{V_f - V_i}{V_f - V(T)}\right) = \tau \ln\left(\frac{\Delta V}{\epsilon}\right)$$

- If $\Delta V = FS$ and $\epsilon < 1LSB = \frac{FS}{2^N}$

$$t_{acq} = \tau \ln(2^N) = 0.69N\tau$$

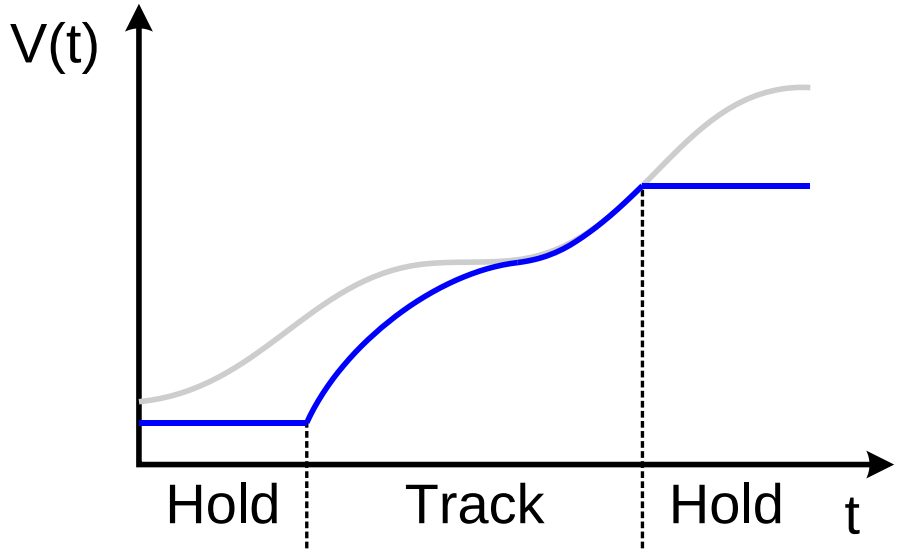


$$\tau = \frac{1}{\text{TBW}} = (R_S + R_{on})C_S$$

Accuracy	t_{acq}
1% (7b)	≥ 5τ
0.1% (10b)	≥ 7τ
0.01% (13b)	≥ 9τ

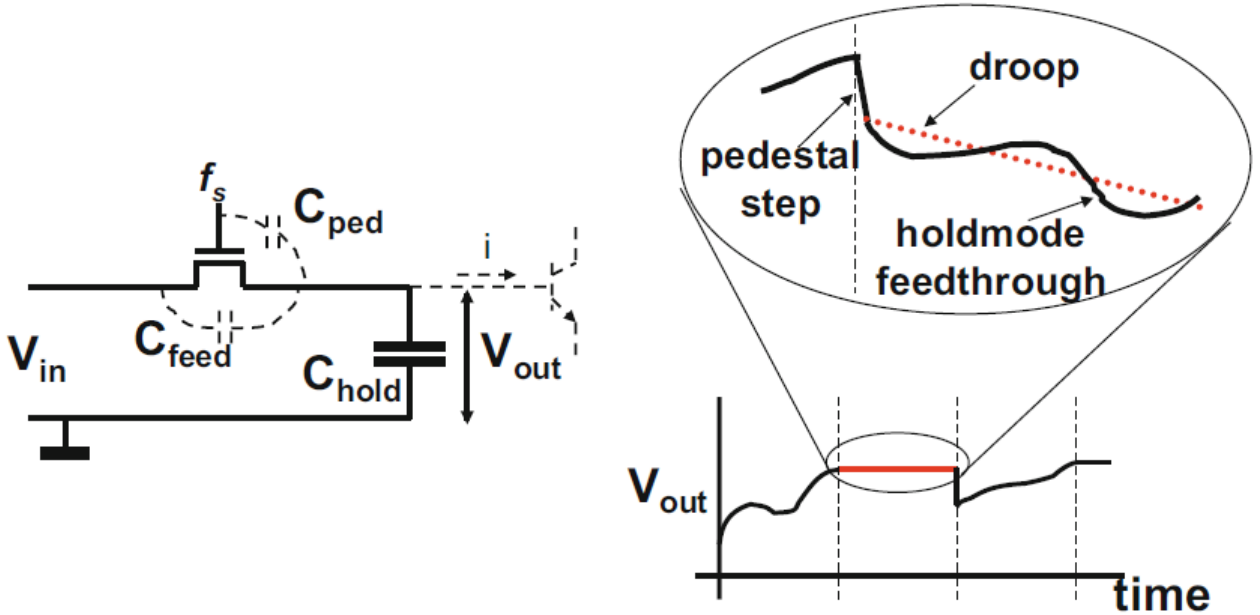
Ideal T/H

- Sufficient tracking bandwidth → negligible tracking error
- Well-defined sampling instant (asserted by clock rising/falling edge)
- Zero track-mode and hold-mode offset errors



T/H Errors (1)

- Pedestal step:
  - Switch charge injection (CI)
  - Clock feedthrough (CF)
- Droop: Due to leakage. Dictates min sample rate. More leakage in deep submicron (DSM) nodes.
- Hold-mode feedthrough (C_{feed}): Usually negligible.



[M. Pelgrom, 2017]

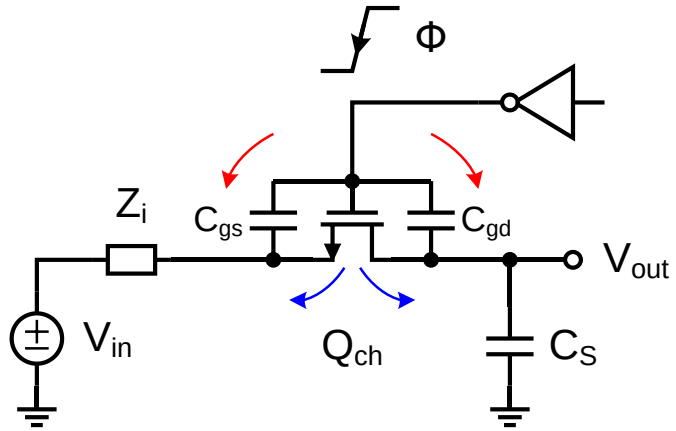
T/H Pedestal Step

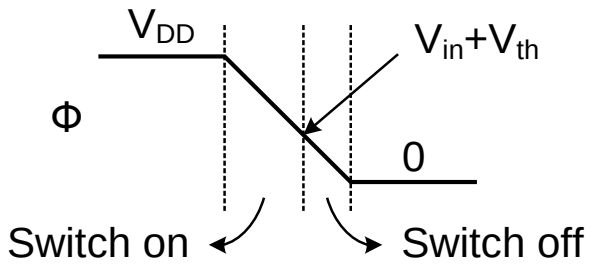
$$V_{pedestal} = \frac{C_{ped}\Delta V_{gate} + Q_{gate}/2}{C_{hold}} = -\frac{WC_{olap}V_{DD} + WLC_{ox}(V_{DD} - V_{in} - V_{T,N})/2}{C_{hold}}$$

- Offset and gain error components
- Nonlinear error component:
  - V_T depends nonlinearly on V_{in} → Distortion
- CF and CI sensitive to source impedance, C_H, and clock rise/fall time
- CF can be simulated by SPICE
  - But CI cannot be accurately simulated with lumped transistor models

Pedestal Step Edge Rate Dependence

- Slow turn-off is good for CI and CF
  - But more sensitive to jitter and signal dependent aperture delay (more later)





	Clock feedthrough	Charge injection
Fast turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S} V_{DD}$	$\Delta V = -\frac{C_{ox} WL (V_{DD} - V_{th} - V_{in})}{2(C_{gs}+C_S)}$
Slow turn-off	$\Delta V = -\frac{C_{gs}}{C_{gs}+C_S}(V_{in}+V_{th})$	$\Delta V = 0$

[Y. Chiu, EECT 7327, UTD]

Top-Plate T/H Pedestal Error

Slow turn-off:

$$V_o = (1+\varepsilon)\cdot V_i + V_{os}$$

$$V_o = \left(1-\frac{C_{gs}}{C_{gs}+C_S}\right)\cdot V_i - \frac{C_{gs}}{C_{gs}+C_S}V_{th}$$

Fast turn-off:

$$V_o = (1+\varepsilon)\cdot V_i + V_{os}$$

$$V_o = \left(1+\frac{1}{2}\frac{C_{ox}WL}{C_{gs}+C_S}\right)\cdot V_i - \left[\frac{C_{gs}}{C_{gs}+C_S}V_{DD} + \frac{1}{2}\frac{C_{ox}WL}{C_{gs}+C_S}(V_{DD}-V_{th})\right]$$

Watch out for nonlinear errors!

T/H Speed-Accuracy Trade-off

- Technology scaling improves T/H performance!

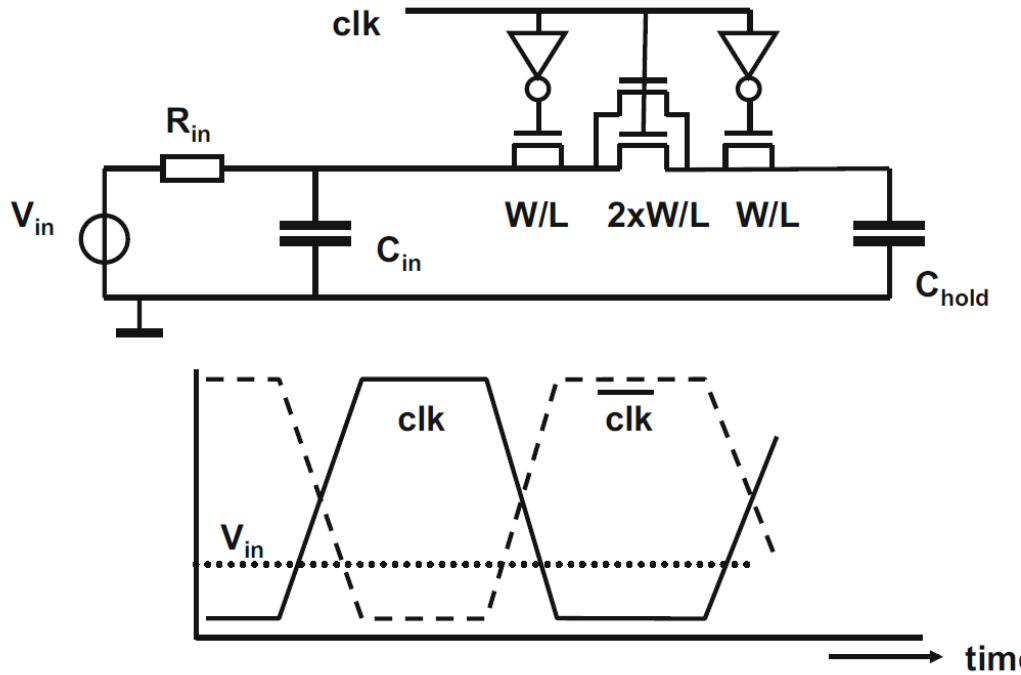
Pedestal error: $\Delta V \approx \frac{1}{2}\frac{Q_{ch}}{C_S}$

TBW: $TBW \approx \frac{1}{R_{on}C_S} = \frac{\mu Q_{ch}}{L^2 C_S}$

$$\boxed{\frac{\Delta V}{TBW} \approx \frac{1}{2}\frac{Q_{ch}}{C_S} \cdot \frac{L^2 C_S}{\mu Q_{ch}} = \frac{L^2}{2\mu}}$$

Dummy Switches

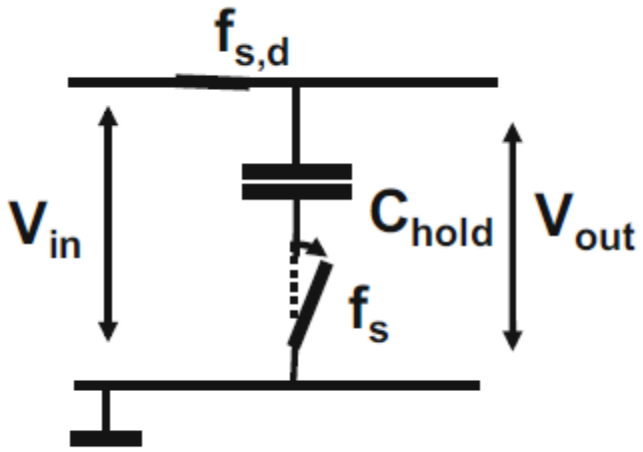
- Switch charge injection (CI) error can be mitigated by using dummy switches
- The nonlinear dependence of CI on R_{in}, C_{hold}, and clock rise/fall time makes it difficult to achieve a precise cancellation
- clk rising edge must trail $\overline{clk}$ falling edge

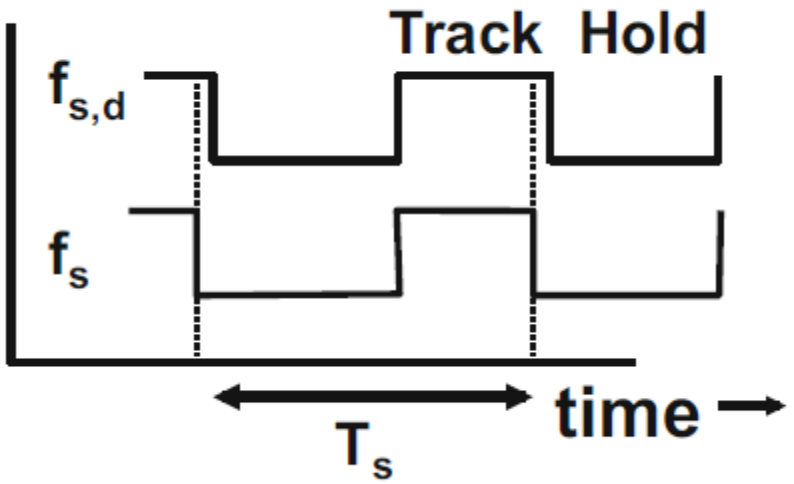


[Y. Chiu, EECT 7327, UTD] [M. Pelgrom, 2017]

Bottom-Plate Sampling Principle

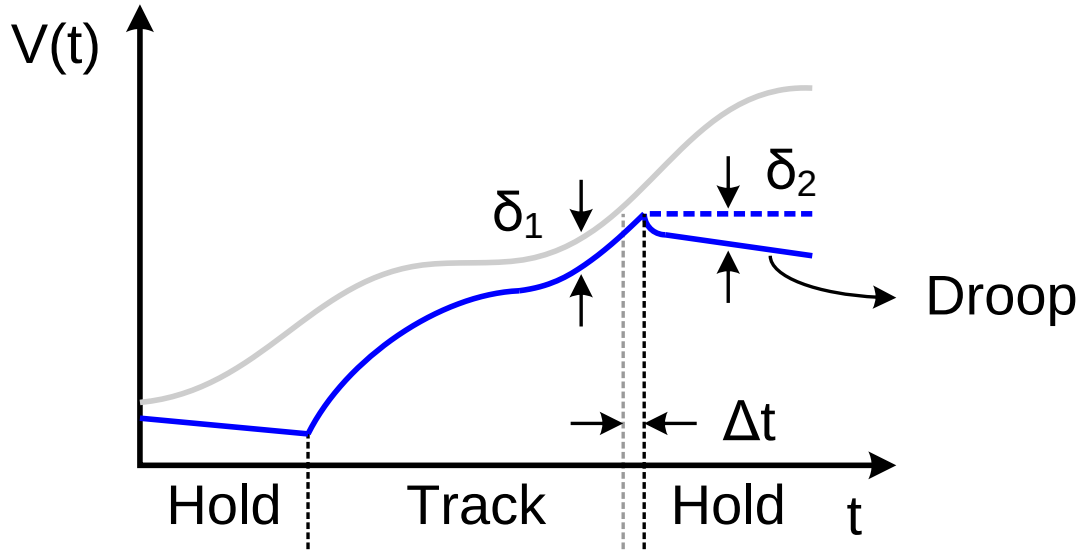
- Add another switch at the bottom plate
  - The new switch charge injection is independent of Vin
  - No non-linear error → No distortion
  - Necessary for more than 8-bit resolution





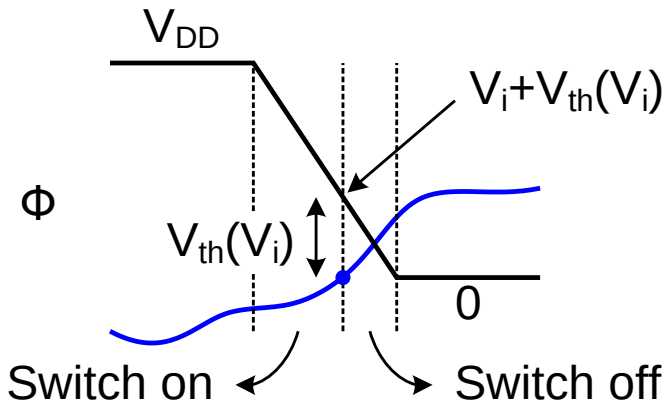
T/H Errors (2)

- Aperture delay – the delay Δt between hold command and hold action
- Aperture jitter – the random variation in Δt (i.e., sampling clock jitter)



Signal-Dependent Aperture Delay

- Non-uniform sampling due to signal-dependent aperture delay causes distortion in top-plate S/H
- Sharp clock edge and small Vin mitigate the delay variation

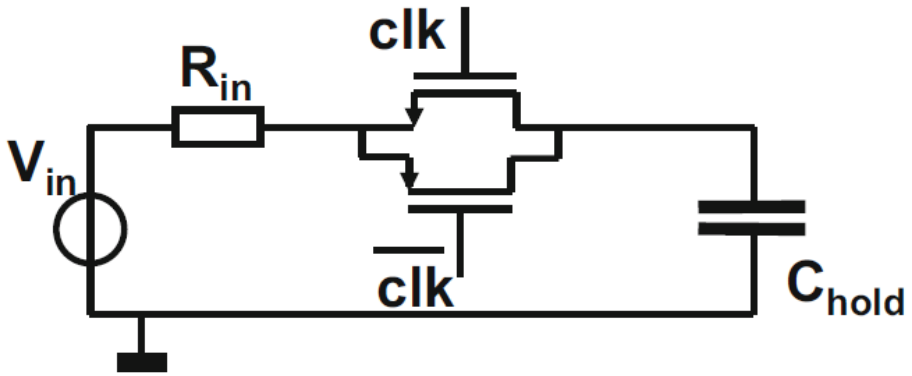


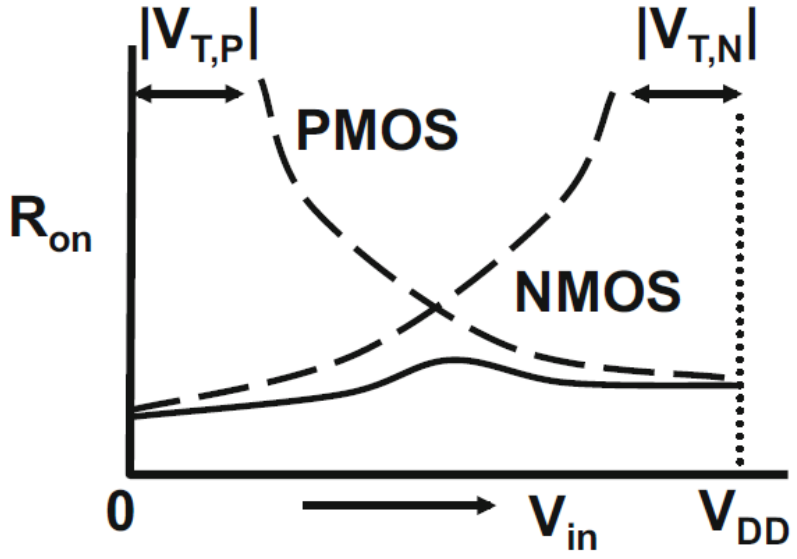
$$V_i(t) = A\sin(\omega t)$$

$$V_o(t) = A\sin\left[\omega\left(t - \frac{V_i(t)}{SR}\right)\right]$$

Transmission Gate (TG)

- Ron (and TBW) depends on Vin
  - Can be reduced by using CMOS switch (TG)
  - May be indispensable for low voltage operation
- Delay mismatch between clk and $\overline{clk}$ will cause distortion error

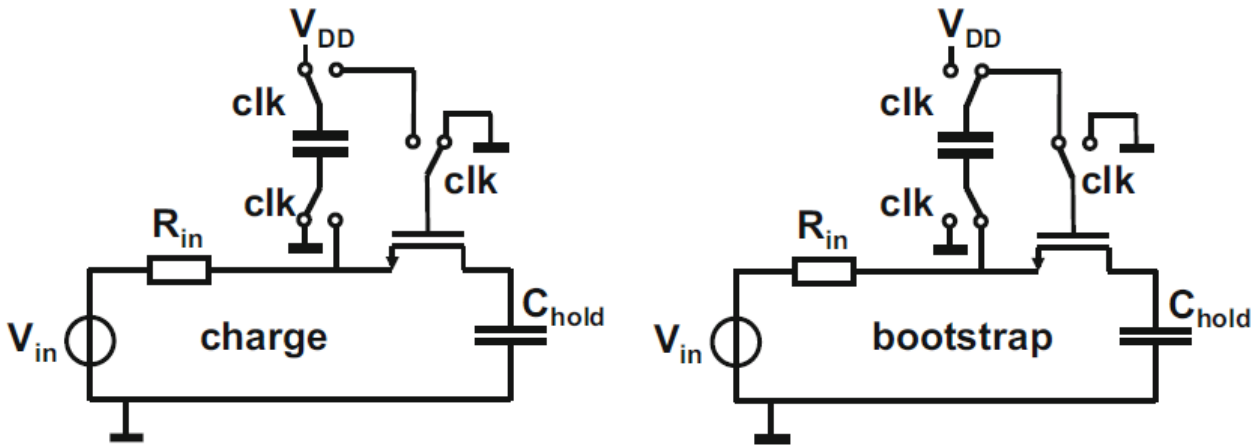




[M. Pelgrom, 2017]

Bootstrapping Principle

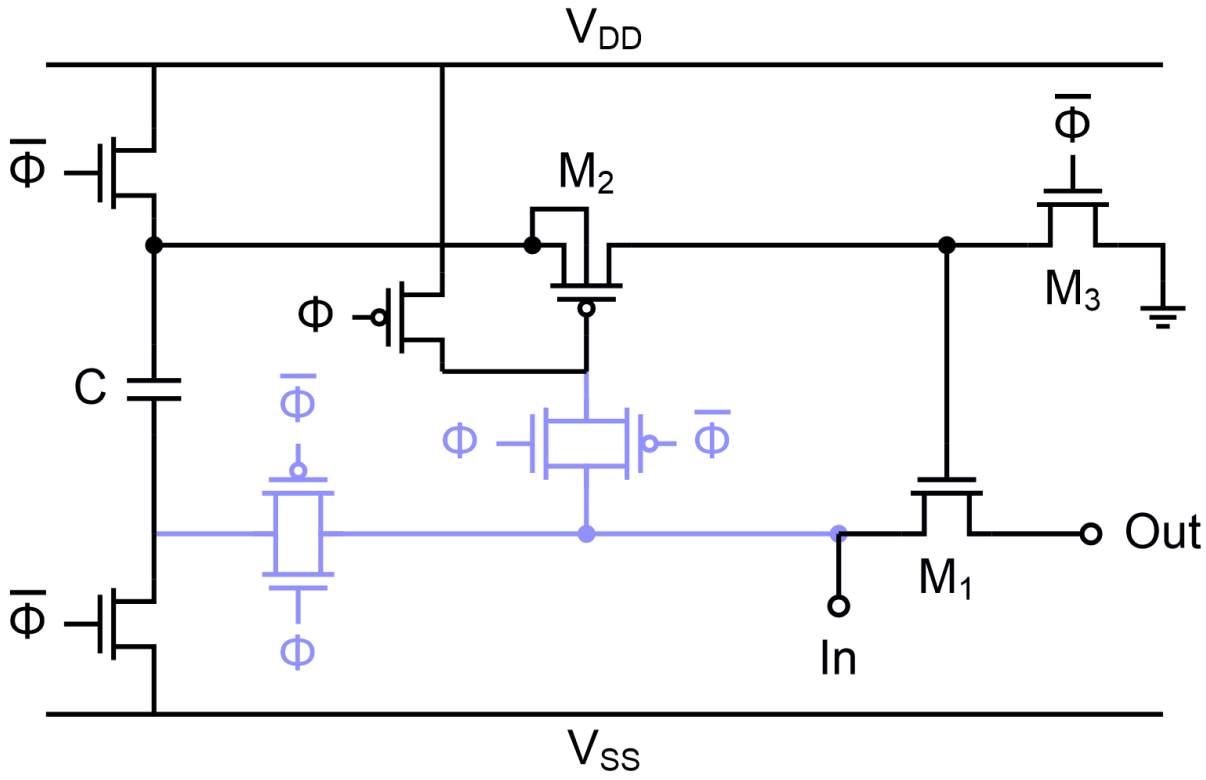
- Pros: VGS = constant = VDD
  - Less Ron variation with Vin → Better linearity and TBW
  - No need for TG (avoids PMOS large cap and parasitics)
  - Use smaller NMOS switch (less clock loading)
- Cons
  - Complexity, area, and power (see next slides)
  - Device reliability (voltages above VDD and/or below GND)
  - Residual error due to body effect



[M. Pelgrom, 2017]

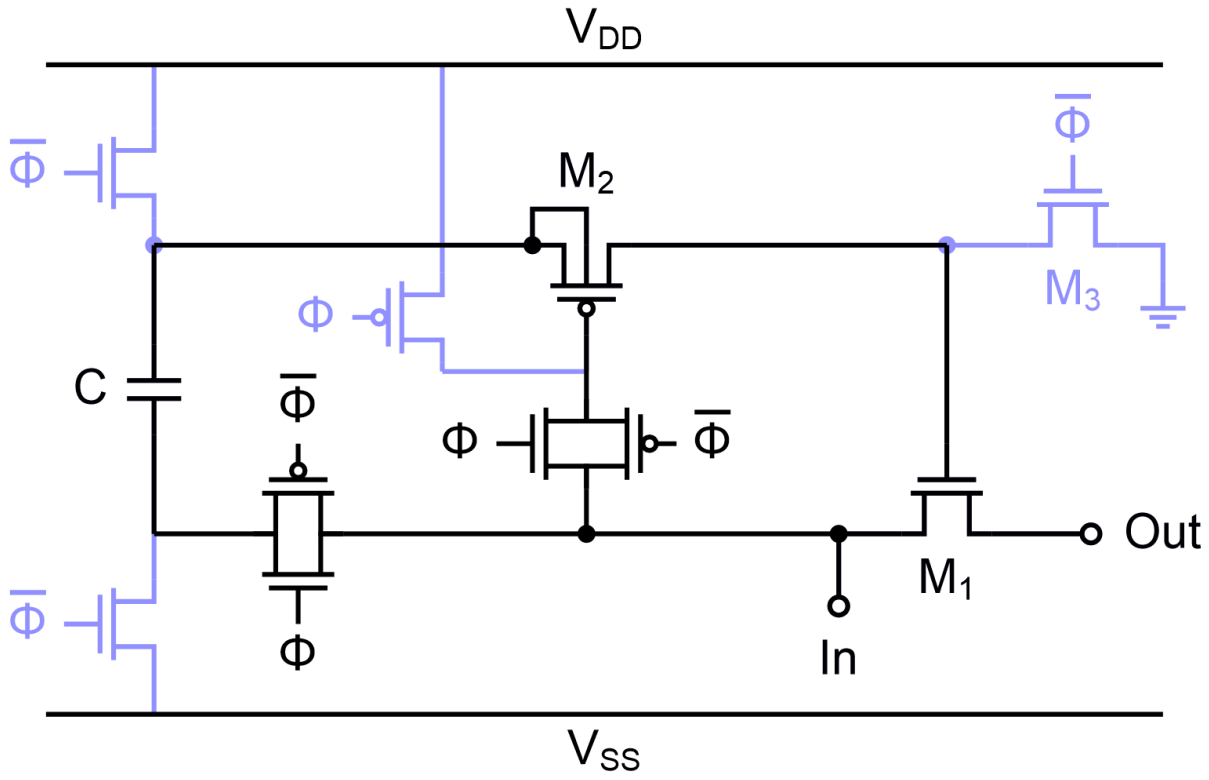
Bootstrapping Example (1)

- Hold Mode: $\Phi = 0$
  - C is precharged



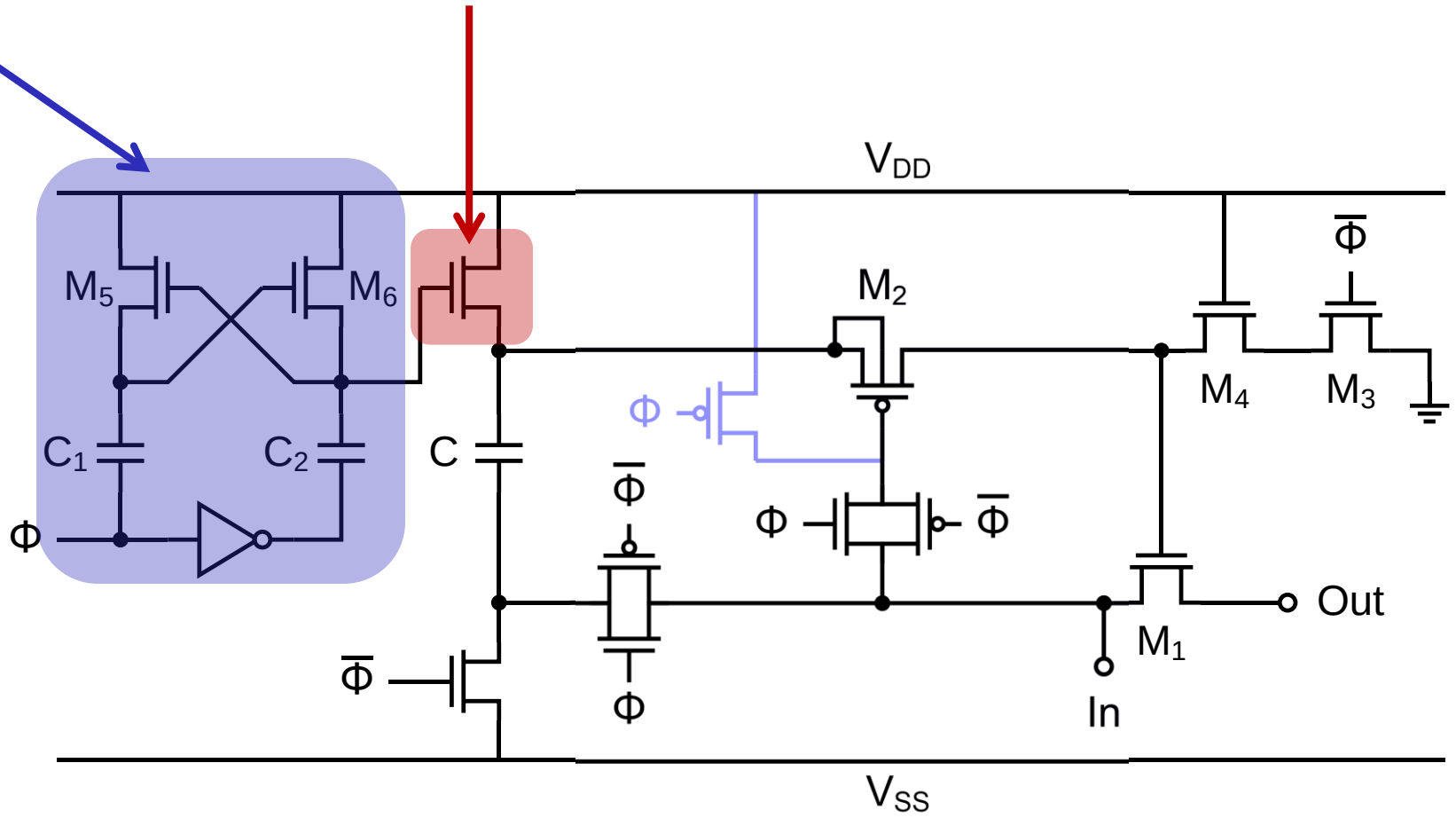
Bootstrapping Example (2)

- Track mode: $\Phi = 1$
  - VGS = constant = VDD



Bootstrapping Example (3)

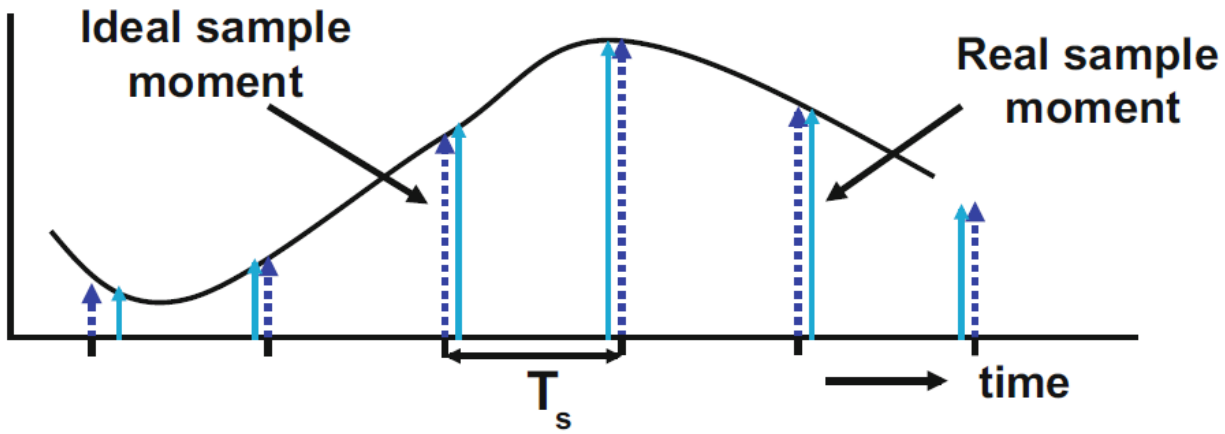
- Charge pump to drive the NMOS switch with $V_G > V_{DD}$



Sampling Jitter

- Jitter causes sample moments to shift from their position.
  - Can be viewed as noise in the time domain.

Part	Description	Jitter
"2011"	Quartz 50–170 MHz	3 ps_{rms}
"8002"	Programmable oscillator	25 ps_{rms}
"1028"	MEMS+PLL combi 100 MHz	95 ps_{rms}
"6909"	RC oscillator 20 MHz	0.2 %
"555"	RC oscillator/timer	>50 ns_{rms}



[M. Pelgrom, 2017]

Jitter vs Phase Noise (1)

- Variations in time (jitter) is equivalent to variations in phase (phase noise)

$$V_s = V_o \sin(\omega_s t) = V_o \sin(\theta)$$

$$\theta = \omega_s t = 2\pi f_s t$$

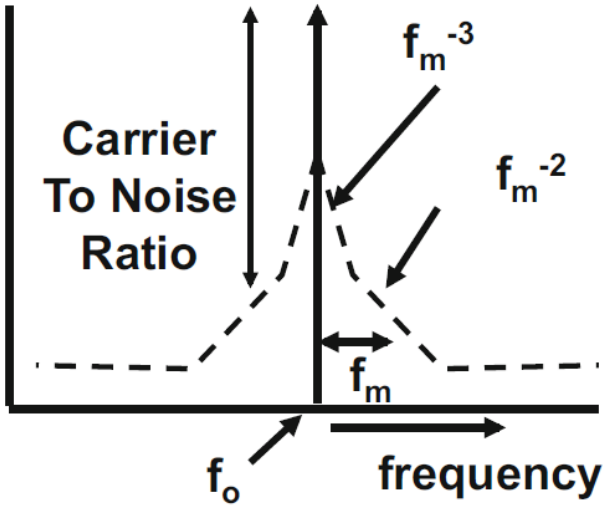
$$\frac{\theta}{2\pi} = \frac{t}{T_s}$$

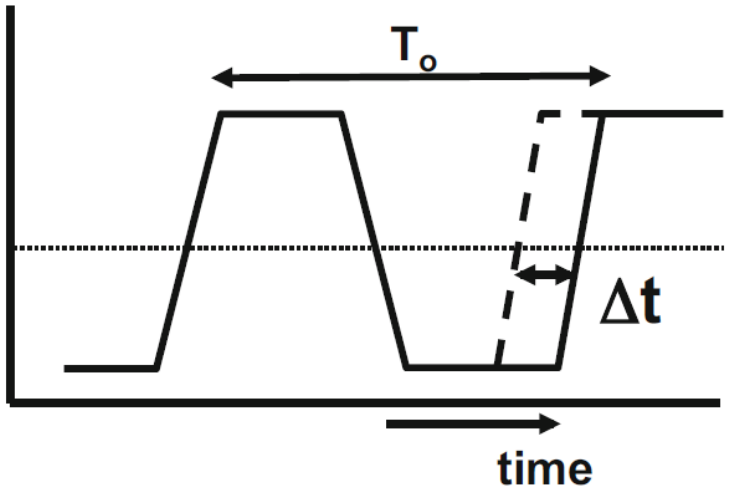
$$\frac{\Delta\theta}{2\pi} = \frac{\Delta t}{T_s}$$

$$\frac{\sigma_{\theta,rms}}{2\pi} = \frac{\sigma_{t,rms}}{T_s}$$

Jitter vs Phase Noise (2)

- Jitter in time domain is equivalent to Phase Noise in frequency domain.
- Jitter terminology usually used in sampled systems.
- Phase noise terminology usually used in RF systems.
  - Noise density is measured at an offset (f_m) w.r.t. the carrier frequency.
- BPF can reduce jitter levels to around 0.1 psrms.





[M. Pelgrom, 2017]

Jitter Limited SNR (1)

- Timing variations means amplitude variations
- Jitter limits the max attainable SNR

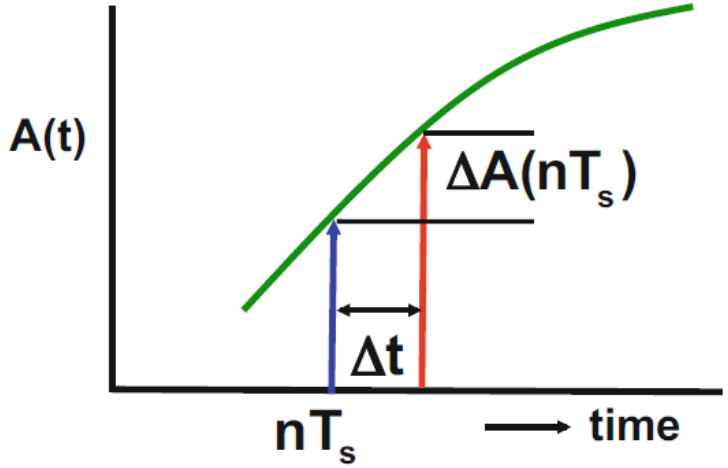
$$A(nT_s + \Delta t(t)) = \hat{A}\sin(\omega \times (nT_s + \Delta t(t))$$

$$\Delta A(nT_s) = \frac{d\hat{A}\sin(\omega t)}{dt} \times \Delta t(nT_s) = \omega\hat{A}\cos(\omega nT_s)\Delta t(nT_s)$$

$$\sigma_A^2(nT_s) = \left(\frac{dA(nT_s)}{dt}\right)^2 \sigma_t^2 = \omega^2\hat{A}^2\cos^2(\omega nT_s)\sigma_t^2$$

$$\sigma_A^2 = \frac{\omega^2\hat{A}^2\sigma_t^2}{2}$$

$$\text{SNR} = \frac{\text{P}_{\text{signal}}}{\text{P}_{\text{jitter}}} = \frac{\hat{A}^2/2}{\sigma_A^2} = \left(\frac{1}{\omega\sigma_t}\right)^2 = \left(\frac{1}{2\pi f\sigma_t}\right)^2$$

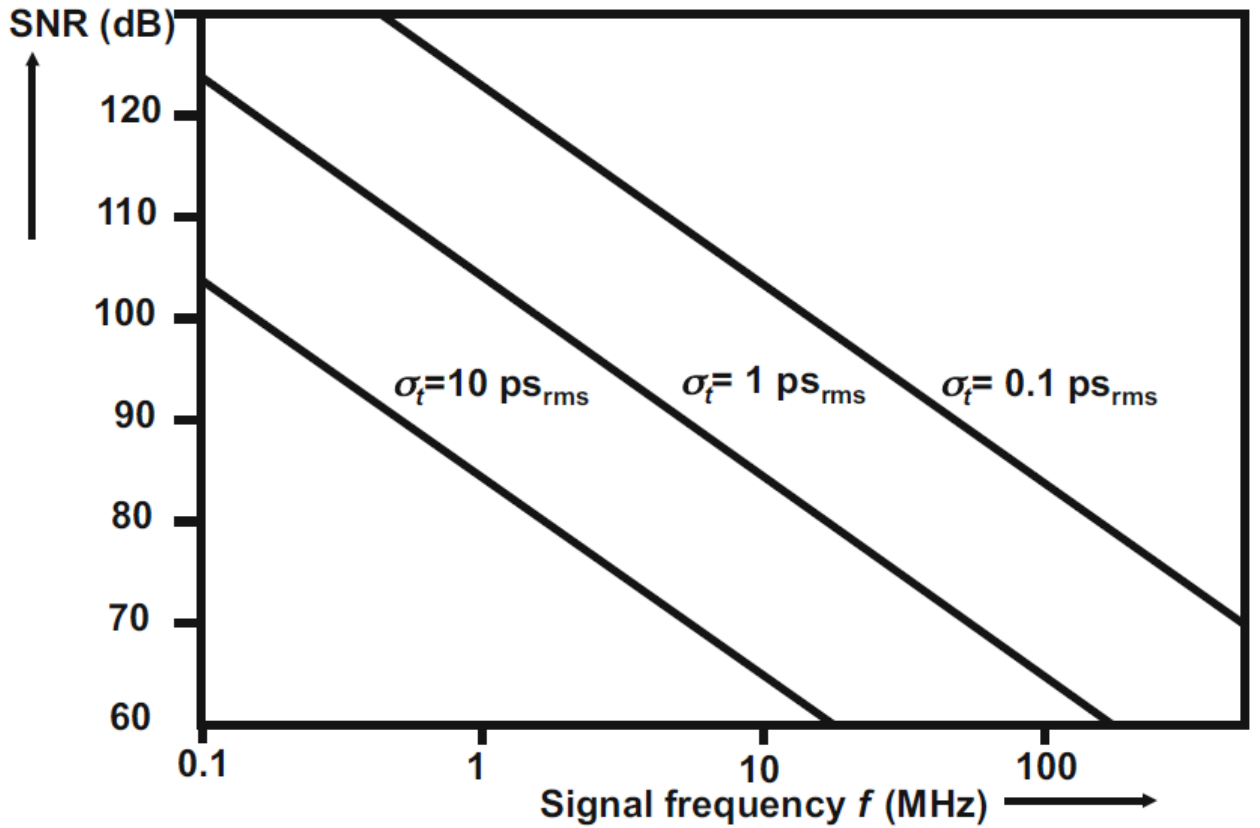


[M. Pelgrom, 2017]

Jitter Limited SNR (2)

$$\mathrm{SNR} = 20\,^{10}\log\left(\frac{1}{\omega\sigma_t}\right) = 20\,^{10}\log\left(\frac{1}{2\pi f\sigma_t}\right)$$

- Jitter can be a limiting factor for high-speed ADCs.



[M. Pelgrom, 2017]

T/H Performance Summary

$$SNDR = \frac{\overline{V_i^2}}{\overline{V_N^2} + \frac{A^2\omega^2}{2}\overline{\delta t^2} + \overline{V_\varepsilon^2}}$$

Noise

Jitter

Distortion

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- W. Kester, The Data Conversion Handbook, ADI, Newnes, 2005.
- B. Boser and H. Khorramabadi, EECS 247 (previously EECS 240), Berkeley.
- B. Murmann, EE 315, Stanford.
- Y. Chiu, EECT 7327, UTD.

Course Resources

Lectures	Labs	YouTube Channel

Thank you!