AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Department of Electronics and Communications Engineering
Credit Hours Engineering Program (CHEP)

1st Semester, 2019/2020	**Course Code: *ECE486***	***Time allowed: 3 Hrs.***

Analog Integrated Systems Design

The Exam Consists of **Four** Questions in **Three** Pages. ***Maximum Marks: 40 Marks*** **1 / 3**

تعليمات هامة

- حيازة التيلفون المحمول داخل لجنة الامتحان تعتبر حالة غش تستوجب العقاب، وإذا كان الدخول بالمحمول ضروريا فيلزم وضعه مغلقا فى الحقائب.
- لا يسمح بدخول سماعة الأذن أو البلوتوث.
- **يسمح لكل طالب باصطحاب ورقة واحدة فقط A4 بدون عليها الطالب ما يشاء (على الوجهين)، ويكتب عليها اسمه بالقلم الجاف.**
- لايسمح بدخول أي كتب أو ملازم أو أوراق داخل اللجنة **زيادة على ما ذكر** والمخالفة تعتبر حالة غش.

Question (1): [10 marks]

Choose the best answer and complete the missing dots:

a) Assume we want to build a 4th order Butterworth filter.
   - If we use RLC ladder filter, then the number of inductors needed is ……..
   - If we use Sallen-Key biquads, the number of op-amps needed is ……..
   - If we use Op-amp-MOSFET-RC CT integrator-based filter, the number of op-amps needed is ……..
   - If we use Op-amp-Gm-C CT integrator-based filter, then we need ……. transconductors in addition to ……. op-amps.

b) The number of comparators needed for a pipelined ADC stage is
   - ……. for 1-bit/stage.
   - ……. for 1.5-bit/stage.
   - ……. for 2-bit/stage.
   - ……. for 2.5-bit/stage.

c) For a given filter order, the smallest transition band is provided by **(Butterworth, Chebychev, Elliptic, Bessel)** filter, the maximally flat group delay is provided by ……. filter, a passband without ripples is provided by ……. filter.

d) The transfer function of a second-order LPF can be converted to a HPF by adding **(one pole, two poles, one zero, two zeros)**, and can be converted to a BPF by adding **(one pole, two poles, one zero, two zeros)**.

e) High frequency filters in the range of 100s of MHz are implemented using **(switched-capacitor, opamp-MOSFET-C, opamp-MOSFET-RC, Gm-C, LC)** filters, while filters in the range of 10s of GHz are implemented using **(switched-capacitor, opamp-MOSFET-C, opamp-MOSFET-RC, Gm-C, LC)** filters.

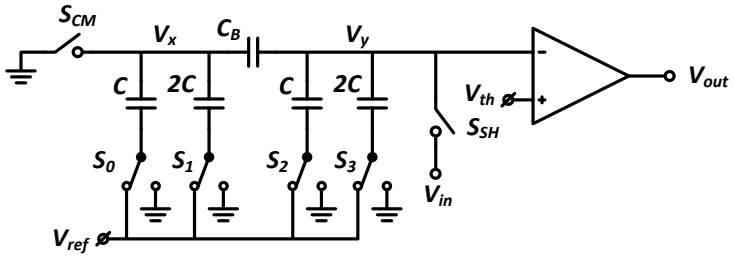
f) A state-of-the-art 10-bit ADC operating at 10 MS/s will have a Walden FoM around **($10\mu J/Step$, $10nJ/Step$, $10fJ/Step$, $10aJ/Step$)**, which translates to a power consumption around ……. W, and will be typically implemented using ……. architecture.

g) The theoretical limit of the maximum Schreier ADC FoM is **(162 dB, 172 dB, 182 dB, 192 dB)**.

Question (2): [13 marks]

The figure below shows partial implementation of a 4-bit SAR ADC with bridge capacitor. Answer the following questions.

Hint: It is suggested that you work in voltage domain, group capacitors in series/parallel when possible, apply superposition, and use simple capacitive divider formula when needed.



a) [1 mark] When S_{CM} and S_{SH} are switched off, is the charge injection error contributed by each of them linear or non-linear error? Why?

b) [1 mark] When S_3 is switched from V_{ref} to GND, show that the change at V_y is equal to $-\frac{8}{15}V_{ref}$.

c) [1 mark] What is voltage at V_y after S_3 is switched from V_{ref} to GND? Given your answer, suggest a suitable value for V_{th}.
Hint: When S_{CM} and S_{SH} are switched off, the voltages at V_x and V_y are unchanged.

d) [3 marks] Assume $V_{in} = 0$ and $V_{ref} = 1.5\ V$. Find the voltage at V_y when:
   i. S_0 is switched from V_{ref} to GND (other switches remain at V_{ref}).
   Hint: $\Delta V_y = \Delta V_x \cdot \frac{C}{4C}$. You can calculate ΔV_x using a simple capacitive divider.
   ii. S_1 is switched from V_{ref} to GND (other switches remain at V_{ref}).
   Hint: What is the relation between the capacitor of S_1 and the capacitor of S_0?
   iii. S_2 is switched from V_{ref} to GND (other switches remain at V_{ref}).

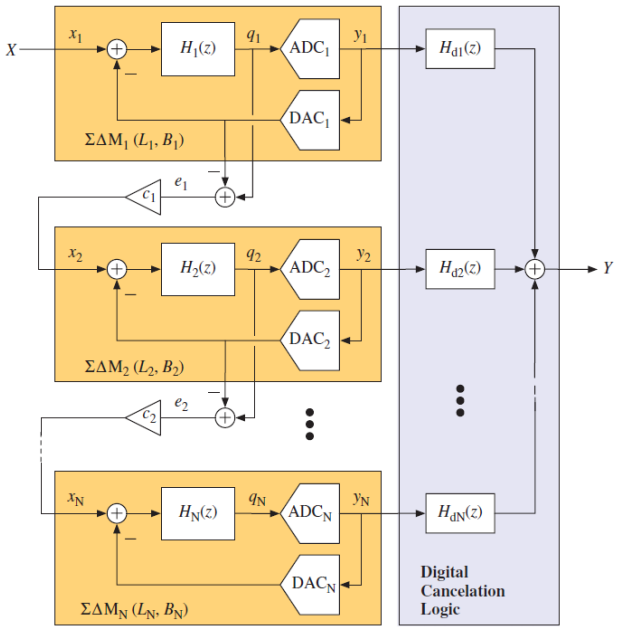
e) [3 marks] Repeat question (d) if there is a parasitic capacitor equal to C at V_x.

f) [3 marks] Repeat question (d) if there is a parasitic capacitor equal to C at V_y.

g) [1 mark] From the perspective of non-linear distortion, which node is more sensitive to parasitics: V_x *or* V_y? Why?
Hint: Try to estimate the DNL error due to the switching of S_0. Keep attention to the difference between gain error and non-linear error.

Question (3): [11 marks]

The opposite figure shows a generic implementation of a MASH ΣΔ ADC.



a) [2 marks] Draw the block diagram of a 2-1 topology. Write the transfer functions of the loop-filters in the block diagram.

b) [2 marks] Prove that in order to achieve 3rd order noise shaping $H_{d1}(z) = z^{-1}$ and $H_{d2}(z) = \frac{1}{c_1}(1 - z^{-1})^2$.
Hint: Start the derivation by assuming that the STFs are given by S_1 and S_2 and the NTFs are given by N_1 and N_2, then substitute with the actual formulas. Note that $X_2 = -c_1 E_1$.

c) [1 mark] c_1 is usually implemented as power of 2. Why?
Hint: $H_{d2}(z)$ is a digital filter implemented in the digital domain.

d) [1 mark] Write the final ADC output as a function of z.
e) [1 mark] If we use a 1-2 topology instead of a 2-1 topology, what will be the drawbacks?
f) [1 mark] Mention the main advantage and disadvantage of the 2-1 MASH implementation compared to a 3rd order modulator with distributed feedback.
g) [1 mark] Assume the signal bandwidth is 20 kHz, what sampling frequency is need for this 2-1 MASH modulator to get 18-bit resolution (assume single-bit quantizer)?
h) [2 marks] Repeat (f) if a 2nd order ΣΔM is used. From the perspective of power consumption and anti-aliasing filtering, mention the main advantage and disadvantage of choosing the 2nd order implementation compared to the 2-1 MASH for the required specs.

Hint: $SQNR = 10\,log\left(\frac{P_{sig}}{IBN}\right) \approx 1.76 + 6.02N + 10\,log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\,log(OSR)$

Question (4): [6 marks]

Considering the design of a 6-bit CMOS flash ADC, answer the following questions:

a) [1 mark] Assume the comparator offset is dominated by V_T mismatch of the input pair. If $\sigma_{V_T} = 4mV$ (given as the deviation between two identical transistors), calculate the standard deviation of the comparator offset voltage (σ_{os}).
b) [1 mark] Assume the comparator is composed of a preamplifier followed by a latch. If the preamplifier has $\sigma_{os,1} = 3mV$ and a gain of 5, what is the maximum tolerated $\sigma_{os,2}$ for the latch such that the overall $\sigma_{os,tot}$ is 5mV?
c) [2 marks] Assume the comparators have $\sigma_{os} = 3mV$, an ideal reference resistor string is used, and $V_{REF} = 1V$. What are the standard deviations of the ADC's worst case DNL and INL?
Hint: Note that the given sigma is for the comparator, not for the resistor string.
d) [1 mark] Assume $\sigma_{DNL} = 0.25LSB$. What DNL spec should go to the datasheet for the ADC to have 99.73% yield?
Hint: For a normal distribution, if C is the Confidence Interval and P is the probability, then $C = \sqrt{2}\,\mathrm{erf}^{-1}(P)$. Note that: $\mathrm{erf}^{-1}(0.9973) \approx 2.12$ and $\mathrm{erf}^{-1}(0.999958) \approx 2.896$.
e) [1 mark] Assume a BiCMOS process is available and BJT will be used for the comparator preamplifier. Mention the main advantage and disadvantage of this design decision.

End of Exam

دعواتي لكم بالتوفيق

Dr. Hesham Omran ***Exam Date: 10-Jan-2020***