وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog Integrated Systems Design

Lecture 14
Oversampling Data Converters (1)

Dr. Hesham A. Omran

Integrated Circuits Laboratory (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

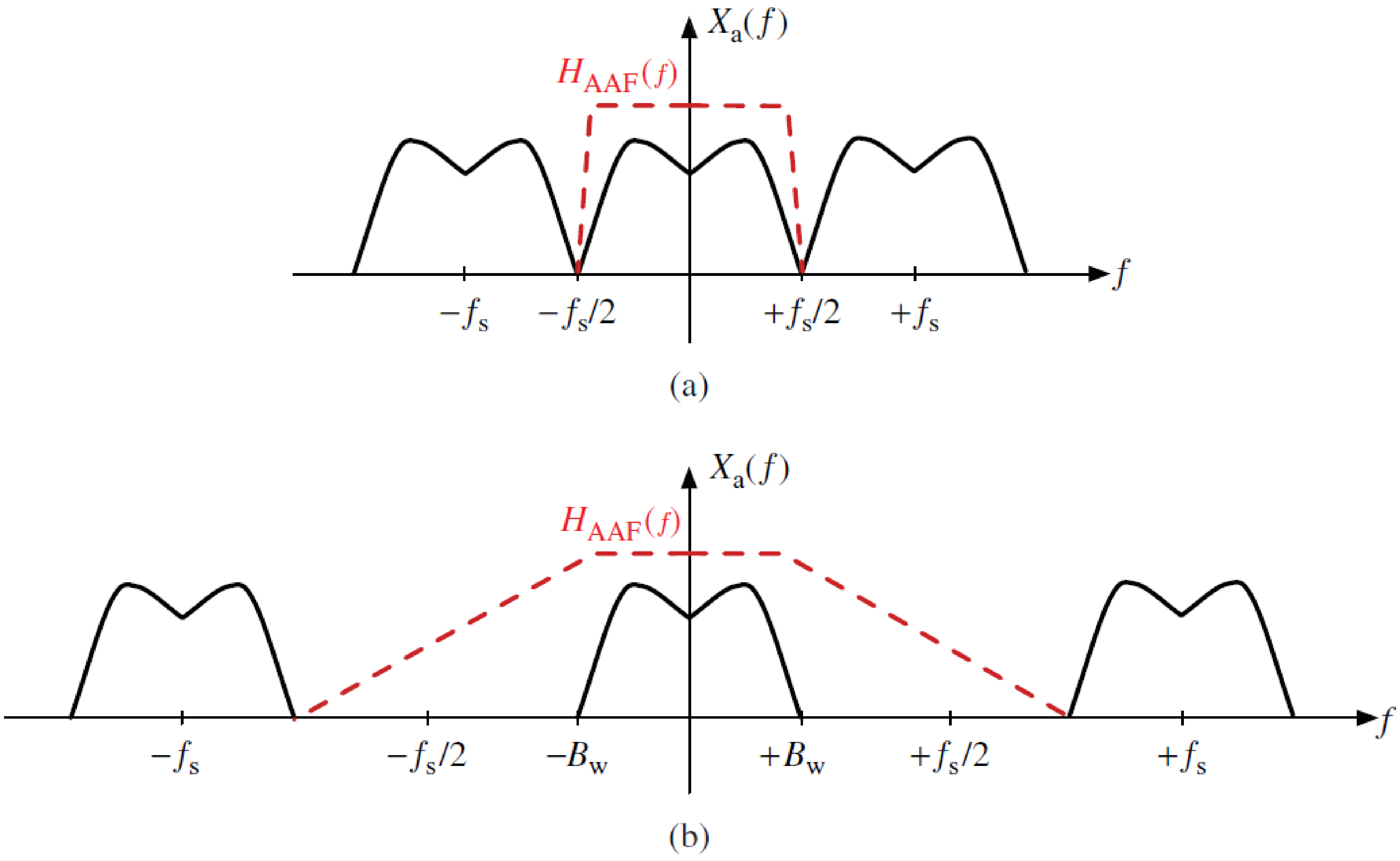
Why Oversampling?

- Technology scaling enable very fast MOS transistors
  - GHz sampling and processing is possible
  - We can build faster ADCs for broadband signals
- But signals in many applications have limited bandwidth
  - Ex: sensors (baseband) and communication systems (passband)
- Oversampling: $f_s \gg f_N = 2BW$
  - Make use of the high sample rate to improve the resolution
    - Oversampling Ratio (OSR)

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2BW}$$

  - Also simpler antialiasing filter
  - But higher digital power consumption

Nyquist vs Oversampling ADC



[J. M. de la Rosa and R. del Rio, 2013]

Quantization Error

- The quantization process generates an error signal
  - Strictly speaking, the quantization error is a distortion component

- But it can be approximated as white noise if:
  - The resolution N is sufficiently large
  - No correlation between the input signal and the sample rate
    - f_s not an integer multiple of f_{in}
    - Also the input is not a DC signal!

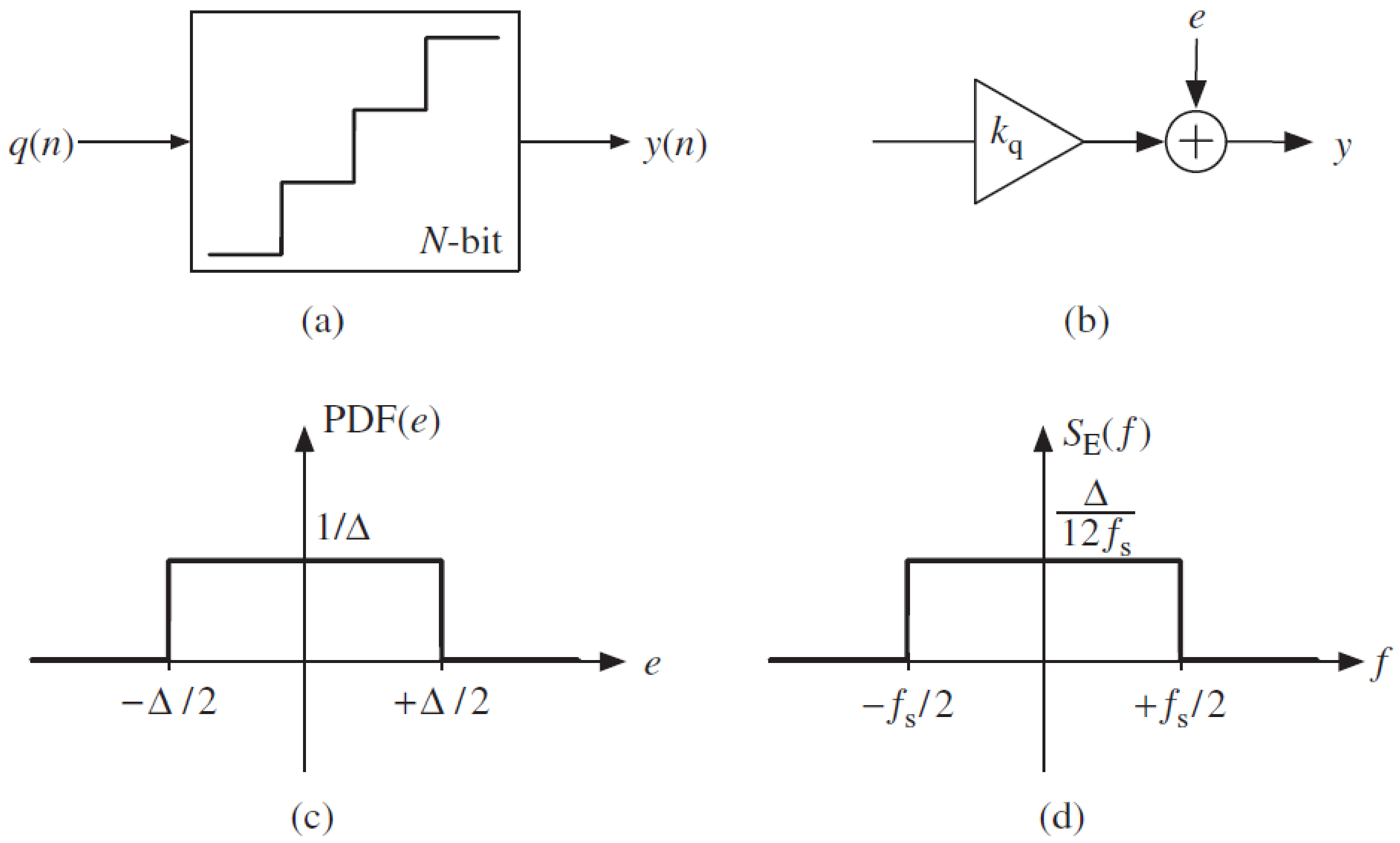
- The quantization noise power is given by

$$P_Q = \frac{V_{LSB}^2}{12} = \frac{\Delta^2}{12}$$

Quantization Linear Model

- Note the q(n) and e(n) are ANALOG signals. ONLY y(n) is quantized.

$$y(n) = k_q q(n) + e(n)$$



[J. M. de la Rosa and R. del Rio, 2013]

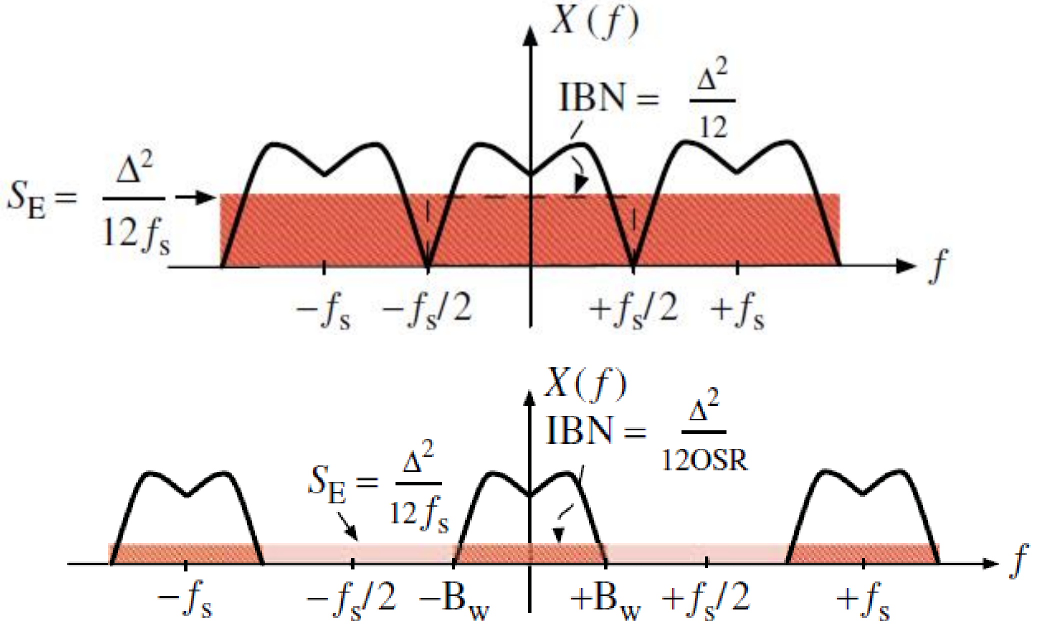
Oversampling Gain

$$SQNR = 10\log\left(\frac{Signal\ Power}{In\text{−}Band\ Noise\ (IBN)}\right) = 10\log\left(\frac{\left(2^N\Delta/2\right)^2/2}{\frac{\Delta^2}{12f_s}\times 2BW}\right)$$

$$= 1.76 + 6.02\times N + 10\log\left(\frac{f_s}{2BW}\right) = SQNR_{Nyq} + \mathbf{10\log(\mathit{OSR})}$$

$$\Delta ENOB = \frac{10\log(OSR)}{6} \approx 0.5\log_2(OSR)$$

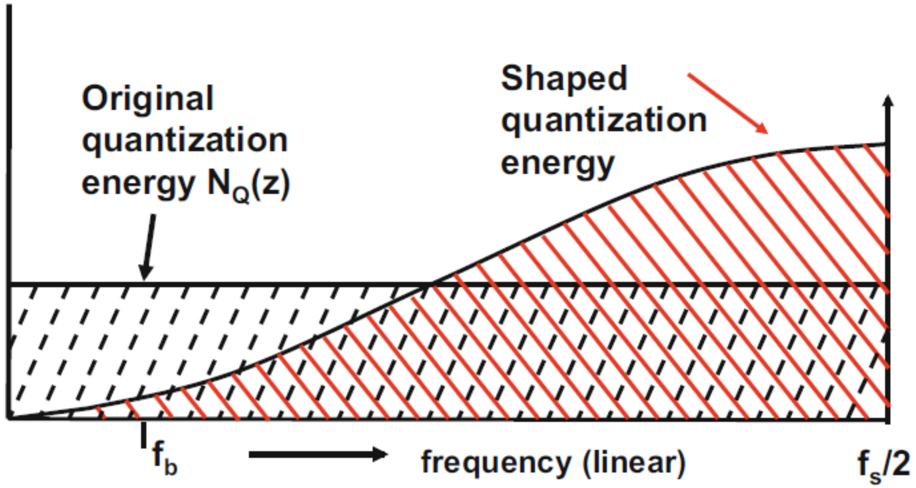
- ENOB improves by 3 dB/octave = 0.5 bit/octave



[J. M. de la Rosa and R. del Rio, 2013]

Noise Shaping

- Noise transfer function (NTF) is a HPF (differentiator)



- For 1st order NTF: The shaped noise has twice the noise power
  - But IBN is significantly reduced

[M. Pelgrom, 2017]

S-Plane vs Z-Plane

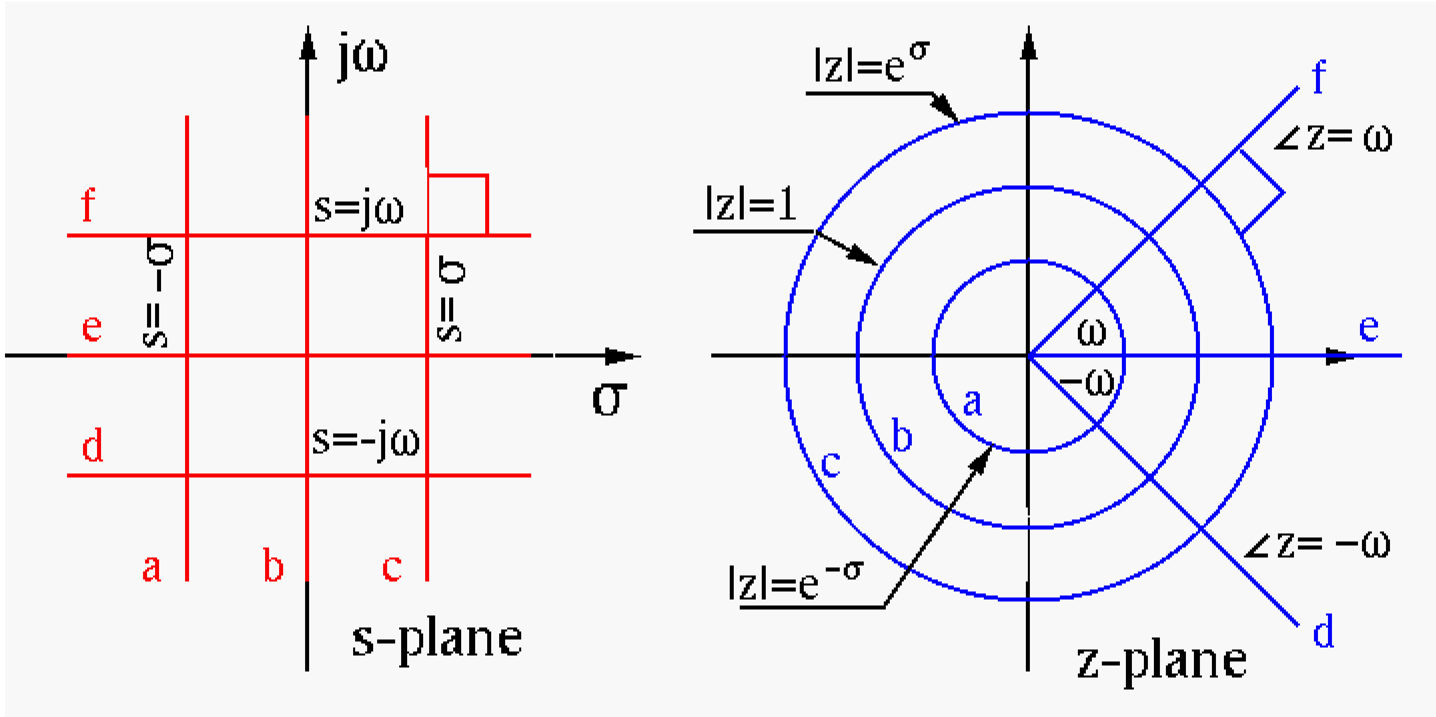
$$z = e^{sT_s} = e^{(\sigma + j\omega)/f_s}$$

- Assume $f_s = 1$ (normalized)

$$|z| = e^{\sigma}$$

$$\angle z = \omega$$

- RHP in s-domain maps to outside unit circle in z-domain



http://fourier.eng.hmc.edu/e102/lectures/Z_Transform/node2.html

1st Order LPF/Integrator in z-domain

- LPF → Integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z - 1}$$

  - No zeros
  - Pole at z = 1

Mapping s/z-domain to Frequency Domain

$$|H(s = j\omega)| = \left|\frac{1}{s+p}\right| = \frac{1}{\sqrt{\omega^2 + p^2}} = \frac{1}{\|\overrightarrow{ps}\|} = \frac{1}{\|\vec{s} - \vec{p}\|}$$

1st Order LPF in z-domain

- LPF → Integrator

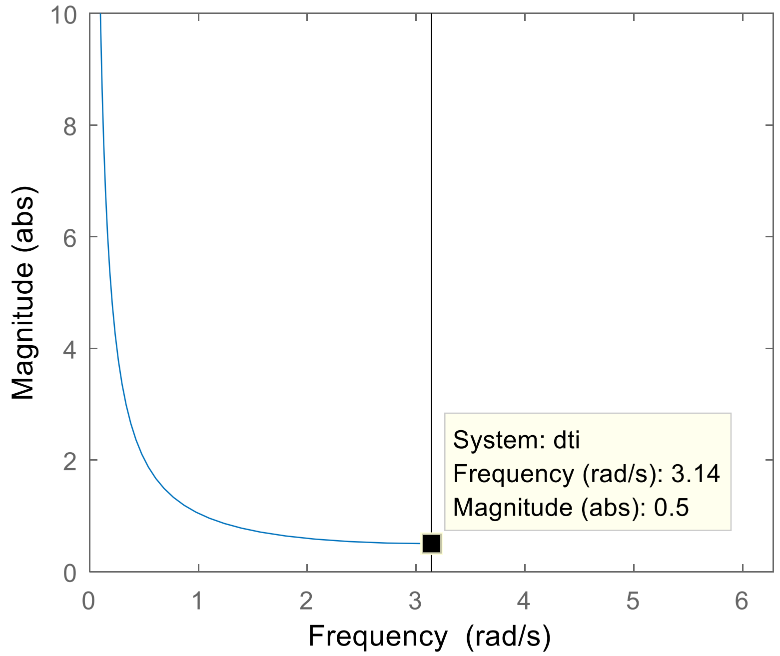
$$H(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z - 1}$$

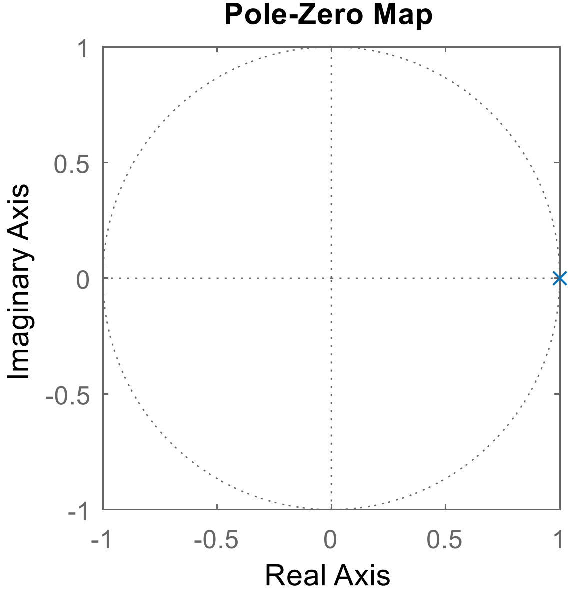
  - No zeros
  - Pole at z = 1
- Frequency response: evaluate H(z) along the unit circle:

$$z = e^{s} = e^{j\omega}$$

$$\left|H\left(e^{j\omega}\right)\right| = \frac{1}{\|\vec{z} - \vec{p}\|} = \frac{1}{\|\overline{pz}\|}$$

- Pole at 1 indicates infinite response at $\omega = 0$
  - A true pole since it lies on the unit circle
  - For ideal integrator, DC input grows indefinitely!





1^{st} Order LPF in z-domain

- LPF → Integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z - 1}$$

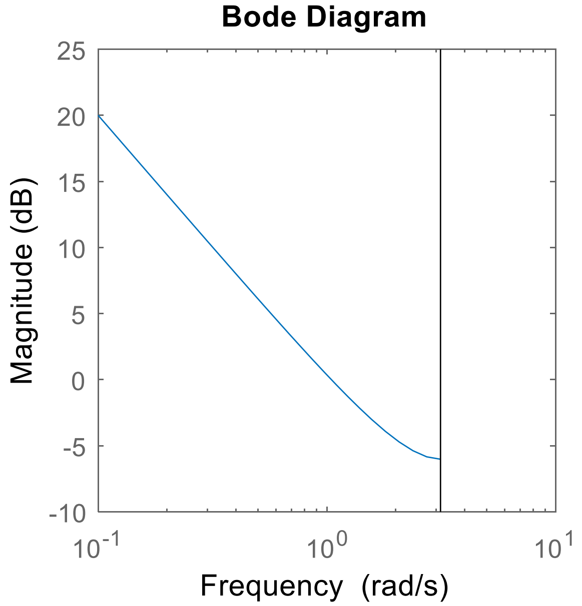
  - No zeros
  - Pole at z = 1

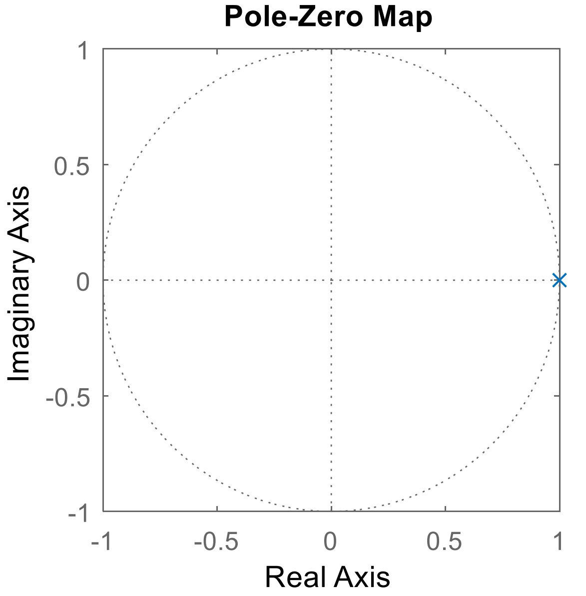
- Frequency response: evaluate H(z) along the unit circle:

$$z = e^{s} = e^{j\omega}$$

$$\left|H\left(e^{j\omega}\right)\right| = \frac{1}{\|\vec{z} - \vec{p}\|} = \frac{1}{\|\overline{pz}\|}$$

- Pole at 1 indicates infinite response at ω = 0
  - A true pole since it lies on the unit circle
  - For ideal integrator, DC input grows indefinitely!





1st Order HPF/Differentiator in z-domain

- HPF → Differentiator

$$H(z) = 1 - z^{-1} = 1 - \frac{1}{z} = \frac{z-1}{z}$$

  - Zero at z = 1
  - Pole at z = 0

1^{st} Order HPF in z-domain

- HPF → Differentiator

$$H(z) = 1 - z^{-1} = 1 - \frac{1}{z} = \frac{z-1}{z}$$

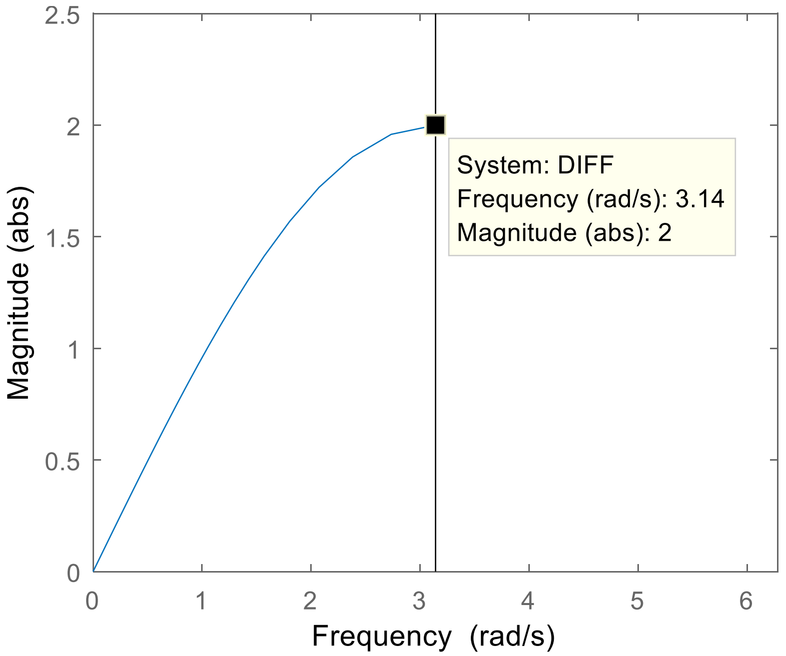
  - Zero at z = 1
  - Pole at z = 0

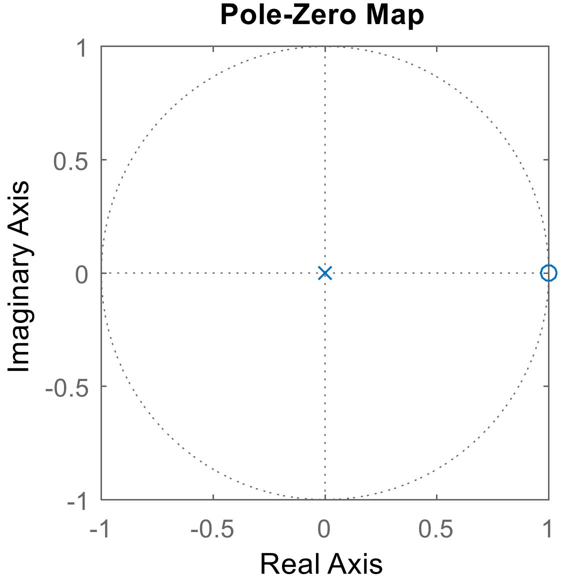
- Frequency response: evaluate H(z) along the unit circle:

$$z = e^{s} = e^{j\omega}$$

$$\left|H\left(e^{j\omega}\right)\right| = \frac{\|\vec{z} - \overrightarrow{z_1}\|}{\|\vec{z} - \overrightarrow{p_1}\|} = \frac{\|\overrightarrow{z_1 z}\|}{\|\overrightarrow{p_1 z}\|}$$

- Poles/zeros at origin do not affect magnitude response
- Zero at 1 indicate a stopband at ω = 0
  - A true zero since it lies on the unit circle: Block DC





1^{st} Order HPF in z-domain

- HPF → Differentiator

$$H(z) = 1 - z^{-1} = 1 - \frac{1}{z} = \frac{z-1}{z}$$

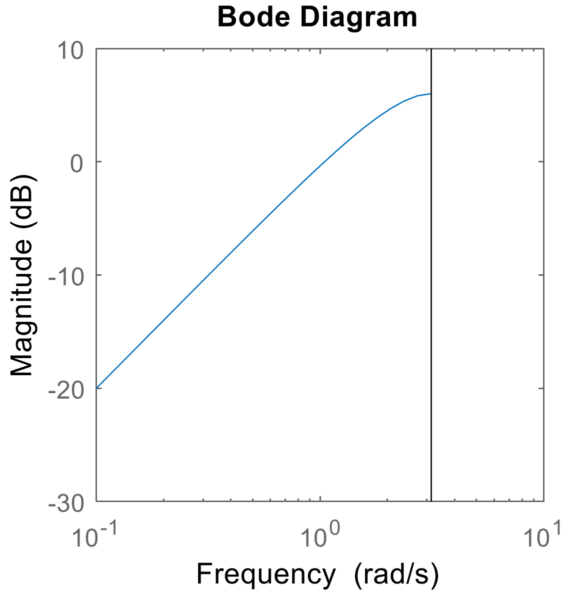
  - Zero at z = 1
  - Pole at z = 0

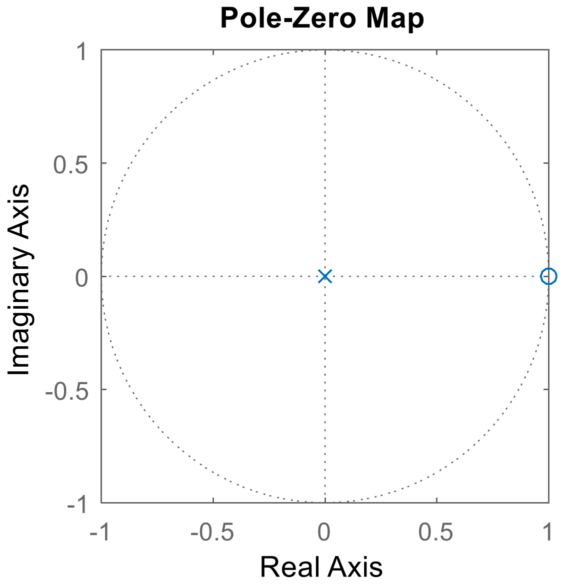
- Frequency response: evaluate H(z) along the unit circle:

$$z = e^{s} = e^{j\omega}$$

$$\left|H\left(e^{j\omega}\right)\right| = \frac{\|\vec{z} - \overrightarrow{z_1}\|}{\|\vec{z} - \overrightarrow{p_1}\|} = \frac{\|\overrightarrow{z_1 z}\|}{\|\overrightarrow{p_1 z}\|}$$

- Poles/zeros at origin do not affect magnitude response
- Zero at 1 indicate a stopband at ω = 0
  - A true zero since it lies on the unit circle: Block DC





Noise Shaping

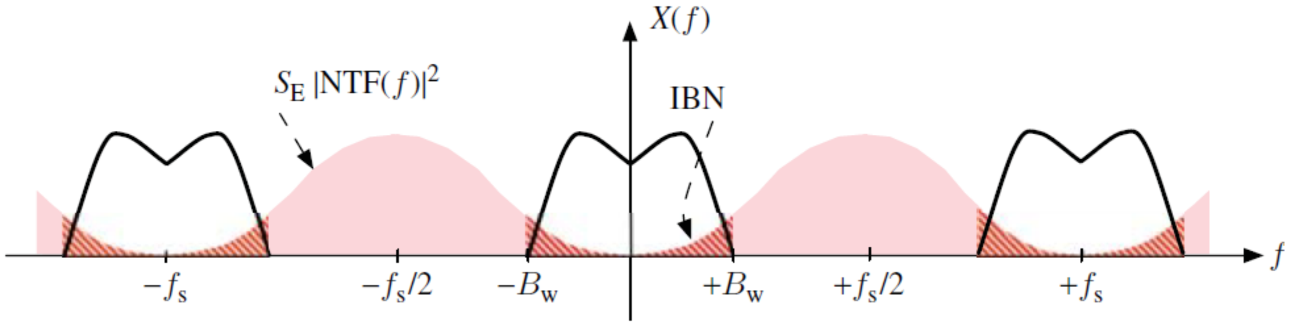
- Noise transfer function (NTF) is a HPF (differentiator)

$$NTF(z) = (1 - z^{-1})^L$$

$$z = e^s = e^{j\omega} = e^{j2\pi f/f_s}$$

$$|NTF(f)| = \left|1 - e^{-j\omega}\right|^L = \left[2\sin\left(\frac{\omega}{2}\right)\right]^L \approx (\omega)^L \approx \left(\frac{2\pi f}{f_s}\right)^L$$

- For 1st order HPF ($L = 1$): $|NTF(f)|^2 \approx \left(\frac{2\pi f}{f_s}\right)^2$



[https://webhome.phy.duke.edu/~rgb/Class/phy51/phy51/node15.html] [J. M. de la Rosa and R. del Rio, 2013]

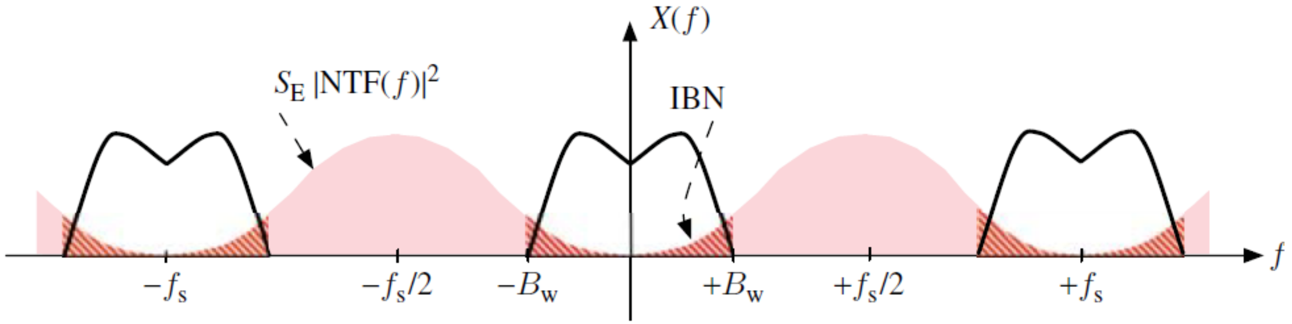
Noise Shaping Gain

$$|NTF(f)| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L \approx \left(\frac{2\pi f}{f_s}\right)^L$$

$$IBN = \int_{-BW}^{BW} \frac{\Delta^2}{12 f_s} |NTF(f)|^2 df \approx \frac{\Delta^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}$$

$$SQNR = 10\log\left(\frac{P_{sig}}{IBN}\right)$$

$$\approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2L+1}{\pi^{2L}}\right)} + \mathbf{(2L+1)10\log(OSR)}$$



[J. M. de la Rosa and R. del Rio, 2013]

Noise Shaping Gain

$$SQNR \approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2L+1}{\pi^{2L}}\right)} + \mathbf{(2L+1)10\log(OSR)}$$

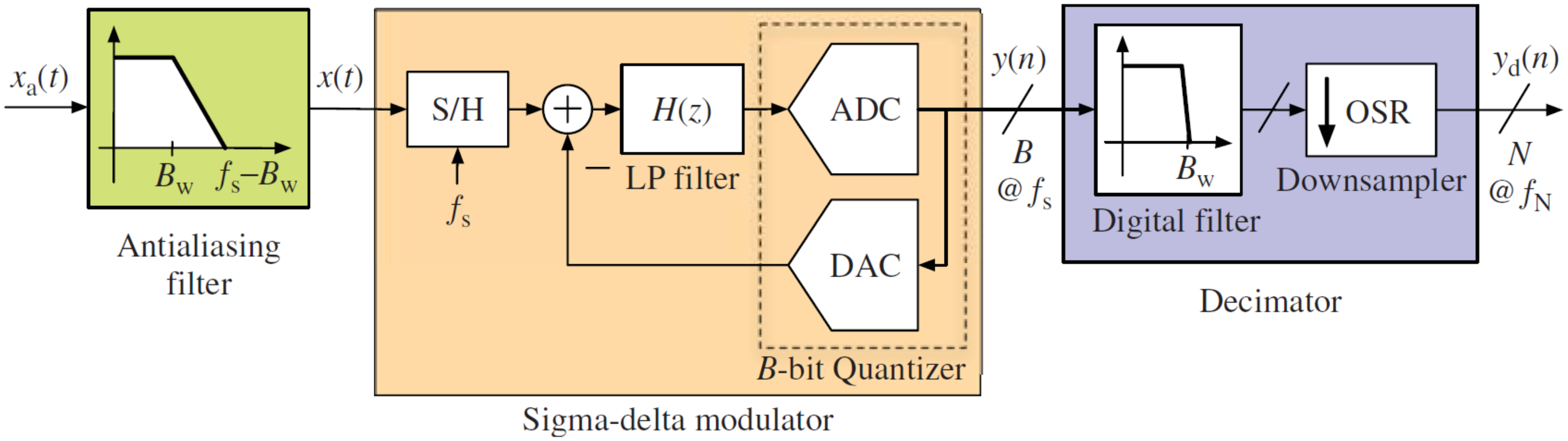
$$ENOB\ Gain = \frac{\mathbf{(2L+1)10\log(OSR)}}{6} \approx \mathbf{(2L+1)} \times 0.5\log_2(OSR)$$

- SNQR increases with OSR by $3(2L+1)$ dB/octave
- ENOB increases with OSR by $(L+0.5)$ bit/octave
- Need OSR > 4 (more than two octaves) to reap $\boldsymbol{\Sigma\Delta}$**M** benefits

Order (L)	Static SNR loss	SNR gain	Static ENOB loss	ENOB gain
0	0	3 dB/octave	0	0.5 bit/octave
1	-5.2 dB	9 dB/octave	-0.86 bit	1.5 bit/octave
2	-12.9 dB	15 dB/octave	-2.14 bit	2.5 bit/octave
3	-21.4 dB	21 dB/octave	-3.55 bit	3.5 bit/octave
4	-30.2 dB	27 dB/octave	-5.02 bit	4.5 bit/octave

Sigma-Delta (ΣΔ) ADC

- Closed loop negative feedback system
- $H(z)$ is the loop filter
- The B-bit quantizer is typically $1-5$ bit
  - Single bit: One bit DAC is inherently linear
    - We care more about DAC linearity (we will know why later)
  - Multibit: Each bit in the ADC/DAC adds 6dB to the SNR

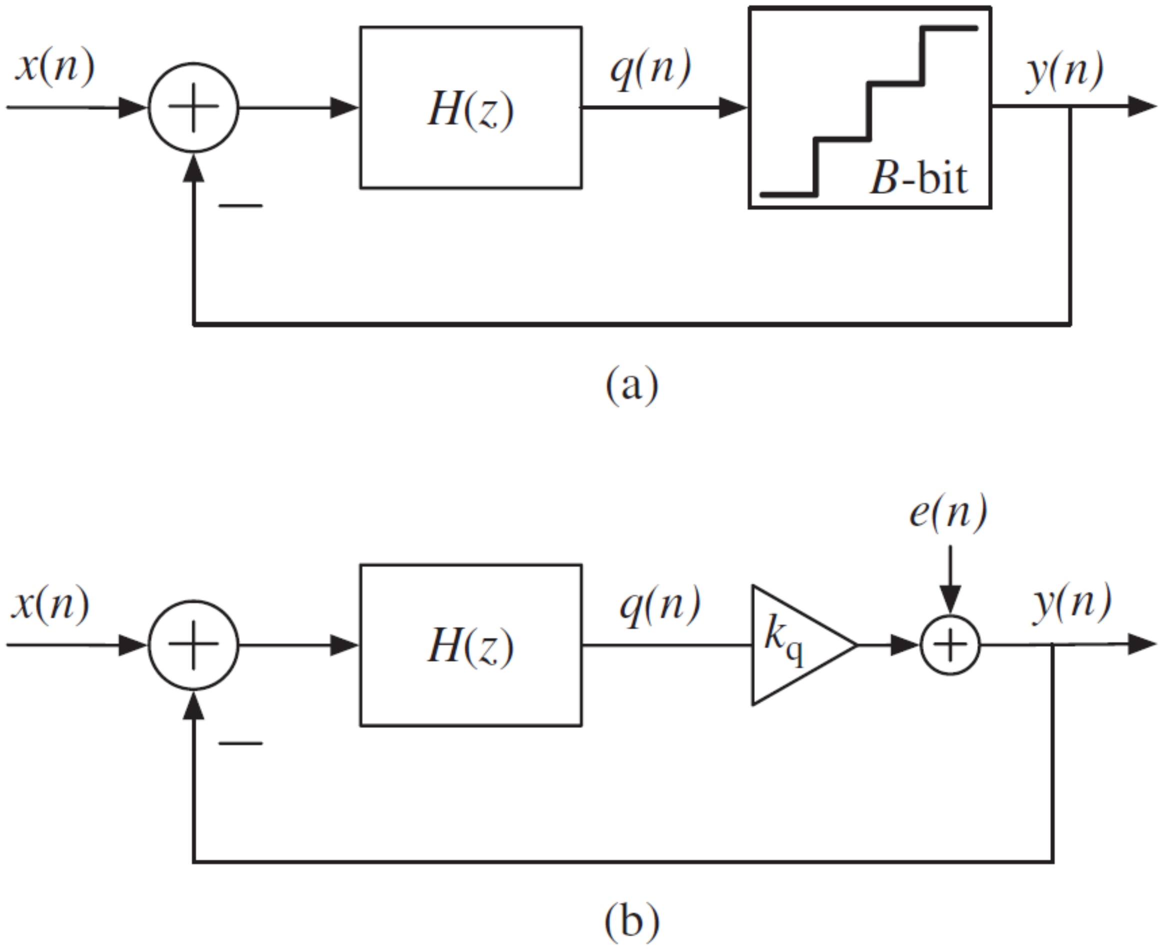


[J. M. de la Rosa and R. del Rio, 2013]

Negative Feedback Reminder

Sigma-Delta Modulator ($\Sigma\Delta\mathbf{M}$)

- ❑ The negative feedback action will minimize the error between $x(n)$ and $y(n)$



[J. M. de la Rosa and R. del Rio, 2013]

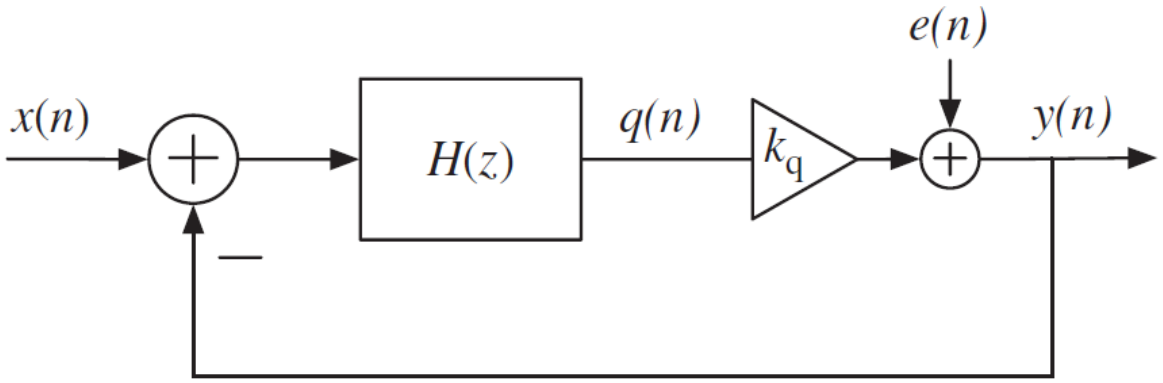
Sigma-Delta Modulator ($\boldsymbol{\Sigma\Delta\mathrm{M}}$)

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}}$$

$$STF(z) = \frac{Y}{X} = \frac{k_q H(z)}{1+k_q H(z)} \quad \rightarrow \quad |STF(z)| \approx 1$$

$$NTF(z) = \frac{Y}{E} = \frac{1}{1+k_q H(z)} \quad \rightarrow \quad |NTF(z)| \ll 1$$

- For $e(n)$ to see a HPF (noise shaping), $H(z)$ must be a LPF (integrator)



[J. M. de la Rosa and R. del Rio, 2013]

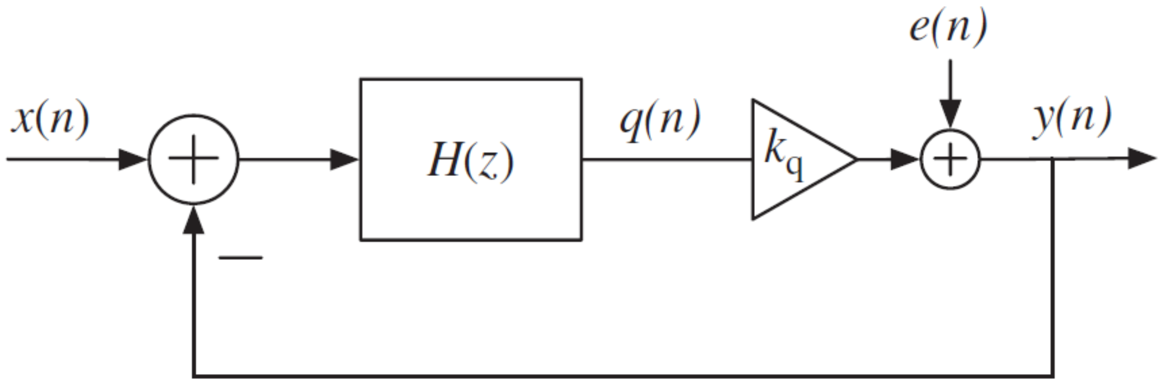
First-Order ΣΔM

Let $H(z) = \frac{z^{-1}}{1-z^{-1}}$ and $k_q = 1$

$$STF(z) = \frac{H(z)}{1+H(z)} = z^{-1}$$ ➔ Delay

$$NTF(z) = \frac{1}{1+H(z)} = 1 - z^{-1}$$ ➔ Noise shaping

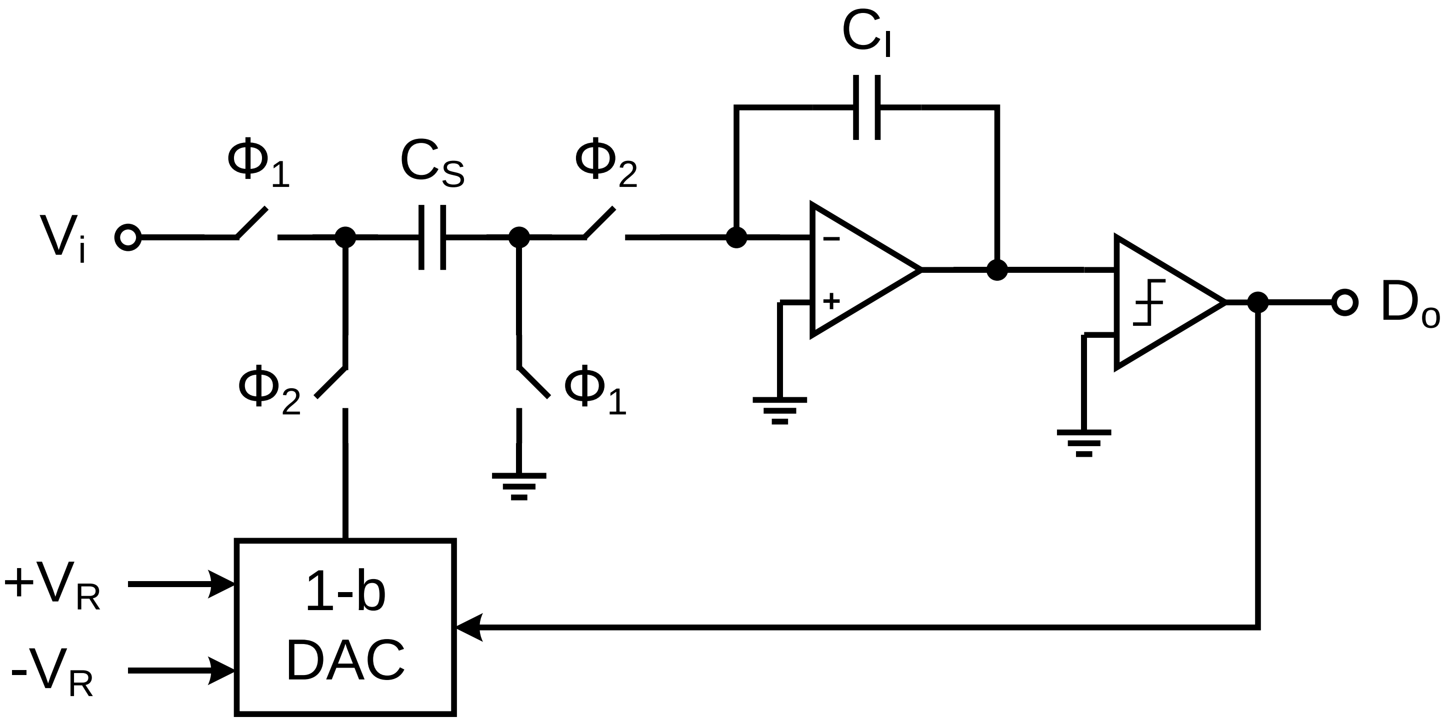
$$Y = STF \cdot X + NTF \cdot E = z^{-1} \cdot X + (1 - z^{-1}) \cdot E$$



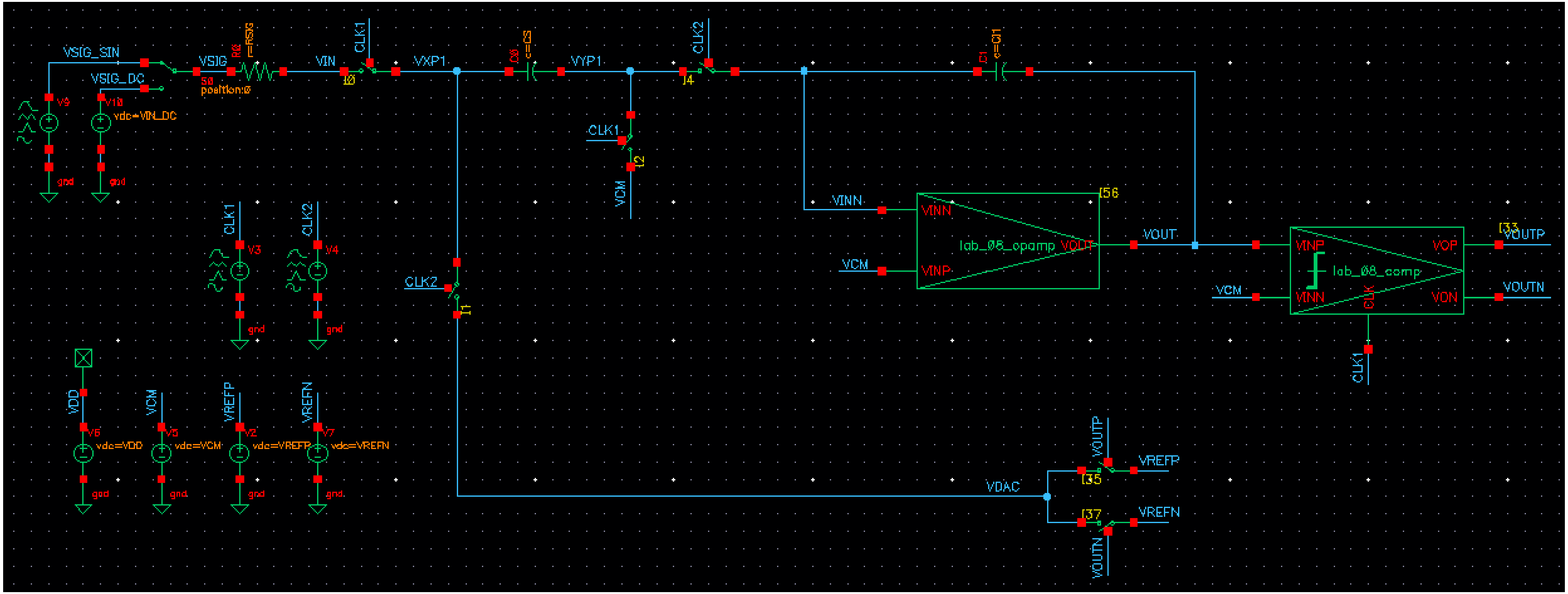
[J. M. de la Rosa and R. del Rio, 2013]

First-Order $\Sigma\Delta\mathbf{M}$: SC Implementation

- SC integrator
- 1-bit ADC → simple, ZX detector
- 1-bit feedback DAC → simple, inherently linear



First-Order ΣΔM: SC Implementation

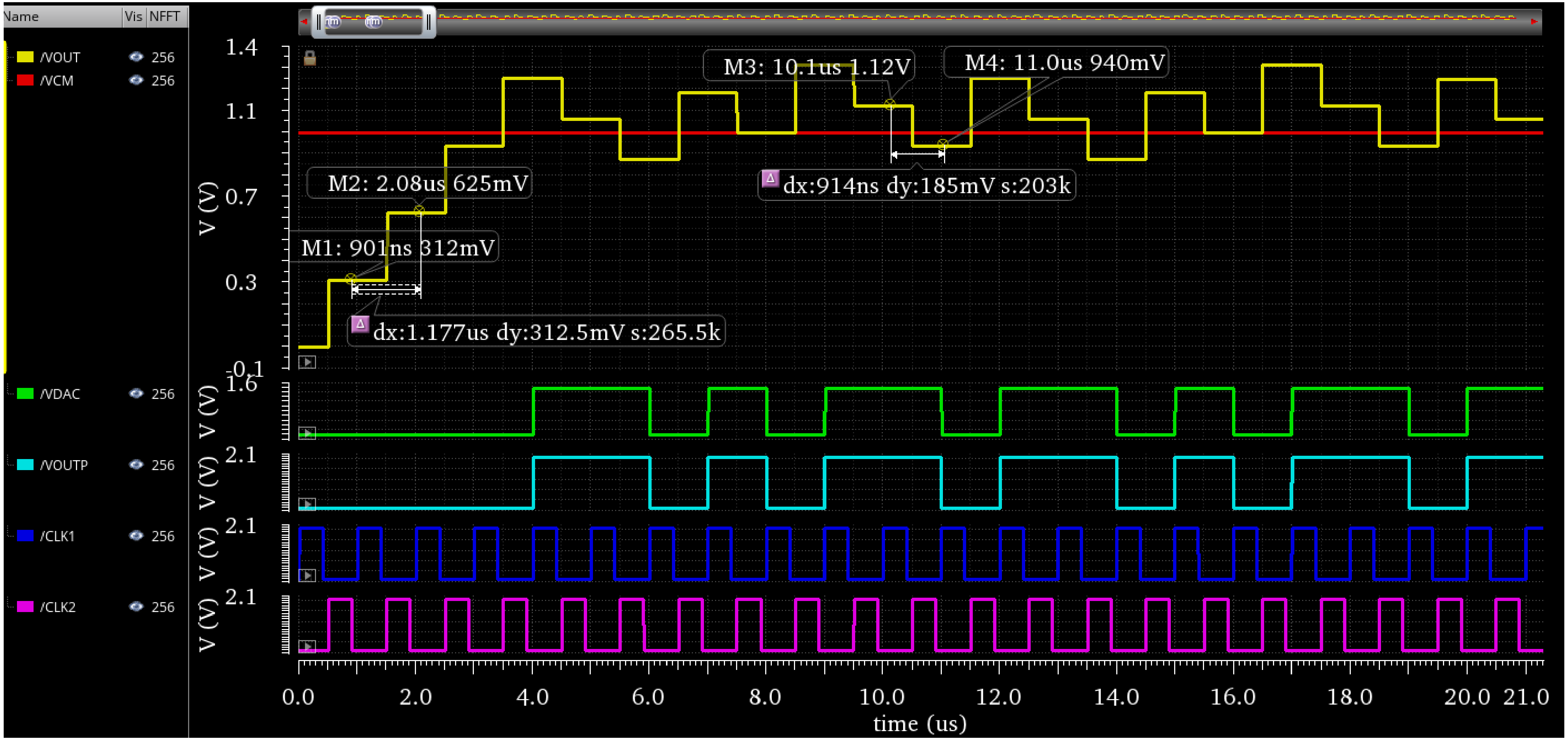


DC Input Simulation Parameters

CI1	2p
CS	1p
TS	1u
TON	0.4*TS
VDD	2
VCM	0.5*(VREFP + VREFN)
VREFP	0.75*VDD = 1.5
VREFN	0.25*VDD = 0.5
OSR	2**5
VIN_DC	0.625*(VREFP – VREFN) + VREFN
TSTOP	2*OSR*TS
SW_POS	2

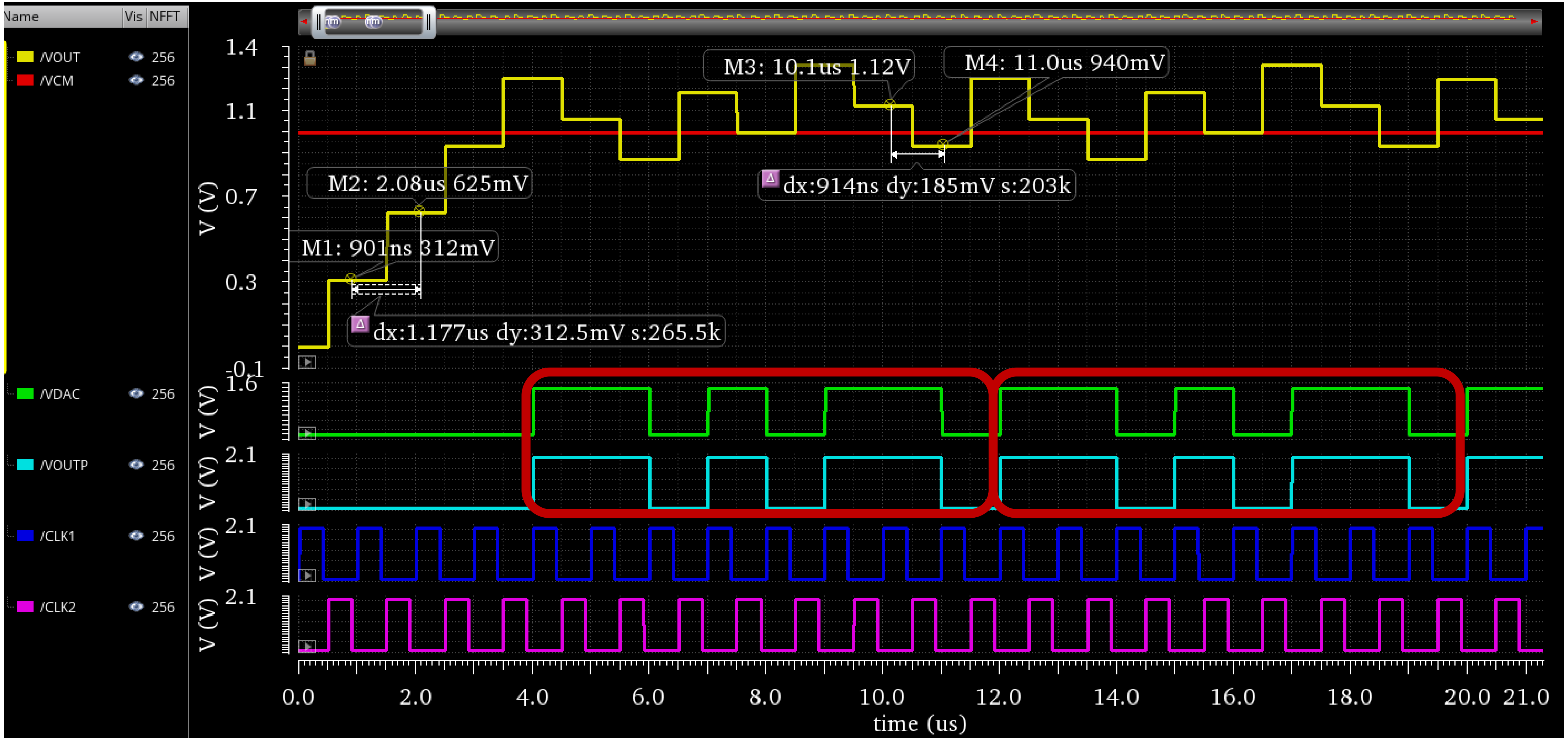
First-Order ΣΔM: Response to DC Input

- *Output step* = $(V_{in} - V_{DAC}) \times C_S/C_{I1} = [(0.625 + 0.5) - (0.5/1.5)] \times 0.5$
  $[0.625/-0.375] \times 0.5 = +312.5m/-187.5m$



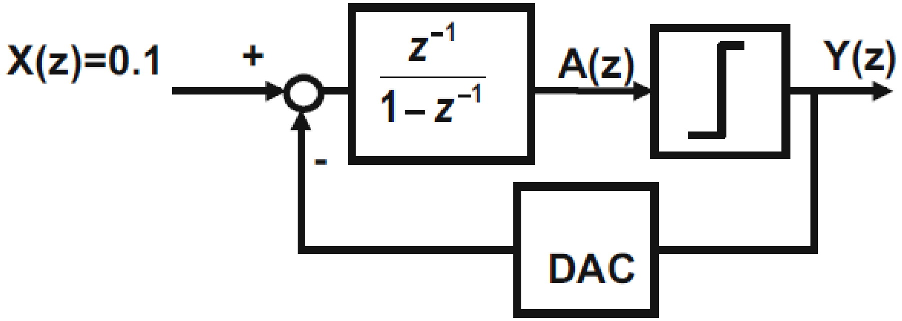
First-Order ΣΔM: Response to DC Input

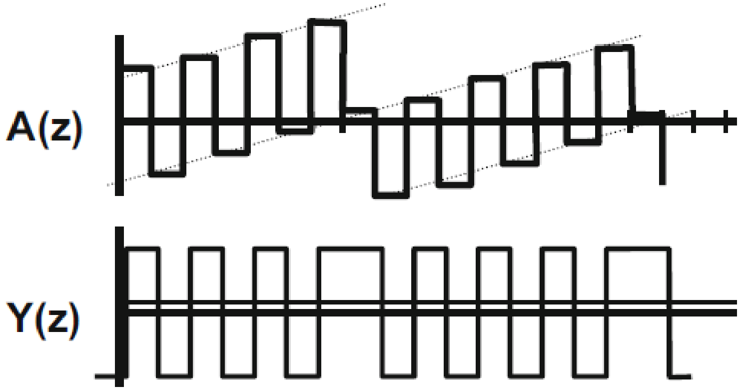
- Average DAC output $= (1.5V \times 5 + 0.5V \times 3)/8 = 9/8 = 1.125V = V_{in}$ (-ve FB action)
- Average COMP output $= (2V \times 5 + 0V \times 3)/8 = 10/8 = 1.25V = 0.625V_{DD}$

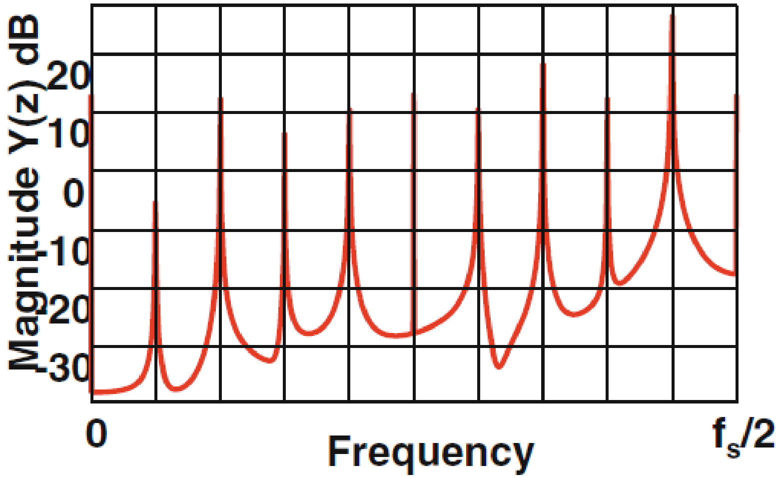


Idle Tones

- The low frequency repetitive pattern in the output creates unwanted tones
- With higher-order modulators or the addition of helper signals (dither) these tones are reduced to acceptable levels.







[M. Pelgrom, 2017]

Higher-Order ΣΔM

Let $H(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right)^L$ and $k_q = 1$

$$STF(z) = \frac{H(z)}{1+H(z)} = z^{-L} \quad \Rightarrow \quad \text{Delay}$$

$$NTF(z) = \frac{1}{1+H(z)} = (1-z^{-1})^L \quad \Rightarrow \quad \text{Noise shaping}$$

$$Y = STF \cdot X + NTF \cdot E = z^{-L} \cdot X + (1-z^{-1})^L \cdot E$$

$$SQNR = 10\log\left(\frac{P_{sig}}{IBN}\right)$$

$$\approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2L+1}{\pi^{2L}}\right)} + \mathbf{(2L+1)10\log(OSR)}$$

Noise Shaping Gain

$$SQNR \approx 1.76 + 6.02N + \mathbf{10\log\left(\frac{2L+1}{\pi^{2L}}\right)} + \mathbf{(2L+1)10\log(OSR)}$$

$$ENOB\ Gain = \frac{\mathbf{(2L+1)10\log(OSR)}}{6} \approx \mathbf{(2L+1)} \times 0.5\log_2(OSR)$$

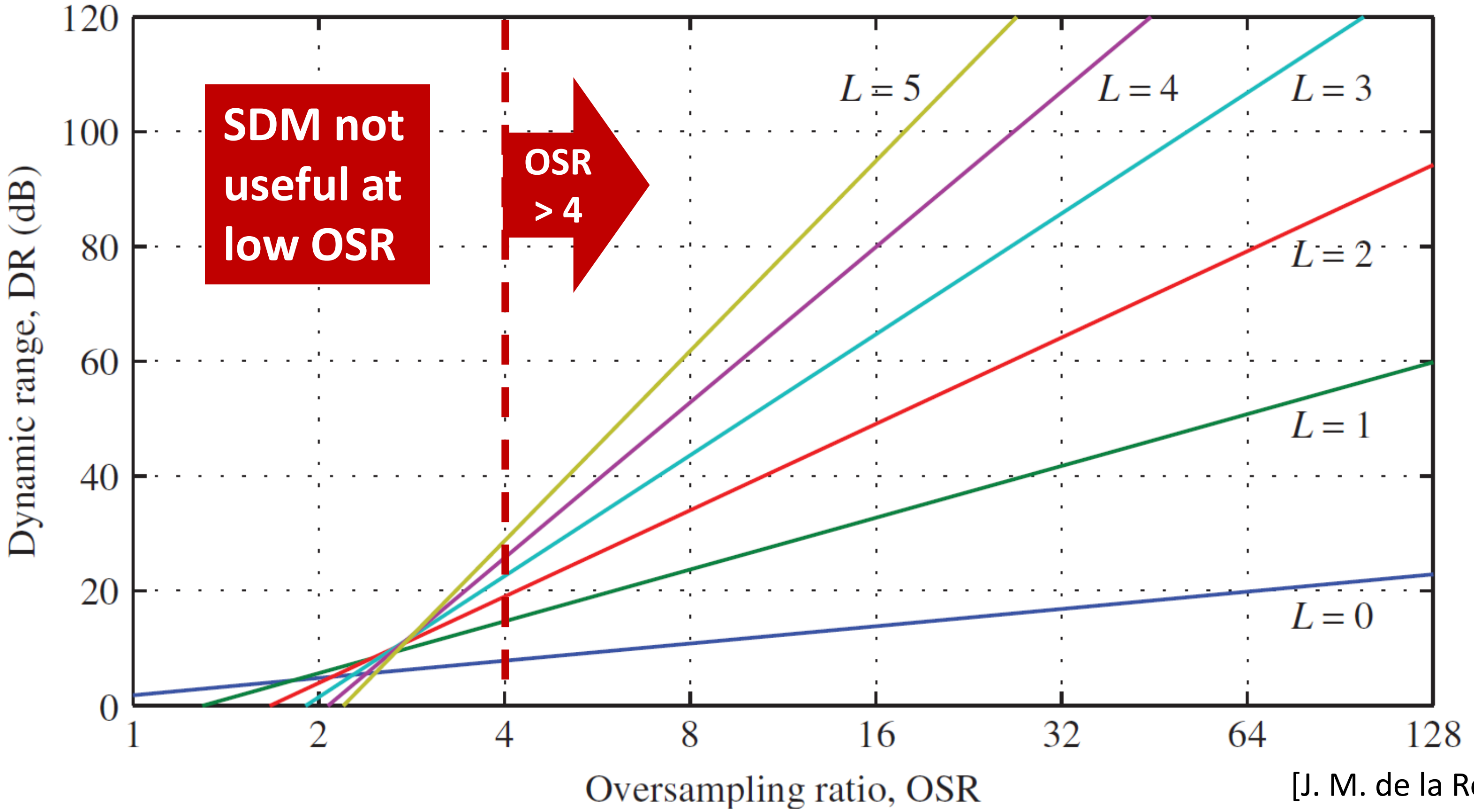
- ❑ SNQR increases with OSR by $3(2L+1)$ dB/octave
- ❑ ENOB increases with OSR by $(L+0.5)$ bit/octave
- ❑ Need OSR > 4 (more than two octaves) to reap **ΣΔM** benefits

Order (L)	Static SNR loss	SNR gain	Static ENOB loss	ENOB gain
0	0	3 dB/octave	0	0.5 bit/octave
1	-5.2 dB	9 dB/octave	-0.86 bit	1.5 bit/octave
2	-12.9 dB	15 dB/octave	-2.14 bit	2.5 bit/octave
3	-21.4 dB	21 dB/octave	-3.55 bit	3.5 bit/octave
4	-30.2 dB	27 dB/octave	-5.02 bit	4.5 bit/octave

Higher-Order ΣΔM

- Higher order gives more noise shaping
  - Ex: For OSR = 32, 4th order will give 3.5-bit more than 3rd order

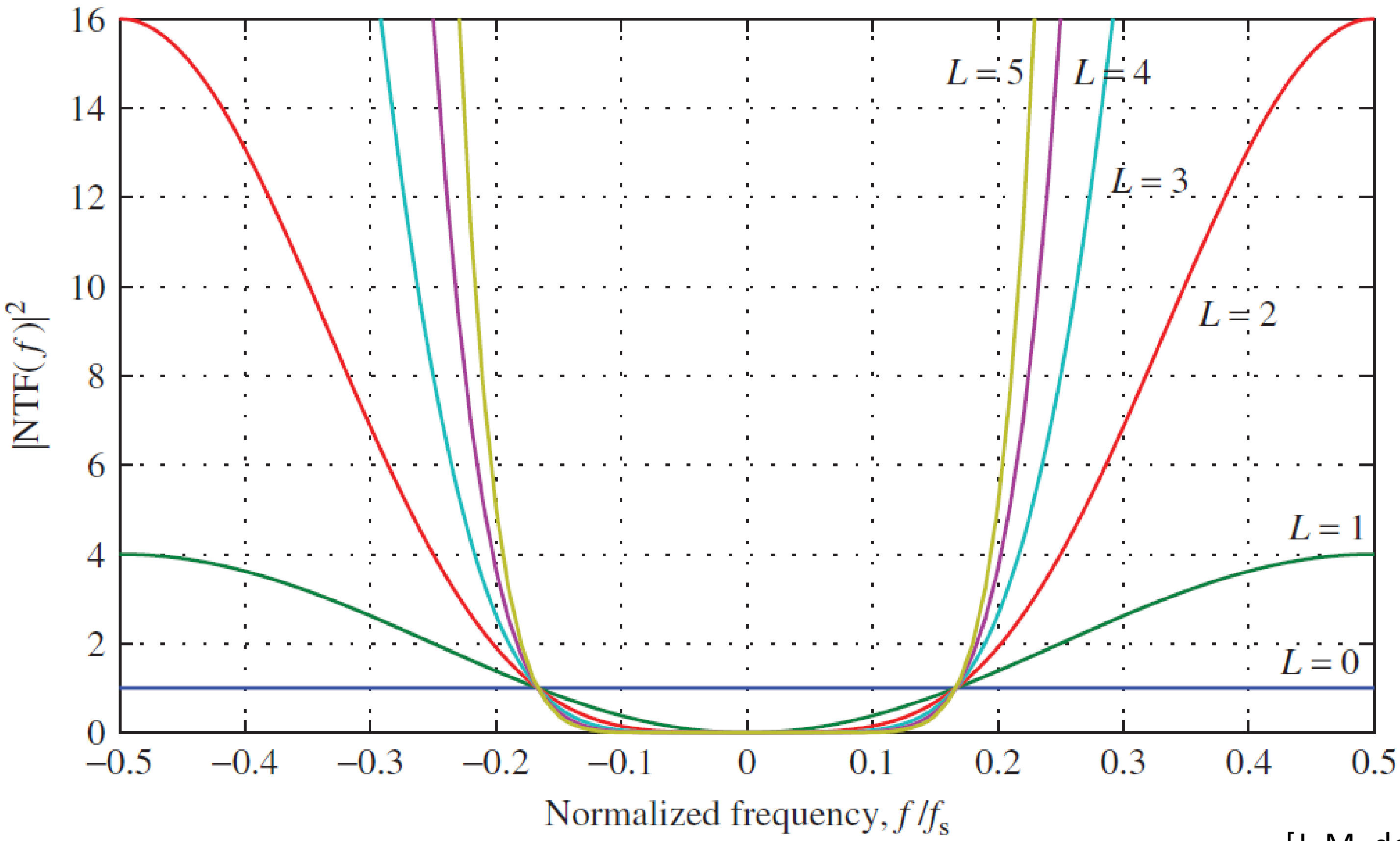
$$(5 \times 4.5 - 5.02) - (5 \times 3.5 - 3.55) \approx 3.5 - bit$$



[J. M. de la Rosa and R. del Rio, 2013]

Higher-Order ΣΔM

- Higher order gives more noise shaping
  - But L > 2 complicates loop stability
  - And more suppression of out-of-band noise is required

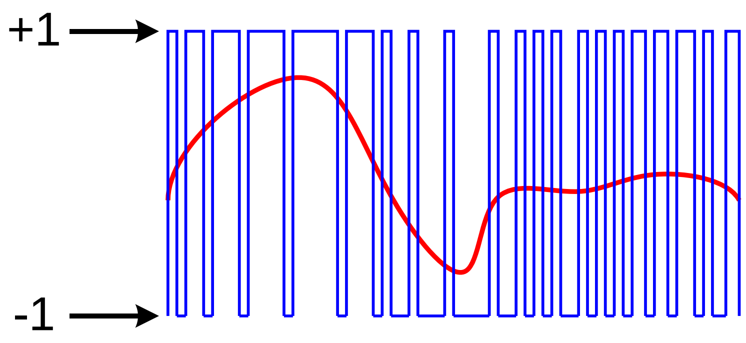


[J. M. de la Rosa and R. del Rio, 2013]

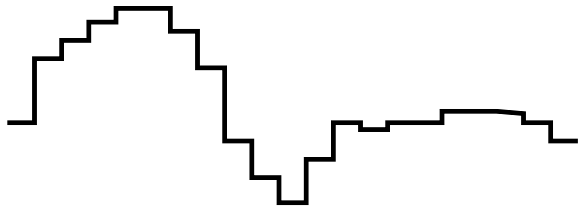
ΣΔ vs Nyquist ADC

- ΣΔ ADC behaves quite differently from Nyquist converters
- Digital codes only display an “average” impression of the input
- INL, DNL, monotonicity, missing code, etc. do not directly apply in ΣΔ converters
- Usually only dynamic ccs are important (SNR, SNDR, SFDR, etc.)

ΣΔ ADC output (1-bit)

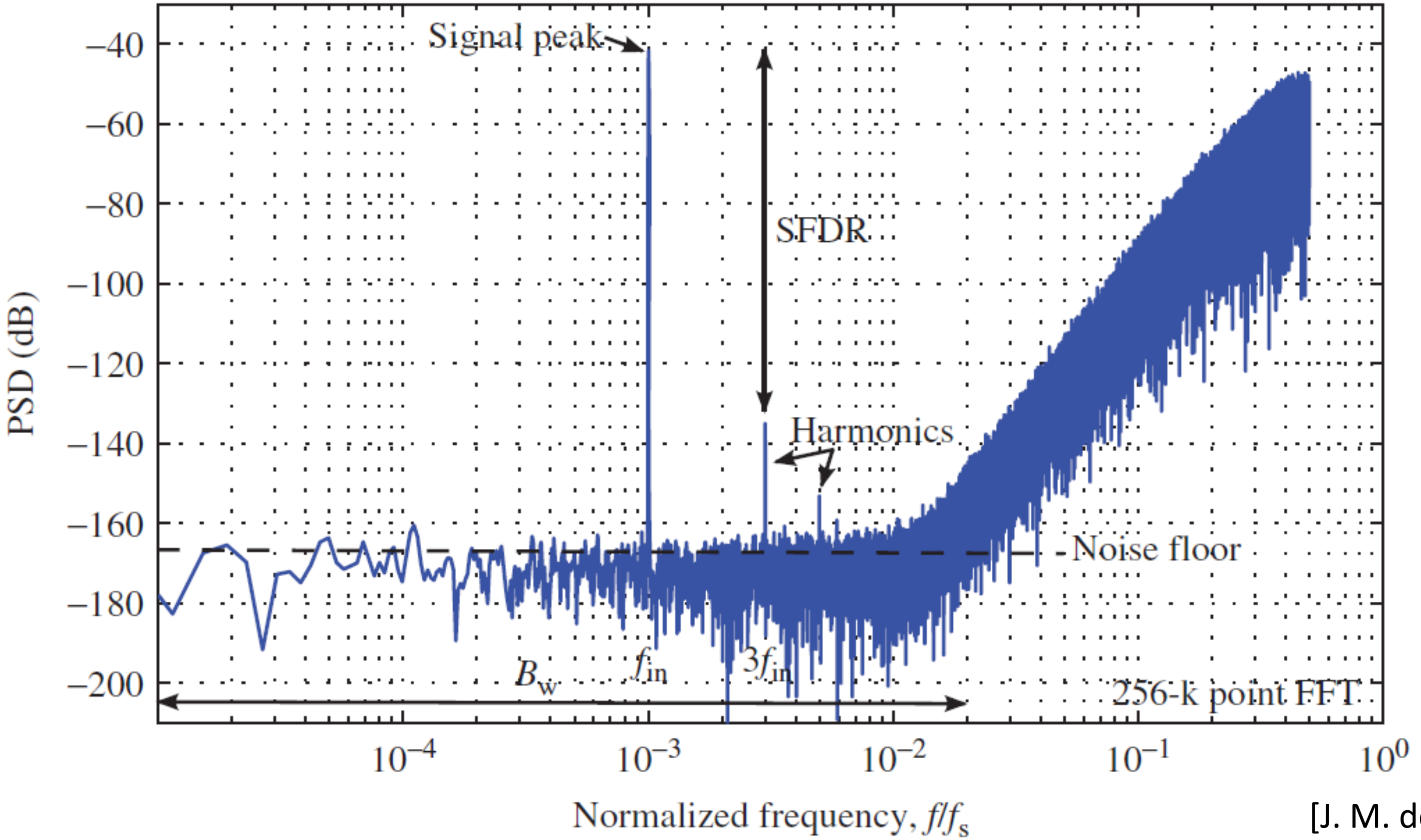


Nyquist ADC output



Sigma-Delta Modulator Specs

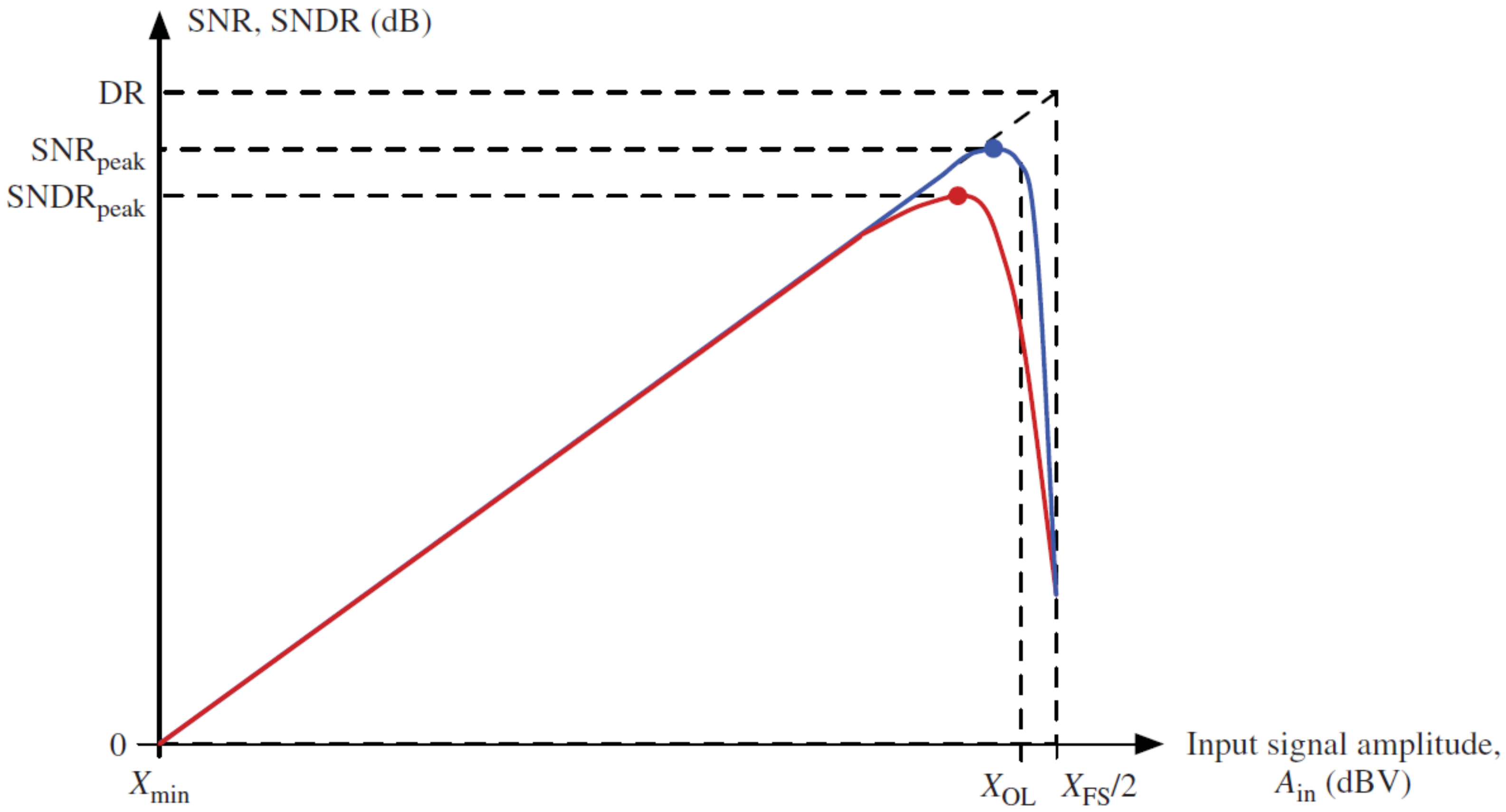
- ΣΔ ADC behaves quite differently from Nyquist converters
- Digital codes only display an "average" impression of the input
- INL, DNL, monotonicity, missing code, etc. do not directly apply in ΣΔ converters
- Usually only dynamic ccs are important (SNR, SNDR, SFDR, etc.)



[J. M. de la Rosa and R. del Rio, 2013]

Sigma-Delta Modulator Specs

- SNDR degrades faster due to distortion of large input signals
- SNR follows due to modulator overload
  - X_{OL}: Overload level
  - The amplitude at which SNR drops by 6dB
- Dynamic range is the span between full scale and noise floor



[J. M. de la Rosa and R. del Rio, 2013]

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- J. M. de la Rosa and R. del Rio, CMOS Sigma-Delta Converters: Practical Design Guide, Wiley, 2013.
- T. C. Carusone, D. Johns, and K. W. Martin, “Analog Integrated Circuit Design,” 2nd ed., Wiley, 2012.
- Y. Chiu, EECT 7327, UTD.

Thank you!