**AIN SHAMS UNIVERSITY**
**FACULTY OF ENGINEERING**
***Electronics & Comm. Eng. Dept.***

***Examination Date: 04-Nov-2017*** ***Allowed Time: 90 minutes***

# CHEP: ECE 486: Analog Integrated Systems Design
# Midterm Exam

**The exam consists of 3 questions in 3 pages** ***Total Marks: 25 Marks***

## Question (1) [8 points]

A novice ADC designer in your company is testing the performance of a 10-bit ADC using FFT spectral analysis test. The sampling frequency is $f_s = 4$ MHz, and he wants to apply a test tone $(f_{in})$ close to 250 kHz. From simulation results, he expects that the ADC will suffer from 3rd order distortion with $SFDR \approx 80\ dB$. He knows that to speed-up the FFT computation, the number of samples should be a power of two; thus, he performed the test with $N = 2^{10}$ samples. He also knows that to avoid spectral leakage, the number of test tone cycles should be an integer number; thus, he selected $N_{cyc} = \frac{N}{f_s/f_{in}} = 64$ cycles. He was surprised that the measurements showed $SFDR \approx 70\ dB$. Because you studied ECE 486, it is well-known in your company that you are an ADC expert; thus, he came to you asking for help.

a) [1 point] Explain to him why the measured SFDR is lower than his expectations.
b) [2 points] Suggest to him a single change in his test parameters (i.e., suggest a new value for either $N$ or $N_{cyc}$, but not both). What $f_{in}$ should he use if he is going to accept your suggestion? Note that $f_{in}$ should be close to 250 kHz.
c) [2 points] After he applied your suggestion, he found that the noise floor is too high to see the 3rd order harmonic he is trying to measure. He came to you again asking for help. Suggest to him a new combination of $N$ and $N_{cyc}$ so that the noise floor is at least 20 dB lower than the expected 3rd harmonic level. Note that $f_{in}$ should be close to 250 kHz. Recalculate $f_{in}$.
d) [3 points] Give him a sketch of the FFT output that he is going to get. Annotate the frequency/power of the fundamental, 3rd harmonic, and the noise floor level on the plot.
e) If he comes to you again, just send him this link ☺: https://www.maximintegrated.com/en/app-notes/index.mvp/id/1040

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## Question (2) [9 points]

A 3-bit ADC is tested using code density (histogram) test with a linear ramp as an input signal. The sampling frequency is 1 MHz. The table below shows the test results.

| Code | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| # of hits | 530 | 121 | 139 | 112 | 89 | 61 | 78 | 470 |

a) [2 points] Plot the DNL vs code (annotate the DNL values on the plot).
b) [2 points] Plot the INL vs code (annotate the INL values on the plot).
c) [2 points] If a ~400 kHz input test tone is applied to this ADC, and the output is plotted by FFT. What is the frequency at which the highest harmonic will appear? (Hint: You can determine the type of distortion from the INL plot.)
d) [1 point] Can we measure DNL/INL with 0.05 LSB resolution using the given test results? What is the best resolution DNL/INL that can be obtained from this test?
e) [1 point] Calculate the total time that was required by this code density test.
f) [1 point] Can you deduce if this ADC is monotonic or not? Why?

## Question (3) [8 points]

Figure 3.1 and Figure 3.2 shows two different implementation of a segmented current steering DAC. Assume unit current relative mismatch is 1%. Answer the following questions:

a) [1 point] Which DAC will have better DNL?
b) [2 points] Give an example of a logic transition that will give the worst case DNL for both DACs (Ex: the logic transition from the binary number $b_{N-1} \dots b_1 b_0$ to the binary number $a_{N-1} \dots a_1 a_0$, where $b$ and $a$ are '0' or '1').
c) [4 points] Calculate the worst case $\sigma_{DNL}$ and $\sigma_{INL}$ for both DACs in LSBs.
d) [1 point] What are the disadvantages of the architecture in Figure 3.2?

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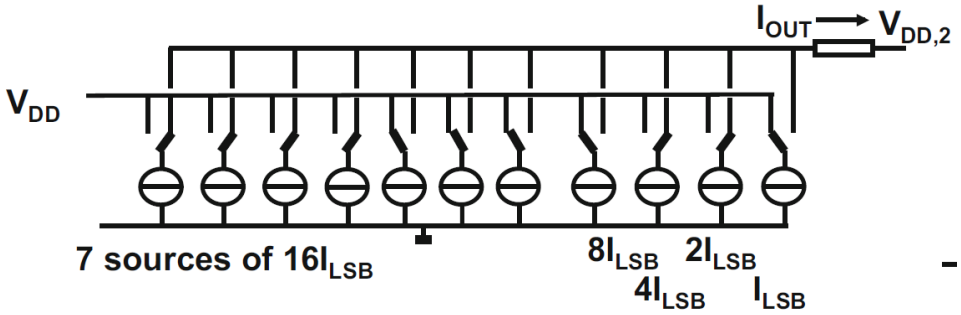


Figure 3.1

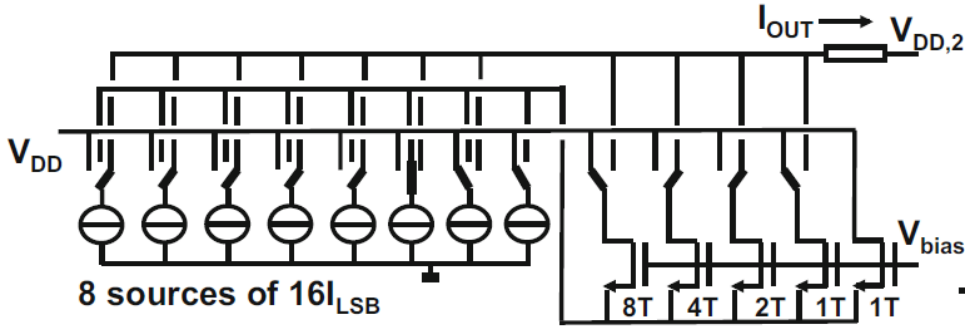


Figure 3.2

## Useful Formulas

$$SQNR = 1.76 + 6.02 \times N + 10\log\left(\frac{fs/2}{BW}\right)$$

$$FFT\ Noise\ Floor = 10\log S_{Q,FFT} = 10\log\frac{q^2}{12} - 10\log\frac{M}{2}$$

| | $\sigma_{INL}$ | $\sigma_{DNL}$ | No. of switches |
|---|---|---|---|
| Unary (thermometer) | $2^{\frac{N}{2}-1}\sigma_{\frac{du}{u}}$ | $\sigma_{\frac{du}{u}}$ | $2^N - 1$ |
| Segmented | | $2^{\frac{N_{binary}+1}{2}}\sigma_{\frac{du}{u}}$ | $2^{N_{unary}} - 1 + N_{binary}$ |
| Binary | | $2^{\frac{N}{2}}\sigma_{\frac{du}{u}}$ | $N$ |