Project 2: SPI Slave with Single Port RAM

Team name: No Moore Bugs

Team members:

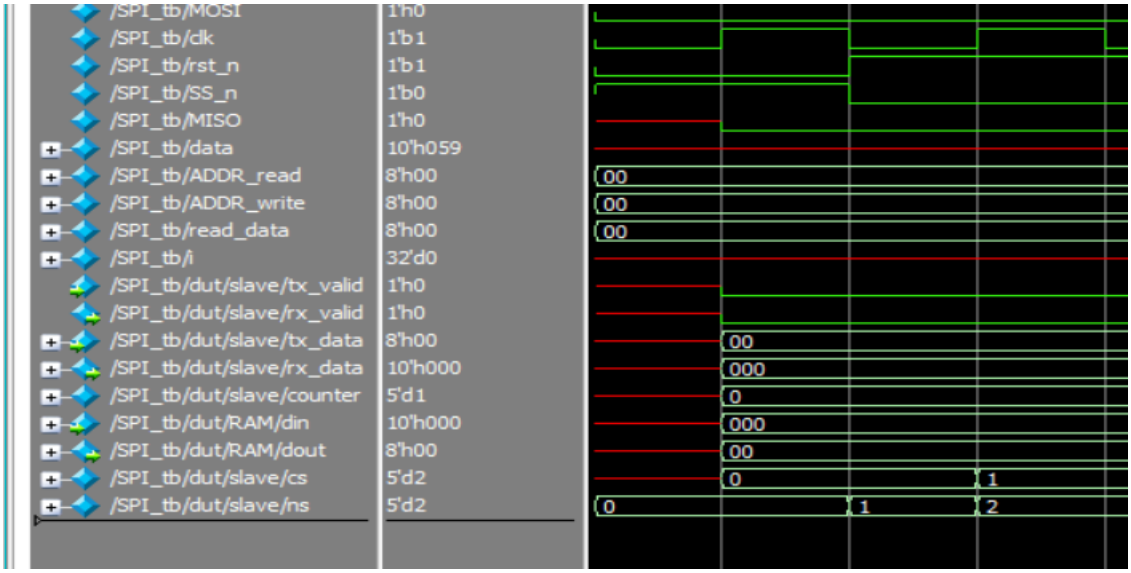
Yousef Wael Mahmoud Alkattan

Hayah Mahmoud

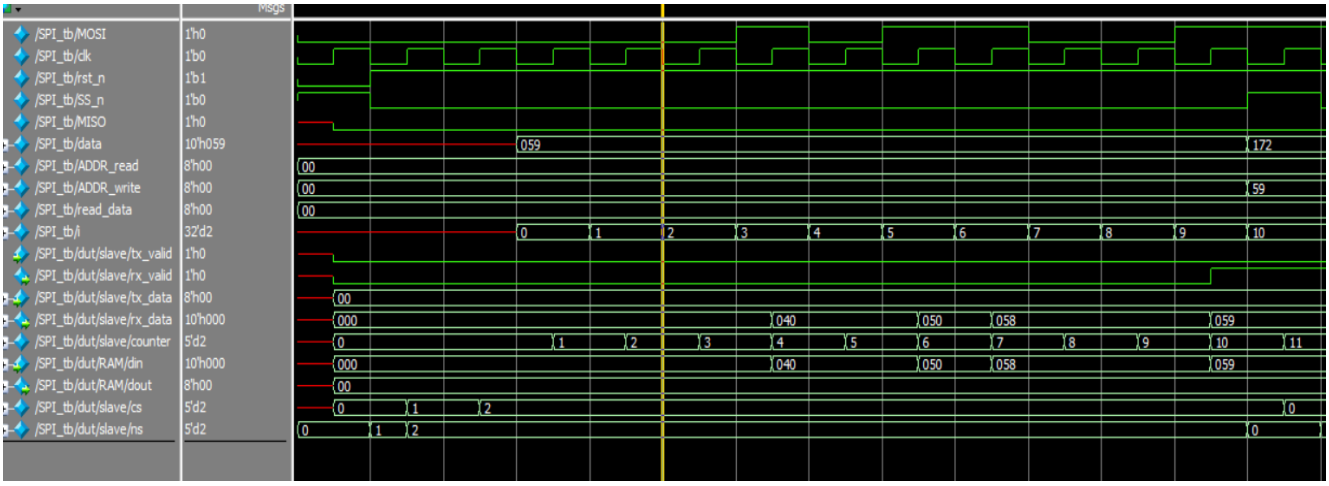
Robert moshref milad azmy

1. Questasim Waveform

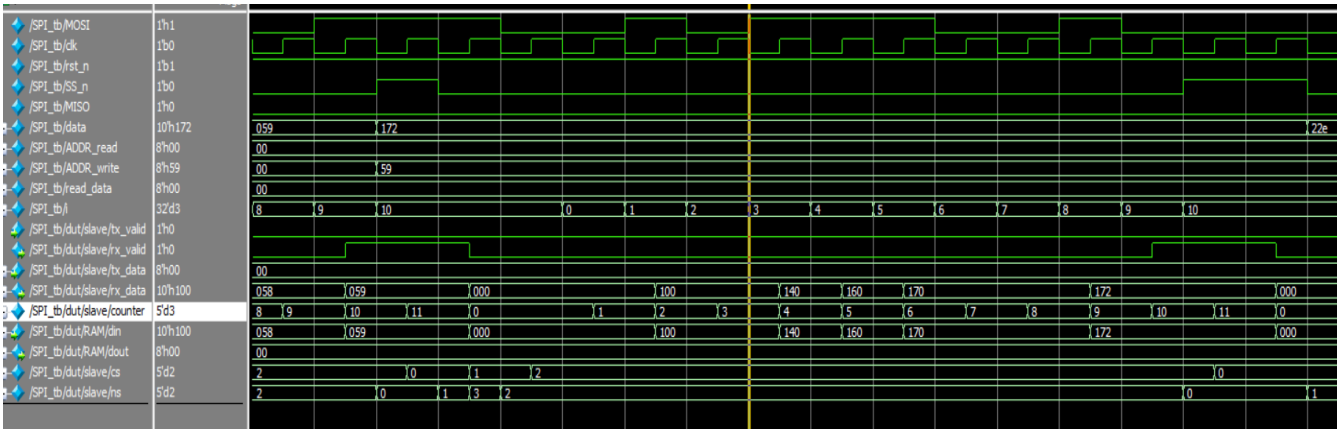
1. reset



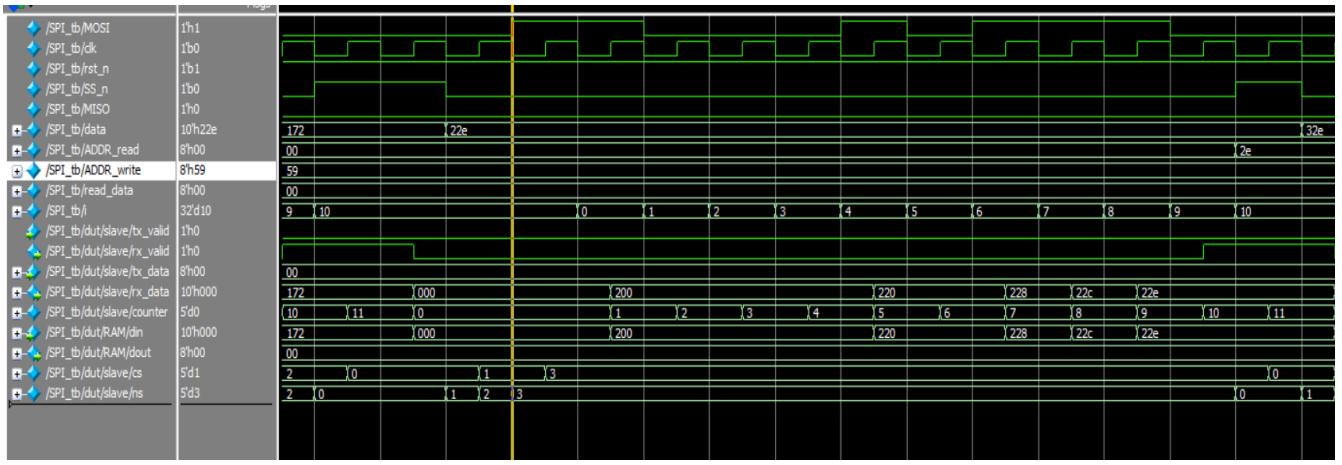
2. write address test



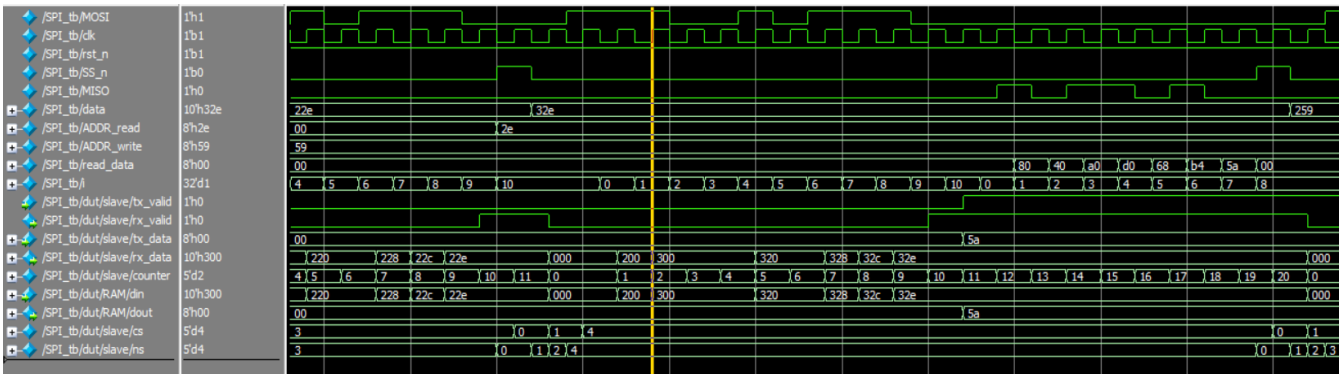
3. write data test



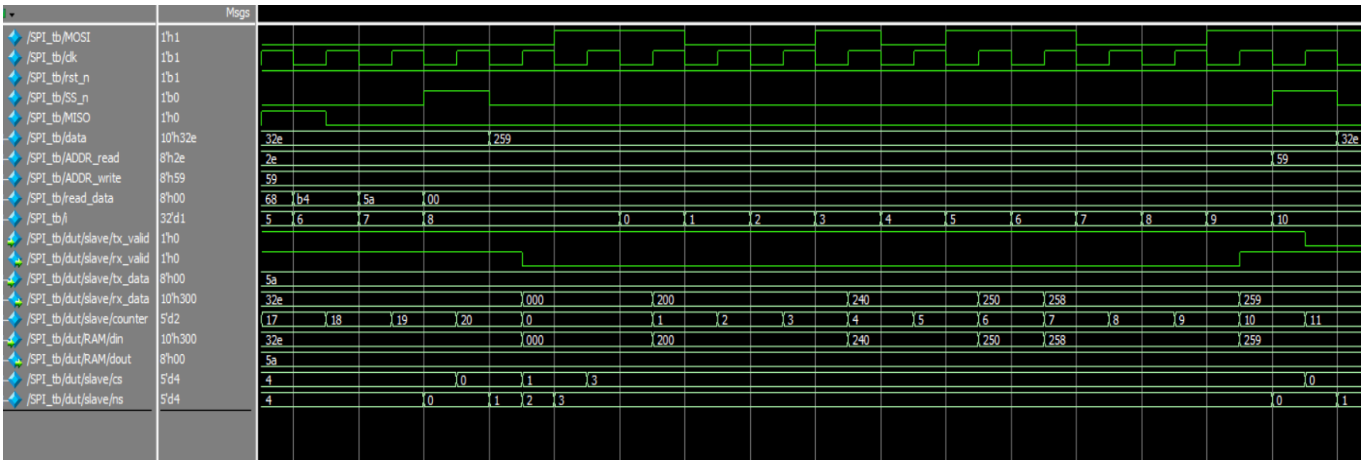
4. read address test.



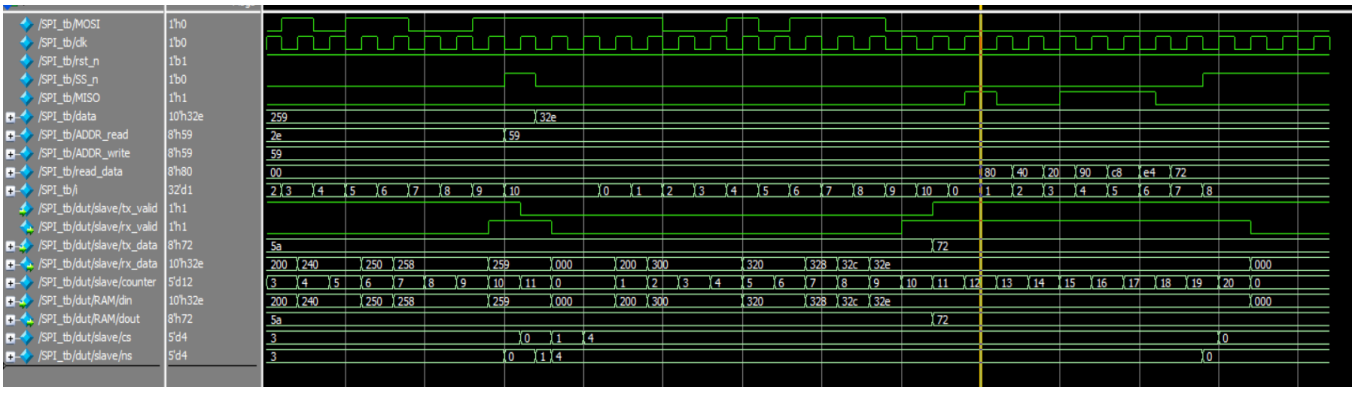
5. read data test



6. read address test 2 at the same location the write address command was executed



7. read data test 2 at the same location the write address command was executed



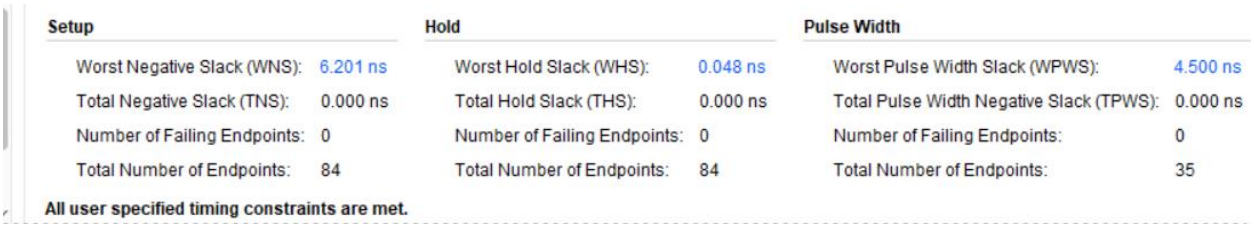
Transcript messages:

```
# WRITE ADDR: RAM[0x59] -> Expected Data: 0x58, Stored Data: 0x58
# WRITE DATA: RAM[0x59] -> Expected Data: 0x72, Stored Data: 0x72
# READ ADDR: Requested RAM[0x2e] -> Expected Data: 0x5A, Stored Data: 0x5a
# READ DATA: Data received from RAM[0x2e] -> Expected: 0x5A, Received: 0x5a
# READ ADDR: Requested RAM[0x59] -> Expected Data: 0x72, Stored Data: 0x72
# READ DATA: Data received from RAM[0x59] -> Expected: 0x72, Received: 0x72
```

2. Vivado simulation:

Implementation timing summary to select the best encoding:

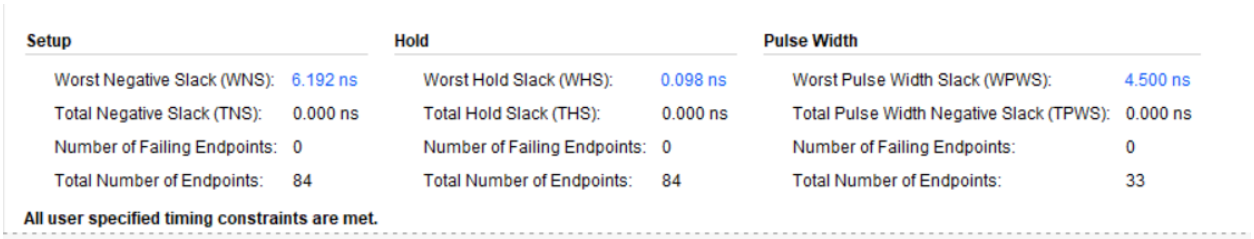
1. One-hot encoding



Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.201 ns	Worst Hold Slack (WHS):	0.048 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	84	Total Number of Endpoints:	84	Total Number of Endpoints:	35

All user specified timing constraints are met.

2. Sequential encoding



Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.192 ns	Worst Hold Slack (WHS):	0.098 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	84	Total Number of Endpoints:	84	Total Number of Endpoints:	33

All user specified timing constraints are met.

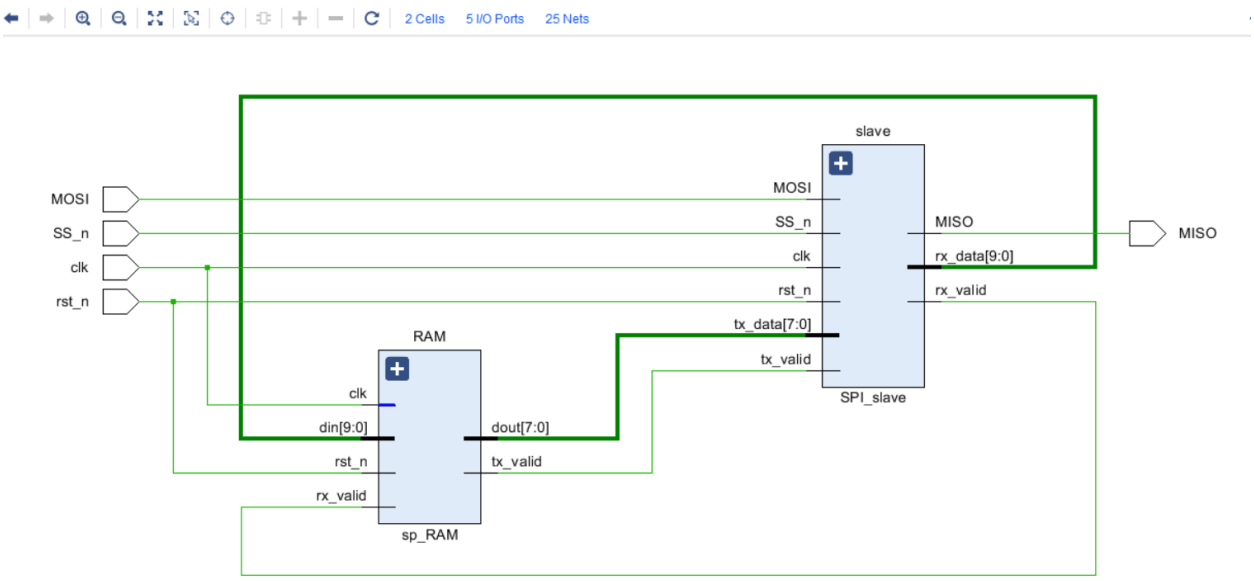
3. Gray encoding

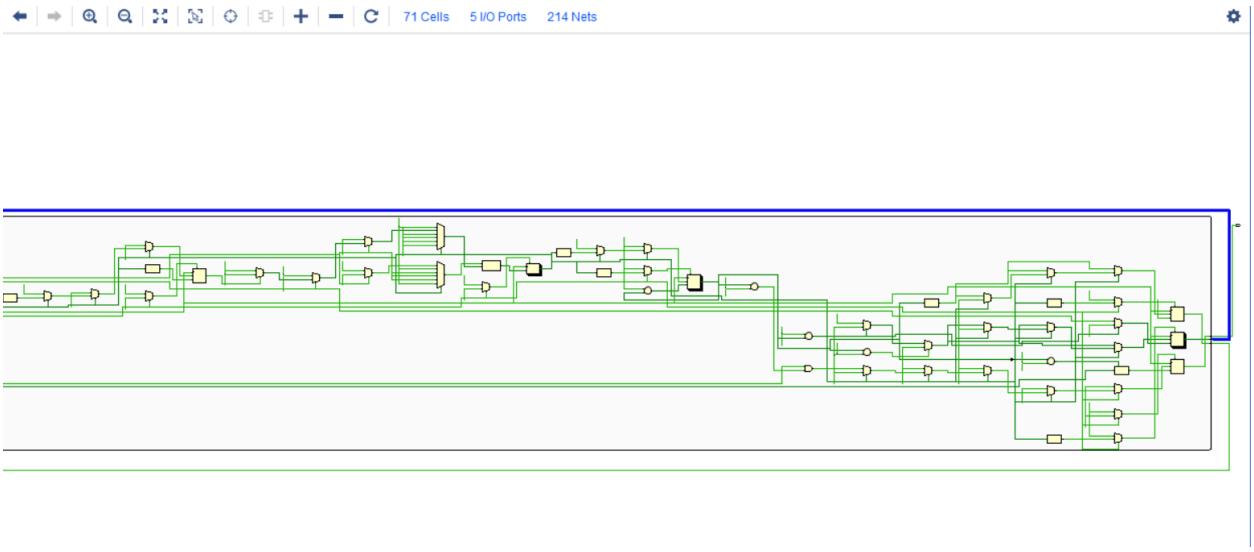
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.208 ns	Worst Hold Slack (WHS):	0.045 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	84	Total Number of Endpoints:	84	Total Number of Endpoints:	33

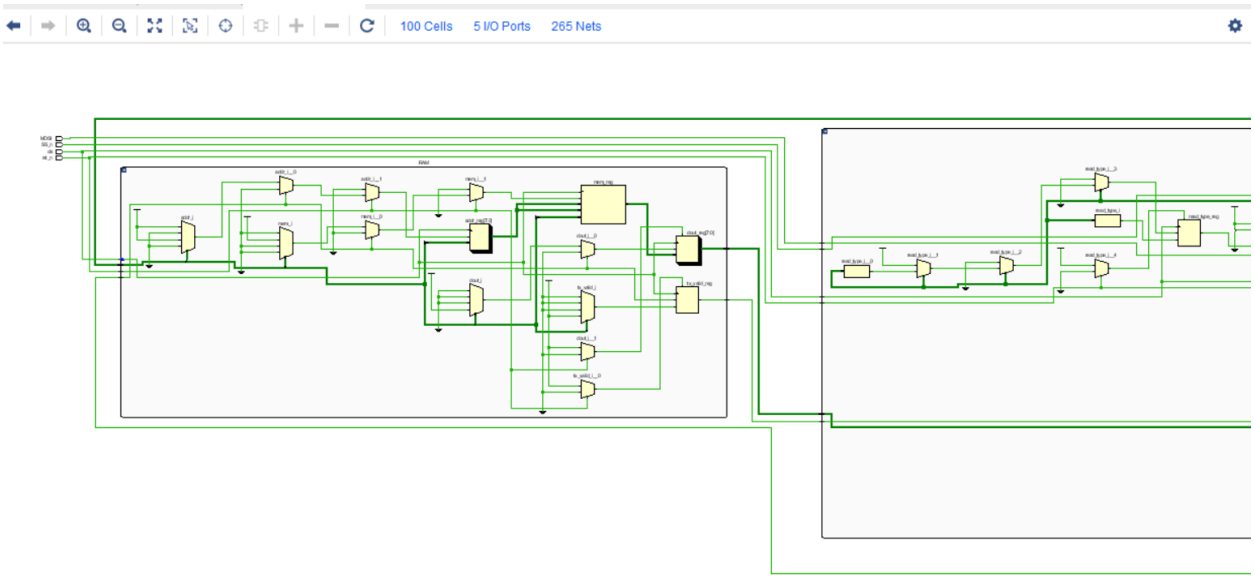
All user specified timing constraints are met.

Best encoding for the design is **gray encoding** which has the highest negative setup slack, which is important for operating at the highest frequency.

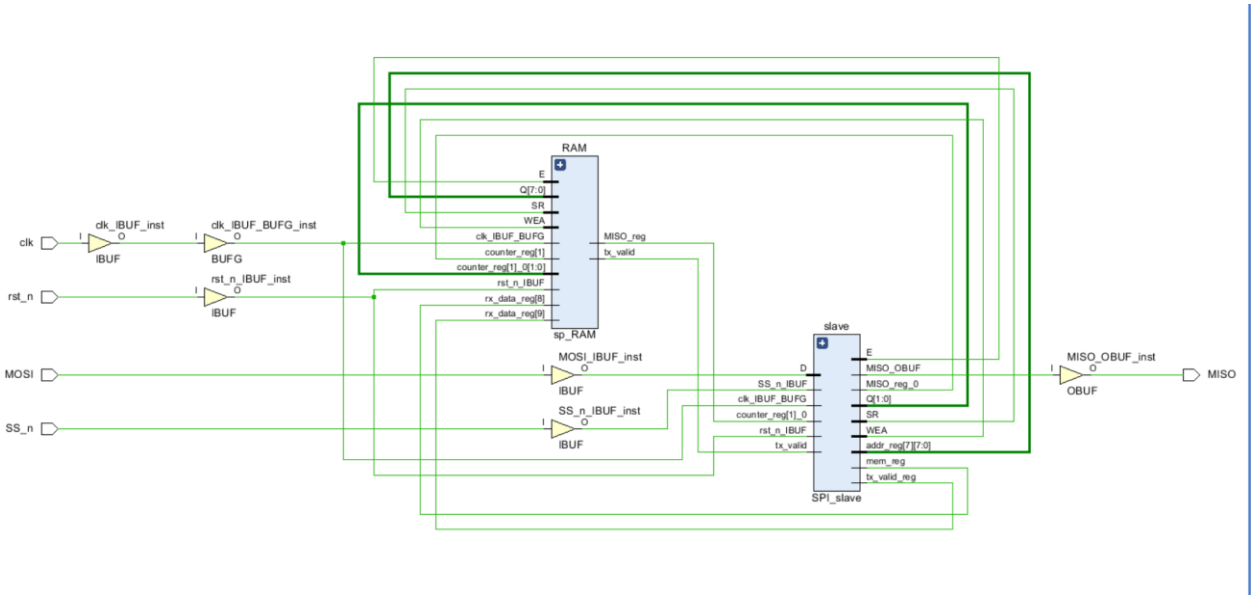
1. Elaboration schematic

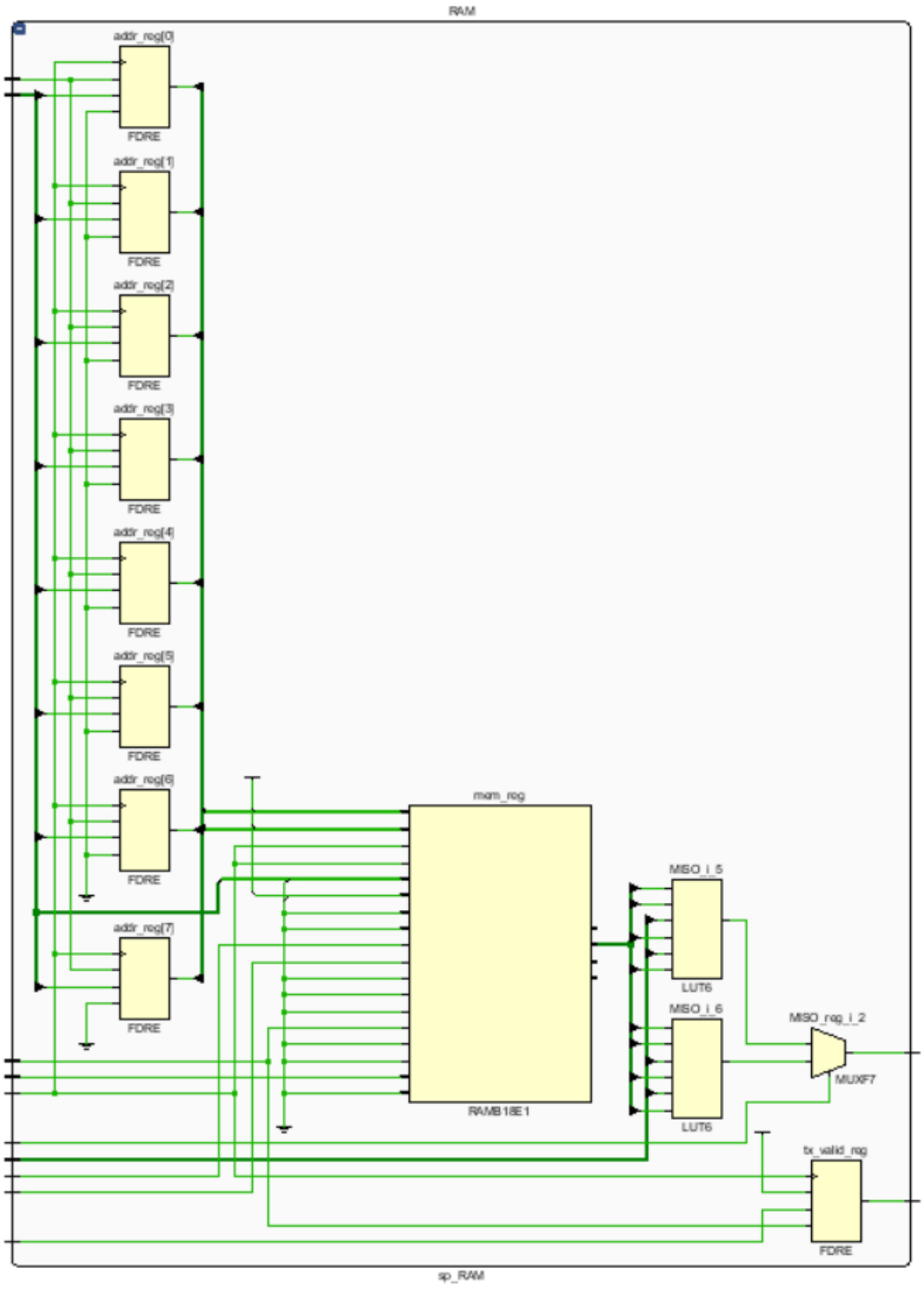




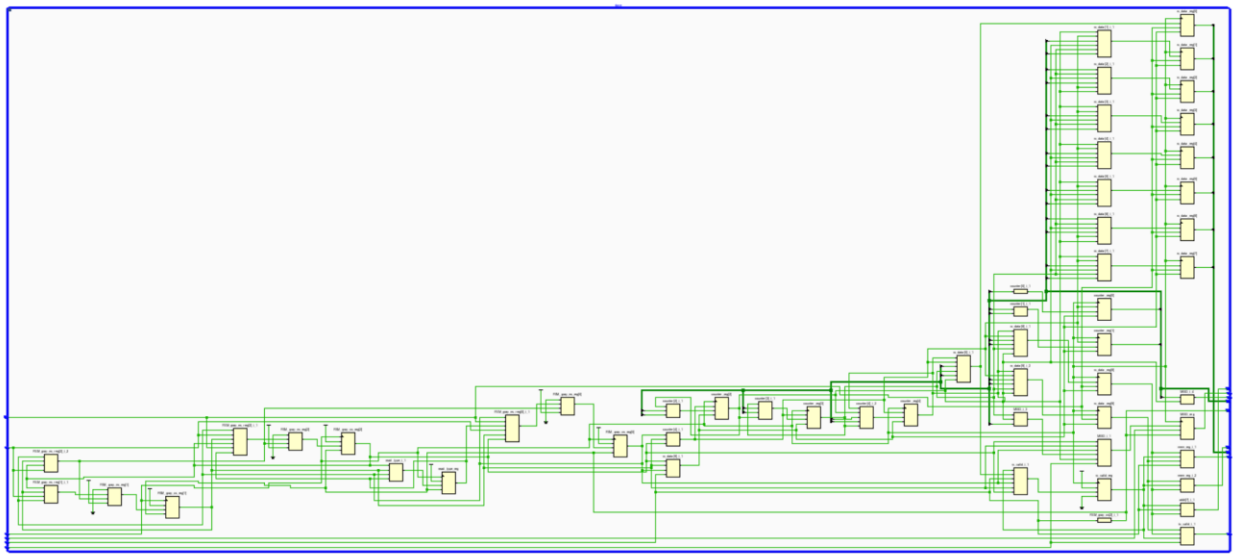

100 Cells
5 I/O Ports
265 Nets

2. Synthesis


RAM
E
Q[7:0]
SR
WEA
clk_IBUF_BUFG
counter_reg[1]
counter_reg[1]_0[1:0]
rst_n_IBUF
rx_data_reg[8]
rx_data_reg[9]
MISO_reg
tx_valid
sp_RAM
clk
clk_IBUF_inst
IBUF
clk_IBUF_BUFG_inst
BUFG
rst_n
rst_n_IBUF_inst
IBUF
MOSI
MOSI_IBUF_inst
IBUF
SS_n
SS_n_IBUF_inst
IBUF
slave
D
SS_n_IBUF
clk_IBUF_BUFG
counter_reg[1]_0
rst_n_IBUF
tx_valid
E
MISO_OBUF
MISO_reg_0
Q[1:0]
SR
WEA
addr_reg[7][7:0]
mem_reg
tx_valid_reg
SPI_slave
MISO_OBUF_inst
OBUF
MISO


RAM
addr_reg[0]
FDRE
addr_reg[1]
FDRE
addr_reg[2]
FDRE
addr_reg[3]
FDRE
addr_reg[4]
FDRE
addr_reg[5]
FDRE
addr_reg[6]
FDRE
addr_reg[7]
FDRE
mem_reg
RAMB18E1
MISO_i_5
LUT6
MISO_i_6
LUT6
MISO_reg_i_2
MUXF7
tx_valid_reg
FDRE
sp_RAM

Slave

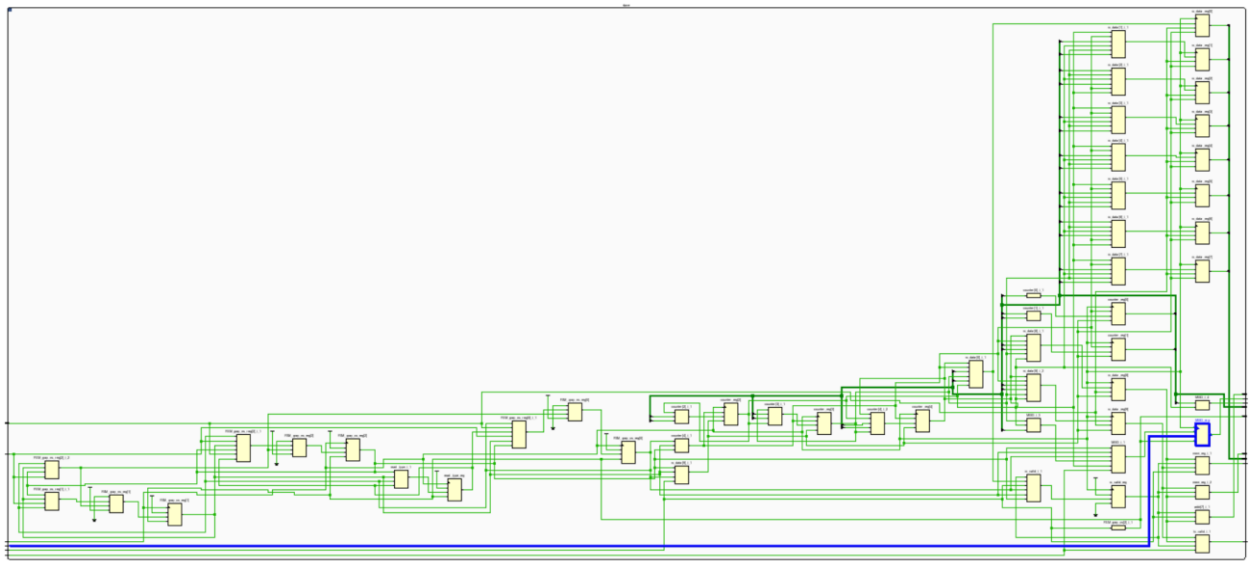


State	New Encoding	Previous Encoding
IDLE	000	00000
CHK_CMD	001	00001
WRITE	011	00011
READ_ADD	010	00111
READ_DATA	111	00110

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_slave'
WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [E:/project2/SPI_slave.v:35]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:57 ; elapsed = 00:01:13 . Memory (MB): peak = 759.2
---------------------------------------------------------------------------------
```

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI	29	33	1	0.5	5	1
RAM (sp_RAM)	2	9	1	0.5	0	0
slave (SPI_slave)	27	24	0	0	0	0

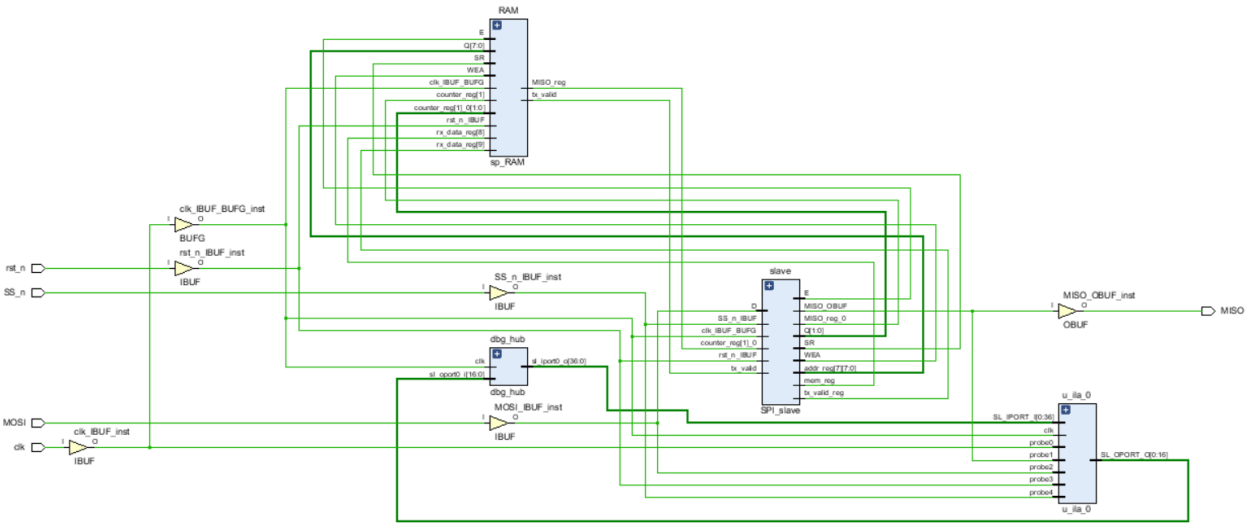
Critical path

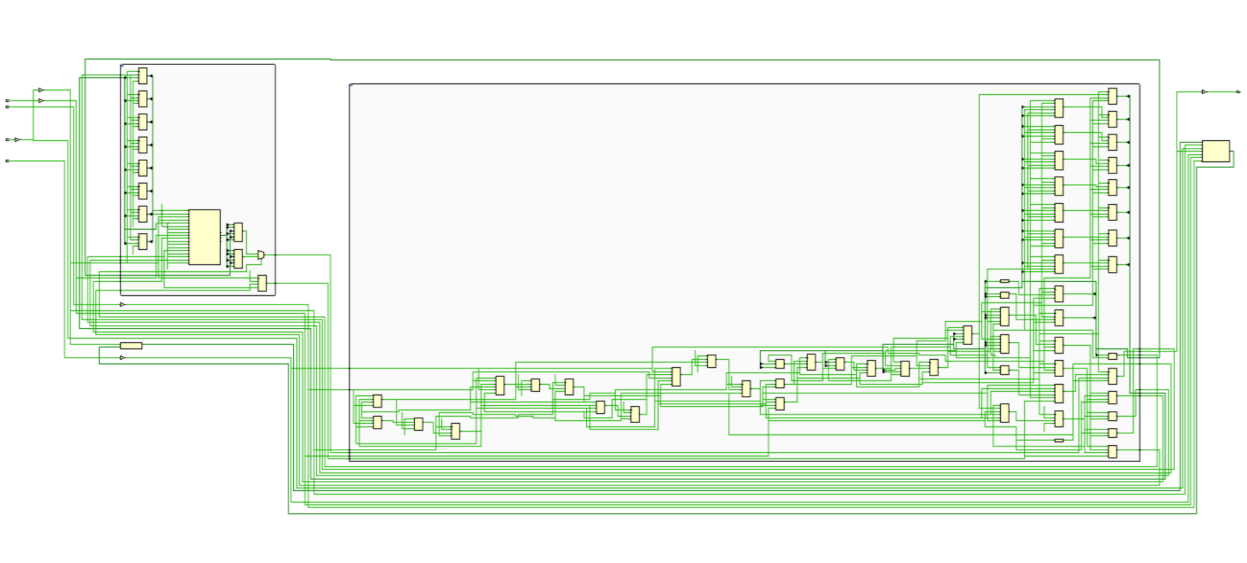


Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.261 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	83	Total Number of Endpoints:	83	Total Number of Endpoints:	33

All user specified timing constraints are met.

Synthesis after adding the debug core

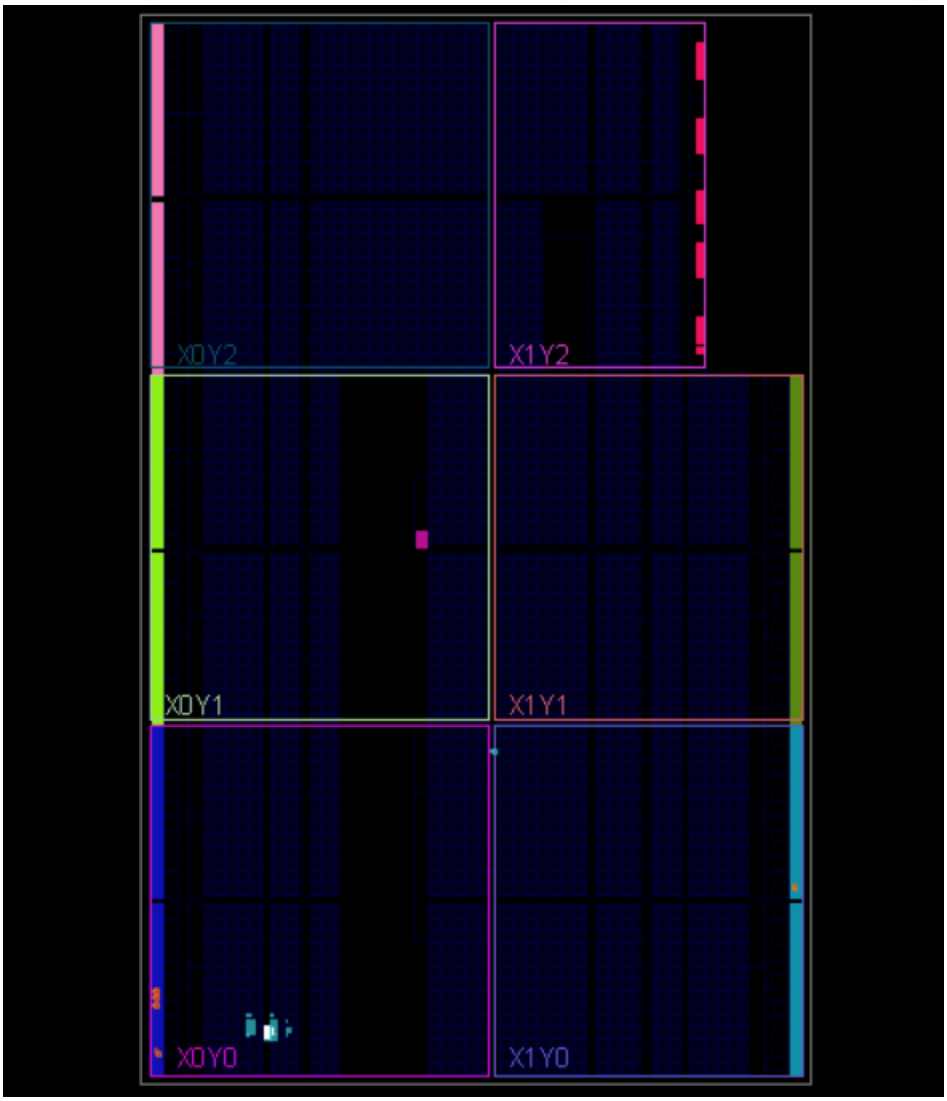


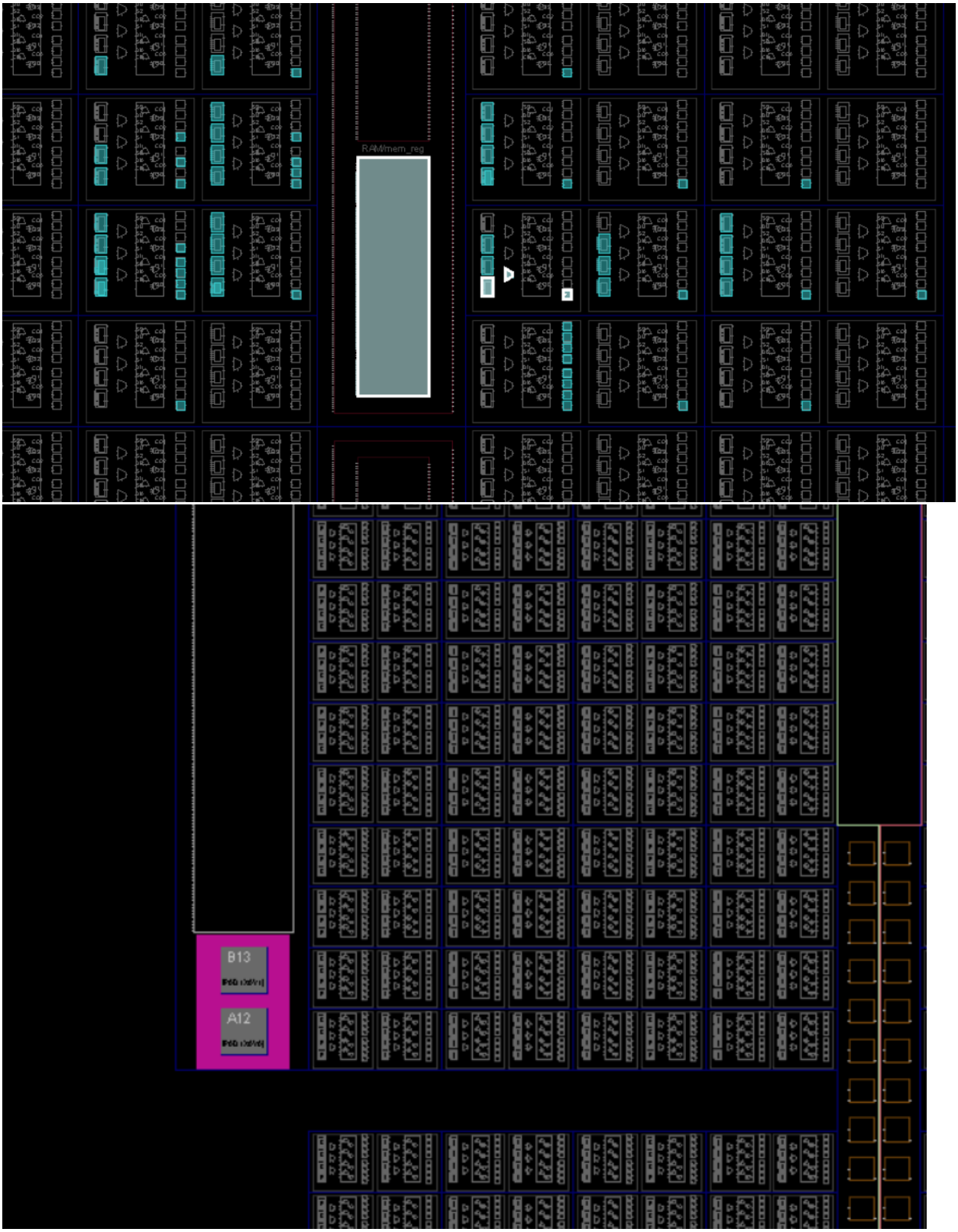


3. Implementation

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI	30	33	1	18	30	7	0.5	5	1
RAM (sp_RAM)	3	9	1	3	3	0	0.5	0	0
slave (SPI_slave)	27	24	0	17	27	5	0	0	0

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.208 ns	Worst Hold Slack (WHS):	0.045 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	84	Total Number of Endpoints:	84	Total Number of Endpoints:	33




RAM/mem_reg
B13
A12

Messages:


Warning (4)
Info (287)
Status (534)
Show All
Synthesis (2 warnings)
[Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [SPI_slave.v:35]
[Constraints 18-5210] No constraint will be written out.
Implementation (1 warning)
Write Bitstream (1 warning)
DRC (1 warning)
Physical Configuration (1 warning)
Chip Level (1 warning)
[DRC PDRC-153] Gated clock check: Net slave/FSM_gray_ns_reg[2]_i_2_n_0 is a gated clock net sourced by a combinational pin slave/FSM_gray_ns_reg[2]_i_2/O, cell slave/FSM_gray_ns_reg[2]_i_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.