Lab 3: The 741 Operational Amplifier

Electronics II

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Schedule for this Lab

Day 1: Students will present their prelabs to a TA. A completed prelab is required in order to do the simulation section. Students should be starting their simulations on this day.

Day 2: Finish your simulations and have your results checked by a TA.

Purpose

The purpose of this laboratory is to become familiar with a two-stage operational amplifier (op-amp). Students will analyze the circuit using Multisim. The op-amp in this lab is based on the 741 that you will study in class. Since the 741 is complicated, the op-amp in this lab has been simplified down to a more manageable size. Most notably the some bias circuitry has been made ideal and the output short circuit protection has been removed. This means that most, but not all of your simulation results will reasonably represent real-life behavior.

The 741 op-amp was once the work horse of circuit engineers due to its good performance (at audio frequencies) and low cost. As inevitably happens with all technology, newer chips improve on those from the past, and as a result, there are many op-amps available today that are faster, cheaper, smaller, less noisy, and more efficient, not to mention the fact that digital signal processing is gradually taking on the roles that traditional op-amp filters used to take. Still, the 741 is relatively easy to analyze, and shows all of the important aspects of an op-amp. Its limitations are actually useful for us since we can measure them easily using relatively cheap lab equipment and simple simulation.

Introduction

Before proceeding with the laboratory, students are advised to read Sedra and Smith 7th Edition (S&S), "Micro-Electronic Circuits", the section in Chapter 13 on the 741 op-amp.

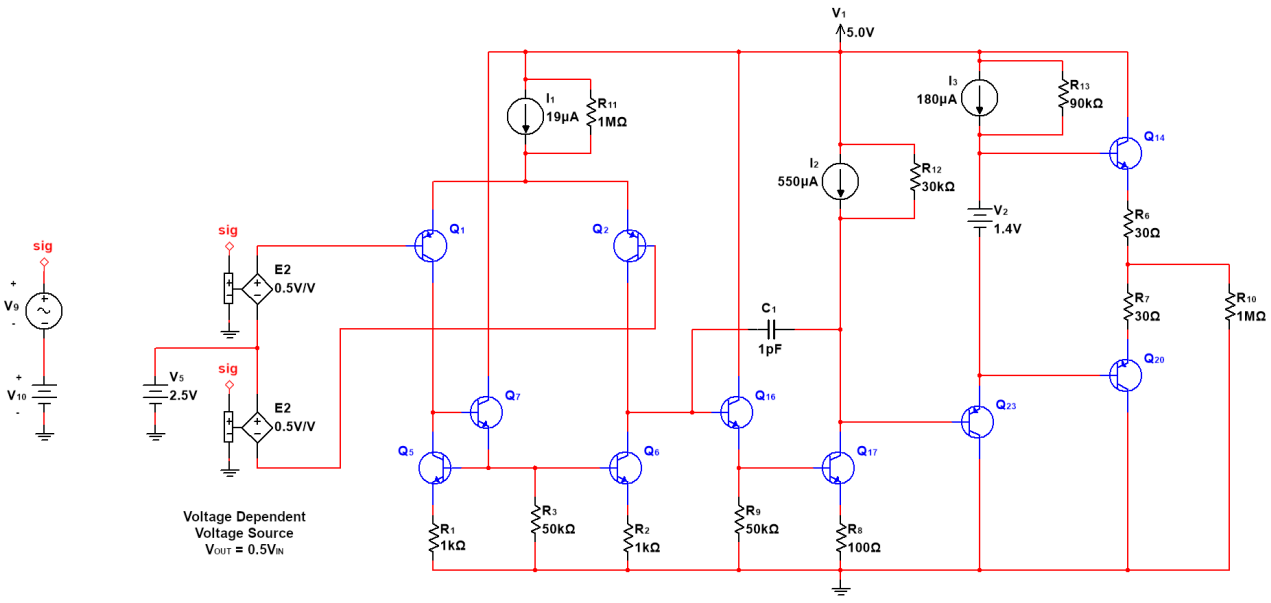

Figure 1: A Scaled-Down 741 Op-Amp Used For Analysis In This Lab

Figure 1 shows the op-amp circuit that you will be simulating using Multisim. The base of Q_2 is the non-inverting input and the base of Q_1 is the inverting input of the op amp. V_{10} is the input DC voltage, which can be used to represent input offset voltage, or be used for input DC voltage sweeps. V_9 is the input sinusoidal voltage, which can be used for AC analysis. The boxes labeled E1 and E2 are voltage-controlled voltage sources each with a gain of 1/2. This allows the input voltage (the sum of V_9 and V_{10}) to be applied deferentially to the two inputs, while adding the common-mode voltage V_5 to each input.

Pre-lab

The prelab calculations are extensive and make up the bulk of the work for this lab. These calculations must be ready at the start of the lab in order to obtain your prelab mark.

You may use the appendix or textbook for assistance in these calculations, although you must perform these derivations yourself in the report, so you must still have this prelab done before the lab.

The table below lists some assumptions for NPN and PNP parameters that will help you with your prelab calculations.

Parameter	**NPN**	**PNP**
Early Voltage (V_A)	80 V	20 V
β (Assume constant, although it normally depends on current)	100	100
I_S (recall that $I_C = I_S e^{V_{BE}/V_T}$)	6.73 fA	1.41 fA
V_{BE}	0.6 V	0.6 V
V_{CC}	5 V	5 V

The BJT used are NPN Transistors (2N3904) and PNP Transistors (2N3906) for the simulations, these transistors are used to approximate the functional 741.

Calculate the parameters listed below. When appropriate, show the small signal equivalent circuit you are using. Your work should be complete without referencing the textbook or notes for figures or equations. **All of this work needs to be integrated in your report.**

While you are progressing through these calculations try to understand the purpose of each transistor.

- Find I_C, r_o and g_m, for every transistor. Note that the transistor output resistance r_o is approximately given by V_A/I_C. You may assume that $\beta = 100$ for all transistors, (although in reality, β is not constant but depends on the current). Put the results in a table and show all calculations.
- Find the gain of the first stage A_1. This stage is defined to end as the input to the base of Q_{16}, including the impedance seen looking into the base of Q_{16} as a load to the first stage.
- Find the gain of the second stage A_2. This stage is defined as the gain from the base of Q_{16} to the base of Q_{23}.
- Thus, determine the DC open-loop voltage gain (DC differential gain). Note that all the output circuitry is made up of CC amplifiers that have a voltage gain close to unity. You can verify this by calculating the gain yourself if you like.
- Determine the input common-mode range. Note that the circuit has a 5 V supply.
- Determine the output voltage swing, which is the voltage range available from all the transistors when they are allowed to operate
- The value for the capacitor C_1, so that the unity-gain frequency $f_u = 1$ MHz, this is the frequency at which the differential gain is 0 dB. Note that this will NOT be 30 pF as specified in S&S.
- The slew rate of the op-amp. Note that this will be limited by how fast the input stage can charge or discharge the capacitor C_1, ie. $V/\mu s$, or how much current per farad of the capacitor.

Report

1. Explain the difference in role of V_{10} and V_5. Why are both needed?
2. What is the purpose of Q_7 and R_3 in this circuit? What difference would there be if instead of both, the collector and base of Q_5 were shorted as in the current mirror in Lab 1? You may want to consider the impact of Q_{16}.
3. What is the role of C_1 and what would happen if it were absent?
4. The circuit uses ideal current sources. How would these be implemented in a real circuit? What differences in performance might be seen as a result? The answer is not finite output impedance since the output impedances are already modeled by R_{11}, R_{12} and R_{13}.

5. What is the purpose of V_2? How would V_2 be implemented in a real circuit?
6. Why are 3 stages used in this op-amp design? Why bother with the third stage if it provides such a low gain?
7. What is the DC power consumption of the entire circuit (assume no input signal).

Simulation

The op amp files can be found on Nagui's website. Open the two .ms14 files on the jpKnight server, as they are needed for the Differential Sweep, Slew Rate, and Frequency Response. The URL for the website is below:

`http://www.doe.carleton.ca/~nagui/Elec3509/Lab3/`

Load up the schematics provided by Nagui's website on Multisim. **Set the capacitor C_1 to the value calculated in the pre-lab**. Figure 1 also shows the input source arrangements that should be used for differential and common mode signals.

Differential Sweep

The file for the differential sweep is the ELEC3509_Lab3_Diff_OP_AMP.mp14. Use this when performing the simulation for the best results.

Perform the following tasks and answer all questions:

1. Perform Parameter Sweep with a nested DC Operating Point simulation of the input differential voltage V_d between -10 mV to 10mV, while the common mode voltage V_{cm} is set to 2.5 V. Plot the transfer curve for V_o versus V_d.
   (a) Add a probe from **Place** → **Probe** → **Voltage**, and add the voltage probe to the end of R_{10}, or the output node.
   (b) Go to **Simulate** → **Analyses and Simulation**, and choose a Parameter Sweep.
   (c) In the Analyses and Simulation window, choose to sweep a voltage source (Vsource) device, and you will be sweeping the DC offset source V_{10}. Choose to sweep the dc parameter.
   (d) In the same window, choose to perform a linear Sweep from the Start voltage -1 mV to 1 mV, with more than 100 points.
   (e) We are performing a DC Operation Point simulation with each parameter step, so the Analysis to sweep across is the DC Operating Point, which will be displayed on the graph when simulated.
   (f) Measure the output voltage across the R_{10} using the voltage probe that was added earlier by going to the Output tab in the Analyses and Simulation window, and add the output voltage probe to the list for Analyses.
   (g) Save and run the simulation.

   From the plot, what is the range of the linear region (the range for which the output is a linear multiple of the input)? What is the output voltage swing? Estimate the differential gain. What is the input offset voltage (i.e., the value of V_d required for the output to be 2.5 V)? Compare the values obtained by Multisim to the ones calculated. If the values differ, explain why.

   In your report, compare these values with the values you calculated in your pre-lab. Refer to each number separately and do not be vague. Explain any differences.

2. When you completed the calculations in the pre-lab you used approximate values for the transistor parameters (I_C, β, g_m, r_o, etc). You can get the actual values for all these parameters from a DC Operating point simulation. Make sure to update the DC biasing point for the input DC supply based on Part 1.
   (a) Clear the XSpice code before running the DC Operation parameter simulation. Go to **Simulate** → **XSPICE command line interface...**, and clear the command line information from the XSPICE Command Line window by pressing the New button.
   (b) Go to the simulation settings, and run a DC Operation Point simulation for the DC operation parameters of the transistors.

(c) Run the simulation, and note that the XSPICE Command Line window is updated with lines of information. Look for the *show all* branch, and find the information on the 2N3906 and 2N3904 BJT. Copy down the values listed for the BJT, and list them in a table. Calculate the DC and AC β from the currents, you may have to run an interactive simulation with a small signal voltage V_9, and measure the peak to peak currents through.

Note down the values I_C, I_B, V_{BE}, V_{CE}, V_{BC}, β_{DC}, g_m, r_π, r_x, r_o, C_{BE}, C_{BC}, C_{JS}, β_{AC}, C_{BX}. Include these values with your lab report in the appendix.

In your report, insert a table showing side-by-side comparisons of your calculated values against the simulated values. Explain any discrepancies and explain whether or not they are significant. Redo your calculations using these numbers and recalculate the differential gain. Compare it with the one calculated previously.

If the values differ, explain why. Show a table in your report listing side-by-side comparisons of the original gains and the recalculated gains. Which calculations have the smaller error? Why? What can you conclude about the accuracy of the equation you used to calculate the gain?

3. Perform a Parameter Sweep with a nested DC Operating Point simulation for the common-mode voltage V_5 from 0 V to 5 V, while the differential voltage V_{10} is set to the input offset voltage from part 1.

   (a) Set a Parameter Sweep from Analyses and Simulation of the Device Vsource for V_5. The DC parameter is that which is being changed, to create a linear sweep from 0 to 5 volts.

   (b) Save and run.

   Plot V_o versus V_5 transfer curve. What is the common-mode range? If the value differs, explain why.

Slew Rate

* **Note** that R_{14} is not completely necessary, except that in circuits made of FETs, this resistor can become useful.

You must open the Multisim file from Nagui's website, the name of which is ELEC3509_Lab3_Slew_Rate.ms14. Make sure the circuit is configured like that from Figure 2.

The slew-rate is the maximum rate-of-change of the output voltage. It is usually measured with the op amp in the unity-gain voltage-follower configuration. The circuit configuration is shown is Figure 2. The input voltage of Figure 2 is a square wave generator (Clock Voltage), stepping between 1 V and 4 V (3 V step in series with a 1 V DC source).

1. Change the capacitor so that the unity gain frequency is 1 MHz.
2. In the Multisim file, you must set the input pulse voltage source settings up properly. The Initial value is 1 V, and the Pulsed value is 4 V. Set the Rise and Fall time to 0.1 μs, and the period to 50 μs, with a Pulse width of 25 μs.
3. Attach a voltage probe to both the input V_{11}, and output V_O.
4. Run a Transient simulation from Analyses and Simulation from 0 to 500 μs, which will show 10 periods of the input and output waves.
5. You should zoom into the input and output waves, and use the cursors to measure the falling and rising rate for the output square wave to find the slew rate of the circuit.

The square wave has a period of 50 μs with a 0.1 μs rise and fall time. Plot the input and output transient voltage waveforms in the report. From the Multisim plots, what is the positive and negative slew rate expressed in V/μs? Compare the simulation values with the slew rate calculated in your pre-lab.

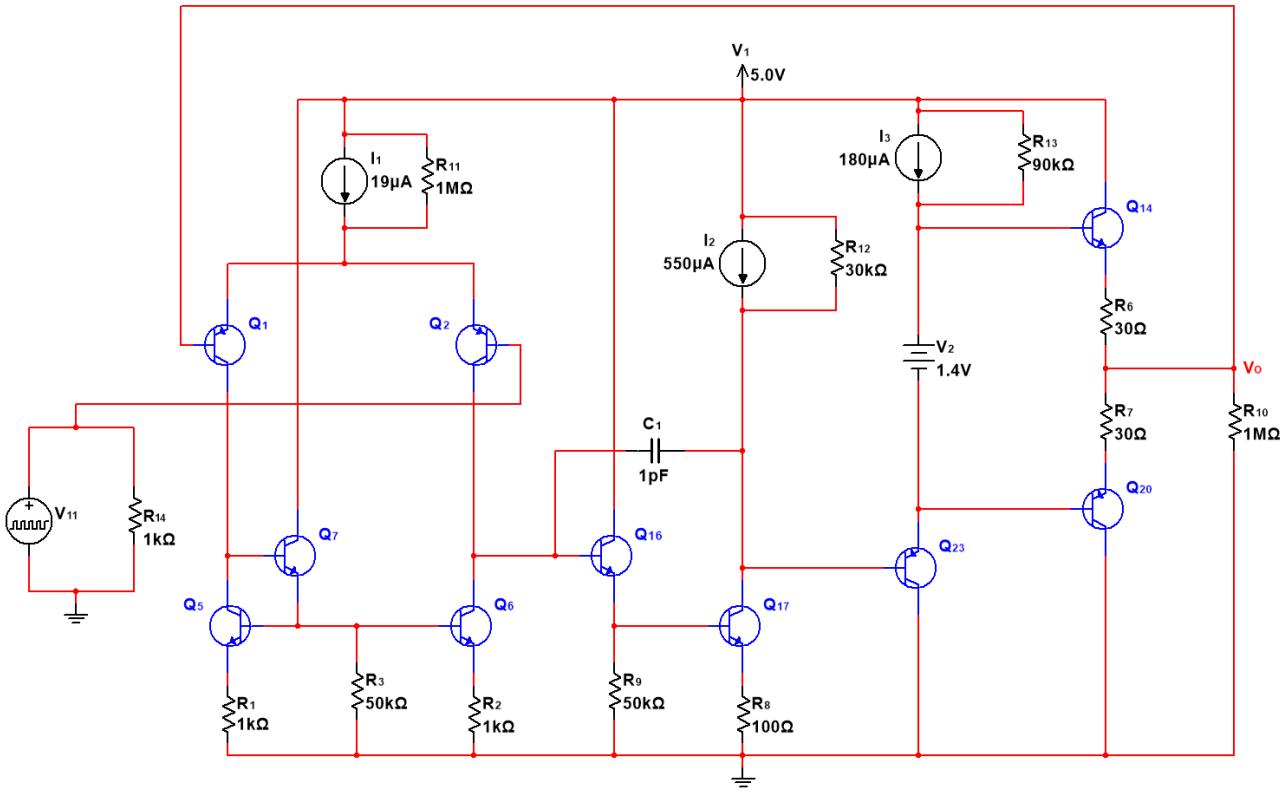

Figure 2: Op-Amp Set Up In Unity Gain Mode For Slew Rate Simulation (General Setup In Top Left-Hand Corner)

Frequency Response

This section uses the same circuit from the Differential Sweep section of lab 3. You can download the same ELEC3509_Lab3_Diff_OP_AMP.mp14 under a different name, or use the same circuit as earlier in this lab. This circuit is found in Figure 1.

The differential mode circuit can be used to perform the frequency response. We must check the input and output frequency, ie. V_{R10} and V_9. Set the amplitude of the input AC signal V_9 to 1 mV_{RMS}, and keep the differential voltage difference found in the Differential Sweep section of the simulations.

1. In Analyses and Simulation, run an AC Sweep, with a Start frequency of 1 Hz, and an End frequency of 10 MHz with 10 points per decade. The Vertical scale should be Decibels, and in the Output tab, analyse the probe on V_{R10} and V_9.
2. Save and run the simulation.
3. Export the results of the simulation to Excel, and analyse the results. Since the signal gain is found as V_{out}/V_{in}, and the AC Sweep only measures the dBV of the V_{out} and V_{in}, you must subtract the decibel input from the decibel output ($dBV_{A_V} = dBV_{V_{out}} - dBV_{V_{in}}$), this is the same case for the phase.
4. Find the unity gain point, along with the high frequency cutoff, and gain.

The frequency domain of the circuit is examined in this section. You will use the circuit configuration shown in Figure 2 for this part. Plot the differential magnitude and phase response of the circuit using Multisim between 1 Hz to 10 MHz with the input voltage set to unity. From the simulation results, what is the unity gain frequency f_u? Compare this result with the value calculated in the pre-lab.

Lab 3 Appendix: Sample Op Amp Calculations

Note: Before looking at this section, you should attempt to analyze the circuit on your own. IF YOU JUST COPY THE EQUATIONS AT THE END AND DO NOT TRY GOING THROUGH THE ENTIRE DERIVATION ON YOUR OWN, YOU WILL NOT LEARN ANYTHING, YOU WILL HAVE PROBLEMS GETTING YOUR SIMULATION TO RUN, AND WILL FAIL MISERABLY ON THE OP-AMP PART OF YOUR EXAM. This section is intended only as a guide in case you get stuck.

In the following pages are some handwritten notes on the analysis of the 741 op-amp. This will give you some more information, but will not give you the full answer – that is for you to work out. For example, the effect of the resistors in parallel with current sources will be that the total current is higher than the current source value. This has not been included in these sample calculations (except once just before the first schematic and it has a line through it when we decided to stick with the simple estimate of current).

In order to give you a starting point, the following set of calculations calculates some of the properties of an op-amp. The following schematic has been used, as seen in Figure 3. This is a reminder that this is a modified version of the 741 Op-Amp that you are to use. Note that there are some differences in the circuit. There are also some errors in the calculations. These have been left in deliberately so that you cannot just copy these numbers or the formulas. However you can follow through the analysis.

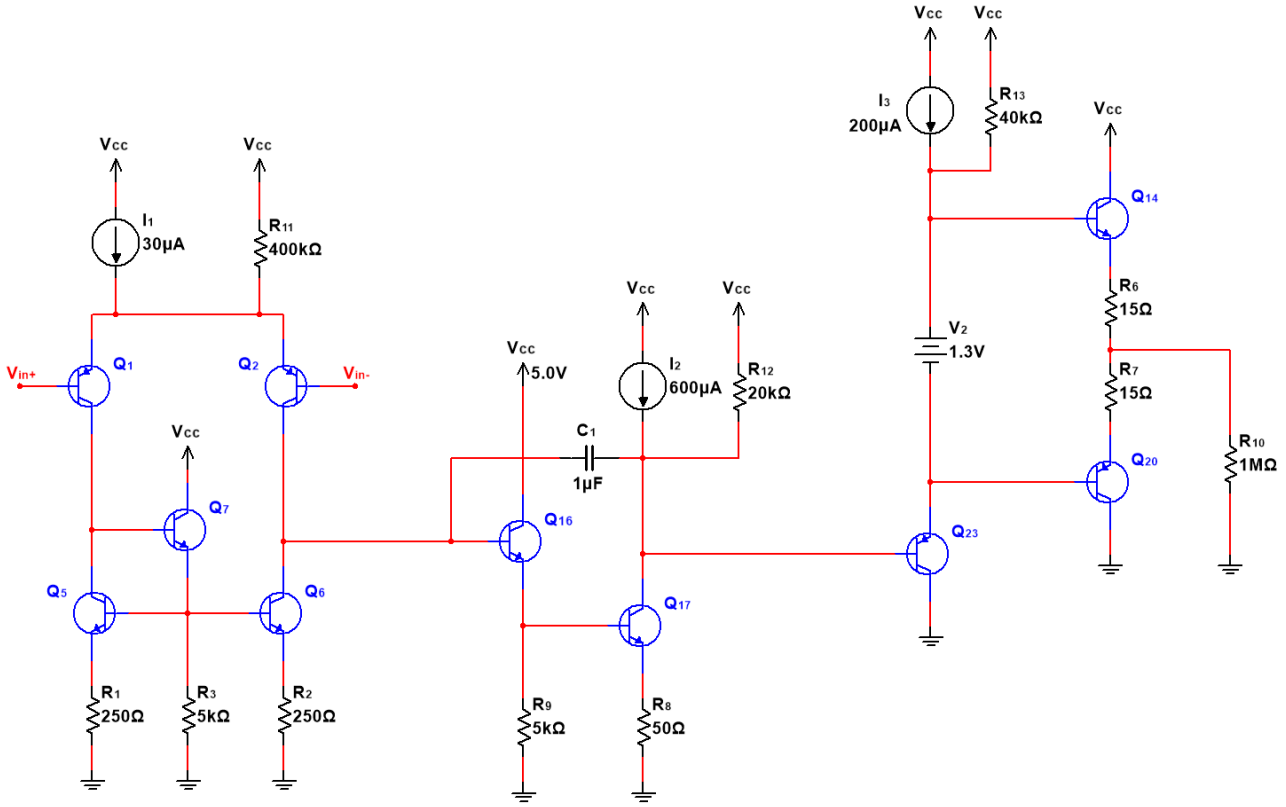

Figure 3: Schematic of Op-Amp Used For Sample Calculations. Incorrect parameters are used.

The following parameters are being used:

Parameter	NPN	PNP
Early Voltage (V_A)	30 V	10 V
β (Assume constant, but note that it normally depends on current)	200	200
I_S (Recall that $I_C = I_S e^{V_{BE}/V_T}$)	12.5 fA	7.5 fA
V_{BE}	0.5 V	0.5 V
V_{CC}	3.3 V	3.3 V

* **Note** that these values are completely different from the ones you will use for your prelab. Thus, you will

need to redo the calculations yourself using the correct values.

Last Stage

First, let us assume that the output is half of V_{CC}, and so is 1.65 V. Then, we can solve for the current flowing through Q_{14} and Q_{20} (ignore the load current for now).

Note that we cannot just assume a V_{BE} of 0.5 V for these transistors because the current flowing through this line is strongly affected by the V_{BE} of Q_{14} and Q_{20}. For the other transistors, we can make this assumption because the design of the circuit makes the bias point less dependent on the transistor parameters. We will investigate the impact of this sensitivity on the op-amp performance later.

Around the output, we can create the following loop equation:

$$1.3V = V_{BE20} + R_7 I_{E20} + R_6(I_{E20} + I_{R10}) + V_{BE14}$$

Remember that

$$V_{BE} = V_T \ln \frac{I_C}{I_S}$$

$$1.3V = V_T \ln \frac{I_{C20}}{I_{S20}} + R_7 I_{E20} + R_6(I_{E20} + I_{R10}) + V_T \ln \frac{I_{C14}}{I_{S14}}$$

And since that

$$I_C = \frac{\beta}{\beta + 1} I_E$$

$$1.3V = V_T \ln \frac{\frac{\beta_{20}}{\beta_{20}+1} I_{E20}}{I_{S20}} + R_7 I_{E20} + R_6(I_{E20} + I_{R10}) + V_T \ln \frac{\frac{\beta_{14}}{\beta_{20}+1}(I_{E20} + I_{R10})}{I_{S14}}$$

$$1.3V = 0.025V \ln \frac{\frac{200}{201} I_{E20}}{7.5 * 10^{-15} A} + 15\Omega * I_{E20} + 15\Omega * I_{E20} + 0.025V \ln \frac{\frac{200}{201} I_{E20}}{12.5 * 10^{-15} A}$$

$$1.3V = 0.025V \ln (1.3267 * 10^{14} A^{-1} * I_{E20}) + 30\Omega * I_{E20} + 0.025V \ln (0.796 * 10^{14} A^{-1} * I_{E20})$$

$$1.3V = 0.81297V + 0.025V \ln (I_{E20}) + 30\Omega * I_{E20} + 0.8002V + 0.025V \ln (I_{E20})$$

$$0 = 0.3132V + 20\Omega * I_{E20} + 0.05V \ln (I_{E20})$$

Solving numerically gives I_{E20} = 1.19 mA. This then lets us calculate the node voltages and currents the normal way. Note that this value of current is much larger than the current flowing through R_{10}, making our assumption of ignoring it valid. If the current was much smaller, we would need to redo our calculations.

Using the calculated currents, the BE voltages for Q_{14} and Q_{20} can be found.

$$V_{BE20} = V_T \ln \frac{I_{C20}}{I_{S20}} = 0.025 \ln \frac{1.18 * 10^{-3}}{12.5 * 10^{-15}} = 0.6318V$$

$$V_{BE14} = V_T \ln \frac{I_{C14}}{I_{S14}} = 0.025 \ln \frac{1.18 * 10^{-3}}{7.5 * 10^{-15}} = 0.6445V$$

This can be used to get the node voltages for the last state (note some rounding was done - high precision is not really required here due to all of the approximations we are making).

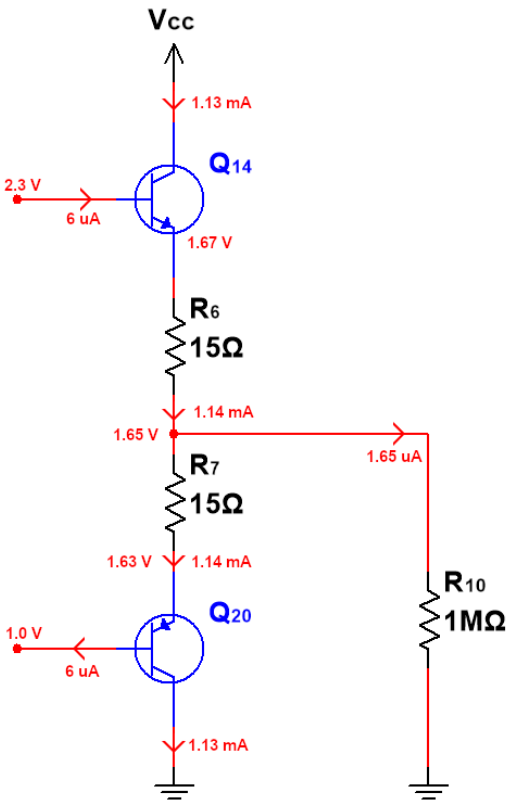

Figure 4: Schematic of Last Stage Showing Node Voltages And Line Currents

The next step is to determine the current flowing through Q_{23}. Since we know the node voltages for V_2, we can calculate the current flowing through R_{13}.

$$I_{R13} = \frac{V_{CC} - V_{2+}}{R_{13}} = \frac{3.3V - 2.3V}{40000\Omega} = 25\mu A$$

Second Stage

Combined with the current source and the 2 base currents of Q_{14} and Q_{20}, we get a collector current of 225μA, and we can calculate the remaining currents. We also assume that the BE junction voltage is 0.5 V

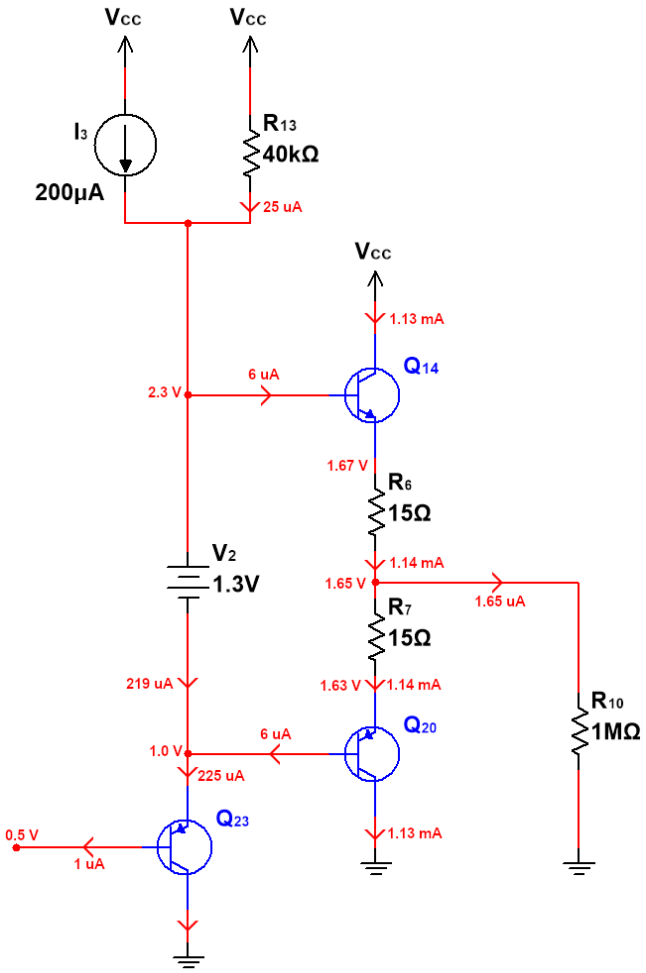

Figure 5: Schematic of Last Stage and Q23, Showing Node Voltages and Line Currents

Similarly, we then calculate the current flowing through R_{12}, and then find the total current flowing through the Q_{17}. The emitter current flows through R_8, allowing use to get the emitter voltage, and by extension, the base voltage (using $V_{BE} = 0.5$ V).

This, in turn lets us calculate the current flowing through R_9, and then we can get the node voltages and currents for Q_{16}.

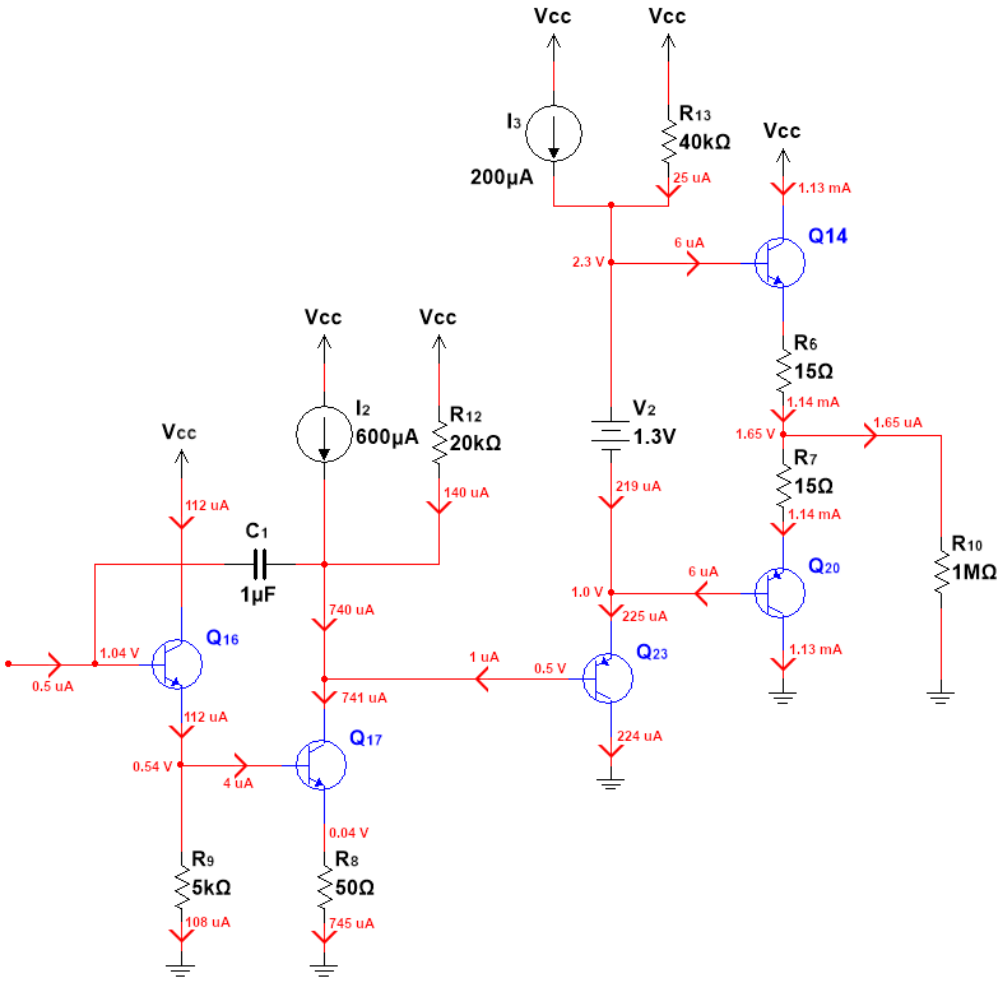

Figure 6: Schematic of Second Two Stages Showing Node Voltages and Line Currents

Input Stage

This leaves us with the input stage. First, we recall that the input common mode voltage is 1.65 V, and we assume each BE junction is 0.5V. This gives us the shared emitter voltage, and the current flowing through R_{11}. Then, we can fill out the rest of the circuit.

Looking at the node voltages, Q_{17} looks to be operating on the edge between saturation and active mode, and would likely change into saturation with a large signal amplitude. This is one of the issues with scaling the supply voltage. We will ignore this issue for now (in a real design, you would not be able to do this).

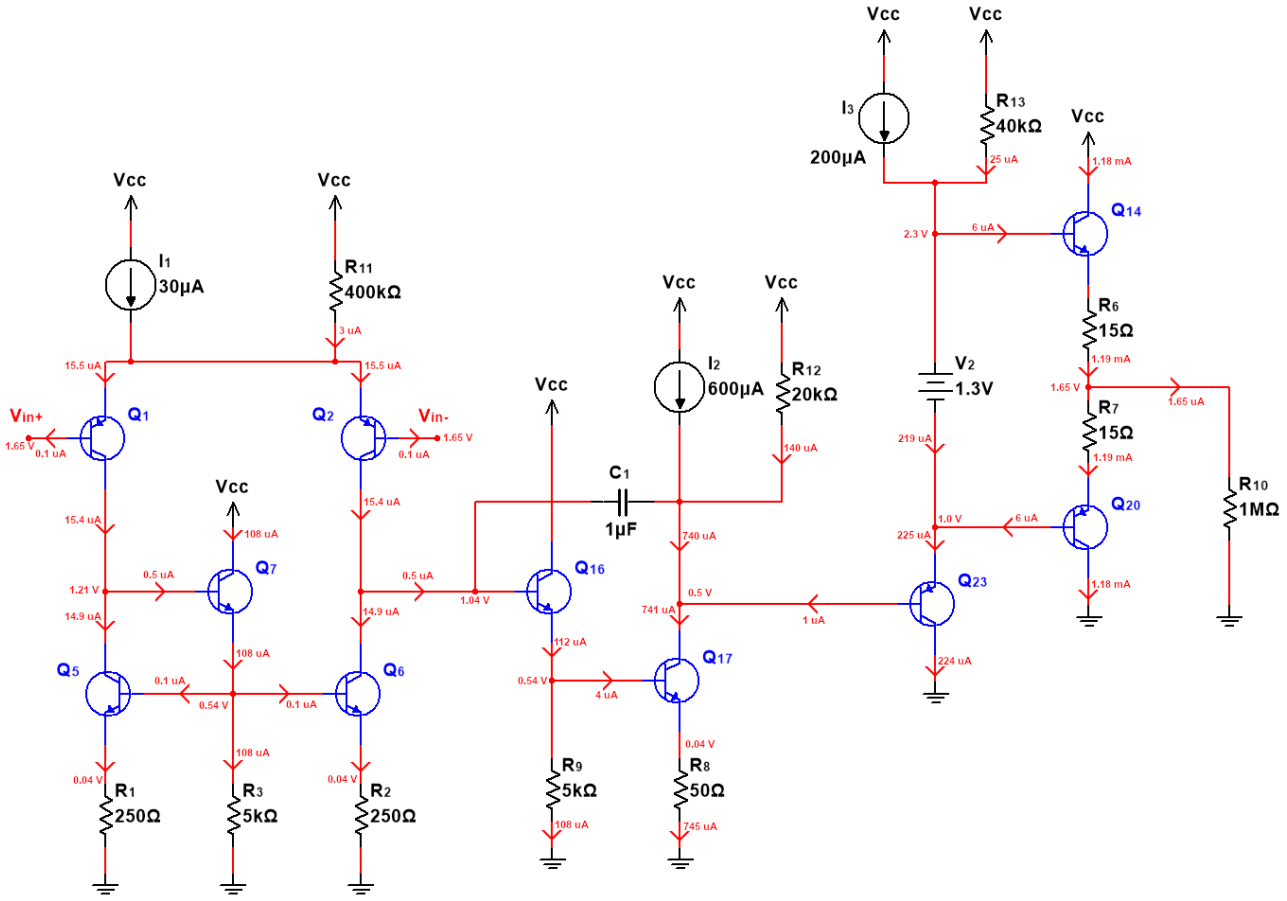

Figure 7: Schematic of all Stages Showing Node Voltages and Line Currents

Then, we can fill out the table of DC parameters:

Transistor	I_C (μA)	R_O (Ω)	g_m (mA/V)
Q_1 (PNP)	15.4	649k	0.616
Q_2 (PNP)	15.4	649k	0.616
Q_5 (NPN)	14.9	2.01M	0.596
Q_6 (NPN)	14.9	2.01M	0.596
Q_7 (NPN)	108	92.6k	4.32
Q_{14} (NPN)	1180	25.4k	47.2
Q_{16} (NPN)	112	89.3k	4.48
Q_{17} (NPN)	741	40.5k	29.6
Q_{20} (PNP)	1180	8.47k	47.2
Q_{23} (PNP)	224	44.6k	8.96

Next, we can perform the small-signal calculations.

We can analyze the circuit as 3 different stages. The only thing we have to keep in mind is that in each analysis, we must model the effects of the other stages. This is done by using linear models: recall that according the linear network theory, we can model any circuit as a single voltage/current source and an impedance (a resistance

here since we are dealing with mid-frequency analysis).

A small signal equivalent of the first circuit can be drawn as seen in Figure 8, but is quite complex. This is technically not a problem, as we can solve it even by hand, using some advanced network analysis techniques. The bigger problem is that this complex circuit does not lead to insight. This is an important drawback: in real life, we can always analyze a circuit as precisely as we want by using a simulator (provided we have accurate models and simulation algorithms- a topic for more advanced courses), but knowing what to simulate and what to components change depends on our own understanding of the circuit.

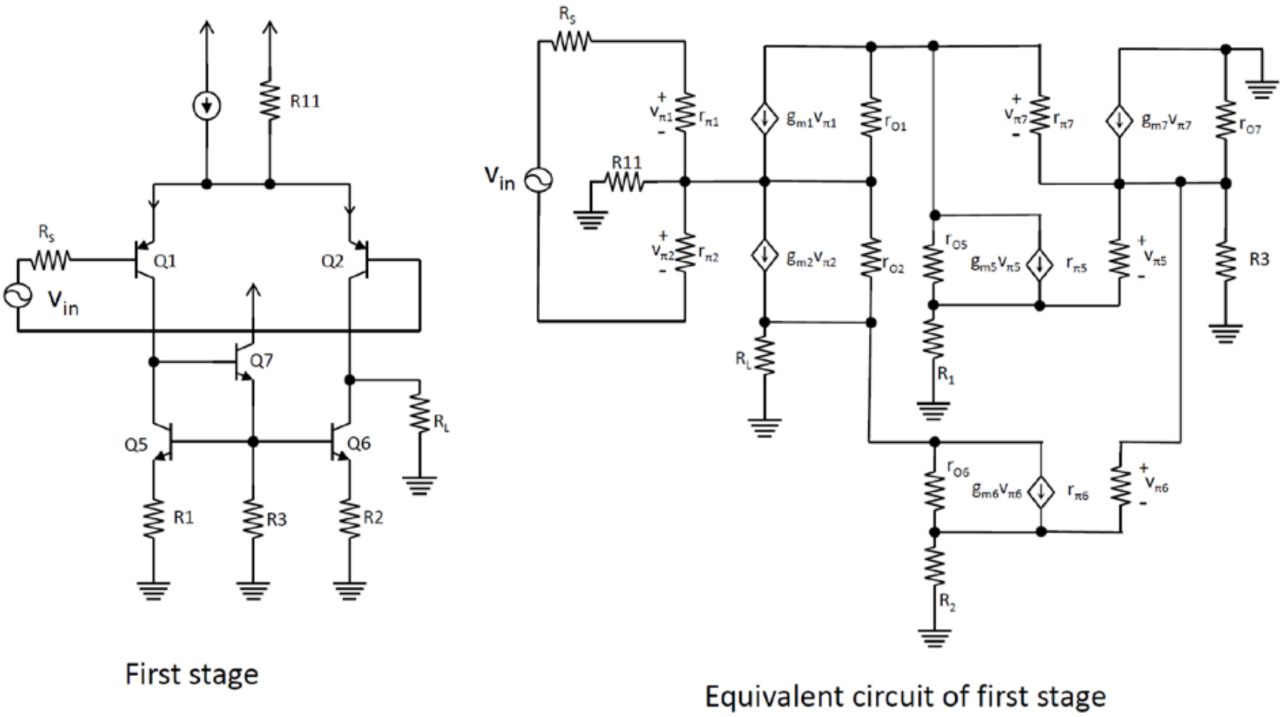

Figure 8: Schematic and Small Signal Equivalent of Differential Stage

Thus, we need to simplify the circuit substantially in order to figure out the basics for this circuit. This gives us a highly approximate solution, but lets us understand how the characteristics of the circuit are controlled. If we were to then improve the design, we could easily figure out what to do. An exact solution, even if it were tractable, would probably not let us do that.

Let us consider a simple differential pair driving a current mirror with no degeneration resistors and a single-ended load. The circuit and small signal equivalent model is shown in Figure 9.

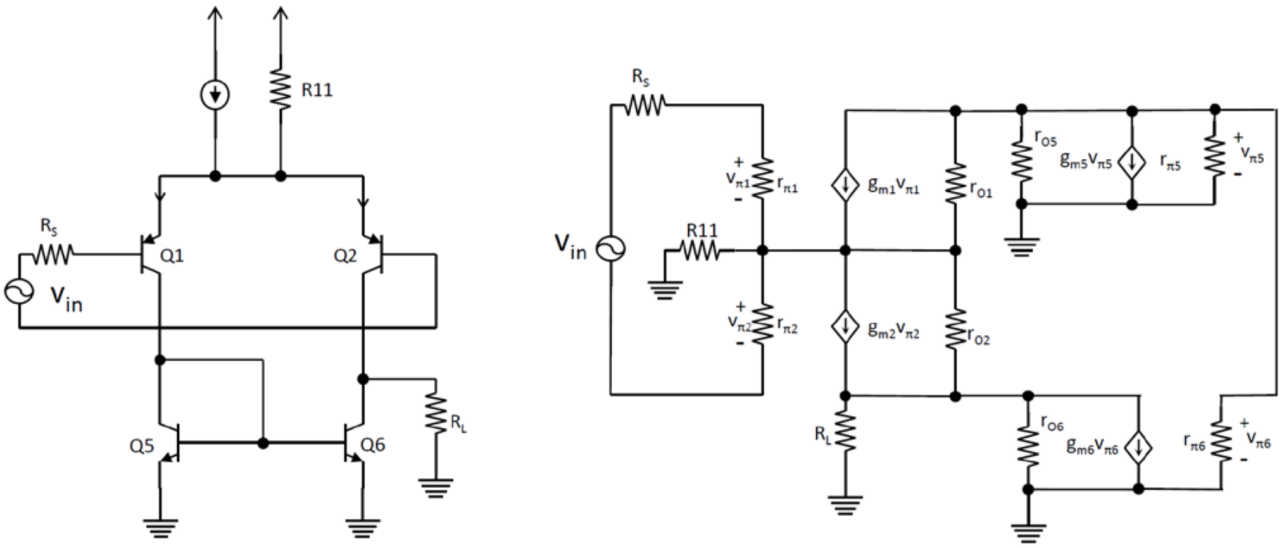

Figure 9: Schematic and Small Signal Equivalent of a Simple Differential Pair Driving a Current Mirror and Resistive, Single Ended Load

We can make some simplifications: recall that with a differential input, we get a virtual ground. Along this line in the middle, the potential will remain constant without the need for current to flow. Thus, we can remove this line with no impact on the circuit's behavior. This of course means we can remove R_{11} with no impact (no AC current is flowing through it). Also note that R_L and r_{O6} are in parallel. As for Q_5, we can make some more simplifications since the base and collector are shorted:

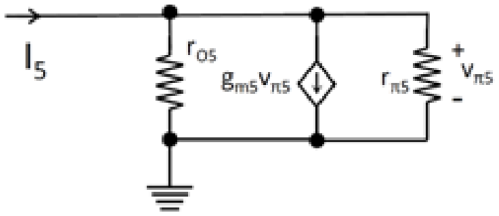

Figure 10: Small Signal Model of Q_5 of Simple Differential Pair

$$I_5 = \frac{v_{\pi 5}}{r_{o5}} + \frac{v_{\pi 5}}{r_{\pi 5}} + g_{m5} v_{\pi 5} = (\frac{1}{r_{o5}} + \frac{1}{r_{\pi 5}} + g_{m5}) V_{\pi 5} = \frac{V_{\pi 5}}{r_{o5} || r_{\pi 5} || \frac{1}{g_{m5}}}$$

And of course, these are parallel with $r_{\pi 6}$.

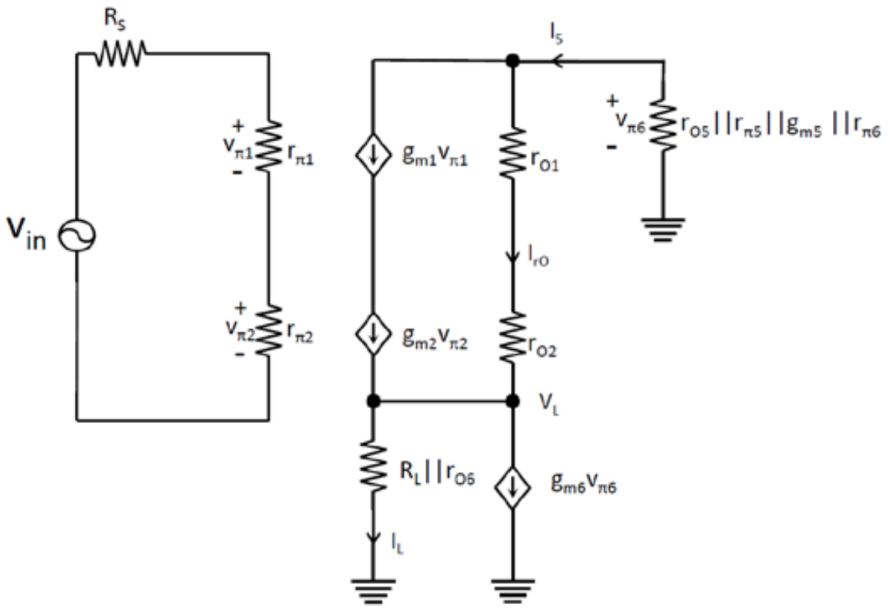

Figure 11: Simplified Small Signal Model of the Differential Pair

We can combine the two trans-conductance modules since both $r_{\pi 1}$ and $r_{\pi 2}$ and g_{m1} and g_{m2} should be identical (a reasonable assumption for a good differential pair) we can combine both. To handle r_{O1} and r_{O2}, we recall that the node connecting the two transistors is a virtual ground, and thus r_{O1} is in parallel with r_{O5}, $r_{\pi 5}$, etc. and r_{O2} is in parallel with the output impedance of Q_6 and the load resistance. We can then calculate the output voltage across the load resistor.

$$V_L = (R_L||r_{o6}||r_{o2})(g_{m2}v_{\pi 2} - g_{m6}v_{\pi 6})$$

We can eliminate $v_{\pi 6}$ using the following equation:

$$v_{\pi 6} = -(g_{m2}v_{\pi 2})(r_{o5}||r_{\pi 5}||\frac{1}{g_{m5}})$$

$$V_L = (R_L||r_{o6}||r_{o2})(g_{m2}v_{\pi 2} + g_{m6}(g_{m2}v_{\pi 2})(r_{o5}||r_{\pi 5}||\frac{1}{g_{m5}}))$$

Next, we note that 1 $g_{m5} = r_{e5}$ is much smaller than the resistances it is in parallel with. Also note that $g_{m5} = g_{m6}$ since both transistors should be biased identically:

$$V_L = (R_L||r_{o6}||r_{o2})(g_{m2}v_{\pi 2} + g_{m6}(g_{m2}v_{\pi 2})(\frac{1}{g_{m5}}))$$

$$V_L = 2g_{m2}v_{\pi 2}(R_L||r_{o6}||r_{o2})$$

Now we can look at the input stage and see that

$$v_{\pi 2} = \frac{r_{\pi 2}v_{in}}{R_S + r_{\pi 1} + r_{pi2}} = \frac{v_{in}}{2}$$

If we assume the source impedance is very small compared to the op-amp input impedance. This gives us

$$V_L = 2g_{m2}\frac{v_{in}}{2}(R_L||r_{o6}||r_{o2})$$

$$A_{v1} = \frac{V_L}{v_{in}} = g_{m2}(R_L||r_{o6}||r_{o2})$$

If the input impedance of the next stage is very large, are gain is partially limited by r_{O6}. Next, let us see what happens to the effective output impedance of the current mirror branch when we add a degeneration resistor (Note that the base is at virtual ground):

$$I_{out} = \frac{V_{out} + v_{\pi 6}}{r_{o6}} + g_{m6}v_{\pi 6}$$

Also note that we have

$$v_{\pi 6} = -I_{out}(R_2||r_{\pi 6}$$

which can be used to give

$$I_{out} = \frac{V_{out}}{r_{o6}} - \frac{I_{out}(R_2||r_{\pi 6})}{r_{o6}} - g_{m6}I_{out}(R_2||r_{\pi 6})$$

$$I_{out}(\frac{r_{o6} + (R_2||r_{\pi 6}) + g_{m6}r_{o6}(R_2||r_{\pi 6})}{r_{o6}}) = \frac{V_{out}}{r_{o6}}$$

$$R_{out} = \frac{V_{out}}{I_{out}} = r_{o6}(1 + g_{m6}(R_2||r_{\pi 6})) + (R_2||r_{\pi 6})$$

With the given bias point in the first stage of the op-amp, we can get the following:

$$R_{out} = 2.01M(1 + 0.000596(250||\frac{200}{0.000596})) + (1000||\frac{200}{0.000596})$$

$$R_{out} = 2.01M(1 + 0.000596(250||\frac{200}{0.000596})) + (1000||\frac{200}{0.000596})$$

$$R_{out} = 2.01M(1 + 0.000596(250)) + 250 \approx 2.01M(1.15) = 2.31M$$

Note that the degeneration resistance improved the output resistance by 15%. For this circuit, the 2MΩ output impedance is already quite large, so there is not much gained by doing this. However, with modern op-amps, the output impedance of a transistor can be 1kΩ or lower, making this technique much more useful. Unfortunately, the degeneration resistor requires a significant voltage drop, which is note easily spared in today's world of low voltage digital optimized I_C processes.

As we mentioned earlier, the circuit we have analyzed is not the same as the first stage of our op-amp, but it is close. The main difference is the higher output impedance of the current mirror, as discussed before- just replace the value of r_{o6} with the new calculated one. The other difference is the transistor Q_7, but the addition of this transistor causes the first stage current mirror to behave like the simple current mirror we described earlier, although it is still necessary.

Now that we have converted the circuit from differential to single ended, the analysis of the remaining stages is much easier. Below is the circuit and the small signal equivalent model of the second stage. To perform the analysis, we used the T-model for the CC amplifier, which makes things much easier.

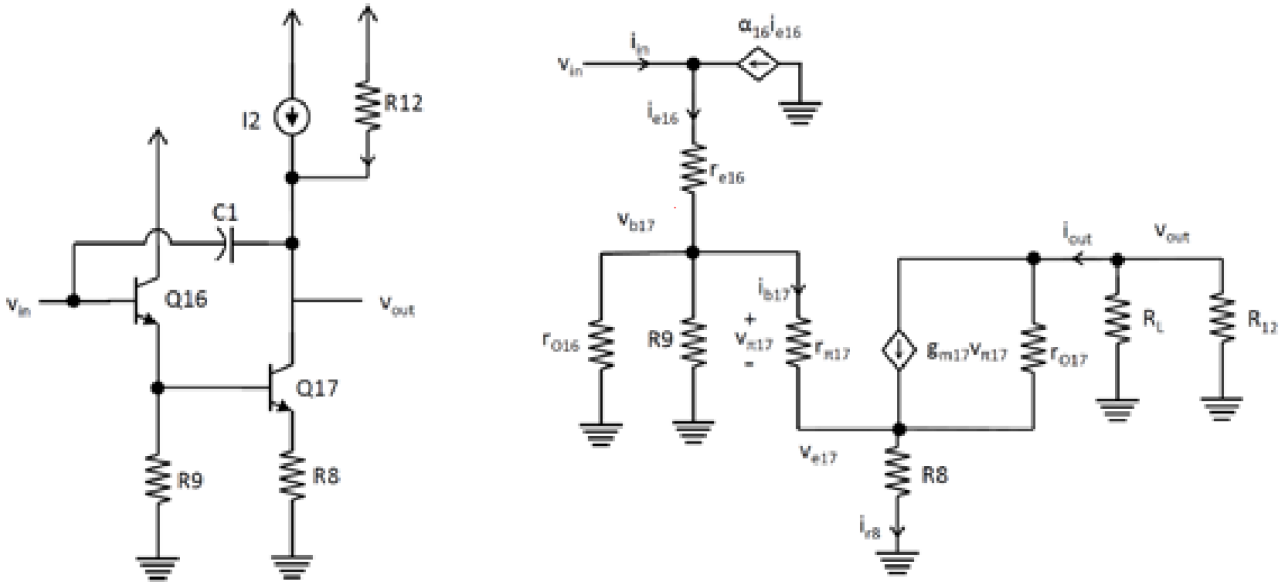

Figure 12: Schematic and Small Signal Model of the Second Stage

We start by first analyzing the CE stage. For the CE stage with degeneration (ignoring r_{O17}):

$$v_{out} = I_{out}(R_L||R_{12})$$

$$I_{out} = g_{m17}v_{\pi 17} = g_{m17}(v_{b17} - v_{e17})$$

$$\frac{v_{e17}}{R_8} = g_{m17}(v_{b17} - v_{e17}) + \frac{v_{b17} - v_{e17}}{r_{\pi 17}}$$

$$\frac{v_{e17}}{R_8||\frac{1}{g_{m17}}||r_{\pi 17}} = \frac{v_{b17}}{(r_{\pi 17}||\frac{1}{g_{m17}})}$$

$$v_{e17} = v_{b17}\frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{(r_{\pi 17}||\frac{1}{g_{m17}})}$$

$$I_{out} = v_{b17}g_{m17}(1 - \frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{r_{\pi 17}||\frac{1}{g_{m17}}})$$

$$I_{out} = v_{b17}\frac{g_{m17}}{1 + R_8 g_{m17} + \frac{R_8}{r_{\pi 17}}}$$

$$v_{out} = v_{b17}\frac{g_{m17}(R_L||R_{12})}{1 + R_8 g_{m17} + \frac{R_8}{r_{\pi 17}}}$$

Next for the input impedance of the CE stage:

$$i_{b17} = \frac{v_{b17} - v_{e17}}{r_{\pi 17}} = v_{b17}\frac{1 - \frac{R_8||\frac{1}{g_{m17}}||r_{\pi 17}}{r_{\pi 17}||\frac{1}{g_{m17}}}}{r_{\pi 17}}$$

$$i_{b17} = v_{b17}\frac{1}{r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}}$$

$$R_{in} = \frac{v_{b17}}{i_{b17}} = r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}$$

Next we can calculate the effect of the CC stage, which lets us calculate the gain:

$$\frac{v_{b17}}{v_{in}} = \frac{r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}{r_{e16} + r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_{b17}}\frac{v_{b17}}{v_{in}} = \frac{r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}{r_{e16} + r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17})}\frac{g_{m17}(R_L||R_{12})}{1 + R_8 g_{m17} + \frac{R_8}{r_{\pi 17}}}$$

We also need the input impedance:

$$i_{in} = i_{e16} - \alpha i_{e16} = i_{e16}(1 - \alpha) = i_{e16}(1 - \frac{\beta}{\beta + 1}) = \frac{i_{e16}}{\beta + 1}$$

$$v_{in} = i_{e16}(r_{e16} + r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}))$$

$$R_{in} = \frac{v_{in}}{i_{in}} = (\beta + 1)(r_{e16} + r_{o16}||R_9||(r_{\pi 17} + R_8 + r_{\pi 17}R_8 g_{m17}))$$

Finally, we can consider the last stage. Again, we draw the small signal equivalent model. Note that again we use the T-model, and that we have omitted r_o for all transistors for simplicity. We will need to put them back when we find the output impedance.

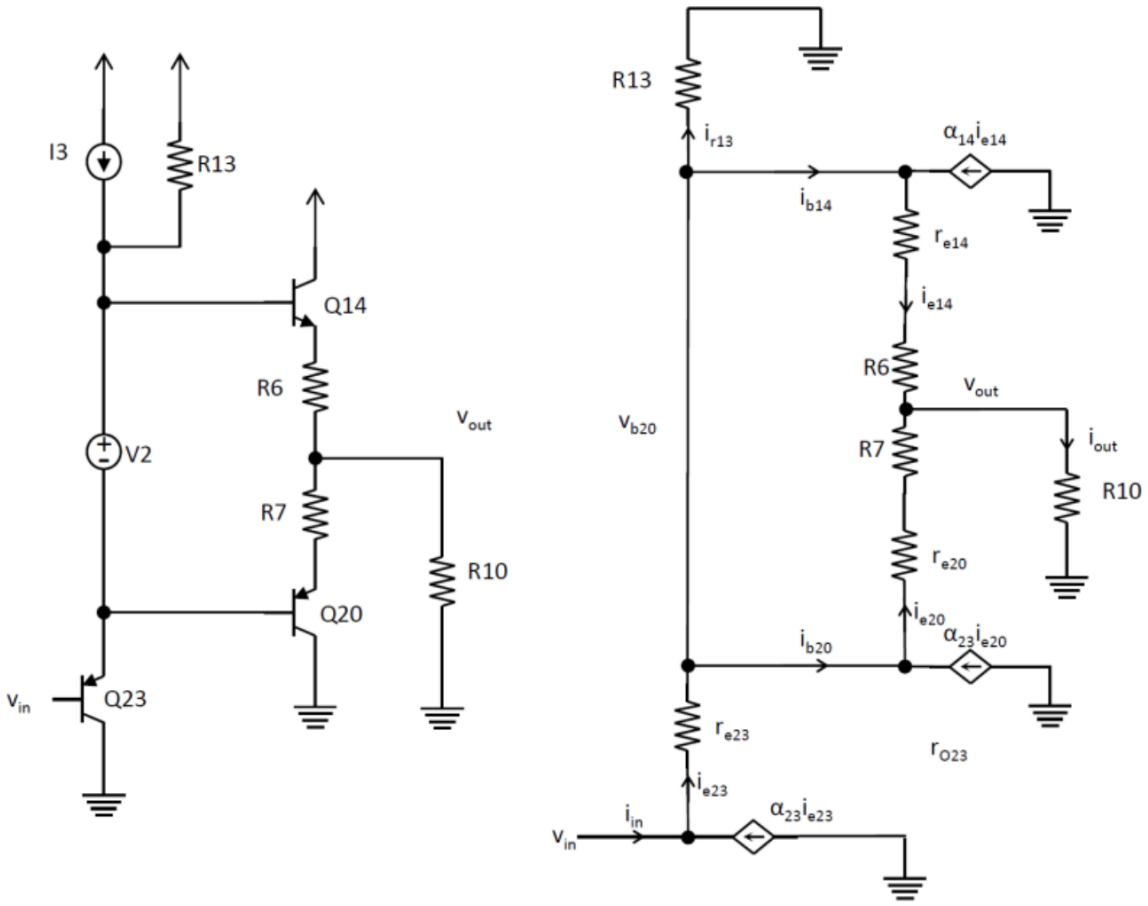

Figure 13: Schematic and Small Signal Model of the Third Stage

First, we find the input impedance of the second set of CC amplifiers:

$$v_{out} = i_{out} R_{10}$$

$$i_{out} = i_{e14} + i_{e20} = (\beta + 1) i_{b14} + (\beta + 1) i_{b20}$$

$$v_{b20} - v_{out} = i_{e14}(r_{e14} + R_6) = i_{e20}(r_{e20} + R_7)$$

$$(\beta + 1) i_{b14} = (\beta + 1) i_{b20} \frac{r_{e20} + R_7}{r_{e14} + R_6}$$

$$i_{b14} = i_{b20} \frac{r_{e20} + R_7}{r_{e14} + R_6}$$

$$R_{in} = \frac{v_{b20}}{i_{b14} + i_{b20}} = \frac{v_{out} + v_{b20} - v_{out}}{i_{b14} + i_{b20}} = \frac{i_{out} R_{10} + i_{e20}(r_{e20} + R_7)}{i_{b20} \frac{r_{e20} + R_7}{r_{e14} + R_6} + i_{b20}}$$

$$R_{in} = \frac{((\beta + 1) i_{b14} + (\beta + 1) i_{b20}) R_{10} + (\beta + 1) i_{b20}(r_{e20} + R_7)}{i_{b20} \frac{r_{e20} + R_7}{r_{e14} + R_6} + i_{b20}}$$

$$R_{in} = (\beta + 1) \frac{(\frac{r_{e20} + R_7}{r_{e14} + R_6} + 1) R_{10} + (r_{e20} + R_7)}{\frac{r_{e20} + R_7}{r_{e14} + R_6} + 1}$$

$$R_{in} = (\beta + 1) \frac{R_{10}(r_{e20} + R_7 + r_{e14} + R_6) + (r_{e14} + R_6)(r_{e20} + R_7)}{r_{e20} + R_7 + r_{e14} + R_6}$$

$$R_{in} = (\beta + 1)(R_{10} \frac{(r_{e14} + R_6)(r_{e20} + R_7)}{r_{e20} + R_7 + r_{e14} + R_6})$$

$$R_{in} = (\beta + 1)(R_{10} + (r_{e14} + R_6) || (r_{e20} + R_7))$$

From v_{b20}, the impedance to ground is just this impedance in parallel with R_{13}.

$$R = (\beta + 1)(R_{10} + (r_{e14} + R_6) || (r_{e20} + R_7)) || R_{13}$$

Note that because the beta values are the same for both PNP and NPN transistors, we can consider to two output paths to be parallel. As such, we can easily find the voltage gain from v_{b23} to the output:

$$\frac{v_{out}}{v_{b20}} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)}$$

The gain for the first stage is just a normal CC, so we can determine the gain and input impedance easily:

$$\frac{v_{b20}}{v_{in}} = \frac{(\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13}}{r_{e23} + (\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13}}$$

$$A_{v3} = \frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_{b20}} \frac{v_{b20}}{v_{in}}$$

$$A_{v3} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7)} \frac{(\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13}}{r_{e23} + (\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13}}$$

Of course, this gain will always be less than 1.

$$R_{in3} = (\beta+1)(r_{e23} + (\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13})$$

$$R_{in3} = (\beta+1)r_{e23} + (\beta+1)((\beta+1)(R_{10} + (r_{e14} + R_6)||(r_{e20} + R_7))||R_{13})$$

It can be seen that, if R_{13} is large enough, the double amplifier stage increases the output impedance by a factor of β^2.

As described in your notes, the capacitor C_1 is added deliberately to provide a dominant pole, which in turn determines the frequency response of the entire circuit. Just as with a transistor, the frequency at which the gain becomes 1 can be calculated:

$$\omega_T = A_0\omega_p$$

Where A_0 is the low frequency gain and ω_p is the pole frequency.

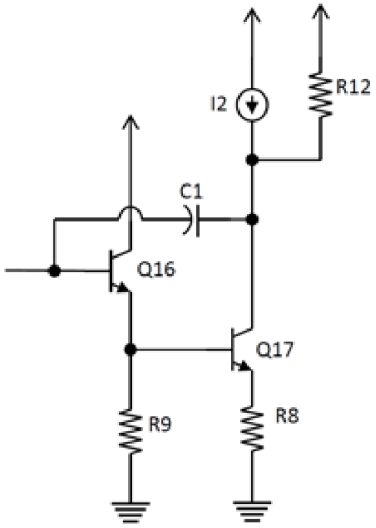

Figure 14: Schematic Showing the Position of C_1 in the Second Stage of the OP-AMP

As can be seen in the circuit above, C_1 links the output and input of the second stage. Assuming a large second stage gain, we can use the Miller multiplication to convert C_1 into 2 equivalent capacitances. Due to the large gain of the second stage, the dominant pole is formed by the first capacitance.

$$C_A = C_1(1 - \frac{v_{c17}}{v_{b16}}) = C_1(1 + A_{v2})$$

This capacitance is in parallel with the input impedance of the second stage and the output impedance of the first stage. The first value was calculated already, and the second value can be determined by the output impedance of the degenerated current mirror created by Q_{16}. Then, our pole frequency can be calculated

$$\omega_p = \frac{1}{C_A(R_{out1}||R_{in2})}$$

The slew rate can be determined by measuring the fastest rate of change of the amplifier. To perform this kind of test, we connect the op-amp in as a unity gain buffer:

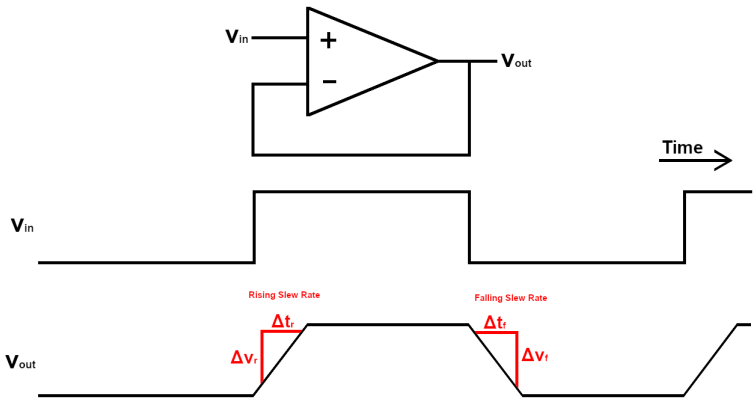

Figure 15: Schematic of the OP-AMP connected as a buffer and 2 Sample Input and Output Waveforms

For this analysis, the input signal is large in magnitude, and so we cannot use the simple linear models, but must instead consider the large signal models (the same ones we use for DC calculations).

The schematic below shows parts of the op-amp. With a large input spike, the BE junction of the first transistors is immediately decreased sharply, causing the transistor to enter into the cutoff mode, effectively shutting it off. The current flowing through the current source attempts to remain constant, so all the current must flow through Q_2. Note that as the left branch no longer has any current flowing through it, Q_6 will shut off and by extension, Q_7 since they share the same base voltages. Thus, all the current must flow into the input of the second stage.

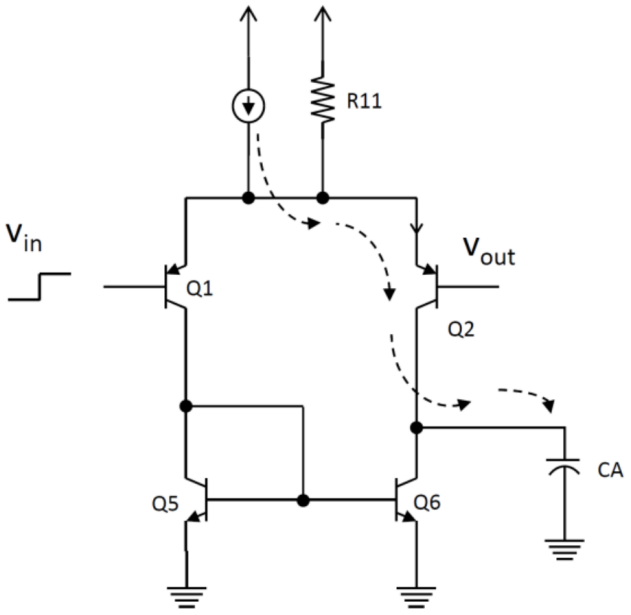

Figure 16: Schematic of OP-AMP Circuit Showing Used for Analysis of Slew Rate

The reaction speed of the circuit is limited by the presence of C_1. When we use the Miller model, it is obvious that the fastest rate of change occurs when all of the current flows into C_A: because of the huge size of C_A, this is a good assumption. This gives us the rate of change for the input of the second node, but not the output. But we know that the output of the second stage compared to the input is simply A_{V2}, and the gain of the third stage is approximately 1. Note that the gain of the second stage increases the effective capacitance, so it is cancelled out. Thus:

$$\frac{\Delta V_{out1}}{\Delta t} = \frac{I_1}{C_A}$$

$$\frac{\Delta V_{out2}}{\Delta t} = A_{V2}\frac{\Delta V_{out1}}{\Delta t} = A_{V2}\frac{I_1}{C_A} = A_{V2}\frac{I_1}{A_{V2}C_1} = \frac{I_1}{C_1}$$

$$slewrate = \frac{\Delta V_{out3}}{\Delta t} = \frac{\Delta V_{out2}}{\Delta t} = \frac{I_1}{C_1}$$