Lab 2 Day 2: The Amplifier Project

Electronics II

Contents

Design Project for Days 2 and 3

During the remaining two lab periods of lab 2 you are expected to design a cascode amplifier similar to Figure 1. You will assemble and test your circuit to verify that it meets the expected requirements.

The onus for correctness in the design is on the student. The TAs are there to help you, but not to do your design for you. You want to have your design ready for Day 2. Your amplifier should be working by the start of Day 3 so that the TAs may check out all students before the end of the period.

Cascode Amplifier Requirements

A cascode amplifier is a type of cascade amplifier, with the cascode amplifier consisting of a common base following a common emitter transistor. This is only one type of amplifier, and it is very similar to that of Day 1's CE-CB 2 Transistor amplifier.

You will need to design a cascode amplifier, which should be built and tested to meet the following requirements:

1. Magnitude of the voltage gain = 12*SQRT(Z+35):± 10%, where Z is the sum of the last 3 digits of your student number.
2. The load resistance $R_L = 6*(Z+40)^2$ Ω, rounded up to the nearest standard value stocked in the lab, i.e., decade multiples of 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, and 8.2 kΩ. As an example, if your R_L is 67.4 kΩ, you will round this to 68 kΩ.
3. The high frequency cutoff f_H is to be maximized. **It must exceed 1 MHz**.
4. The output voltage should be able to get to 2 V peak-peak without appreciable distortion[1]. To ensure this, the AC base-emitter voltage must be kept under 10 mV peak-peak for such an output.
5. No DC current may flow in R_L and no DC current may flow into or out of the signal generator.
6. The low frequency f_L must be less than 200 Hz.
7. The input and output impedances are left to the discretion of the designer, but their magnitudes at 1 kHz are to be determined by calculation and then measured.
8. Total circuit power is not to exceed 50 mW.
9. The transistors are all to be 2N3904.
10. Collector currents in the transistors are to be 1.0 mA ±10%.
11. Power-supply voltages are to be limited to +5 volts and/or +15 volts and/or -15 volts.
12. No adjustable components, e.g. a trimmer potentiometer, will be allowed.
13. Available capacitors are limited to: 1 x 100 μF, 1 x 33 μF, 1 x 10 μF, 2 x 1 μF, 1 x 0.1 μF [2].
14. The choice of all other components is left up to the designer.

[1] Many students have a hard time deciphering if their signal is distorted or not. Your input is a sine wave and your output should also be a sine wave. Distortion can be obvious (jagged edges, clipping) or more subtle (rounder peaks compared to valleys

[2] As a designer, you want your components to be small in size to fit on a PCB, or into an Integrated Circuit. This means a higher value capacitance should be avoided whenever possible, as higher capacitances require significantly more area than diode and resistive components. This also means that large inductors should be avoided for similar reasons.

Design Approach - To Be Done By Days 2-3

There is no unique solution to the amplifier design problem that has been laid out. There are more variables in the circuit than there are design parameters that have to be met. Consequently, a design solution requires the fixing of some of the unspecified degrees of freedom in the circuit in order to begin to solve the problem. In almost all cases the solution requires iteration because the choices made to optimize one design parameter will often impact negatively on the other parameters.

In the Appendix an example design approach is presented for a single-stage common-emitter amplifier, along with many of the assumptions and approximations that are usually made in making the problem tractable. Much of what will be presented will provide insight into the design of the project amplifier, and indeed, much of it can be directly applied, or modified to suit. The course notes should also provide significant insight as to how to start your design.

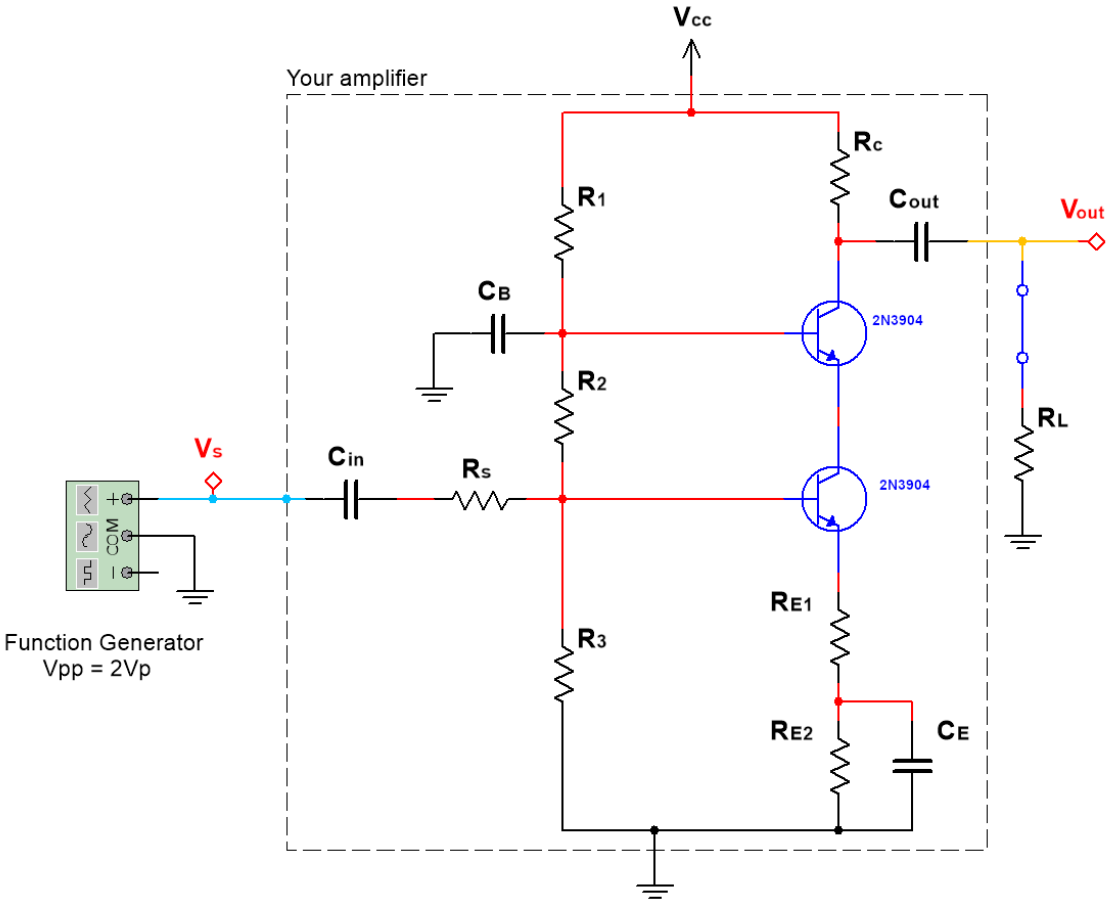

Figure 1: Schematic of Cascode Amplifier

* **Note** that this figure is built off the cascode amplifier starting template file on Nagui's website.

Figure 1 shows an example schematic. The signal generator will likely need a voltage divider in order to get a small enough input signal, but is not actually part of your circuit. R_S and R_{E1} are used to reduce the gain which is needed, due to the large value of R_C need to maintain a small AC V_{BE}. You don't need both of them, but you will need one or the other.

Additional Design Practice Suggestions

The following short list of practices is intended to give a starting point for setting some of the additional parameters found in two-transistor amplifiers.

1. Set the collector currents of the transistors to the same value unless there is good reason not to.
2. A single base-bias network is used to provide the base currents for two transistors. Set the bias network current to be about 10 times the sum of the two transistor's base currents.

3. For the cascode configuration, it is reasonable to initially allot 0.1 to 0.3 of the V_{CC} supply voltage to R_E, 2 to 3 volts to the V_{CEQ} of the lower transistor (to make sure that it is in the active mode yet still leave ample signal swing for the output), and to allot the remaining supply voltage to the upper transistor and R_C.

Pre-lab

Design your Cascode amplifier and show it to a TA. You will be choosing **resistors** and **capacitors** that will allow you to meet the specific requirements stated below. **This design needs to be ready at the start of the lab**.

Experiment

* **Note** that it is often the case with ICs that the only probes available to the designer is that of the input and output, and the rest must be derived similar to that of any other black box testing. In the case of simulation, you are able to probe each individual component, although this is hardly suggested.

As a fun challenge to the students, try to extract all the parameters by only measuring the current/voltage from outside the dotted line of the amplifier.

Simulating the Circuits in Multisim

- Download the file ELEC3509_Lab2_Cascode_Amplifier from Nagui's website, and open the file in Multisim 14:

  `http://www.doe.carleton.ca/~nagui/Elec3509/Lab2/`

- You must construct the cascode amplifier inside the dotted box, and attach the input and output to get the signal. All of the components needed can be found in the Place → Component menu in the Sources, Basics, and Transistors Groups.
- Run an Interactive simulation, and open the 2 channel oscilloscope window to see the signal. You should be able to take measurements of the input and output signals easily. Simple measurements of voltage or amperage can be taken with probes at Place → Probe.
- Measure R_{in}, R_{out}, A_{mid}, f_H and f_L using the same techniques that you did in Lab 2 Day 1. It is not uncommon for your initial circuit to miss some of these requirements, so be prepared to iterate. When tweaking your design you want to understand the circuit and identify which component can be adjusted to change a certain performance metric. This is especially true with f_H.
- In order to demonstrate the amount of **distortion** your amplifier has as the signal amplitude increases, you will need to make a series of measurements:
  - Measure the input and output peak-peak voltage swings at a low input signal amplitude (6 mV peak-peak).
  - Gradually increase the input signal and again measure the peak-peak voltage swing of both the input and the output. Keep this up until at least 80 mV peak-peak at the input. Use at least 15 points.
- Create a **frequency response** plot of gain vs frequency. Take 50 - 60 measurements starting lower than f_L and going significantly beyond than f_H.

  To perform an AC Sweep for this function:
  - Open Simulate → Analysis and Simulation, and open the AC Sweep menu.
  - Start at 1 Hz, and Stop at 100 MHz. It should be a Decade Sweep Type, with 20 points per decade. The Vertical Scale should be Decibels.
  - In the Output menu of the AC Sweep simulation, you must include the input V(vs), and the output V(vout).
  - Run the sweep, and analyse the output. In the Grapher View window, go to Tools → Export to Excel, and save the Excel file to your H:Drive.
  - You should keep in mind that the AC Sweep takes the dBVp ($20*\log_{10}(V_{\text{signal peak}}/1V_{\text{peak}})$) of the signal, so in order to get the dB of your signal, you must subtract the input signal dBVp from the output signal dBVp.

Digitally Amplification of the Human Voice (Microphone and Speakers needed)

One of the advantages of Multisim is that the tools you use can be connected to the circuits you want to simulate. As an example only, we can amplify the human voice using LabVIEW Instrument's Microphone and Speaker, even through a Remote Desktop Environment.

This is not necessary for your lab, although it is well worth your time if you want a real application of this software.

Connecting your Mic through the Remote Desktop Environment (Windows)

- Save your file, and close your Multisim software. Also log out of the jpKnight environment. Now prepare to log in again using the Remote Desktop Connection application.
- In the Remote Desktop application, Show Options → Local Resources, and in the Remote Audio panel, open Settings...
- In the new window there should be two panels: Remote audio playback (Set to Play on this computer) and Remote audio recordings (Set to Record from this computer). Press OK, and Connect to jpKnight.

Powering the Amplifier with your Voice

- Open the cascode amplifier file from your H: Drive, and save the new file separately from the normal cascode file.
- Remove the input function generator.
- In Simulate → Instruments → LabVIEW Instruments find the Microphone and Speaker to add to the design window.
- Keep in mind, the output from the Microphone has a peak voltage of around 20 mV, so you can adjust the amplitude of the input signal using a voltage divider like that found in Day 1's AC voltage measurements for the CE amplifiers.
- The output of the Microphone should feed into V_S, and a Speaker should listen to the Microphone on V_S, the input of another Speaker should connect to V_{out}. Open the Speaker and Microphone windows, and make sure both devices are using the Remote Audio Device, recording for a 5 second duration, and sampling at 22000 Hz. You can Record Sound, and speak or play music into your Microphone.
- If your Microphone and Speaker are attached, change the simulation type to an Interactive Simulation, and set the End time to 5 seconds, like that in the Microphone and Speakers. Run the simulation, and let the 5 second simulation run until the Transient time (Tran) in the bottom right corner reaches 5.000 s.
- Stop the simulation, and open the Speaker window to Play Sound (Be careful, as this sound may be very amplified).
- Comment on any distortion that might have occurred between the input and output Speakers.
- Change some values to get a large amount of distortion by changing the biasing conditions.

Results

As with all labs, you must show your pre-lab work and calculations for both parts of the lab. You need to show several plots and tables in order to clearly demonstrate that your circuit meets specifications. For R_{in} and R_{out}, show a table comparing measured and calculated results. Explain any significant differences.

Show a plot showing measured gain vs. frequency. Show the theoretical result you expected using your pre-lab calculations (the gain should be constant across your frequency range and that the f_H and f_L represent parts where the gain drops by 3 dB. Also note that past f_H or f_L, the gain drops by 20 dB/decade. Show solid lines indicating the minimum and maximum gain that is required, as per the specifications. See Figure 2 for a similar example (this is for a filter, not an amplifier).

Show a plot measuring gain as a function of input peak-peak voltage swing. The x-axis (input voltage) should be plotted on a log scale, and the gain should be plotted in dB. Calculate the gain as the ratio between output

and input peak-peak voltage swings. The gain should be constant for low voltage swings, and drop as the input increases (sometimes a rise is possible). Identify the location where the gain differs from the low signal gain by 1 dB (you may need to interpolate). In later courses, you will learn about something called the 1-dB compression point - just so we are clear, this is NOT how you measure it, but we will ignore this for now.

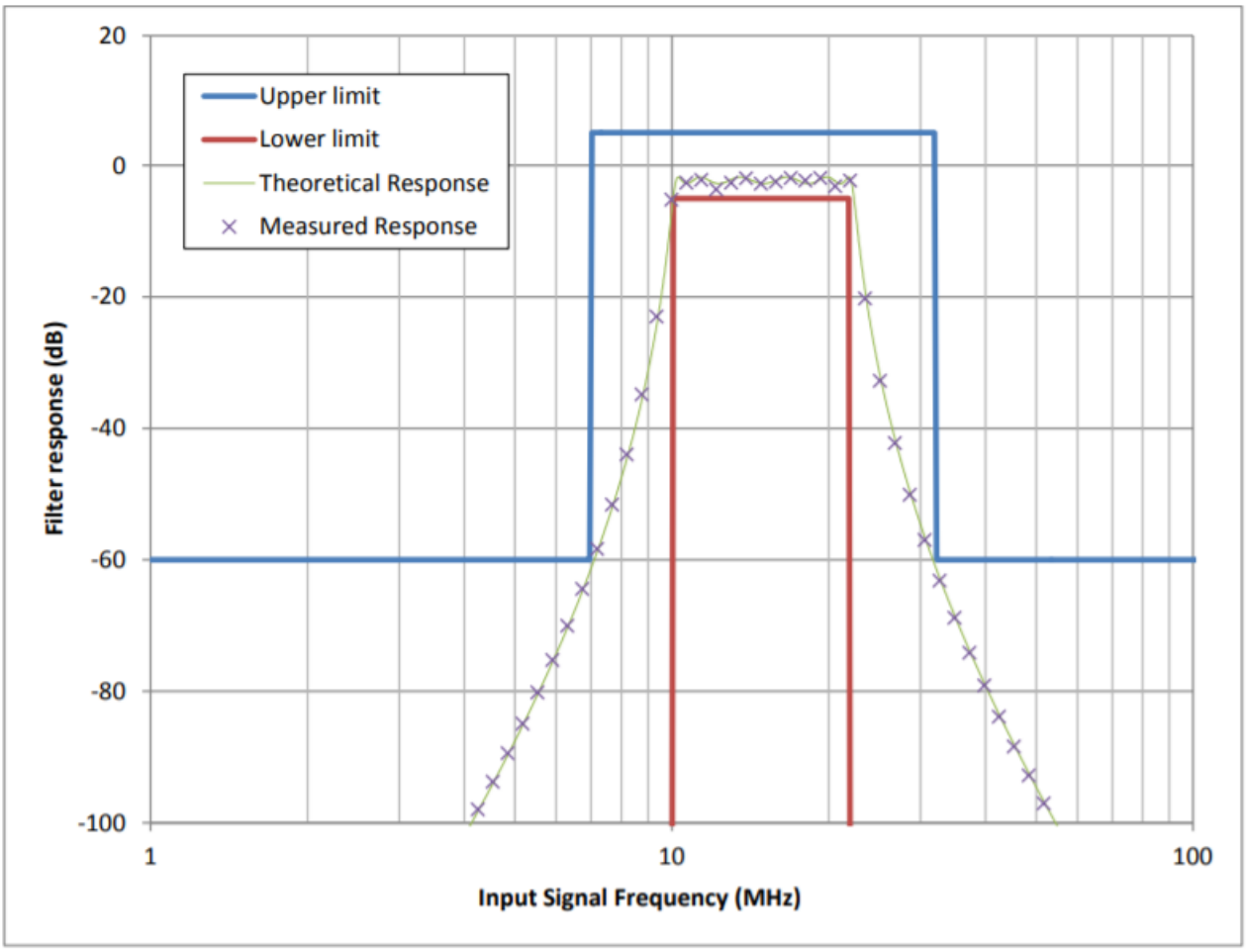

Figure 2: Example of a Graph Showing Measured, Calculated and Required Response of a Band-Pass Filter

APPENDIX

Example Design Approach for a Classical Common-Emitter Amplifier

As an example design approach we will consider the classical common-emitter voltage amplifier with a four-resistor bias network, as shown in Figure 3.

In designing such a circuit, it is generally first necessary to establish the DC bias conditions in the circuit. This action fixes many of the free variables thus making the subsequent design choices simpler. Unfortunately, at this point, the establishment of the DC bias conditions must be done with only a qualitative understanding of their implications on the other design parameters, likely making the solution sub-optimal. However, it does provide the most efficient starting point for the design.

Following the establishment of the DC bias conditions, the AC characteristics can be set. If this first design proves to be inadequate, the process can be repeated, under different assumptions, and the circuit improved. This iterative approach may have to be repeated several times before a satisfactory solution is generated.

The approach proceeds as follows:

1. **Choose $\mathbf{I_{CQ}}$:** Setting I_{CQ} (or I_{EQ}) is often the most reasonable starting point as it is fairly simply related to many design parameters that are often specified. The collector current itself, or the output current of the circuit, or the power dissipated in the circuit, may be specified. In addition, if a wide-bandwidth or high-frequency amplifier is called for, it may be necessary to optimize I_{CQ} in order to maximize f_T of the transistor. Trade-offs exist between these considerations in determining I_{CQ}.

2. **Choose Power-Supply Voltage(s):** In making this choice, consideration must be given to any restrictions that may exist on the choice, such as power dissipation in the circuit elements, what voltages are available, and the magnitude of the output voltage swing that is required.

3. **Choose $\mathbf{V_{EQ}}$:** This choice involves a direct trade-off between bias stability, with respect to variations between individual transistors, variations in temperature etc., and the magnitude of the required output voltage swing. Figure 3 shows this trade-off in a graphical form. Typically, V_{EQ} is chosen to be between 0.1 V_{CC} and 0.3 V_{CC}.

4. **$\mathbf{R_E}$ is now defined by:**

$$R_E = \frac{\alpha V_{EQ}}{I_{CQ}}, \alpha \approx 1 \tag{0.0.1}$$

$$\therefore R_E = \frac{V_{EQ}}{I_{CQ}} \tag{0.0.2}$$

   Choose the nearest standard resistor value, and recalculate V_{EQ} based on this real value.

5. **$\mathbf{I_{BQ}}$ is now defined by:**

$$\therefore I_{BQ} = \frac{I_{CQ}}{\beta_{DC}} \tag{0.0.3}$$

   As β_{DC} can take on a range of values, consult the manufacturer's specification of β_{DC}. This choice will guarantee that the subsequent design will provide enough base current for the transistor, regardless of what actual transistor is put into the circuit, which is a valuable advantage in production.

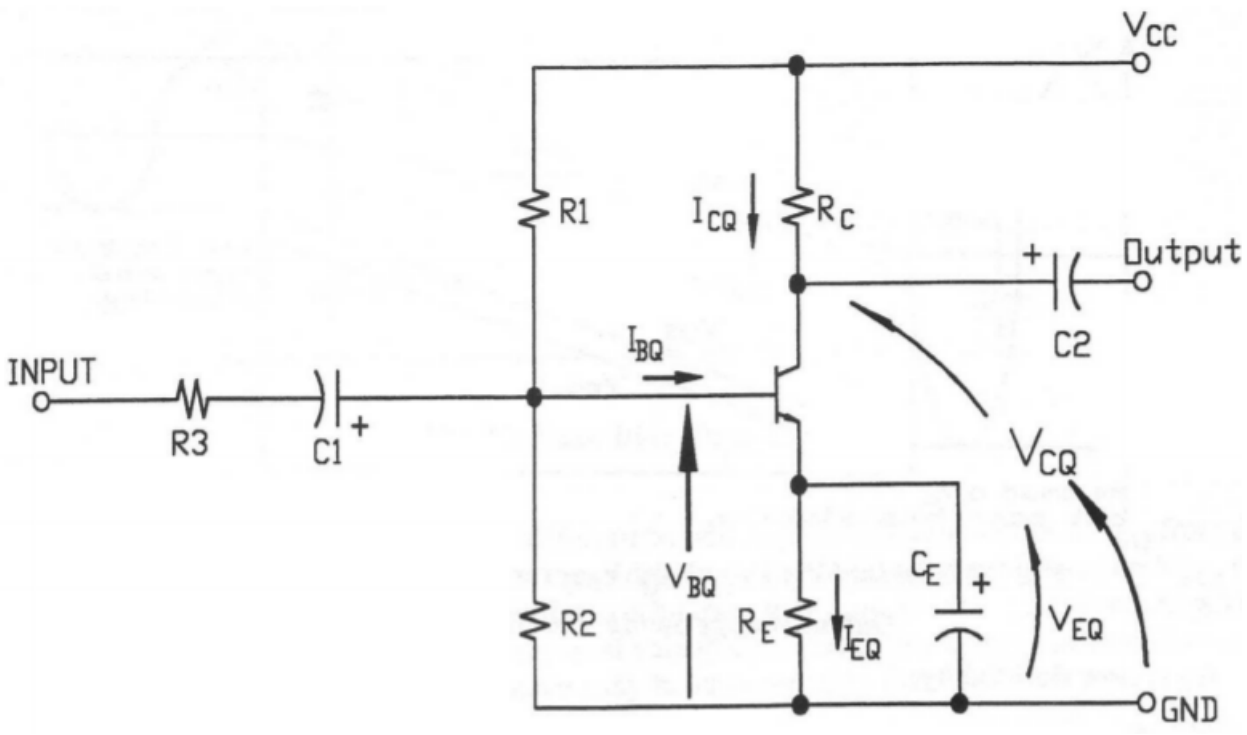

Figure 3: The Classical Common-Emitter Amplifier

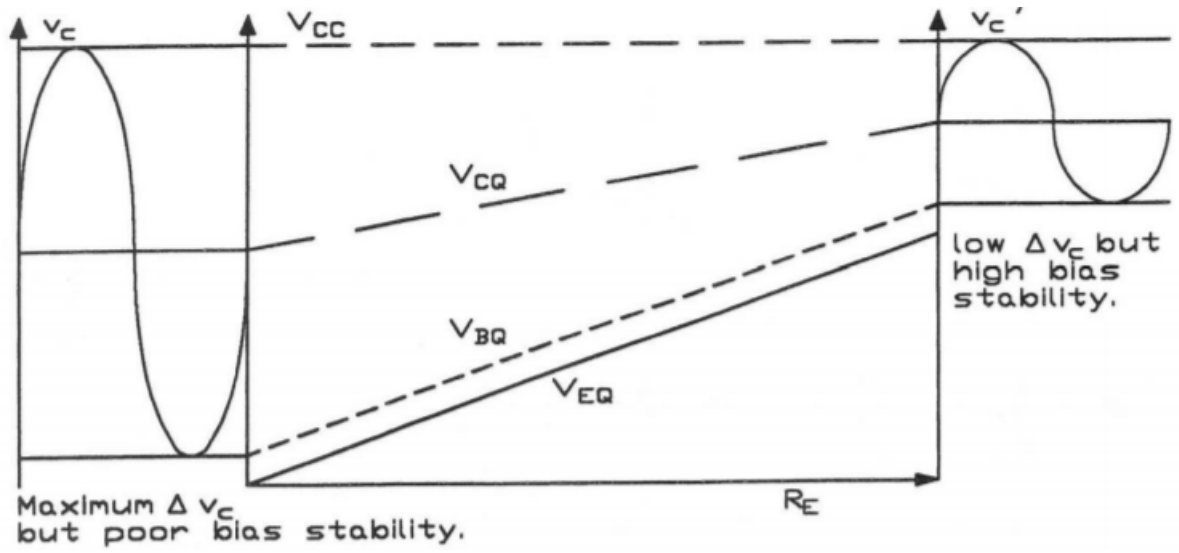

Figure 4: Graph of V_C, V_{CQ}, V_{BQ}, V_{EQ} Versus R_E Showing the Available Output Voltage Swing and Stability Trade-Off

6. **Choose the Base Bias Resistors, R_1 and R_2:** In the circuit, the base bias resistors fix the base voltage and provide the base bias current to the transistor. The process of choosing the resistors is best broken down, as follows:

   (a) The base bias circuit is analyzed. Figure 5 shows the base bias circuit removed from the rest of the amplifier.

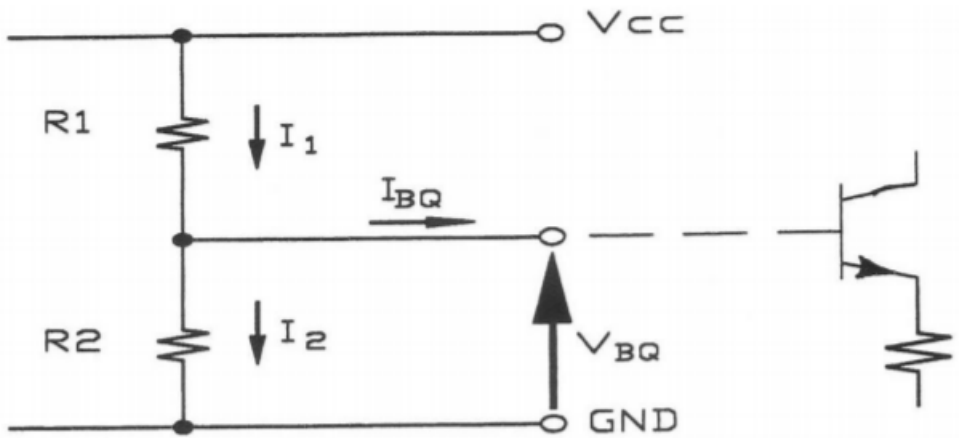

Figure 5: Base Bias Circuit

Different transistors with different values of β will require different values of I_{BQ} from the bias circuit. To minimize the effect that these different current demands will have on V_{BQ}, the bias network currents, I_1 and I_2, should be much larger than I_{BQ}. On the other hand, to get large values of bias network currents may cost valuable power, and/or imply such small resistor values that the circuit's input impedance may be unacceptably low.

As a very practical and easy-to-work-with compromise, I_2 is usually made to be about 10 x I_{BQ}. Thus set: I_2 = 10 x I_{BQ}; I_1 = 10 x I_{BQ} + I_{BQ} = 11 x I_{BQ}

(b) V_{BQ} is defined by choices already made to be: $V_{BQ} = V_{EQ} + 0.7$ volts

(c) R_1 and R_2 are now defined by the circuit conditions:

$$R_1 = \frac{V_{CC} - V_{BQ}}{I_1} = \frac{V_{CC} - V_{BQ}}{11 * I_{BQ}} \tag{0.0.4}$$

$$R_2 = \frac{V_{BQ}}{I_2} = \frac{V_{BQ}}{10 * I_{BQ}} \tag{0.0.5}$$

Choose the nearest standard resistor values that keep V_{BQ} nearest the level determined at step 6(ii) and use the new value of V_{BQ} in subsequent steps.

(d) The new I_{BQ} value is determined by

$$I_{BQ} = \frac{\frac{V_{CC}R_2}{R_1+R_2} - 0.7}{\frac{R_1R_2}{R_1+R_2} + R_E(1+\beta_{DC})} \tag{0.0.6}$$

Thus

$$V_{BQ} = \frac{V_{CC}R_2}{R_1+R_2} - I_{BQ}\frac{R_1R_2}{R_1+R_2} \tag{0.0.7}$$

Consequently, V_{EQ} should be recalculated using: $V_{EQ} = V_{BQ}$ - 0.7 volts and so should I_{EQ}, using:

$$I_{EQ} = \frac{V_{EQ}}{R_E} \tag{0.0.8}$$

and finally I_{CQ}, using: $I_{CQ} \sim I_{EQ}$

7. **Choose R_C:** R_C primarily determines V_{CQ}, the maximum v_c signal swing, and the maximum gain. Usually, the signal swing is maximized, and the small compromise that this places on the gain is accepted. To maximize the signal swing, V_{CQ} is placed at the midpoint between V_{BQ} and V_{CC}. Consequently,

$$R_C = \frac{V_{CC} - V_{BQ}}{2I_{CQ}} \tag{0.0.9}$$

Choose the nearest standard resistor value, and recalculate V_{CQ} and the v_c signal swing.

$$V_{CQ} = V_{CC} - I_{CQ}R_C \tag{0.0.10}$$

This then concludes the DC biasing for the transistor. Next, the AC circuit parameters will be set.

8. **Choose R_3:** This resistor is determined by the gain that is required of the circuit. Generally, the value used for the gain in the calculation is set high by about 10% in an attempt to compensate for unaccounted circuit losses. Any resulting extra gain usually can be tolerated, as opposed to a deficit which cannot. If necessary, the extra gain can be removed by increasing the resistance value of R_3.

   Analysis of the circuit will determine the required value for R_3. Choose the nearest lower standard resistance value in order to maintain the gain. (N.B. For maximum bandwidth R_3 should really be zero.)

9.-12. **Determine (9) the Bandwidth, (10) the Magnitude of the Input Impedance, (11) the Magnitude of the Output Impedance, and (12) the Loaded Output Signal Swing:** These parameters can all be determined by analyses of the circuit under the assumption that all external capacitor values are infinite.

13.-15. **Choose C_1, C_2, and C_E:** These capacitors determine the lower band-limit of the amplifier by introducing poles into its response. Analyses of the circuit will yield equations for each pole frequency. Using equations from example 10.2 in the Sedra and Smith, 7th Ed, textbook, the values for the capacitors in the circuit can be determined.

16. **Iterate Solution:** With the completion of this last step, the amplifier design procedure will have finished its first iteration. If nowhere along the way were one or more of the specifications not met, then the design could be considered to be complete. If, however, one or more of the specifications were not met, then it will be necessary to iterate the solution, with the knowledge that certain parameters of the design must be improved, and with the insight into how best to improve them that consideration of the first solution can give.

Following the example design approach just given, a common-emitter amplifier was designed to meet the following specifications:

Gain:	35 ± 20%
R_L:	4.7 kΩ
Bandwidth:	unimportant
V_{out}:	2 volts peak-to-peak
Distortion:	"low"
I_C:	1.0 mA ± 20%
f_L:	< 200 Hz

The highlights of the design procedure, along with results, without the details of analysis, are presented below.

CE DESIGN CALCULATIONS

1. I_{CQ} = 1.0 mA (spec.)
2. Let V_{CC} = 15 volts (available, and should easily allow 2 volt p-p output swing)
3. Let V_{EQ} = 0.2, V_{CC} = 3 volts (moderate stability)
4. $\therefore R_E$ = 3 kΩ, use R_E = 3.3 kΩ
   $\therefore$ New V_{EQ} = 3.3 volts
5. I_{BQ} = 2.5 to 10 μA (since β = 100 to 400) Use I_{BQ} = 10 μA
6. (a) $I_1 = I_2 = 10{*}I_{BQ}$ = 100 μA (very approx.)
   (b) $\therefore V_{BQ}$ = 4.0 volts
   (c) $\therefore R_1$ = 100 kΩ and R_2 = 40 kΩ. Use 39 kΩ. New I_{BQ} = 9.7 μA
   $\therefore$ New V_{BQ} = 3.94 volts New V_{EQ} = 3.24 volts
   New I_{EQ} = 0.98 mA
   New I_{CQ} = 0.98 mA
7. Let $V_{CQ} = \frac{V_{CC}+V_{BQ}}{2} = \frac{15V+3.94V}{2} = 9.47V$
   $\therefore R_C$ = 5.53 kΩ .
   Use R_C = 5.6 kΩ (to give max. signal swing, but V_{be} will exceed 20 mVpp causing distortion before either cut-off or saturation occur; see (step 12)

8. R3: Following the same steps as Sedra and Smith 7th Edition part 10.3.2, Figures 10.19

$$|A_M| = |\frac{V_o}{V_S}| = g_m(r_o||R_C||R_L) * \frac{R_B||(r_x + r_\pi)}{R_S + R_B||(r_X + r_\pi)} * \frac{r_\pi}{r_X + r_\pi} \tag{0.0.11}$$

where we take $R_S = R_3$ and include it in the amplifier to limit the gain with

g_m	= 0.04 A/V (measured)
r_o	= 100 kΩ (measured) (actual value is large)
R_B	= 100 kΩ ∥ 39kΩ = 28.1 kΩ
r_x	= 20 Ω (measured) (actual value is small)
r_π	= 2.5 kΩ (measured) (actual value has large range)
A_M + 10%	= 38.5
R_3	= 3.65 kΩ. Use R3 = 3.3 kΩ
New A_M	= 40.9 v/v

9. f_H Not required.
10. Analysis of the input of Figure 10.19 using the values above yields | Z_{in} | = 5.6 kΩ
11. Analysis of the output of Figure 10.19 using the values above yields | Z_{out} | = 5.3 kΩ
12. Setting V_π = 20 mV peak to peak, V_{out} (low distortion) = 2.0 volts
13. Similar to Sedra and Smith 7th Edition's Example 10.2 we have $\omega_L = 2\pi*200 = 400\pi$ rad/sec.

$$C_1 = \frac{1}{0.1\omega_L R_{C1}} = \frac{1}{0.1 * 400\pi * 5600} = 1.42\mu F \rightarrow 2.2\mu F \tag{0.0.12}$$

14.

$$C_2 = \frac{1}{0.1\omega_L R_{C2}} = \frac{1}{0.1 * 400\pi * 10000} = 0.796\mu F \rightarrow 1\mu F \tag{0.0.13}$$

15.

$$C_E = \frac{1}{0.8\omega_L R_E} = \frac{1}{0.1 * 400\pi * 13} = 76.5\mu F \rightarrow 100\mu F \tag{0.0.14}$$

(β_{max} = 400 for W.C. value)

$\therefore f_L < 200$Hz

16. Some increase in R_3 to remove excessive gain may have to be undertaken, say R_3 = 3.9 kOhms