ELEC 3908 – Lab 3: MOSFET Drain Current Modeling

1 Summary

In this experiment I_D versus V_{DS} and I_D versus V_{GS} characteristics are measured for a silicon MOSFET, and are used to determine the parameters necessary for the square law model. The device tested in this experiment is a commercially available n-channel MOSFET switching transistor. The results are compared to theoretically calculated characteristics for a device that was fabricated in the microfab of the Department of Electronics at Carleton University.

2 Theory

A MOSFET, or Metal-Oxide-Semiconductor Field Effect Transistor, is a transconductance device constructed by depositing a layer of insulting dielectric, referred to as the "oxide", on the surface of a doped semiconductor sample, referred to as the "substrate". A conductive layer of aluminum or poly-crystalline Silicon is then deposited on top of the dielectric, forming the "gate". Diffused regions of an opposite type to the substrate are then formed on either side of the gate, called the source and drain. We define the width of the transistor to be the extent of the gate electrode along the line of the diffusion and the length to be the distance between the source and drain under the gate. Figure 1 below shows a typical integrated MOSFET structure.

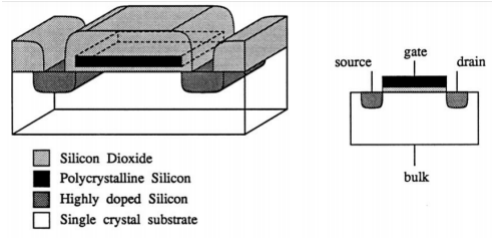


Figure 1: Integrated MOSFET Structure

In simple terms, the MOSFET conducts current between the source and drain only when there is a conductive path between the terminals. This conductive path, often called a "channel", is created by establishing a sufficient potential on the gate to attract a large concentration of minority carriers to the surface of the substrate under the gate. If the substrate is p-type, the minority carriers will be electrons, and a positive gate potential will be required to attract these electrons to the surface. Since the conductive path in this case is composed of minority electrons, the device is called n channel. Similarly, if the substrate is n-type, the minority carriers will be holes, and a negative potential will be required on the gate to attract the holes to the surface. A device whose conductive path is formed from minority holes is called a p-channel device. In the following discussion, we will assume a p-type substrate, hence an n-channel device whose conductive path is formed by electrons.

Although the exact details of operation of the MOSFET are quite involved, and will be covered in detail in the lectures, it is enough for this experiment to note that there are basically three modes of operation for the MOSFET: cutoff, triode and saturation. When the gate to source potential is not sufficient to cause the conductive electron path to form, no current can flow between the source and drain regardless of the value of the drain to source potential, and the device is said to be in the cutoff region. The critical value of gate to source voltage necessary to cause conduction between the source and drain is usually referred to as the threshold voltage, and given the symbol V_T. The condition for cutoff is then $V_{GS} < V_T$.

If the gate to source potential is large enough to cause a conduction channel to form but the drain to

source voltage is small, the current flowing between the source and drain will be a function of both the gate to source and drain to source voltages. This operating region, called the triode region, will persist until the drain to source voltage reaches a particular value called the saturation voltage, usually given the symbol V_{DSsat}. This is in fact the point where the concentration of electrons in the channel at the drain end, which is affected by the drain to source potential, becomes very small.

If the drain to source potential is increased past this point, the current ceases to become a strong function of the drain to source voltage, instead being mostly determined by the gate to source voltage. This device is then said to be in the saturation region of operation. However, there is a weak residual dependence of the current on the drain to source voltage, an effect known as channel length modulation because it arises from an intrusion of the drain depletion region into the channel. As the channel length of a device becomes shorter, the channel length modulation term becomes more prominent because the intrusion of the drain depletion region becomes a greater fraction of the total channel length

The simplest set of equations for the drain current is the "square-law" model, arrived at by considering the amount of charge under the gate as a function of bias, then integrating the expression along the channel to arrive at the final current equation. For this model, the saturation drain source voltage is given by:

$$V_{DSsat} = V_{GS} - V_T \tag{1}$$

Where V_T is the threshold voltage (V). In the triode region, the current expression is:

$$I_D = \mu_n \widehat{C}_{ox} \frac{W}{L} (V_{DS}(V_{GS} - V_T) - \frac{V_{DS}^2}{2}) \tag{2}$$

for $V_{GS} > V_T$ and $V_{DS} < V_{DSsat}$. Where μ_n is the surface mobility of electrons (cm^2/V-sec) and $\widehat{C}_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the oxide capacitance per unit area (F/cm^2).

In the saturation region, the current is only weakly dependent on the drain source voltage, modeled by the inclusion of a $\lambda V_D S$ term, where λ is called the *channel length modulation parameter*. The current in saturation is modelled by:

$$I_D = \mu_n \widehat{C}_{ox} \frac{W}{L} (\frac{(V_{GS} - V_T)^2}{2})(1 - \lambda V_{DS}) \tag{3}$$

for $V_{GS} > V_T$ and $V_{DS} \geq V_{DSsat}$. Where λ is the channel length modulation parameter (1/V)

The threshold voltage, for reasons that will be described in class, is a function of the bias voltage between the substrate and source, an effect called threshold modulation. This dependence is modelled by having the threshold voltage be the sum of a "zero bias" value plus a term depending on the source substrate bias, specifically:

$$V_T = V_{TO} - \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}) \tag{4}$$

where: V_{TO} is the zero bias threshold voltage (V), γ is the threshold modulation coefficient (V), V_{SB} is the source to bulk (substrate) potential (V) and ϕ_F is the bulk potential $\approx$ 0.6V.

Extraction of the parameters in the equations (2) and (3) for I_D above is accomplished as follows. First, a measurement of I_D versus V_{GS} in the triode region (c.f. the latter equation above) with $V_{SB} = 0$, is plotted I_D versus V_{GS} will yield the term $\mu_n \widehat{C}_{ox} V_{DS} \frac{W}{L}$ as the slope of the linear portion, and V_{TO} as the projected intercept on the x axis, assuming that the value of the channel length modulation term, λ, is small. Measuring the same characteristic for non-zero values of substrate voltage will give the threshold modulated V_T as the intercept, and allows the value of γ to be extracted.

3 Experiment

3.1 $I_D - V_D$ Curves

The setup in the lab has been constructed to allow MOSFET I_D characteristics to be measured using ORCAD PSPICE software, as used in the previous two experiments. Both I_D versus V_{DS} at fixed V_{GS} and I_D versus

V_{GS} at fixed V_{DS} characteristics will be investigated. The bulk voltage, V_B, will be adjusted to enable the extraction of the threshold modulation parameter

The first MOSFET measurement will be a typical active region I_D versus V_{DS} at constant V_G plot.

1. Create a new project and save it in a known location on your computer
2. Place a MbreakN MOSFET on the schematic (Found under Place → Pspice Component → Search). Note this "MbreakN" is a default MOSFET with the substrate unconnected – if you use the NMOS from Place → PSpice Component → Discrete the substrate will be connected to the source.

   Place two voltage sources on the schematic and connect one to the the DRAIN and SOURCE terminals of the MOSFET and the other to the GATE and SOURCE terminals respectively. Reference Figure (3) for schematic directions.

   Edit the Mosfet model and add two parameters "VTO=1.5" and "GAMMA=1" – setting the default threshold value and the source-bulk threshold parameter.

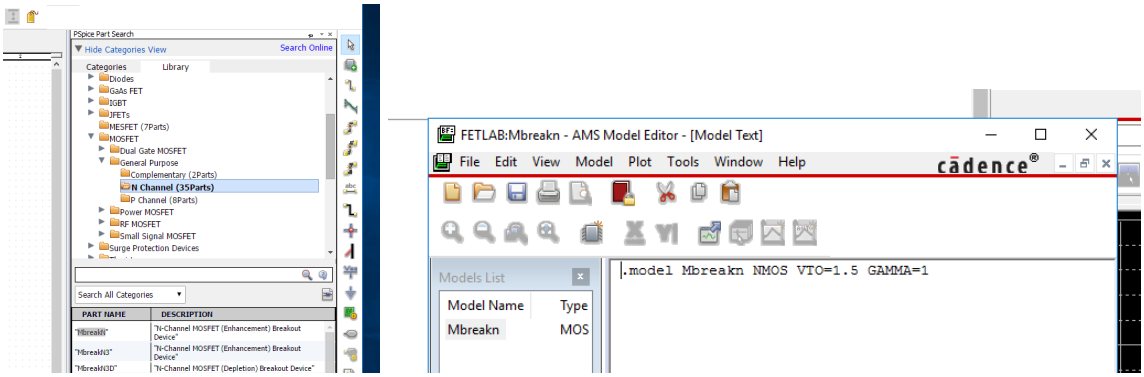
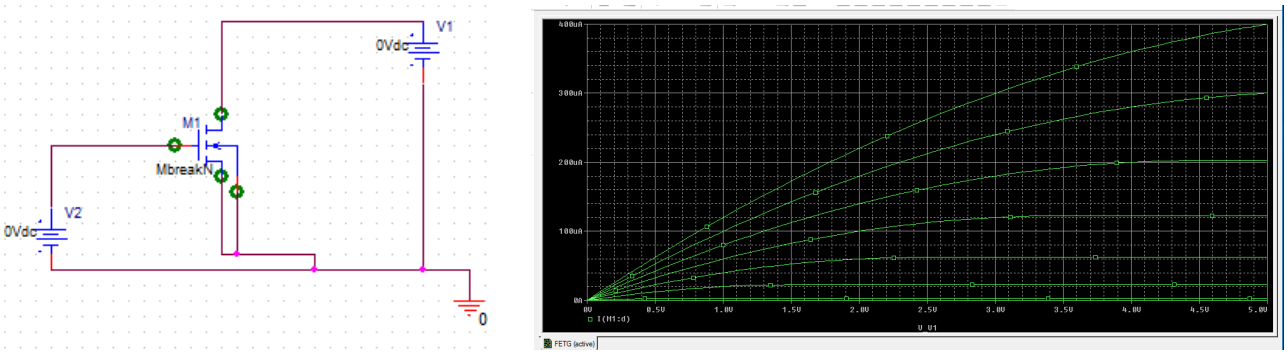


Figure 2: Pspice NMOS Screen Captures showing "Pspice Component Search" and edit window for NMOS component.

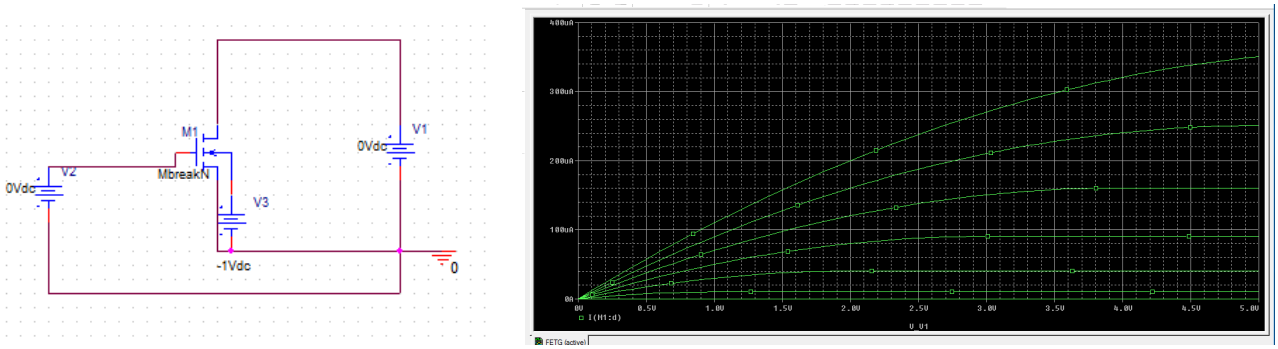
3. Create a Simulation Profile, set the drain voltage V_{DS}, to sweep from 0 to 5V in steps of 0.1V, the gate voltage V_G, to sweep from 1V to 8V in steps of 1V.
4. Run the simulation. Change the x axis to show the voltage of the drain (V_D which is identical to V_{DS} as $V_S = 0$). Add a trace of current over the drain (Ex. I(M1:D)). While on the graph screen, export your data for later use in MATLAB. This can be done by going to FILE → EXPORT → COMMA SEPARATED FILE → Add V(M1:g) to the left table for output variables to export. Make sure you have I(M1:d), V(M1:d), and V(M1:g) in your export. → Select a name for the file → OK (the file saves in the location of your PSPICE project).



a) Circuit b) I-V curve

Figure 3: Schematic of MOSFET Circuit

5. Now leaving all the other parameters the same change the bulk voltage to -1V ($V_{SB} = 1$V) by adding a voltage source on the branch and setting it's voltage to -1V (Watch polarity). Consult Figure (5) for schematic information. While on the graph screen, export your data for later use in MATLAB. This can be done by going to FILE → EXPORT → COMMA SEPARATED FILE → Select a name for the file → OK (the file saves in the location of your PSPICE project).



a) Circuit b) I-V curve

3.2 $I_D - V_G$ Curves

The next step is to perform the measurements necessary to extract the MOSFET parameters in equations (2) and (4) above. To do this the I_D versus V_G at constant V_D characteristics will be measured.

1. Modify the Simulation Profile to set the gate voltage,V_G, to sweep from 1 to 6V in steps of 0.1V, the bulk voltage, V_B, to step by -1V from 0 to -3V and the drain voltage, V_D, to be set to 0.1V
2. Run the simulation, add a trace of I_D (I(M1:d)) and set the X Axis to V_G (V(M1:g)). In your report, determine the slope and intercept of the linear triode region of the I_D versus V_G as You will need the data to extract the MOSFET square law model parameters. Reference Figure (4) for details. While on the graph screen, export your data for later use in MATLAB. This can be done by going to FILE → EXPORT → COMMA SEPARATED FILE → Select a name for the file → OK (the file saves in the location of your PSPICE project).

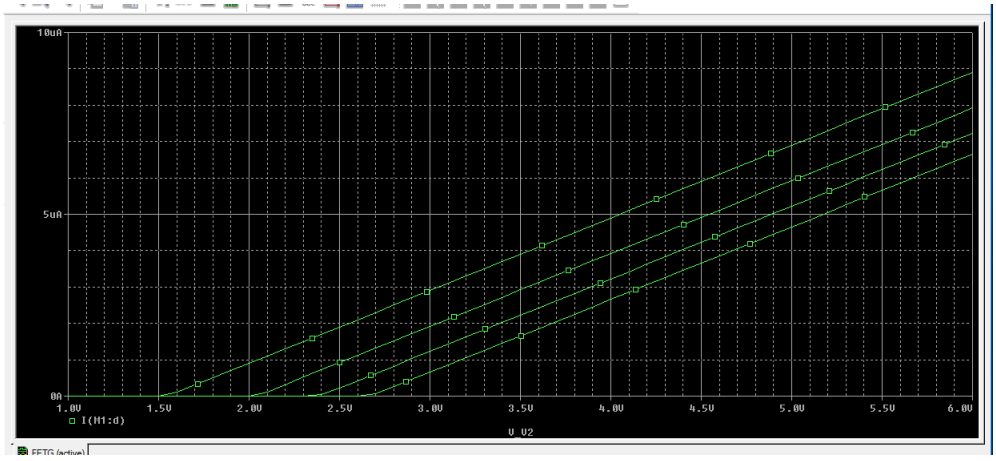


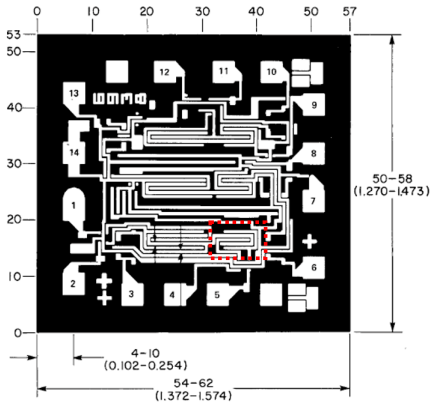
Figure 4: Plot of MOSFET Circuit in part 3 step 2

4 Data Analysis

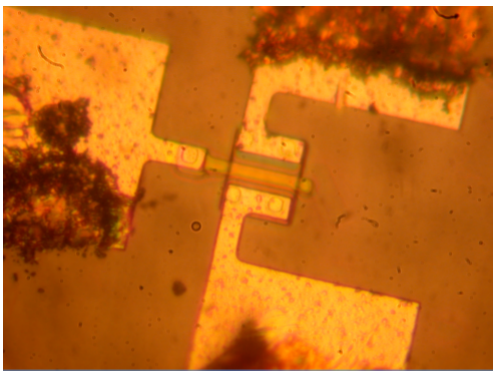
A photomicrograph of the device tested is shown in Figure (5) below. The isolated n-channel MOSFET is shown surrounded by the dashed box. The drawn gate length of this device is about 12 μm. However, lateral diffusion of the source and drain under the gate leads to an effective gate length of about L = 10 μm for the device. The channel width is about W = 350 μm, and the gate oxide thickness is about t_{ox} = 50 nm.

1. From the slope of the curves measured in Sec. 3.2 above at $V_{DS} = 0.1$V extract the value of the channel mobility, μ_n by using equation (2). Use the given values for W and L and calculate $\widehat{C}_{ox}$ from the value of t_{ox}.

2. From the intercept of the linear portion of the curve with the voltage axis in Sec. 3.2, determine the threshold voltage for each value of V_{SB}, and hence find V_{TO} and γ by using equation (4)



(a)



(b)

Figure 5: a) CD4007 IC with measured n-Channel Silicon MOSFET device in box. b) MOSFET Under Microscope

A photomicrograph of an n-MOSFET device fabricated in the Carleton University Microfabrication Facility (CUMFF) is shown in Figure (5). The drawn gate length of this device is 5 μm. However, lateral diffusion of the source and drain under the gate leads to an effective gate length of L = 3.5 μm for the device. The channel width is W = 25 μm, and the gate oxide thickness is t_{ox} 200 nm.

3. Using your values of μ_n and V_{TO} from above , plot the predicted of I_D versus V_{DS} curves for this device at V_G = 3V, 5V and V_{SB} = 0V by applying equation (2) and equation (3).

4.1 MATLAB Analysis

With the data you collected you will now verify it and plot it in MATLAB as well as get a basic introduction to Neural Networks in MATLAB. Make sure the correct version of MATLAB is installed as well as the appropriate toolboxes.

1. Open MATLAB and create a new script. Make sure to save it in a known location. I would place it in the same folder as your FET data.

2. Use the 'Import Data' function from the Home Screen to create a script to read in your data from Sec. 3.1 as a **Table**. Save the script.

3. Write a script like the code below (Consult Figure (6)) (Hint: the code uses an indexing strategy by the name of logical indexing). The function 'FET1B' was the script created by the process above to read the data. Yours will have different name.

```
ReadFET1B

MosD = FETB1;
input = [MosD.V_V1,MosD.VM1g];
output = MosD.IM1d;
output_1E6 = MosD.IM1d*1E6;

inVg1 = MosD.VM1g == 1;
inVg2 = MosD.VM1g == 2;
inVg3 = MosD.VM1g == 3;
inVg4 = MosD.VM1g == 4;
inVg5 = MosD.VM1g == 5;
inVg6 = MosD.VM1g == 6;
inVg7 = MosD.VM1g == 7;
inVg8 = MosD.VM1g == 8;

IdVg1 = MosD.IM1d(inVg1);
IdVg2 = MosD.IM1d(inVg2);
IdVg3 = MosD.IM1d(inVg3);
IdVg4 = MosD.IM1d(inVg4);
IdVg5 = MosD.IM1d(inVg5);
IdVg6 = MosD.IM1d(inVg6);
IdVg7 = MosD.IM1d(inVg7);
IdVg8 = MosD.IM1d(inVg8);

IdVg1_U = MosD.IM1d(inVg1)*1E6;
IdVg2_U = MosD.IM1d(inVg2)*1E6;
IdVg3_U = MosD.IM1d(inVg3)*1E6;
IdVg4_U = MosD.IM1d(inVg4)*1E6;
IdVg5_U = MosD.IM1d(inVg5)*1E6;
IdVg6_U = MosD.IM1d(inVg6)*1E6;
IdVg7_U = MosD.IM1d(inVg7)*1E6;
IdVg8_U = MosD.IM1d(inVg8)*1E6;

Vd = MosD.V_V1(inVg1);

figure
plot(Vd,IdVg1); hold on
plot(Vd,IdVg2)
plot(Vd,IdVg3)
plot(Vd,IdVg4)
plot(Vd,IdVg5)
plot(Vd,IdVg6)
plot(Vd,IdVg7)
plot(Vd,IdVg8)

xlabel('V_d')
ylabel('I_d')
legend('V_g = 1','V_g = 2','V_g = 3','V_g = 4','V_g = 5','V_g = 6')

figure
plot(Vd,IdVg1_U); hold on
plot(Vd,IdVg2_U)
plot(Vd,IdVg3_U)
plot(Vd,IdVg4_U)
plot(Vd,IdVg5_U)
plot(Vd,IdVg6_U)
plot(Vd,IdVg7_U)
plot(Vd,IdVg8_U)

xlabel('V_d')
ylabel('I_d')
legend('V_g = 1','V_g = 2','V_g = 3','V_g = 4',...
    'V_g = 5','V_g = 6','V_g = 7','V_g = 8')
```

Figure 6: MATLAB code for logical indexing. Note: scaled currents defined for NN building.

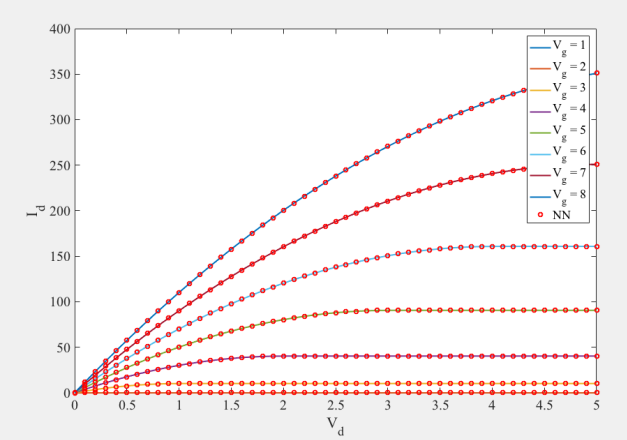


Figure 7: MATLAB Graph for Part 1

4. **Capture a copy the MATLAB plot for your write-up.**
5. Repeat the steps above for all the other .csv files created, this may include changing the code above slightly depending on the .csv.

4.1.1 MATLAB Neural Net Analysis

1. Create a new script and save it appropriately.
2. Run the code to import the first .csv file that was saved to your computer as a Table. The code divides the .csv file columns into 2 input voltages and one output current, this is what your going to use to train your network. Define and input and output vector as in Fig. 8.

```
Input = [MosD.V_V1,MosD.VM1g];
Output = MosD.IM1d;

% Build NN

outputnn = net(input.');

plot(input(:,1),outputnn,'ro')
```

Figure 8: Code for step above: (MosData.csv is the name of the .csv file in this example)

3. Build the NN[1] using the Command Window type "nnstart", select Fitting App and click "Next" twice. In the select data page select the Input under Inputs and Output under Outputs accordingly. Also make sure to select Matrix Rows to properly divide the samples for the training. Click "Next".
4. Keep the neurons default and click next, you will go back and modify them later.
5. In the training algorithms, change the training algorithm to Bayesian Regularization as it is better suited for small data sets like this one. Next click "Train and wait for the algorithm to finish training". Then click "Next" twice.
6. Click, "Simple Script" and save the script to your computer. Next run the Simple Script, this should create your neural net in your work-space.
7. In the "Command Window" type some test numbers and record your results. If your result's are way off go back to the neural net GUI and increase the number of neurons in your neural network (watch out too high of a number may freeze or even crash your computer) and repeat the process. In your report talk about the difference of the neural net numbers and the actual exported values.

[1] I had issues building a NN using the raw data from Pspice this is due (I think) to the very small currents produced for $V_g < V_{TO}$). In the code above I scaled all the currents to microamps and found I could build nice NN using this data with 50 neurons. See Fig. 7

8. Using the measured numerical data (from Part 2) and the extracted parameters from above, plot the theoretical prediction of the square law model on the same axis as the measured data. Note that this will involve finding the saturation drain source voltage in each case then applying equation (2) and equation (3) using experimental values for the parameters (in all cases assume that channel modulation can be ignored). The final plots should compare the plots/parameters from your PSPICE analysis and the neural net models.

5 References

Streetman, B. G., Solid State Electronic Devices, ed., Sections 8.3.5 - 8.3.9.

Puifrey, D. and Tarr, N. G., Introduction to Microelectronic Devices, pp. 200 - 206, 216.

Muller, R. S. and Kamins, T. I., Device Electronics for Integrated Circuits, pp. 422 – 442.

Tsividis, Y. P., Operation and Modeling of the MOS Transistor, pp. 75 - 98, 102 – 117.