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Computer Sciences Division Solution Sheet 1 Chapter 1 Operating System 2025 Dr. Hatem Moharram

O 1- Data Registers O 2-	sters is used b	y operating-s	ystem routines to cor	itrol the ex	ecution of programs?	
o i Bata Registers	<u> </u>	O3- Add	dress Registers O4	- 2 and 3	O 5- All of the previous	
2 is One of the In	terrupt types	that a proces	sor can handle is		_	
O 1- cache memory	Overflow	<u>Arithmetic</u>	O 3- OS interrupts	O 4- fl	ash interrupt	
3. Which of the following regis	sters is used b	y operating-s	ystem routines to cor	ntrol the ex	ecution of programs?	
O1- Data Registers O2- Po			•			
4. Which of the following regis						
	- PC		dress Registers		O 4- All of the previous	
5. Which of the following registers is used by operating-system routines to control the execution of programs?						
O 1- Data Registers O 2-	- Address Re	gisters	0 <u>3- PSW</u>		O 4- All of the previous	
6. The Instruction Register (IR)	) belongs to				•	
O 1-control registers.	O 2-Dat	ta registers.	O 3-User-visible re	egisters.	O 4-none of the previous	
7. The Instruction Register (IR)	) belongs to	-				
O1-Status and cont	rol O2-Dat	ta registers.	O 3-User-visible re	egisters.	O 4-none of the previous	
<u>registers.</u>						
8. One of the Interrupt types the	nat a processo	r can handle	is			
O1- Interrupt Timer C	2- Arithmet	tic Overflow	O 3- I/O interrupts	O 4- H	lardware failure interrupt	
O All the previous	None of the	e previous				
9. One of the Interrupt types the	nat a processo	r can handle	is			
O 1- logic interrupts	02- program	failure	O 3- signal interrup	ts   O4- p	age interrupt	
O All the previous	None of the	e previous				
10. In the Memory Hierarchy		1				
			• • • • • • • • • • • • • • • • • •		ter capacity, slower	
bit.			' NIT	acces	s speed.	
		cost per				
O4-All the previous		•	of the previous	0	•	
O 4-All the previous  11. In the Memory Hierarchy	llan aast man	O 5-None o	of the previous	0		
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal	ller cost per	O 5-None o	of the previous  r capacity, greater	O 3-Grea	ter capacity, faster access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit.	ller cost per	O 5-None of O 2-Greater cost per	of the previous  r capacity, greater	0	ter capacity, faster access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous	ller cost per	O 5-None of O 2-Greater cost per	of the previous  r capacity, greater bit.	O 3-Grea	ter capacity, faster access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy		O 5-None of O 2-Greater cost per O 5-None of	of the previous  r capacity, greater bit.	O 3-Grea	ter capacity, faster access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous		O 5-None of O 2-Greater cost per O 5-None of	r capacity, greater bit.  of the previous  r capacity, smaller	O 3-Grea	ter capacity, faster access ter capacity, slower access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, great		O 5-None of O 2-Greater cost per O 2-Greater cost per C 2-Greater cost p	r capacity, greater bit.  of the previous  r capacity, smaller	O 3-Grea	ter capacity, faster access ter capacity, slower access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, grea bit.	ter cost per	O 2-Greater cost per O 2-Greater cost per O 5-None o	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous	O 3-Grea speed	ter capacity, faster access ter capacity, slower access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, grea bit. O 4-All the previous	ter cost per	O 5-None of O 2-Greater cost per O 5-None of the data to be	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Grea speed	ter capacity, faster access ter capacity, slower access	
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O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, small bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, great bit. O 4-All the previous  13. Which of the following regist O 1- MAR  14. The Program Counter (PC) by O 1-Status and continuous	ter cost per sters contains O 2- I/O pelongs to:	O 5-None of O 2-Greater cost per O 5-None of the data to be	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Great speed O 3-Great speed Ty? 3- MBR	ter capacity, faster access ter capacity, slower access	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, small bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, great bit. O 4-All the previous  13. Which of the following registion of the Program Counter (PC) by the option of the Program Counter (PC) by the option of the previous of the Program Counter (PC) by the option of the Program Counter (PC) by the Op	ter cost per  sters contains O 2- I/O pelongs to: rol O 2-Dat	O 5-None of Cost per O 5-None	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Great speed O 3-Great speed Ty? 3- MBR	ter capacity, faster access ter capacity, slower access .	
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O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, small bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, great bit. O 4-All the previous  13. Which of the following regist O 1- MAR  14. The Program Counter (PC) by O 1-Status and contained and contained are gisters.  15. The Program Counter (PC) by O 1-control registers.	ter cost per  sters contains O 2- I/O pelongs to: pelongs to: O 2-Dat	O 5-None of Cost per O 5-None	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Grea speed O 3-Grea speed ry? 3- MBR	ter capacity, faster access ter capacity, slower access .	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, grea bit. O 4-All the previous  13. Which of the following registion of the following registers.  15. The Program Counter (PC) by O 1-control registers.  16. One of the instruction types	ter cost per  sters contains O 2- I/O pelongs to: O 2-Dat pelongs to: O 2-Dat that a process	O 5-None of Cost per O 5-None of Cost per O 5-None of the data to be OAR ta registers.	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Great speed O 3-Great speed Ty? 3-MBR egisters.	ter capacity, faster access ter capacity, slower access O4-I/OBR O4-None of the previous  O4-none of the previous	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smalbit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, greabit. O 4-All the previous  13. Which of the following registors O 1- MAR  14. The Program Counter (PC) books O 1-Status and contregisters.  15. The Program Counter (PC) books O 1-control registers.  16. One of the instruction types O 1- memory-buffer	ter cost per  sters contains O 2- I/O pelongs to: pelongs to: O 2-Dat	O 5-None of Cost per O 5-None of Cost per O 5-None of the data to be OAR ta registers.	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Great speed O 3-Great speed Ty? 3-MBR egisters.	ter capacity, faster access ter capacity, slower access O4- I/OBR O4-None of the previous	
O 4-All the previous  11. In the Memory Hierarchy O 1-Faster access time, smal bit. O 4-All the previous  12. In the Memory Hierarchy O 1-Faster access time, grea bit. O 4-All the previous  13. Which of the following registion of the following registers.  15. The Program Counter (PC) by O 1-control registers.  16. One of the instruction types	ter cost per  sters contains O 2- I/O pelongs to: O 2-Dat pelongs to: O 2-Dat that a process	O 5-None of Cost per O 5-None of Cost per O 5-None of the data to be OAR ta registers.	r capacity, greater bit.  of the previous  r capacity, smaller bit.  of the previous  r capacity, smaller bit.  of the previous  e written into memor	O 3-Great speed O 3-Great speed Ty? 3-MBR egisters. eegisters.	ter capacity, faster access ter capacity, slower access O4-I/OBR O4-None of the previous  O4-none of the previous	

O 1- Part of the Hard Disk		O 3- Is a hardware				
		O 4-non	O <u>4-none of the previous</u>			
19.	With the Direct Memory	Access (DMA) approach:				
O 1- I/O exchanges occur directly with memory				O 3- The processor is free to do other things		
O 2- The processor is only involved at the beginning an the I/O		nd end of	O <u>4- All the prev</u>	<u>vious</u>		
20.	is the princ	cipal internal memory system of	f the comp	outer.		
C	1- the hard disk	O 2- the main memory		O 3- OS	O 4- All the previous	
		ne right statements and × in	front of	the wrong statem	ents <u>and correct them.</u>	
2.		odes are bits set by the proce n but not altered. True	essor har	dware as a result	of operations and can be	
3.	Interrupts worsen pro	ocessor utilization. False imp	orove			
	The disk cache is a desimprove performance.	vice for staging the movement. False cache	nt of data	a between memory	y and processor registers to	
5.	Even with multiprogra	amming, a processor could b	be idle mo	ost of the time. tru	1e	
6.	in Direct Memory Acc	cess (DMA), input/output op	erations	is the processor's	responsibility. false	
7.	Data access from regis	sters is slower than that from			contrary	
8.	The locality of referen	ice principle states that "me	mory ref	erences by the pro		
9.	the contrary	the contents of the Main Me	-		-	
10.		on of the Hard Disk . False of				
11.		rrupt Handler for all types (				
12.	In the Memory Hierar	rchy, the memory with slowe	er access	time has greater o	cost per bit. False faster	
13.	Cache Memory is visib	ble to the operating system.	False inv	isible		
14.		the contents of the Main M				

15. Data access from the Hard Disk is slower than that from Cache memory. True			
16. Disk Cache is a portion of the Hard Disk .False of the main memory			
17. Disk writes in the Disk Cache are clustered. True			
18. Each type of Interrupts has its own Interrupt Handler. True			
19. In the Memory Hierarchy, the memory with faster access time has greater cost per bit. True			

Q(3): Illustrate the differences between the cache and the disk cache.

cache	disk cache
Faster	Slower
smaller capacity	Greater capacity
greater cost per bit	smaller cost per bit
A portion of main memory used as a buffer to	a device for staging the movement of data between
temporarily hold data that are to be read out to disk.	memory and processor registers

## $\mathbf{Q}(4)$ : State the different Classes of Interrupts.

- 1- Program Interrupts
  2- Timer Interrupt

- 3- I/O Interrupts4- Hardware failure Interrupts