Cairo University
Faculty of science
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Computer Sciences Division
Solution Sheet 1 Chapter 1
Operating System 2025
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1. **Which of the following registers is used by operating-system routines to control the execution of programs?**

O 1- Data Registers	O **2- PC**	O 3- Address Registers	O 4- 2 and 3	O 5- All of the previous

2. **……. is One of the Interrupt types that a processor can handle is**

O 1- cache memory	O **2- Arithmetic Overflow**	O 3- OS interrupts	O 4- flash interrupt

3. **Which of the following registers is used by operating-system routines to control the execution of programs?**

O 1- Data Registers	O 2- PC	O 3- Address Registers	O 4- PSW	O **5- 2 and 4**	O 6- All of the previous

4. **Which of the following registers is used by operating-system routines to control the execution of programs?**

O 1- Data Registers	O **2- PC**	O 3- Address Registers	O 4- All of the previous

5. **Which of the following registers is used by operating-system routines to control the execution of programs?**

O 1- Data Registers	O 2- Address Registers	O **3- PSW**	O 4- All of the previous

6. **The Instruction Register (IR) belongs to**

O 1-control registers.	O 2-Data registers.	O 3-User-visible registers.	O **4-none of the previous**

7. **The Instruction Register (IR) belongs to**

O **1-Status and control registers.**	O 2-Data registers.	O 3-User-visible registers.	O 4-none of the previous

8. **One of the Interrupt types that a processor can handle is**

O 1- Interrupt Timer	O 2- Arithmetic Overflow	O 3- I/O interrupts	O 4- Hardware failure interrupt
O **All the previous**	O None of the previous		

9. **One of the Interrupt types that a processor can handle is**

O 1- logic interrupts	O 2- program failure	O 3- signal interrupts	O 4- page interrupt
O All the previous	O **None of the previous**		

10. **In the Memory Hierarchy**

O 1-Faster access time, smaller cost per bit.	O 2-Greater capacity, greater cost per bit.	O **3-Greater capacity, slower access speed.**
O 4-All the previous	O 5-None of the previous	O

11. **In the Memory Hierarchy**

O 1-Faster access time, smaller cost per bit.	O 2-Greater capacity, greater cost per bit.	O 3-Greater capacity, faster access speed.
O 4-All the previous	O **5-None of the previous**	

12. **In the Memory Hierarchy**

O 1-Faster access time, greater cost per bit.	O 2-Greater capacity, smaller cost per bit.	O 3-Greater capacity, slower access speed.
O **4-All the previous**	O 5-None of the previous	

13. **Which of the following registers contains the data to be written into memory?**

O 1- MAR	O 2- I/OAR	O **3- MBR**	O 4- I/OBR

14. **The Program Counter (PC) belongs to:**

O **1-Status and control registers.**	O 2-Data registers.	O 3-User-visible registers.	O 4-None of the previous

15. **The Program Counter (PC) belongs to:**

O 1-control registers.	O 2-Data registers.	O 3-User-visible registers.	O **4-none of the previous**

16. **One of the instruction types that a processor can execute is**

O 1- memory-buffer	O **2- Processor-memory**	O 3- Register-Processor	O 4- All the previous

17. **The Interrupt Handler is**

O 1- Part of the Hard Disk	O **3- One of OS programs**
O 2- Part of the Main Memory	O 4- One of interrupt that a processor can handle

18. **The Interrupt Handler is**

O 1- Part of the Hard Disk	O 3- Is a hardware
O 2- Part of the Main Memory	O **4-none of the previous**

19. **With the Direct Memory Access (DMA) approach:**

O 1- I/O exchanges occur directly with memory	O 3- The processor is free to do other things
O 2- The processor is only involved at the beginning and end of the I/O	O **4- All the previous**

20. **…….. is the principal internal memory system of the computer.**

O 1- the hard disk	O **2- the main memory**	O 3- OS	O 4- All the previous

Q(2): Put √ in front of the right statements and × in front of the wrong statements and correct them.

1. **Disk writes in the Disk Cache are clustered. True**
2. **In PSW, Condition Codes are bits set by the processor hardware as a result of operations and can be accessed by a program but not altered. True**
3. **Interrupts worsen processor utilization. False improve**
4. **The disk cache is a device for staging the movement of data between memory and processor registers to improve performance. False cache**
5. **Even with multiprogramming, a processor could be idle most of the time. true**
6. **in Direct Memory Access (DMA), input/output operations is the processor's responsibility. false**
7. **Data access from registers is slower than that from cache memory. False the contrary**
8. **The locality of reference principle states that "memory references by the processor tend to cluster". True**
9. **The Processor checks the contents of the Main Memory first then the contents of Cache Memory . False the contrary**
10. **Disk Cache is a portion of the Hard Disk . False of the main memory**
11. **There is only one Interrupt Handler for all types of interrupts. False one for each type**
12. **In the Memory Hierarchy, the memory with slower access time has greater cost per bit. False faster**
13. **Cache Memory is visible to the operating system. False invisible**
14. **The Processor checks the contents of the Main Memory first then the contents of Cache Memory. False the contrary**

15. Data access from the Hard Disk is slower than that from Cache memory. True

16. Disk Cache is a portion of the Hard Disk .False of the main memory

17. Disk writes in the Disk Cache are clustered. True

18. Each type of Interrupts has its own Interrupt Handler. True

19. In the Memory Hierarchy, the memory with faster access time has greater cost per bit. True

Q(3): Illustrate the differences between the cache and the disk cache.

cache	disk cache
Faster	Slower
smaller capacity	Greater capacity
greater cost per bit	smaller cost per bit
A portion of main memory used as a buffer to temporarily hold data that are to be read out to disk.	a device for staging the movement of data between memory and processor registers

Q(4): State the different Classes of Interrupts.

1- **Program Interrupts**
2- **Timer Interrupt**
3- **I/O Interrupts**
4- **Hardware failure Interrupts**