Spartan6 - DSP48A1

By

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Contents

Reg & Mux Pair Code

reg_mux_pair.v

```
module REG_MUX (IN, CLK, RST, EN, OUT);

parameter STAGE = 1;
parameter WIDTH = 18;
parameter RSTTYPE = "SYNC"; //ASYNC

input CLK, RST, EN;
input [WIDTH - 1 : 0] IN;
output reg [WIDTH - 1 : 0] OUT;

generate
    if (STAGE == 1 && RSTTYPE == "ASYNC") begin
        always @(posedge CLK or posedge RST) begin
            if (RST)
                OUT <= 0;

            else if (EN)
                OUT <= IN;
        end
    end

    else if (STAGE == 1 && RSTTYPE == "SYNC") begin
        always @(posedge CLK) begin
            if (RST)
                OUT <= 0;

            else if (EN)
                OUT <= IN;
        end
    end

    else if (~STAGE) begin
        always @(*) begin
            OUT = IN;
        end
    end

endgenerate
endmodule
```

RTL Code

DSP.v

```
//---------------------------------------------------- DSP48A1 ----------------------------------------------------//

module DSP_48A1 (A,B,C,D,CLK,CARRYIN,RSTCARRYIN,RSTOPMODE,RSTA,RSTB,RSTC,RSTD,RSTM,RSTP,
                 CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE, PCIN, OPMODE, BCIN,
                 BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);

parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;

parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;

parameter CARRYINSEL = "OPMODE5";  //CARRYIN
parameter B_INPUT = "DIRECT";  //CASCADE
parameter RSTTYPE = "SYNC"; //ASYNC

input CLK, CARRYIN;
input RSTCARRYIN, RSTOPMODE, RSTA, RSTB, RSTC, RSTD, RSTM, RSTP;
input CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
input [17:0] A, B, D;
input [47:0] C, PCIN;
input [7:0] OPMODE;
input [17:0] BCIN;

output CARRYOUT , CARRYOUTF;
output [17:0] BCOUT;
output [35:0] M;
output [47:0] PCOUT , P;

//-------------------------------------------------------------------------------------------------------------//

wire [7:0] opmode_r;
wire [17:0] a0_out , b0_out , d_out , b_in , pre_adder_out , bypass_b;
wire [47:0] c_out;

REG_MUX #(.STAGE(OPMODEREG) , .WIDTH(8) , .RSTTYPE(RSTTYPE)) OPMODE_REG (OPMODE , CLK , RSTOPMODE , CEOPMODE , opmode_r);
REG_MUX #(.STAGE(A0REG) , .WIDTH(18) , .RSTTYPE(RSTTYPE)) A0_REG (A , CLK , RSTA , CEA , a0_out);
REG_MUX #(.STAGE(B0REG) , .WIDTH(18) , .RSTTYPE(RSTTYPE)) B0_REG (b_in , CLK , RSTB , CEB , b0_out);
REG_MUX #(.STAGE(CREG) , .WIDTH(48) , .RSTTYPE(RSTTYPE)) C_REG (C , CLK , RSTC , CEC , c_out);
REG_MUX #(.STAGE(DREG) , .WIDTH(18) , .RSTTYPE(RSTTYPE)) D_REG (D , CLK , RSTD , CED , d_out);

assign b_in = (B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? BCIN : 18'b0;
assign pre_adder_out = (opmode_r[6])? (d_out - b0_out) : (d_out + b0_out);
assign bypass_b = (opmode_r[4])? pre_adder_out : b0_out;

//-------------------------------------------------------------------------------------------------------------//

wire [17:0] a1_out , b1_out;
wire [35:0] multiplier_out , m_out;

reg [47:0] x_out , z_out;

REG_MUX #(.STAGE(A1REG) , .WIDTH(18) , .RSTTYPE(RSTTYPE)) A1_REG (a0_out , CLK , RSTA , CEA , a1_out);
REG_MUX #(.STAGE(B1REG) , .WIDTH(18) , .RSTTYPE(RSTTYPE)) B1_REG (bypass_b , CLK , RSTB , CEB , b1_out);
REG_MUX #(.STAGE(MREG) , .WIDTH(36) , .RSTTYPE(RSTTYPE)) M_REG (multiplier_out , CLK , RSTM , CEM , m_out);

assign multiplier_out = a1_out * b1_out;

```

```
66  //------------------ X_MUX & Z_MUX ------------------//
67  always @(*) begin
68      case (opmode_r[1:0])
69          0 : x_out = 0;
70          1 : x_out = { {12{m_out[35]}} , m_out};
71          2 : x_out = P;
72          3 : x_out = {d_out[11:0] , a1_out , b1_out};
73      endcase
74
75      case (opmode_r[3:2])
76          0 : z_out = 0;
77          1 : z_out = PCIN;
78          2 : z_out = P;
79          3 : z_out = c_out;
80      endcase
81  end
82
83  //-----------------------------------------------------------------------------------------------//
84
85  wire carry_cascade_out , COUT , CIN;
86  wire [47:0] post_adder_out;
87
88  REG_MUX #(.STAGE(PREG) , .WIDTH(48) , .RSTTYPE(RSTTYPE)) P_REG (post_adder_out , CLK , RSTP , CEP , P);
89  REG_MUX #(.STAGE(CARRYINREG), .WIDTH(1), .RSTTYPE(RSTTYPE)) CYI_REG (carry_cascade_out, CLK, RSTCARRYIN, CECARRYIN, CIN);
90  REG_MUX #(.STAGE(CARRYOUTREG) , .WIDTH(1) , .RSTTYPE(RSTTYPE)) CYO_REG (COUT , CLK , RSTCARRYIN , CECARRYIN , CARRYOUT);
91
92  assign carry_cascade_out = (CARRYINSEL == "OPMODE5")? opmode_r[5] : (B_INPUT == "CARRYIN")? CARRYIN : 1'b0;
93  assign {COUT , post_adder_out} = (opmode_r[7])? (z_out - (x_out + CIN)) : (z_out + x_out + CIN);
94  assign CARRYOUTF = CARRYOUT;
95  assign PCOUT = P;
96  assign BCOUT = b1_out;
97  assign M = ~(~m_out); //buf( M , m_out);
98
99  endmodule
```

Testbench Code

- This test bench is:
  - A mix between directed and randomized test benches
  - Self-checking test bench

- **Note:**
  The explanation of the testbench code and the reasons for each input pattern in each test case is in the "**Result of the Testbench**" section (Page 12)

```
//------------------------ DSP Testbench ------------------------------------//

module TB_DSP ();

parameter A0REG = 1;//
parameter A1REG = 1;
parameter B0REG = 1;//
parameter B1REG = 1;
```

```
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;

parameter CARRYINSEL = "OPMODE5";  //CARRYIN
parameter B_INPUT = "DIRECT";  //CASCADE
parameter RSTTYPE = "SYNC"; //ASYNC

reg clk, CARRYIN;
reg RSTCARRYIN, RSTOPMODE, RSTA, RSTB, RSTC, RSTD, RSTM, RSTP;
reg CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
reg [17:0] A, B, D, PRE_EXP;
reg [47:0] C, PCIN;
reg [7:0] OPMODE;
reg [17:0] BCIN;

wire CARRYOUT , CARRYOUTF;
wire [17:0] BCOUT;
wire [35:0] M;
wire [47:0] PCOUT , P;

reg [47:0] EXPECTED;

DSP48A1
#(A0REG,A1REG,B0REG,B1REG,CREG,DREG,MREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG,CA
RRYINSEL,B_INPUT,RSTTYPE)
        DUT
(A,B,C,D,clk,CARRYIN,RSTCARRYIN,RSTOPMODE,RSTA,RSTB,RSTC,RSTD,RSTM,RSTP,
            CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE, PCIN, OPMODE,
BCIN,
            BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);

initial begin
    clk = 0;
    forever
        #10 clk = ~clk;
end

initial begin
    $display("\n----------------------------------------> Testing Reset <-----
-----------------------------------\n");
```

```
    RSTOPMODE= 1; RSTA= 1; RSTB= 1; RSTC= 1; RSTD= 1; RSTM= 1; RSTP= 1; RSTM= 1;
RSTCARRYIN= 1;

    repeat (10) begin
        CEA=$random; CEB=$random; CEM=$random;
        CEP=$random; CEC=$random; CED=$random;
        CECARRYIN=$random; CEOPMODE=$random; CARRYIN=$random;
        OPMODE=$random; PCIN=$random; BCIN=$random;
        A=$random; B=$random; C=$random; D=$random;

        EXPECTED = 0;

        @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //---------------------------------enable-----------------------------------------
    $display("\n----------------------------------------> Testing Enable <----
--------------------------------------\n");

    RSTOPMODE= 0; RSTA= 0; RSTB= 0; RSTC= 0; RSTD= 0; RSTM= 0; RSTP= 0; RSTM= 0;
RSTCARRYIN= 0;
    CEA= 0; CEB= 0; CEM= 0; CEP= 0; CEC= 0; CED= 0; CECARRYIN= 0; CEOPMODE= 0;

    repeat (10) begin
        CARRYIN=$random;
        OPMODE=$random; PCIN=$random; BCIN=$random;
        A=$random; B=5; C=$random; D=$random;

        EXPECTED = 0;

        @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //-----------------------------------------bypass B-----------------------------
     $display("\n----------------------------------------> Testing bypass B <-
-----------------------------------------\n");
```

```
    CEA= 1; CEB= 1; CEM= 1; CEP= 1; CEC= 1; CED= 1; CECARRYIN= 1; CEOPMODE= 1;

 // OPMODE = 8'b 7_6_5_4_32_10;
    OPMODE = 8'b 0_0_0_0_11_01;

    A = 1; C = 0;

    repeat (10) begin

        B = $urandom_range(0,15);

        PCIN=$random; BCIN=$random; D=$random;

        EXPECTED = B;

        repeat (4) @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //-------------------------------------operation---------------------------------
    $display("\n------------------------------------------> Testing arithmetic
operations <------------------------------------------\n");

    RSTOPMODE= 1; RSTA= 1; RSTB= 1; RSTC= 1; RSTD= 1; RSTM= 1; RSTP= 1; RSTM= 1;
RSTCARRYIN= 1;

    repeat (4) @(negedge clk);

    RSTOPMODE= 0; RSTA= 0; RSTB= 0; RSTC= 0; RSTD= 0; RSTM= 0; RSTP= 0; RSTM= 0;
RSTCARRYIN= 0;


    OPMODE[4:0] = 5'b 1_11_01;

    repeat (100) begin

        D = $urandom_range(7);
        B = $urandom_range(7);
        A = $urandom_range(7);
        C = $urandom_range(7);
        OPMODE[7:5] = $random;
```

```
        case (OPMODE[7:6])
            2'b00 : begin PRE_EXP = D+B; EXPECTED = C + (A*PRE_EXP + OPMODE[5]);
end
            2'b01 : begin PRE_EXP = D-B; EXPECTED = C + (A*PRE_EXP + OPMODE[5]);
end
            2'b10 : begin PRE_EXP = D+B; EXPECTED = C - (A*PRE_EXP + OPMODE[5]);
end
            2'b11 : begin PRE_EXP = D-B; EXPECTED = C - (A*PRE_EXP + OPMODE[5]);
end
        endcase

        repeat (4) @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //-----------------------------------accumlator x ----------------------------
    $display("\n----------------------------------------> Testing Accumlator
through X <----------------------------------------\n");

    RSTOPMODE= 1; RSTA= 1; RSTB= 1; RSTC= 1; RSTD= 1; RSTM= 1; RSTP= 1; RSTM= 1;
RSTCARRYIN= 1;
    @(negedge clk);
    RSTOPMODE= 0; RSTA= 0; RSTB= 0; RSTC= 0; RSTD= 0; RSTM= 0; RSTP= 0; RSTM= 0;
RSTCARRYIN= 0;

    OPMODE = 8'b 0_0_0_0_11_10;
    C = 2;
    EXPECTED = 2;

    repeat (2) @(negedge clk);

    repeat (100) begin

        D = $random;
        B = $random;
        A = $random;

        EXPECTED = EXPECTED + 2;

        @(negedge clk);
```

```
        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //----------------------------accumlator z-------------------------------------
    $display("\n-----------------------------------------> Testing Accumlator
through Z <-----------------------------------------\n");

    RSTOPMODE= 1; RSTA= 1; RSTB= 1; RSTC= 1; RSTD= 1; RSTM= 1; RSTP= 1; RSTM= 1;
RSTCARRYIN= 1;
    @(negedge clk);
    RSTOPMODE= 0; RSTA= 0; RSTB= 0; RSTC= 0; RSTD= 0; RSTM= 0; RSTP= 0; RSTM= 0;
RSTCARRYIN= 0;

    OPMODE = 8'b 0_0_0_0_10_01;
    B = 2;
    A = 1;

    EXPECTED = 2;

    repeat (4) @(negedge clk);

    repeat (100) begin
        D = $random;
        C = $random;

        EXPECTED = EXPECTED + 2;

        @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
 //----------------------------mux 0-------------------------------------------
    $display("\n-----------------------------------------> Testing Placing all
zeros <-----------------------------------------\n");

    OPMODE[7:0] = 8'b 0_0_0_0_00_00;
    repeat (10) begin

        D = $random;
        B = $random;
```

```
        A = $random;
        C = $random;

        EXPECTED = 0;
        repeat (2) @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end
//---------------------------------conc & pcin-----------------------------------
    $display("\n----------------------------------------> Testing
Concatenation & PCIN <----------------------------------------\n");

    OPMODE[7:0] = 8'b 0_0_0_0_01_11;
    repeat (100) begin
        PCIN = $random;
        D = $random;
        B = $random;
        A = $random;
        C = $random;

        EXPECTED = PCIN + {D[11:0] , A , B};
        repeat (4) @(negedge clk);

        if (P != EXPECTED) begin
            $display("ERROR!! Incorrect Output :(");
            $stop;
        end
    end

    //If the simulation reached this line then no errors were found
    $display("\n--->  NO ERRORS, All Outputs are Correct :)  <---\n");
    $stop;
end

initial begin
    $monitor("CLK= %b ,D= %d ,B= %d ,A= %d ,C= %d ,OPMODE= %b_%b_%b ,BCOUT= %d
,M= %d ,CARRYOUT= %b ,P= %d ,EXPECTED = %d",
            clk , D, B, A, C, OPMODE[7:6], OPMODE[5], OPMODE[4:0], BCOUT, M,
CARRYOUT, P, EXPECTED);
end

endmodule
```

DO File

2.do

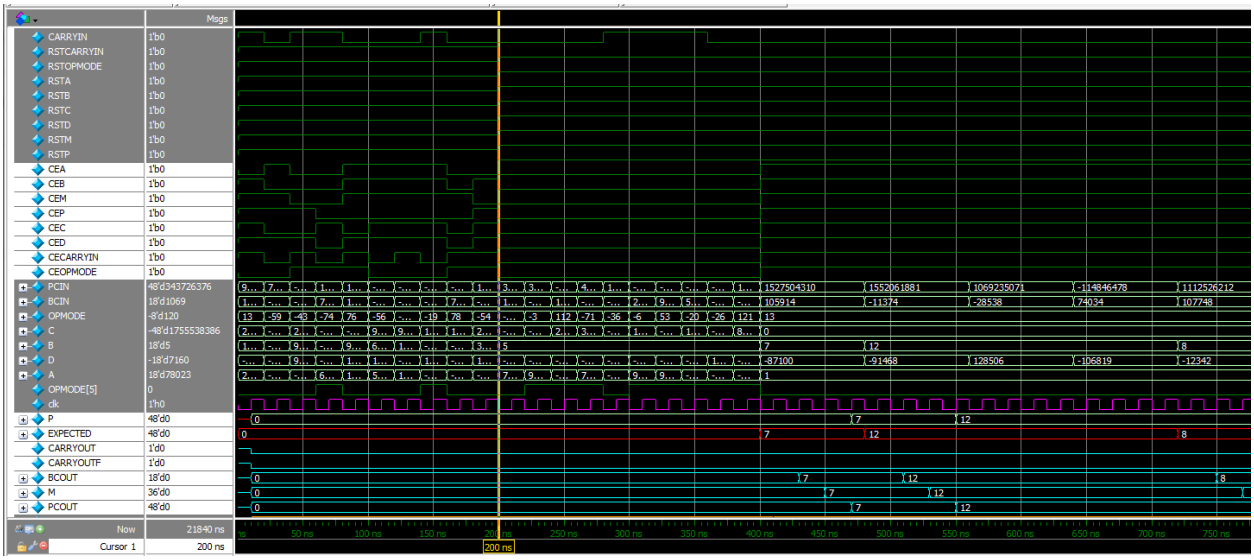
```
.main clear

vlib work

vlog DSP.v TB_DSP.v reg_mux_pair.v

vsim -voptargs=+acc work.TB_DSP

#add wave *

add wave -radix decimal -position insertpoint  \
sim:/TB_DSP/CARRYIN \
sim:/TB_DSP/RSTCARRYIN \
sim:/TB_DSP/RSTOPMODE \
sim:/TB_DSP/RSTA \
sim:/TB_DSP/RSTB \
sim:/TB_DSP/RSTC \
sim:/TB_DSP/RSTD \
sim:/TB_DSP/RSTM \
sim:/TB_DSP/RSTP \
sim:/TB_DSP/CEA \
sim:/TB_DSP/CEB \
sim:/TB_DSP/CEM \
sim:/TB_DSP/CEP \
sim:/TB_DSP/CEC \
sim:/TB_DSP/CED \
sim:/TB_DSP/CECARRYIN \
sim:/TB_DSP/CEOPMODE \
sim:/TB_DSP/PCIN \
sim:/TB_DSP/BCIN \
sim:/TB_DSP/OPMODE \
sim:/TB_DSP/C \
sim:/TB_DSP/B \
sim:/TB_DSP/D \
sim:/TB_DSP/A \
{sim:/TB_DSP/OPMODE[5]}

add wave -color magenta -position insertpoint  \
sim:/TB_DSP/clk
```

2.do

```

add wave -radix decimal -color red -position insertpoint  \
sim:/TB_DSP/EXPECTED

add wave -radix decimal -color cyan -position insertpoint  \
sim:/TB_DSP/P \
sim:/TB_DSP/CARRYOUT \
sim:/TB_DSP/CARRYOUTF \
sim:/TB_DSP/BCOUT \
sim:/TB_DSP/M \
sim:/TB_DSP/PCOUT


add wave -radix decimal -color orange -position insertpoint  \
sim:/TB_DSP/DUT/opmode_r \
sim:/TB_DSP/DUT/a0_out \
sim:/TB_DSP/DUT/b0_out \
sim:/TB_DSP/DUT/d_out \
sim:/TB_DSP/DUT/b_in \
sim:/TB_DSP/DUT/pre_adder_out \
sim:/TB_DSP/DUT/bypass_b \
sim:/TB_DSP/DUT/c_out \
sim:/TB_DSP/DUT/a1_out \
sim:/TB_DSP/DUT/b1_out \
sim:/TB_DSP/DUT/multiplier_out \
sim:/TB_DSP/DUT/m_out \
sim:/TB_DSP/DUT/x_out \
sim:/TB_DSP/DUT/z_out \
sim:/TB_DSP/DUT/carry_cascade_out \
sim:/TB_DSP/DUT/COUT \
sim:/TB_DSP/DUT/CIN \
sim:/TB_DSP/DUT/post_adder_out

run -all

#quit -sim

```

Result of the Testbench

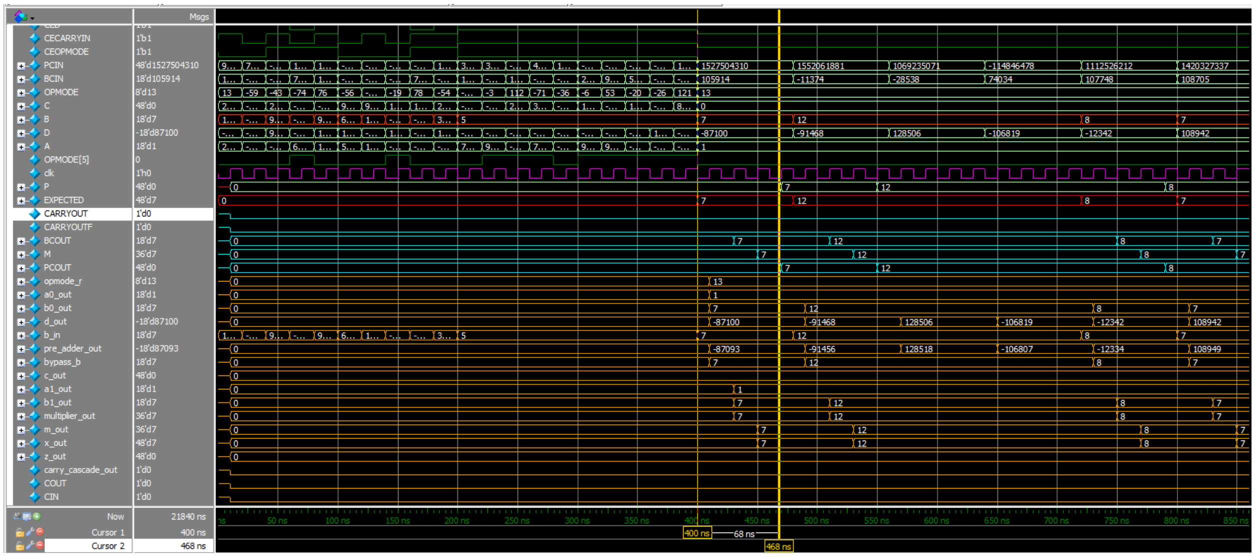
- Testing **reset** and **enable** signals of all registers




```
# ------------------------------------------> Testing Reset <--------------------------------------
#
# CLK= 0 ,A= 206022 ,B= 128908 ,C=  22509 ,D=      2097015289 ,OPMODE= 00_0_01101 ,BCOUT=      x ,M=          x ,CARRYOUT= x ,P=          x ,EXPECTED =          0
# CLK= 1 ,A= 206022 ,B= 128908 ,C=  22509 ,D=      2097015289 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 231178 ,B= 206437 ,C= 219181 ,D= 281473666998883 ,OPMODE= 11_0_00101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 231178 ,B= 206437 ,C= 219181 ,D= 281473666998883 ,OPMODE= 11_0_00101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A=  91402 ,B=  94927 ,C= 256285 ,D=       293882147 ,OPMODE= 11_0_10101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A=  91402 ,B=  94927 ,C= 256285 ,D=       293882147 ,OPMODE= 11_0_10101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 245361 ,B= 253226 ,C=  66236 ,D= 281472927242763 ,OPMODE= 10_1_10110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 245361 ,B= 253226 ,C=  66236 ,D= 281472927242763 ,OPMODE= 10_1_10110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 103516 ,B=  90295 ,C= 109048 ,D= 281474167494303 ,OPMODE= 01_0_01100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 103516 ,B=  90295 ,C= 109048 ,D= 281474167494303 ,OPMODE= 01_0_01100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 124729 ,B=  65662 ,C=  56082 ,D=       921010541 ,OPMODE= 11_0_01000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 124729 ,B=  65662 ,C=  56082 ,D=       921010541 ,OPMODE= 11_0_01000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 242851 ,B= 113702 ,C= 104954 ,D=       966137715 ,OPMODE= 10_0_00110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 242851 ,B= 113702 ,C= 104954 ,D=       966137715 ,OPMODE= 10_0_00110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 130884 ,B= 169183 ,C= 189109 ,D=      1022433657 ,OPMODE= 11_1_01101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 130884 ,B= 169183 ,C= 189109 ,D=      1022433657 ,OPMODE= 11_1_01101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 246968 ,B= 166456 ,C= 244150 ,D=      1020364665 ,OPMODE= 01_0_01110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 246968 ,B= 166456 ,C= 244150 ,D=      1020364665 ,OPMODE= 01_0_01110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A=   1897 ,B=  39684 ,C= 203334 ,D=      2077385207 ,OPMODE= 11_0_01010 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A=   1897 ,B=  39684 ,C= 203334 ,D=      2077385207 ,OPMODE= 11_0_01010 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
#
# ------------------------------------------> Testing Enable <-------------------------------------
#
# CLK= 0 ,A= 254984 ,B=      5 ,C=  78023 ,D= 281473221172270 ,OPMODE= 10_0_01000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 254984 ,B=      5 ,C=  78023 ,D= 281473221172270 ,OPMODE= 10_0_01000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 247357 ,B=      5 ,C=  92038 ,D= 281474661353690 ,OPMODE= 11_1_11101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 247357 ,B=      5 ,C=  92038 ,D= 281474661353690 ,OPMODE= 11_1_11101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 132565 ,B=      5 ,C= 176990 ,D=      2101836282 ,OPMODE= 01_1_10000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 132565 ,B=      5 ,C= 176990 ,D=      2101836282 ,OPMODE= 01_1_10000 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 137910 ,B=      5 ,C=  74176 ,D=       321232678 ,OPMODE= 10_1_11001 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 137910 ,B=      5 ,C=  74176 ,D=       321232678 ,OPMODE= 10_1_11001 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 243407 ,B=      5 ,C= 170878 ,D= 281474667217115 ,OPMODE= 11_0_11100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 243407 ,B=      5 ,C= 170878 ,D= 281474667217115 ,OPMODE= 11_0_11100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 235088 ,B=      5 ,C=  96417 ,D=      1131909510 ,OPMODE= 11_1_11010 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 235088 ,B=      5 ,C=  96417 ,D=      1131909510 ,OPMODE= 11_1_11010 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 162635 ,B=      5 ,C=  95429 ,D= 281474104407192 ,OPMODE= 00_1_10101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 162635 ,B=      5 ,C=  95429 ,D= 281474104407192 ,OPMODE= 00_1_10101 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 167073 ,B=      5 ,C= 229544 ,D=      1419705769 ,OPMODE= 11_1_01100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 167073 ,B=      5 ,C= 229544 ,D=      1419705769 ,OPMODE= 11_1_01100 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 130974 ,B=      5 ,C= 138538 ,D= 281474015556749 ,OPMODE= 11_1_00110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 130974 ,B=      5 ,C= 138538 ,D= 281474015556749 ,OPMODE= 11_1_00110 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 0 ,A= 241351 ,B=      5 ,C= 213267 ,D=       899729771 ,OPMODE= 01_1_11001 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
# CLK= 1 ,A= 241351 ,B=      5 ,C= 213267 ,D=       899729771 ,OPMODE= 01_1_11001 ,BCOUT=      0 ,M=          0 ,CARRYOUT= 0 ,P=          0 ,EXPECTED =          0
#
```

- Testing **bypassing the pre-adder**, by forcing A = 1 & C = 0, so the output "**P**" will take the value of "**B**" after 4 clock cycle (# Pipeline Stages)

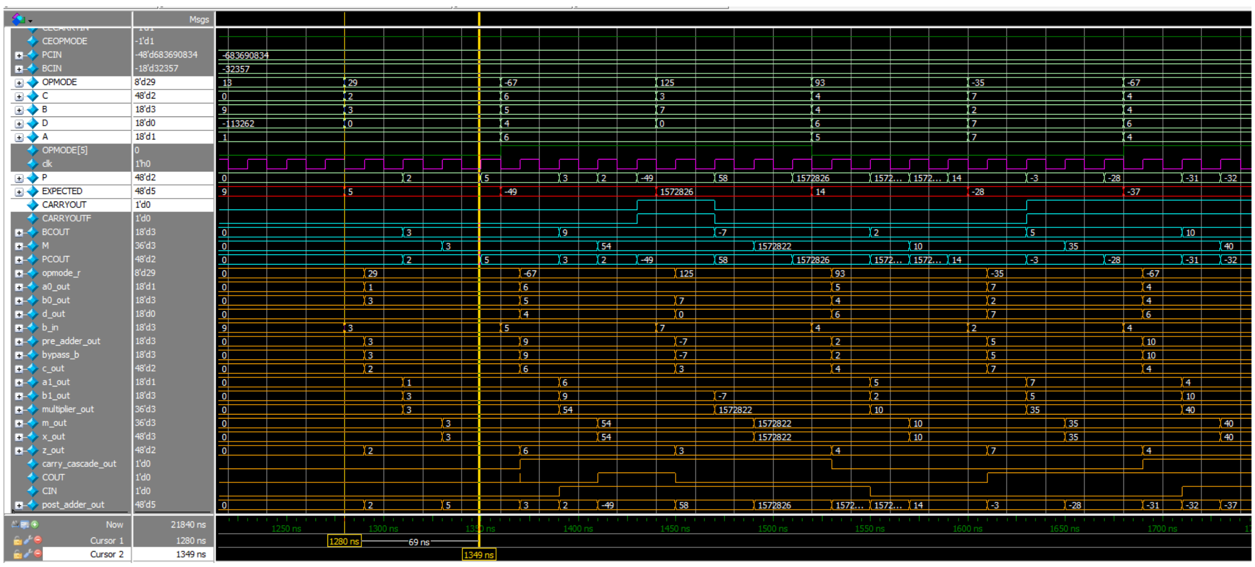
- **Note:**
  - The orange signal are the internal signals of the DUT




```
#
# -----------------------------------------> Testing bypass B <------------------------------------------
#
# CLK= 0 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     0 ,M=         0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 1 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     0 ,M=         0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 0 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     0 ,M=         0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 1 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 0 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 1 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 0 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =          7
# CLK= 1 ,D= 175044 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =          7
# CLK= 0 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 1 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 0 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     7 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 1 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 0 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=         7 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 1 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 0 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=              7 ,EXPECTED =         12
# CLK= 1 ,D= 170676 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 128506 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 1 ,D= 155325 ,B=     12 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =         12
# CLK= 0 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 1 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 0 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=    12 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 1 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 0 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=        12 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 1 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=         8 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 0 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=         8 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =          8
# CLK= 1 ,D= 249802 ,B=      8 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=         8 ,CARRYOUT= 0 ,P=              8 ,EXPECTED =          8
# CLK= 0 ,D= 108942 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=         8 ,CARRYOUT= 0 ,P=              8 ,EXPECTED =          7
# CLK= 1 ,D= 108942 ,B=      7 ,A=      1 ,C=              0 ,OPMODE= 00_0_01101 ,BCOUT=     8 ,M=         8 ,CARRYOUT= 0 ,P=              8 ,EXPECTED =          7
```

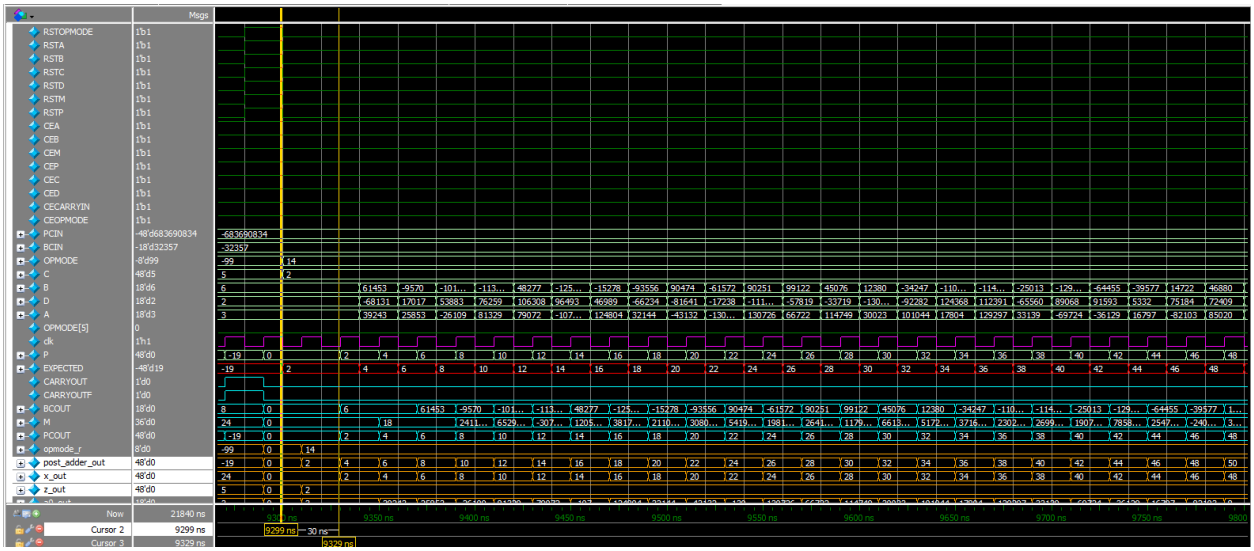
- Testing **arithmetic operations**, by randomizing **A,B,C,D** and **OPMODE**[7:5], Then compare the output "**P**" with Expected value calculated by the following golden model

```
case (OPMODE[7:6])
    2'b00 : begin PRE_EXP = D+B; EXPECTED = C + (A*PRE_EXP + OPMODE[5]); end
    2'b01 : begin PRE_EXP = D-B; EXPECTED = C + (A*PRE_EXP + OPMODE[5]); end
    2'b10 : begin PRE_EXP = D+B; EXPECTED = C - (A*PRE_EXP + OPMODE[5]); end
    2'b11 : begin PRE_EXP = D-B; EXPECTED = C - (A*PRE_EXP + OPMODE[5]); end
endcase
```



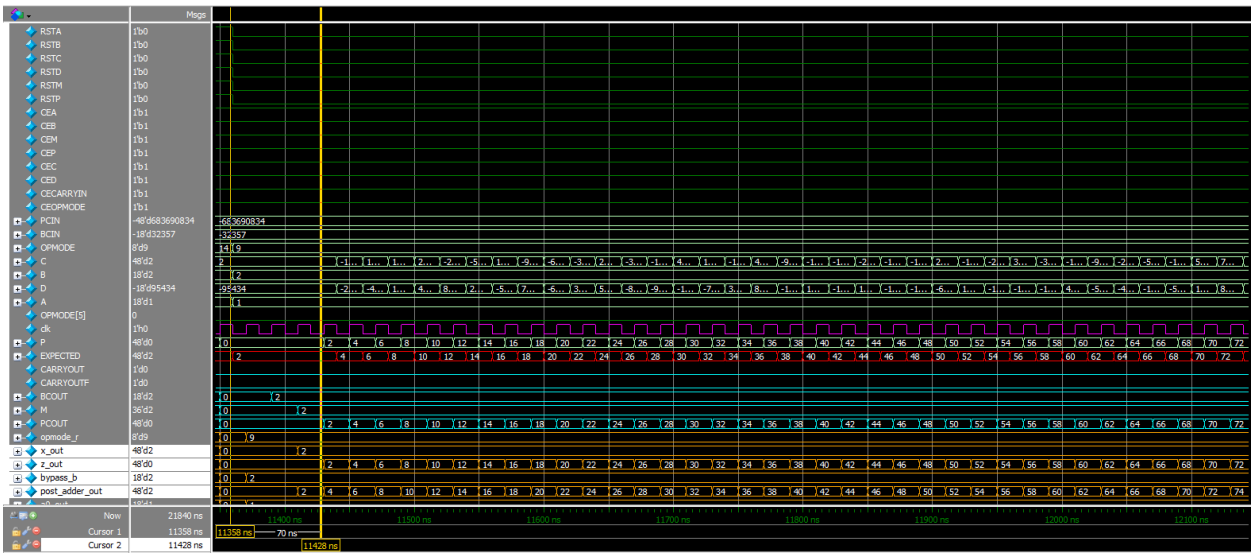
```
# -----------------------------------------> Testing arithematic operations <-----------------------------------------
#
# CLK= 0 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      9 ,M=         9 ,CARRYOUT= 0 ,P=               9 ,EXPECTED =               9
# CLK= 1 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 0 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 1 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 0 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 1 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 0 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 1 ,D= 148882 ,B=     9 ,A=     1 ,C=            0 ,OPMODE= 00_0_01101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               9
# CLK= 0 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               5
# CLK= 1 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               5
# CLK= 0 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      0 ,M=         0 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =               5
# CLK= 1 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      3 ,M=         0 ,CARRYOUT= 0 ,P=               2 ,EXPECTED =               5
# CLK= 0 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      3 ,M=         0 ,CARRYOUT= 0 ,P=               2 ,EXPECTED =               5
# CLK= 1 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               2 ,EXPECTED =               5
# CLK= 0 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               2 ,EXPECTED =               5
# CLK= 1 ,D=      0 ,B=     3 ,A=     1 ,C=            2 ,OPMODE= 00_0_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               5 ,EXPECTED =               5
# CLK= 0 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               5 ,EXPECTED = 281474976710607
# CLK= 1 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               5 ,EXPECTED = 281474976710607
# CLK= 0 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      3 ,M=         3 ,CARRYOUT= 0 ,P=               5 ,EXPECTED = 281474976710607
# CLK= 1 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      9 ,M=         3 ,CARRYOUT= 0 ,P=               3 ,EXPECTED = 281474976710607
# CLK= 0 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      9 ,M=         3 ,CARRYOUT= 0 ,P=               3 ,EXPECTED = 281474976710607
# CLK= 1 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 0 ,P=               2 ,EXPECTED = 281474976710607
# CLK= 0 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 0 ,P=               2 ,EXPECTED = 281474976710607
# CLK= 1 ,D=      4 ,B=     5 ,A=     6 ,C=            6 ,OPMODE= 10_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 1 ,P= 281474976710607 ,EXPECTED = 281474976710607
# CLK= 0 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 1 ,P= 281474976710607 ,EXPECTED =         1572826
# CLK= 1 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 1 ,P= 281474976710607 ,EXPECTED =         1572826
# CLK= 0 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT=      9 ,M=        54 ,CARRYOUT= 1 ,P= 281474976710607 ,EXPECTED =         1572826
# CLK= 1 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT= 262137 ,M=        54 ,CARRYOUT= 0 ,P=              58 ,EXPECTED =         1572826
# CLK= 0 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT= 262137 ,M=        54 ,CARRYOUT= 0 ,P=              58 ,EXPECTED =         1572826
# CLK= 1 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=              58 ,EXPECTED =         1572826
# CLK= 0 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=              58 ,EXPECTED =         1572826
# CLK= 1 ,D=      0 ,B=     7 ,A=     6 ,C=            3 ,OPMODE= 01_1_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =         1572826
# CLK= 0 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =              14
# CLK= 1 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =              14
# CLK= 0 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT= 262137 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =              14
# CLK= 1 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT=      2 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572827 ,EXPECTED =              14
# CLK= 0 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT=      2 ,M=   1572822 ,CARRYOUT= 0 ,P=         1572827 ,EXPECTED =              14
# CLK= 1 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT=      2 ,M=        10 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =              14
# CLK= 0 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT=      2 ,M=        10 ,CARRYOUT= 0 ,P=         1572826 ,EXPECTED =              14
# CLK= 1 ,D=      6 ,B=     4 ,A=     5 ,C=            4 ,OPMODE= 01_0_11101 ,BCOUT=      2 ,M=        10 ,CARRYOUT= 0 ,P=              14 ,EXPECTED =              14
# CLK= 0 ,D=      7 ,B=     2 ,A=     7 ,C=            7 ,OPMODE= 11_0_11101 ,BCOUT=      2 ,M=        10 ,CARRYOUT= 0 ,P=              14 ,EXPECTED = 281474976710628
# CLK= 1 ,D=      7 ,B=     2 ,A=     7 ,C=            7 ,OPMODE= 11_0_11101 ,BCOUT=      2 ,M=        10 ,CARRYOUT= 0 ,P=              14 ,EXPECTED = 281474976710628
```

- Testing accumulator through Mux “X”, the resetting to force all FF’s output to be zero, then forcing **C** = 2 to make **P** = 2 after 2 cycles then **P** will be increased by 2 every 1 clock cycle



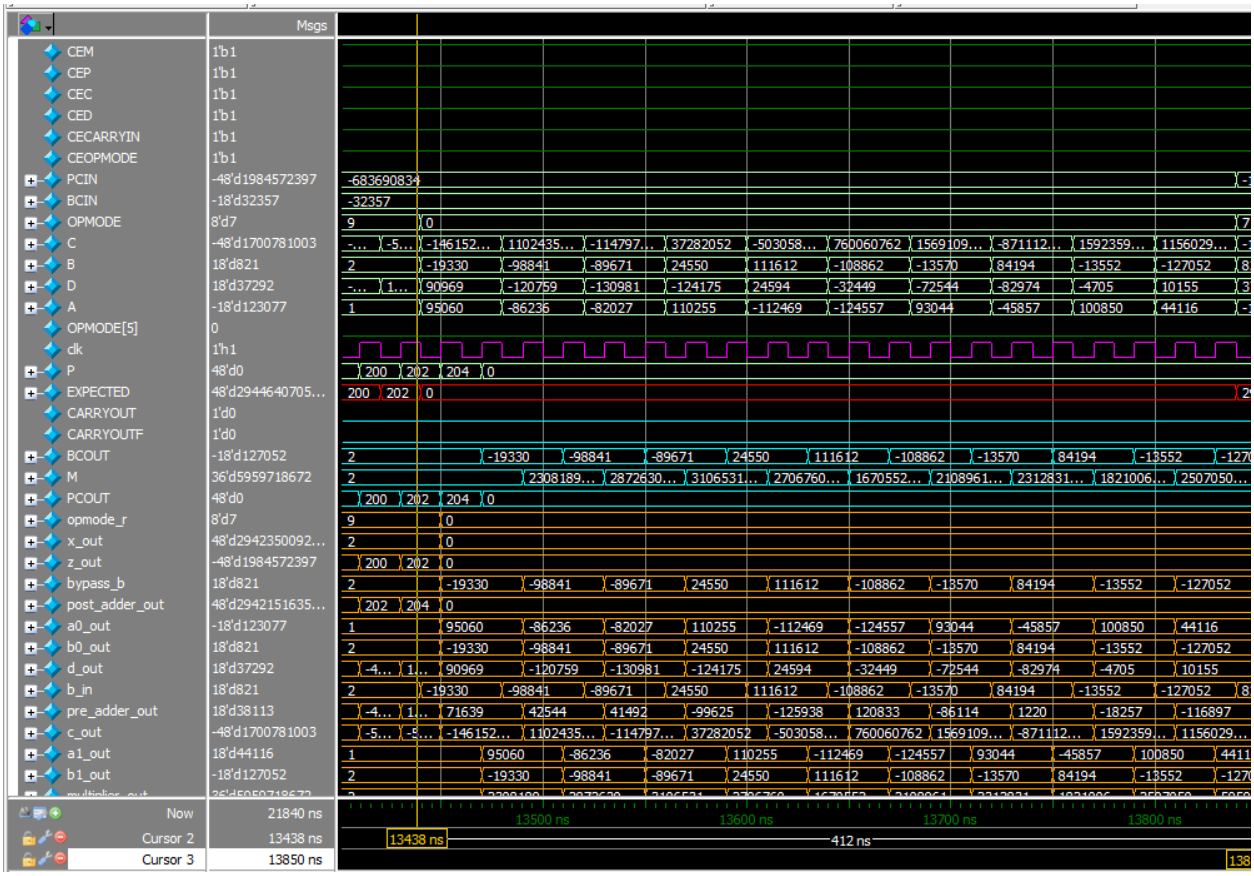

```
# ----------------------------------------> Testing Accumulator through X <----------------------------------------
#
# CLK= 0 ,D=       2 ,B=       6 ,A=       3 ,C=               5 ,OPMODE= 10_0_11101 ,BCOUT=       8 ,M=          24 ,CARRYOUT= 1 ,P= 281474976710637 ,EXPECTED = 281474976710637
# CLK= 1 ,D=       2 ,B=       6 ,A=       3 ,C=               5 ,OPMODE= 10_0_11101 ,BCOUT=       0 ,M=           0 ,CARRYOUT= 0 ,P=                 0 ,EXPECTED = 281474976710637
# CLK= 0 ,D=       2 ,B=       6 ,A=       3 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       0 ,M=           0 ,CARRYOUT= 0 ,P=                 0 ,EXPECTED =                 2
# CLK= 1 ,D=       2 ,B=       6 ,A=       3 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       0 ,M=           0 ,CARRYOUT= 0 ,P=                 0 ,EXPECTED =                 2
# CLK= 0 ,D=       2 ,B=       6 ,A=       3 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       0 ,M=           0 ,CARRYOUT= 0 ,P=                 0 ,EXPECTED =                 2
# CLK= 1 ,D=       2 ,B=       6 ,A=       3 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       6 ,M=           0 ,CARRYOUT= 0 ,P=                 2 ,EXPECTED =                 2
# CLK= 0 ,D= 194013 ,B=   61453 ,A=   39243 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       6 ,M=           0 ,CARRYOUT= 0 ,P=                 2 ,EXPECTED =                 4
# CLK= 1 ,D= 194013 ,B=   61453 ,A=   39243 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       6 ,M=          18 ,CARRYOUT= 0 ,P=                 4 ,EXPECTED =                 4
# CLK= 0 ,D=  17017 ,B= 252574 ,A=   25853 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=       6 ,M=          18 ,CARRYOUT= 0 ,P=                 4 ,EXPECTED =                 6
# CLK= 1 ,D=  17017 ,B= 252574 ,A=   25853 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=   61453 ,M=          18 ,CARRYOUT= 0 ,P=                 6 ,EXPECTED =                 6
# CLK= 0 ,D=  53883 ,B= 160655 ,A= 236035 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=   61453 ,M=          18 ,CARRYOUT= 0 ,P=                 6 ,EXPECTED =                 8
# CLK= 1 ,D=  53883 ,B= 160655 ,A= 236035 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 252574 ,M=  2411600079 ,CARRYOUT= 0 ,P=                 8 ,EXPECTED =                 8
# CLK= 0 ,D=  76259 ,B= 148253 ,A=  81329 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 252574 ,M=  2411600079 ,CARRYOUT= 0 ,P=                 8 ,EXPECTED =                10
# CLK= 1 ,D=  76259 ,B= 148253 ,A=  81329 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 160655 ,M=  6529795622 ,CARRYOUT= 0 ,P=                10 ,EXPECTED =                10
# CLK= 0 ,D= 106308 ,B=  48277 ,A=  79072 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 160655 ,M=  6529795622 ,CARRYOUT= 0 ,P=                10 ,EXPECTED =                12
# CLK= 1 ,D= 106308 ,B=  48277 ,A=  79072 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 148253 ,M= 37920202925 ,CARRYOUT= 0 ,P=                12 ,EXPECTED =                12
# CLK= 0 ,D=  96493 ,B= 136530 ,A= 154616 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 148253 ,M= 37920202925 ,CARRYOUT= 0 ,P=                12 ,EXPECTED =                14
# CLK= 1 ,D=  96493 ,B= 136530 ,A= 154616 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  48277 ,M= 12057268237 ,CARRYOUT= 0 ,P=                14 ,EXPECTED =                14
# CLK= 0 ,D=  46989 ,B= 246866 ,A= 124804 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  48277 ,M= 12057268237 ,CARRYOUT= 0 ,P=                14 ,EXPECTED =                16
# CLK= 1 ,D=  46989 ,B= 246866 ,A= 124804 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 136530 ,M=  3817358944 ,CARRYOUT= 0 ,P=                16 ,EXPECTED =                16
# CLK= 0 ,D= 195910 ,B= 168588 ,A=  32144 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 136530 ,M=  3817358944 ,CARRYOUT= 0 ,P=                16 ,EXPECTED =                18
# CLK= 1 ,D= 195910 ,B= 168588 ,A=  32144 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 246866 ,M= 21109722480 ,CARRYOUT= 0 ,P=                18 ,EXPECTED =                18
# CLK= 0 ,D= 180503 ,B=  90474 ,A= 219012 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 246866 ,M= 21109722480 ,CARRYOUT= 0 ,P=                18 ,EXPECTED =                20
# CLK= 1 ,D= 180503 ,B=  90474 ,A= 219012 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 168588 ,M= 30809864264 ,CARRYOUT= 0 ,P=                20 ,EXPECTED =                20
# CLK= 0 ,D= 244906 ,B= 200572 ,A= 131680 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 168588 ,M= 30809864264 ,CARRYOUT= 0 ,P=                20 ,EXPECTED =                22
# CLK= 1 ,D= 244906 ,B= 200572 ,A= 131680 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  90474 ,M=  5419092672 ,CARRYOUT= 0 ,P=                22 ,EXPECTED =                22
# CLK= 0 ,D= 150970 ,B=  90251 ,A= 130726 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  90474 ,M=  5419092672 ,CARRYOUT= 0 ,P=                22 ,EXPECTED =                24
# CLK= 1 ,D= 150970 ,B=  90251 ,A= 130726 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 200572 ,M= 19814891688 ,CARRYOUT= 0 ,P=                24 ,EXPECTED =                24
# CLK= 0 ,D= 204325 ,B=  99122 ,A=  66722 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT= 200572 ,M= 19814891688 ,CARRYOUT= 0 ,P=                24 ,EXPECTED =                26
# CLK= 1 ,D= 204325 ,B=  99122 ,A=  66722 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  90251 ,M= 26411320960 ,CARRYOUT= 0 ,P=                26 ,EXPECTED =                26
# CLK= 0 ,D= 228425 ,B=  45076 ,A= 114749 ,C=               2 ,OPMODE= 00_0_01110 ,BCOUT=  90251 ,M= 26411320960 ,CARRYOUT= 0 ,P=                26 ,EXPECTED =                28
```

- Testing accumulator through Mux “Z”, the resetting to force all FF’s output to be zero, then bypassing **B** = 2, then mutilpy it by **A** = 1 to make **P** = 2 after 4 cycles then **P** will be increased by 2 every 1 clock cycle




```
# ----------------------------------------> Testing Accumlator through Z <----------------------------------------
#
# CLK= 0 ,D= 166710 ,B= 131890 ,A= 206969 ,C=              2 ,OPMODE= 00_0_01110 ,BCOUT=  16900 ,M= 39697527936 ,CARRYOUT= 0 ,P=            202 ,EXPECTED =            202
# CLK= 1 ,D= 166710 ,B= 131890 ,A= 206969 ,C=              2 ,OPMODE= 00_0_01110 ,BCOUT=      0 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =            202
# CLK= 0 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      0 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 1 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      0 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 0 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      0 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 1 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 0 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           0 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 1 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 0 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              0 ,EXPECTED =              2
# CLK= 1 ,D= 166710 ,B=      2 ,A=      1 ,C=              2 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              2 ,EXPECTED =              2
# CLK= 0 ,D= 241380 ,B=      2 ,A=      1 ,C= 281473018162198 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              2 ,EXPECTED =              4
# CLK= 1 ,D= 241380 ,B=      2 ,A=      1 ,C= 281473018162198 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              4 ,EXPECTED =              4
# CLK= 0 ,D= 257194 ,B=      2 ,A=      1 ,C=      1615881664 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              4 ,EXPECTED =              6
# CLK= 1 ,D= 257194 ,B=      2 ,A=      1 ,C=      1615881664 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              6 ,EXPECTED =              6
# CLK= 0 ,D= 100398 ,B=      2 ,A=      1 ,C=      1181038476 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              6 ,EXPECTED =              8
# CLK= 1 ,D= 100398 ,B=      2 ,A=      1 ,C=      1181038476 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              8 ,EXPECTED =              8
# CLK= 0 ,D=  49777 ,B=      2 ,A=      1 ,C=      2113835003 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=              8 ,EXPECTED =             10
# CLK= 1 ,D=  49777 ,B=      2 ,A=      1 ,C=      2113835003 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             10 ,EXPECTED =             10
# CLK= 0 ,D=   8636 ,B=      2 ,A=      1 ,C= 281474682087644 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             10 ,EXPECTED =             12
# CLK= 1 ,D=   8636 ,B=      2 ,A=      1 ,C= 281474682087644 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =             12
# CLK= 0 ,D=  22295 ,B=      2 ,A=      1 ,C= 281474454521025 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             12 ,EXPECTED =             14
# CLK= 1 ,D=  22295 ,B=      2 ,A=      1 ,C= 281474454521025 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             14 ,EXPECTED =             14
# CLK= 0 ,D= 205291 ,B=      2 ,A=      1 ,C=      1520253877 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             14 ,EXPECTED =             16
# CLK= 1 ,D= 205291 ,B=      2 ,A=      1 ,C=      1520253877 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             16 ,EXPECTED =             16
# CLK= 0 ,D=  77449 ,B=      2 ,A=      1 ,C= 281474032132751 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             16 ,EXPECTED =             18
# CLK= 1 ,D=  77449 ,B=      2 ,A=      1 ,C= 281474032132751 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             18 ,EXPECTED =             18
# CLK= 0 ,D= 194239 ,B=      2 ,A=      1 ,C= 281474310220464 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             18 ,EXPECTED =             20
# CLK= 1 ,D= 194239 ,B=      2 ,A=      1 ,C= 281474310220464 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             20 ,EXPECTED =             20
# CLK= 0 ,D=  39635 ,B=      2 ,A=      1 ,C= 281474626290390 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             20 ,EXPECTED =             22
# CLK= 1 ,D=  39635 ,B=      2 ,A=      1 ,C= 281474626290390 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             22 ,EXPECTED =             22
# CLK= 0 ,D=  52354 ,B=      2 ,A=      1 ,C=       224621850 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             22 ,EXPECTED =             24
# CLK= 1 ,D=  52354 ,B=      2 ,A=      1 ,C=       224621850 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             24 ,EXPECTED =             24
# CLK= 0 ,D= 173937 ,B=      2 ,A=      1 ,C= 281474633303255 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             24 ,EXPECTED =             26
# CLK= 1 ,D= 173937 ,B=      2 ,A=      1 ,C= 281474633303255 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             26 ,EXPECTED =             26
# CLK= 0 ,D= 167438 ,B=      2 ,A=      1 ,C= 281474855539953 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             26 ,EXPECTED =             28
# CLK= 1 ,D= 167438 ,B=      2 ,A=      1 ,C= 281474855539953 ,OPMODE= 00_0_01001 ,BCOUT=      2 ,M=           2 ,CARRYOUT= 0 ,P=             28 ,EXPECTED =             28
```

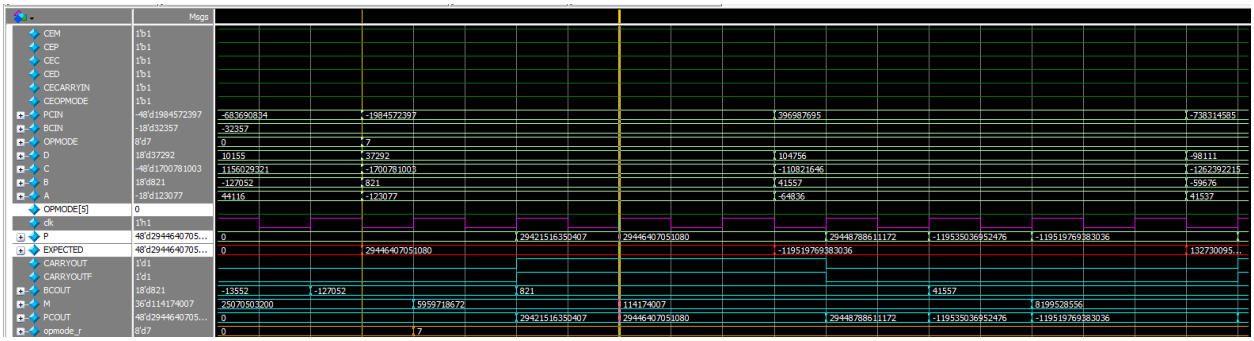
- Testing Placing all zeros in the two Muxs (Mux X & Mux Z)




```
# ----------------------------------------> Testing Placing all zeros <----------------------------------------
#
# CLK= 0 ,D=   4216 ,B=   3367 ,A=  75359 ,C=       297818915 ,OPMODE= 00_0_00000 ,BCOUT=       2 ,M=           2 ,CARRYOUT= 0 ,P=             202 ,EXPECTED =             0
# CLK= 1 ,D=   4216 ,B=   3367 ,A=  75359 ,C=       297818915 ,OPMODE= 00_0_00000 ,BCOUT=       2 ,M=           2 ,CARRYOUT= 0 ,P=             204 ,EXPECTED =             0
# CLK= 0 ,D=   4216 ,B=   3367 ,A=  75359 ,C=       297818915 ,OPMODE= 00_0_00000 ,BCOUT=       2 ,M=           2 ,CARRYOUT= 0 ,P=             204 ,EXPECTED =             0
# CLK= 1 ,D=   4216 ,B=   3367 ,A=  75359 ,C=       297818915 ,OPMODE= 00_0_00000 ,BCOUT=    3367 ,M=           2 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 191403 ,B= 137016 ,A= 216354 ,C=      1693629897 ,OPMODE= 00_0_00000 ,BCOUT=    3367 ,M=           2 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 191403 ,B= 137016 ,A= 216354 ,C=      1693629897 ,OPMODE= 00_0_00000 ,BCOUT=    3367 ,M=   253733753 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 191403 ,B= 137016 ,A= 216354 ,C=      1693629897 ,OPMODE= 00_0_00000 ,BCOUT=    3367 ,M=   253733753 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 191403 ,B= 137016 ,A= 216354 ,C=      1693629897 ,OPMODE= 00_0_00000 ,BCOUT= 137016 ,M=   253733753 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 216263 ,B=  25218 ,A=  55246 ,C= 281474499486407 ,OPMODE= 00_0_00000 ,BCOUT= 137016 ,M=   253733753 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 216263 ,B=  25218 ,A=  55246 ,C= 281474499486407 ,OPMODE= 00_0_00000 ,BCOUT= 137016 ,M= 29643959664 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 216263 ,B=  25218 ,A=  55246 ,C= 281474499486407 ,OPMODE= 00_0_00000 ,BCOUT= 137016 ,M= 29643959664 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 216263 ,B=  25218 ,A=  55246 ,C= 281474499486407 ,OPMODE= 00_0_00000 ,BCOUT=  25218 ,M= 29643959664 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 238628 ,B= 225243 ,A=  70664 ,C=       985821045 ,OPMODE= 00_0_00000 ,BCOUT=  25218 ,M= 29643959664 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 238628 ,B= 225243 ,A=  70664 ,C=       985821045 ,OPMODE= 00_0_00000 ,BCOUT=  25218 ,M=  1393193628 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 238628 ,B= 225243 ,A=  70664 ,C=       985821045 ,OPMODE= 00_0_00000 ,BCOUT=  25218 ,M=  1393193628 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 238628 ,B= 225243 ,A=  70664 ,C=       985821045 ,OPMODE= 00_0_00000 ,BCOUT= 225243 ,M=  1393193628 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 204213 ,B=  94746 ,A= 135992 ,C= 281473922054786 ,OPMODE= 00_0_00000 ,BCOUT= 225243 ,M=  1393193628 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 204213 ,B=  94746 ,A= 135992 ,C= 281473922054786 ,OPMODE= 00_0_00000 ,BCOUT= 225243 ,M= 15916571352 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 204213 ,B=  94746 ,A= 135992 ,C= 281473922054786 ,OPMODE= 00_0_00000 ,BCOUT= 225243 ,M= 15916571352 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 204213 ,B=  94746 ,A= 135992 ,C= 281473922054786 ,OPMODE= 00_0_00000 ,BCOUT=  94746 ,M= 15916571352 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 106584 ,B= 158288 ,A=  39587 ,C=      1380180900 ,OPMODE= 00_0_00000 ,BCOUT=  94746 ,M= 15916571352 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 106584 ,B= 158288 ,A=  39587 ,C=      1380180900 ,OPMODE= 00_0_00000 ,BCOUT=  94746 ,M= 12884698032 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 106584 ,B= 158288 ,A=  39587 ,C=      1380180900 ,OPMODE= 00_0_00000 ,BCOUT=  94746 ,M= 12884698032 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 106584 ,B= 158288 ,A=  39587 ,C=      1380180900 ,OPMODE= 00_0_00000 ,BCOUT= 158288 ,M= 12884698032 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 0 ,D= 253797 ,B=   6122 ,A=  14598 ,C= 281473535148116 ,OPMODE= 00_0_00000 ,BCOUT= 158288 ,M= 12884698032 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
# CLK= 1 ,D= 253797 ,B=   6122 ,A=  14598 ,C= 281473535148116 ,OPMODE= 00_0_00000 ,BCOUT= 158288 ,M=  6266147056 ,CARRYOUT= 0 ,P=               0 ,EXPECTED =             0
```

- Testing Concatenation & PCIN, the (correct concatenated output+ PCIN) will be available after 3 clock cycle after forcing the inputs (**A,B,C,D** and **OPMODE**)

- **Note:**
  There is no relation between concatenation & PCIN, I just have tested them together as they are simple cases. However, PCIN can be used with the other functionalities.




```
# CLK= 0 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT=  98085 ,M=  5798294775 ,CARRYOUT= 1 ,P=  90243379841990 ,EXPECTED = 274661678458180
# CLK= 1 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT=  98085 ,M=  5798294775 ,CARRYOUT= 1 ,P=  90242412526931 ,EXPECTED = 274661678458180
# CLK= 0 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT=  98085 ,M=  5798294775 ,CARRYOUT= 1 ,P=  90242412526931 ,EXPECTED = 274661678458180
# CLK= 1 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M=  5798294775 ,CARRYOUT= 1 ,P= 274616768609619 ,EXPECTED = 274661678458180
# CLK= 0 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M=  5798294775 ,CARRYOUT= 1 ,P= 274616768609619 ,EXPECTED = 274661678458180
# CLK= 1 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274661678458180 ,EXPECTED = 274661678458180
# CLK= 0 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274661678458180 ,EXPECTED = 274661678458180
# CLK= 1 ,D=  94108 ,B= 222998 ,A= 230432 ,C= 281474459889346 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274661678458180 ,EXPECTED = 274661678458180
# CLK= 0 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274661678458180 ,EXPECTED = 179041259803034
# CLK= 1 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274662539222955 ,EXPECTED = 179041259803034
# CLK= 0 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 222998 ,M= 51385875136 ,CARRYOUT= 1 ,P= 274662539222955 ,EXPECTED = 179041259803034
# CLK= 1 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 186629 ,M= 51385875136 ,CARRYOUT= 1 ,P= 179073747083179 ,EXPECTED = 179041259803034
# CLK= 0 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 186629 ,M= 51385875136 ,CARRYOUT= 1 ,P= 179073747083179 ,EXPECTED = 179041259803034
# CLK= 1 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 186629 ,M= 19876548387 ,CARRYOUT= 1 ,P= 179041259803034 ,EXPECTED = 179041259803034
# CLK= 0 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 186629 ,M= 19876548387 ,CARRYOUT= 1 ,P= 179041259803034 ,EXPECTED = 179041259803034
# CLK= 1 ,D=  10797 ,B= 186629 ,A= 106503 ,C=      1952183784 ,OPMODE= 00_0_00111 ,BCOUT= 186629 ,M= 19876548387 ,CARRYOUT= 1 ,P= 179041259803034 ,EXPECTED = 179041259803034
#
# --->  NO ERRORS, All Outputs are Correct :)  <---
#
# ** Note: $stop    : TB_DSP.v(246)
#    Time: 21840 ns  Iteration: 1  Instance: /TB_DSP
# Break in Module TB_DSP at TB_DSP.v line 246

VSIM(paused)>
```

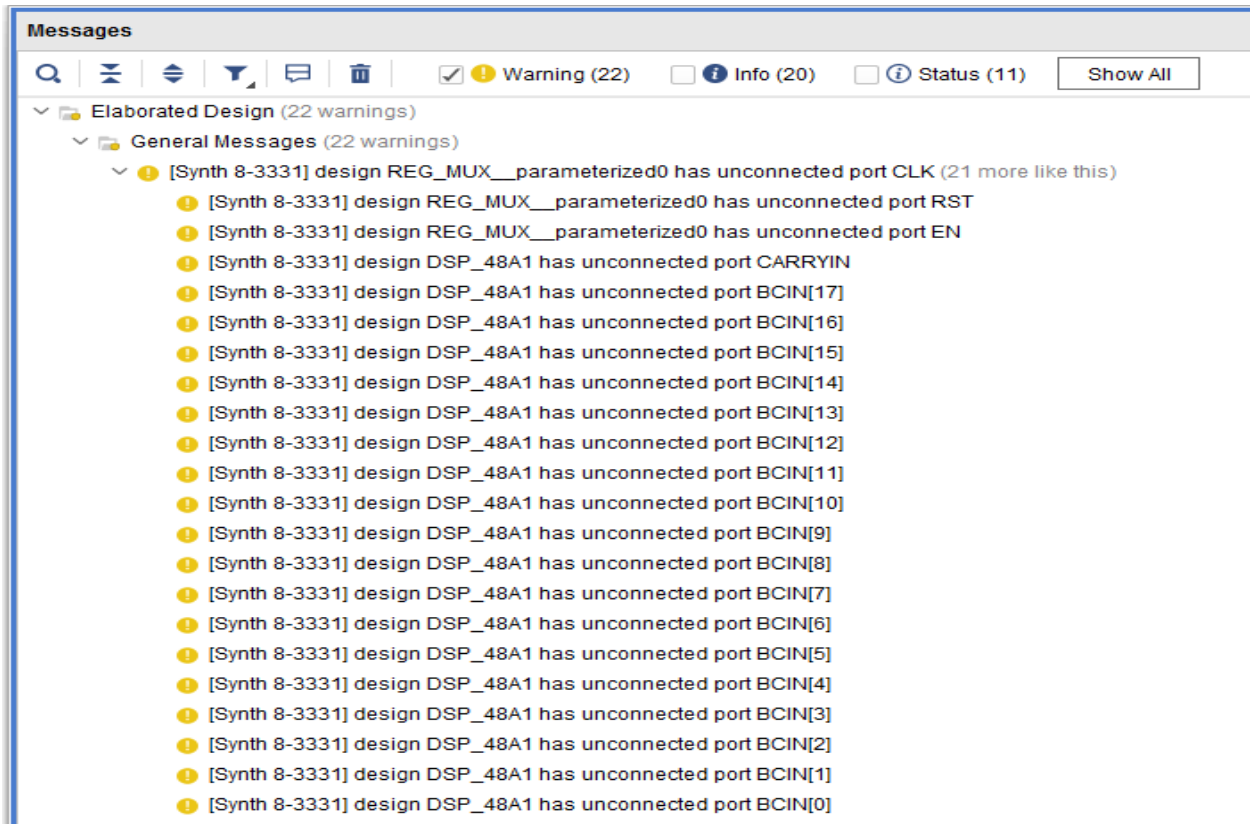
Constraint File

Constraints_basys3.xdc

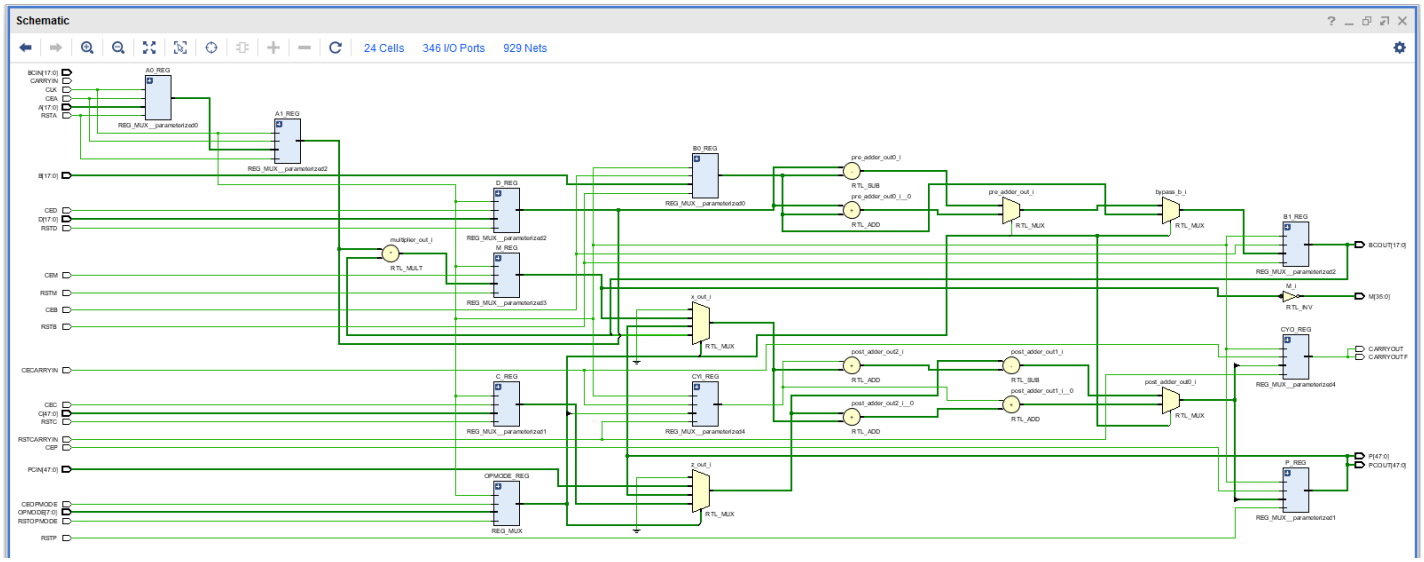
```
5
6   ## Clock signal
7   set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
8   create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
9
```

Elaboration

- Messages tab after elaboration.
- As shown in the snippet → **No critical warnings or errors**.

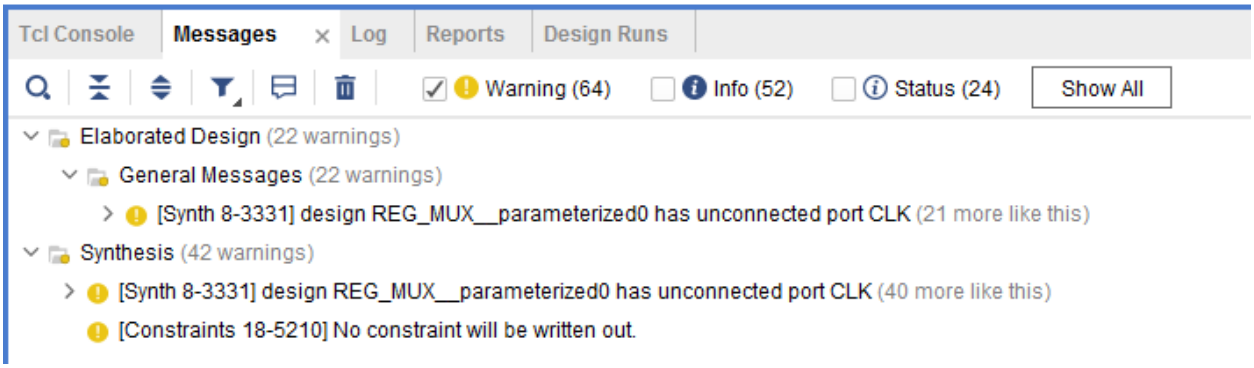


- Schematic after elaboration.

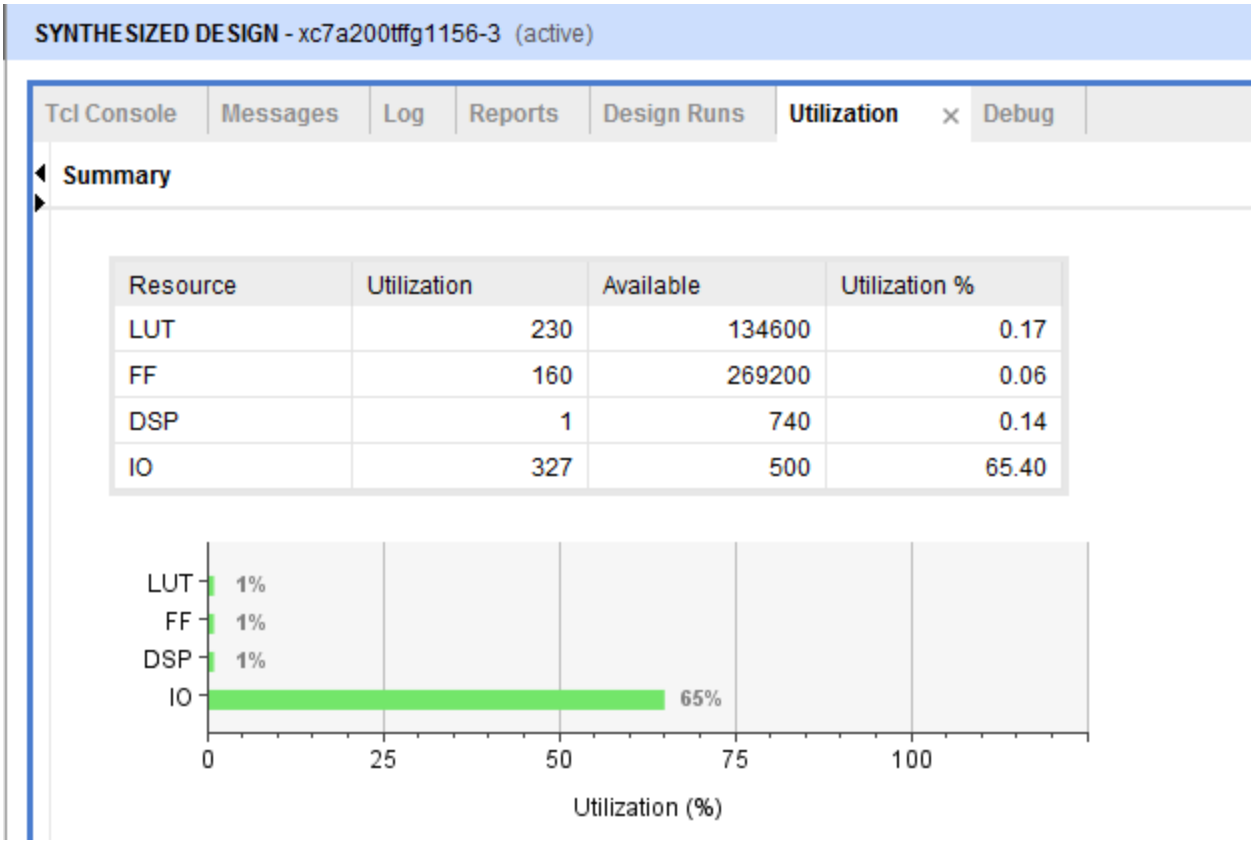


Synthesis

- Messages tab after running synthesis.
- As shown in the snippet → **No critical warnings or errors**.

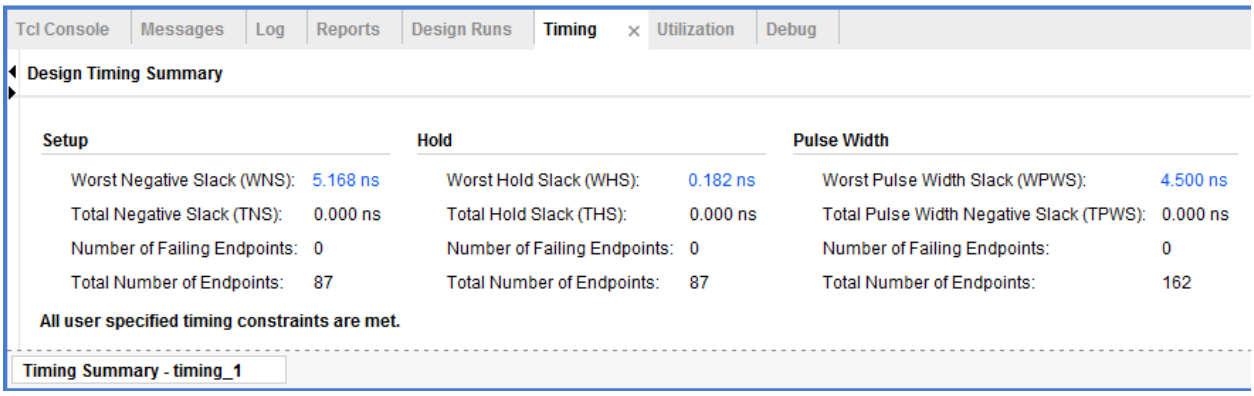


- Utilization after running synthesis.

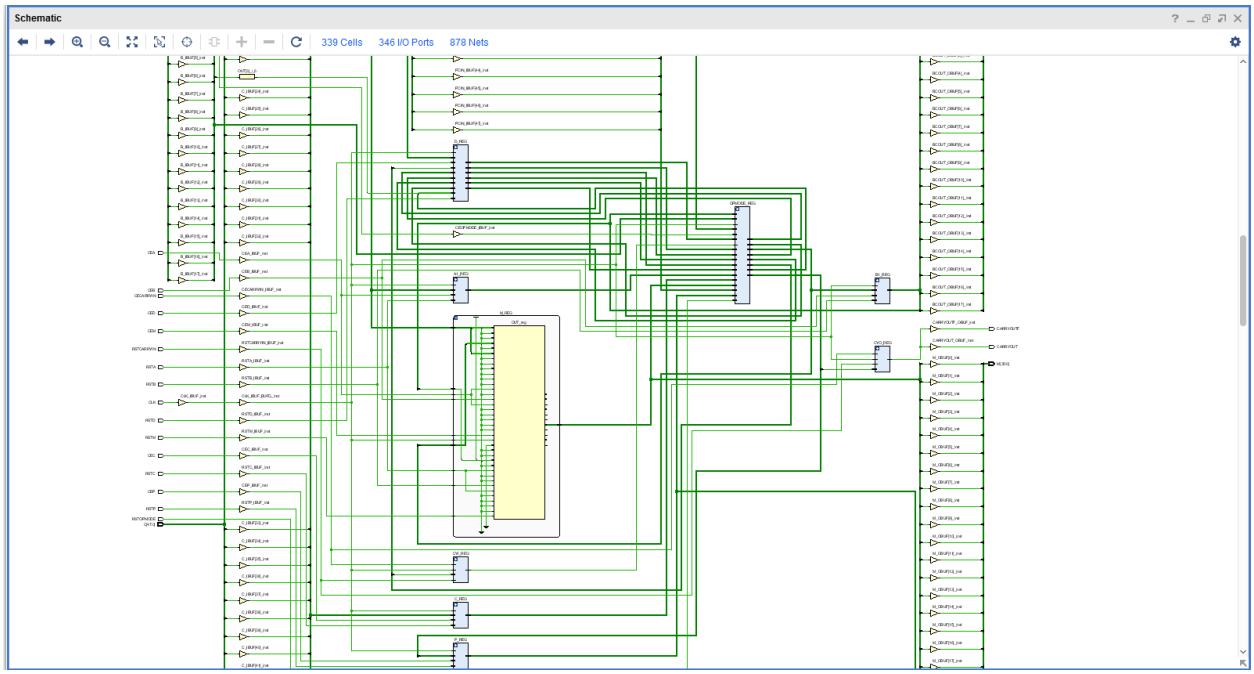


Resource	Utilization	Available	Utilization %
LUT	230	134600	0.17
FF	160	269200	0.06
DSP	1	740	0.14
IO	327	500	65.40

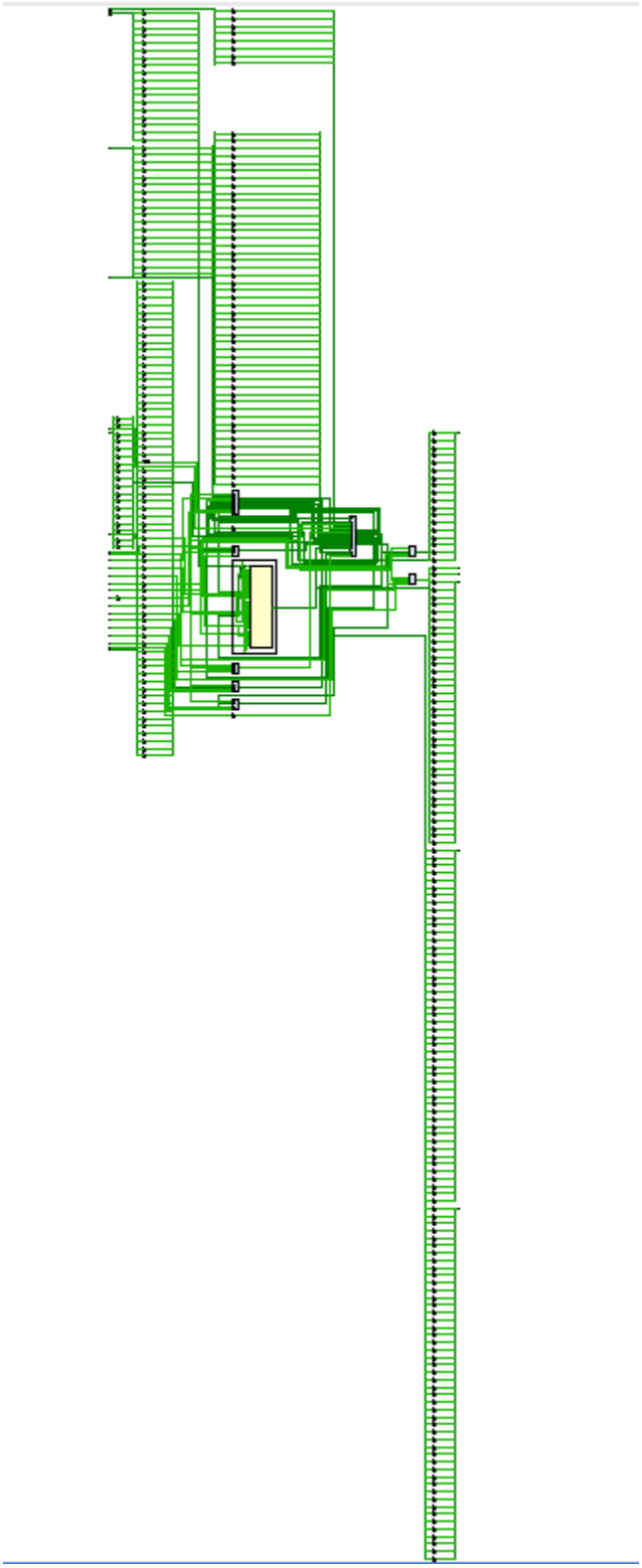
- Timing Summary after running synthesis.
- As shown in the snippet:
  - **Both setup time & hold time slacks are positive.**
  - **Which means that there no timing violations.**



- Schematic after running synthesis.



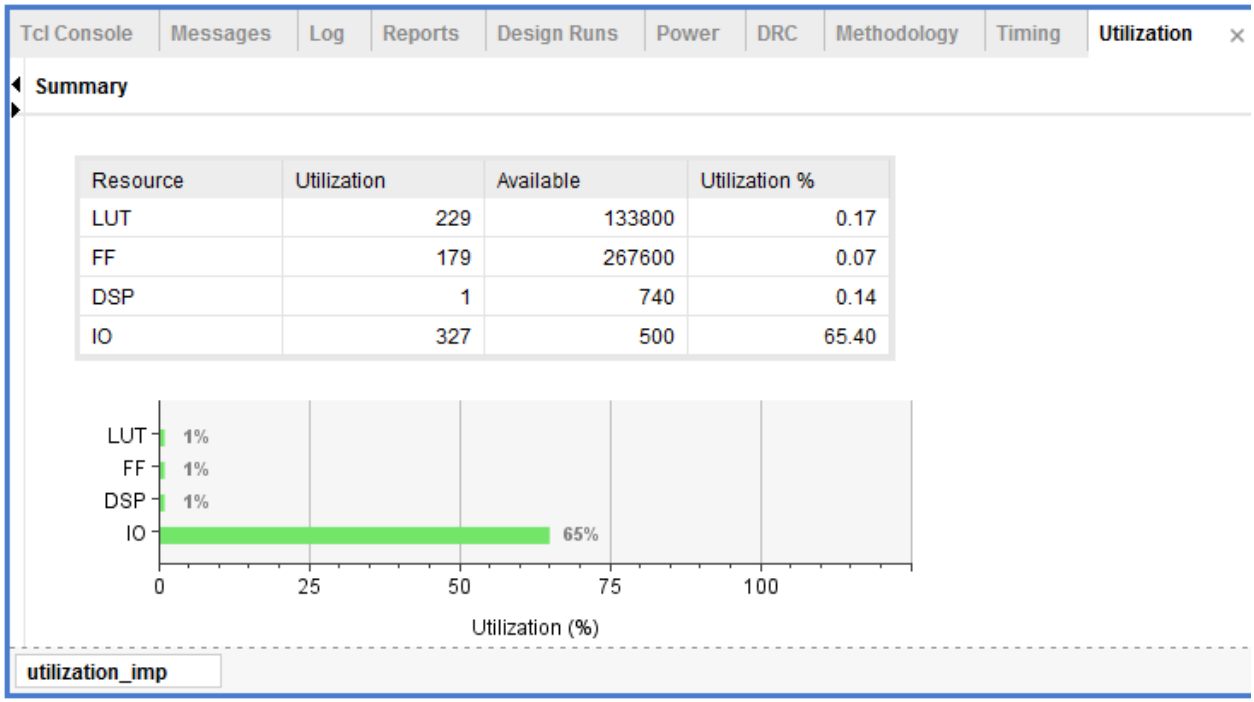
- Schematic after running synthesis (Zoomed Out).



Implementation

- Messages tab after running implementation.
- As shown in the snippet → **No critical warnings or errors**.

- Utilization after implementation.



Resource	Utilization	Available	Utilization %
LUT	229	133800	0.17
FF	179	267600	0.07
DSP	1	740	0.14
IO	327	500	65.40

- Timing Summary after implementation.
- As shown in the snippet:
  - **Both setup time & hold time slacks are positive.**
  - **Which means that there no timing violations.**

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.612 ns	Worst Hold Slack (WHS):	0.273 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	181

All user specified timing constraints are met.

Timing Summary - timing_imp

- Device snippet.