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PROJECT REPORT

CMPN301 Phase 1

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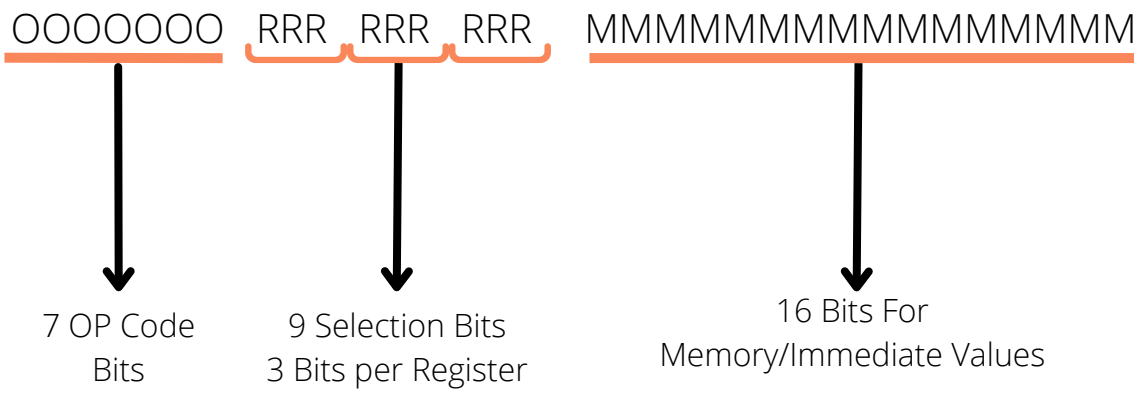
Instruction Format

Each Instruction is 32 bits, where the Last 16 bits are mainly used for memory addresses or Immediate values. 9 bits in the middle are used mainly for register selection and the first 7 bits are used to decode instructions.



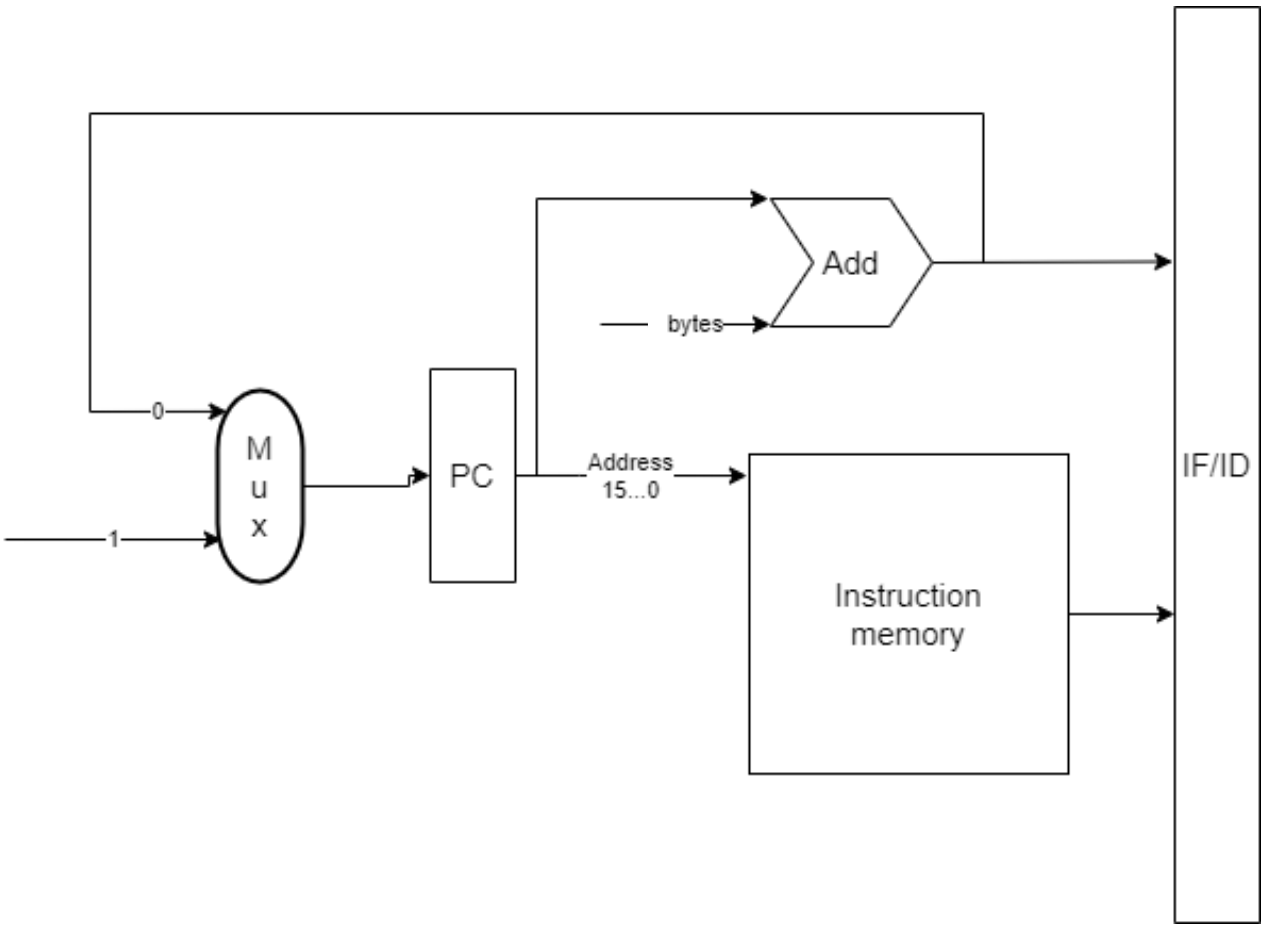
NO PROBLEMS OP CODE	00000XX	Rdst	Rsrc1	Rsrc2	Imm/Address
NOP	0000000	-	-	-	-
HLT	0000001	-	-	-	-
SETC	0000010	-	-	-	-
FULL FORWARDING OP CODES	01XXXXX				
NOT	0100000	RRR	-	-	-
INC	0100001	RRR	-	-	-
POP	0100010	RRR	-	-	-
IN	0100011	RRR	-	-	-
MOV	0100100	RRR	RRR	-	-
SWAP	0100101	RRR	RRR	-	-
ADD	0100110	RRR	RRR	RRR	-
SUB	0100111	RRR	RRR	RRR	-
AND	0101000	RRR	RRR	RRR	-
IADD	0101001	RRR	RRR	-	16bits

MEMORY (LOAD USE CASE)	1xxxxxx				
LDM	1000000	RRR	-	-	16bits
LDD	1000001	RRR	RRR	-	16bits
STD	1100000	-	RRR	RRR	16bits
OUT	1100001	-	-	-	-
PUSH	1100010	-	-	-	-
JZ	1100011	-	-	-	16bits
JN	1100100	-	-	-	16bits
JC	1100101	-	-	-	16bits
JMP	1100110	-	-	-	16bits
CALL	1100111	-	-	-	16bits
RET	1101000	-	-	-	-
INT	1101001	-	-	-	-
RTI	1101010	-	-	-	-

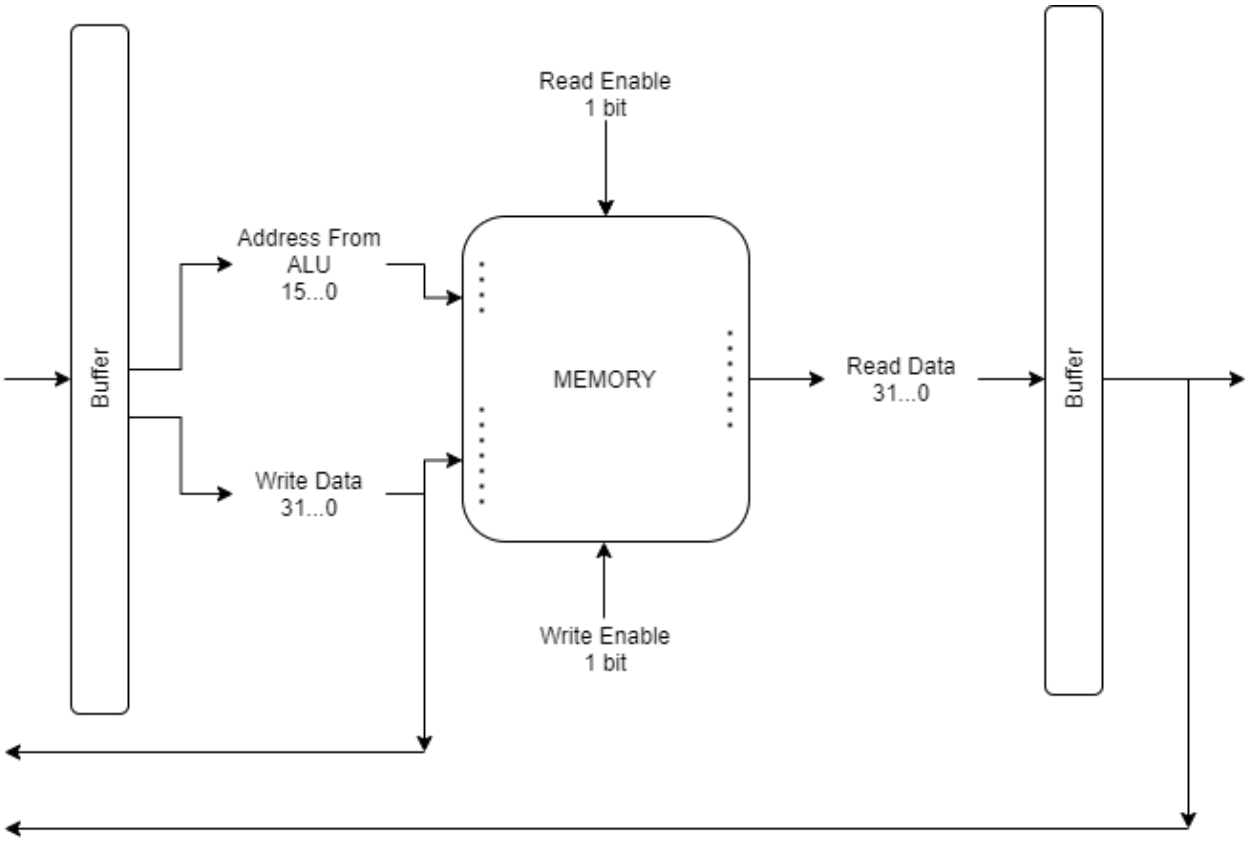
Schematics

BLOCKS, AND DATA-FLOW CONNECTIONS

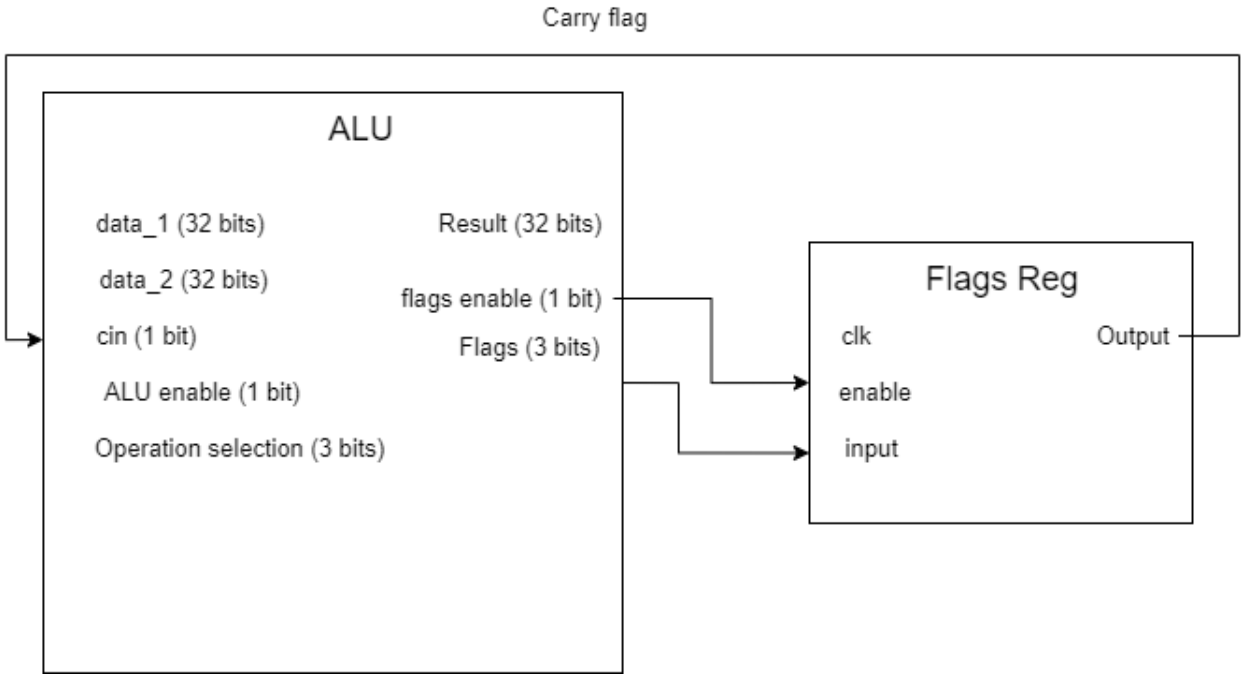
Fetching Instructions



MEMORY


Read Enable
1 bit
Address From
ALU
15...0
Buffer
MEMORY
Read Data
31...0
Buffer
Write Data
31...0
Write Enable
1 bit

ALU


Carry flag
ALU
data_1 (32 bits)
data_2 (32 bits)
cin (1 bit)
ALU enable (1 bit)
Operation selection (3 bits)
Result (32 bits)
flags enable (1 bit)
Flags (3 bits)
Flags Reg
clk
enable
input
Output

Control Unit

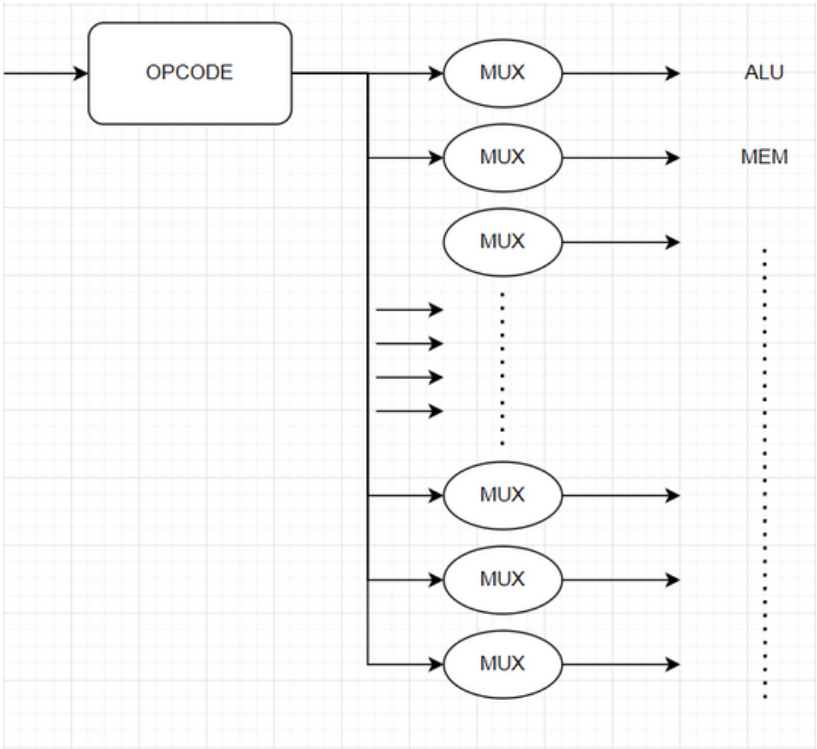
Examples of Control signals:

- Alu Enable
- Alu Operations
- Memory Read and write Enables
- Forwarding unit
- Write Back Selector
- Write Back Rdist decoder
- Register selector
- Buffers enable
- Buffers Hlt/reset
- branching mux
- in and out ports enables
- stack enables

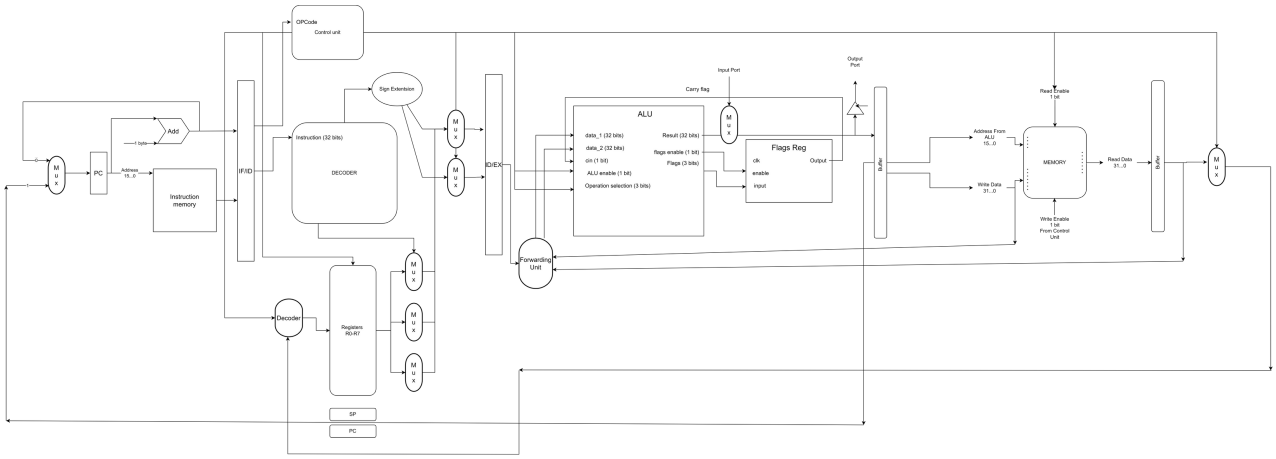
Control unit function:
The control unit checks the provided opcode when a certain opcode is found, corresponding enables are set, and so on. The Control unit also keeps track of the forwarding process and manages some of the hazards if detected.

Example:
AND Operation when detected, the control unit sends the anding operation to the ALU and sets enable to 1, this means that the Alu will AND its 2 operands.

Control Unit is a collection of multiplexers that depend on the OPCODE:



Full Connected Schematic



Pipeline Stages

REGISTER DETAILS AND HAZARDS

Pipeline hazard solutions:

- Full Data forwarding (alu and mem) is used alongside a forwarding unit.
- Static branch prediction is used (assuming Not Taken)
  - load new instructions until alu determine if the branch is taken or not
  - if not taken, continue
  - if taken, flush the pipe and jump to new instruction

Pipeline register details:

- IF/ID:
  - 32-bit instruction
  - 32-bit PC
- ID/EX:
  - 3-bit Rdst decoder
  - 32-bit Rsrc1
  - 32-bit Rsrc2
  - Control Signals
- EX/MEM
  - 32-bits Result
  - Control Signals
  - 32-bit Rsrc1
- MEM/WB
  - Control Signals (contains Rdst)
  - 32-bit ALU Result
  - 32-bit Mem Read