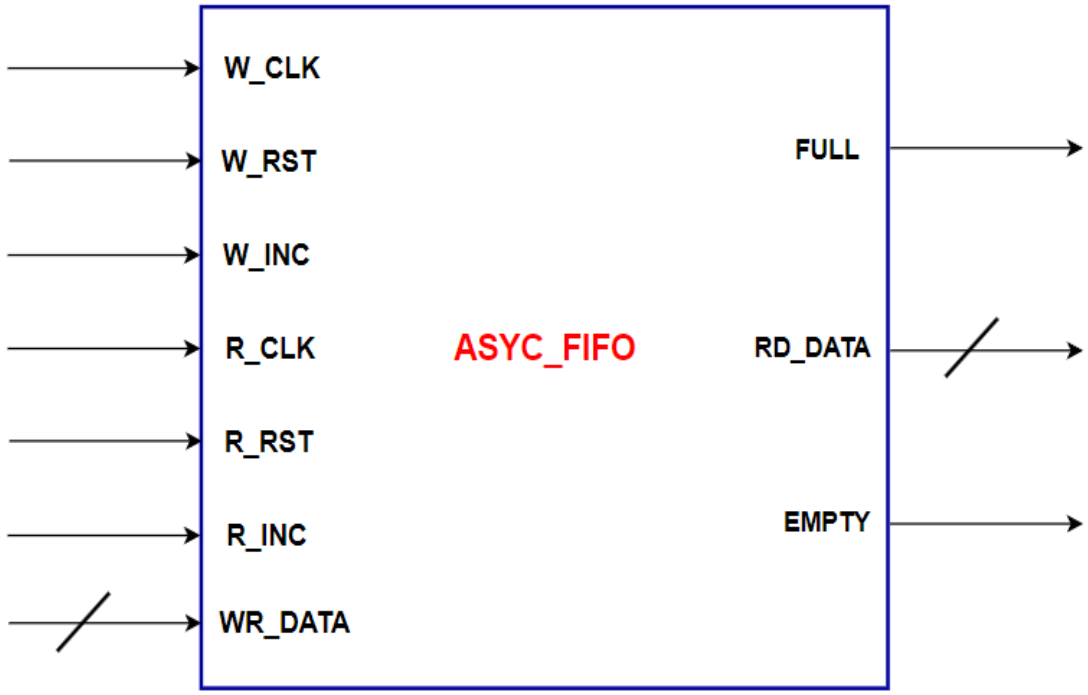
Asynchronous FIFO

Introduction: -

- **Asynchronous FIFO is a 2-port memory with certain depth.**
- **It has two clocks, one for read (i_rclk) and one for write (i_wclk).**
- **It has two addresses, one for read and one for write.**
- **Writing happens at location specified by write address.**
- **Reading happens at location specified by read address.**

Block Interface



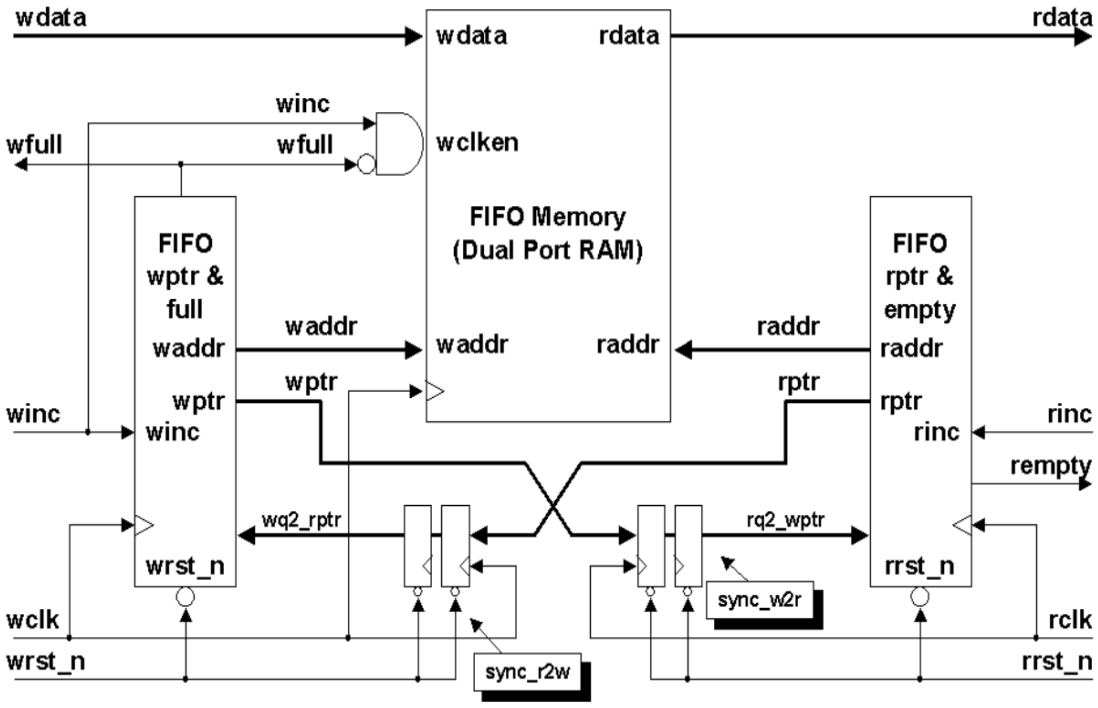
Ports Description

Signal Name	Description	Width
W_CLK	Source domain clock	1
W_RST	Source domain Async reset	1
W_INC	Write operation enable	1
R_CLK	Destination domain clock	1
R_RST	Destination domain Async reset	1
R_INC	Read operation enable	1
WR_DATA	Write Data Bus	Parameterized default (8-bits)
RD_DATA	Read Data Bus	Parameterized default (8-bits)
FULL	FIFO Buffer full flag	1
EMPTY	FIFO Buffer empty flag	1

Parameter Description

parameter Name	Description
DATA_WIDTH	Data Bus width

Block Diagram



Required

1. Write a Verilog Code for the above block diagram for the following blocks: -
    - FIFO_MEM_CNTRL (FIFO Buffer)
    - DF_SYNC.v (double flop synchronizer)
    - FIFO_WR (generate FIFO write address & FIFO full flag)
    - FIFO_RD (generate FIFO read address & FIFO empty flag)
    - ASYNC_FIFO (Top Module)

2. Write a testbench to validate the asynchronous FIFO operation with the following specifications: -
    - Reading frequency: 40 MHz
    - Writing frequency: 100 MHz
    - Writing Data Bytes: 9 Bytes
    - Calculate the FIFO Buffer depth to overcome data overflow