FSM Assignment

Q1) Construct a state diagram for detecting the sequence '101'

    For 4 cases:
1- Mealy overlapping
2- Moore overlapping
3- Mealy non-overlapping
4- Moore non-overlapping

✓ **Hand analysis in paper & The code that satisfies the cases above is needed and attach both in PDF**

Q2) Design a **Finite State Machine (FSM)** to control a simple vending machine. Your design should manage coin insertion, handle cancel requests and dispense items when sufficient coins have been inserted with **Gray Encoding**.

📌 Inputs:

Signal	Width	Description
clk	1 bit	Clock signal (positive edge triggered)
rst	1 bit	Active-high reset signal
coin_in	1 bit	High for one cycle when a coin is inserted
cancel	1 bit	High to cancel the current transaction
dispense	1 bit	High to request item dispensing

📌 Output:

Signal	Width	Description
Item_out	1 bit	Goes high for 1 cycle when an item is dispensed

🚦 States:

State	Description
IDLE	Ideal state & waiting for coins (coins <5)
READY	Enough coins received (After 5 coins), waiting for dispense signal
DISPENSE	Dispense item, then return to IDLE

💰 Coin Handling Rules:

- Need to create a coin counter to store a number of coins.
- One coin increases the coin count by 1.
- A total of **5 coins** is required to reach the READY state.
- The coin count should:
  - ✓ **Increment** only on coin pulses in IDLE.
  - ✓ **Reset** on cancel or after dispensing in DISPENSE.

⚠️ Notes:
- Write a testbench to validate your design using a 50 MHz clock frequency.

💡 **Hints:**

- Take care to avoid latch inference.
- You need to **store** the coin count, not only the current State.

Submission Guidelines:

- **The submitted file must be a PDF file.**
- **Name the file in the following format: StudentName_assignment5.pdf**
- **The PDF must include:**
  1- Screens of diagrams Paper (for Q1).
  2- Verilog design codes.
  3- Testbenches and the DO file.
  4- Waveform snippets from QuestaSim showing test results.

Deadline Time is Thursday, 1/5/2025 11:59 PM