

Tab 1



IEEE CAIRO UNIVERSITY SB



ieeecusb

# Digital Electronics Plan

2024-  
2025



**IEEE**

IEEE CAIRO UNIVERSITY  
STUDENT BRANCH

# Workshops Content

## *Digital Design workshop content plan*

This is the plan for the Digital Design workshop throughout the season.

### **Session 1 (introduction to Digital Electronics)**

1. Intro to Digital
2. Digital vs analog
3. Digital design flow
4. Gates and Tech. mapping
5. Break
6. Verilog basics
7. Start coding with Verilog
8. [Lab1](#)
9. [Lab2](#)

### **Session 2 (Combinational Circuits)**

1. Building code & code outlines
2. Comb. Logic
3. [Lab 1](#)
4. Behavioral modeling (always block)
5. If & case statements
6. [Lab 2](#)
7. Gate level & structural modeling
8. [Lab 3](#)
9. Recap and compare between styles

### **Session 3 (Sequential Circuits)**

1. Testbenches
2. Tasks and functions
3. [Lab 1](#)
4. Do file
5. Break
6. Intro to seq. logic
7. Seq. vs comb.
8. Basic storage elements (latches and FF)
9. Blocking vs non-blocking assignment
10. Synch. Vs Asynch.
11. Event queue
12. How to avoid unintentional latch
13. Race conditions
14. [Lab 2](#)

#### **Session 4 (Registers & Counters)**

1. Cont. Seq.
2. Registers & shift registers
3. Counters and their types
4. [Lab 1](#)
5. Break
6. Casex & Casez
7. Generate block
8. Local parameter
9. Testbenches for seq.
10. [Lab 2](#)

#### **Session 5 (FSM & STA)**

1. Revision on FSM types and states
2. Coding FSMs with Verilog
3. [Lab 1](#)
4. Break
5. STA (timing)
6. Linting techniques and linting tool errors

#### **Session 6 (Memories)**

1. Memory types
2. Coding memory with Verilog
3. Single port RAM
4. Double port RAM
5. [Lab 1](#)
6. FIFO
7. Break
8. FPGA Basics
9. FPGA flow using a tool
10. [Lab 2](#)

#### **Session 7 (Designing techniques)**

1. CDC
2. Power consumption and reduction techniques
3. Break
4. FPGA (design on the whole flow)
5. [Lab](#)