* Indicates required question

Questions

1) The main difference between Latch and Flip Flop is that Latch is ..... while Flip Flop is ..... * 5 points

- [x] Level triggered – Edge triggered.
- [ ] Edge triggered – Level triggered.
- [ ] Both are edge triggered.
- [ ] Both are level triggered.

2) If we want to Implement an Odd parity Checker with only one gate which one should we use? * 5 points

- [ ] XNOR.
- [ ] NOR.
- [ ] AND.
- [x] XOR.

Even: xnor

3) You can implement 8 to 1 * 5 points

- NOR.
- AND.
- XOR.

3) You can implement 8 to 1 MUX from ..... 2 to 1 MUXs * 5 points

- 4
- 5
- 6
- 7

2N→1Mux needs 3 N→1 Mux

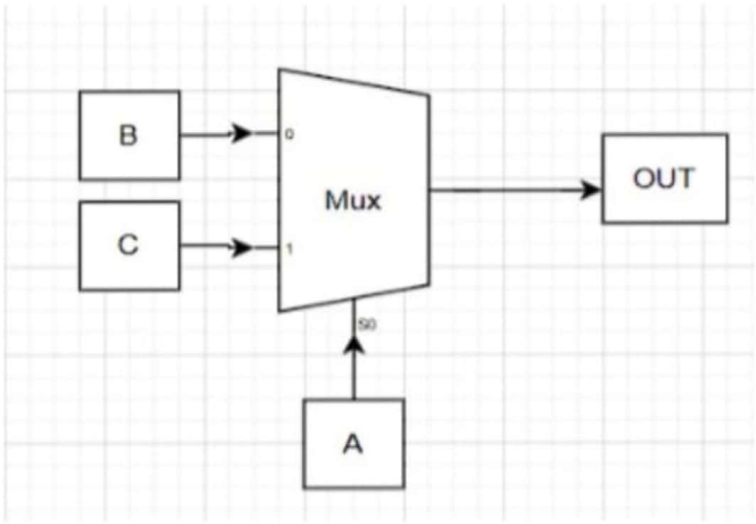
4) 3 stages Ripple counter divides the clock frequency by ..... * 5 points

- 2
- 4
- 8
- 16

2^3

5) Which of the following C++ * 5 points

5) Which of the following C++ statements describes the behavior of the figure: (assuming that A & B is 1 bit) * 5 points

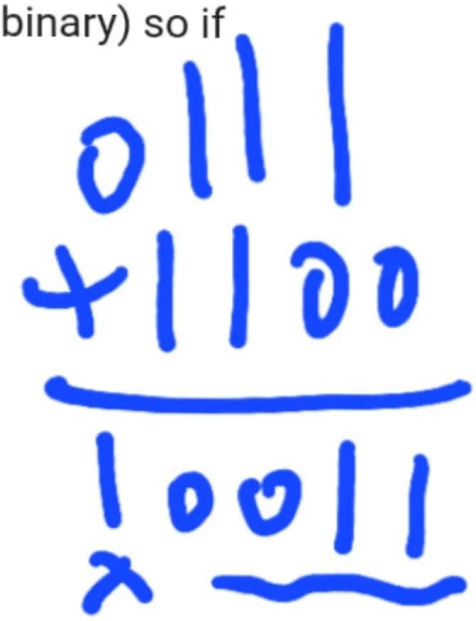


- [x] If(A==1) { Out =C; } else { Out=B; };
- [ ] If(B==1) { Out =C; } else { Out=A; };
- [ ] If(B==1) { Out =A; } else { Out=0; };
- [ ] If(A==1) { Out =C; };

6) Assuming that I have 2 signed 4bits number (the 4th bit is the sign) **A=0111** and **B=1100** (the signed number is in 2's complement representation) * 5 points

6) Assuming that I have 2 signed 4bits number (the 4th bit is the sign) **A=0111** and **B=1100** (the signed number is in 2's complement representation) (The values in binary) so if **C=A+B** * 5 points

- ○ 1001
- ● 0011
- ○ 1100
- ○ 1010



7) What's the implementation of Boolean Function as Sum of Products? * 5 points

- ○ Group of OR gates outputs into Single AND gate.
- ● Group of AND gates outputs into Single OR gate.
- ○ Group of XOR gate outputs into Single NAND gate.
- ○ None of the above

8) Which of the following is NOT a characteristic of a Moore finite state machine? * 5 points

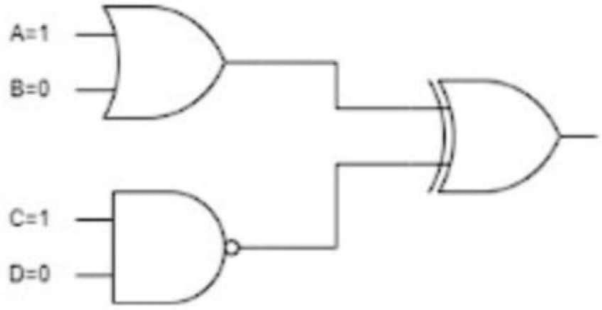
- [x] Output depends only on the current state.
- [ ] Output depends only on the current input.
- [ ] It has more states compared to a Mealy finite state machine.
- [ ] Output changes after the clock edge.

9) What is the purpose of a multiplexer (MUX) in digital design? * 5 points

- [x] To combine multiple signals into one
- [ ] To generate clock signals.
- [ ] To synchronize asynchronous signals.
- [ ] To store data temporarily.

10) What is the output for this combinational circuit : * 5 points

10) What is the output for this combinational circuit : * 5 points



- ○ z
- ○ 1
- ○ x
- ● 0

Mealy
- Faster
- Less states and smaller logic circuit
- Asynchronous Output

Moore
- More stable
- Synchronous Output
- Simpler

11) What is the advantage of Moore FSM over Mealy FSM for the same circuit functionality? * 5 points

- ○ Moore generates the output of the FSM faster than Mealy.
- ○ Moore needs a smaller number of states than that of Mealy.
- ● Moore is more stable compared to Mealy in terms of its output.
- ○ Moore takes smaller area implementation compared to Mealy.

12) For the following counter with a sequence of 0, then 5,7,9,1 and again back to 0 to repeat, State the minimum number of bits needed to design such FSM counter. * 5 points

- ○ 4
- ● 3
- ○ 2
- ○ 5

$\lceil Log(N) \rceil$

↳ 5

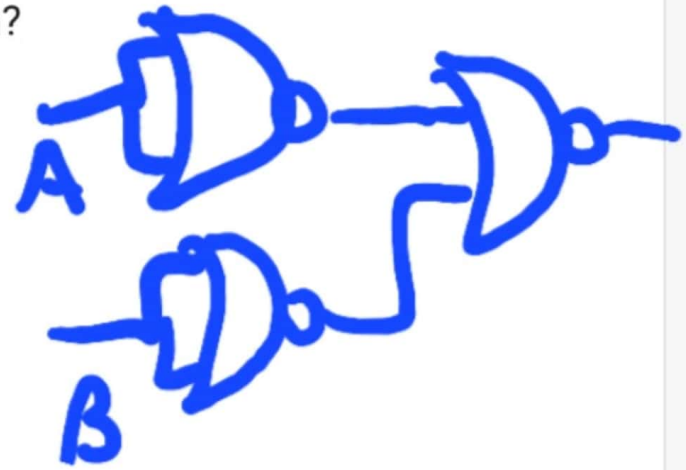
13) Write 2's complement for 100100 * 5 points

- ○ 101100
- ● 11100
- ○ 100111
- ○ 11011

14) What are the basic gates in MOS logic family? * 5 points

- [x] NAND and NOR
- [ ] AND and OR
- [ ] NAND and OR
- [ ] AND and NOR

15) How many NOR gates are required to obtain AND operation? * 5 points



- [ ] 1
- [ ] 2
- [x] 3
- [ ] 4

Back Submit Clear form