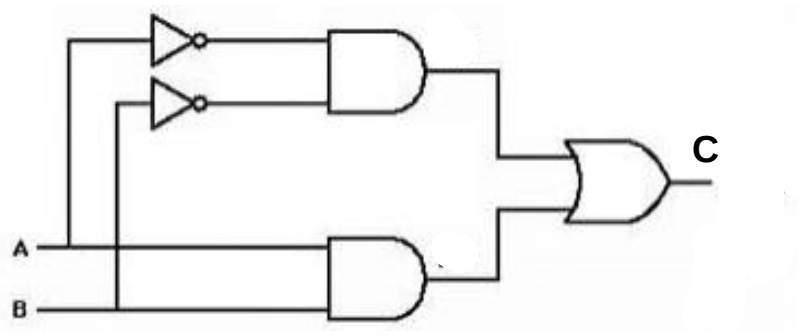
Assignment1

Q1) Schematic-to-Verilog:

Given the following schematic circuit of specific functionality, write a Verilog code to describe the circuit and comment on the functionality of the circuit:

input: A, B (1 bit)

output: C (1 bit)



Q2) Conditional Operator:

Given the following C++ if condition code, try to convert it into a Verilog code using condition operator given in session.

input: A (1 bit)

output: B (2 bit)

```
if (A)
    B=1;
else
    B=2;
```

Bonus question:

Try to execute this conditional Code:

input: A (2 bit), C (1 bit)

output: B (1 bit)

```
if (A==1)
    B=C;
else if(A==2)
    B=~C;
else
    B=0;
```

Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Assignment1 for example Ahmed_Abdellatif_Assignment1.

2) Snippets from the waveforms captured from QuestaSim (ModelSim) for the design with inputs assigned values and output values visible.