🧩 **Module: ESC_Serializer**

🔍 **Issue (from SpyGlass):**

1-Asynchronous reset RstN was used inconsistently—some flip-flops had reset, others didn't

(e.g.,TxDataEsc_reg), causing reset mismatch warnings.

2- checks inside sequential always block caused errors.

- Using counter == 0
- Using counter == 7

🛠️ **Fix:**

1-Added asynchronous reset to TxDataEsc_reg to ensure consistent reset behavior across all registers.

2- Replaced counter == 0 with (~|counter) (checks if all bits are zero).

Replaced counter == 7 with (&counter) (checks counter equals 7 by bits).

🧩 **Module: HS_Serializer**

🔍 **Issue (from SpyGlass):**

1-checks inside sequential always block caused errors..

- Using counter == 0
- Using counter == 6

🛠️ **Fix:**

Replaced counter == 0 with(~|counter) (checks if all bits are zero).

Replaced counter == 6 with (counter[2] & counter[1] & ~counter[0]) (checks counter equals 6 by bits).

🧩 **Module: Esc_Sequencer**

🔍 **Issue (from SpyGlass):**

1-checks inside sequential always block caused errors..

msg: Combinational and sequential parts of an FSM 'Esc_Sequencer.Count' described in same always block (59)

- Using counter == 7

🛠️ **Fix:**

Replaced counter == 7 with(&Count) (checks if all bits are one).

🧩 **Module: HS_Sequencer**

🔍 **Issue (from SpyGlass):**
1-checks inside sequential always block caused errors..

msg: Combinational and sequential parts of an FSM described in same always block (57)

- Using counter == 95

🛠️ **Fix:**
Replaced counter == 7 with((Count[6] && !Count[5] && Count[4] && Count[3] && Count[2] && Count[1] && Count[0])) (checks if all bits are 1011111).

🧩 **Module: FSM_TX**

🔍 **Issue (from SpyGlass):**
1- Missing default of case statement..

msg: Case statement does not have a default clause and is not preceded by assignment of target signal in combinational block[Hierarchy: ':cphy_tx_fsm']

🛠️ **Fix:**
Added a default state

🔍 **Issue (from SpyGlass):**
1- Small width..

msg: Constant 6'd89 will be truncated (918)

🛠️ **Fix:**
7’d89

🔍 **Issue (from SpyGlass):**
1- Multiple assignment..

msg: Signal Direction is being assigned multiple times (previous assignment at line 755) in same always block [Hierarchy: ':cphy_tx_fsm']

🛠️ **Fix:**
Removed the wrong one