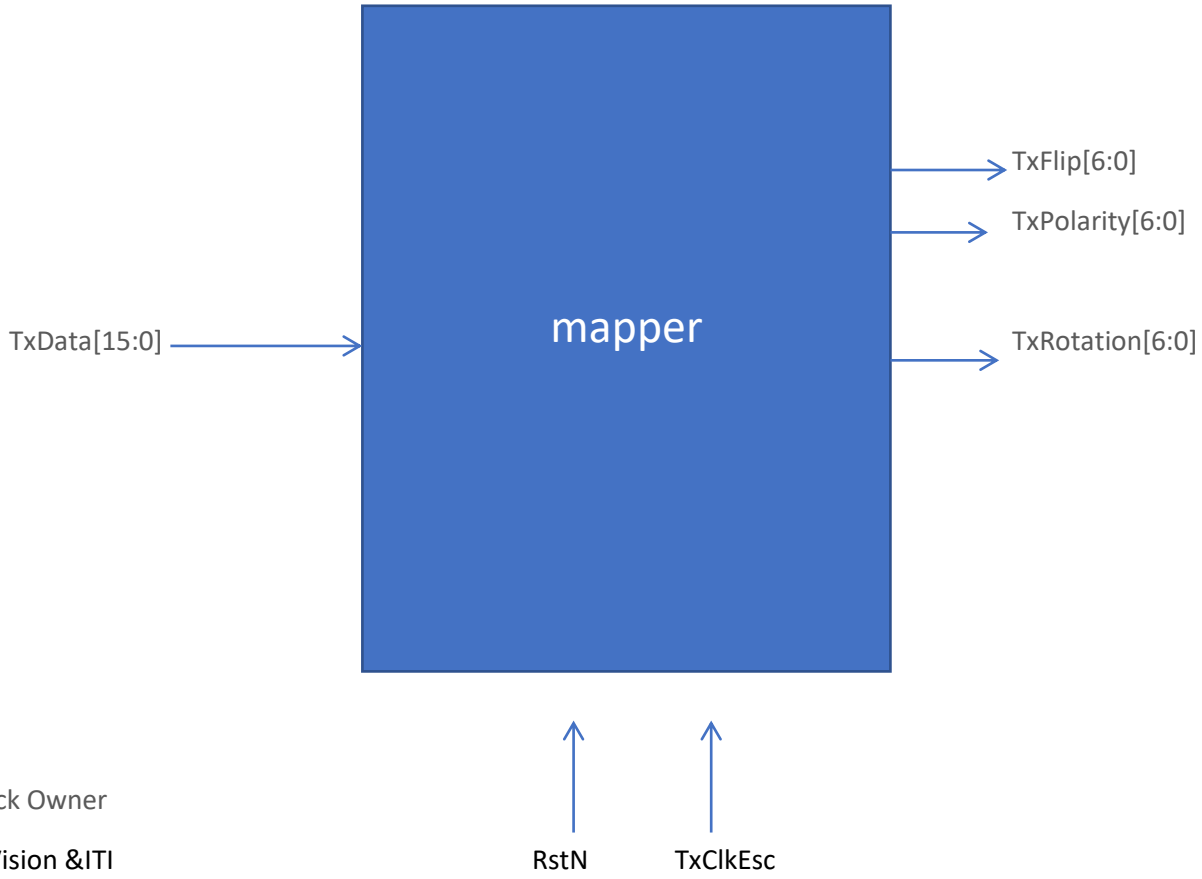
mapper

Induction Training

Version 1.0



Block Owner

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3 Operation and Description

3.1 Digital Interface

3.1.1 Parameters Names

Parameter Name	Default	Description
None		

3.1.2 Ports Names

Port Name	Port Width	Port Type	Description
TxData	16	Input	16-bit input data to be mapped
TxRotation	7	output	7-bit output rotation signal
TxPolarity	7	Output	7-bit output polarity signal
TxFlip	7	Output	7-bit output flip signal

3.2 Functional Description

The `mapper` block in the C-PHY design takes a 16-bit input data word (TxData) and maps it to three 7-bit output vectors: TxRotation, TxPolarity, and TxFlip. The mapping depends on the upper 6 bits of TxData, which determine how the input data is distributed across the output signals.This logic is used to prepare the data for the subsequent C-PHY encoding stages, ensuring the correct polarity, rotation, and flip pattern for each symbol period in the C-PHY interface.

4.1 Timing diagram