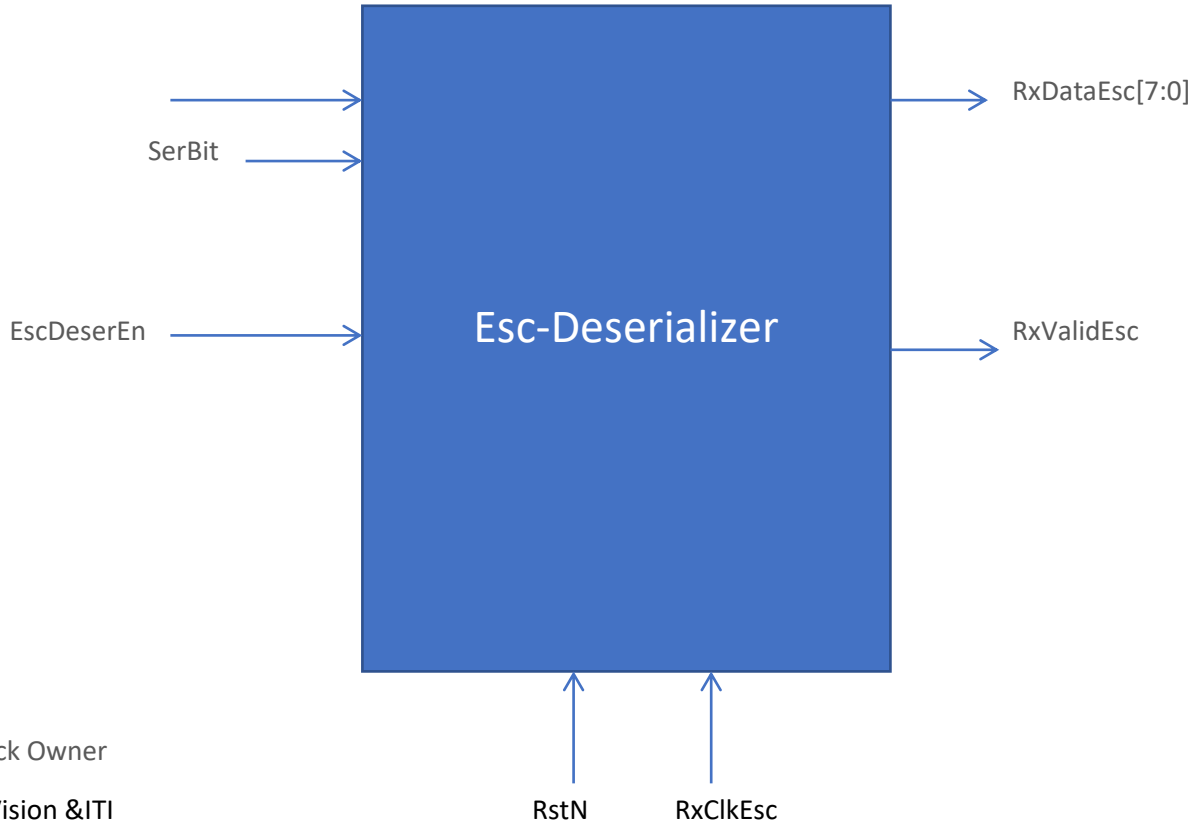
Esc-Deserializer

Induction Training

Version 1.0



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3.1 Digital Interface

3.1.1 Parameters Names

Parameter Name	Default	Description
None		

3.1.2 Ports Names

Port Name	Port Width	Port Type	Description
SerBit	1	Input	Incoming serial data bit (LSB first)
EscSerEn	1	Input	Enable signal
RstN	1	Input	Negative reset
RxClkEsc	1	Input	Clock
RxValidEsc	1	Output	Output flag indicating that RxEscData is valid (1 cycle pulse)
RxEscData	8	Output	8-bit parallel output of the deserialized byte

3.2 Functional Description

The `ESC_Deserializer` module converts a serial bit stream (LSB first) into parallel 8-bit data words in Escape mode reception of C-PHY. It samples incoming bits on the falling edge of the `RxClkEsc` clock and assembles them in a shift register. When a full byte is assembled, it outputs the byte (`RxEscData`) and asserts the `RxValidEsc` flag for one cycle to indicate that valid data is ready. The deserialization is gated by the `EscDeserEn` enable signal, and reset logic ensures proper alignment and initialization.

4.1 Timing diagram