SpyGlass Receiver

- **Clk_Gating**
  - InferLatch: Latch inferred

    always @(ClkIn or Enable) begin

    if (!ClkIn) begin

    LatchEn <= Enable;

    End

  ➔ Ignore this error as we already want this latch

- **Esc_Deserializer**
  - Sequential and combinational parts of an FSM description should be separated
    - ➢ Combinational and sequential parts of an FSM bit_count described in the same always block.

    if (bit_count==7) begin

    RxEscData <= {SerBit, shift_reg[6:0]};

  ➔ Solution:

    if (&(bit_count[2:0])) begin

    RxEscData <= {SerBit, shift_reg[6:0]};
  - ImproperRangeIndex-ML
    - ➢ Index ‘bit_count’ of width ‘4’ is larger than the width ‘3’ required for the max value ‘7’ of the signal ‘shift_reg’

    shift_reg[bit_count] <= SerBit;

  ➔ Solution:

reg [2:0] bit_count ; // 3-bit counter (0 to 7)

- Clock_check04: Flags usage of both edges in a design
  - ➢ Recommended edge (positive) of clock not used
    always @(negedge RxClkEsc or negedge RstN)

➔ Ignore this warning as we already need to check at the negedge.

- **Sequence_Detector**
  - Unequal length operands in bit wise logical/arithmetic/ternary/relational operator
    - ➢ For operator (^), left expression: 'symbol_count' width 4 should match right expression : 'saved_five' width 3.
      if (&(~(symbol_count ^ saved_five)))

➔ Solution:
reg [3:0] saved_five;

- **Word_Clock_Gen**
  - Design has a clock driving it on both edges
    always @(posedge SymClk or negedge RST)
    :
    always @(negedge SymClk or negedge RST)

➔ Ignore that error as we need to count the both edges in the design.

- **SlaveFSM**
  - Signal may be multiply assigned (beside initialization) in the same scope
    - ➢ Signal ‘nextState’ is being assigned multiple times in the same always block.

```
                    :
FORCE_RX: begin
        if (CtrlDecoderOut==2'b00) nextState= RX_STOP;
        else nextState = FORCE_RX;
    end
            default: nextState = RX_STOP;
        endcase
if (ForceTxStopmode) nextState = TX_STOP;
if (ForceRxmode) nextState = FORCE_RX;
end
```

➔ Solution:

```
if (ForceTxStopmode) nextState = TX_STOP;
else if (ForceRxmode) nextState = FORCE_RX;
else begin
   case (currentState)
      RX_STOP: begin
       if (CtrlDecoderOut == 2'b01) nextState = RX_HS_REQUEST;
                    :
                    :
```

  - NoFeedThrus-ML: Block should not contain feed-throughs
    - ➢ There is feed-through from input ‘HsClk’ to output ‘RxWordClkHs’

assign RxWordClkHS = HsCLK;

➔ Ignore this warning and the same warnings from the other signals.