Functional Design Specifications

Induction Training

Version 1.0

Block Owner

Si-Vision

Authors

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1 Table of Contents

1 Table of Contents 1
2 Revision History 2
3 Overview 3
4 Operation and Description 3
4.1 Digital Interface 3
4.1.1 Parameters Names 3
4.1.2 Ports Names 3
4.1.3 CDC Table 3
4.2 Functional Description 3
4.3 Timing Diagram 3
4.4 Verification Requirements 3

2 Revision History

Version	Date	Author(s)	Revision Notes	Owner Approval
1.0	1/6/2025	Youssef Ehab Nagy	Full block documentation	

3 Overview

The Decoder module implements the symbol decoding logic for the MIPI C-PHY receiver path. It translates transition sequences between two consecutive states (captured from the analog wire states) into 3-bit symbols, enabling the deserialization of the transmitted high-speed data. This decoding follows MIPI C-PHY v1.0 specification logic for rotation, Flip and polarity.

4 Operation and Description

4.1 Digital Interface

4.1.1 Parameters Names

Parameter Name	Default	Description
None	-	The module currently uses no parameters.

4.1.2 Ports Names

Port Name	Port Width	Port Type	Description
reset	1 bit	Input	Asynchronous active-low reset. Initializes internal state.
DecoderEn	1 bit	Input	Enables the decoding logic. When low, decoder is inactive and resets state.
RxSymbolClkHS	1 bit	Input	Clock signal used to sample state transitions; recovered from input data.
State	3 bits	Input	Current 3-wire digital representation from analog PHY input.
Sym	3 bits	Output	Decoded 3-bit symbol based on the transition from previous to current state.

4.1.3 CDC Table

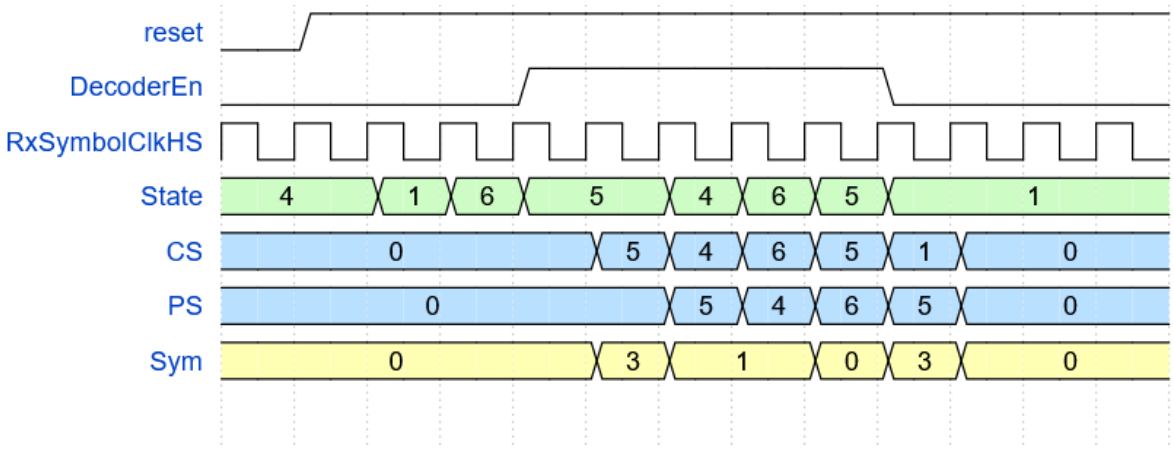
CDC signal	Source Domain	Destination Domain	Synchronization method
DecoderEn	RxClkFsm	RxSymbolClkHS	2-stage flip-flop synchronizer (outside this module)

4.2 Functional Description

The decoder operates on a stream of 3-bit states sampled at RxSymbolClkHS. It stores the current (CS) and previous (PS) states and compares them based on known transition patterns defined by the MIPI C-PHY protocol:

- Rotate CCW, Same Polarity: Sym = 000
- Rotate CCW, Opposite Polarity: Sym = 001
- Rotate CW, Same Polarity: Sym = 010
- Rotate CW, Opposite Polarity: Sym = 011
- Same Phase, Opposite Polarity: Sym = 100

4.3 Timing Diagram



4.4 Verification Requirements

The encoder was verified using a SystemVerilog testbench that includes the following assertions:

Assertion Name	**Description**
reset_output	Ensures the output Sym is 000 during asynchronous reset.
disabled_output	Ensures Sym is 000 when decoder is disabled (DecoderEn == 0).
valid_outputs_when_enabled	Checks that output Sym is one of the allowed legal values when enabled.
decoding_ccw_same	Verifies correct decoding when CS = {PS[1:0], PS[2]} (CCW, same polarity).
decoding_ccw_opposite	Verifies correct decoding when CS = ~{PS[1:0], PS[2]} (CCW, opposite).
decoding_cw_same	Verifies correct decoding when CS = {PS[0], PS[2:1]} (CW, same polarity).
decoding_cw_opposite	Verifies correct decoding when CS = ~{PS[0], PS[2:1]} (CW, opposite).
decoding_opposite_polarity	Verifies correct decoding when CS = ~PS (same phase, opposite polarity).

All assertions passed successfully during simulation.