Functional Design Specifications

Induction Training

Version 1.0

Block Owner

Si-Vision

Authors

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2 Revision History

Version	Date	Author(s)	Revision Notes	Owner Approval
1.0	1/6/2025	Youssef Ehab Nagy	Full block documentation	

3 Overview

The HS Sequencer module generates predefined 3-phase HS sequences—Preamble, Sync, and Post—required during the initialization of high-speed data transmission in a MIPI C-PHY v1.0 interface. It is controlled by an FSM using the HsSeqCtr field and HsSeqEn signal. The module outputs SeqSym values per symbol clock cycle and raises SeqDone when a sequence completes.

4 Operation and Description

4.1 Digital Interface

4.1.1 Parameters Names

Parameter Name	Default	Description
None	-	The module currently uses no parameters.

4.1.2 Ports Names

Port Name	Port Width	Port Type	Description
RstN	1 bit	Input	Active-low asynchronous reset.
HsSeqEn	1 bit	Input	Sequencer enable, allows sequence progression
TxSymbolClkHS	1 bit	Input	High-speed symbol clock
TxReqHS	1 bits	Input	Request to begin HS transmission, sets the default symbol.
HsSeqCtr	2 bits	input	Selects sequence phase: Pre (00), Sync (01), Post (10)
SeqDone	1 bits	Output	Indicates the selected sequence has finished
SeqSym	3 bits	Output	Current 3-bit symbol to be sent to encoder

4.1.3 CDC Table

CDC signal	Source Domain	Destination Domain	Synchronization method
HsSeqEn	TxWordClk	TxSymbolClkHS	2-stage flip-flop synchronizer (outside this module)
TxReqHS	TxWordClk	TxSymbolClkHS	2-stage flip-flop synchronizer (outside this module)
HsSeqCtr	TxWordClk	TxSymbolClkHS	2-stage flip-flop synchronizer (outside this module) (2-bits Gray code)
SeqDone	TxSymbolClkHS	TxWordClk	2-stage flip-flop synchronizer (outside this module)

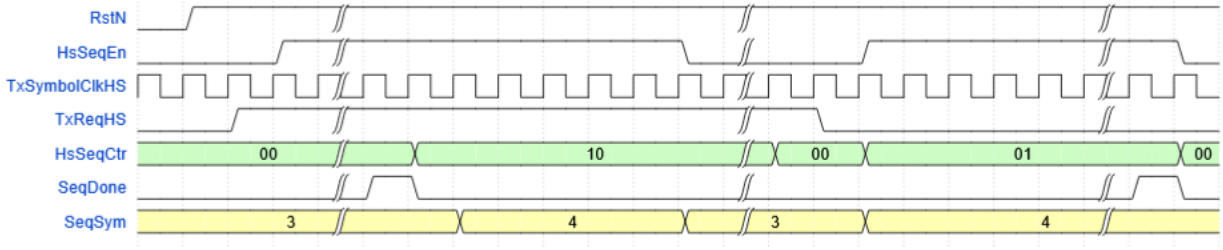
4.2 Functional Description

The sequencer responds to an enable signal and mode selector (HsSeqCtr) to issue one of three predefined 3-phase sequences:

- Preamble (00): Outputs 112 cycles of symbol 011. Ends with SeqDone = 1.
- Sync (01): Outputs a defined 7-cycle pattern: 011, five 100, then 011. Repeats per request.
- Post (10): Outputs 21 100 symbols. Ends with SeqDone = 1.

When not enabled (HsSeqEn = 0), the module drives a default symbol determined by TxReqHS: 011 if asserted, 100 otherwise. This avoids redundant symbols on the first enable pulse.

4.3 Timing Diagram



4.4 Verification Requirements

The functionality of the HS_Sequencer module is validated using SystemVerilog Assertions (SVA) within a testbench. Assertions cover timing of SeqDone for both the Preamble and Post sequences, with observed values compared against the expected symbol durations per the MIPI C-PHY v1.0 spec.

Assertion Name	Description
SeqDone_Preamble_assertion	Ensures SeqDone is asserted after 112 symbol cycles of preamble output (011)
SeqDone_Post_assertion	Ensures SeqDone is asserted after 21 100 symbols during the Post sequence.

All assertions passed successfully during simulation.