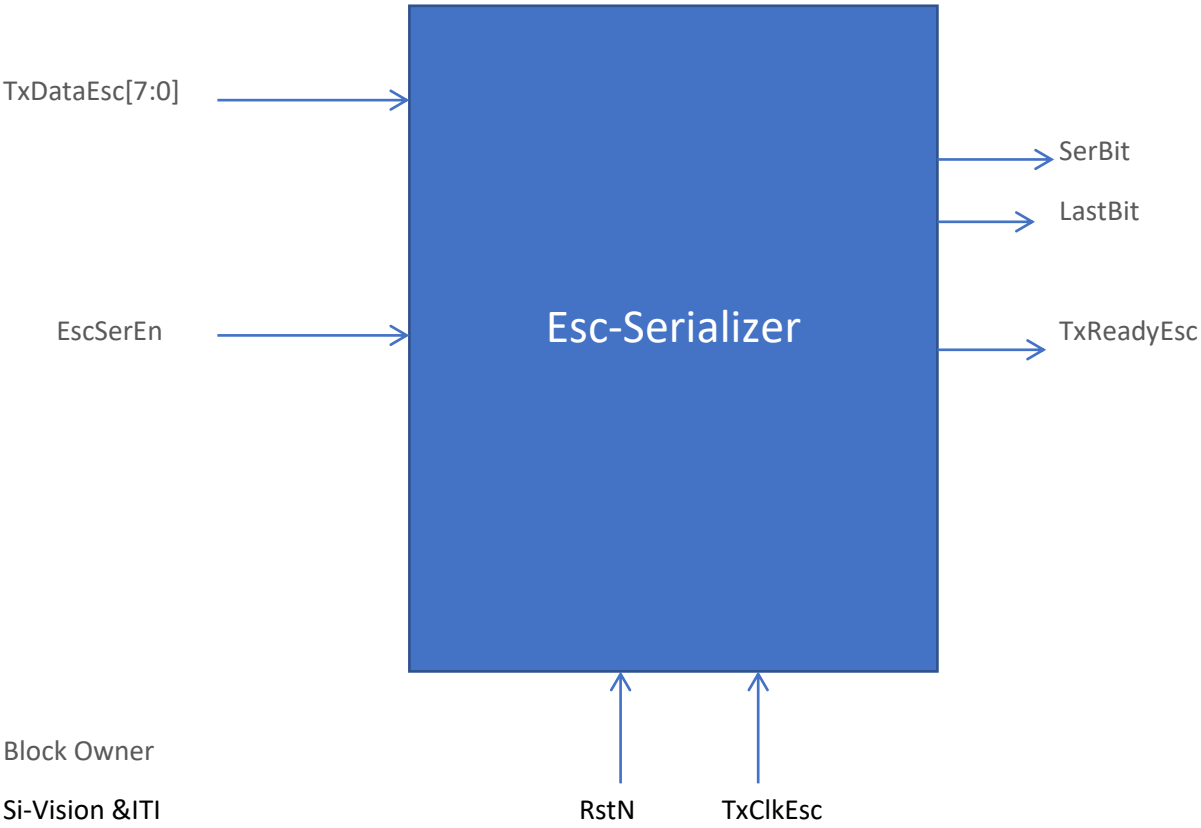
Esc-Serializer

Induction Training

Version 1.0



Block Owner

Si-Vision &ITI

Authors

<Ahmed Thabit>

This Page is left Blank Intentionally

1 Table of Contents

2 Overview

3 Operation and Description

3.1 Digital Interface

3.1.1 Parameters Names

Parameter Name	Default	Description
None		

3.1.2 Ports Names

Port Name	Port Width	Port Type	Description
TxDataEsc	8	Input	8-bit parallel data input to be serialized
EscSerEn	1	Input	Enable signal
RstN	1	Input	Negative reset
TxClkEsc	1	Input	Clock
SerBit	1	output	Serialized 1-bit output of the parallel input
LastBit	1	Output	Indicates that the last bit of the current byte is being transmitted
TxReadyEsc	1	Output	Indicates that the module is ready to accept new data

3.2 Functional Description

The `ESC_Serializer` block is responsible for serializing 8-bit parallel data during Escape (ESC) mode in C-PHY interfaces. It takes an 8-bit parallel input, loads it when enabled, and outputs serialized bits sequentially at each clock edge. The module also generates signals to indicate when it's ready for new data (`TxReadyEsc`) and when the last bit of the current byte is being transmitted (`LastBit`). This ensures synchronization of ESC mode data transmission between PHY layers.

4.1 Timing diagram