Functional Design Specifications

Induction Training

Version 1.0

Block Owner

Si-Vision

Authors

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2 Revision History

Version	Date	Author(s)	Revision Notes	Owner Approval
1.0	1/6/2025	Youssef Ehab Nagy	Full block documentation	

3 Overview

The Encoder block is responsible for converting a 3-bit input symbol into 3-phase encoded outputs (A, B, and C) according to the MIPI C-PHY v1.0 specification. Each phase output is represented by two digital control signals: PU (pull-up) and PD (pull-down), which interface with analog driver circuitry to produce the required voltages (VDD, GND, or 0.5*VDD). The encoder generates valid 3-phase signaling states (X+, X−, Y+, Y−, Z+, Z−) and transitions between them based on (input symbols) clockwise or counter-clockwise rotation, with or without polarity inversion.

4 Operation and Description

4.1 Digital Interface

4.1.1 Parameters Names

Parameter Name	Default	Description
None	-	The module currently uses no parameters.

4.1.2 Ports Names

Port Name	Port Width	Port Type	Description
RstN	1 bit	Input	Active-low asynchronous reset. Initializes encoder to state (X+), and drives GND on all wires.
EncoderEn	1 bit	Input	Encoder enable signal. Must be high for encoding to occur; otherwise, outputs remain in a safe idle state.
TxSymbolClkHS	1 bit	Input	High-speed symbol clock. All state transitions occur on its rising edge.
Sym	3 bits	Input	Encoded symbol input determining the rotation, Flip and polarity of the next output state.
A	2 bits	Output	A output control signal: {PU_A, PD_A}
B	2 bits	Output	B output control signal: {PU_B, PD_B}
C	2 bits	Output	C output control signal: {PU_C, PD_C}

4.1.3 CDC Table

CDC signal	Source Domain	Destination Domain	Synchronization method
EncoderEn	TxWordClk	TxSymbolClkHS	2-stage flip-flop synchronizer (outside this module)

4.2 Functional Description

Upon system reset (`RstN = 0`), the encoder enters a safe idle state (X+), where all outputs A, B, C drives wires with GND to avoid short circuit currents.

When EncoderEn = 1, and at each rising edge of TxSymbolClkHS, the encoder:

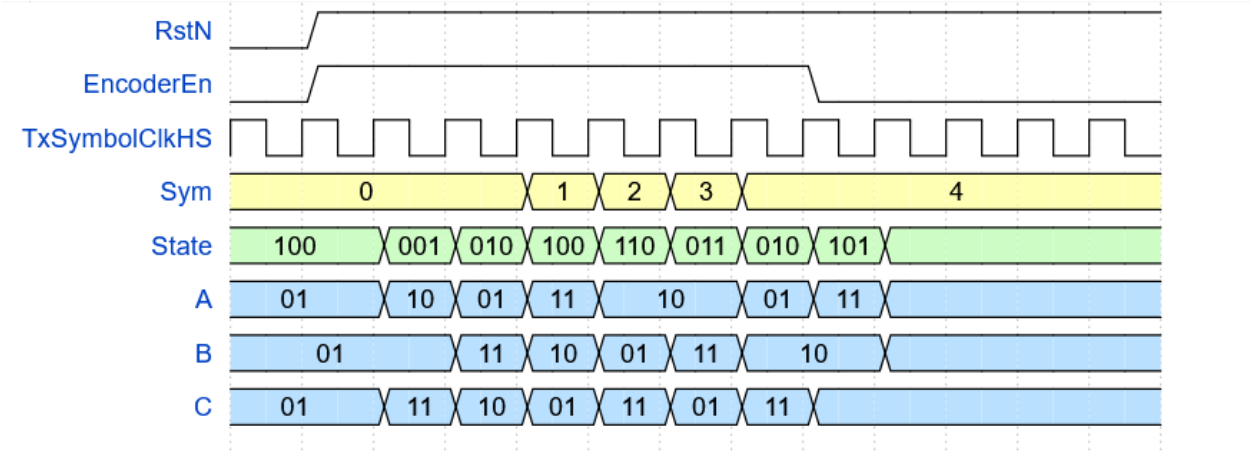
- Evaluates the 3-bit symbol Sym to determine the next valid 3-phase state.
- Determine wether to change current state polarity or rotate.
- Determines whether to rotate the state clockwise (CW) or counter-clockwise (CCW).
- Optionally inverts the polarity of the output state.

The output signals A, B, and C are each composed of {PU, PD} control bits and are used to drive analog MOSFETs. The logic is:

- PU=1, PD=0 → Drive VDD
- PU=0, PD=1 → Drive GND
- PU=1, PD=1 → Drive 0.5*VDD

If EncoderEn is low or a reset is asserted, outputs are forced to {PU=0, PD=1}, corresponding to GND. This guarantees electrical safety on analog lines.

4.3 Timing Diagram



4.4 Verification Requirements

The encoder was verified using a SystemVerilog testbench that includes the following assertions:

Assertion Name	Description
safe_outputs_when_reset	Ensures that when RstN = 0, all outputs drive GND (PU=0, PD=1).
safe_outputs_when_disabled	Ensures that when EncoderEn = 0, outputs remain safe and idle.
valid_outputs_when_enabled	Ensures that when EncoderEn = 1, outputs cycle through only the six valid states (X+/X−/Y+/Y−/Z+/Z−).

The testbench covers all eight possible input symbols, testing clockwise/CCW rotations with or without polarity inversion.

All assertions passed successfully during simulation.