

# REPORT CACHE SIMULATOR

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Course: Computer Organization and Assembly Language

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# Description:

The implementation is a **cache simulator** that supports both **unified** and **split cache configurations**, simulating instruction and data accesses separately when configured as split caches (bonus feature). The simulator processes an input file containing memory access sequences in hexadecimal format, simulates cache behavior, and outputs detailed logs of each access.

Key functionalities of the simulator include:

- Cache Type Support: Allows users to choose between a unified or split cache configuration.
- **Flexible Parameters**: Accepts user-defined memory size, cache size, line size, and access time for customization.
- Per-Access Logs: Outputs detailed logs for every memory access, including whether it resulted in a hit or a miss, the calculated index, and tag values (in binary format).
- Performance Statistics: At the end of the simulation, the program outputs the
  cache's final state, hit and miss ratios, total clock cycles, and the Average Memory
  Access Time (AMAT).
- **Bonus Feature**: Implements separate caches for instructions and data in the split cache mode, with independent hit/miss tracking and statistics.

# Decision and assumptions:

- The simulator supports both **unified** and **split cache configurations**.
- Binary output for index and tag

# Bugs and Issues:

- The program has no issues or bugs at the time we are submitting this file

#### **User Guide:**

- You will run the program and then you will have to fill the following

```
Choose cache type (1 = Unified, 2 = Split): 2
Enter memory size in bits (16 to 40): 32
Enter memory access time in clock cycles (50 to 200): 100
Enter cache access time in clock cycles (1 to 10): 5
Enter cache size in bytes: 80
Enter line size in bytes: 30
Enter the file name for instruction access sequence: "C:\\Users\\youss\\Downloads\\test_case_1.txt"
Enter the file name for data access sequence: "C:\\Users\\youss\\Downloads\\test_case_2.txt"
```

You have to choose either you want separate chaches for instruction and data or not,

Then choose memory size, access time for chache and memory, chache size, line size, then insert the path for text file for the instruction and data access sequences

The text files in this cases included the following:

#### Test case 1:

# A,B,C,D,E,F,10,11,12,13,A,B,C,D,E,F,10,11,12,13

# Test case 2:

6f1,8c5,b07,8b2,8b2,7c3,46c,385,889,43e,fb6,c4,939,bf1,cd,faf,908,bcb,10,4a

# Output:

First you will get the updates after each access in the instruction set:

```
Processing Instruction Cache Accesses...
Access: MISS
Total Hits: 0, Total Misses: 1, Total Accesses: 1
Access: HIT
Total Hits: 1, Total Misses: 1, Total Accesses: 2
Access: HIT
Total Hits: 2, Total Misses: 1, Total Accesses: 3
Access: HIT
Total Hits: 3, Total Misses: 1, Total Accesses: 4
Access: HIT
Total Hits: 4, Total Misses: 1, Total Accesses: 5
Access: HIT
Total Hits: 5, Total Misses: 1, Total Accesses: 6
Access: HIT
Total Hits: 6, Total Misses: 1, Total Accesses: 7
Total Hits: 7, Total Misses: 1, Total Accesses: 8
Access: HIT
Total Hits: 8, Total Misses: 1, Total Accesses: 9
```

```
Access: HIT
Total Hits: 9, Total Misses: 1, Total Accesses: 10
Access: HIT
Total Hits: 10, Total Misses: 1, Total Accesses: 11
Access: HIT
Total Hits: 11, Total Misses: 1, Total Accesses: 12
Access: HIT
Total Hits: 12, Total Misses: 1, Total Accesses: 13
Access: HIT
Total Hits: 13, Total Misses: 1, Total Accesses: 14
Access: HIT
Total Hits: 14, Total Misses: 1, Total Accesses: 15
Access: HIT
Total Hits: 15, Total Misses: 1, Total Accesses: 16
Access: HIT
Total Hits: 16, Total Misses: 1, Total Accesses: 17
Access: HIT
Total Hits: 17, Total Misses: 1, Total Accesses: 18
```

Then the data access updates:

```
Processing Data Cache Accesses...
Access: MISS
Tag: 27 (binary: 00000000000000000000000000011011)
Total Hits: 0, Total Misses: 1, Total Accesses: 1
Access: MISS
Tag: 35 (binary: 000000000000000000000000000100011)
Total Hits: 0, Total Misses: 2, Total Accesses: 2
Access: MISS
Tag: 44 (binary: 000000000000000000000000000101100)
Total Hits: 0, Total Misses: 3, Total Accesses: 3
Access: MISS
Total Hits: 0, Total Misses: 4, Total Accesses: 4
Access: HIT
Total Hits: 1, Total Misses: 4, Total Accesses: 5
Access: MISS
Tag: 31 (binary: 00000000000000000000000000011111)
Total Hits: 1, Total Misses: 5, Total Accesses: 6
Access: MISS
Tag: 17 (binary: 00000000000000000000000000001)
Total Hits: 1, Total Misses: 6, Total Accesses: 7
Access: MISS
Tag: 14 (binary: 00000000000000000000000000001110)
Total Hits: 1, Total Misses: 7, Total Accesses: 8
Access: MISS
Total Hits: 1, Total Misses: 8, Total Accesses: 9
```

```
Access: MISS
Total Hits: 1, Total Misses: 9, Total Accesses: 10
Access: MISS
Tag: 62 (binary: 00000000000000000000000000111110)
Total Hits: 1, Total Misses: 10, Total Accesses: 11
Access: MISS
Total Hits: 1, Total Misses: 11, Total Accesses: 12
Access: MISS
Total Hits: 1, Total Misses: 12, Total Accesses: 13
Access: MISS
Tag: 47 (binary: 00000000000000000000000000101111)
Total Hits: 1, Total Misses: 13, Total Accesses: 14
Access: HIT
Total Hits: 2, Total Misses: 13, Total Accesses: 15
Access: MISS
Tag: 62 (binary: 00000000000000000000000000111110)
Total Hits: 2, Total Misses: 14, Total Accesses: 16
Access: MISS
Total Hits: 2, Total Misses: 15, Total Accesses: 17
Access: MISS
Tag: 47 (binary: 00000000000000000000000001111)
Total Hits: 2, Total Misses: 16, Total Accesses: 18
```

The data provided in both are following the criteria specified in the report

Then the output after all access are done for both caches:

```
Instruction Cache State:
Final Cache State:
Index (bits) Valid Tag (bits)
               0
       0
               000000000000000000000000000
Final Statistics:
Hit Ratio: 0.95
Miss Ratio: 0.05
AMAT (Average Memory Access Time): 10 cycles
Total Clock Cycles: 200
Data Cache State:
Final Cache State:
Index (bits) Valid Tag (bits)
               00000000000000000000111110
Final Statistics:
Hit Ratio: 0.1
Miss Ratio: 0.9
AMAT (Average Memory Access Time): 95 cycles
Total Clock Cycles: 1900
```

#### Testing:

For the testing we used 3 20-access sequences to test our system;

Note: to show each test case individually I will use one single cache for instructions and data

#### Test case 1:

```
Choose cache type (1 = Unified, 2 = Split): 1
Enter memory size in bits (16 to 40): 32
Enter memory access time in clock cycles (50 to 200): 100
Enter cache access time in clock cycles (1 to 10): 10
Enter cache size in bytes: 1A0
Enter line size in bytes: 79
Enter the file name containing unified memory access sequence: "C:\\Users\\youss\\Downloads\\test_case_1.txt"
```

```
A,B,C,D,E,F,10,11,12,13,A,B,C,D,E,F,10,11,12,13
```

Output for test case 1:

```
Processing Unified Cache Accesses...
Access: MISS
Total Hits: 0, Total Misses: 1, Total Accesses: 1
Access: HIT
Total Hits: 1, Total Misses: 1, Total Accesses: 2
Access: HIT
Total Hits: 2, Total Misses: 1, Total Accesses: 3
Access: HIT
Total Hits: 3, Total Misses: 1, Total Accesses: 4
Access: HIT
Total Hits: 4, Total Misses: 1, Total Accesses: 5
Access: HIT
Total Hits: 6, Total Misses: 1, Total Accesses: 7
Access: HIT
Total Hits: 7, Total Misses: 1, Total Accesses: 8
Access: HIT
Total Hits: 8, Total Misses: 1, Total Accesses: 9
```

```
Access: HIT
Total Hits: 9, Total Misses: 1, Total Accesses: 10
Access: HIT
Total Hits: 10, Total Misses: 1, Total Accesses: 11
Access: HIT
Total Hits: 11, Total Misses: 1, Total Accesses: 12
Access: HIT
Total Hits: 12, Total Misses: 1, Total Accesses: 13
Access: HIT
Total Hits: 13, Total Misses: 1, Total Accesses: 14
Access: HIT
Total Hits: 14, Total Misses: 1, Total Accesses: 15
Access: HIT
Total Hits: 15, Total Misses: 1, Total Accesses: 16
Access: HIT
Total Hits: 16, Total Misses: 1, Total Accesses: 17
Access: HIT
```

```
Access: HIT
Total Hits: 18, Total Misses: 1, Total Accesses: 19
Access: HIT
Total Hits: 19, Total Misses: 1, Total Accesses: 20
Final Cache State:
Index (bits)
        Valid
            Tag (bits)
        0
        0
        Final Statistics:
Hit Ratio: 0.95
Miss Ratio: 0.05
AMAT (Average Memory Access Time): 15 cycles
Total Clock Cycles: 300
```

#### Test case 2:

```
Choose cache type (1 = Unified, 2 = Split): 1
Enter memory size in bits (16 to 40): 16
Enter memory access time in clock cycles (50 to 200): 150
Enter cache access time in clock cycles (1 to 10): 8
Enter cache size in bytes: 56
Enter line size in bytes: 32
Enter the file name containing unified memory access sequence: "C:\\Users\\youss\\Downloads\\test_case_2.txt"
```

```
6f1,8c5,b07,8b2,8b2,7c3,46c,385,889,43e,fb6,c4,939,bf1,cd,faf,908,bcb,10,4a
```

#### Output for test case 2:

```
Processing Unified Cache Accesses...
Access: MISS
Tag: 55 (binary: 00000000000000000000000000110111)
Total Hits: 0, Total Misses: 1, Total Accesses: 1
Access: MISS
Tag: 70 (binary: 00000000000000000000000001000110)
Total Hits: 0, Total Misses: 2, Total Accesses: 2
Access: MISS
Total Hits: 0, Total Misses: 3, Total Accesses: 3
Access: MISS
Tag: 69 (binary: 000000000000000000000000001000101)
Total Hits: 0, Total Misses: 4, Total Accesses: 4
Access: HIT
Total Hits: 1, Total Misses: 4, Total Accesses: 5
Access: MISS
Tag: 62 (binary: 00000000000000000000000000111110)
Total Hits: 1, Total Misses: 5, Total Accesses: 6
Access: MISS
Tag: 35 (binary: 00000000000000000000000000011)
Total Hits: 1, Total Misses: 6, Total Accesses: 7
Access: MISS
Tag: 28 (binary: 00000000000000000000000000011100)
Total Hits: 1, Total Misses: 7, Total Accesses: 8
Access: MISS
Total Hits: 1, Total Misses: 8, Total Accesses: 9
```

```
Access: MISS
Total Hits: 1, Total Misses: 9, Total Accesses: 10
Access: MISS
Tag: 125 (binary: 0000000000000000000000001111101)
Total Hits: 1, Total Misses: 10, Total Accesses: 11
Access: MISS
Total Hits: 1, Total Misses: 11, Total Accesses: 12
Access: MISS
Total Hits: 1, Total Misses: 12, Total Accesses: 13
Access: MISS
Tag: 95 (binary: 0000000000000000000000001011111)
Total Hits: 1, Total Misses: 13, Total Accesses: 14
Access: MISS
Tag: 6 (binary: 0000000000000000000000000000110)
Total Hits: 1, Total Misses: 14, Total Accesses: 15
Access: MISS
Tag: 125 (binary: 0000000000000000000000001111101)
Total Hits: 1, Total Misses: 15, Total Accesses: 16
Access: MISS
Total Hits: 1, Total Misses: 16, Total Accesses: 17
Access: MISS
Tag: 94 (binary: 0000000000000000000000001011110)
Total Hits: 1, Total Misses: 17, Total Accesses: 18
```

```
Access: MISS
Total Hits: 1, Total Misses: 18, Total Accesses: 19
Access: MISS
Total Hits: 1, Total Misses: 19, Total Accesses: 20
Final Cache State:
Index (bits) Valid
              Tag (bits)
         00000000010
Final Statistics:
Hit Ratio: 0.05
Miss Ratio: 0.95
AMAT (Average Memory Access Time): 150.5 cycles
Total Clock Cycles: 3010
```

#### Test case 3:

```
Choose cache type (1 = Unified, 2 = Split): 1
Enter memory size in bits (16 to 40): 32
Enter memory access time in clock cycles (50 to 200): 50
Enter cache access time in clock cycles (1 to 10): 5
Enter cache size in bytes: 80
Enter line size in bytes: 80
Enter the file name containing unified memory access sequence: "C:\\Users\\youss\\Downloads\\test_case_3.txt"
```

777,37,565,13b,35e,ef,1ae,2d3,4b7,715,d2,134,7dd,8ce,79e,190,d43,7e,777,609

Output for test case 3:

```
Processing Unified Cache Accesses...
Access: MISS
Tag: 14 (binary: 0000000000000000000000000001110)
Total Hits: 0, Total Misses: 1, Total Accesses: 1
Access: MISS
Total Hits: 0, Total Misses: 2, Total Accesses: 2
Access: MISS
Total Hits: 0, Total Misses: 3, Total Accesses: 3
Access: MISS
Total Hits: 0, Total Misses: 4, Total Accesses: 4
Access: MISS
Total Hits: 0, Total Misses: 5, Total Accesses: 5
Access: MISS
Total Hits: 0, Total Misses: 6, Total Accesses: 6
Access: MISS
Total Hits: 0, Total Misses: 7, Total Accesses: 7
Access: MISS
Total Hits: 0, Total Misses: 8, Total Accesses: 8
Access: MISS
Total Hits: 0, Total Misses: 9, Total Accesses: 9
```

```
Access: MISS
Tag: 14 (binary: 00000000000000000000000000001110)
Total Hits: 0, Total Misses: 10, Total Accesses: 10
Access: MISS
Total Hits: 0, Total Misses: 11, Total Accesses: 11
Access: MISS
Total Hits: 0, Total Misses: 12, Total Accesses: 12
Access: MISS
Tag: 15 (binary: 00000000000000000000000000001111)
Total Hits: 0, Total Misses: 13, Total Accesses: 13
Access: MISS
Total Hits: 0, Total Misses: 14, Total Accesses: 14
Access: MISS
Tag: 15 (binary: 00000000000000000000000000001111)
Total Hits: 0, Total Misses: 15, Total Accesses: 15
Access: MISS
Tag: 3 (binary: 000000000000000000000000000000011)
Total Hits: 0, Total Misses: 16, Total Accesses: 16
Access: MISS
Tag: 26 (binary: 00000000000000000000000000011010)
Total Hits: 0, Total Misses: 17, Total Accesses: 17
Access: MISS
Total Hits: 0, Total Misses: 18, Total Accesses: 18
```

Total Clock Cycles: 1100