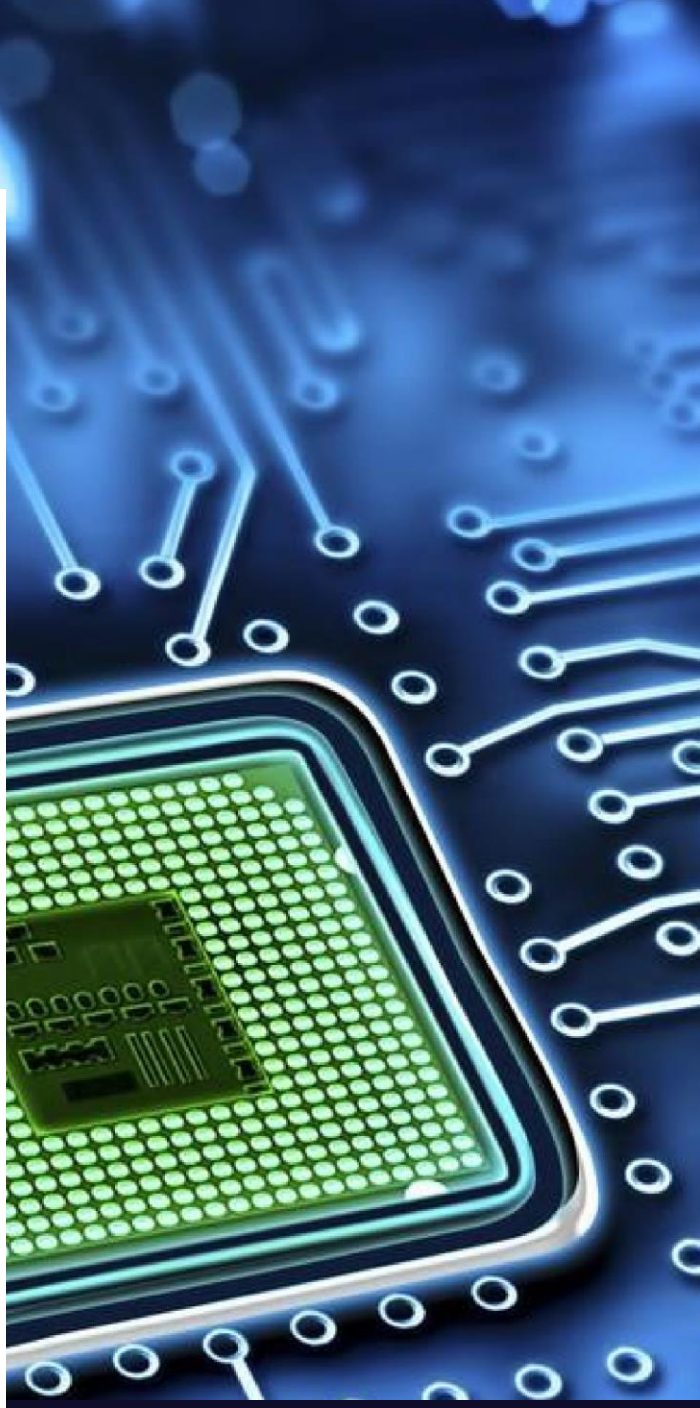
Single Cycle Project.



Tested Instruction & their corresponding object code:

X"00”, X"85”, X"10”, X"20" --> add $v0, $a0,

X"AC”, X"02”, X"00”, X"08" --> SW $v0, 8($zero)

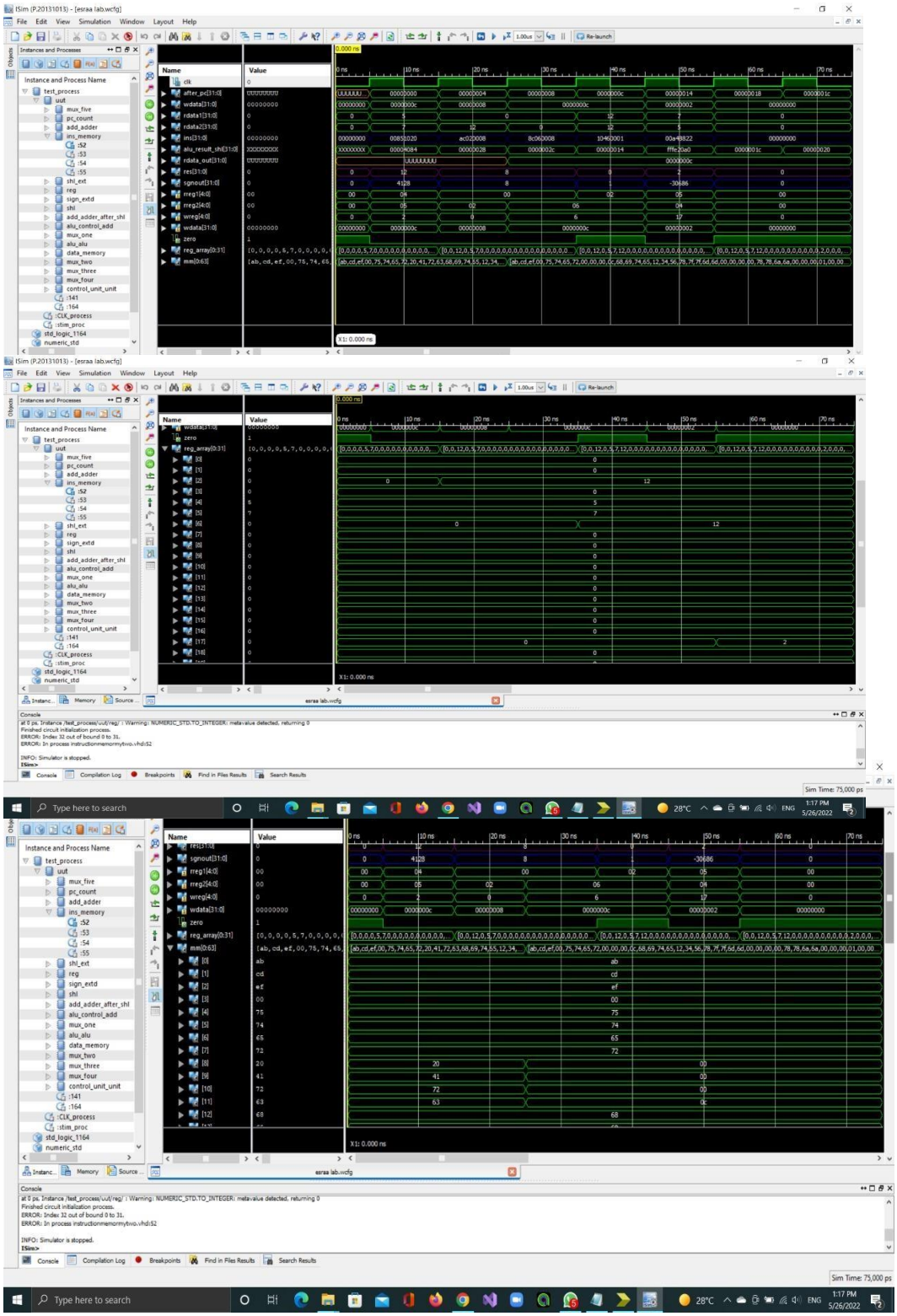
X"8C”, X"06”, X"00”, X"08" --> lw $a2, 8($zero)

X"10”, X"46”, X"00”, X"01" --> beq $v0, $a2, Good Processor

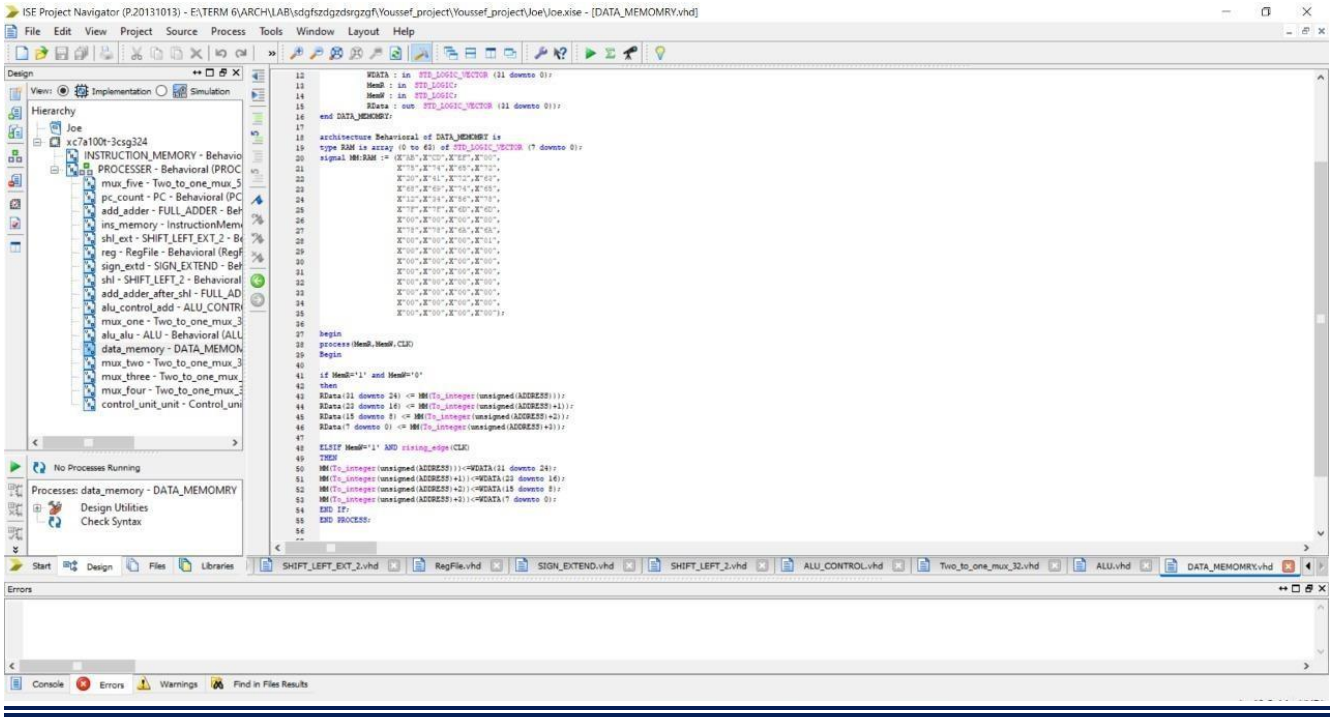
X"00”, X"46”, X"88”, X"2A" --> slt $s1, $v0, $a2

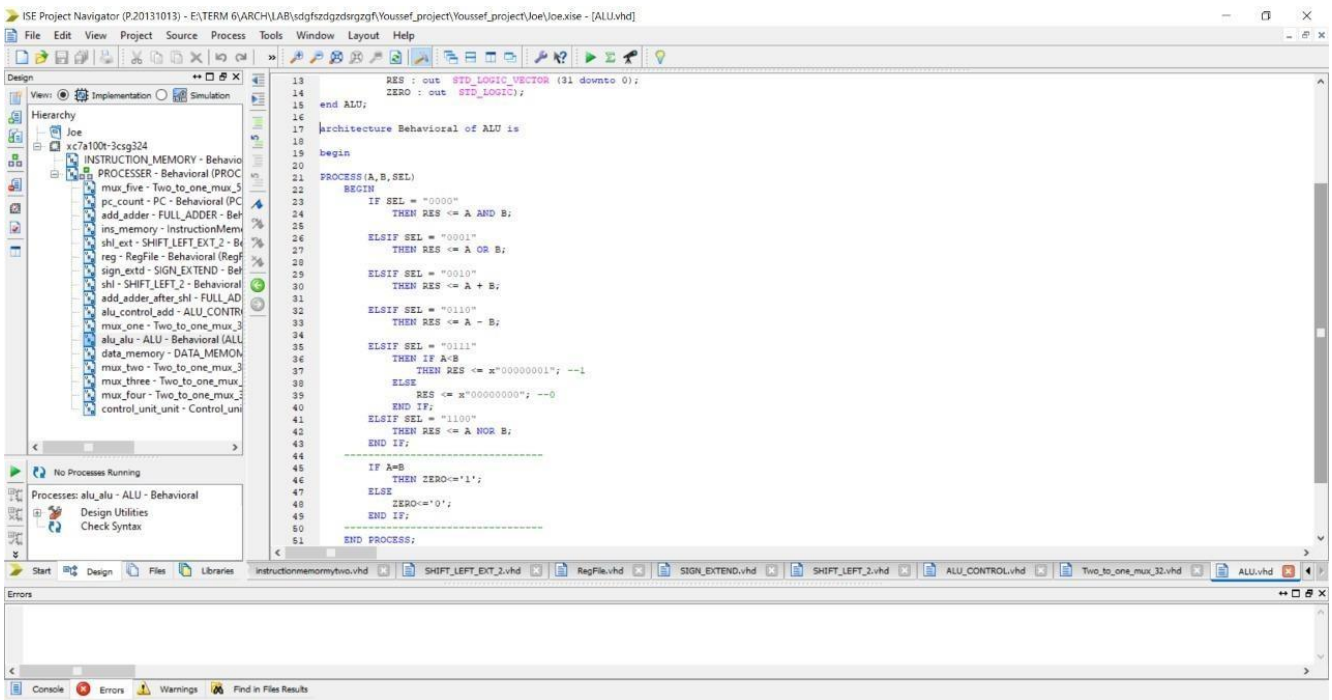
X"00", X"A4", X"88", X"22" --> Good Processor: sub $s1, $a1, $a0

Screen shot of simulation:



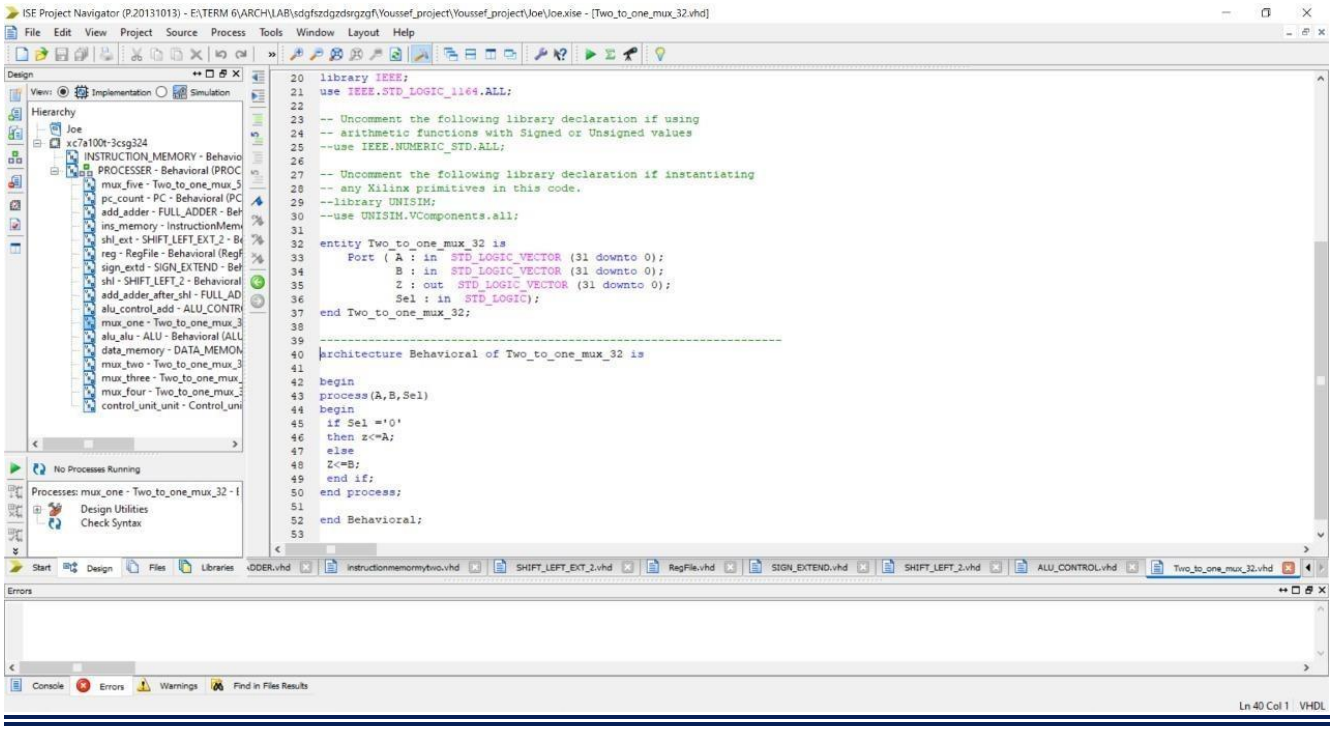
Screen Shoot of VHDL components:


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [DATA_MEMOMRY.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - Be
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: data_memory - DATA_MEMOMRY
Design Utilities
Check Syntax
WDATA : in STD_LOGIC_VECTOR (31 downto 0);
MemR : in STD_LOGIC;
MemW : in STD_LOGIC;
RData : out STD_LOGIC_VECTOR (31 downto 0));
end DATA_MEMOMRY;
architecture Behavioral of DATA_MEMOMRY is
type RAM is array (0 to 62) of STD_LOGIC_VECTOR (7 downto 0);
signal MM:RAM := (X"AB",X"CD",X"EF",X"00",
X"75",X"74",X"65",X"72",
X"20",X"61",X"72",X"63",
X"68",X"69",X"74",X"65",
X"12",X"34",X"56",X"78",
X"7F",X"7F",X"6D",X"6D",
X"00",X"00",X"00",X"00",
X"75",X"78",X"69",X"65",
X"00",X"00",X"00",X"01",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00");
begin
process(MemR,MemW,CLK)
Begin
if MemR='1' and MemW='0'
then
RData(31 downto 24) <= MM(To_integer(unsigned(ADDRESS)));
RData(23 downto 16) <= MM(To_integer(unsigned(ADDRESS)+1));
RData(15 downto 8) <= MM(To_integer(unsigned(ADDRESS)+2));
RData(7 downto 0) <= MM(To_integer(unsigned(ADDRESS)+3));
ELSIF MemW='1' AND rising_edge(CLK)
THEN
MM(To_integer(unsigned(ADDRESS)))<=WDATA(31 downto 24);
MM(To_integer(unsigned(ADDRESS)+1))<=WDATA(23 downto 16);
MM(To_integer(unsigned(ADDRESS)+2))<=WDATA(15 downto 8);
MM(To_integer(unsigned(ADDRESS)+3))<=WDATA(7 downto 0);
END IF;
END PROCESS;
Start Design Files Libraries
SHIFT_LEFT_EXT_2.vhd
RegFile.vhd
SIGN_EXTEND.vhd
SHIFT_LEFT_2.vhd
ALU_CONTROL.vhd
Two_to_one_mux_32.vhd
ALU.vhd
DATA_MEMOMRY.vhd
Errors
Console Errors Warnings Find in Files Results

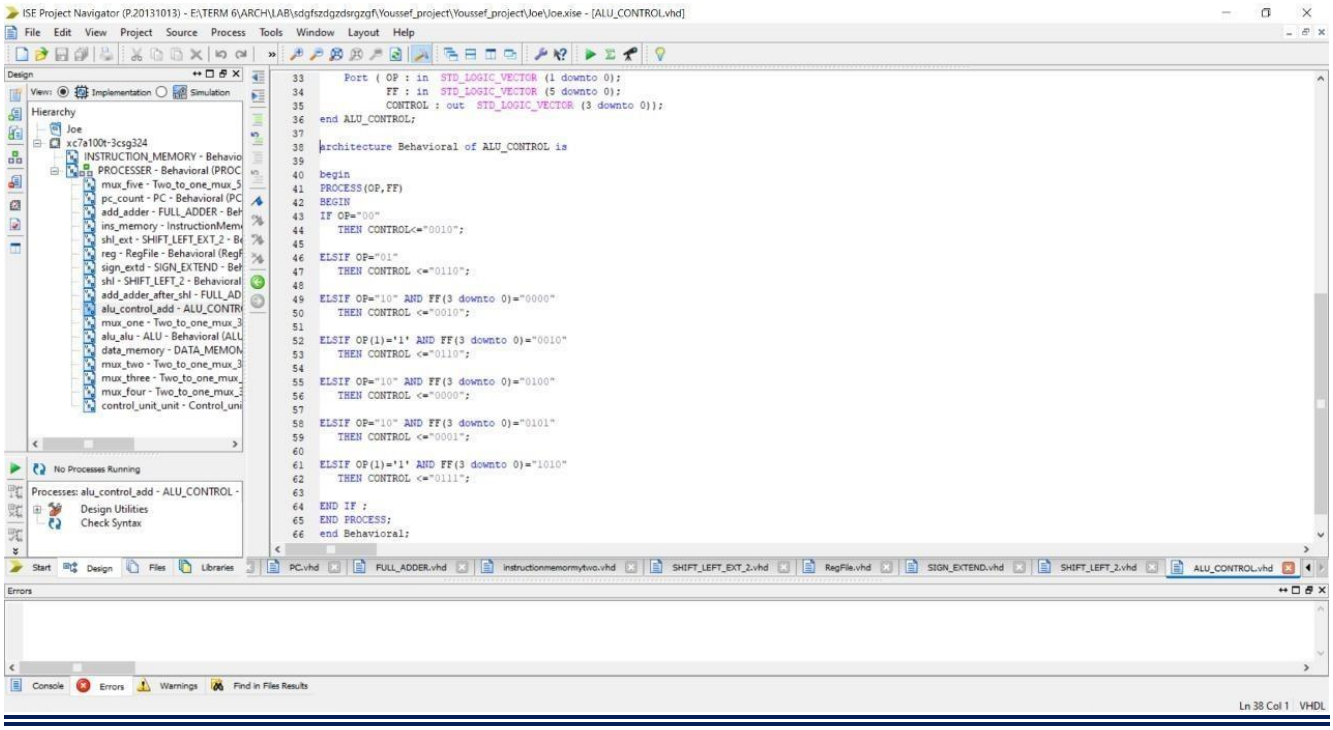

ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [ALU.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - Be
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: alu_alu - ALU - Behavioral
Design Utilities
Check Syntax
RES : out STD_LOGIC_VECTOR (31 downto 0);
ZERO : out STD_LOGIC);
end ALU;
architecture Behavioral of ALU is
begin
PROCESS(A,B,SEL)
BEGIN
IF SEL = "0000"
THEN RES <= A AND B;
ELSIF SEL = "0001"
THEN RES <= A OR B;
ELSIF SEL = "0010"
THEN RES <= A + B;
ELSIF SEL = "0110"
THEN RES <= A - B;
ELSIF SEL = "0111"
THEN IF A<B
THEN RES <= x"00000001"; --1
ELSE
RES <= x"00000000"; --0
END IF;
ELSIF SEL = "1100"
THEN RES <= A NOR B;
END IF;

IF A=B
THEN ZERO<='1';
ELSE
ZERO<='0';
END IF;

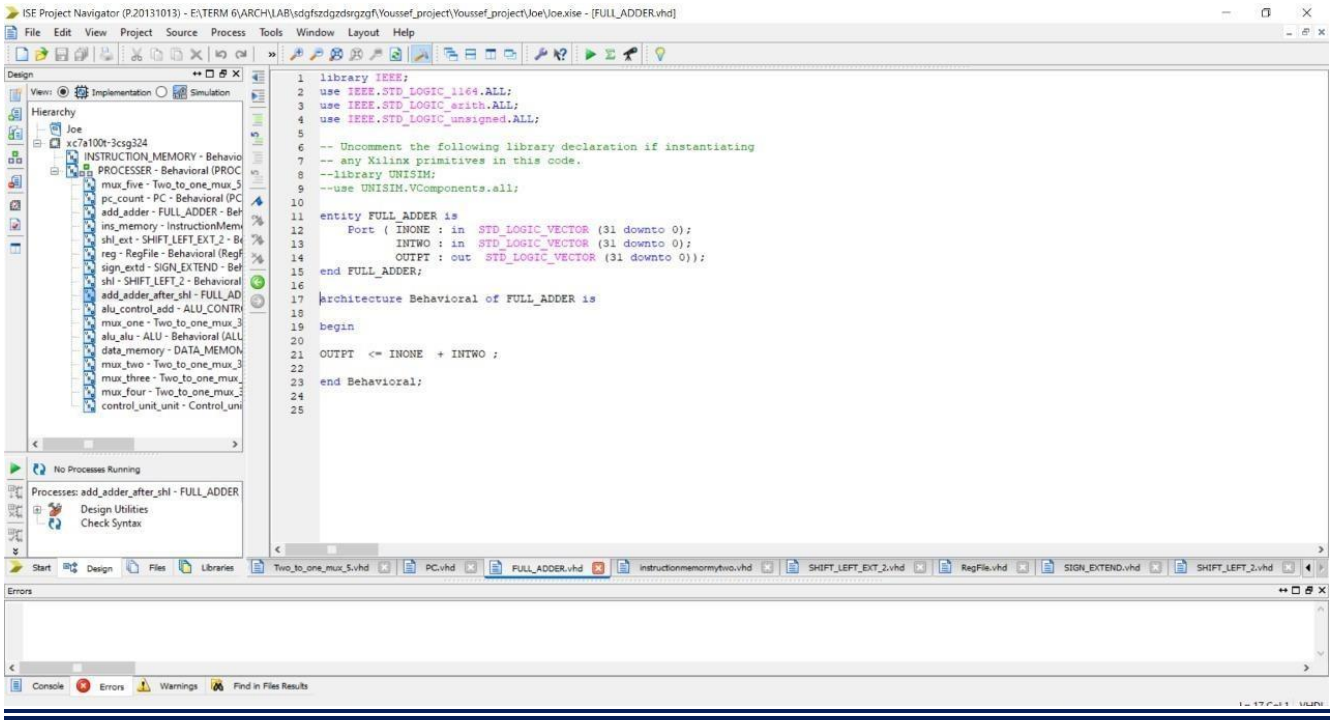
END PROCESS;
Start Design Files Libraries
instructionmemormytwo.vhd
SHIFT_LEFT_EXT_2.vhd
RegFile.vhd
SIGN_EXTEND.vhd
SHIFT_LEFT_2.vhd
ALU_CONTROL.vhd
Two_to_one_mux_32.vhd
ALU.vhd
Errors
Console Errors Warnings Find in Files Results

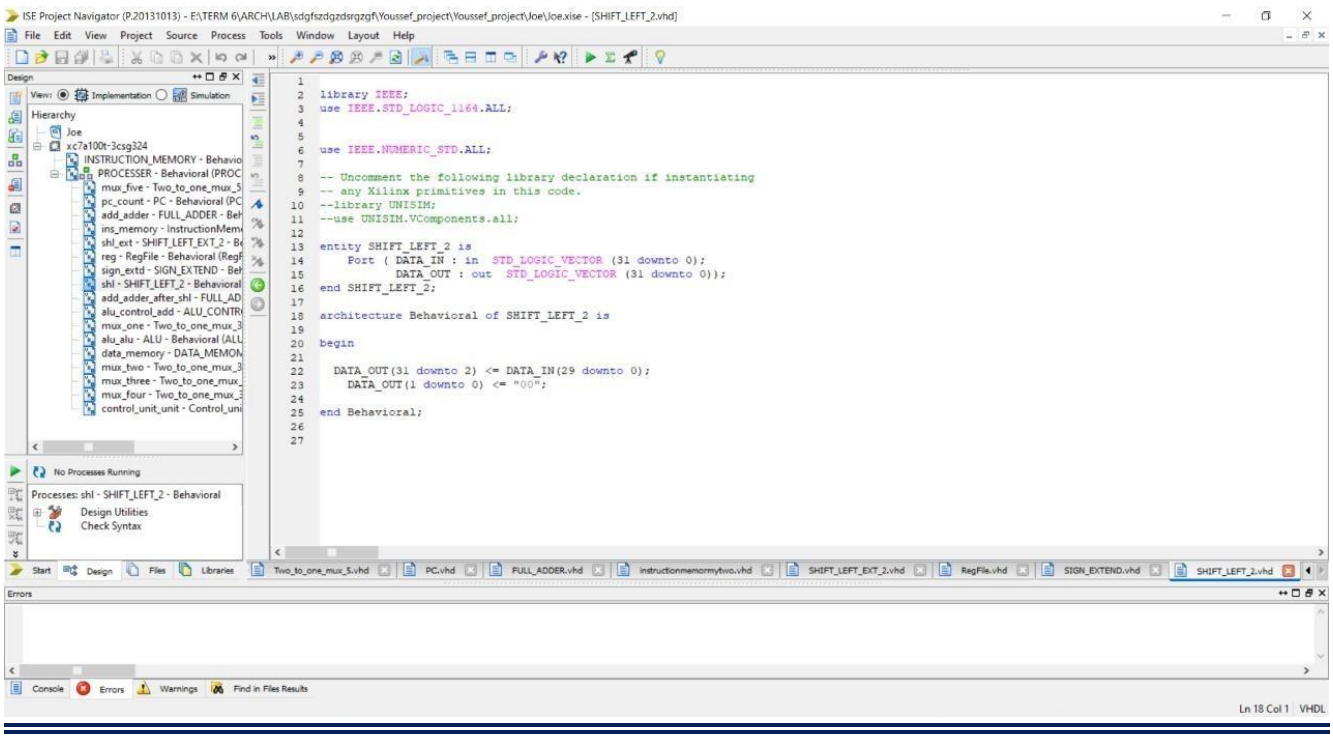


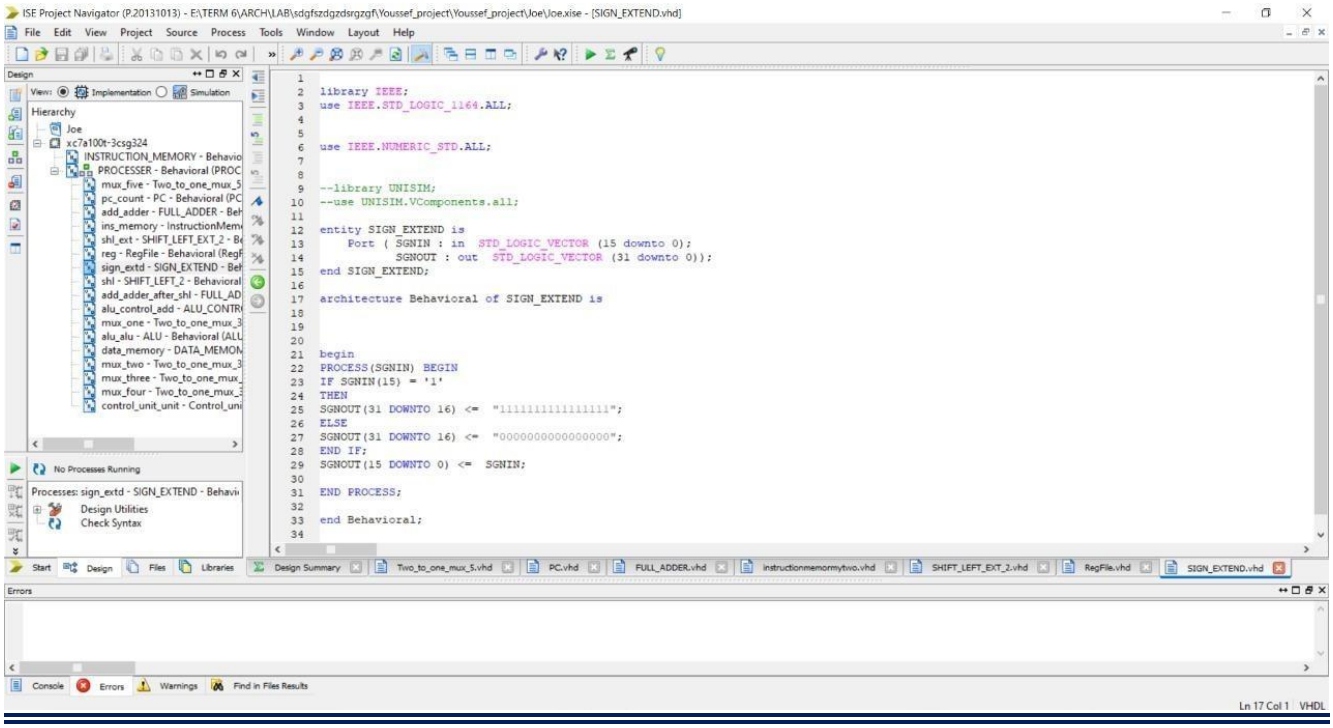
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Two_to_one_mux_32 is
    Port ( A : in  STD_LOGIC_VECTOR (31 downto 0);
           B : in  STD_LOGIC_VECTOR (31 downto 0);
           Z : out  STD_LOGIC_VECTOR (31 downto 0);
           Sel : in  STD_LOGIC);
end Two_to_one_mux_32;

----------------------------------------------------------------------------
architecture Behavioral of Two_to_one_mux_32 is

begin
process(A,B,Sel)
begin
 if Sel ='0'
 then z<=A;
 else
 Z<=B;
 end if;
end process;

end Behavioral;
```

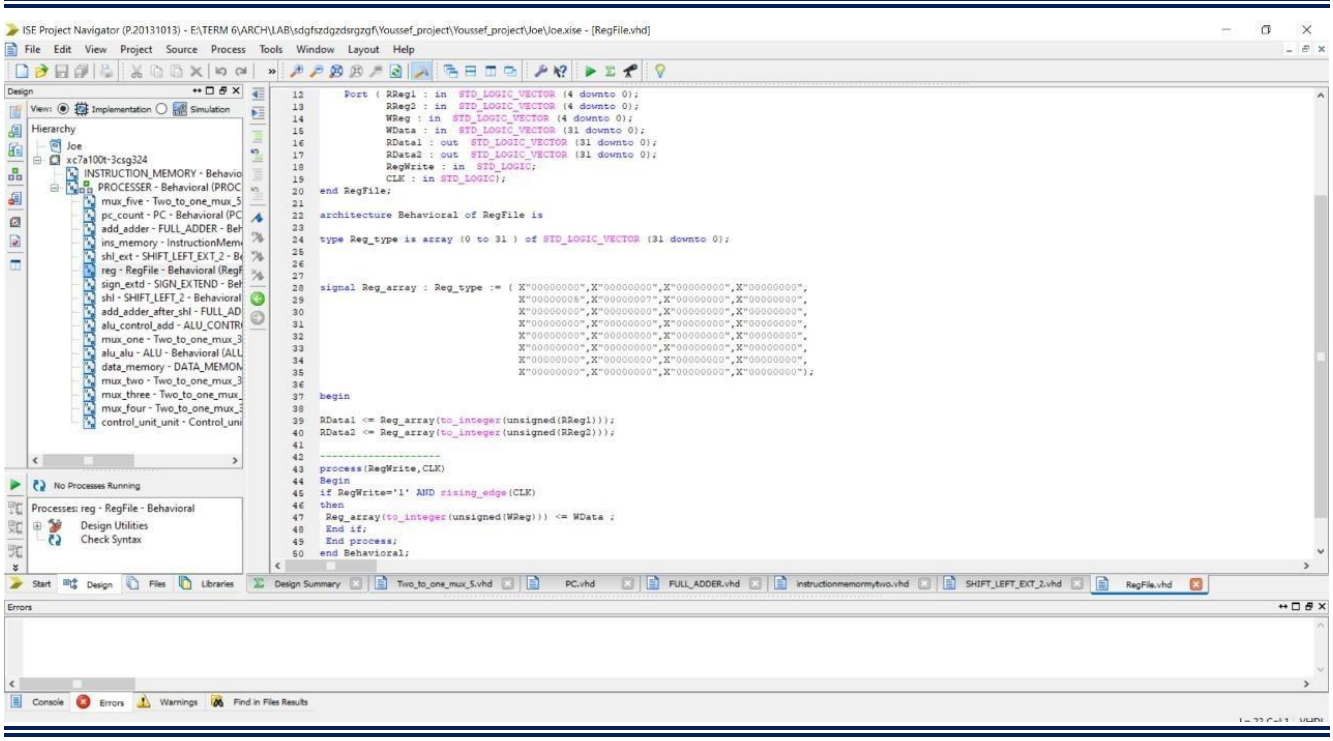


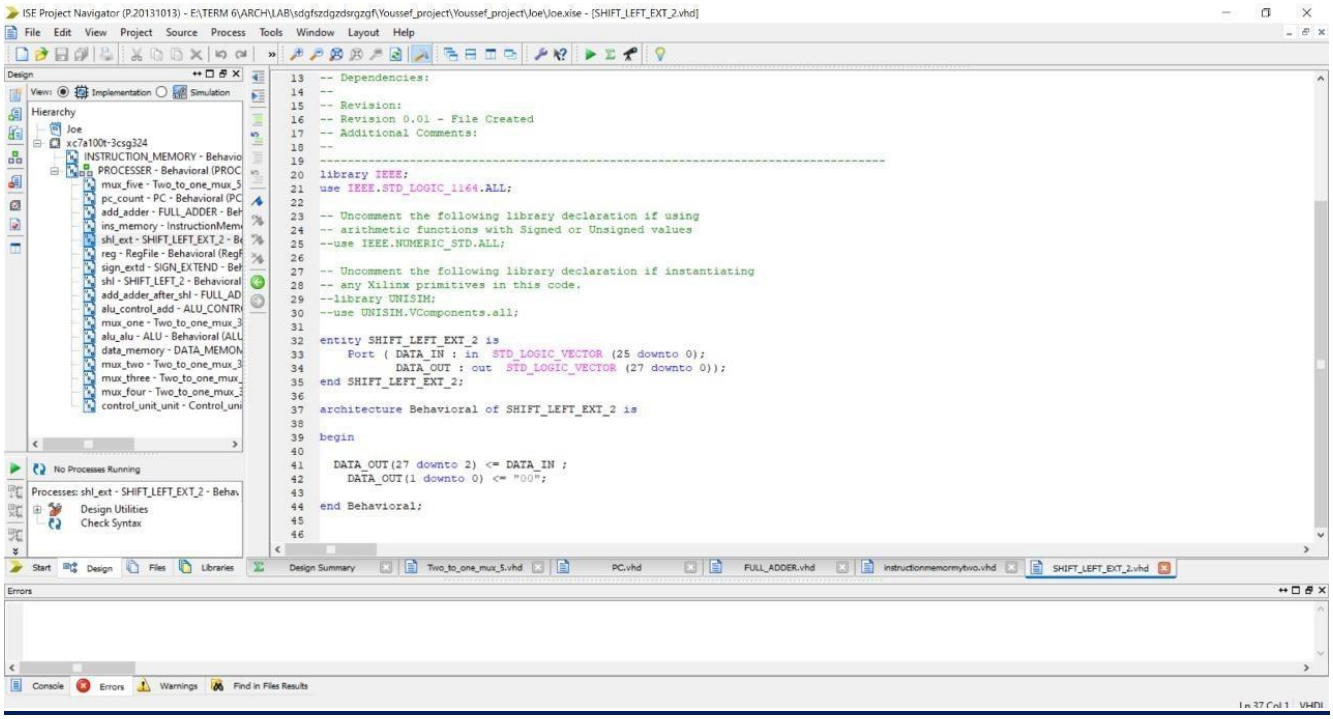
```
    Port ( OP : in  STD_LOGIC_VECTOR (1 downto 0);
           FF : in  STD_LOGIC_VECTOR (5 downto 0);
           CONTROL : out  STD_LOGIC_VECTOR (3 downto 0));
end ALU_CONTROL;

architecture Behavioral of ALU_CONTROL is

begin
PROCESS(OP,FF)
BEGIN
IF OP="00"
   THEN CONTROL<="0010";

ELSIF OP="01"
   THEN CONTROL <="0110";

ELSIF OP="10" AND FF(3 downto 0)="0000"
   THEN CONTROL <="0010";

ELSIF OP(1)='1' AND FF(3 downto 0)="0010"
   THEN CONTROL <="0110";

ELSIF OP="10" AND FF(3 downto 0)="0100"
   THEN CONTROL <="0000";

ELSIF OP="10" AND FF(3 downto 0)="0101"
   THEN CONTROL <="0001";

ELSIF OP(1)='1' AND FF(3 downto 0)="1010"
   THEN CONTROL <="0111";

END IF ;
END PROCESS;
end Behavioral;
```

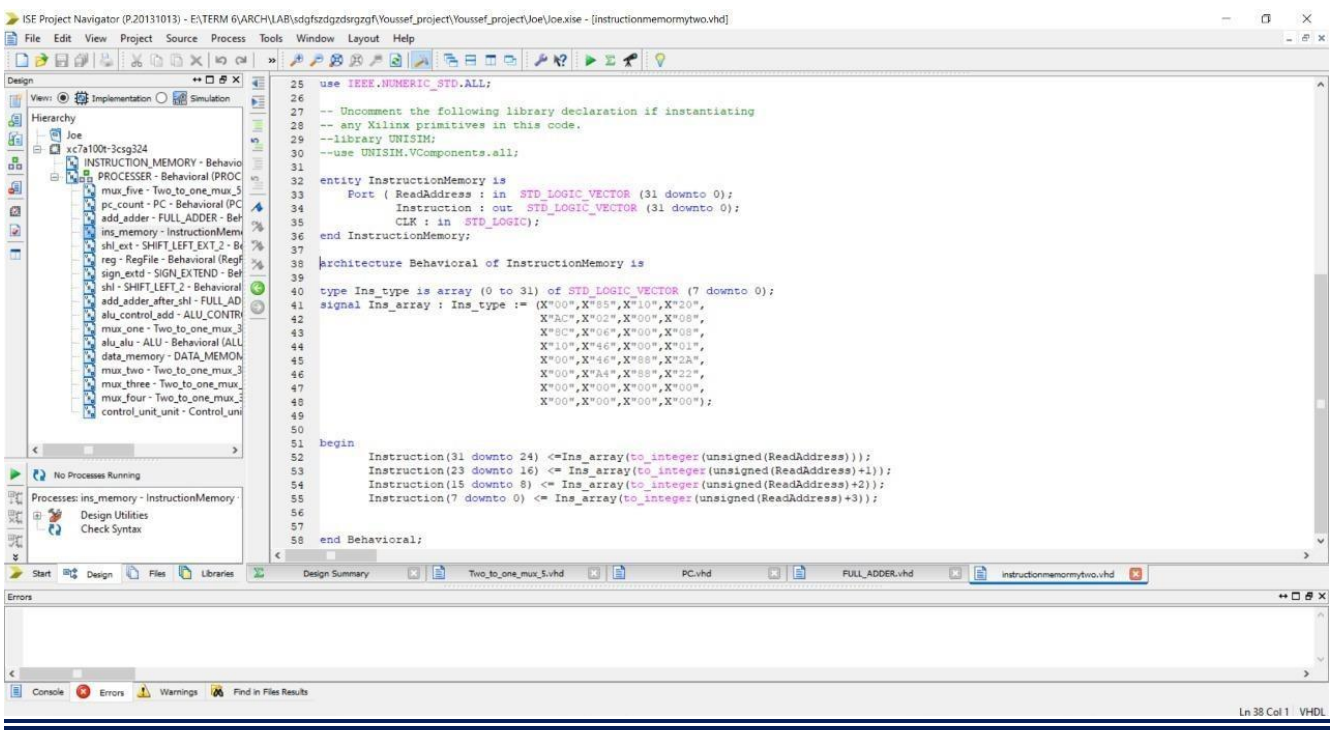

ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [FULL_ADDER.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: add_adder_after_shl - FULL_ADDER
Design Utilities
Check Syntax
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_arith.ALL;
4 use IEEE.STD_LOGIC_unsigned.ALL;
5
6 -- Uncomment the following library declaration if instantiating
7 -- any Xilinx primitives in this code.
8 --library UNISIM;
9 --use UNISIM.VComponents.all;
10
11 entity FULL_ADDER is
12 Port (INONE : in STD_LOGIC_VECTOR (31 downto 0);
13 INTWO : in STD_LOGIC_VECTOR (31 downto 0);
14 OUTPT : out STD_LOGIC_VECTOR (31 downto 0));
15 end FULL_ADDER;
16
17 architecture Behavioral of FULL_ADDER is
18
19 begin
20
21 OUTPT <= INONE + INTWO ;
22
23 end Behavioral;
24
25
Start Design Files Libraries
Two_to_one_mux_5.vhd PC.vhd FULL_ADDER.vhd instructionmemorymytwo.vhd SHIFT_LEFT_EXT_2.vhd RegFile.vhd SIGN_EXTEND.vhd SHIFT_LEFT_2.vhd
Errors
Console Errors Warnings Find in Files Results

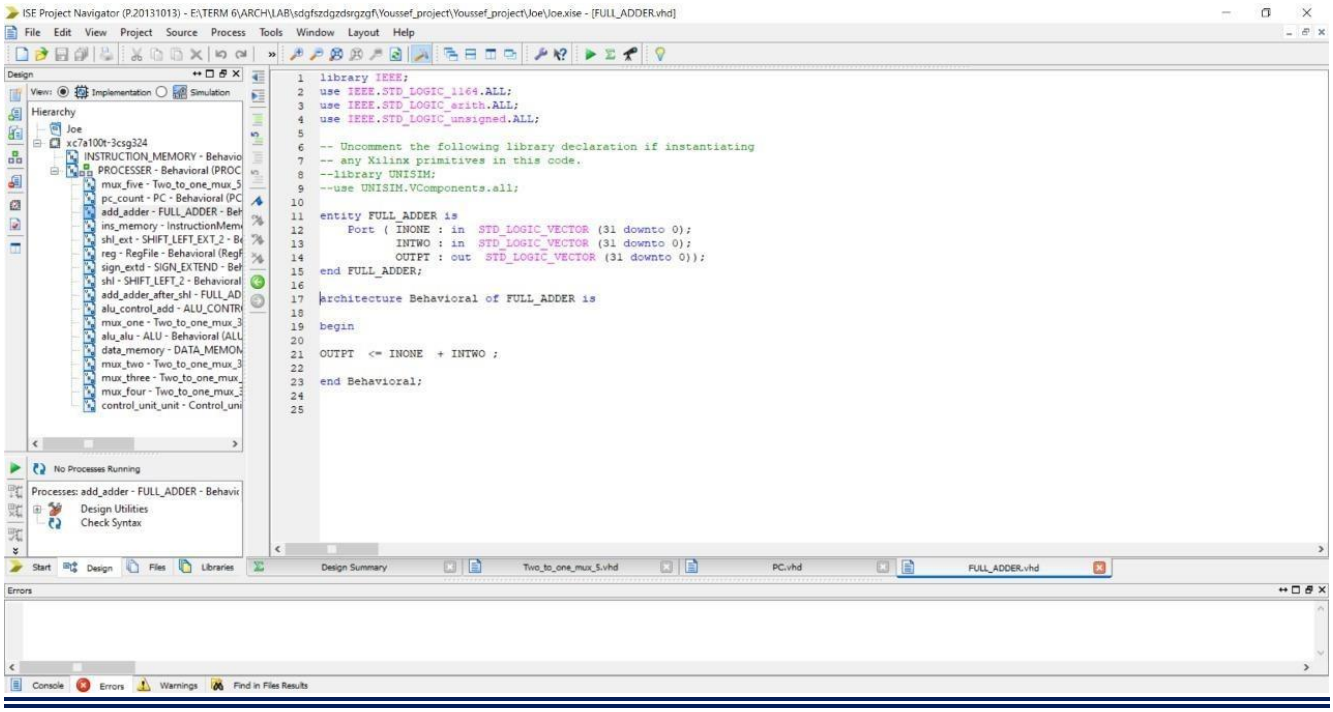

ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [SHIFT_LEFT_2.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: shl - SHIFT_LEFT_2 - Behavioral
Design Utilities
Check Syntax
1
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5
6 use IEEE.NUMERIC_STD.ALL;
7
8 -- Uncomment the following library declaration if instantiating
9 -- any Xilinx primitives in this code.
10 --library UNISIM;
11 --use UNISIM.VComponents.all;
12
13 entity SHIFT_LEFT_2 is
14 Port (DATA_IN : in STD_LOGIC_VECTOR (31 downto 0);
15 DATA_OUT : out STD_LOGIC_VECTOR (31 downto 0));
16 end SHIFT_LEFT_2;
17
18 architecture Behavioral of SHIFT_LEFT_2 is
19
20 begin
21
22 DATA_OUT(31 downto 2) <= DATA_IN(29 downto 0);
23 DATA_OUT(1 downto 0) <= "00";
24
25 end Behavioral;
26
27
Start Design Files Libraries
Two_to_one_mux_5.vhd PC.vhd FULL_ADDER.vhd instructionmemorymytwo.vhd SHIFT_LEFT_EXT_2.vhd RegFile.vhd SIGN_EXTEND.vhd SHIFT_LEFT_2.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 18 Col 1 VHDL

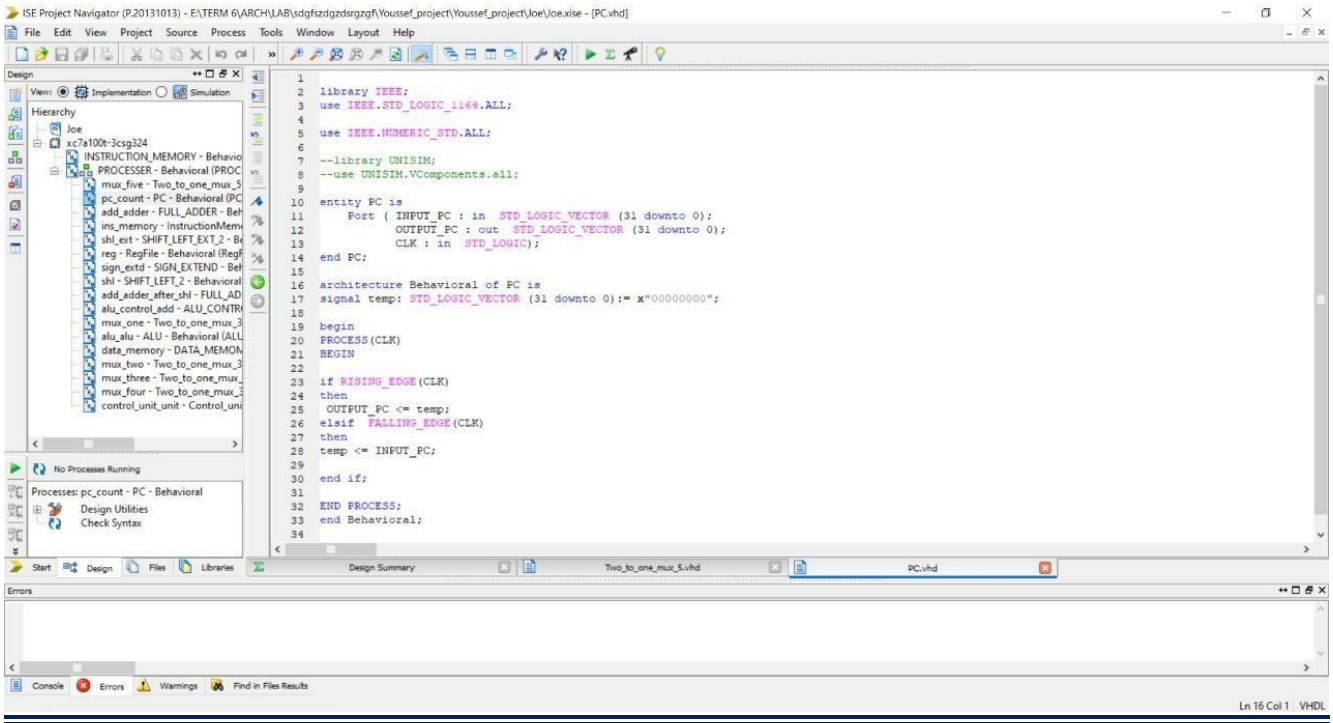

ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [SIGN_EXTEND.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: sign_extd - SIGN_EXTEND - Behavi
Design Utilities
Check Syntax
Start Design Files Libraries
Design Summary Two_to_one_mux_5.vhd PC.vhd FULL_ADDER.vhd instructionmemormytwo.vhd SHIFT_LEFT_EXT_2.vhd RegFile.vhd SIGN_EXTEND.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 17 Col 1 VHDL
1
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5
6 use IEEE.NUMERIC_STD.ALL;
7
8
9 --library UNISIM;
10 --use UNISIM.VComponents.all;
11
12 entity SIGN_EXTEND is
13 Port (SGNIN : in STD_LOGIC_VECTOR (15 downto 0);
14 SGNOUT : out STD_LOGIC_VECTOR (31 downto 0));
15 end SIGN_EXTEND;
16
17 architecture Behavioral of SIGN_EXTEND is
18
19
20
21 begin
22 PROCESS(SGNIN) BEGIN
23 IF SGNIN(15) = '1'
24 THEN
25 SGNOUT(31 DOWNTO 16) <= "1111111111111111";
26 ELSE
27 SGNOUT(31 DOWNTO 16) <= "0000000000000000";
28 END IF;
29 SGNOUT(15 DOWNTO 0) <= SGNIN;
30
31 END PROCESS;
32
33 end Behavioral;
34


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [RegFile.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: reg - RegFile - Behavioral
Design Utilities
Check Syntax
Start Design Files Libraries
Design Summary Two_to_one_mux_5.vhd PC.vhd FULL_ADDER.vhd instructionmemormytwo.vhd SHIFT_LEFT_EXT_2.vhd RegFile.vhd
Errors
Console Errors Warnings Find in Files Results
12 Port (RReg1 : in STD_LOGIC_VECTOR (4 downto 0);
13 RReg2 : in STD_LOGIC_VECTOR (4 downto 0);
14 WReg : in STD_LOGIC_VECTOR (4 downto 0);
15 WData : in STD_LOGIC_VECTOR (31 downto 0);
16 RData1 : out STD_LOGIC_VECTOR (31 downto 0);
17 RData2 : out STD_LOGIC_VECTOR (31 downto 0);
18 RegWrite : in STD_LOGIC;
19 CLK : in STD_LOGIC);
20 end RegFile;
21
22 architecture Behavioral of RegFile is
23
24 type Reg_type is array (0 to 31) of STD_LOGIC_VECTOR (31 downto 0);
25
26
27
28 signal Reg_array : Reg_type := (X"00000000",X"00000000",X"00000000",X"00000000",
29 X"00000000",X"00000000",X"00000000",X"00000000",
30 X"00000000",X"00000000",X"00000000",X"00000000",
31 X"00000000",X"00000000",X"00000000",X"00000000",
32 X"00000000",X"00000000",X"00000000",X"00000000",
33 X"00000000",X"00000000",X"00000000",X"00000000",
34 X"00000000",X"00000000",X"00000000",X"00000000",
35 X"00000000",X"00000000",X"00000000",X"00000000");
36
37 begin
38
39 RData1 <= Reg_array(to_integer(unsigned(RReg1)));
40 RData2 <= Reg_array(to_integer(unsigned(RReg2)));
41
42 --------------------
43 process(RegWrite,CLK)
44 Begin
45 if RegWrite='1' AND rising_edge(CLK)
46 then
47 Reg_array(to_integer(unsigned(WReg))) <= WData ;
48 End if;
49 End process;
50 end Behavioral;


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [SHIFT_LEFT_EXT_2.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: shl_ext - SHIFT_LEFT_EXT_2 - Behav
Design Utilities
Check Syntax
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity SHIFT_LEFT_EXT_2 is
Port (DATA_IN : in STD_LOGIC_VECTOR (25 downto 0);
DATA_OUT : out STD_LOGIC_VECTOR (27 downto 0));
end SHIFT_LEFT_EXT_2;
architecture Behavioral of SHIFT_LEFT_EXT_2 is
begin
DATA_OUT(27 downto 2) <= DATA_IN ;
DATA_OUT(1 downto 0) <= "00";
end Behavioral;
Design Summary
Two_to_one_mux_5.vhd
PC.vhd
FULL_ADDER.vhd
instructionmemorymytwo.vhd
SHIFT_LEFT_EXT_2.vhd
Errors
Console
Errors
Warnings
Find in Files Results
Ln 37 Col 1 VHDL


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [instructionmemorymytwo.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: ins_memory - InstructionMemory
Design Utilities
Check Syntax
use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity InstructionMemory is
Port (ReadAddress : in STD_LOGIC_VECTOR (31 downto 0);
Instruction : out STD_LOGIC_VECTOR (31 downto 0);
CLK : in STD_LOGIC);
end InstructionMemory;
architecture Behavioral of InstructionMemory is
type Ins_type is array (0 to 31) of STD_LOGIC_VECTOR (7 downto 0);
signal Ins_array : Ins_type := (X"00",X"85",X"10",X"20",
X"AC",X"02",X"00",X"08",
X"8C",X"06",X"00",X"08",
X"10",X"46",X"00",X"01",
X"00",X"46",X"88",X"2A",
X"00",X"A4",X"88",X"22",
X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00");
begin
Instruction(31 downto 24) <=Ins_array(to_integer(unsigned(ReadAddress)));
Instruction(23 downto 16) <= Ins_array(to_integer(unsigned(ReadAddress)+1));
Instruction(15 downto 8) <= Ins_array(to_integer(unsigned(ReadAddress)+2));
Instruction(7 downto 0) <= Ins_array(to_integer(unsigned(ReadAddress)+3));
end Behavioral;
Design Summary
Two_to_one_mux_5.vhd
PC.vhd
FULL_ADDER.vhd
instructionmemorymytwo.vhd
Errors
Console
Errors
Warnings
Find in Files Results
Ln 38 Col 1 VHDL


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [FULL_ADDER.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Reg
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: add_adder - FULL_ADDER - Behavic
Design Utilities
Check Syntax
Start Design Files Libraries
Design Summary
Two_to_one_mux_5.vhd
PC.vhd
FULL_ADDER.vhd
Errors
Console Errors Warnings Find in Files Results
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_arith.ALL;
4 use IEEE.STD_LOGIC_unsigned.ALL;
5
6 -- Uncomment the following library declaration if instantiating
7 -- any Xilinx primitives in this code.
8 --library UNISIM;
9 --use UNISIM.VComponents.all;
10
11 entity FULL_ADDER is
12 Port (INONE : in STD_LOGIC_VECTOR (31 downto 0);
13 INTWO : in STD_LOGIC_VECTOR (31 downto 0);
14 OUTPT : out STD_LOGIC_VECTOR (31 downto 0));
15 end FULL_ADDER;
16
17 architecture Behavioral of FULL_ADDER is
18
19 begin
20
21 OUTPT <= INONE + INTWO ;
22
23 end Behavioral;
24
25


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [PC.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
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xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
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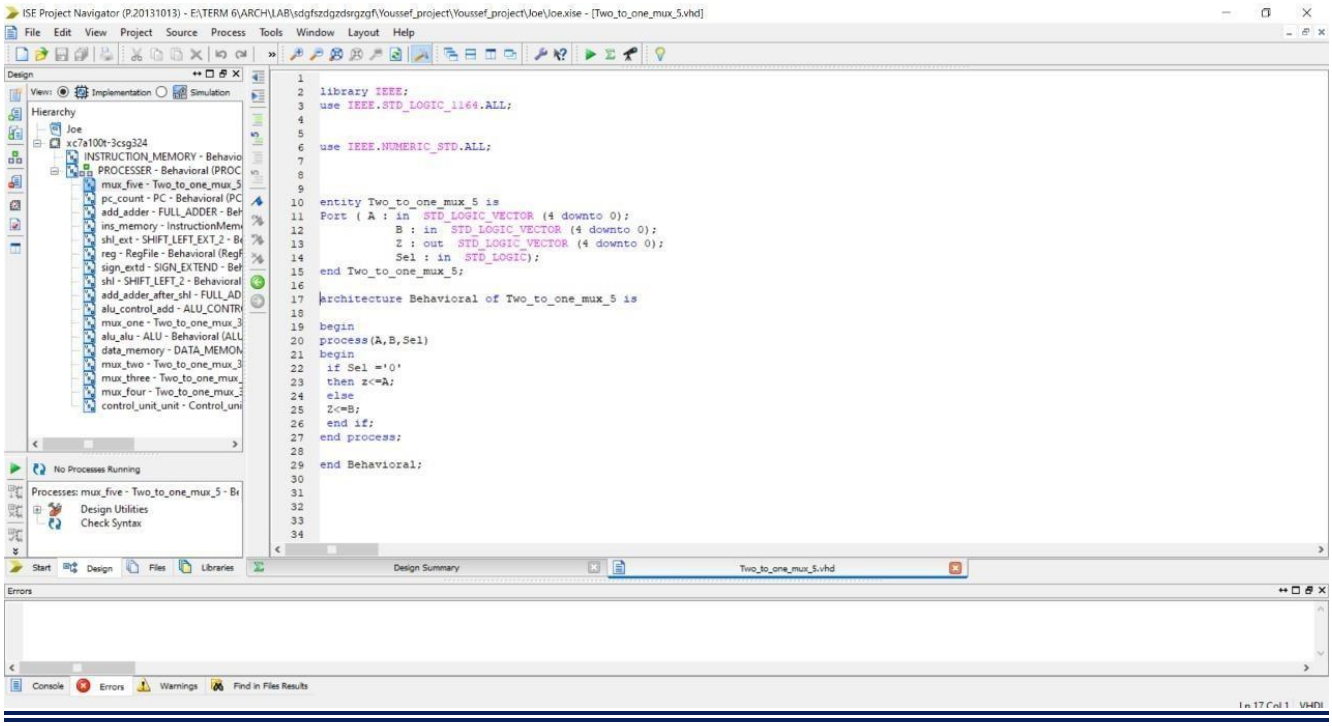
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Reg
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: pc_count - PC - Behavioral
Design Utilities
Check Syntax
Start Design Files Libraries
Design Summary
Two_to_one_mux_5.vhd
PC.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 16 Col 1 VHDL
1
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5 use IEEE.NUMERIC_STD.ALL;
6
7 --library UNISIM;
8 --use UNISIM.VComponents.all;
9
10 entity PC is
11 Port (INPUT_PC : in STD_LOGIC_VECTOR (31 downto 0);
12 OUTPUT_PC : out STD_LOGIC_VECTOR (31 downto 0);
13 CLK : in STD_LOGIC);
14 end PC;
15
16 architecture Behavioral of PC is
17 signal temp: STD_LOGIC_VECTOR (31 downto 0):= x"00000000";
18
19 begin
20 PROCESS(CLK)
21 BEGIN
22
23 if RISING_EDGE(CLK)
24 then
25 OUTPUT_PC <= temp;
26 elsif FALLING_EDGE(CLK)
27 then
28 temp <= INPUT_PC;
29
30 end if;
31
32 END PROCESS;
33 end Behavioral;
34


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [Two_to_one_mux_5.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
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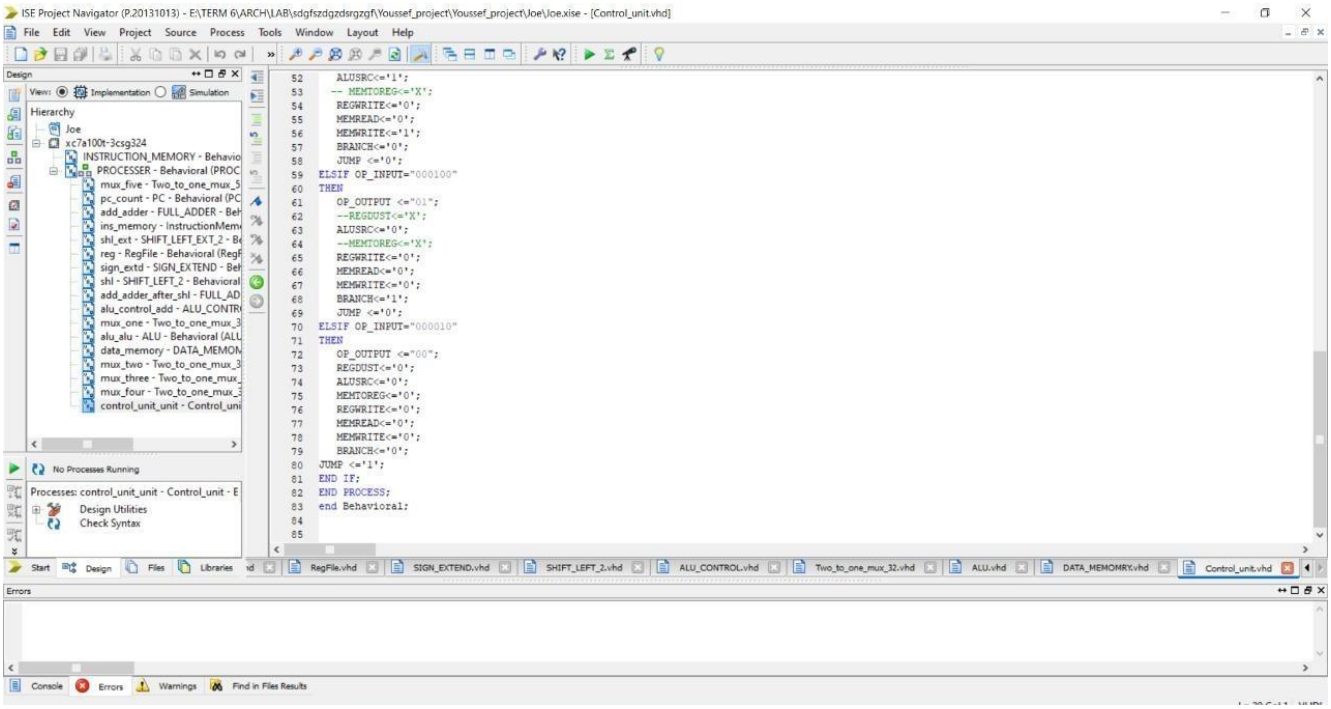
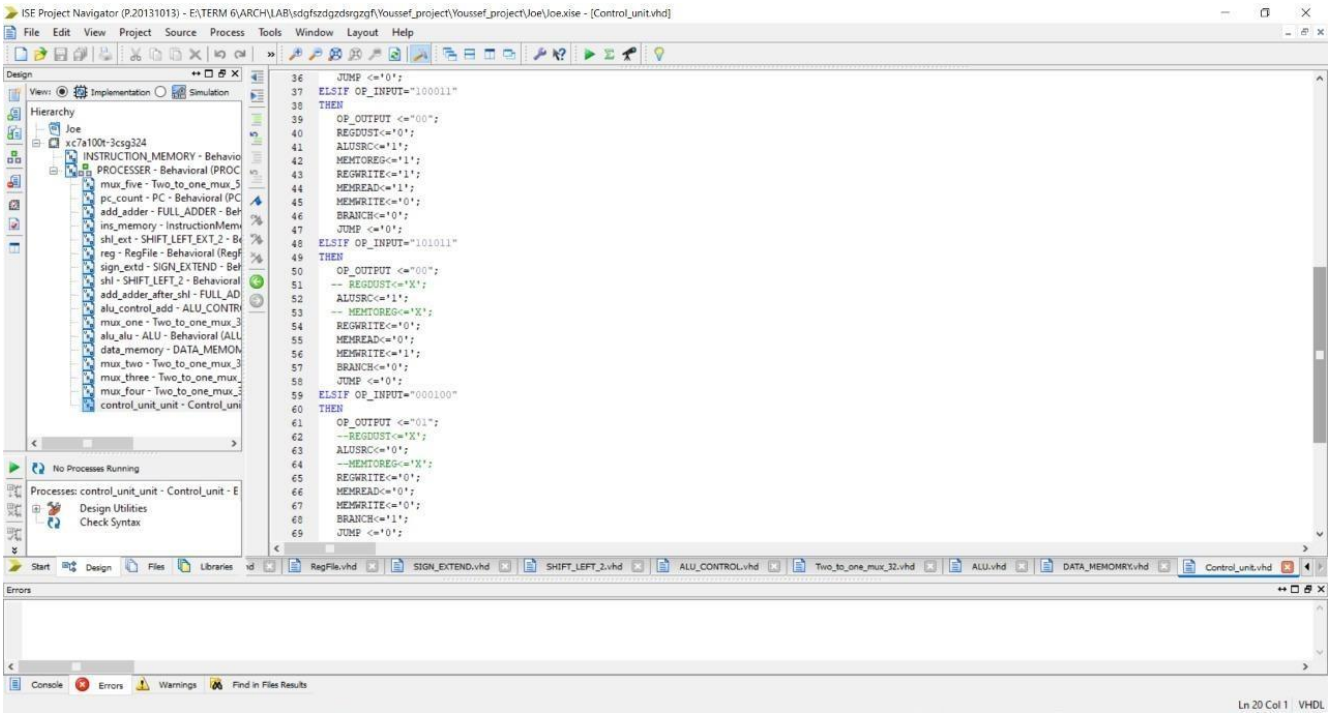
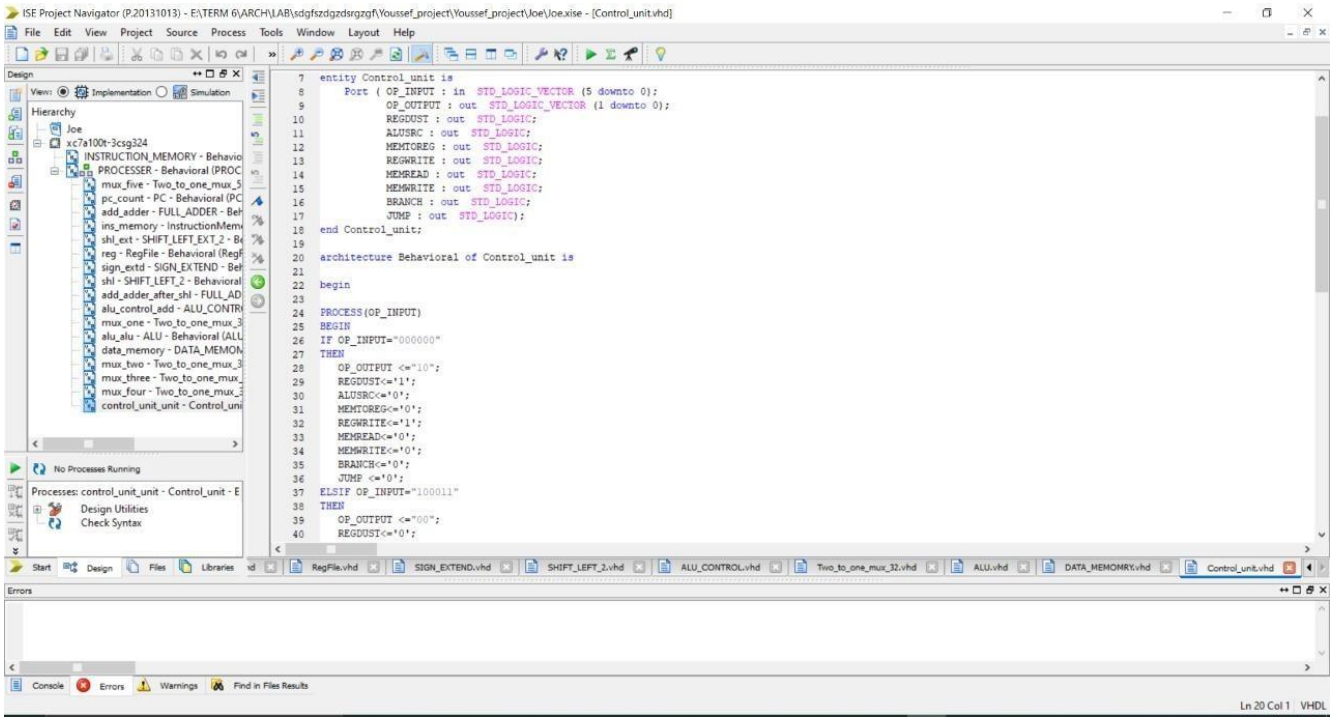
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Reg
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: mux_five - Two_to_one_mux_5 - B
Design Utilities
Check Syntax
Start Design Files Libraries
Design Summary
Two_to_one_mux_5.vhd
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3
4 use IEEE.NUMERIC_STD.ALL;
5
6
7 entity Two_to_one_mux_5 is
8 Port (A : in STD_LOGIC_VECTOR (4 downto 0);
9 B : in STD_LOGIC_VECTOR (4 downto 0);
10 Z : out STD_LOGIC_VECTOR (4 downto 0);
11 Sel : in STD_LOGIC);
12 end Two_to_one_mux_5;
13
14 architecture Behavioral of Two_to_one_mux_5 is
15
16 begin
17 process(A,B,Sel)
18 begin
19 if Sel ='0'
20 then z<=A;
21 else
22 Z<=B;
23 end if;
24 end process;
25
26 end Behavioral;
27
28
29
30
31
32
33
34
Errors
Console Errors Warnings Find in Files Results
Ln 17 Col 1 VHDL


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [Control_unit.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: control_unit_unit - Control_unit - E
Design Utilities
Check Syntax
ALUSRC<='1';
-- MEMTOREG<='X';
REGWRITE<='0';
MEMREAD<='0';
MEMWRITE<='1';
BRANCH<='0';
JUMP <='0';
ELSIF OP_INPUT="000100"
THEN
OP_OUTPUT <="01";
--REGDUST<='X';
ALUSRC<='0';
--MEMTOREG<='X';
REGWRITE<='0';
MEMREAD<='0';
MEMWRITE<='0';
BRANCH<='1';
JUMP <='0';
ELSIF OP_INPUT="000010"
THEN
OP_OUTPUT <="00";
REGDUST<='0';
ALUSRC<='0';
MEMTOREG<='0';
REGWRITE<='0';
MEMREAD<='0';
MEMWRITE<='0';
BRANCH<='0';
JUMP <='1';
END IF;
END PROCESS;
end Behavioral;
Start Design Files Libraries
RegFile.vhd SIGN_EXTEND.vhd SHIFT_LEFT_2.vhd ALU_CONTROL.vhd Two_to_one_mux_32.vhd ALU.vhd DATA_MEMOMRY.vhd Control_unit.vhd
Errors
Console Errors Warnings Find in Files Results


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [Control_unit.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - B
reg - RegFile - Behavioral (Regf
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMOM
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: control_unit_unit - Control_unit - E
Design Utilities
Check Syntax
JUMP <='0';
ELSIF OP_INPUT="100011"
THEN
OP_OUTPUT <="00";
REGDUST<='0';
ALUSRC<='1';
MEMTOREG<='1';
REGWRITE<='1';
MEMREAD<='1';
MEMWRITE<='0';
BRANCH<='0';
JUMP <='0';
ELSIF OP_INPUT="101011"
THEN
OP_OUTPUT <="00";
-- REGDUST<='X';
ALUSRC<='1';
-- MEMTOREG<='X';
REGWRITE<='0';
MEMREAD<='0';
MEMWRITE<='1';
BRANCH<='0';
JUMP <='0';
ELSIF OP_INPUT="000100"
THEN
OP_OUTPUT <="01";
--REGDUST<='X';
ALUSRC<='0';
--MEMTOREG<='X';
REGWRITE<='0';
MEMREAD<='0';
MEMWRITE<='0';
BRANCH<='1';
JUMP <='0';
Start Design Files Libraries
RegFile.vhd SIGN_EXTEND.vhd SHIFT_LEFT_2.vhd ALU_CONTROL.vhd Two_to_one_mux_32.vhd ALU.vhd DATA_MEMOMRY.vhd Control_unit.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 20 Col 1 VHDL


ISE Project Navigator (P.20131013) - E:\TERM 6\ARCH\LAB\sdgfszdgzdsrgzgf\Youssef_project\Youssef_project\Joe\Joe.xise - [Control_unit.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Joe
xc7a100t-3csg324
INSTRUCTION_MEMORY - Behavio
PROCESSER - Behavioral (PROC
mux_five - Two_to_one_mux_5
pc_count - PC - Behavioral (PC
add_adder - FULL_ADDER - Beh
ins_memory - InstructionMem
shl_ext - SHIFT_LEFT_EXT_2 - Be
reg - RegFile - Behavioral (RegF
sign_extd - SIGN_EXTEND - Beh
shl - SHIFT_LEFT_2 - Behavioral
add_adder_after_shl - FULL_AD
alu_control_add - ALU_CONTR
mux_one - Two_to_one_mux_3
alu_alu - ALU - Behavioral (ALU
data_memory - DATA_MEMON
mux_two - Two_to_one_mux_3
mux_three - Two_to_one_mux_
mux_four - Two_to_one_mux_3
control_unit_unit - Control_uni
No Processes Running
Processes: control_unit_unit - Control_unit - E
Design Utilities
Check Syntax
7 entity Control_unit is
8 Port (OP_INPUT : in STD_LOGIC_VECTOR (5 downto 0);
9 OP_OUTPUT : out STD_LOGIC_VECTOR (1 downto 0);
10 REGDUST : out STD_LOGIC;
11 ALUSRC : out STD_LOGIC;
12 MEMTOREG : out STD_LOGIC;
13 REGWRITE : out STD_LOGIC;
14 MEMREAD : out STD_LOGIC;
15 MEMWRITE : out STD_LOGIC;
16 BRANCH : out STD_LOGIC;
17 JUMP : out STD_LOGIC);
18 end Control_unit;
19
20 architecture Behavioral of Control_unit is
21
22 begin
23
24 PROCESS(OP_INPUT)
25 BEGIN
26 IF OP_INPUT="000000"
27 THEN
28 OP_OUTPUT <="10";
29 REGDUST<='1';
30 ALUSRC<='0';
31 MEMTOREG<='0';
32 REGWRITE<='1';
33 MEMREAD<='0';
34 MEMWRITE<='0';
35 BRANCH<='0';
36 JUMP <='0';
37 ELSIF OP_INPUT="100011"
38 THEN
39 OP_OUTPUT <="00";
40 REGDUST<='0';
Start Design Files Libraries
RegFile.vhd SIGN_EXTEND.vhd SHIFT_LEFT_2.vhd ALU_CONTROL.vhd Two_to_one_mux_32.vhd ALU.vhd DATA_MEMOMRY.vhd Control_unit.vhd
Errors
Console Errors Warnings Find in Files Results
Ln 20 Col 1 VHDL