Analog IC Design
Lab 04
Common Drain Frequency Response

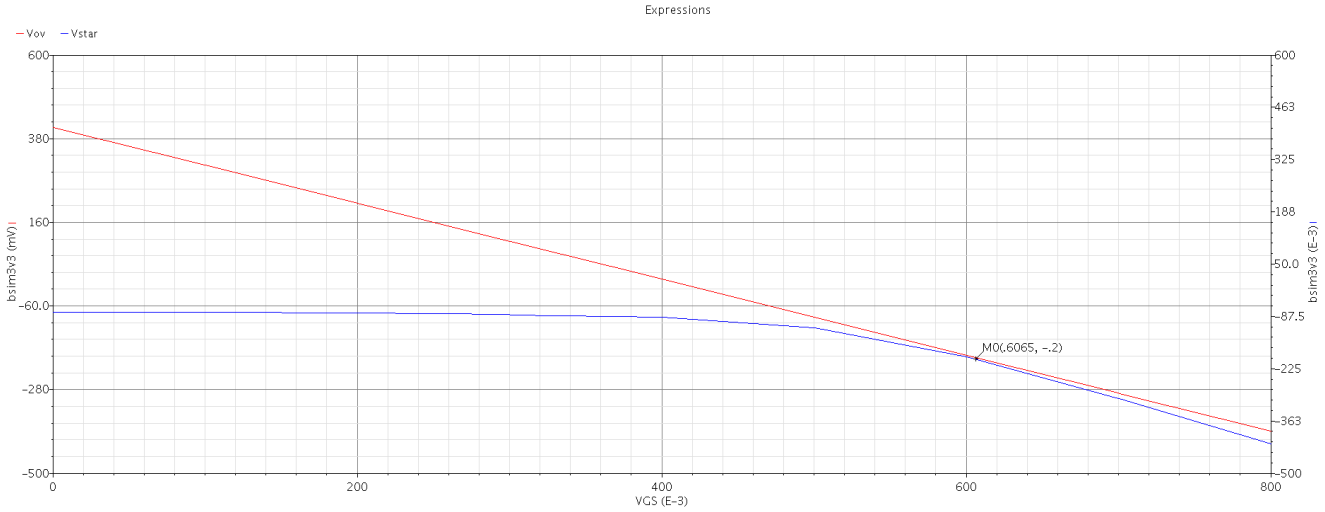
Part 1: Sizing Chart

Our design specs.

L=1uM V*=200mV VDD=1.8V Id=10uA Start with w=10uM

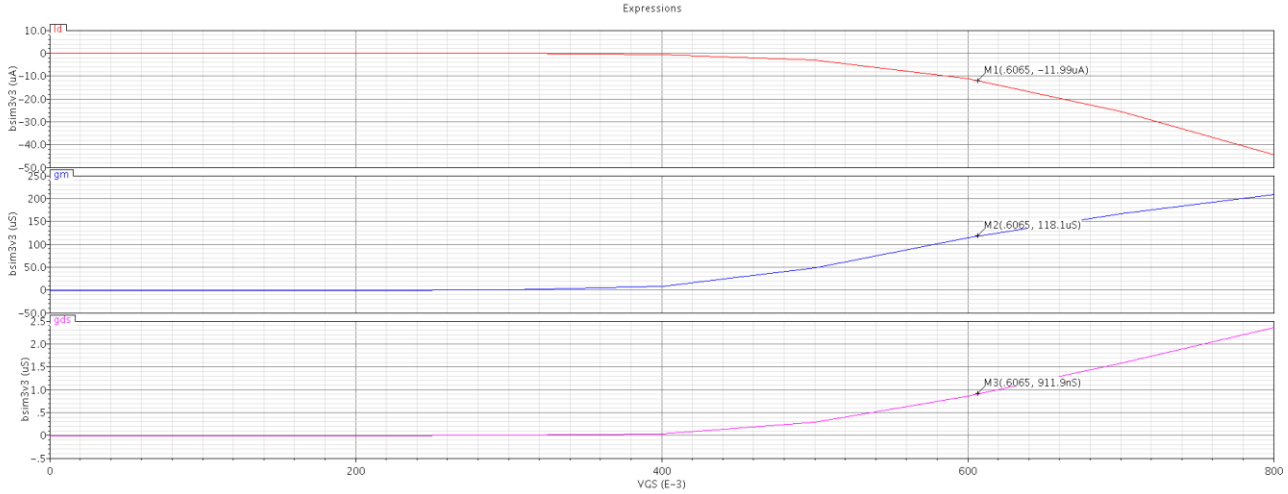
Sweep VGS from 0 to ≈V_{TH}+0.4V with 10mV step. Set V_{DS}=V_{DD}/2.

Plot V_* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range.



Vgsq=606.5mV Vovq=-192mV

Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.



Idx=-11.99uA gmx=118.1uS gdsx=911.9nS

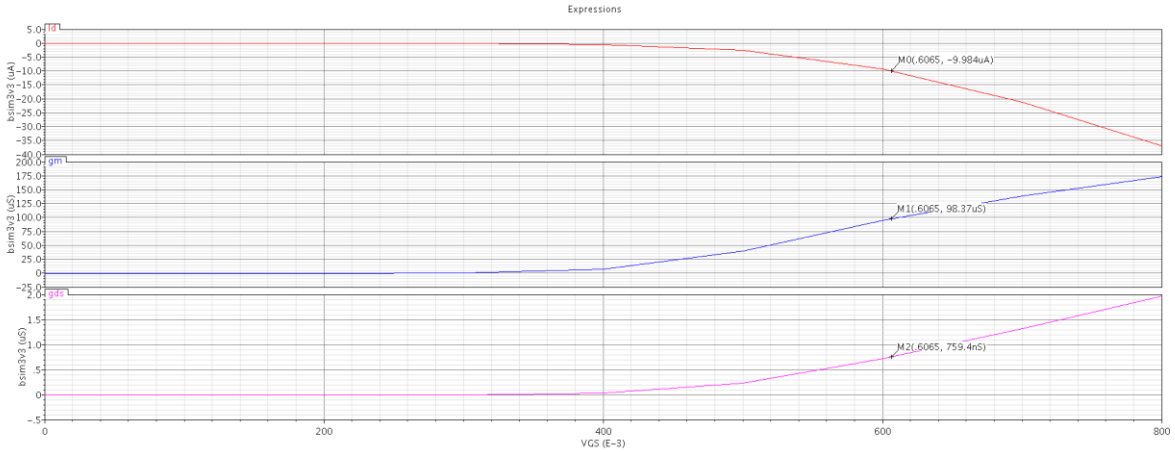
we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be I_{DQ}=10μA as given in the specs. Calculate W as shown below.

Wnew=10u*10u/11.99u=8.34uM

Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, r_o=1/g_{ds} is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

gmq=98.495uS gdsq=760.52nS ro=1.314Mohm

and here are the values calculated from cadence at w=8.34 uM

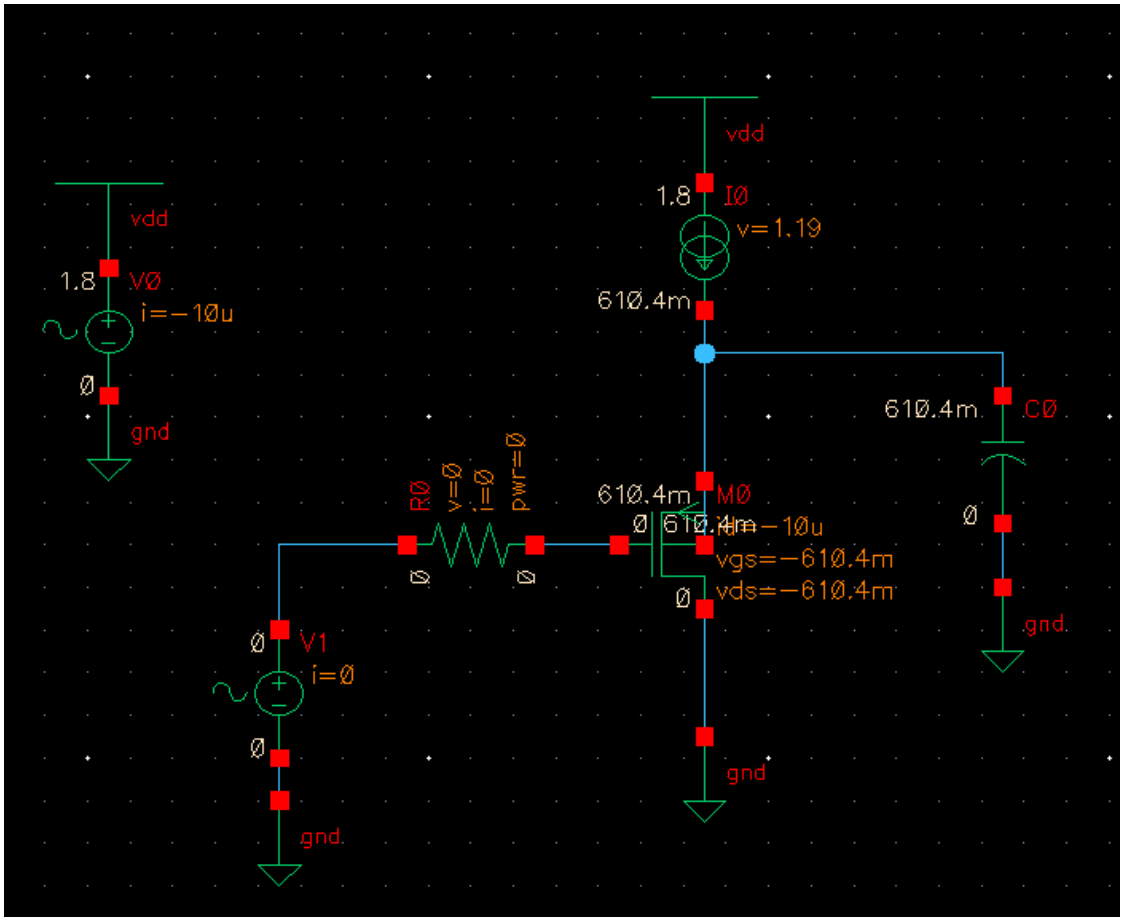


We can see that the values are close to the cross multiplication results.

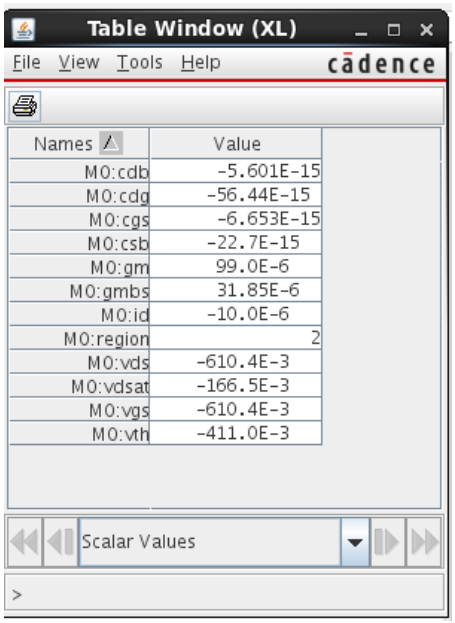
PART 2: CD Amplifier

OP (Operating Point) Analysis:

Schematic:



Simulate the OP point. Report a snapshot clearly showing the following parameters.



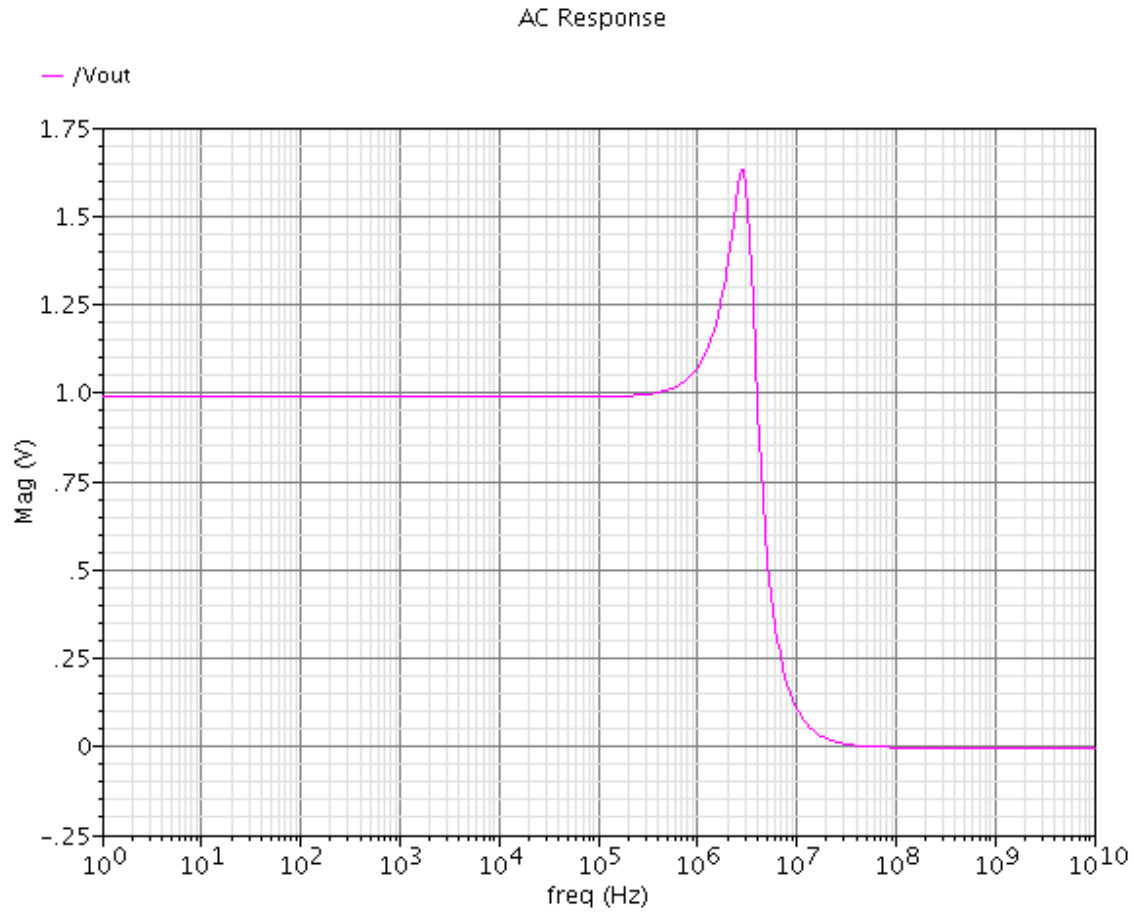
Check that the transistor operates in saturation.

Transistor is in region 2 which means saturation.

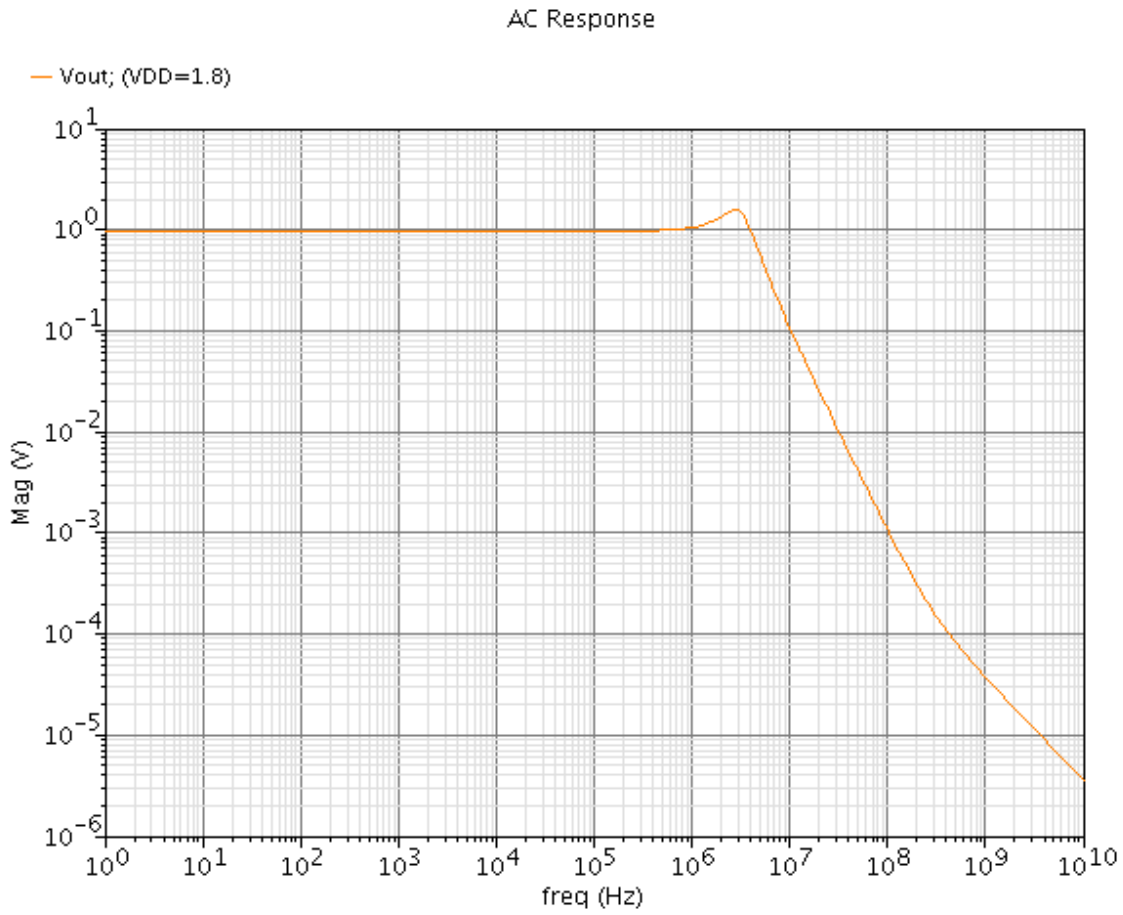
AC Analysis

Perform AC analysis (1Hz:10GHz, logarithmic, 20points/decade) to investigate the frequency domain peaking.

Report the Bode plot magnitude.



Vout in log scale:



Do you notice frequency domain peaking?

yes, the peaking is very clear at the log scale as shown in the above figure.

And the value of peaking in db is:

Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:CD_Amplifier:1	Vout				
AIC_Training:CD_Amplifier:1	Peaking_DB	4.28			

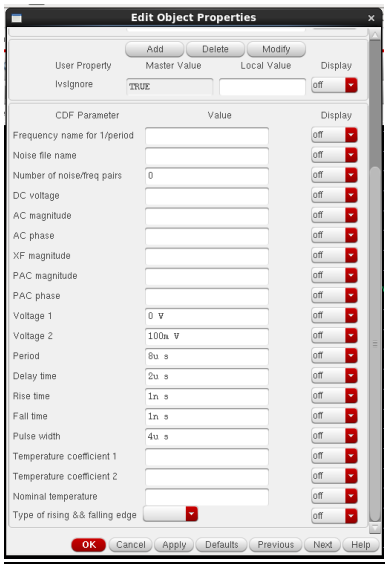
Analytically calculate quality factor (use approximate expressions). Is the system underdamped or overdamped?

$$Q = \sqrt{\frac{g_m(C_{gs}+C_{gd})*(R_{sig})}{C_l}} = 2.499$$ underdamped system.

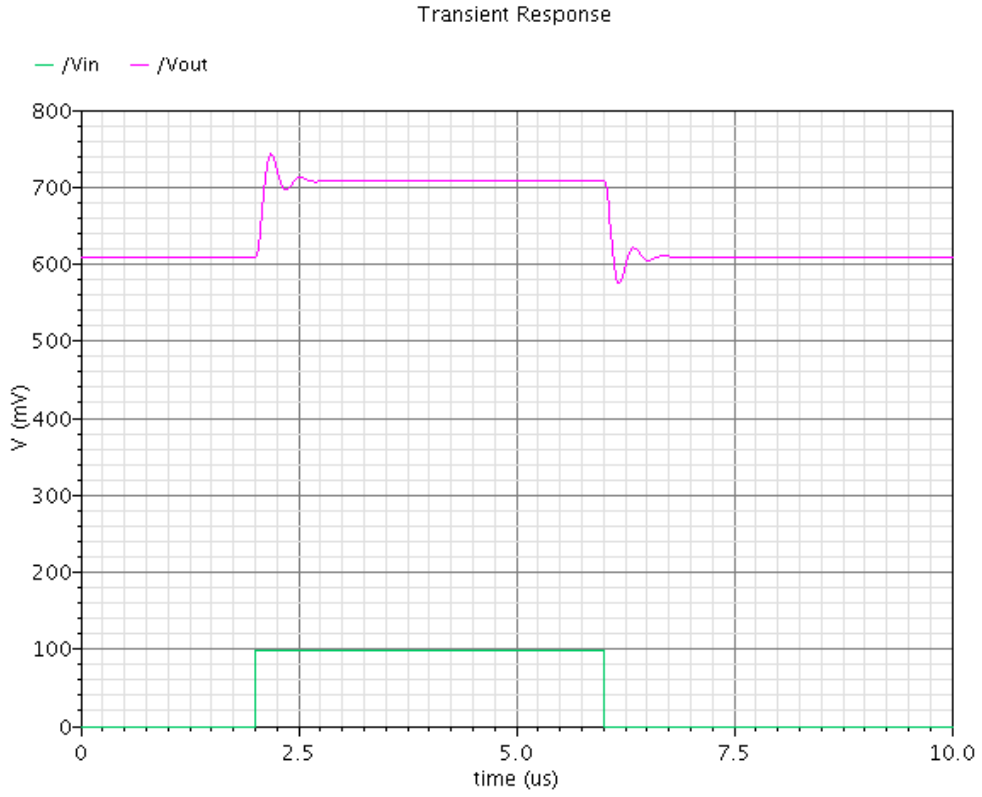
Transient Analysis:

Use a pulse source (pulse_v_source) as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis (max step = 10n) for 10us to investigate the time domain ringing.

Source properties:



Report Vin and Vout overlaid vs time.



Calculate the DC voltage difference (DC shift) between Vin and Vout

The dc voltage difference (dc shift) is clear from the figure =600mV

What is the relation between the DC shift and VGS?

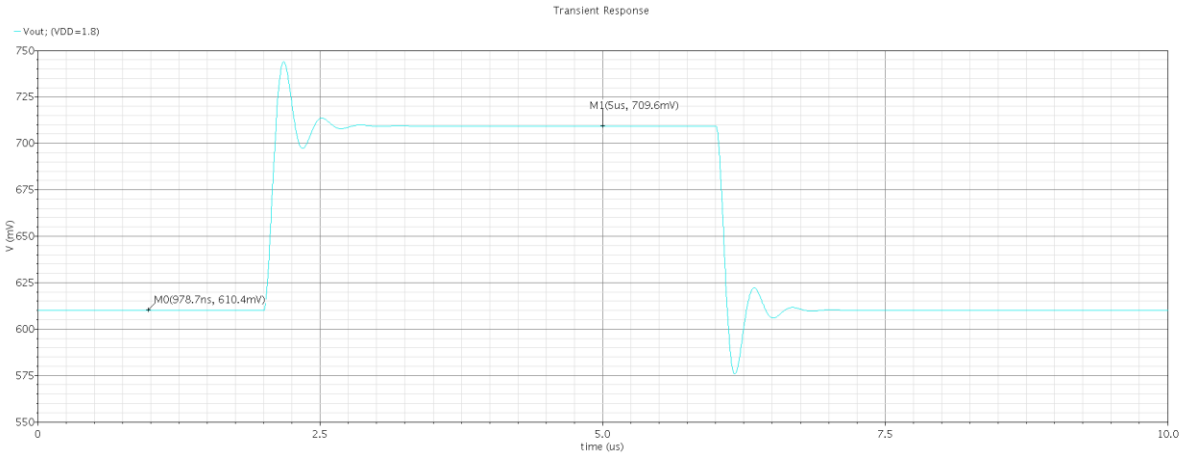
The dc shift is equal to Vsg DC bias point.

So if the source terminal voltage inc the gate terminal follows to stay at Vsg

How to shift the signal down instead of shifting it up?

in our case we used Pmos with the CD and it shifted the signal up , we want to shift the signal down which is a complementary action so we can use the same topology but use it with Nmos.

Do you notice time domain ringing?



the ringing is very clear in the time domain
I used these values to calculate the overshoot

Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:CD_Amplifier:1	Vout				
AIC_Training:CD_Amplifier:1	Vin				
AIC_Training:CD_Amplifier:1	Overshoot	34.93			

The overshoot is about 35%