Analog IC Design
Design Challenge
Digitally Controlled Variable Gain Amplifier (VGA)

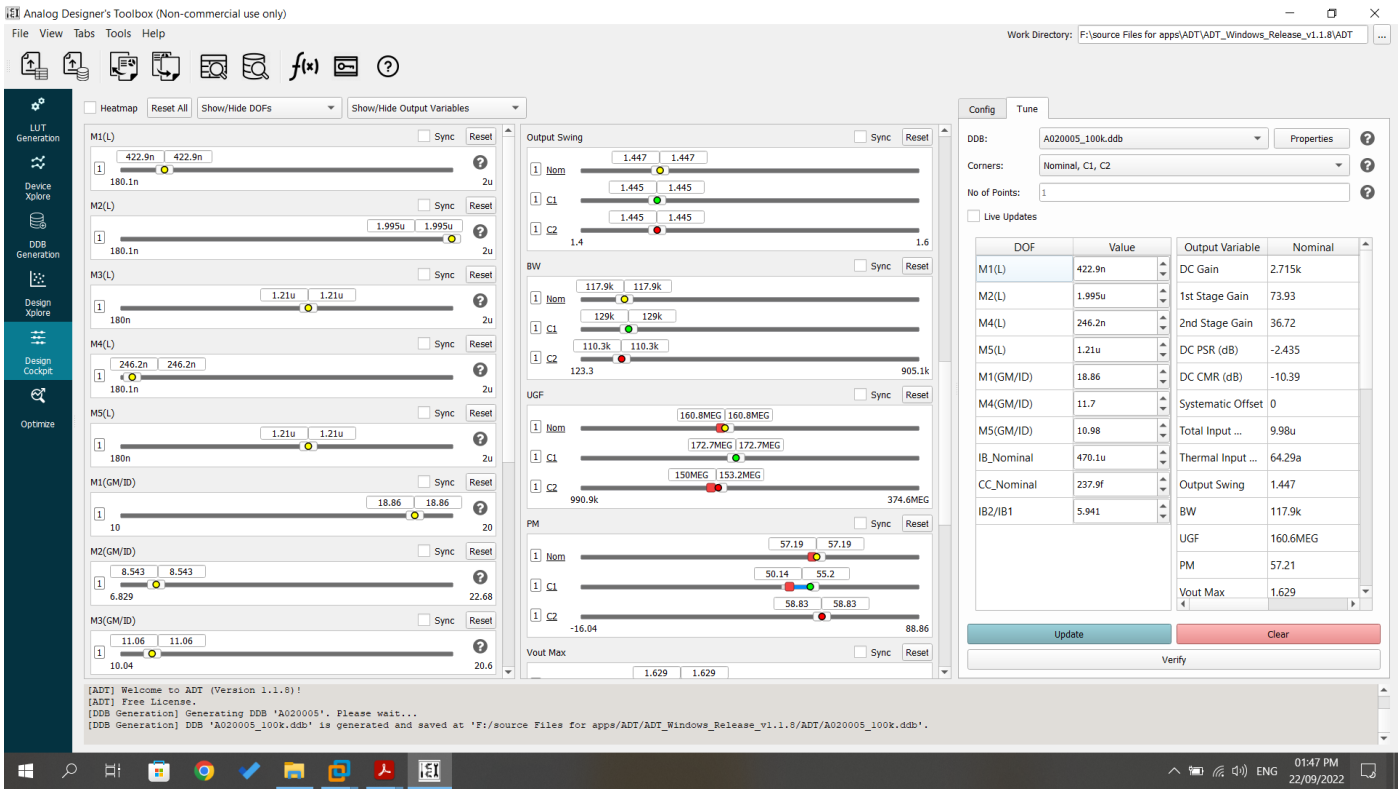
OTA selection and design strategy.

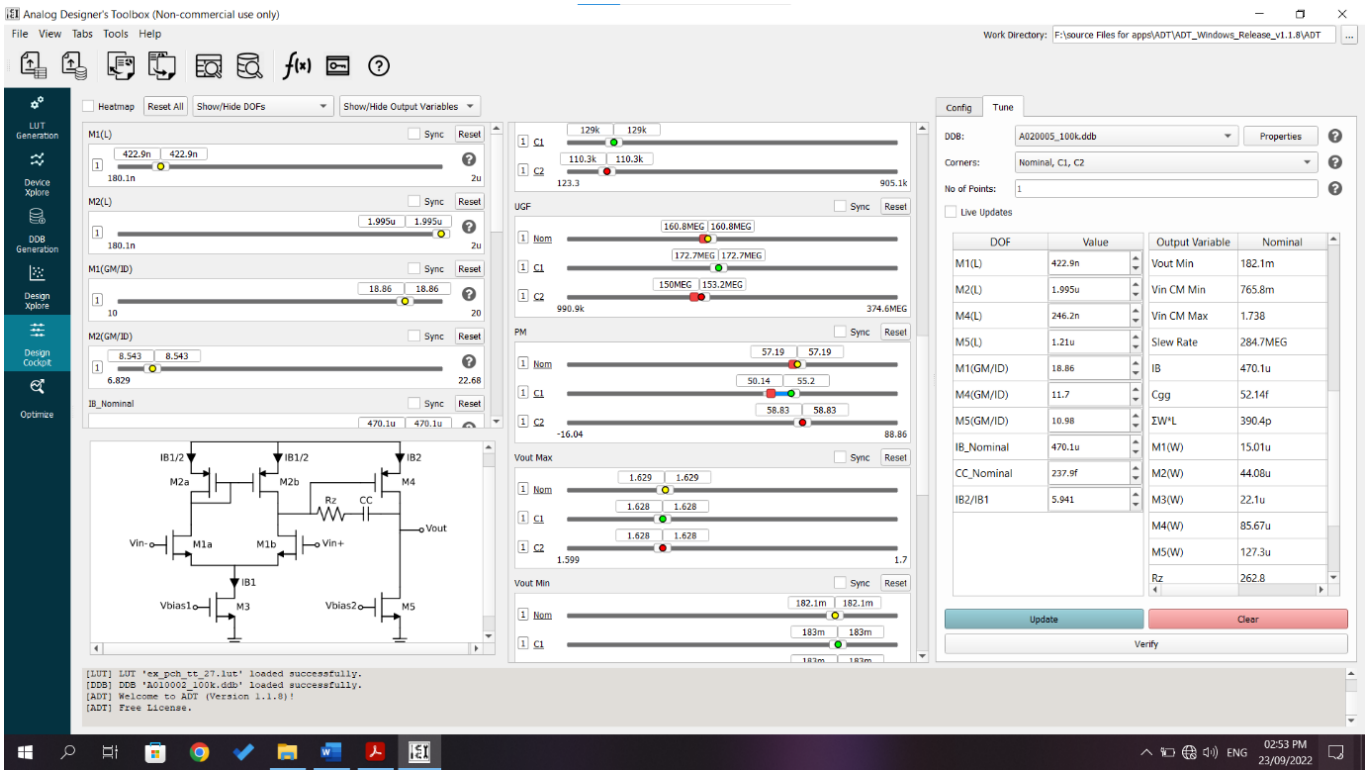
Two stage miller OTA.

NMOS input pair.

Non-inverting OP amp.

Here are all the devices sizing.



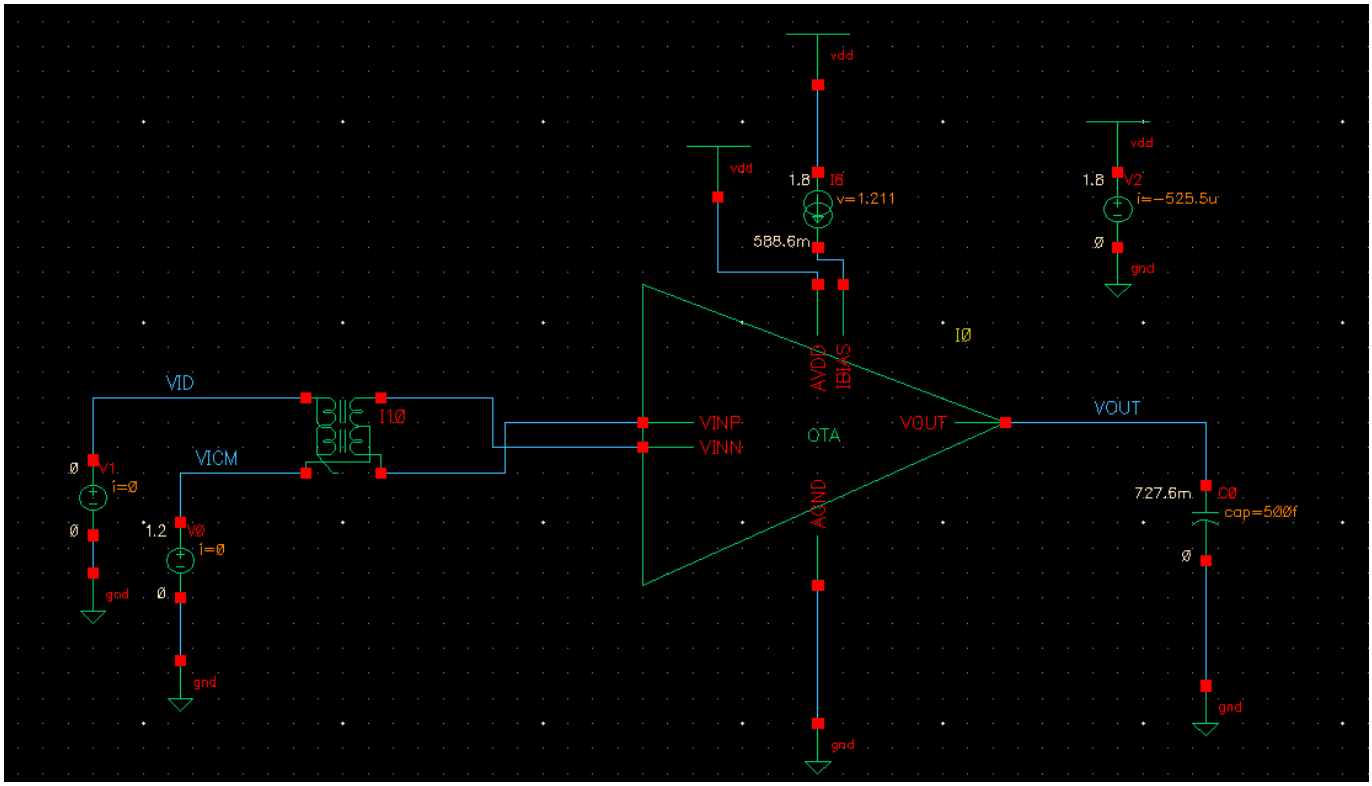


I used ADT tool to help me do the design and meet the specs.

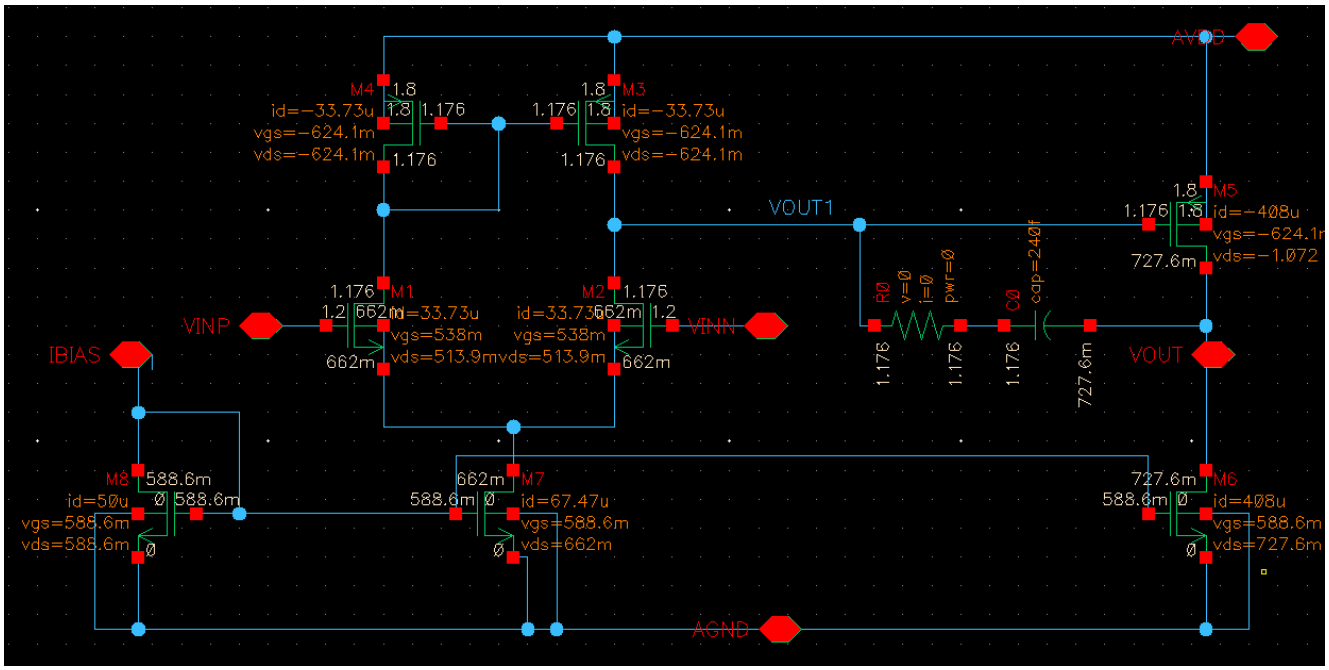
Here I needed an open loop gain of 2000 and UGF of 150 M and phase margin above 50.

I put these specs and ADT and then started simulation.

The block schematic:



The OTA schematic and operating point:



The open loop specs:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Design_challenge:open_loop_simulation:1	Aol	2.814k			
Design_challenge:open_loop_simulation:1	Aol_dB	68.99			
Design_challenge:open_loop_simulation:1	BW	110.2k			
Design_challenge:open_loop_simulation:1	GBW	310.7M			
Design_challenge:open_loop_simulation:1	UGF	152.9M			
Design_challenge:open_loop_simulation:1	PM	57.15			

Gain above 2000 satisfied.

UGF satisfied.

Phase margin satisfied.

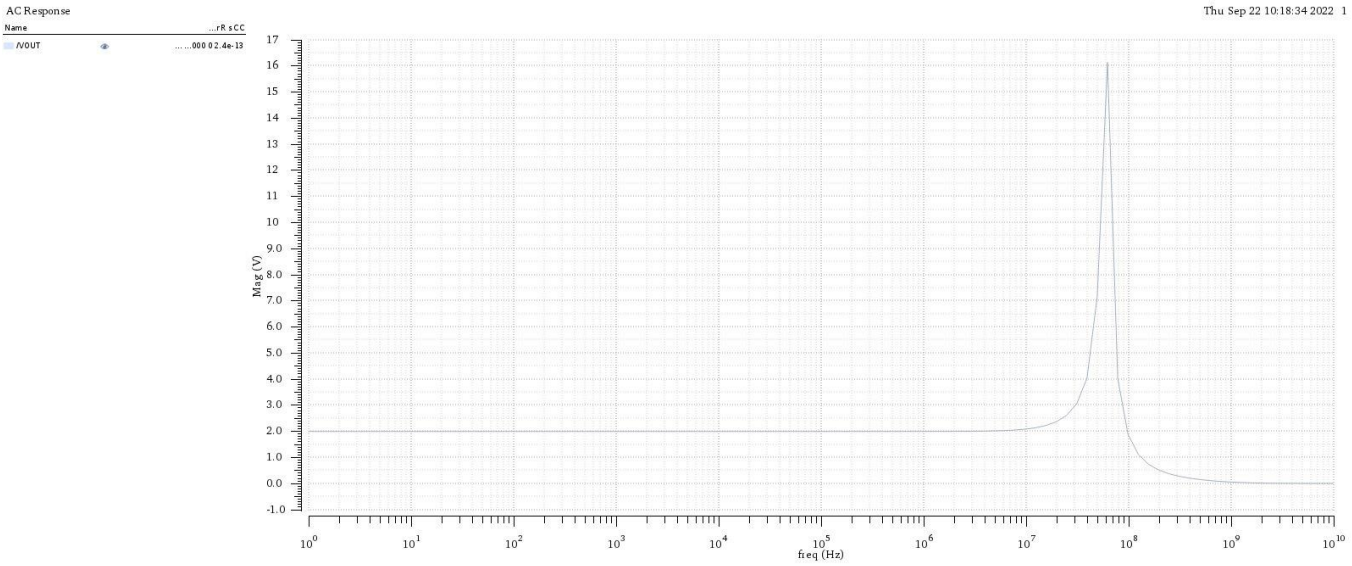
Here is the open loop simulation with the corners and variations of the caps and the resistors:

	Parameter	Nominal						C0_0	C0_1
	CC	240f						216f	264f

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1
Design_challenge:open_loop_simulation:1	Aol	2.814k				2.814k	2.814k	2.814k	2.814k
Design_challenge:open_loop_simulation:1	Aol_dB	68.99				68.99	68.99	68.99	68.99
Design_challenge:open_loop_simulation:1	BW	110.2k				101.9k	119.5k	119.5k	101.9k
Design_challenge:open_loop_simulation:1	GBW	310.7M				287.4M	336.9M	336.9M	287.4M
Design_challenge:open_loop_simulation:1	UGF	152.9M				145.2M	161.8M	161.8M	145.2M

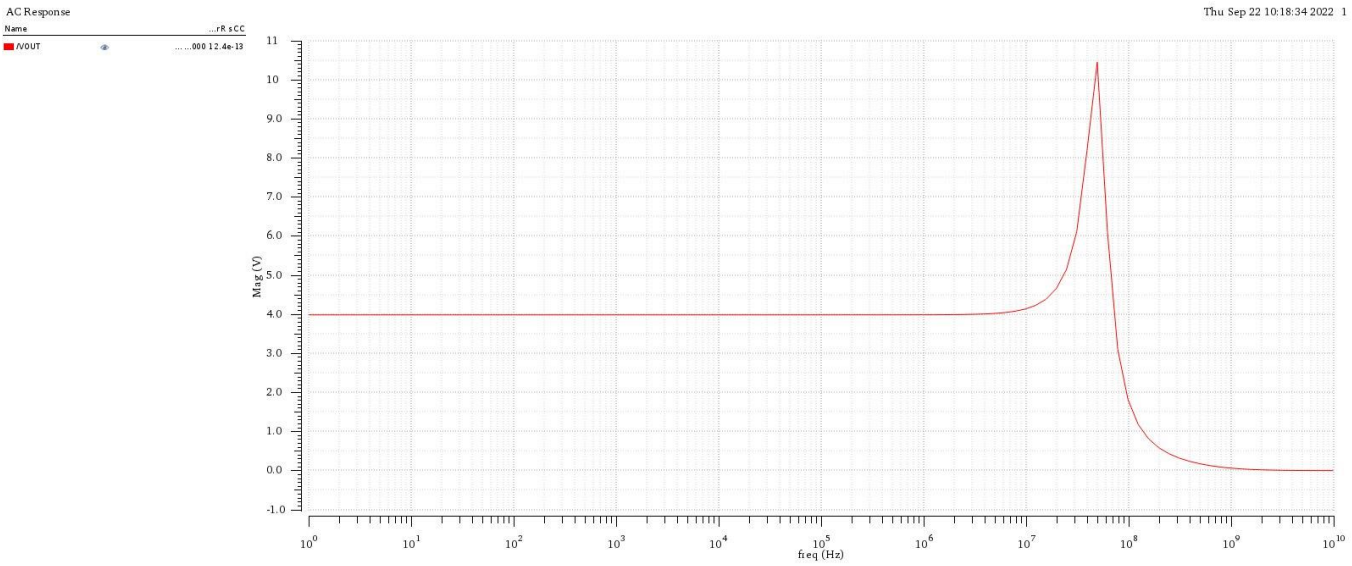
The closed loop simulations:

Closed loop gain at D0 signal = 0
the closed loop gain is equal to 2 as designed as beta here is equal to 0.5



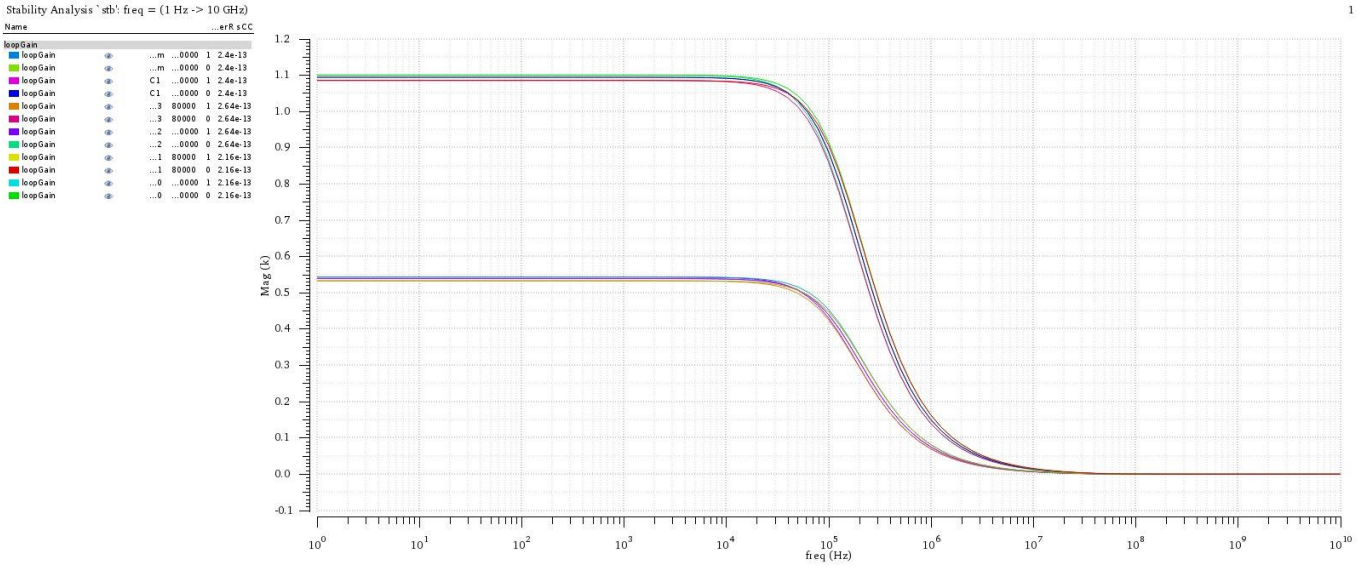
The closed loop gain at D0 = 1

the closed loop gain is equal to 4 as designed as beta here is equal to 0.25



So, the closed loop gain spec is satisfied.

The loop gain:



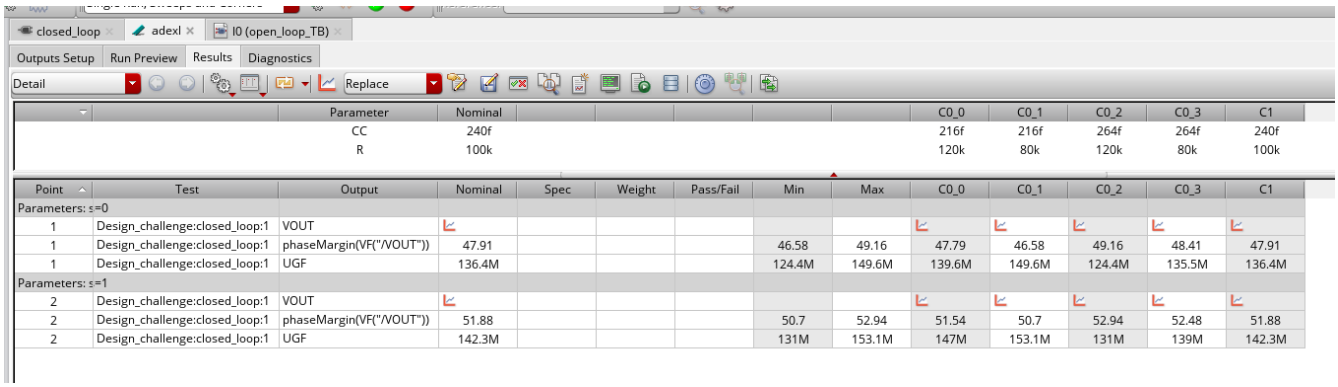
Here the loop gain of the closed loop at D0 = 0 and D0 = 1

When the digital signal is zero, beta = 0.5 so the loop gain which is equal to B*Aol = 0.5*2K = 1k

When the digital signal is 1, beta = 0.25 so the loop gain which is equal to B*Aol = 0.25*2K = 0.5k

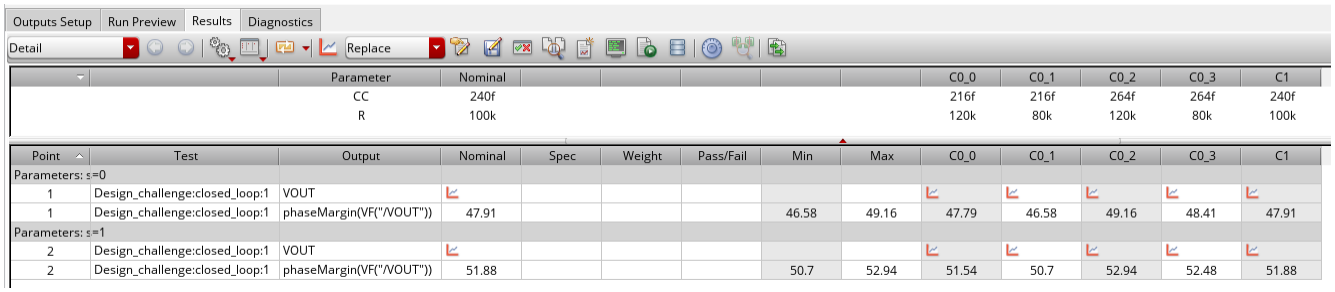
The other curves are those of the corners.

Here are the closed loop specs with the corners:



Parameter	Nominal	C0_0	C0_1	C0_2	C0_3	C1
CC	240f	216f	216f	264f	264f	240f
R	100k	120k	80k	120k	80k	100k

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3	C1
Parameters: s=0													
1	Design_challenge:closed_loop:1	VOUT											
1	Design_challenge:closed_loop:1	phaseMargin(VF("/VOUT"))	47.91				46.58	49.16	47.79	46.58	49.16	48.41	47.91
1	Design_challenge:closed_loop:1	UGF	136.4M				124.4M	149.6M	139.6M	149.6M	124.4M	135.5M	136.4M
Parameters: s=1													
2	Design_challenge:closed_loop:1	VOUT											
2	Design_challenge:closed_loop:1	phaseMargin(VF("/VOUT"))	51.88				50.7	52.94	51.54	50.7	52.94	52.48	51.88
2	Design_challenge:closed_loop:1	UGF	142.3M				131M	153.1M	147M	153.1M	131M	139M	142.3M



Parameter	Nominal	C0_0	C0_1	C0_2	C0_3	C1
CC	240f	216f	216f	264f	264f	240f
R	100k	120k	80k	120k	80k	100k

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3	C1
Parameters: s=0													
1	Design_challenge:closed_loop:1	VOUT											
1	Design_challenge:closed_loop:1	phaseMargin(VF("/VOUT"))	47.91				46.58	49.16	47.79	46.58	49.16	48.41	47.91
Parameters: s=1													
2	Design_challenge:closed_loop:1	VOUT											
2	Design_challenge:closed_loop:1	phaseMargin(VF("/VOUT"))	51.88				50.7	52.94	51.54	50.7	52.94	52.48	51.88

Loop gain phase margin with the corners:

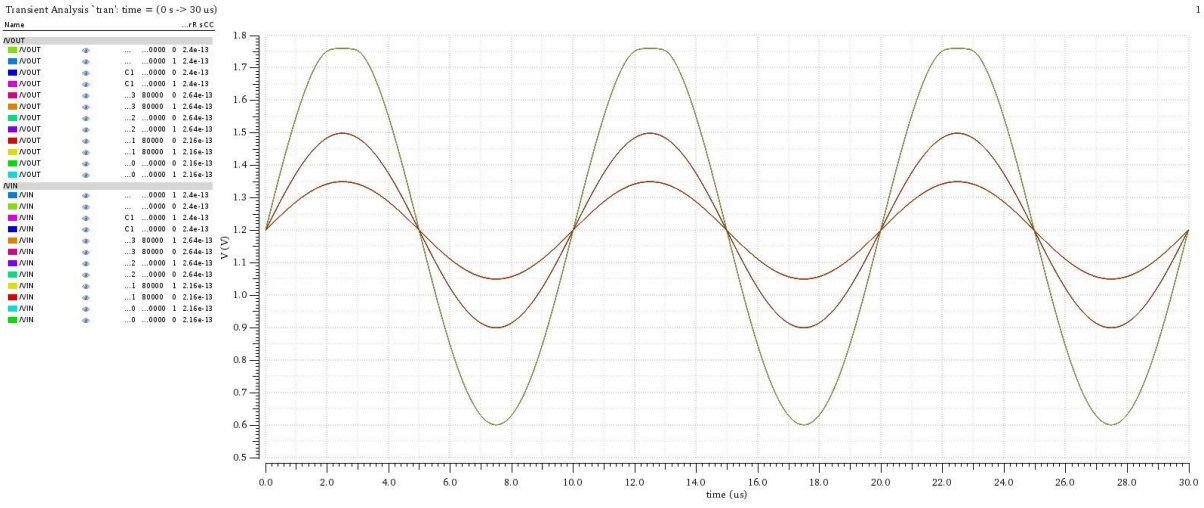
	1
CC	216.0E-15
/phaseMargin Corner C0_1 R 80000 s 0 (Deg)	10.65
/phaseMargin Corner C0_1 R 80000 s 1 (Deg)	27.79
/phaseMargin Corner C0_0 R 120000 s 0 (Deg)	4.503
/phaseMargin Corner C0_0 R 120000 s 1 (Deg)	19.84
CC	240.0E-15
/phaseMargin Corner C1 R 100000 s 0 (Deg)	9.048
/phaseMargin Corner C1 R 100000 s 1 (Deg)	25.71
/phaseMargin Corner nom R 100000 s 0 (Deg)	9.048
/phaseMargin Corner nom R 100000 s 1 (Deg)	25.71
CC	264.0E-15
/phaseMargin Corner C0_3 R 80000 s 0 (Deg)	14.25
/phaseMargin Corner C0_3 R 80000 s 1 (Deg)	32.20
/phaseMargin Corner C0_2 R 120000 s 0 (Deg)	8.115
/phaseMargin Corner C0_2 R 120000 s 1 (Deg)	24.35

Compare to open loop specs and comment.

	Open loop	Closed loop
UGF @D0=0,D=1	152.9M	136.4M,142.3M
PM @ D0=0,D0=1	57.15	47.9,51.8

The closed loop parameters decreased a bit from the open loop.

Closed loop transient analysis:



Vout

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