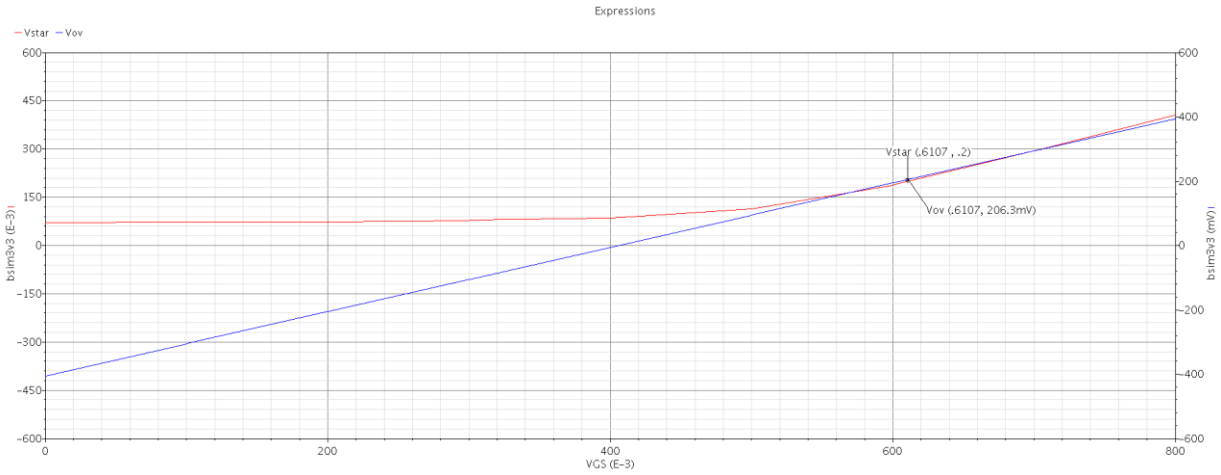
Analog IC Design
Lab 05
Simple vs Low Compliance Cascode Current Mirror

Part 1: Sizing Chart

V*=200 mV VDD=1.8 V Iref=20 uA W=10 uM L=1uM

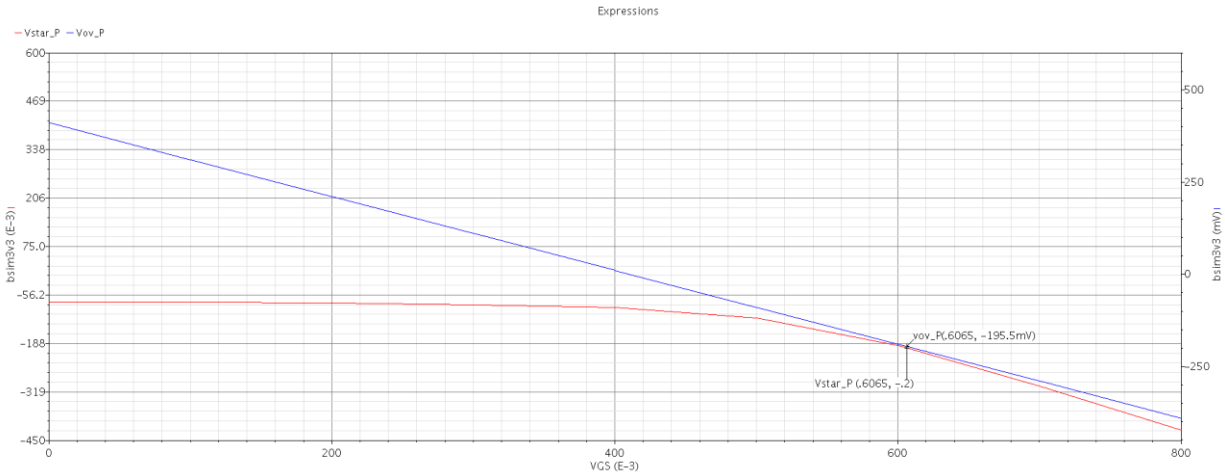
Plot $V*$ and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range, Locate the point at which V_*=200mV. Find the corresponding V_{ovQ} and V_{GSQ}.

For NMOS



Vgsq=610.7 mV Vovq=206.3 mV

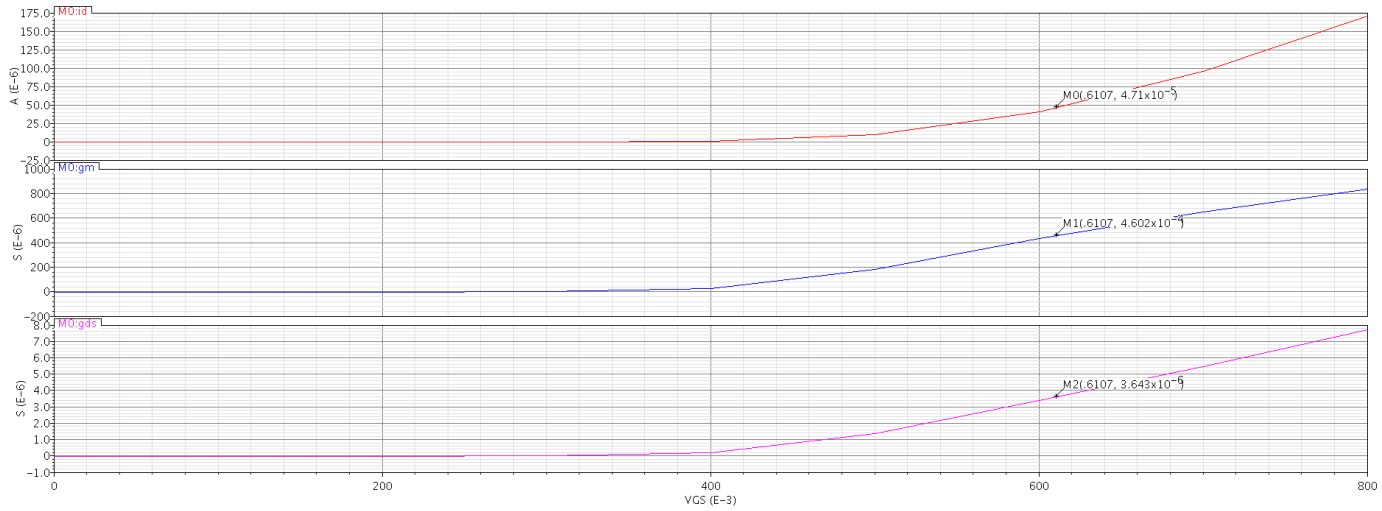
For PMOS



Vgsq=606.5 mV Vovq=-195.5 mV

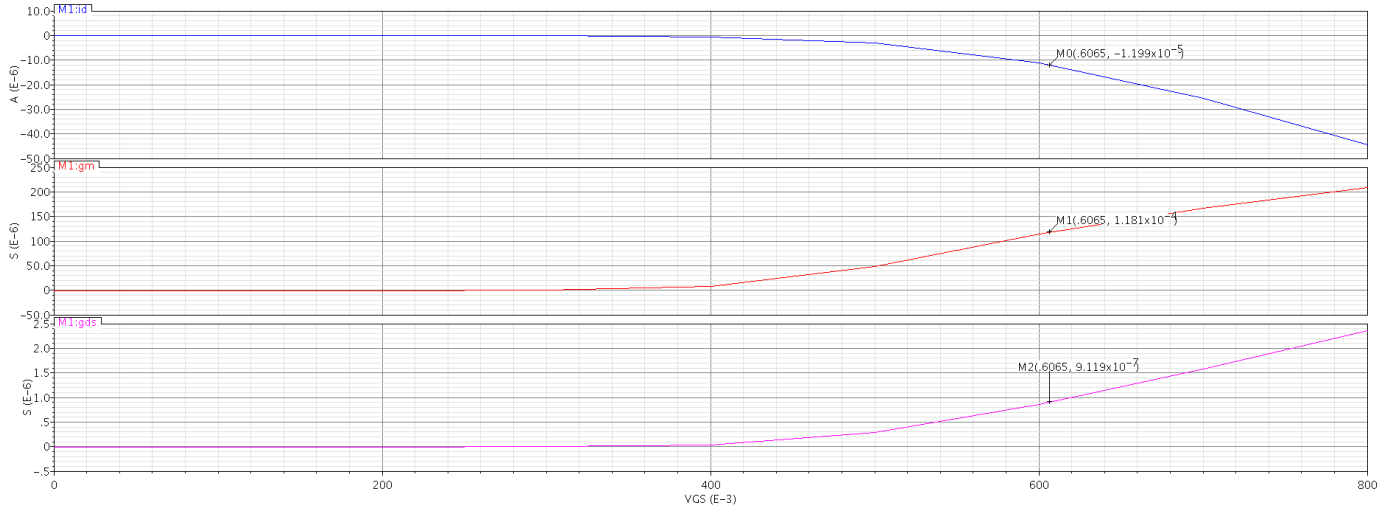
Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.

Plots for NMOS



Idx=47.1 uA gmx=0.462 mS gdsx=3.643 uS

Plots for PMOS



Idx=-11.99 uA gmx=0.1081 mS gdsx=0.9119 uS

Therefore we can use the cross multiplication to calculate theWn,Wp of the mosfets

WN=10u*20u/47.1u=4.246 uM

WP=10u*10u/11.99u=16.68uM

Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

For NMOS:

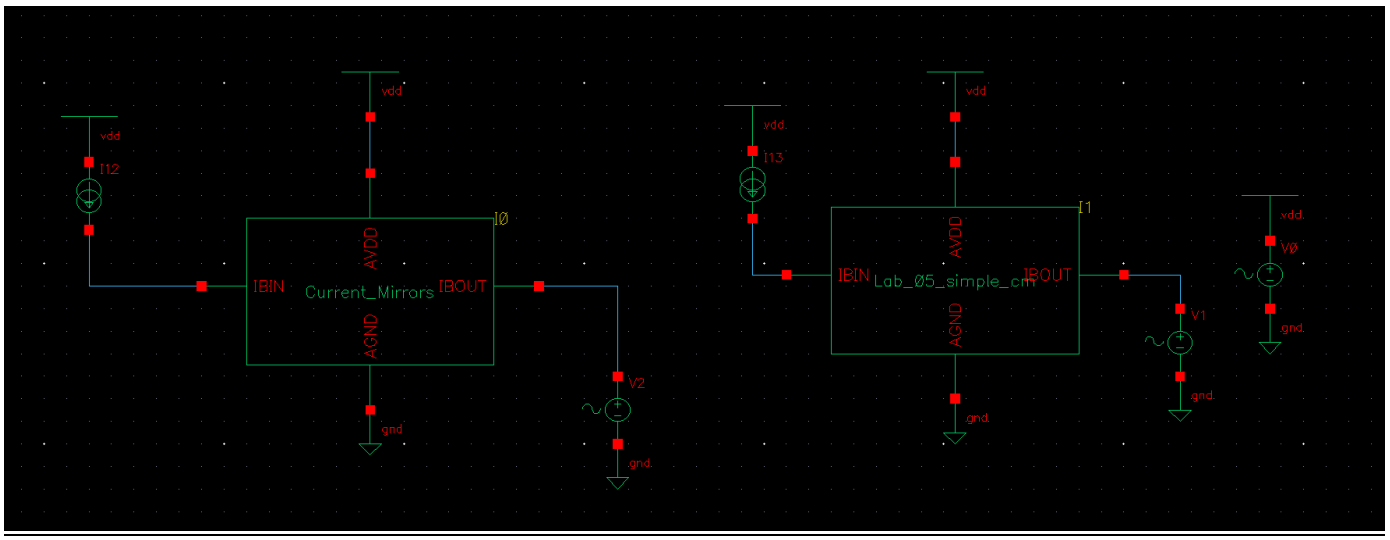
Gmx=0.2954 mS gdsq=1.5468 uS ro=646.488 Kohm

For PMOS:

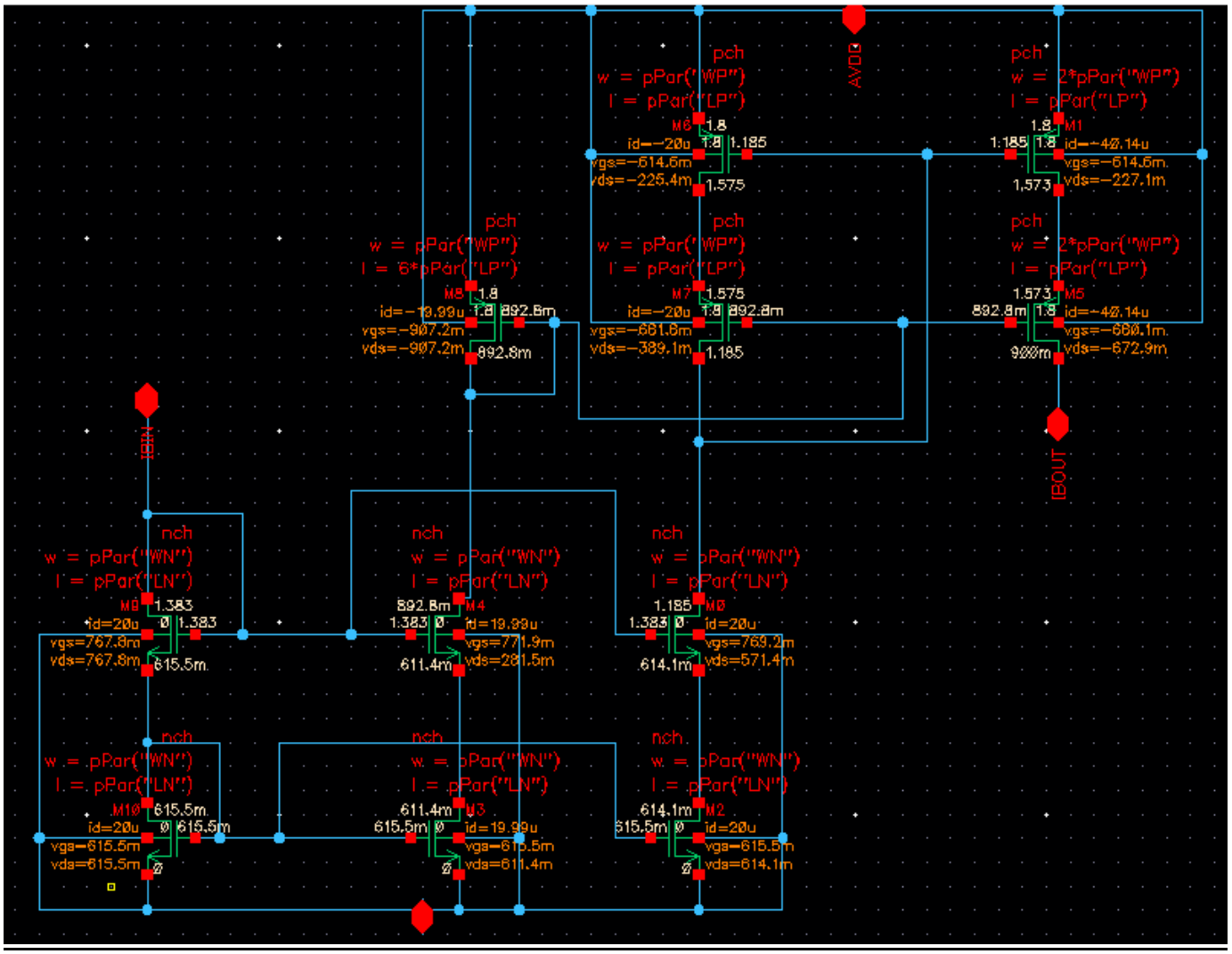
Gmq=196.99 uS gdsq=1.521 uS ro=657.44 kohm

PART 2: Current Mirror

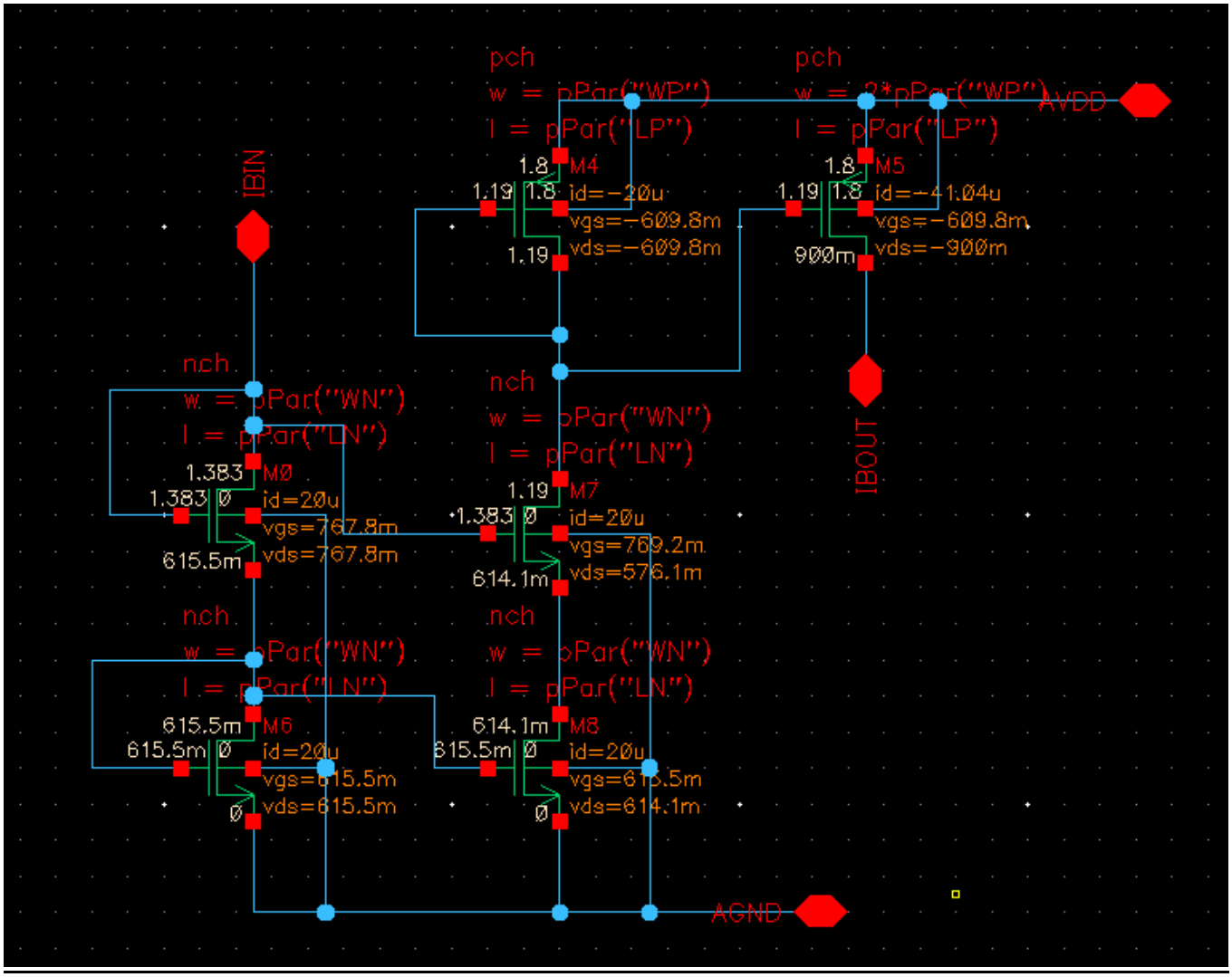
Schematic of the two CMs with DC node voltages clearly annotated at VOUT = VDD/2 (double click the symbol to go to lower level of hierarchy and show the schematic).



Current mirror wide-swing:



Simple Current mirror:



Snapshots showing the following parameters for all transistors at VOUT = VDD/2. You may summarize the results in a table.

Name	/I0/M0	/I0/M1	/I0/M10	/I0/M2	/I0/M3	/I0/M4	/I0/M5	/I0/M6	/I0/M7	/I0/M8	/I0/M9	/I1/M0	/I1/M4	/I1/M5	/I1/M6	/I1/M7	/I1/M8
cgd	-1.973f	-25.56f	-1.974f	-1.974f	-1.974f	-2.158f	-21.99f	-12.81f	-11.21f	-11.55f	-1.963f	-1.963f	-11f	-21.94f	-1.974f	-1.972f	-1.974f
cgs	-28.73f	-226.4f	-29.24f	-29.24f	-29.24f	-28.78f	-225.4f	-113.2f	-112.8f	-644.2f	-28.71f	-28.71f	-112.9f	-225.6f	-29.24f	-28.73f	-29.24f
gds	1.828u	14.2u	1.694u	1.695u	1.697u	3.942u	3.154u	7.239u	1.993u	221.9n	1.699u	1.699u	1.639u	3.13u	1.694u	1.823u	1.695u
gm	202.5u	384.7u	198.1u	198.1u	198.1u	199.6u	393.4u	191.6u	194.4u	70.92u	203u	203u	198.5u	405.2u	198.1u	202.5u	198.1u
gmoverid	10.13	9.584	9.907	9.907	9.908	9.981	9.801	9.579	9.722	3.547	10.15	10.15	9.925	9.873	9.907	10.13	9.907
id	20u	-40.14u	20u	20u	19.99u	19.99u	-40.14u	-20u	-20u	-19.99u	20u	20u	-20u	-41.04u	20u	20u	20u
region	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2		
type	0	1	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0
vds	571.4m	-227.1m	615.5m	614.1m	611.4m	281.5m	-672.9m	-225.4m	-389.1m	-907.2m	767.8m	767.8m	767.8m	-609.8m	-900m	615.5m	576.1m	614.1m
vdsat	165.4m	-171.1m	158.6m	158.6m	158.6m	166.6m	-172.4m	-170.6m	-173.6m	-409.8m	165m	165m	-167m	-167.5m	158.6m	165.4m	158.6m
vgs	769.2m	-614.6m	615.5m	615.5m	615.5m	771.9m	-680.1m	-614.6m	-681.8m	-907.2m	767.8m	767.8m	-609.8m	-609.8m	615.5m	769.2m	615.5m
vth	576.5m	-411.1m	405.9m	405.9m	406m	577.5m	-483.3m	-411.1m	-482.6m	-380.9m	575.7m	575.7m	-411.1m	-411.1m	405.9m	576.5m	405.9m

Region 0 is cutoff.
Region 1 is linear.
Region 2 is saturation .
Region 3 is subthreshold.
Region 4 is breakdown.

Type 0 is nMOS.
Type 1 is pMOS.

Check that all transistors have V_{GS}, g_m and g_{ds} as designed in Part 1

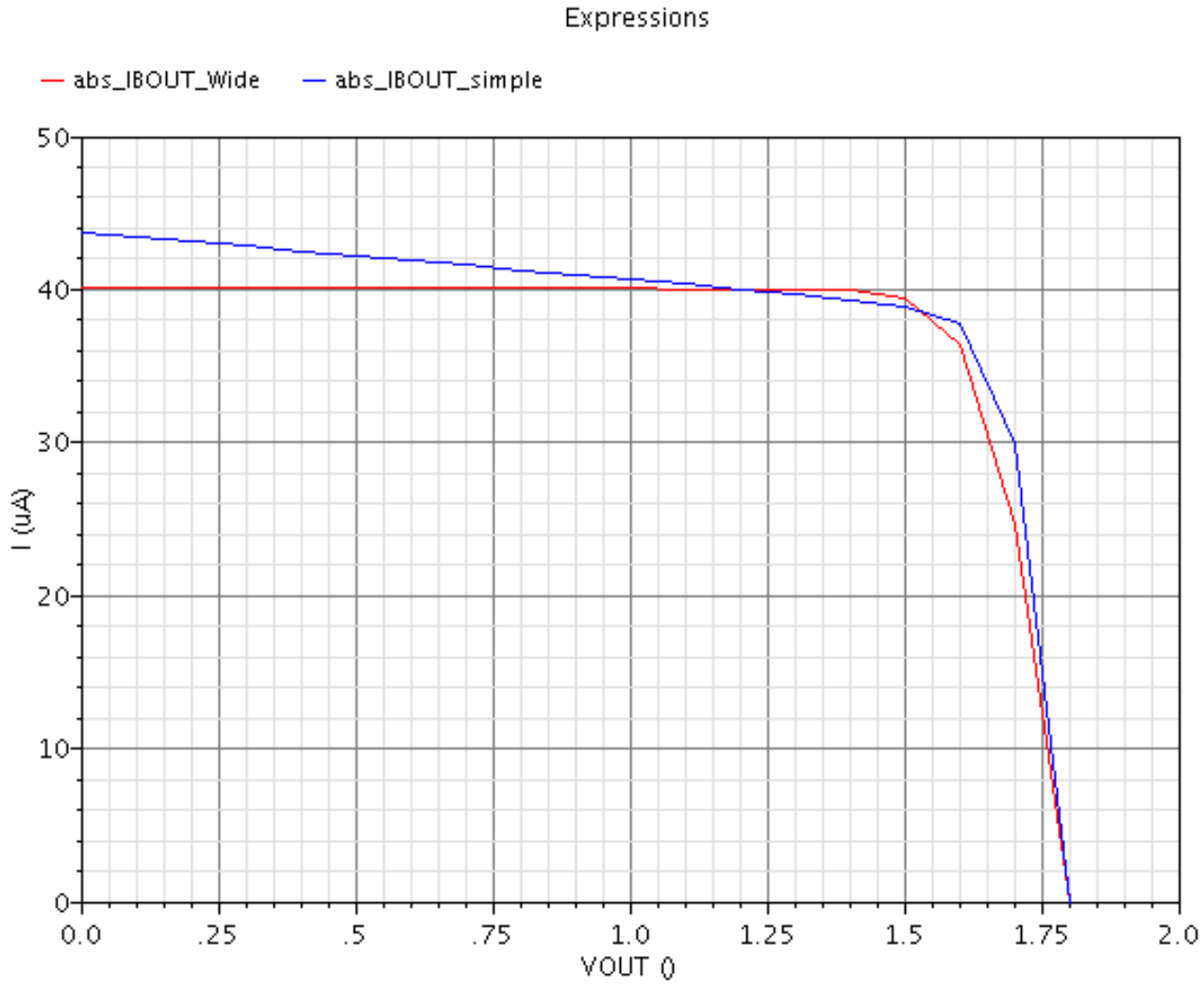
All mosfets which are either bulks connected to the ground (the mosfets at the bottom layer of the schematic) or their bulks connected to the VDD (the PMOS at the top layer of the schematic) they are almost as the designed ones in part 1

While the other mosfets which have their body terminal floating suffer from the body effect which will increase their Vth and then decrease their Vov so to sustain the same overdrive voltage their Vgs increases.

Are all transistors operating in saturation?

Yes, all transistors are in region 2 (saturation)

Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report IBOUT vs VOUT for the two CMs overlaid in the same plot.



Comment on the difference between the two circuits.

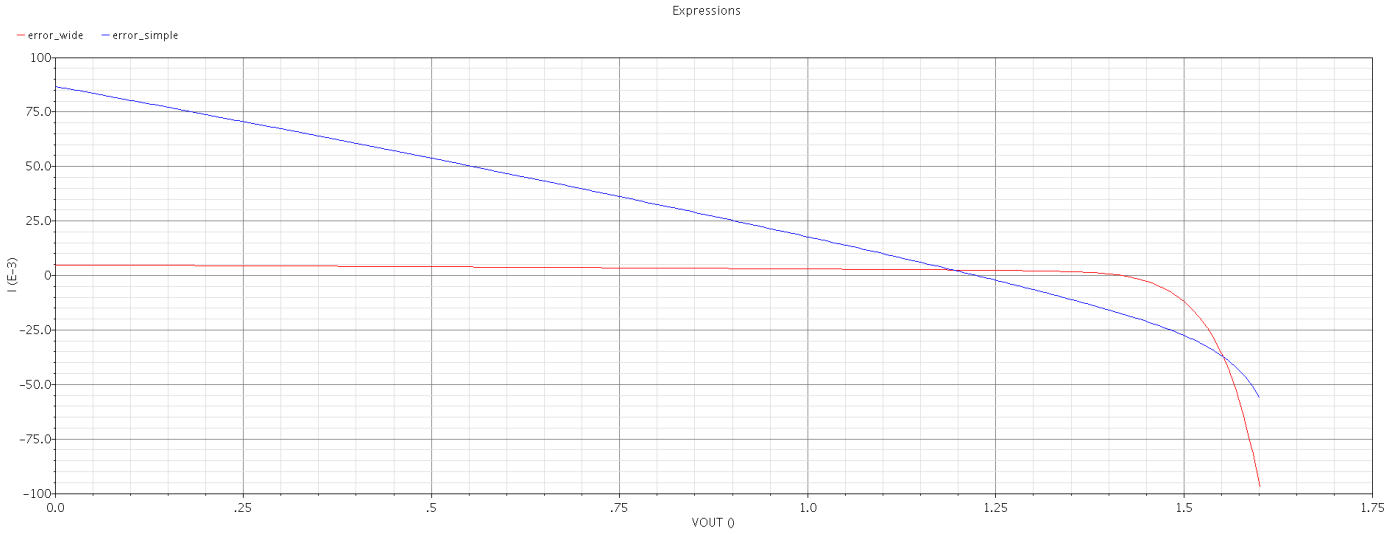
The wide-swing CM gives more accurate result which is almost 40 uA while the simple CM gives a little bit of an error in its output current.

But both current mirrors fail after some point where some mosfets will get out of saturation

IBOUT of the simple CM is exactly equal to IBIN*2 at a specific value of VOUT. Why?

Because at this specific point , Vds of the two mirror mosfets are the same so there won't be any mismatch error the the mirroring will be more accurate as Vgs is the same and Vds is the same.

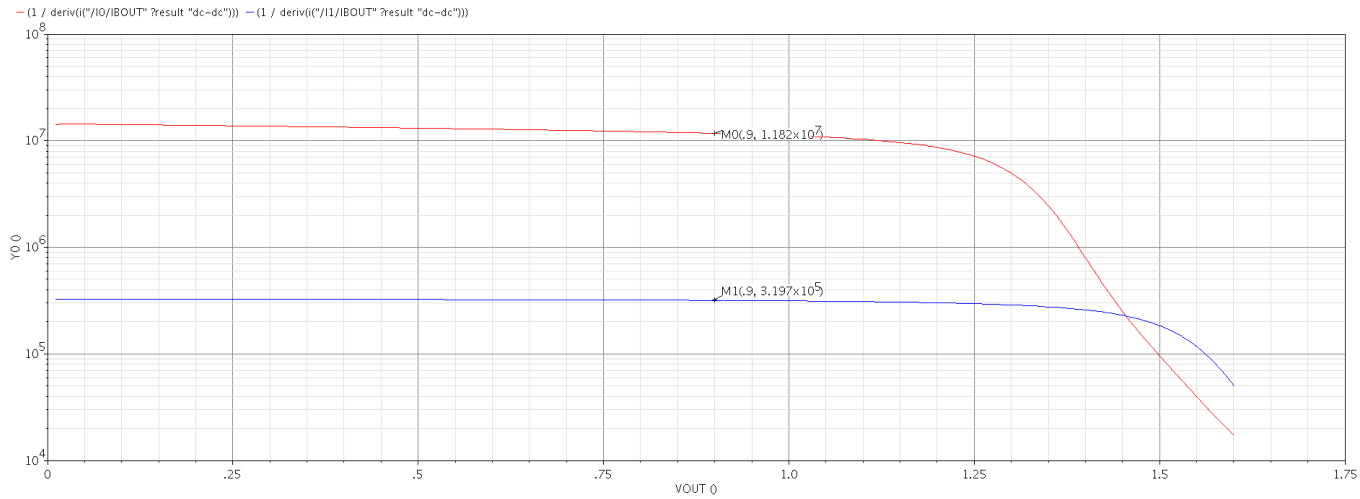
Percent of error in IBOUT vs VOUT (ideal IBOUT should be IBIN*2) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – V_*) overlaid in the same plot.



Comment on the difference between the two circuits.

The wide-swing current mirror has better efficiency than the simple current mirror so the error in the wide-swing is less than the simple current mirror and also the simple current mirror has lower Rout.

Rout vs VOUT (take the inverse of the derivative of IBOUT plot) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – V_*) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.



The red curve is the wide-swing CM and the blue is the simple CM

Comment on the difference between the two circuits.

From the graph, Rout of the wide-swing CM is much higher than that of the simple CM

Rout_simple is in the order of r0

Rout_WS is in the order of gm(ro)^2

These results above are calculated exactly in the analytical solution so I used it here

Does Rout change with VOUT? Why?

yes, because Vout is the Vds of the output mosfet so as vout changes vds changes so the transistor either go deeper into saturation or towards the edge of saturation which will change the value of ro.

Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

$$R_{out_{simple}} = R_{LFD_{M5}} = r_{05}(1 + g_m R_{s5})$$
$$R_{s5} = 0$$
$$\boldsymbol{R_{out_{simple}} = r_{05} = \frac{1}{g_{ds5}} = 319.488k\Omega}$$

//Rout_simple is in the order of r0

$$R_{out_{WS}} = R_{LFD_{M5}} = r_{05}(1 + g_m R_{s5})$$

$$R_{s5} = R_{LFD_{M1}} = r_{01}$$

$$\boldsymbol{R_{out_{WS}} = R_{LFD_{M5}} = r_{05}(1 + g_{m5} r_{01}) = r_{05} * r_{01} * g_{m5} = 8.7833M\Omega}$$

//Rout_WS is in the order of gm(ro)^2

	Analytically	Simulated
Wide-swing	$8.7833M\Omega$	11.82 $M\Omega$
Simple	$319.488k\Omega$	$319.7k\Omega$