Analog IC Design

Lab 11 (Mini Project 02)

Fully-Differential Folded Cascode OTA

PART 2: OTA Design

The specs:

Technology: 180 nm

Supply voltage: 1.8 V

Closed loop gain: 2

Phase margin >= 70 degrees

OTA current <= 80 uA

CMFB circuit current <= 40 uA

CM input range – low <=0

CM input range – high >= 1.1 V

Differential output swing: 1.2Vpk-to-pk

Load: 1pF

DC Loop gain: 60 dB

Closed loop bandwidth: 10MHz

You can use the following ideal sources in your testbench:

- **A single 20uA DC current source**
- **A DC voltage source for VDD**
- **Two DC voltage sources for biasing the cascode transistors (VCASCP and VCASCN)**
- **A DC voltage source for the CM output level (VREF)**

Sizing:

I started my flow by writing the equation of the gain to see what mosfets are contributing to the gain spec in order to achieve it.

Here I found that the gain spec has the following parameters affecting it:

(gm of input pair – gm of NMOS cascode – gm of PMOS cascode – ro of the 4 cascode branch and ro of the input pair)

So as a smart guess first I increased the gm/Id of the input pair and set a spec in ADT on gm/gds to achieve my gain spec.

Also, I then checked the BW equation and saw what Rout affect it and then tuned in that direction that will give me the BW spec needed.

I had a condition of the LG which was B*Aol = 60 dB = 1000

And from the lecture the dr explained that the $LG = B_G * A_{olR} = B_v * A_{vol} = 1000$

And beta will be a capacitive divider which will be equal to approx. 1/3

So, the open loop gain must be more than 3000

As beta will actually be less than this value as it should consider the OTA internal caps.

The approx. gain expression will be $LG = B * A_{vol} = \frac{(g_m r_o)^2}{4} * \frac{1}{3} = 1000$

So, I have a spec to meet for the input pair for gm/gds with about 110

I will use this value in ADT to size the input pair.

After doing my sizing and checking the gain and BW and PM specs I did some fine tuning to the currents to flow the exact needed current in each branch.

And here are the final values after the sizing is done.

PMOS input pair:

L=300 nm	W=21 um	gm/Id = 18

Cascode PMOS:

L=900 nm	W=50 um	gm/Id = 16

Cascode NMOS:

L=900 nm	W=19 um	gm/Id = 18

Tail current source:

L=1.2 um W=41 um gm/Id = 10

PMOS current mirror:

L=1.2 um W=20 um gm/Id = 10

NMOS current mirror:

L=1.2 um W=5 um gm/Id = 10

PMOS cascode mirror:

L=1.2 um W=21 um gm/Id = 10

NMOS cascose sink mirror:

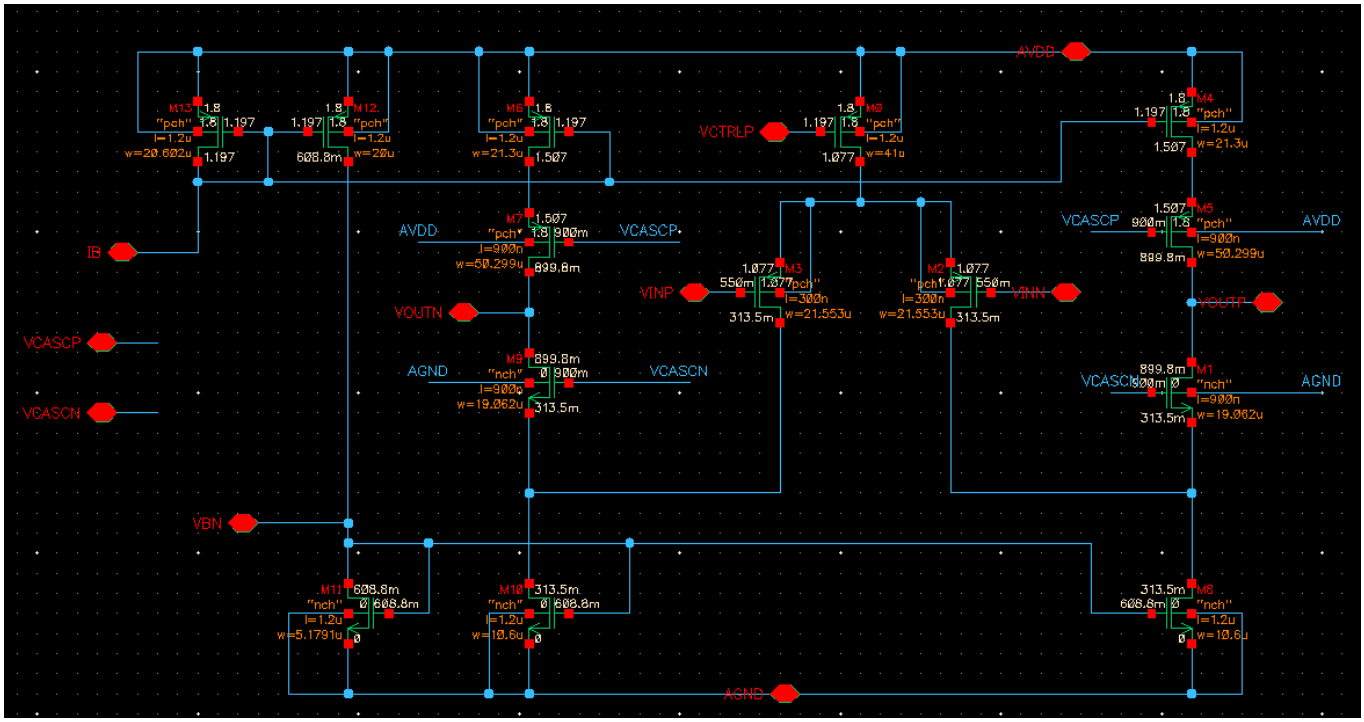
L=1.2 um W=10 um gm/Id = 10

VCASCN_min = Vgsn + V* =586 + 200 = 786 mV
I will set VCASCN = 900 mV

VCASCP_max = VDD – Vgsp – V* = 1800m – 607 – 200 = 993 mV

I will set VCASCP = 900 mV

The final sizing of my folded cascode OTA is in the figure below:

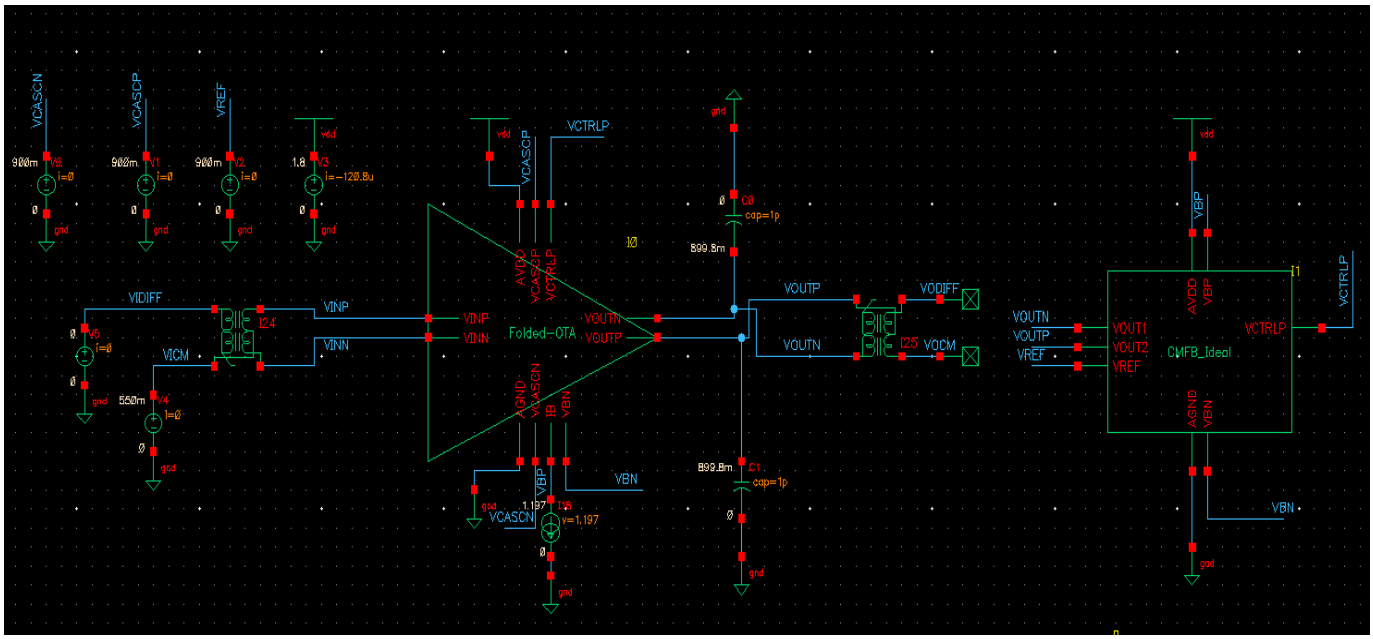


PART 3: Open Loop OTA Simulation (Behavioural CMFB)

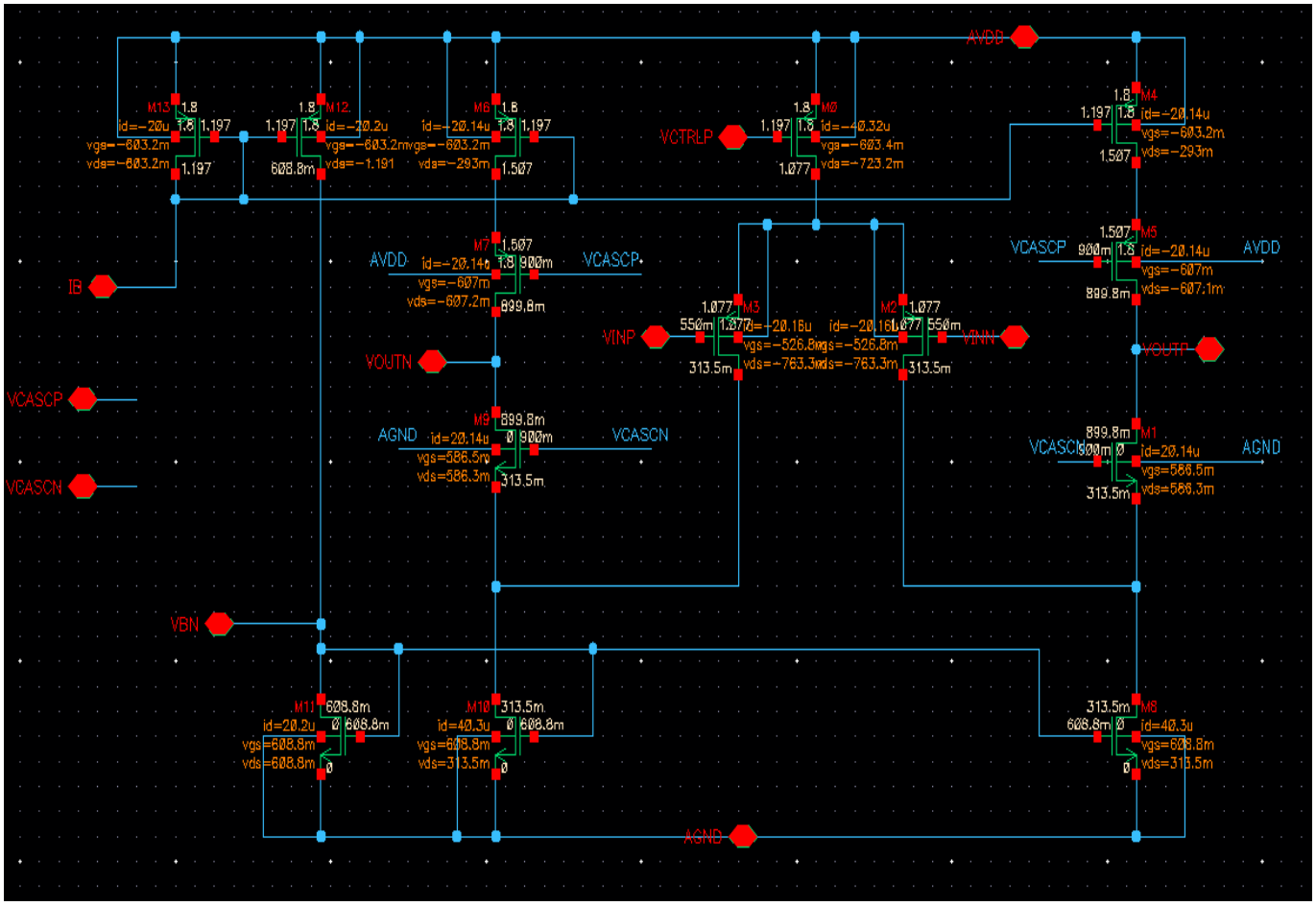
Report the following:

<u>1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.</u>

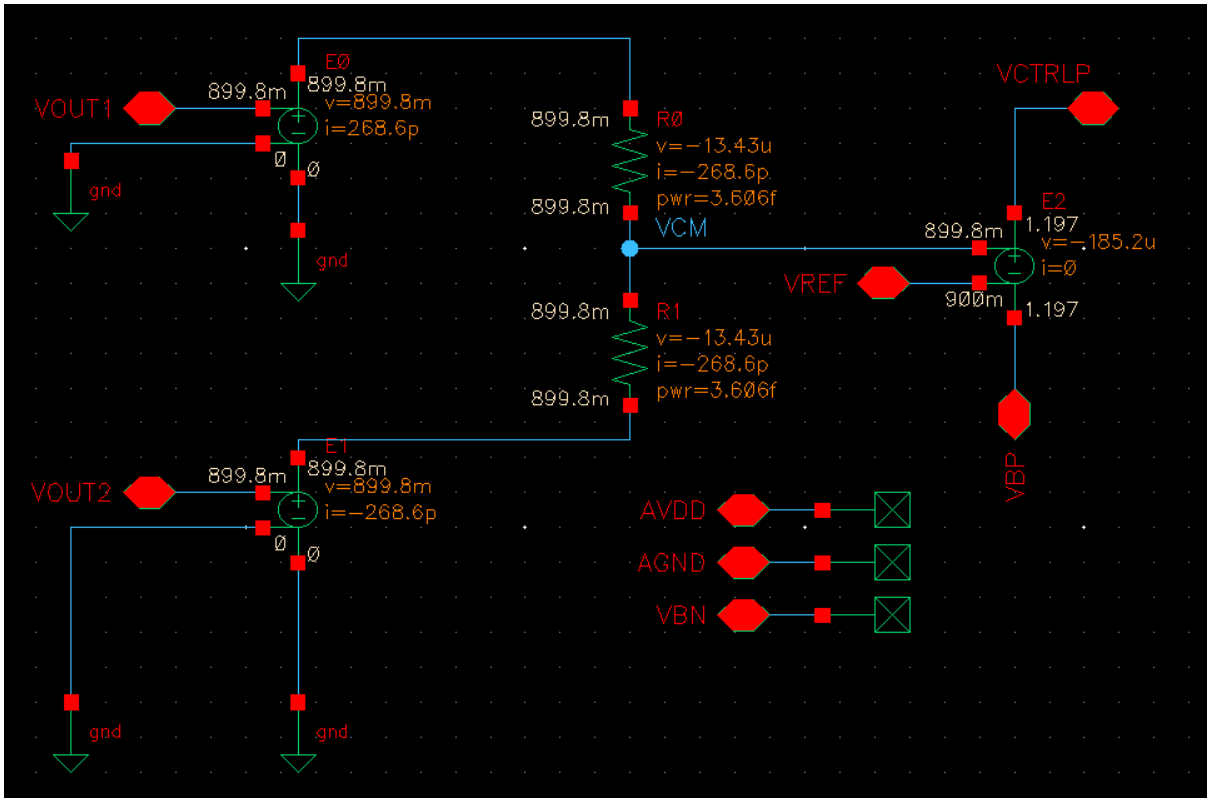
VICM=550 mV VREF=900 mV



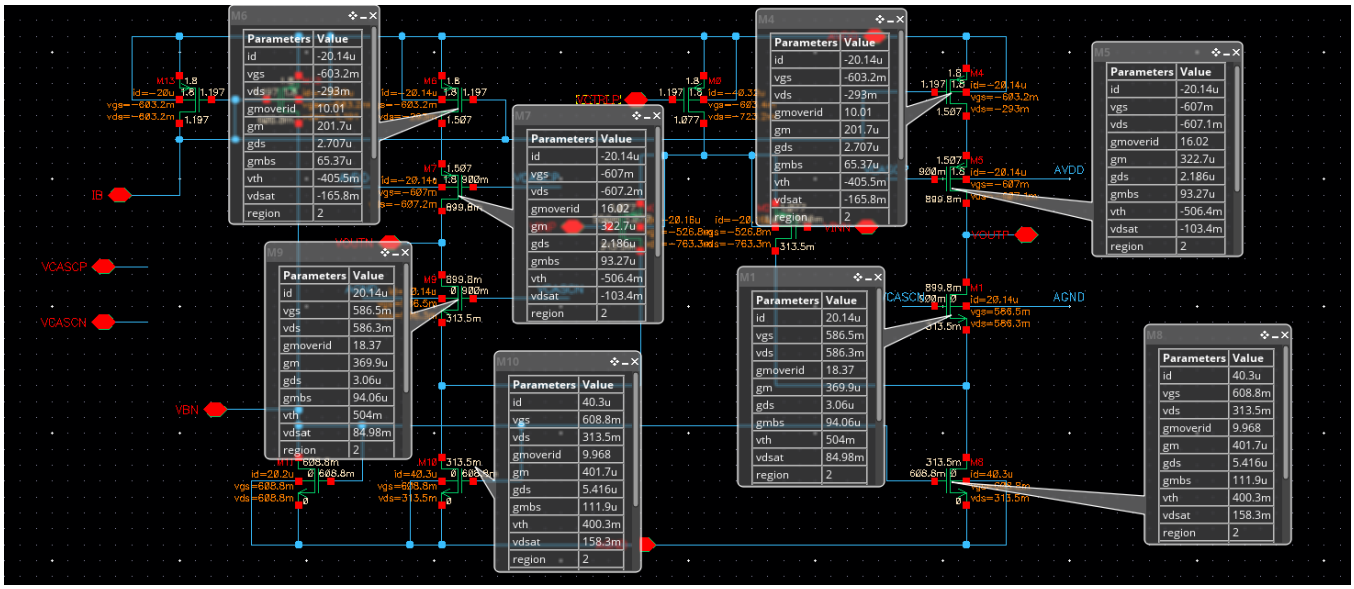
The figure below shows the dc currents of the folded cascode:

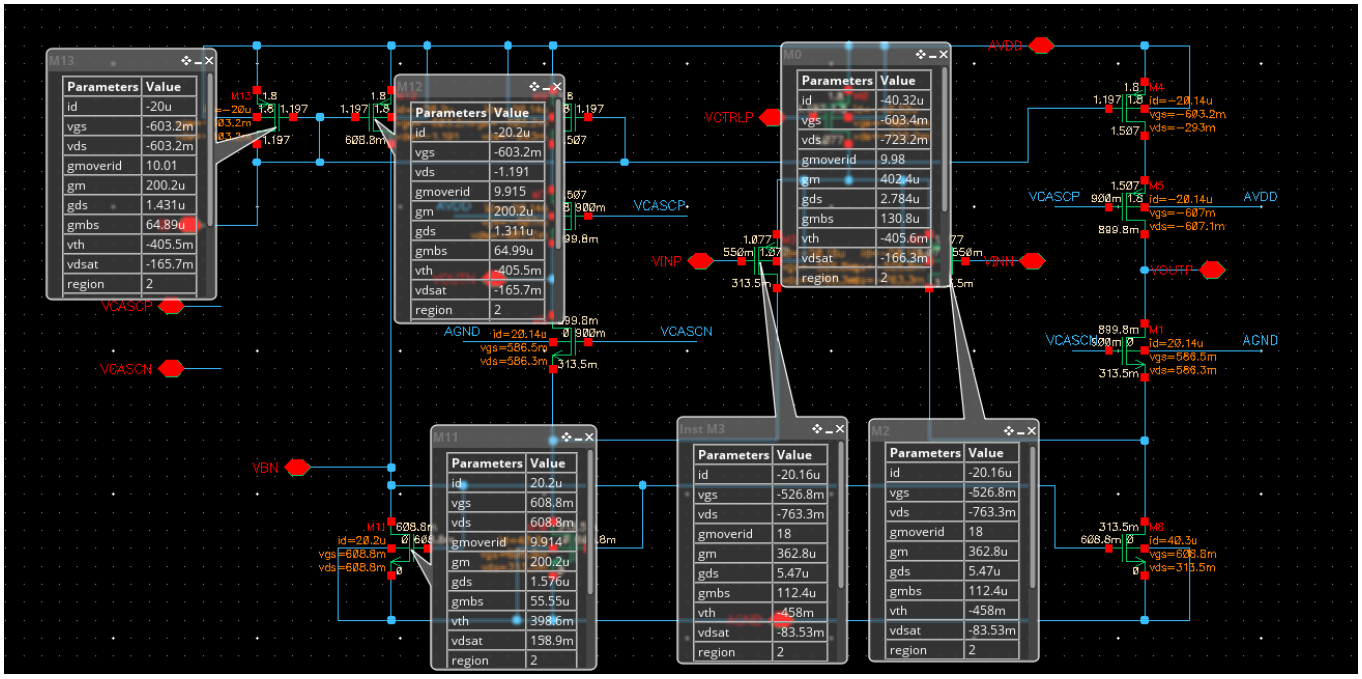


The figure below shows the ideal CMFB circuit behavioural model:



Transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.





What is the CM level at the OTA output?

VOCM = 899.8 mV

What are the differential input and output voltages of the error amplifier? What is the relation between them?

The differential input is = VREF – VCM = 0.9 – 899.8m = 0.2 mV almost = 0

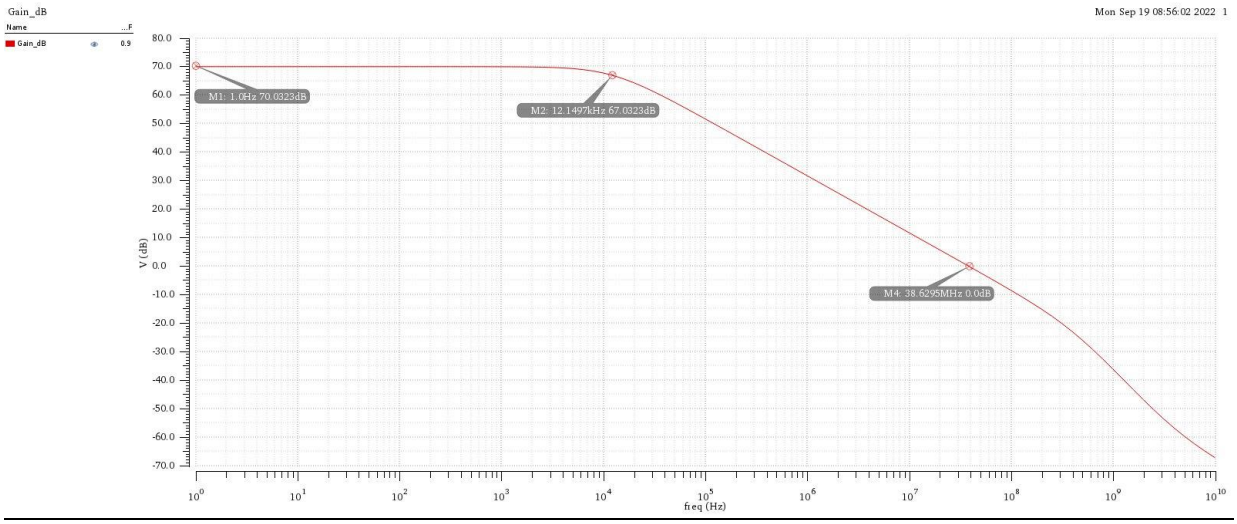
Differential output = VCTRLP – VBP = 1.197 – 1.197 =0

They are equal as we expect as we use unity gain buffer with ideal CMFB circuit.

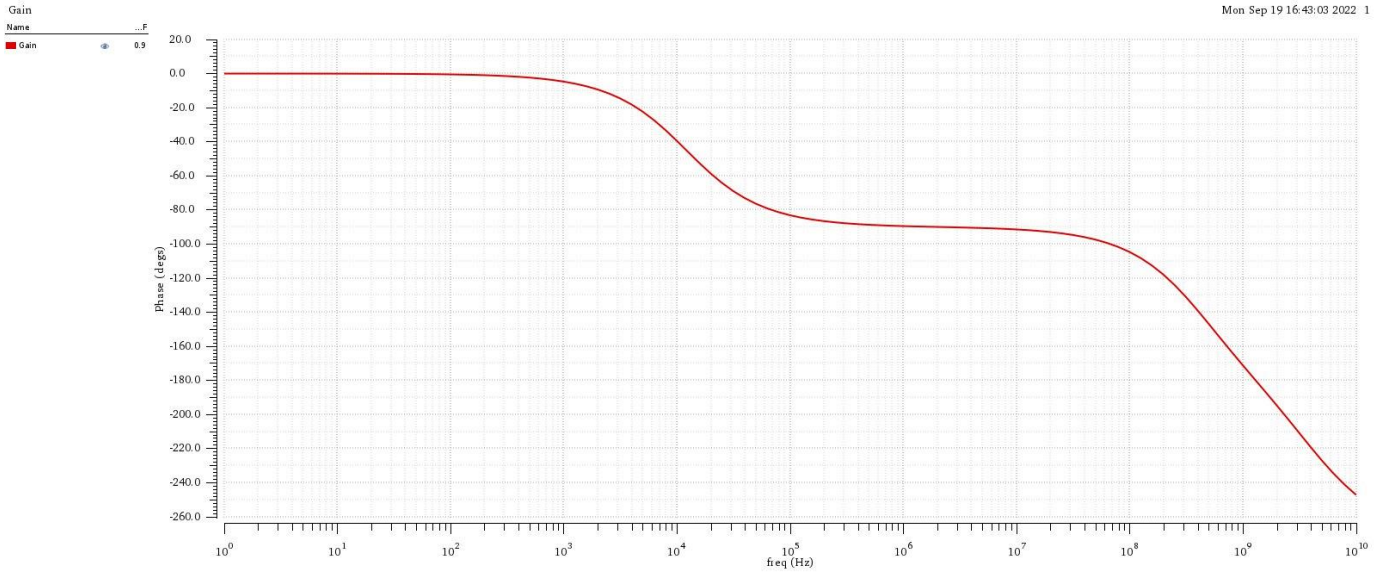
---

2) Diff small signal ccs:

Plot diff gain (magnitude in dB and phase) vs frequency.



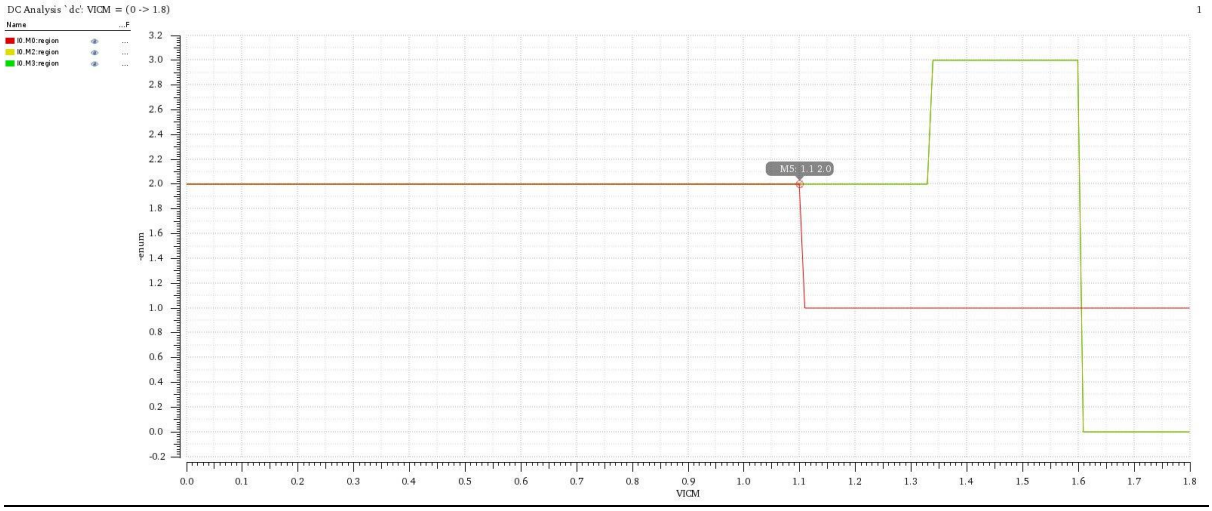
Phase:



Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:CMFB_TB:1	Gain				
Lab_11:CMFB_TB:1	Gain_dB				
Lab_11:CMFB_TB:1	Ao	3.174k			
Lab_11:CMFB_TB:1	Ao_dB	70.03			
Lab_11:CMFB_TB:1	BW	12.17k			
Lab_11:CMFB_TB:1	UGF	38.74M			
Lab_11:CMFB_TB:1	GBW	38.71M			
Lab_11:CMFB_TB:1	PM	84.35			

Checked the CMIR:



Check on the CMIR spec by hand analysis

$$\text{VICMmin} = \text{Vgs2} - \text{Vds2} - \text{Vds8} = -79\ \text{mV}$$

$$VICMmax = Vgs2 + Vov0 + Vdd = 1106.9\ mV = 1.1069\ V$$

CMIR spec is satisfied through hand analysis and regions.

Check on the output swing spec:

$$Vout_{max} = VDD - 2\,Vov = 1.5308\ V$$

$$V_{outmin} = 2\,Vov = 234\ mV$$

$$Vpeak - to - peak = 1.2968\ V$$

So, output swing spec is satisfied.

Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).

I will use the right branch in the numbering of mosfets and off course the left is identical as they are matched

$$\text{gain} = \left(\text{g}_{\text{m}_2}\right) * \text{R}_{\text{out}}$$

g_{m2} is not very accurate is it suffers from degeneration from the tail current source thats why the gain is a bit higher than what is simulated

$$R_{out} = \left(r_{o_1} * \left(g_{m_1} + g\_mb_1\right) * ((r_{o8})\backslash\backslash(r_{o2}))\right) \backslash\backslash \left(r_{o5} * \left(g_{m5} + g_{mb_5}\right) * (r_{o4})\right)$$

$$BW = \frac{1}{2 * pi * Rout * (C_L + C\_out)}$$

$$C_{out} = C_{dd_1} + C_{dd_5}$$

I0.M1:cdd I0.M5:cdd

	I0.M1:cdd	I0.M5:cdd
1	22.52E-15	69.41E-15

$$GBW = \frac{1}{2 * pi * (C_L + C_{out})}$$

$$w_{pnd} = \frac{w_t}{3} = \frac{g_{m1}}{6 * pi * C_{gg}} = 456.3\ M$$

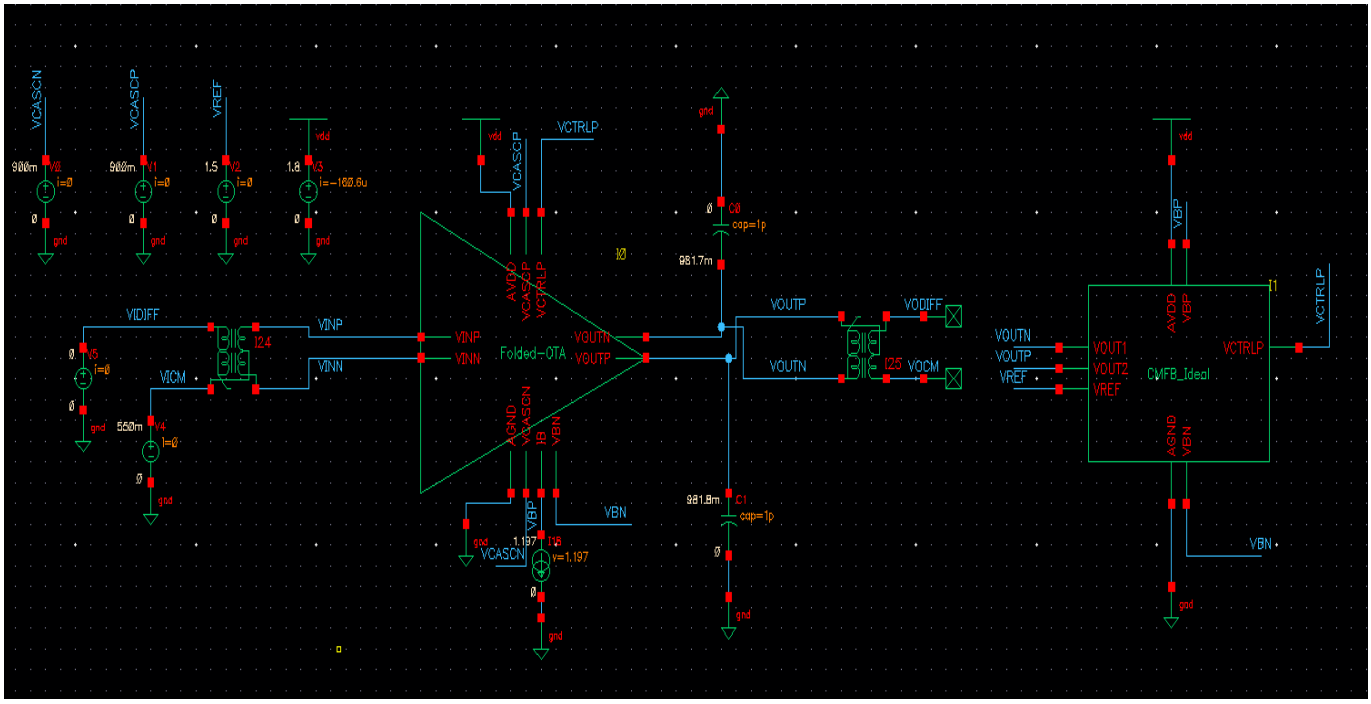
$$PM = 90 - \tan^{-1}\left(\frac{W_u}{w_{pnd}}\right)$$

	Simulation	Analytical
Gain	3.174 K = 70.03 dB	3.4 K = 70.62dB
BW	12.17 K	12.54 K
GBW	38.71 M	42 M
PM	84.35	85

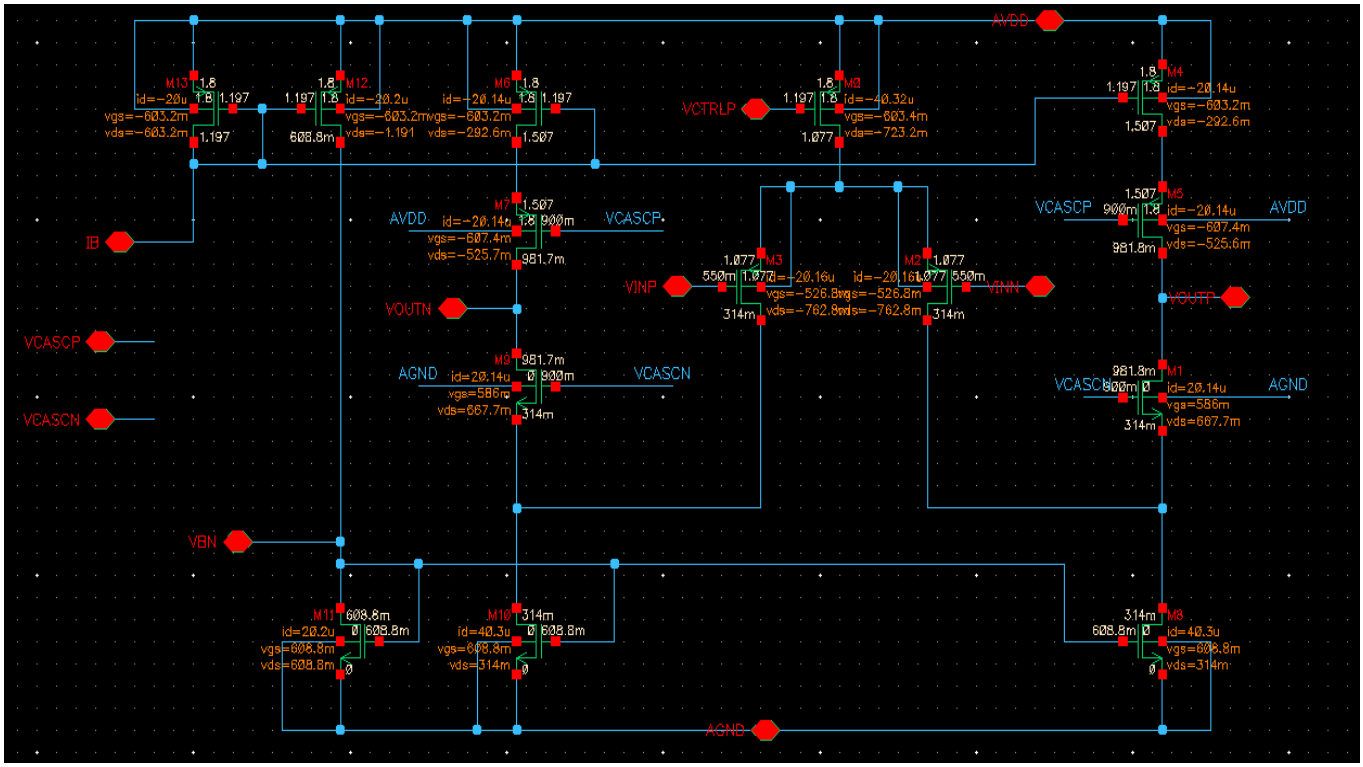
PART 4: Open-Loop OTA Simulation (Actual CMFB)

Report the following:

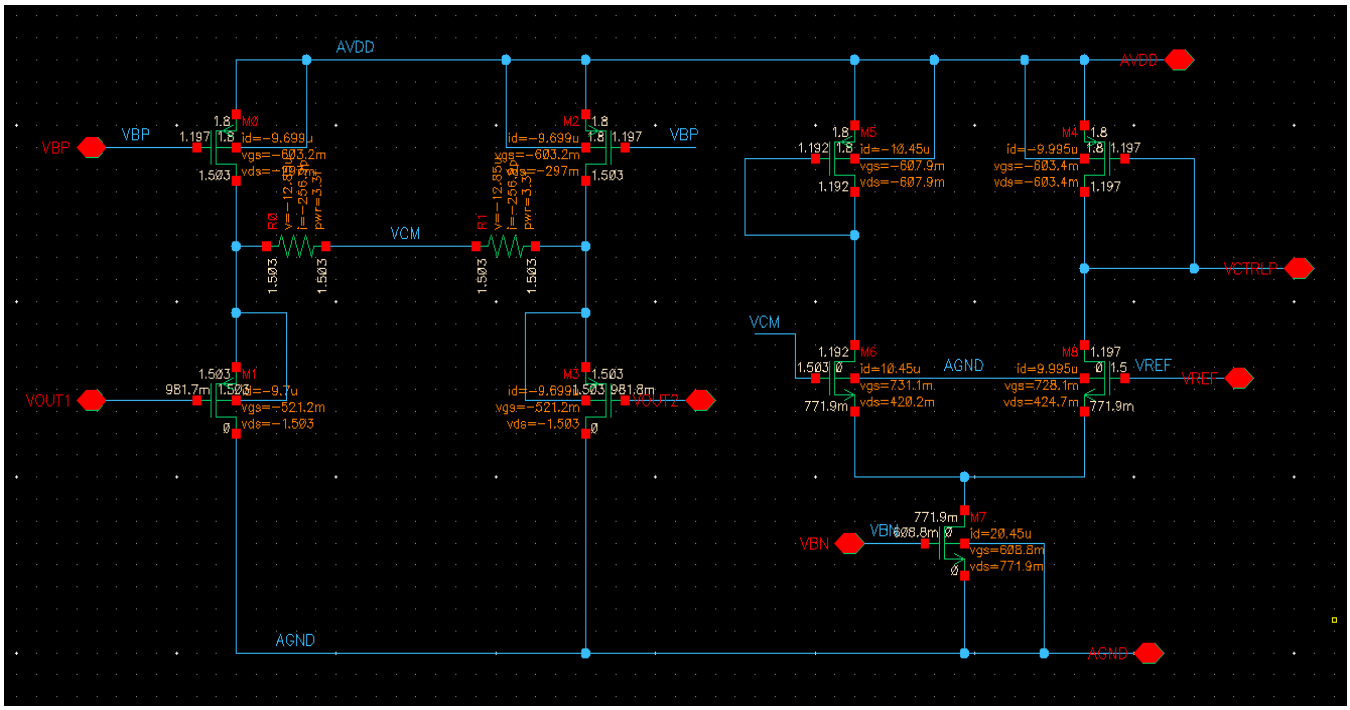
1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.



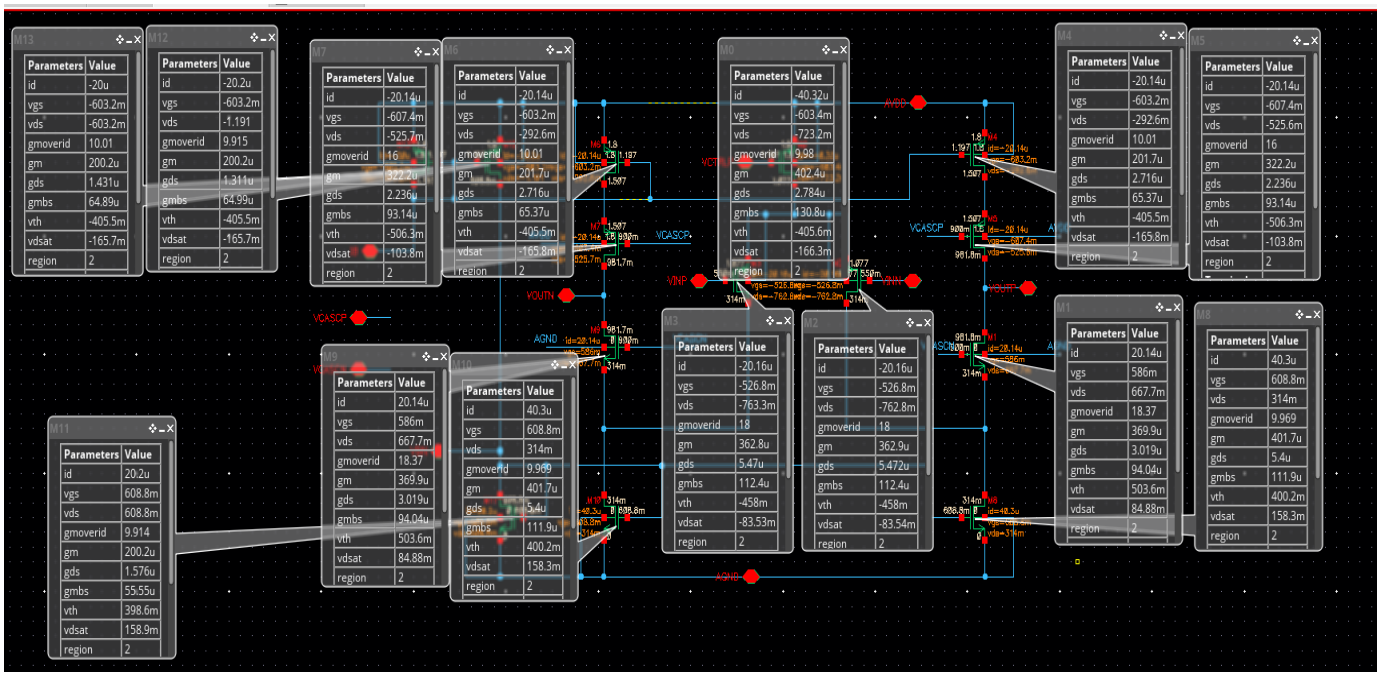
This is the operating point of folded cascode:



The operating point of the actual CMFB circuit.



Transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.



All operating point of the actual CMFB network:

Here I sized the transistors as the following.

Here I want to flow 10 uA of current in each branch so the current is known.

The two top right PMOS are the same as the PMOS current mirrors in the folded cascode design

I used the ADT sizing assistant where I set the current, L = length of PMOS current mirror

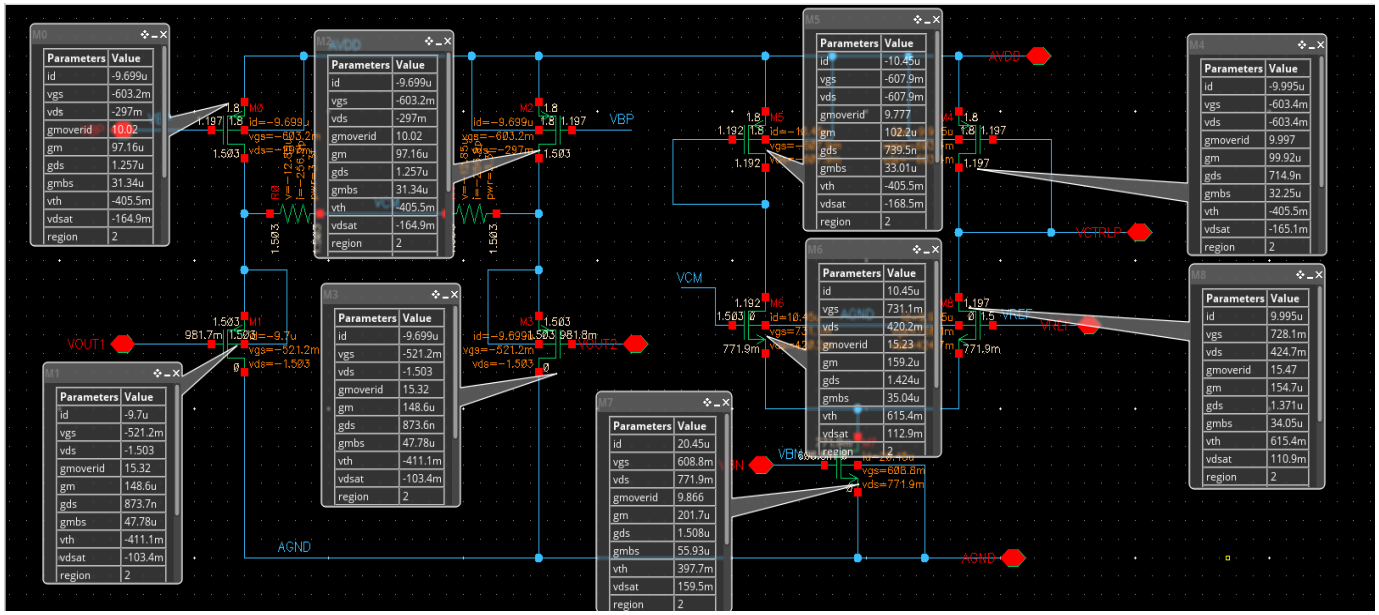
And vgs equal to the tail current source Vgs to cancel the systematic offset

The NMOS tail current sourceis sinking 20 uA of current and has the same L as the NMOS mirror in the folded cascode and same gm/Id =10 so I sized it as well.

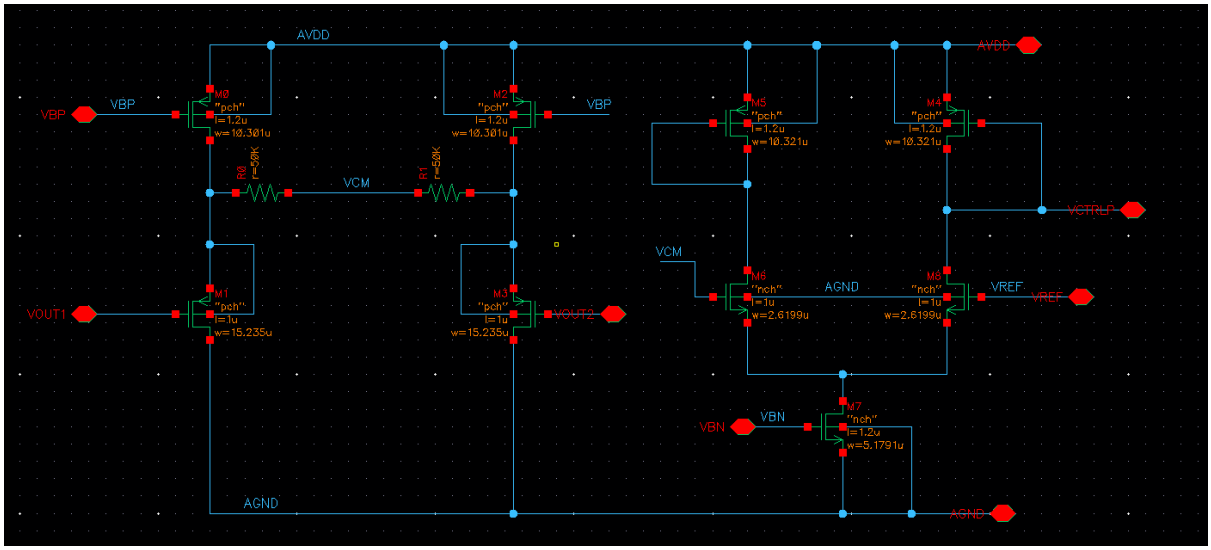
The two top left PMOS transistors are also the same as the mirror PMOS in the folded design so I used the same L, same gm/Id so it was also sized.

The rest of the mosfets are set to an initial guess of L= 1 um and gm/Id = 15

Which will be changed further in my design to tune a certain spec.



And this is the final sizing of the CMFB circuit after all the tuning



What is the CM level at the OTA output? Why?

VOCM = 981.7 mV

I needed VOCM to be equal 0.9 V so I used VREF = 900 m + Vgsp = 1.5 V

This will compensate the dc shift of the actual CMFB circuit.

What are the differential input and output voltages of the error amplifier? What is the relation between them?

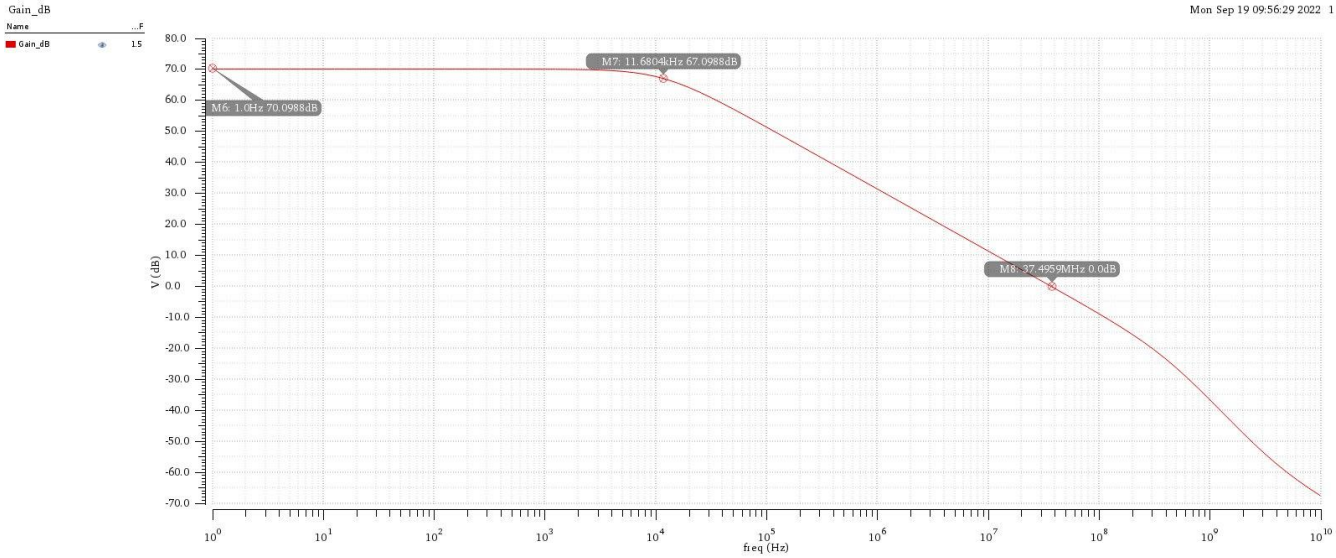
Differential input = VCM – VREF = 1.503 – 1.5 = 3 mV

Differential output = VCTRLP – VBP = 1192.1 mV - 1196.8 mV = 4 mV

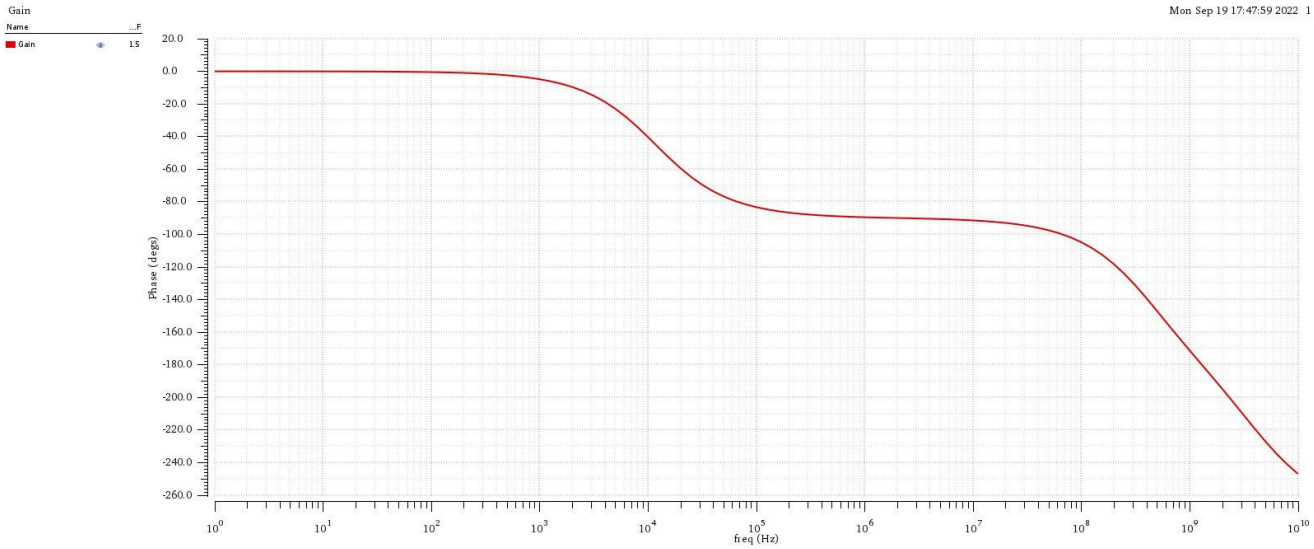
Relation between them is the 5-OTA gain (the gain of the error amplifier)

2) Diff small signal ccs:

Plot diff gain (magnitude in dB and phase) vs frequency.



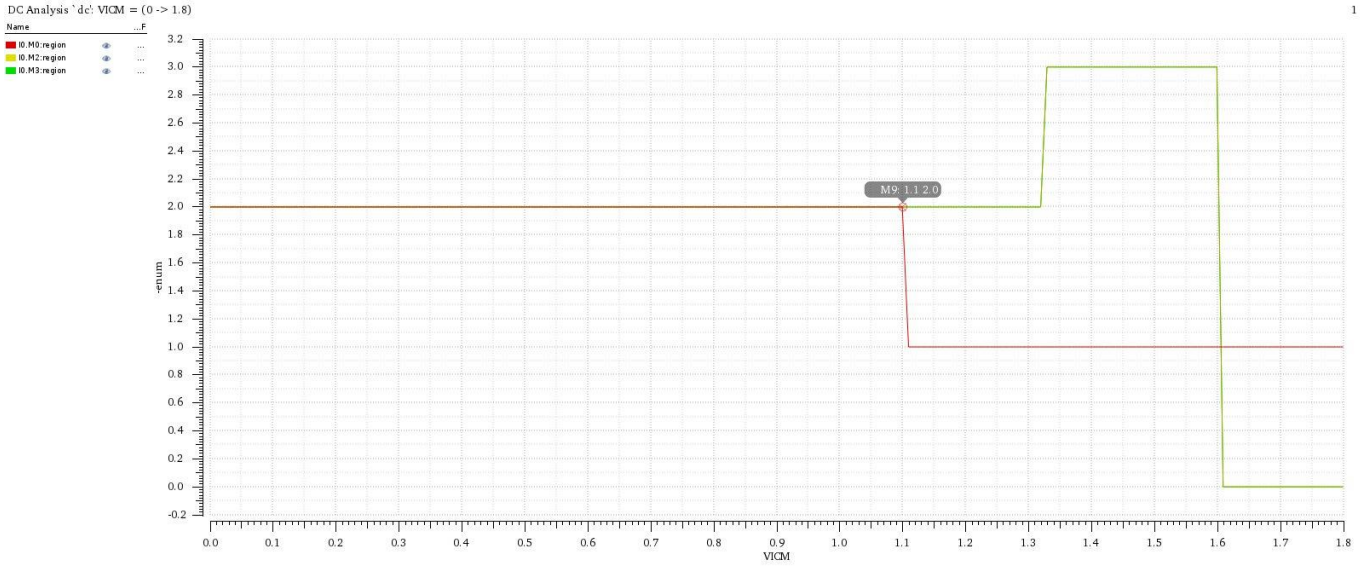
Phase:



Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:CMFB_TB:1	Gain				
Lab_11:CMFB_TB:1	Gain_dB				
Lab_11:CMFB_TB:1	Ao	3.198k			
Lab_11:CMFB_TB:1	Ao_dB	70.1			
Lab_11:CMFB_TB:1	BW	11.71k			
Lab_11:CMFB_TB:1	UGF	37.69M			
Lab_11:CMFB_TB:1	GBW	37.55M			
Lab_11:CMFB_TB:1	PM	84.45			

CMIR check:

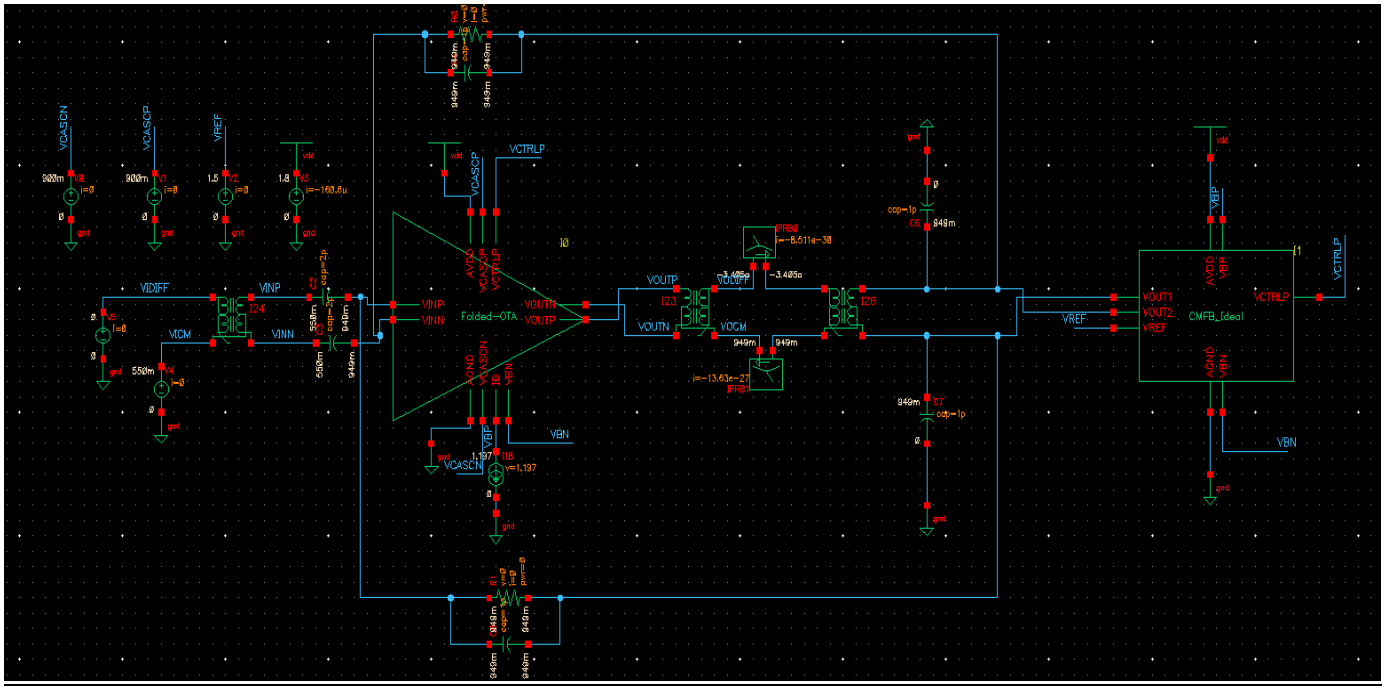


CMIR spec satisfied.

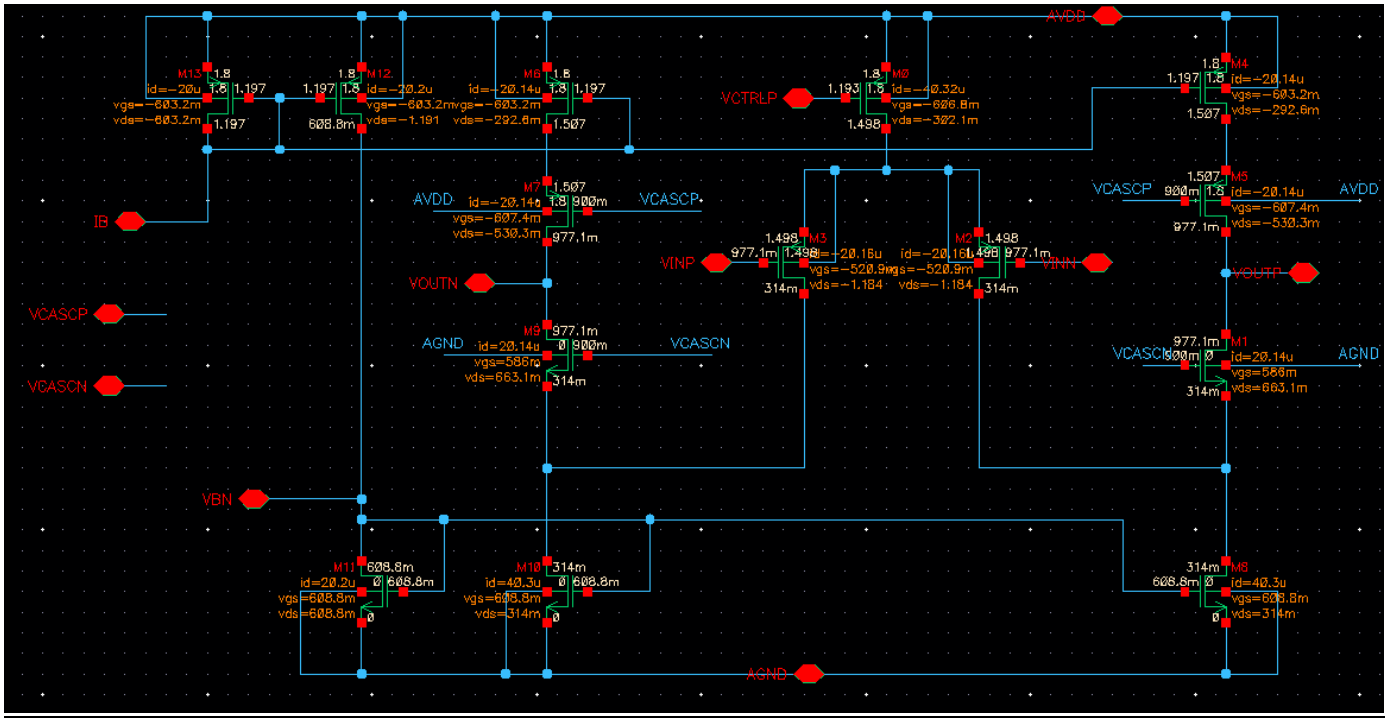
PART 5: Closed Loop Simulation (AC and STB Analysis)

Report the following:

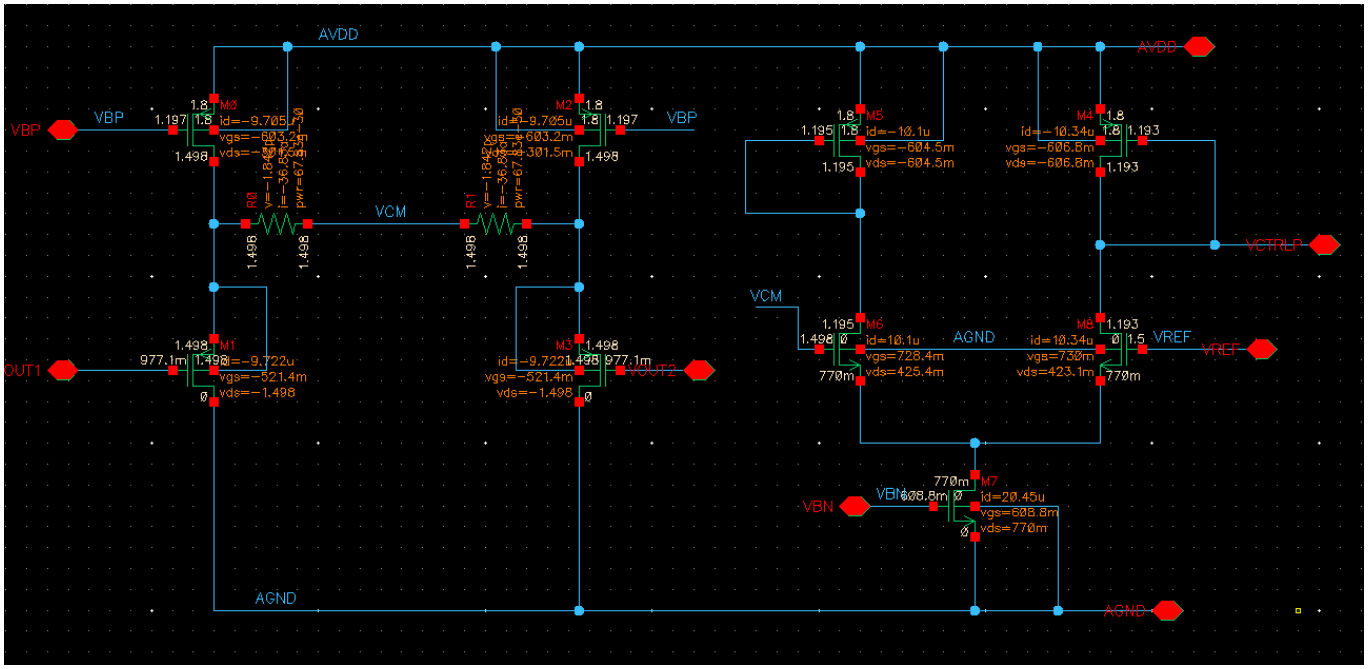
1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.



Folded cascode operating point:



Actual CMFB circuit operating point:



What is the CM level at the OTA output? Why?

VOCM = 949 mV

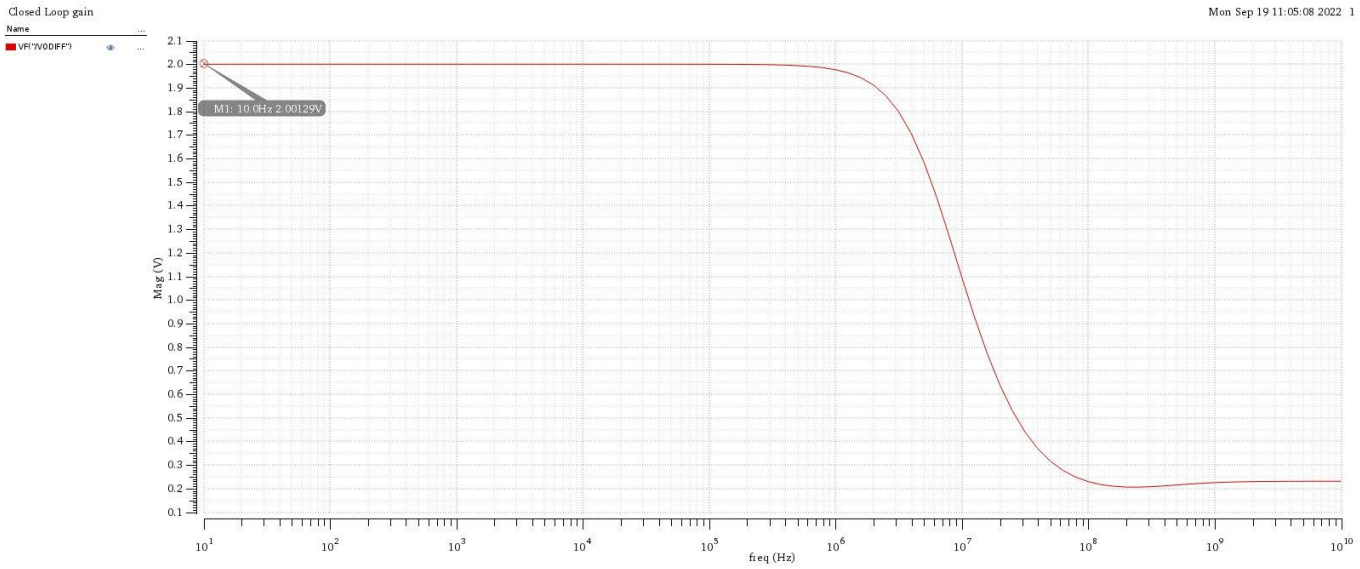
This is what I designed the circuit too keep cm level at about 0.9 V and I did it by setting VREF=1.5 V

What is the CM level at the OTA input? Why?

VICM = 949 mV = VOCM as the connection is a buffer connection so VOCM =VICM

2) Differential closed-loop response:

Plot VODIFF vs frequency



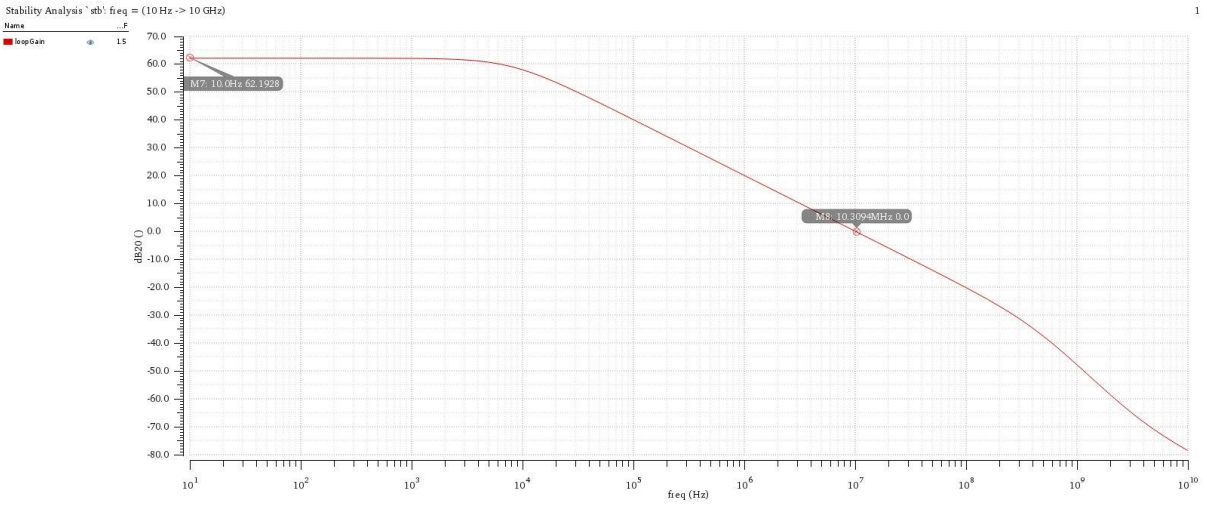
Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:Closed_Loop:1	VF("/VODIFF")				
Lab_11:Closed_Loop:1	BW_cl	10.23M			
Lab_11:Closed_Loop:1	GBW_cl	20.53M			

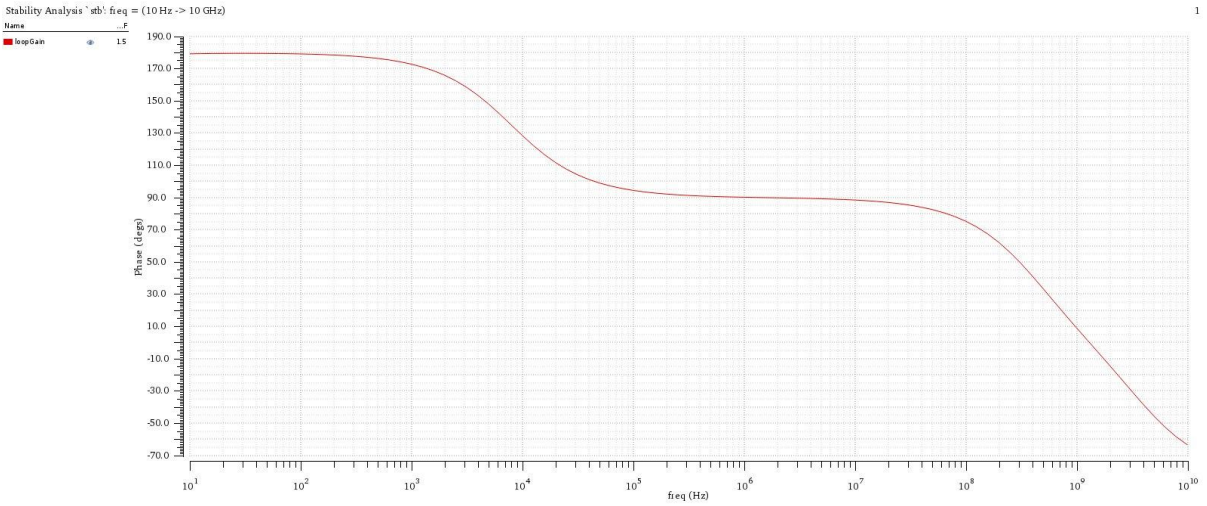
Note that the closed loop gain spec is satisfied and also the closed loop bandwidth spec is satisfied.

3) Differential and CMFB loops stability (STB analysis):

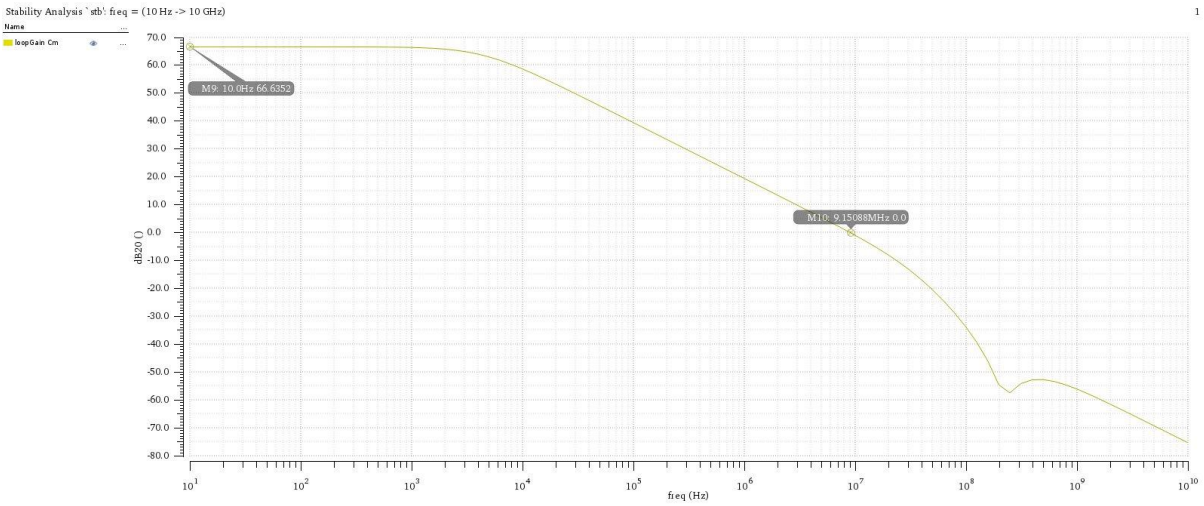
Differential LG in dB:



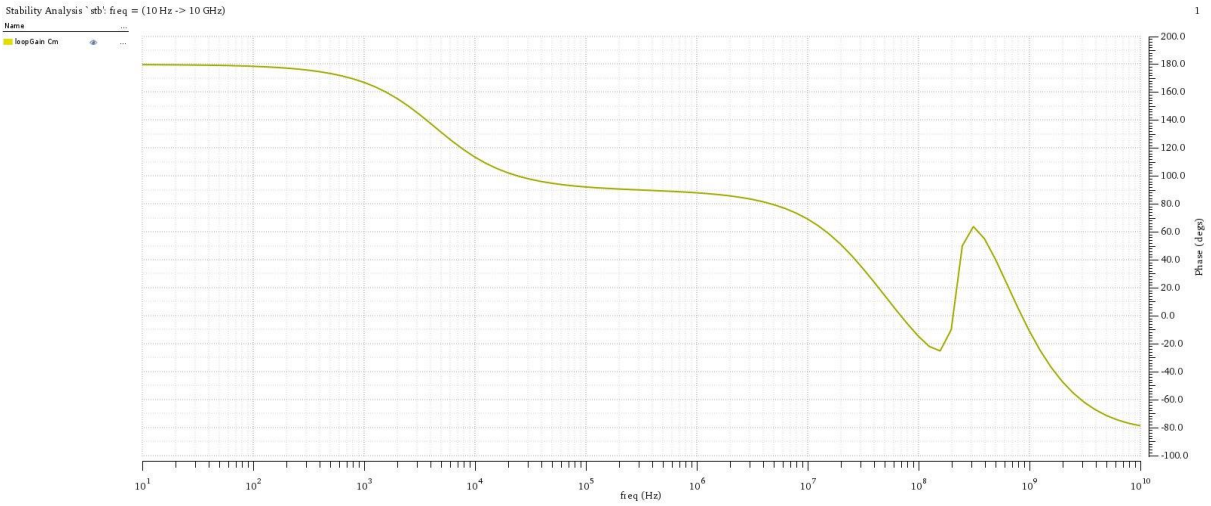
Differential LG phase:



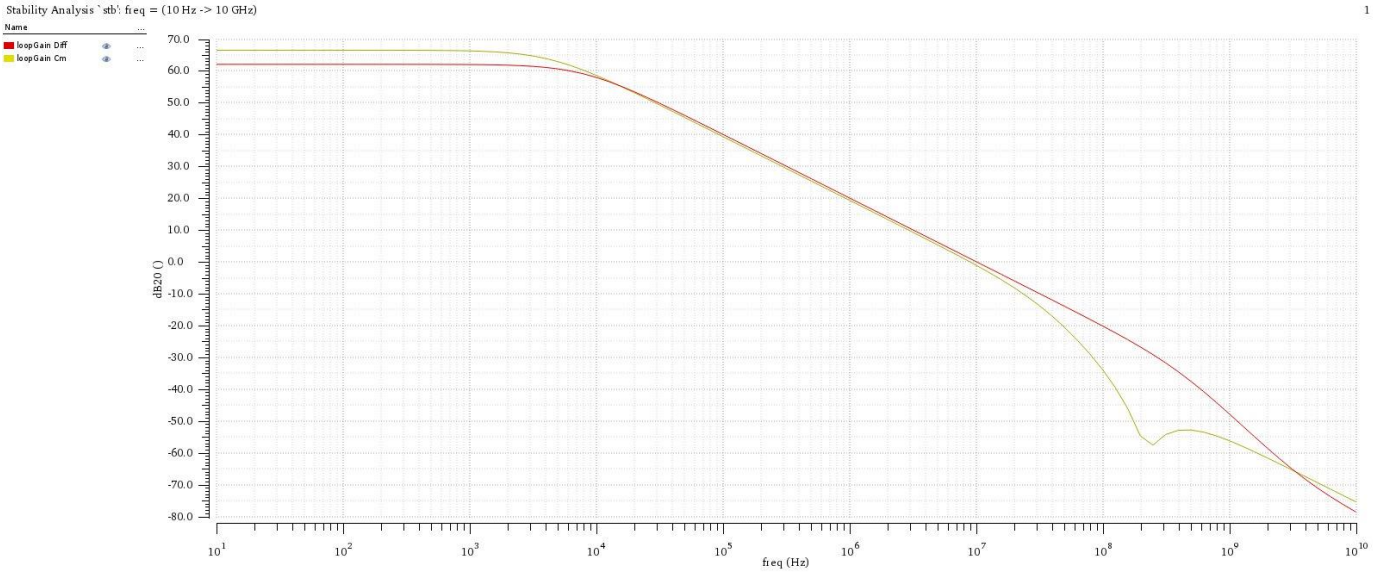
CM LG in dB:

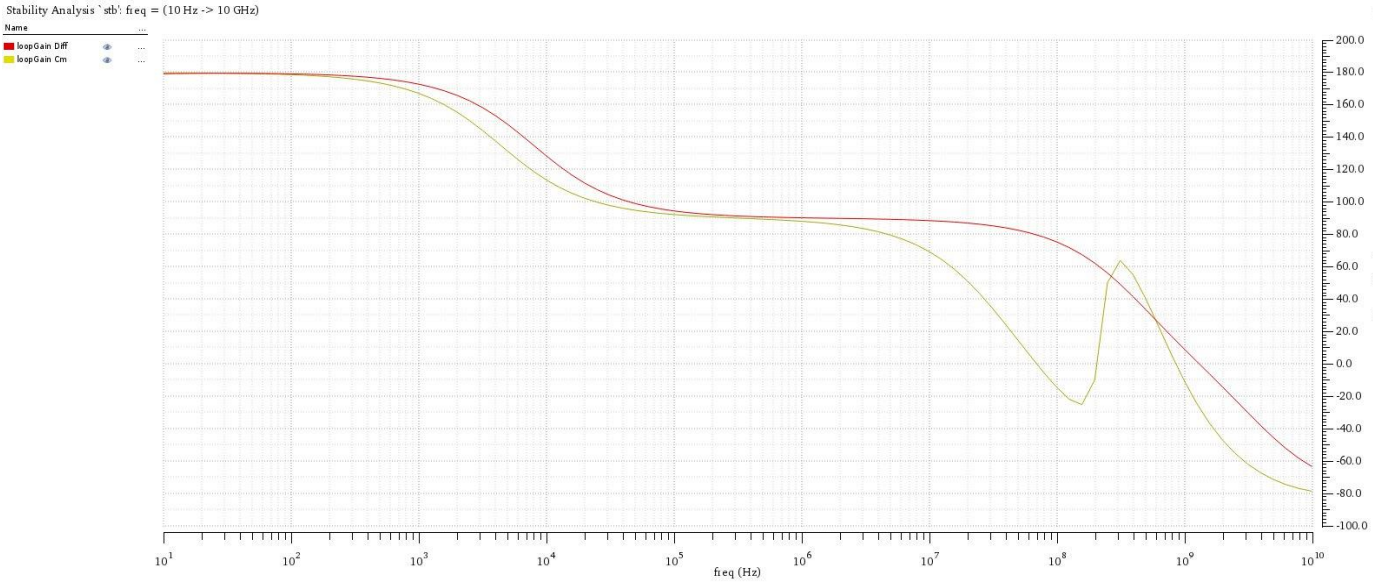


CM LG phase:



Plot loop gain in dB and phase vs frequency for the two simulations overlaid.





<u>Compare GBW and PM of diff and CM loops. Comment.</u>

Differential:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:Closed_Loop:1	phase_margin_Diff	88.53			
Lab_11:Closed_Loop:1	GBW_diff	10.28M			

Common mode:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:Closed_Loop:1	phase_margin_CM	71.31			
Lab_11:Closed_Loop:1	GBW_cm	9.483M			

Note:

Here the phase margin of the CM loop was not satisfied so I tuned in the CMFB circuit.

I lowered the gm/Id of the NMOS of the input of the CMFB circuit (M6 & M8) from 15 down to 11 to meet the PM spec.

Phase margin spec is satisfied in both differential and CM.

GBW in the differential mode is higher than that of the CM.

The phase margin of the CM is 71 which is stable but not yet 76 so we might see a slight peeking in the transient run.

Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment

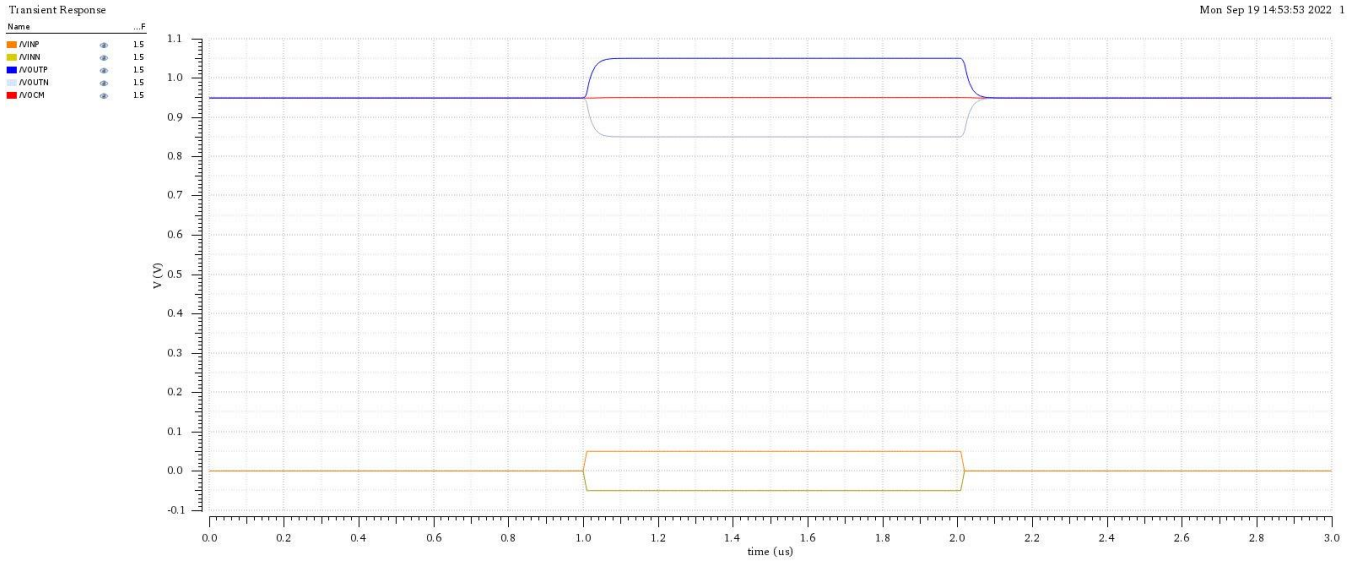
	Open loop	Closed loop
DC LG	60.55 dB	62.192 dB
GBW	12.51 M	10.28 M

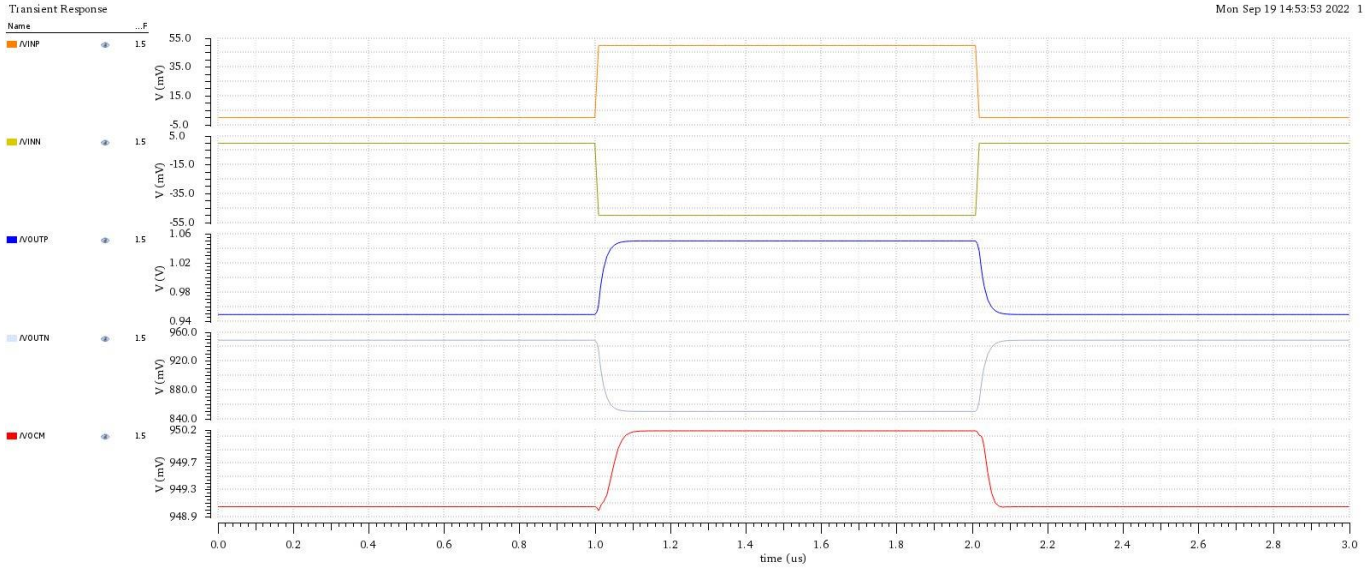
The results are not exactly the same as I calculated the values of the open loop LG and GBW by assuming that beta = 1/3 which is not so accurate as it should include the OTA parasitic capacitances.

PART 6: Closed Loop Simulation (Transient Analysis)

Report the following:

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

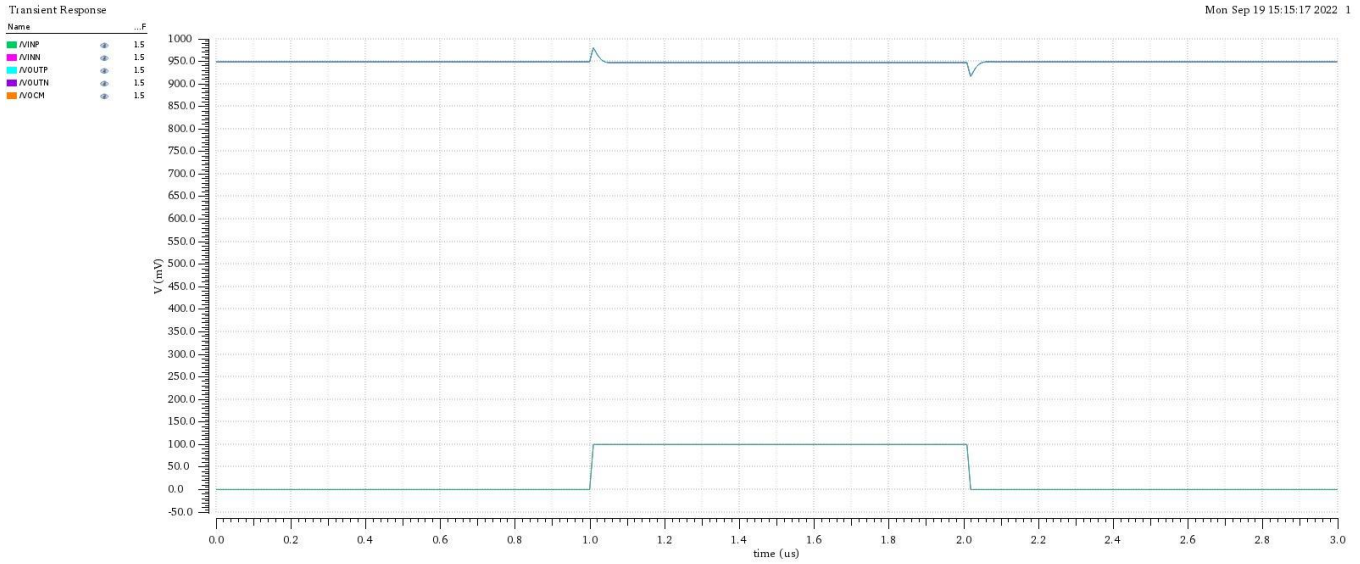


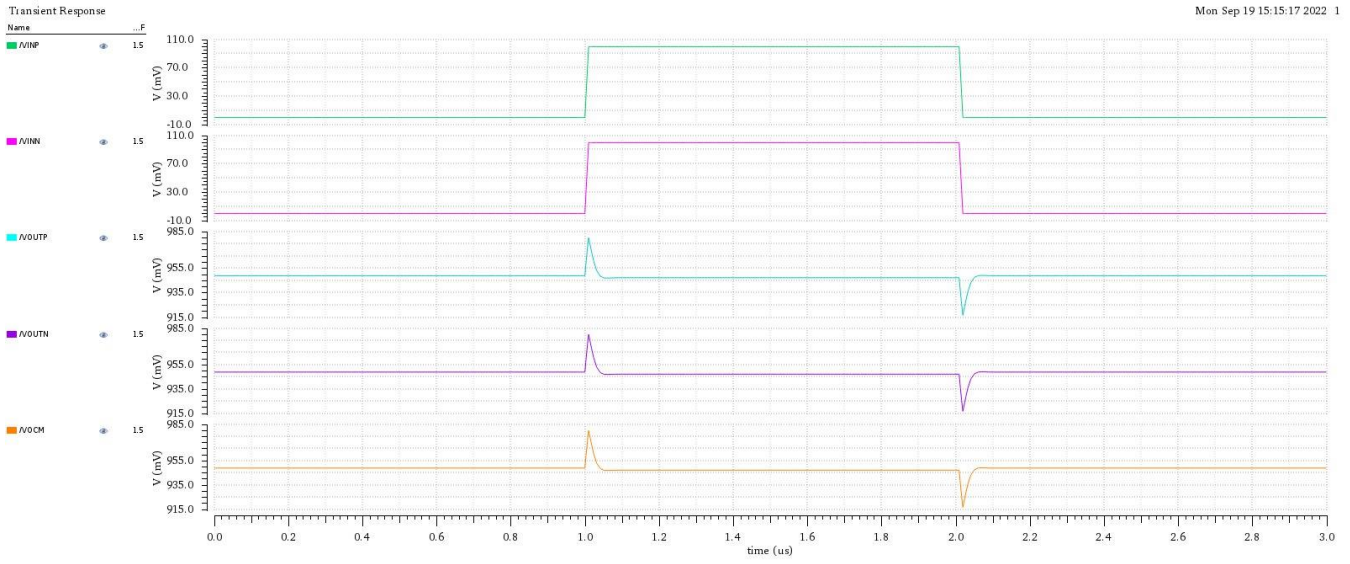


Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

Yes, there is some CM ringing as expected as the phase margin of the CM loop is 71 which is less than 76 but also, it's still stable.

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.





<u>Do you notice any differential/CM ringing? Are both loops stable with adequate PM?</u>

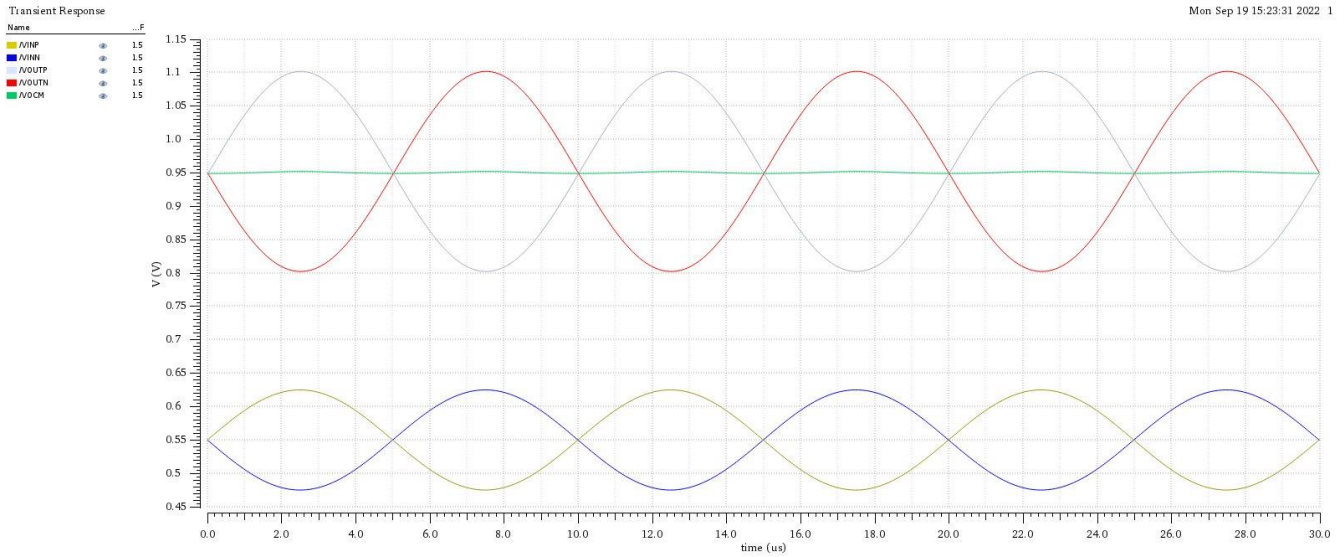
There is a differential overshot in VOUTP, VOUTN, VOCM.

Both loops are stable.

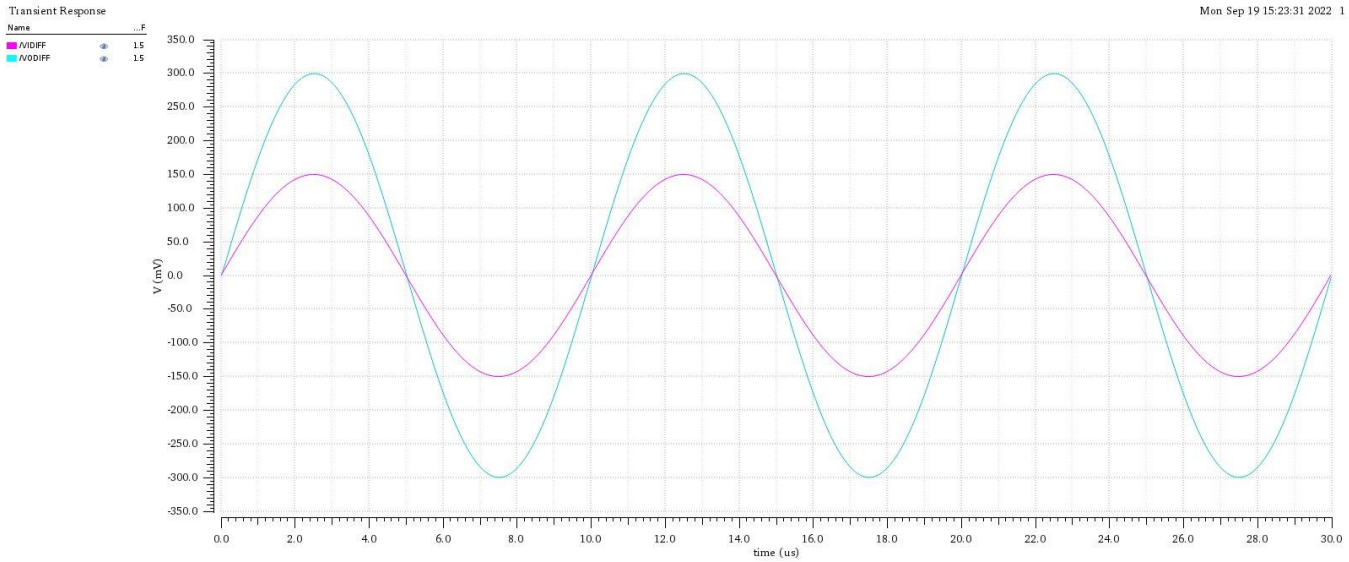
Phase margin of the differential loop is much bigger than that of the CM loop.

2) Output swing:

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.



Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:part_6:1	/VINP				
Lab_11:part_6:1	/VINN				
Lab_11:part_6:1	/VOUTP				
Lab_11:part_6:1	/VOUTN				
Lab_11:part_6:1	/VOCM				
Lab_11:part_6:1	/VIDIFF				
Lab_11:part_6:1	/VODIFF				
Lab_11:part_6:1	Vout_PTP	599.3m			
Lab_11:part_6:1	Vin_PTP	300m			
Lab_11:part_6:1	Av_cl	1.998			

$$A_{vcl} = \frac{V_{out_{peak-to-peak}}}{V_{in_{peak-to-peak}}} = 1.998$$

Almost equal to 2 so here is another check that the closed loop gain is satisfied.