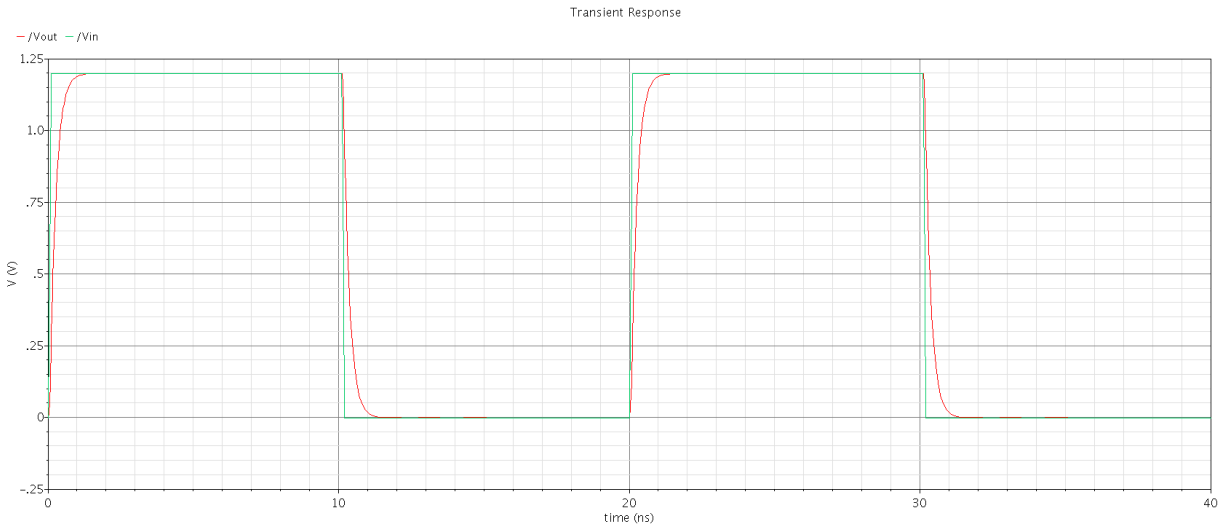
Lab 01

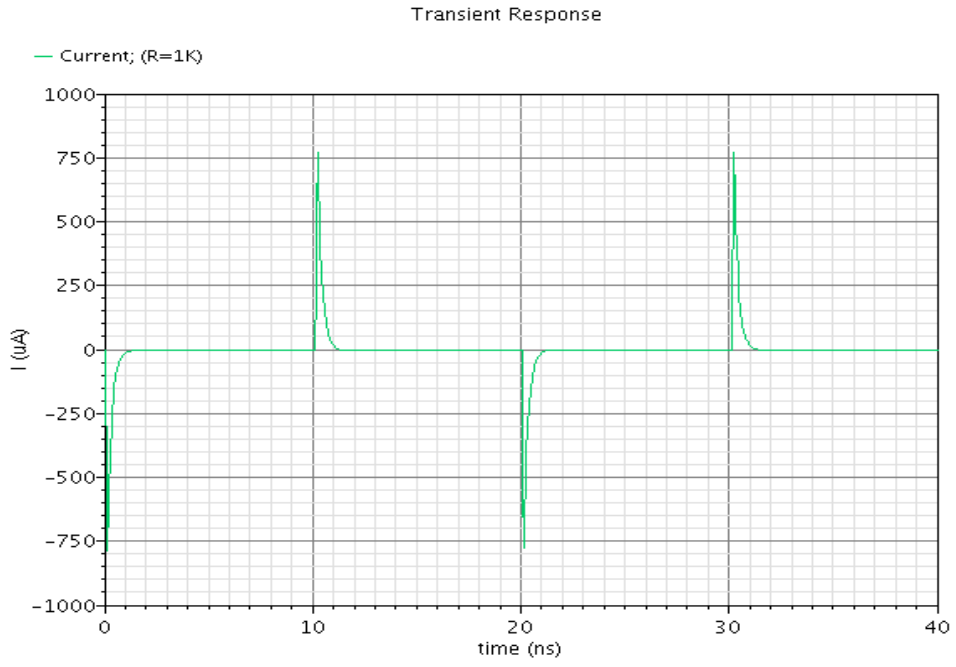
LPF Simulation and MOSFET Characteristics

PART 1: Low Pass Filter Simulation (LPF)

Transient Analysis:

Report transient analysis results for two periods (use max time step $=T_{clk}/100$).





Comment:

• When the input voltage is applied, the capacitor takes approximately 5τ to reach full charging or discharging.

The current is maximum at the input edges and reaches zero after the capacitor finishes charging or discharging.

Calculate rise and fall time (10% to 90%) using Cadence calculator expressions. Export the expressions to adexl.

Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:lpf:1	/vout				
AIC_Training:lpf:1	/vin				
AIC_Training:lpf:1	T_rise	446.7p			
AIC_Training:lpf:1	T_fall	446.7p			

Comment:

• The output takes 2.2 τ to reach from 10% to 90% of the input.

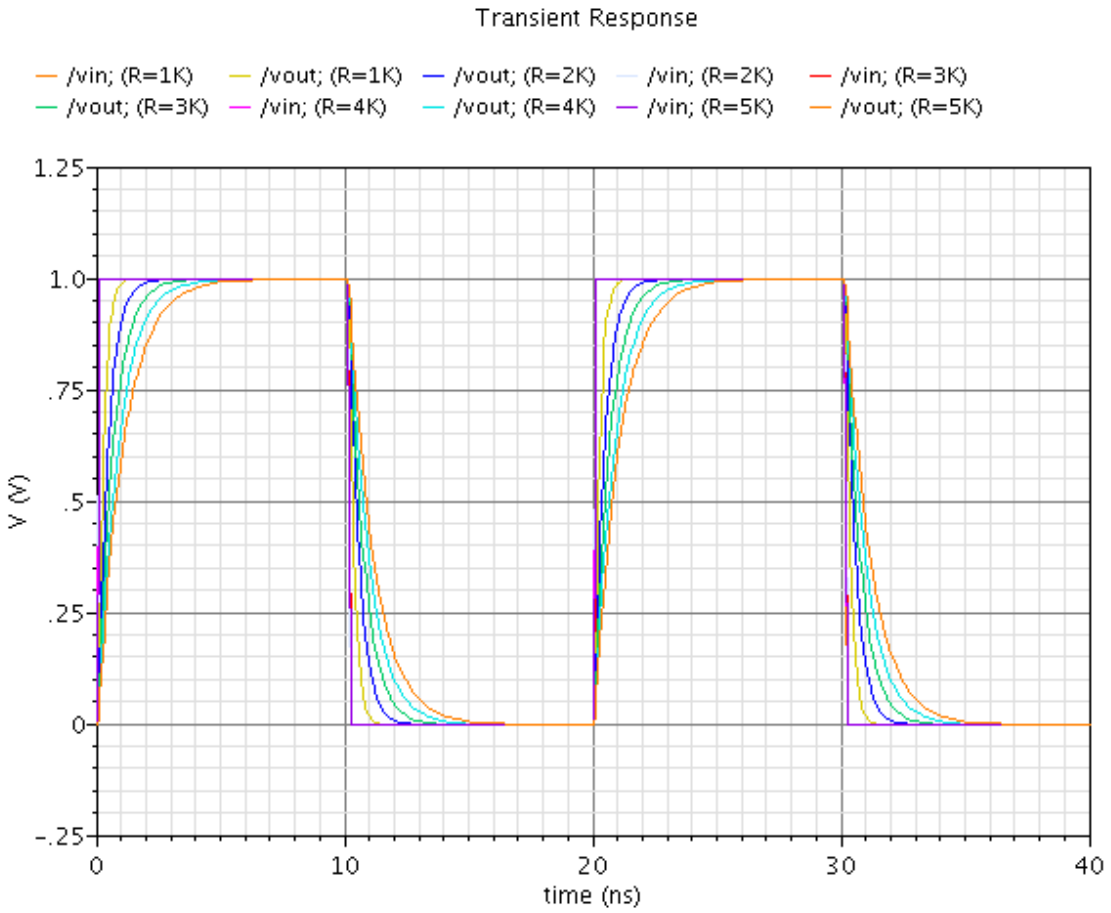
• The falling time is equal to the rising time.

Compare simulation with analytical results in a table.

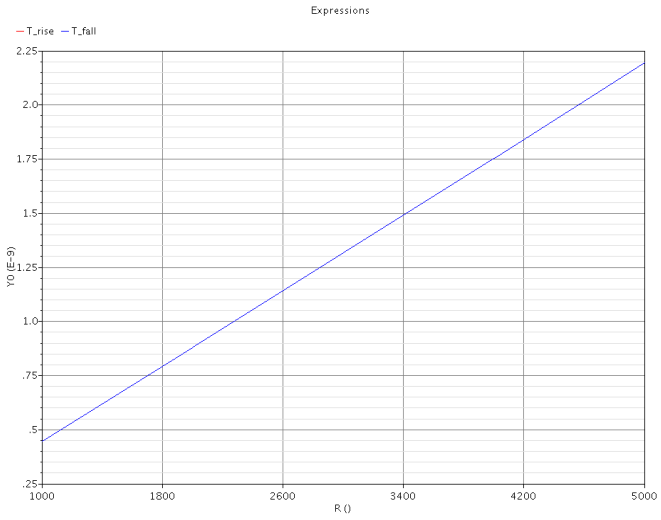
	Simulation	Analytic
T_rise	446.7p	**2.2*0.2n=440 p**
T_fall	446.7p	**2.2*0.2n=440 p**

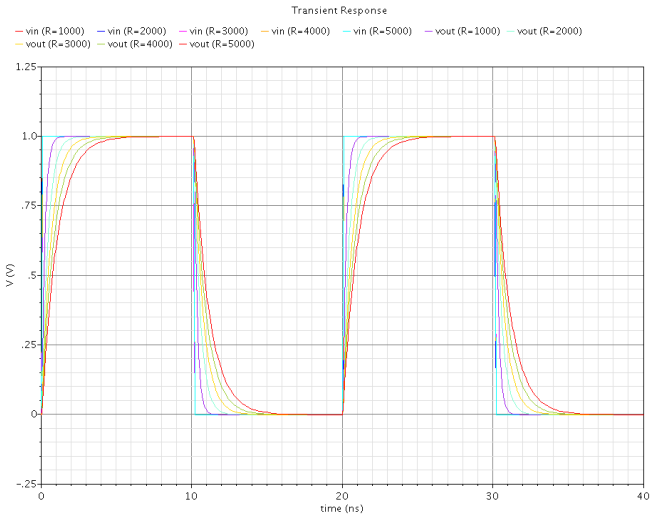
-The results are very close to the analytical solution.

Do parametric sweep for R=1:1:5$k\Omega$. Report overlaid results. Comment on the results.



This graph is sweeping the R and the T_rise and Fall graphs.





Rising time equals falling time = 2.2τ and $\tau = RC$, therefore as R increases τ also increases and both of rising and falling time will increase linearly with R.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: R=1k						
1	AIC_Training:lpf:1	/vout				
1	AIC_Training:lpf:1	/vin				
1	AIC_Training:lpf:1	T_rise	446.7p			
1	AIC_Training:lpf:1	T_fall	446.7p			
Parameters: R=2k						
2	AIC_Training:lpf:1	/vout				
2	AIC_Training:lpf:1	/vin				
2	AIC_Training:lpf:1	T_rise	881.2p			
2	AIC_Training:lpf:1	T_fall	881.2p			
Parameters: R=3k						
3	AIC_Training:lpf:1	/vout				
3	AIC_Training:lpf:1	/vin				
3	AIC_Training:lpf:1	T_rise	1.319n			
3	AIC_Training:lpf:1	T_fall	1.319n			
Parameters: R=4k						
4	AIC_Training:lpf:1	/vout				
4	AIC_Training:lpf:1	/vin				
4	AIC_Training:lpf:1	T_rise	1.755n			
4	AIC_Training:lpf:1	T_fall	1.755n			
Parameters: R=5k						
5	AIC_Training:lpf:1	/vout				
5	AIC_Training:lpf:1	/vin				
5	AIC_Training:lpf:1	T_rise	2.196n			
5	AIC_Training:lpf:1	T_fall	2.196n			

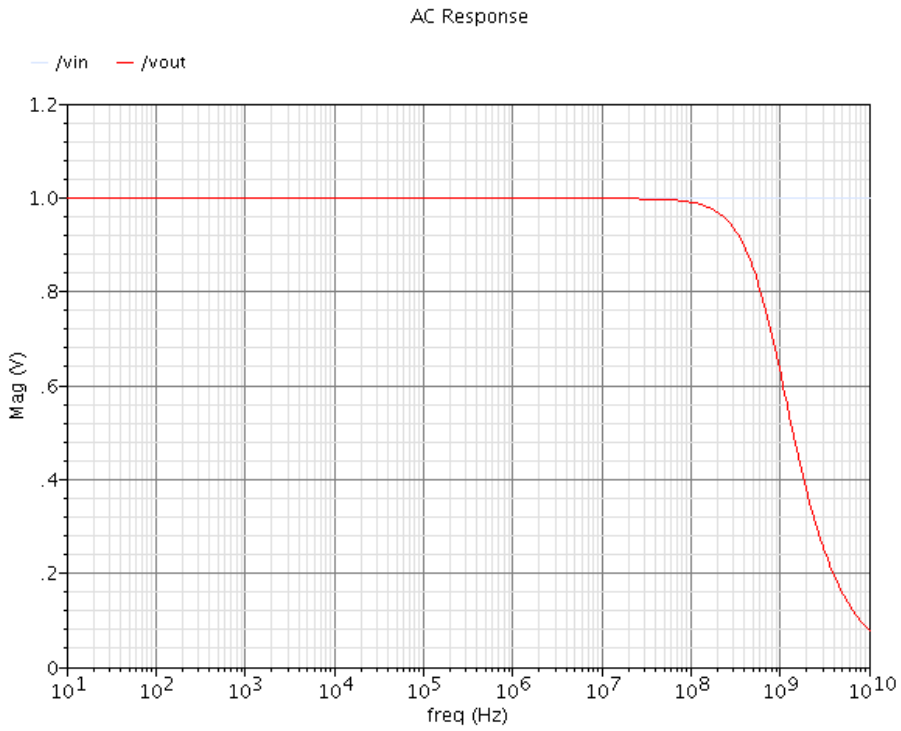
Comment:

As resistance increases the time constant τ increases, as $\tau = RC$ and the capacitor needs nearly 5τ to charge or discharge, therefore the charging and discharging time of the capacitor will increase as we increase the resistance.

AC Analysis

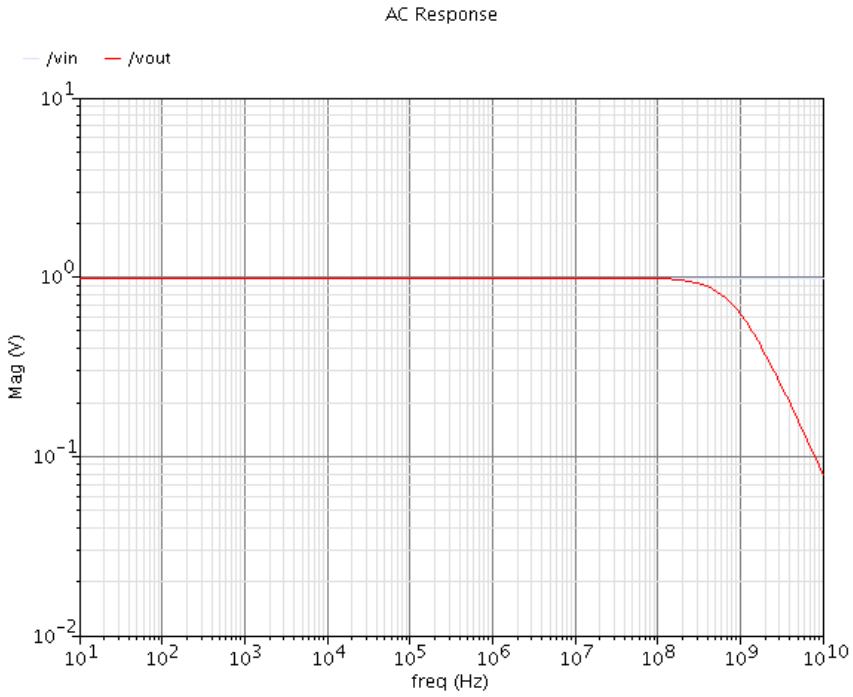
Report Bode Plot (magnitude and phase) for the previous LPF

Vin vs Vout:

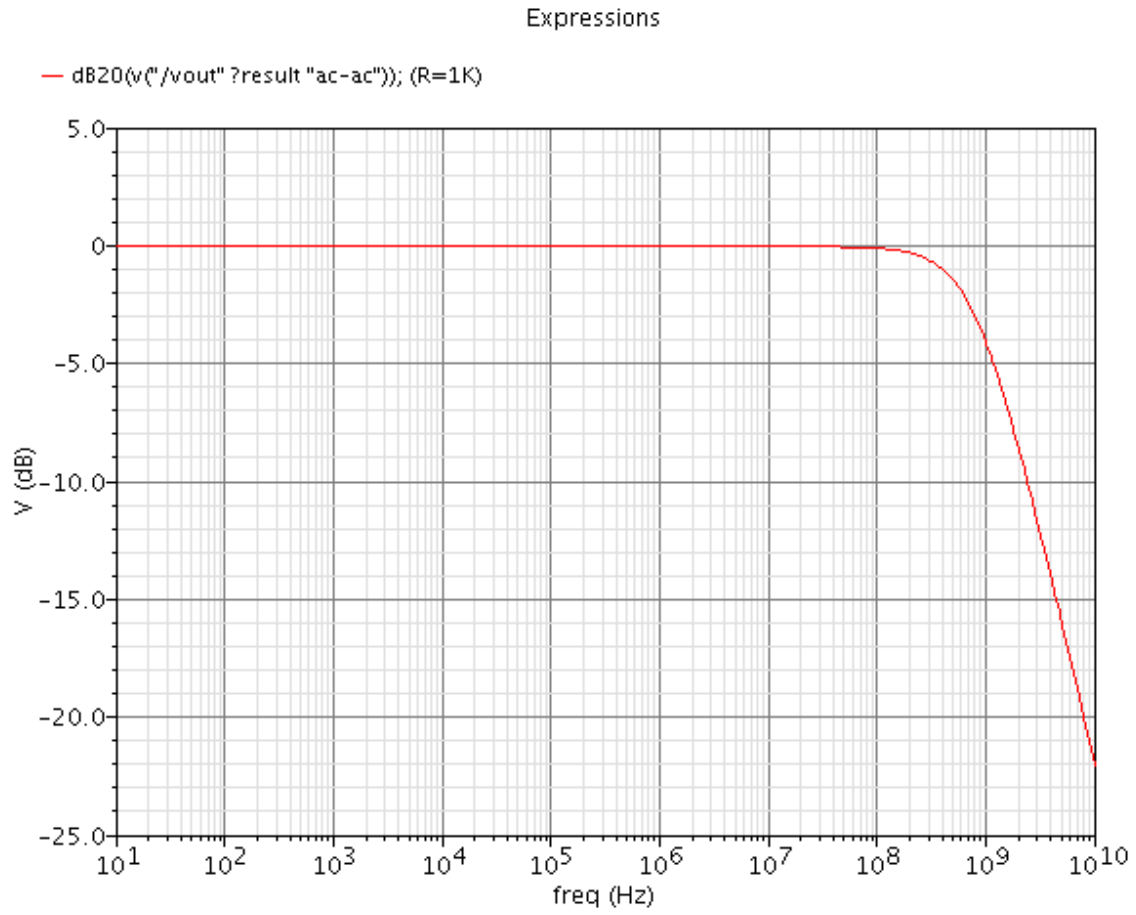


At low frequencies $V_{out}=V_{in}$, as the frequency increases the cap starts to drag the output node to the ground. So it really does work as a low pass filter

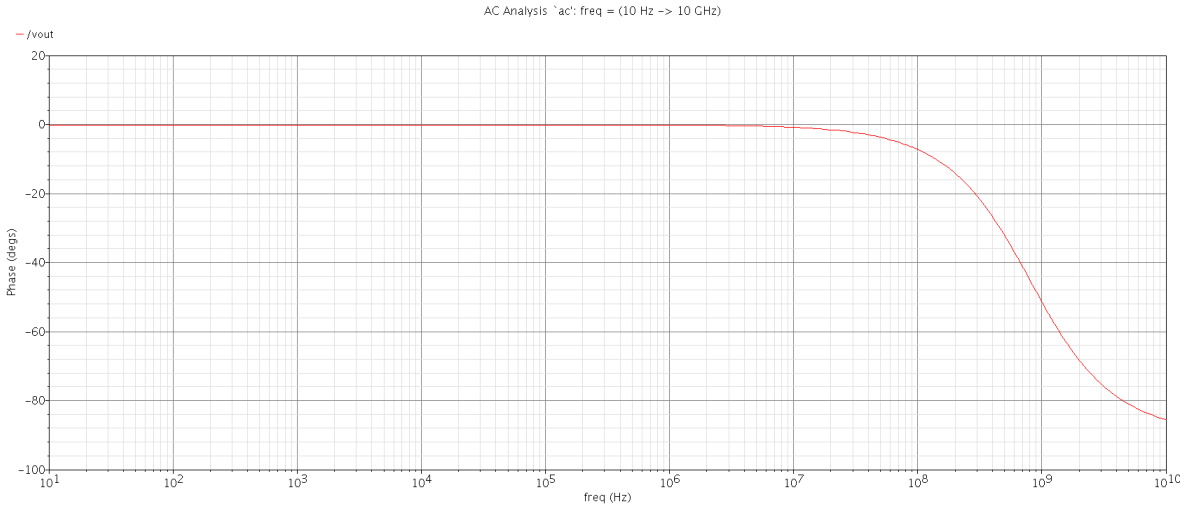
Vout in Log scale:



db20:



Vout phase:



-The LP characteristics gives phase shift 0 at DC and -$90\circ$at $f = \infty$.
-Before the pole frequency by one decade the phase curve start decreasing by $-45\circ/dec$ till reach $-45\circ$ at the pole frequency.
-We can get $-90\circ$ phase shift at $f = \infty$ only which is not a practical frequency.

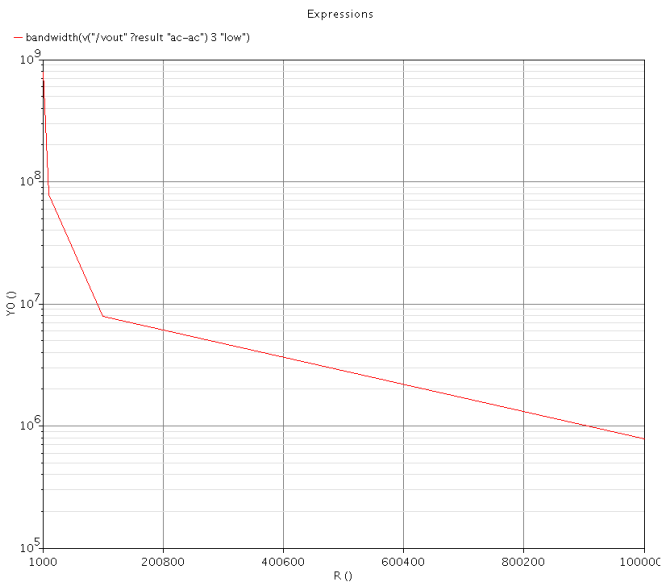
Calculate DC gain and 3dB bandwidth using Cadence calculator expressions. Export the expressions to adexl.

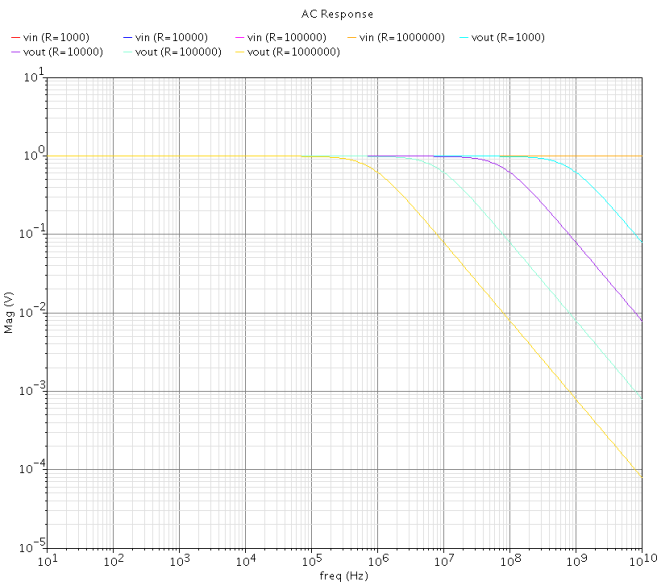
Test	Output	Nominal	Spec	Weight	Pass/Fail
dr.Hesham_assi:lpf:1	/vout				
dr.Hesham_assi:lpf:1	/vin				
dr.Hesham_assi:lpf:1	bandwidth(v("/vout" ?result "...	793.9M			

Compare simulation with analytical results in a table.

	Analytic	Simulation
BW	1/(2*pi*R*C) =795.77MHz	793.9MHz
DC gain	1	1

Do parametric sweep for R=1,10,100,1000$k\Omega$. Report overlaid results. Comment on the results.





Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: R=1k						
1	dr.Hesham_assi:lpf:1	/vout				
1	dr.Hesham_assi:lpf:1	/vin				
1	dr.Hesham_assi:lpf:1	bandwidth(v("/vout" ?result "...	793.9M			
1	AIC_Training:lpf:1	none				
Parameters: R=10k						
2	dr.Hesham_assi:lpf:1	/vout				
2	dr.Hesham_assi:lpf:1	/vin				
2	dr.Hesham_assi:lpf:1	bandwidth(v("/vout" ?result "...	79.39M			
2	AIC_Training:lpf:1	none				
Parameters: R=100k						
3	dr.Hesham_assi:lpf:1	/vout				
3	dr.Hesham_assi:lpf:1	/vin				
3	dr.Hesham_assi:lpf:1	bandwidth(v("/vout" ?result "...	7.939M			
3	AIC_Training:lpf:1	none				
Parameters: R=1M						
4	dr.Hesham_assi:lpf:1	/vout				
4	dr.Hesham_assi:lpf:1	/vin				
4	dr.Hesham_assi:lpf:1	bandwidth(v("/vout" ?result "...	793.9k			
4	AIC_Training:lpf:1	none				

Comment:

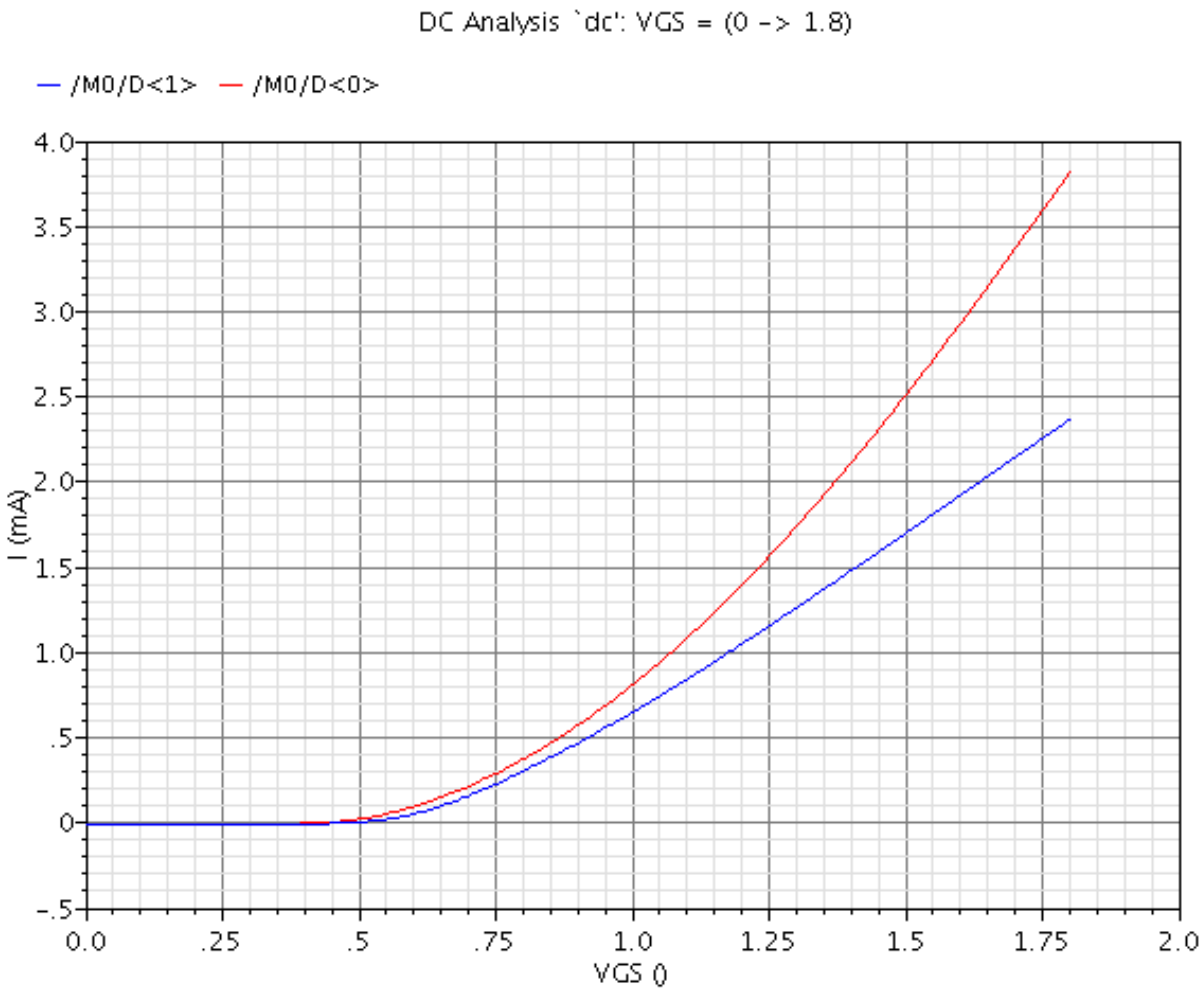
-Pole frequency $\omega_o = 1/RC$, therefore each time we multiply R by 10, the pole frequency (Bandwidth) will be divided by 10.

-The DC gain will not be affected; it is still one for all values of R.

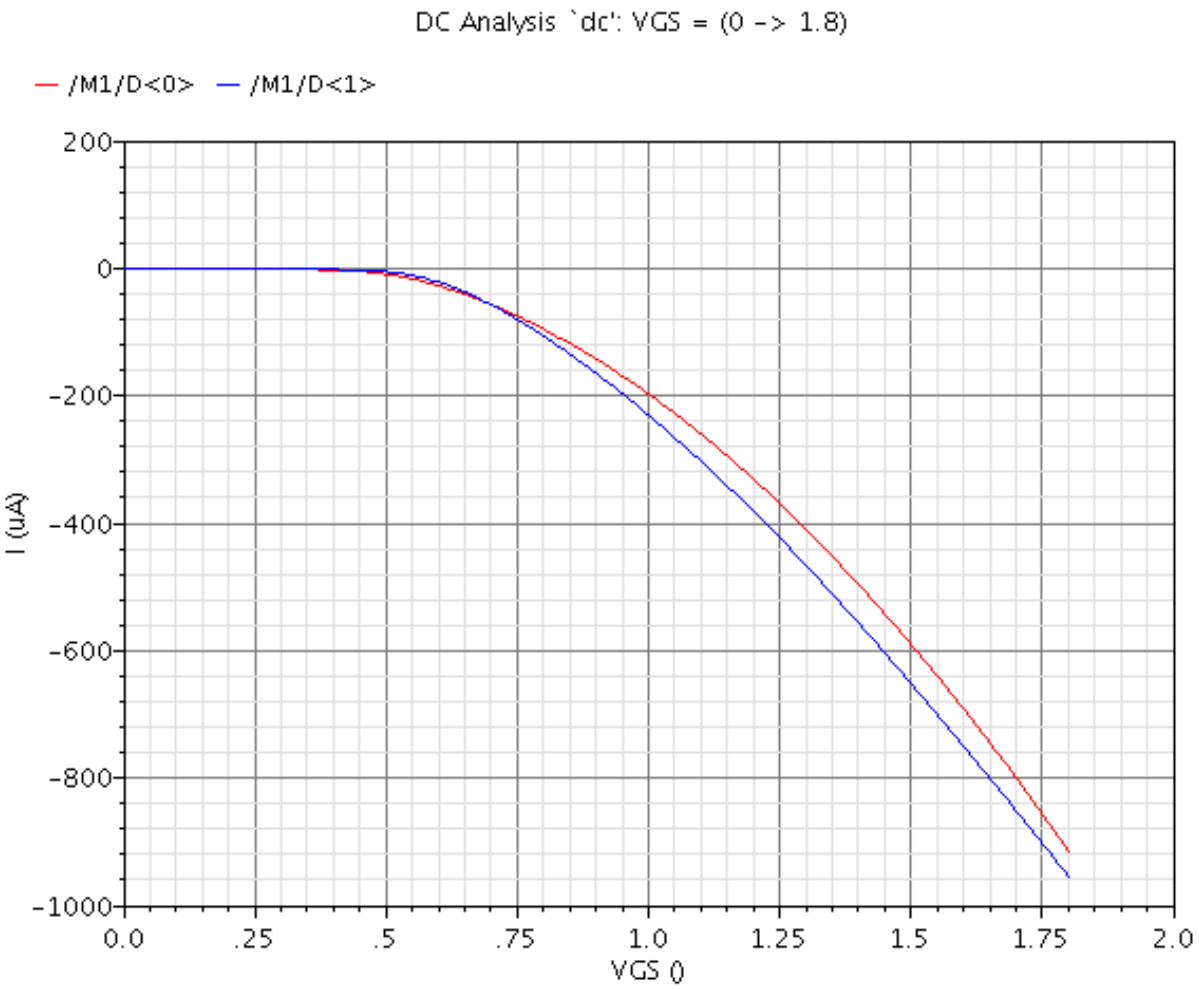
Part 2: MOSFET Characteristics

ID vs VGS:

N_MOS Ids long channel Vs short channel;



P_MOS Ids long channel Vs short channel;



Comment on the differences between short channel and long channel results

Which one has higher current? Why?

NMOS the long channel has higher current than the short channel because of

The aggressive scale down of L causes aggressive increase in the lateral electric field which is responsible for accelerating the free electrons in the channel. The drift velocity of the electrons is directly proportional to the electric field, therefore as E increases the velocity also is also increasing but at certain E the drift velocity will saturate and stop increasing. As V_{GS} increase the V_{ov} also increases till we have V_{ov} greater than the V_{DSsat} which causes velocity saturation and current saturation before we go into the saturation region at $V_{DS} > V_{ov}$ giving much lower current than the expected current

The reduction of L also leads to reduction in the t_{ox} causing higher vertical electric field that will try to pull the free electrons to the gate rather than the drain reducing the mobility of the electrons which will give lower current. This is called mobility degeneration

For PMOS the long channel and short channel are very close to each other since the holes have low mobility and speed therefore the PMOS is far away from the velocity saturation and the saturate when pinch off occurs.

Is the relation linear or quadratic? Why?

For long channel NMOS the relation is quadratic because current saturates when pinch off occurs in saturation region, therefore the square law is still applied

For short channel NMOS the relation starts quadratic but when Vov is higher than $VDSsat$ the current will saturate at $VDSsat$ in the triode region at VGS= VTH+$VDSsat$ and the relation between current and VGS in the triode is a linear relation.

For long and short channel PMOS the relation is quadratic because of that Vov is less than $VDSsat$ therefore current will saturate in the saturation region where the relation between ID and VGS is quadratic.

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Comment on the differences between NMOS and PMOS

Which one has higher current? Why?

• What is the ratio between NMOS and PMOS currents at VGS = VDD?

The NMOS has a higher current than the PMOS because of the difference of the mobility ratio between the NMOS, PMOS devices

The ratio between NMOS, PMOS:

Short channel:

Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:MOS_char:1	N_current				
AIC_Training:MOS_char:1	P_current				
AIC_Training:MOS_char:1	Short_ratio	-2.488			

Long channel:

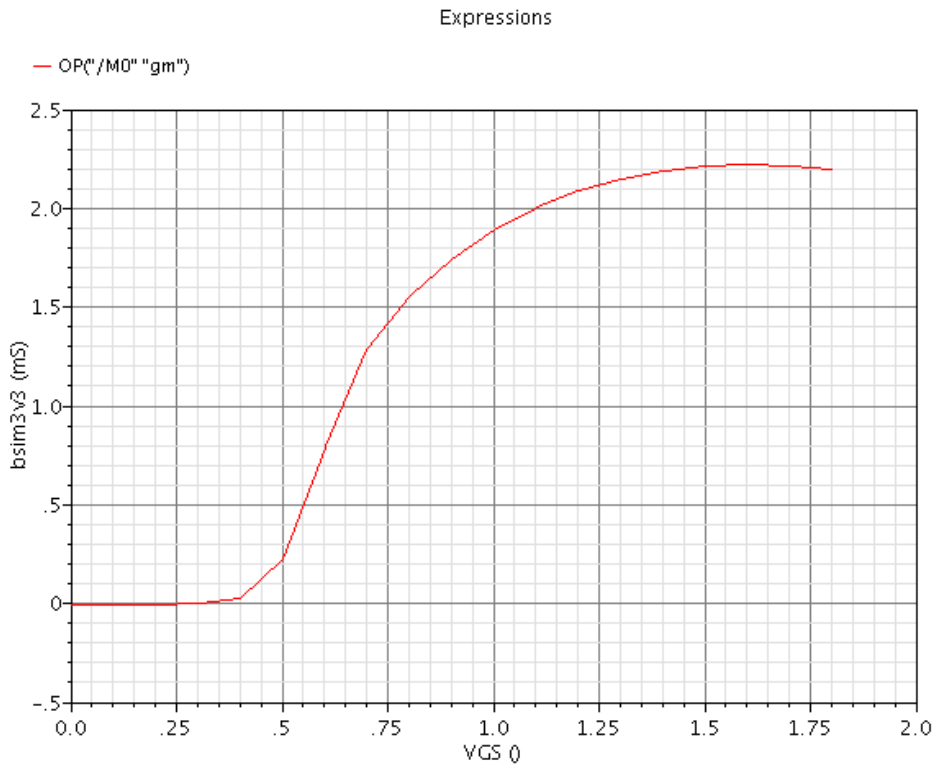
Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:MOS_char:1	N_current				
AIC_Training:MOS_char:1	P_current				
AIC_Training:MOS_char:1	Long_ratio	-4.191			

• Which one is more affected by short channel effects?

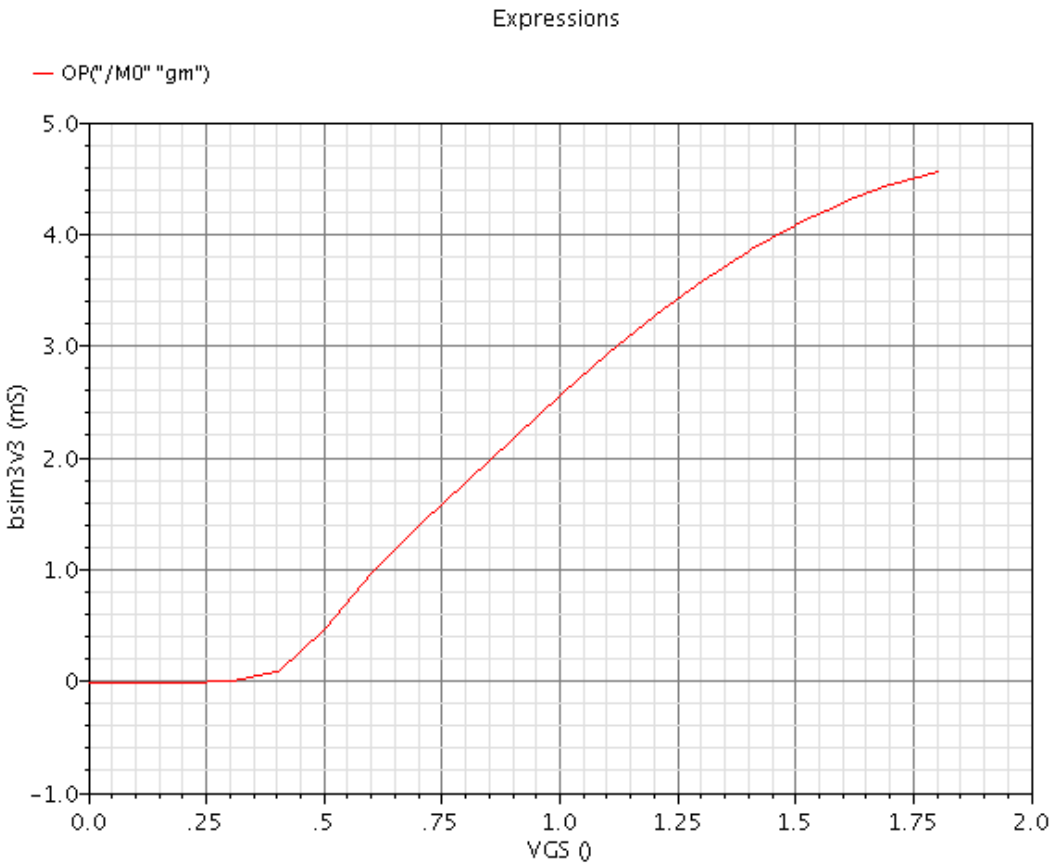
The NMOS is more effected by the short channel (velocity saturation).

g_m vs VGS

Gm VS Vgs for short channel MOS:



Gm VS Vgs for Long channel MOS:



Comment on the differences between short channel and long channel results.

For Long NMOS:

• Does g_m increase linearly? Why?

YES, since when we are in saturation region the relation between $I_D - V_{GS}$ is quadratic and $gm = \partial ID \partial VGS$ which gives a linear relation

• Does g_m saturate? Why?

YES, at $V_{GS} > V_{DS} + V_{TH}$ the NMOS will enter the triode region where the relation between $I_D - V_{GS}$ is linear and $gm = \partial ID / \partial VGS$ which gives a constant

For short NMOS:

Does g_m increase linearly? Why?

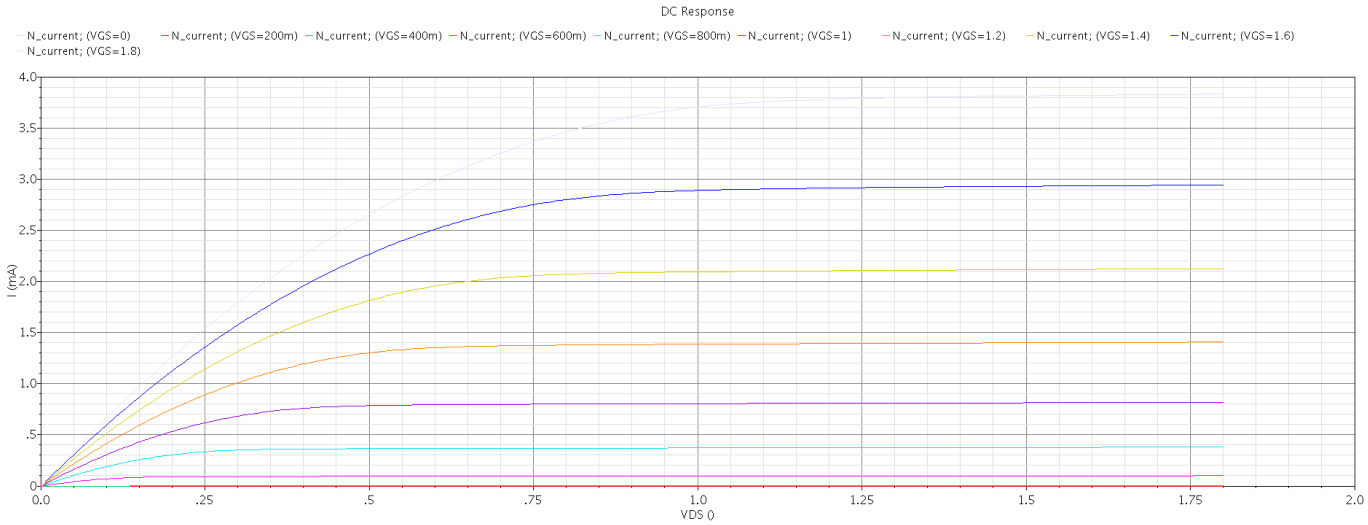
It increases linearly at small V_{GS} when $V_{ov} < V_{DSsat}$ since the relation between $I_D - V_{GS}$ is quadratic and $gm = \partial ID \partial VGS$ = linear, but due to the velocity saturation the current will saturate quickly in triode region where the relation between $I_D - V_{GS}$ is a linear relation and $gm = \partial ID / \partial VGS$ = constant.

• Does g_m saturate? Why?

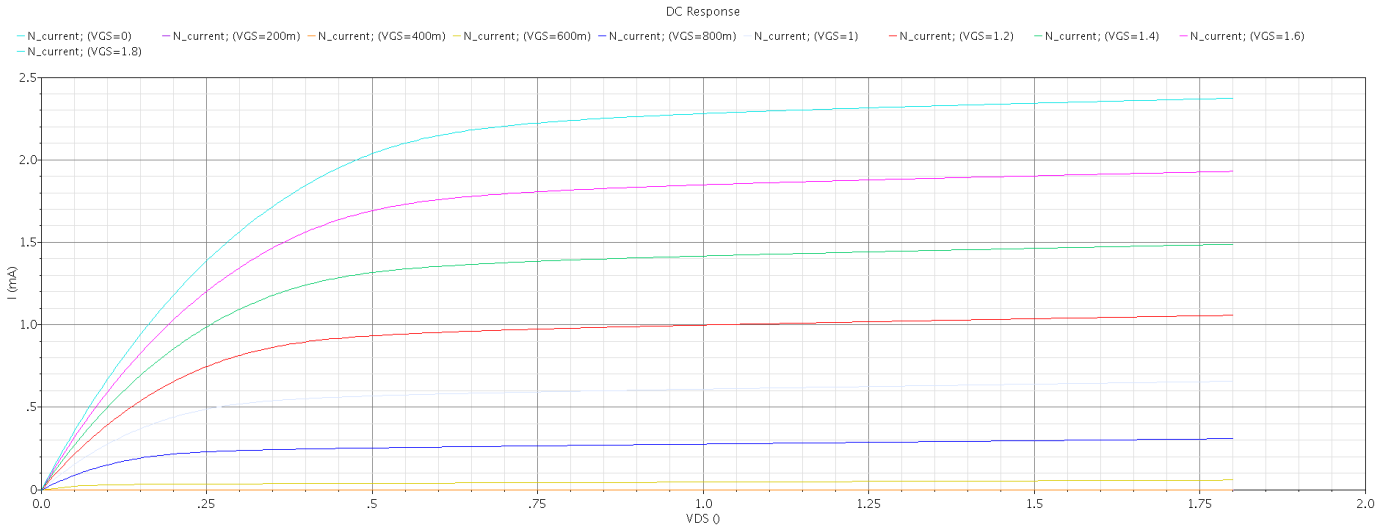
yes, and at much smaller V_{GS} and V_{ov} due to velocity saturation.

ID vs VDS

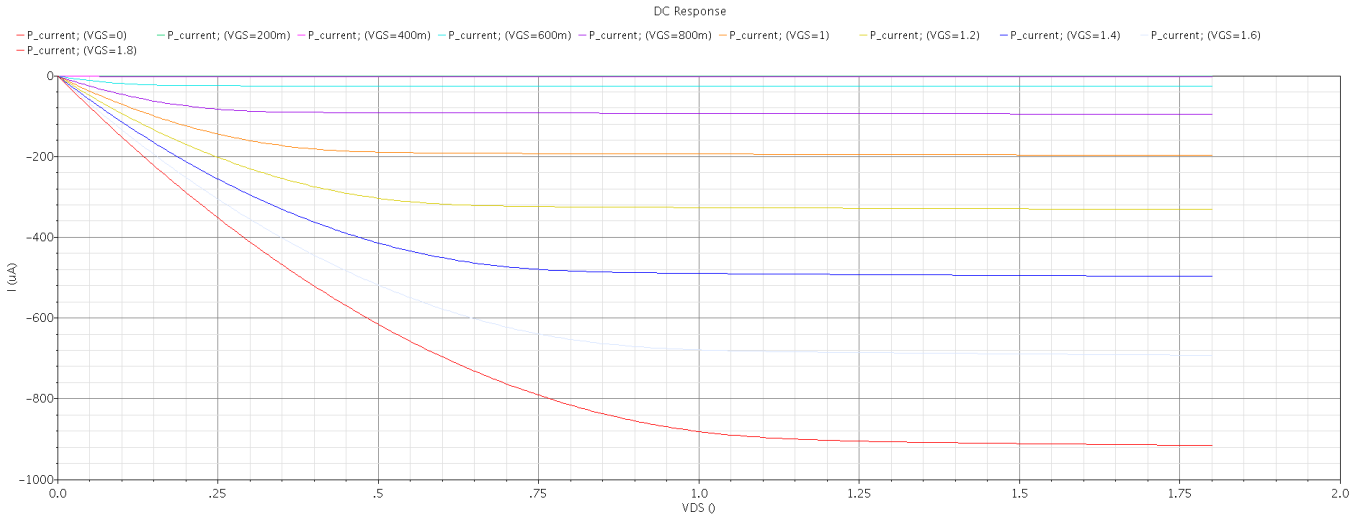
$I_D - V_{DS}$ characteristics for NMOS device for Long channel device:



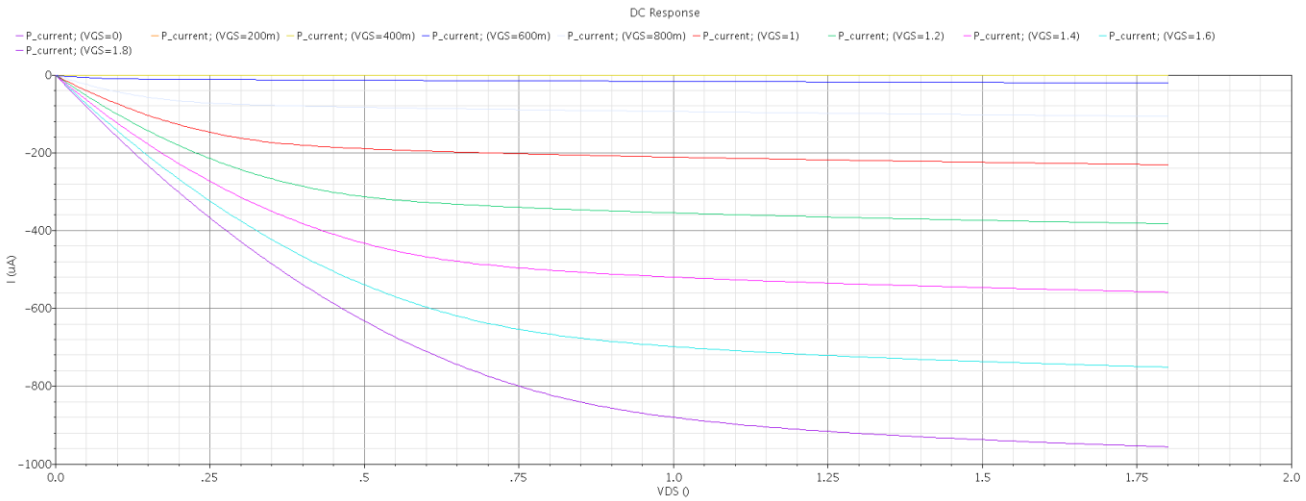
$I_D - V_{DS}$ characteristics for NMOS device for short channel device:



$I_D - V_{DS}$ characteristics for PMOS device for Long channel device:



$I_D - V_{DS}$ characteristics for PMOS device for short channel device:



Comment on the differences between short channel and long channel results.

Which one has higher current? Why?

Long channel has higher current, because that short channel suffers from velocity saturation and mobility degeneration.

Which one has higher slope in the saturation region? Why?

Short channel has higher slope than long channel, since the short channel current has higher dependence on V_{DS} much more than long channel current due to the DIPLE effect in addition to the channel length modulation is more significant in short channel MOS.