Analog IC
Design Lab 06
Differential Amplifier

PART 1: Sizing Chart

W=10 uM L=1 uM VCM=0.7V VDD=1.8V Av=8 ISS=40uA

Id=20 uA

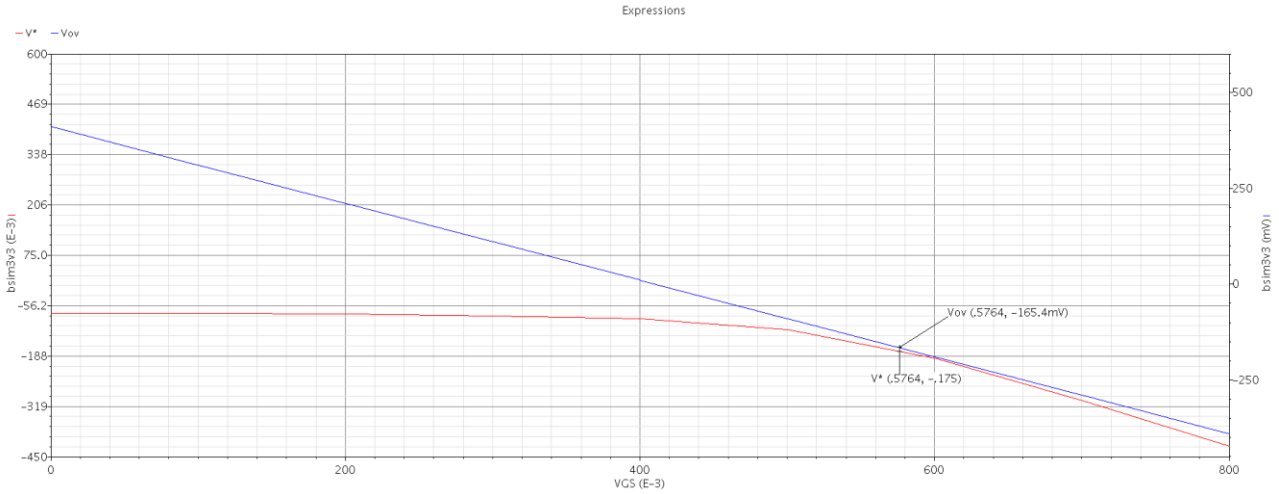
Choose R_D to meet the CM output level spec.

$$Vcm_{out} = \frac{I_{ss}}{2} * R_d \rightarrow R_d = 35\ k\ \Omega$$

Choose V_* to meet the differential gain spec.

$$A_v = 2 * \frac{I_d}{V^*} R_d \rightarrow V^* = 175\ mV$$

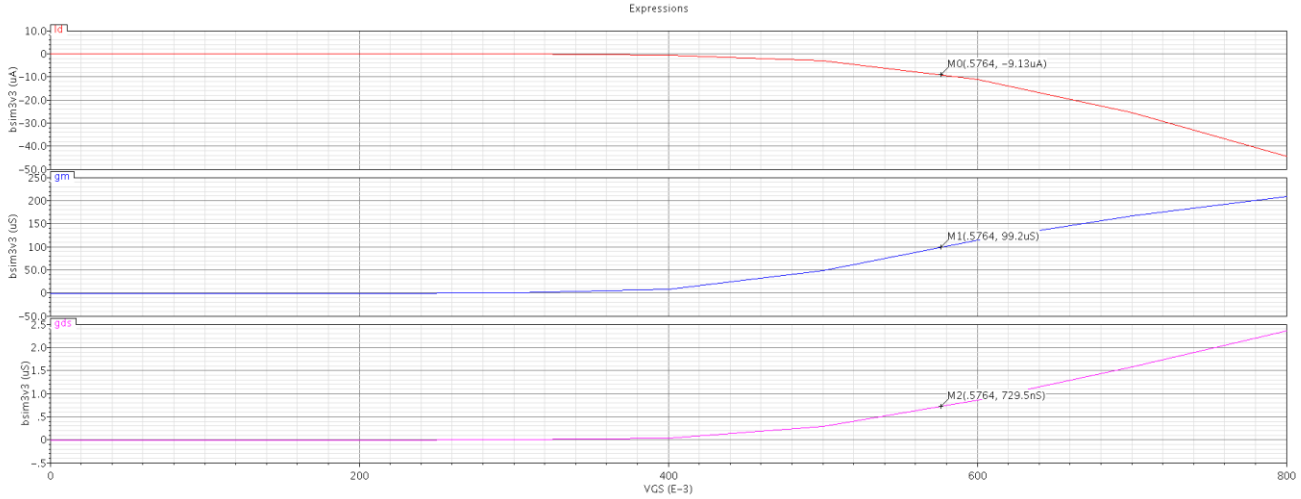
Plot V_* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range



On the V_* and V_{ov} chart locate the point at which V_* is equal to the value your previously calculated to meet the gain spec. Find the corresponding V_{ovQ} and V_{GSQ}.

Vgsq=576.4 mV Vovq=-165.4 mV

Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.



Idx=-9.13 uA gmx=99.2 uS gdsx=729.5 nS

Calculate W

$W_{new} = 10u * \frac{20u}{9.13u}$=21.905 uM

calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication)

gmq=217.2976 uS gdsq=1.5979 uS ro=625.79 kΩ

PART 2: Differential Amplifier

Analytically calculate the valid range for Vicm: the common mode input range (CMIR). Set Vicm at the center of this range.

$$VICM_{min} = \frac{I_{ss}}{2} R_D - V_{th} = 0.2888V$$

$$VICM\_\max = VDD - 2V_{ov} - V_{th} = 1.0556V$$

Then we will use the center which is equal to VICM=0.67 V

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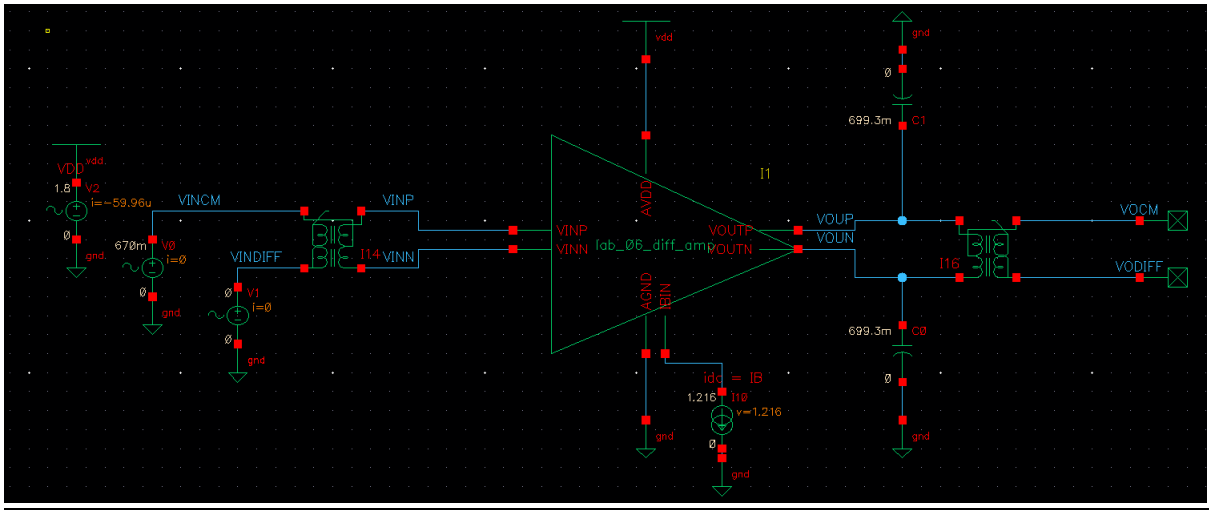
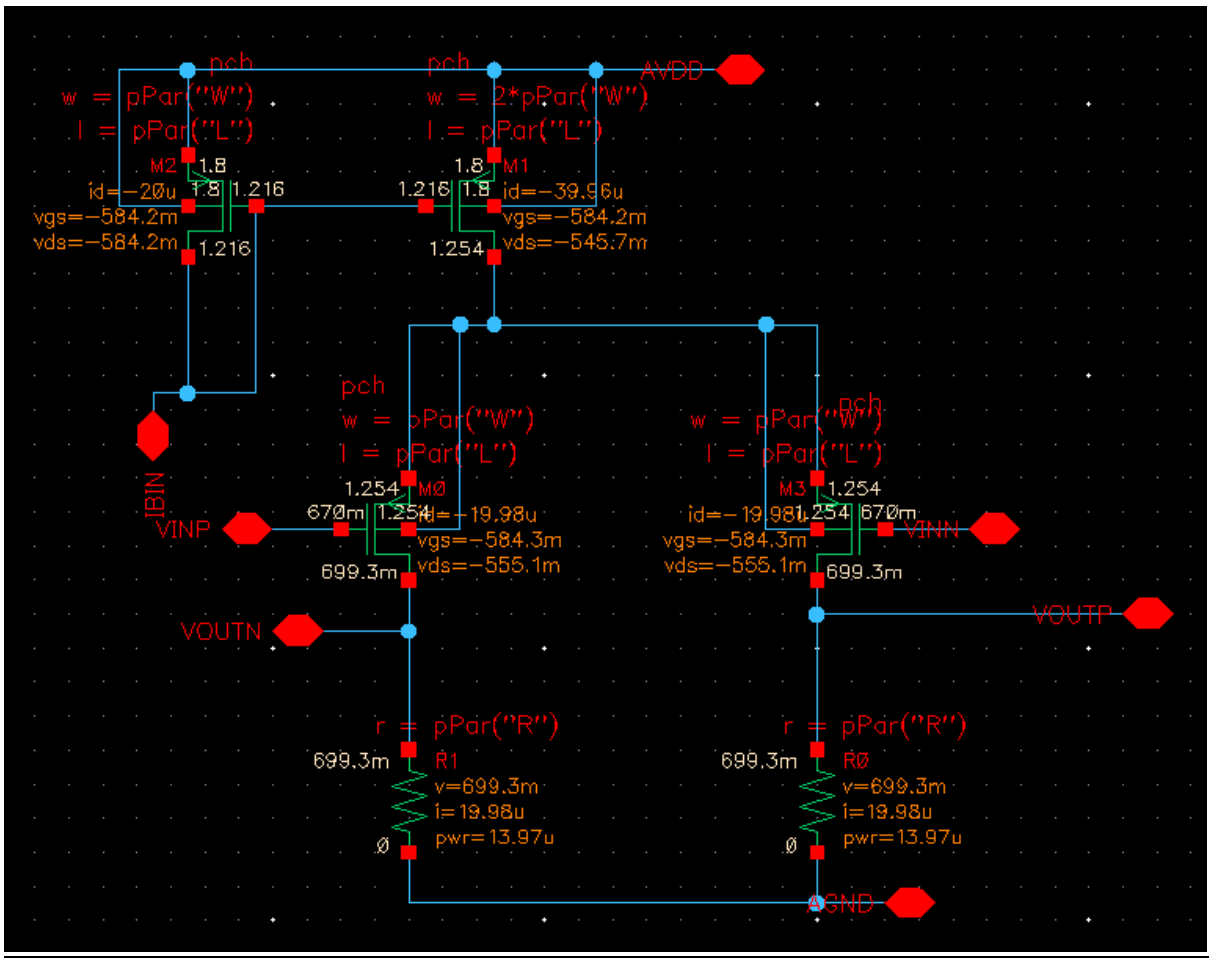
1) **OP simulation**

Report the schematic of the diff pair with DC OP point clearly annotated: id, vgs, vds, vth, vdsat, gm, gds, gmb, region.





DC node voltages and all other specs:

	A			
1				
2				
3	Name	/I1/M0	/I1/M1	/I1/M2	/I1/M3
4	cgd	-14.46f	-28.93f	-14.45f	-14.46f
5	cgs	-147.5f	-294.9f	-147.5f	-147.5f
6	gds	1.768u	3.553u	1.749u	1.768u
7	gm	225.8u	452u	226.1u	225.8u
8	gmoverid	11.3	11.31	11.3	11.3
9	id	-19.98u	-39.96u	-20u	-19.98u
10	region	2	2	2	2
11	type	1	1	1	1
12	vds	-555.1m	-545.7m	-584.2m	-555.1m
13	vdsat	-148m	-148.3m	-147.9m	-148m
14	vgs	-584.3m	-584.2m	-584.2m	-584.3m
15	vth	-411.1m	-411.2m	-411.1m	-411.1m
16					
17					
18	Region 0 is cutoff.				
19	Region 1 is linear.				
20	Region 2 is saturation .				
21	Region 3 is subthreshold.				
22	Region 4 is breakdown.				
23					
24	Type 0 is nMOS.				
25	Type 1 is pMOS.				
26					

Check that all transistors operate in saturation

All transistors are in region 2 (sat).

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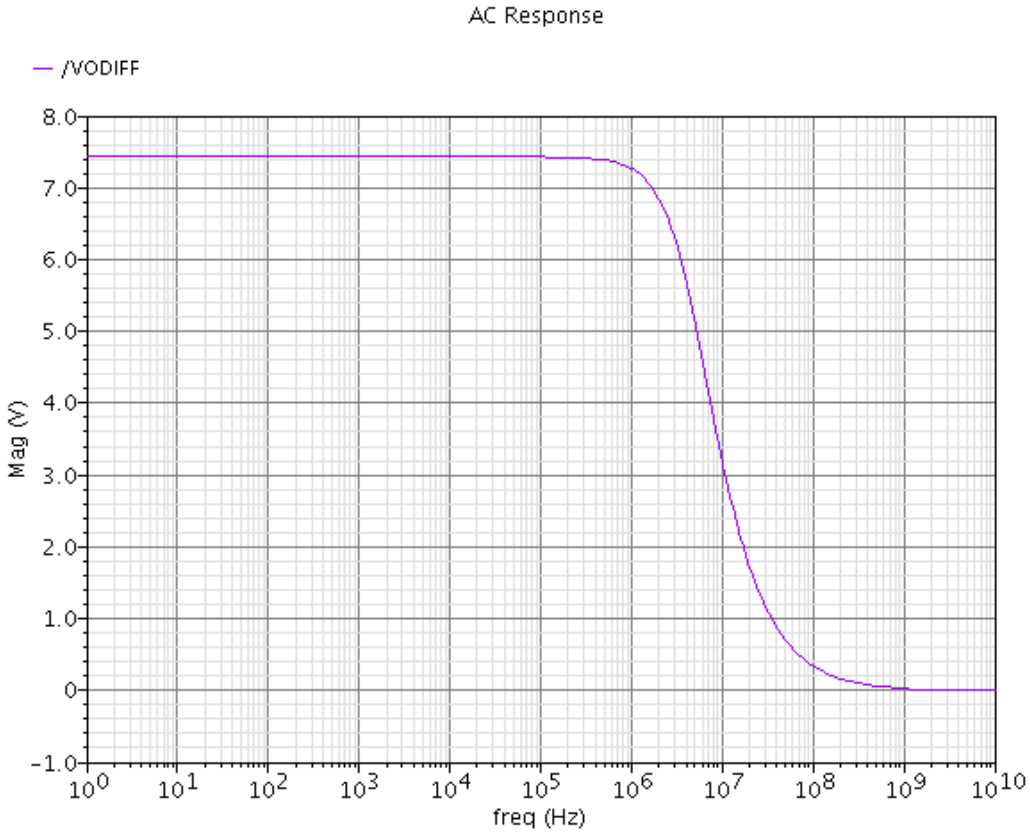
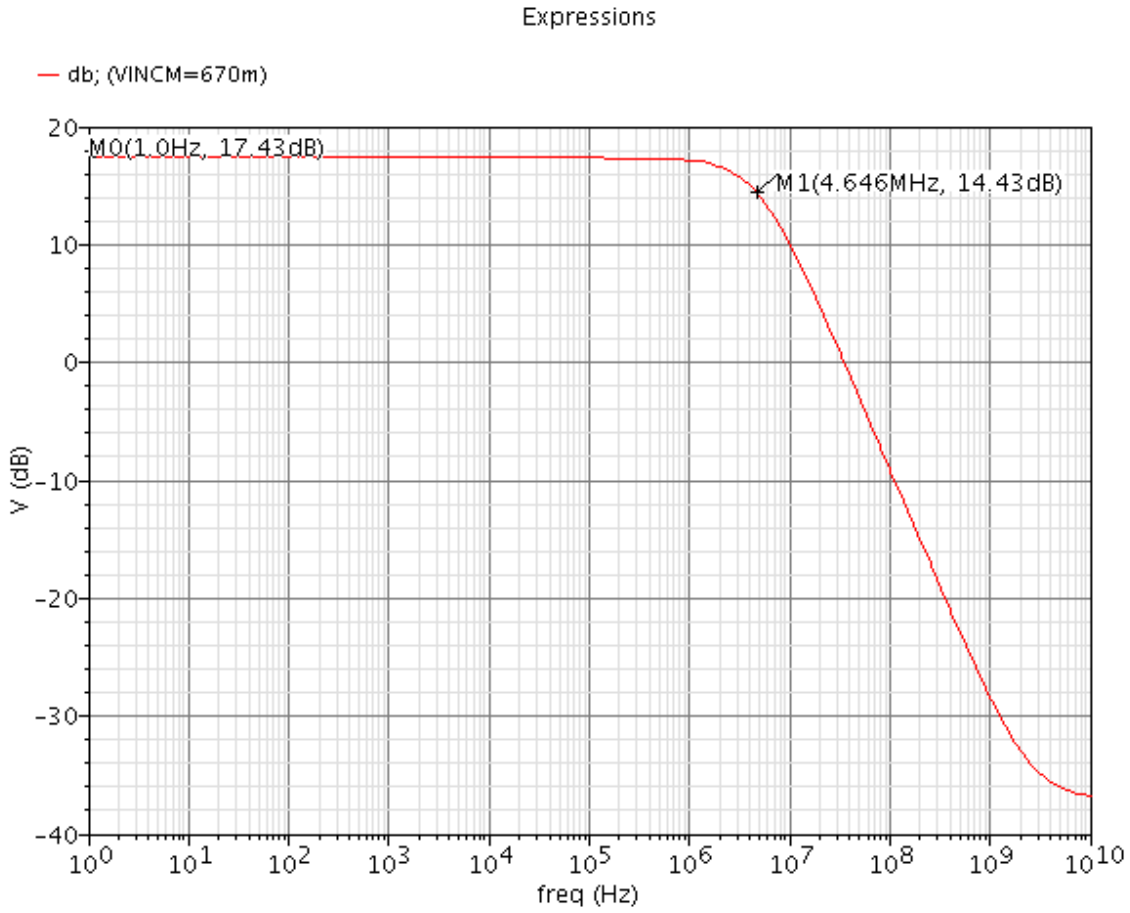
2) Diff small signal ccs:

Report the Bode plot of small signal diff gain.



Bandwidth:



Compare the DC diff gain and BW with hand analysis in a table.

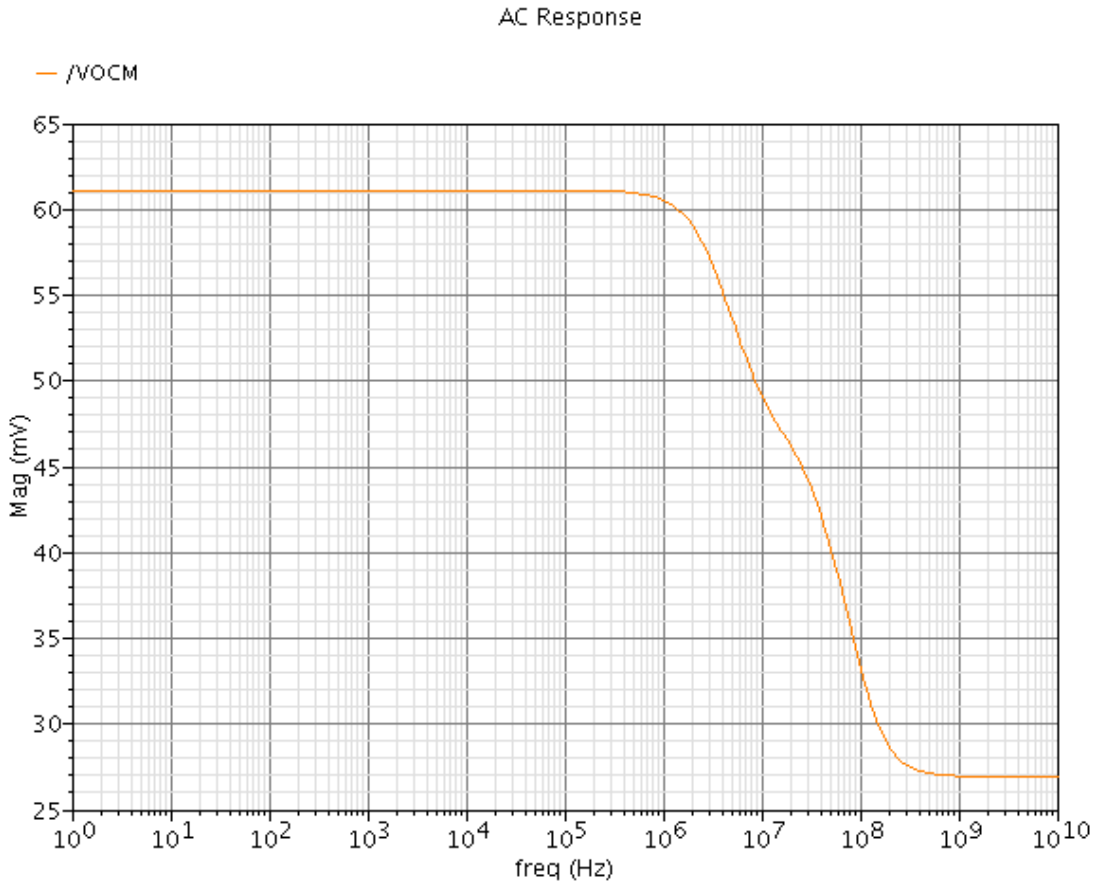
$A_{vd} = g_m * (r_0 \,//R_D)$=7.442

Bandwidth = $\frac{1}{2pi*(r_0//R_d)*C_L}$=4.547 MHz

	Analytically	Simulation
Gain	7.442	7.4387
BW	4.547 MHz	4.646 MHz

3) CM small signal ccs:

Report the Bode plot of small signal CM gain



Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?

	Analytical	Simulation
DC CM gain	61.6m	61 mV

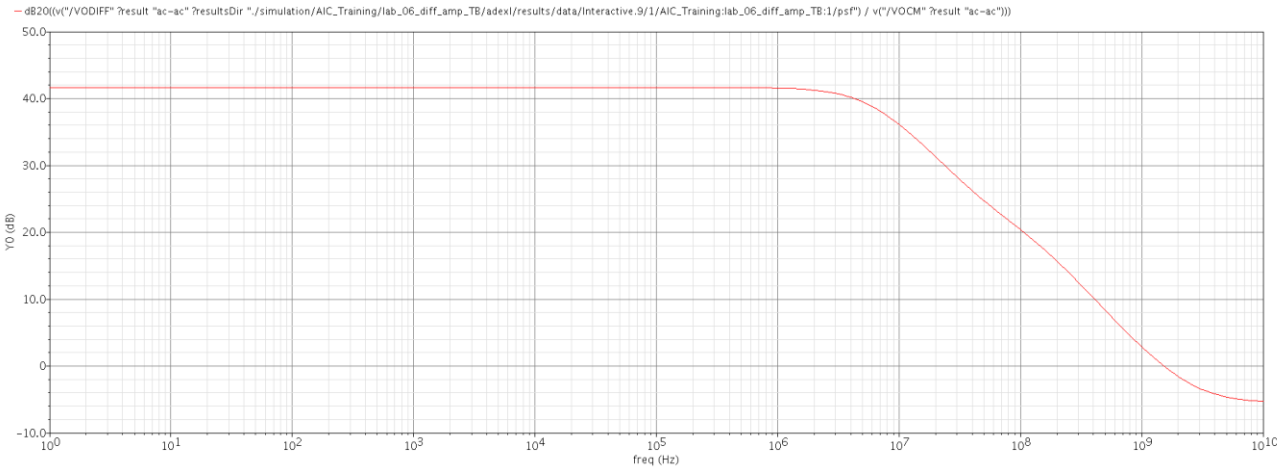
Yes, less than 1 as expected because I design this circuit to reject the CM signal

Justify the variation of Avcm vs frequency.

The system first faces the dominant pole which gives the -20db/dec that the graphs shows

Then it faces a zero which tries to increase the slope which shows the slight increase in slope at about 10^7 Hz then comes the non dominant pole which decreases the slope again.

Plot Avd/Avcm in dB. Compare Avd/Avcm



Compare Avd/Avcm @ DC with hand analysis in a table.

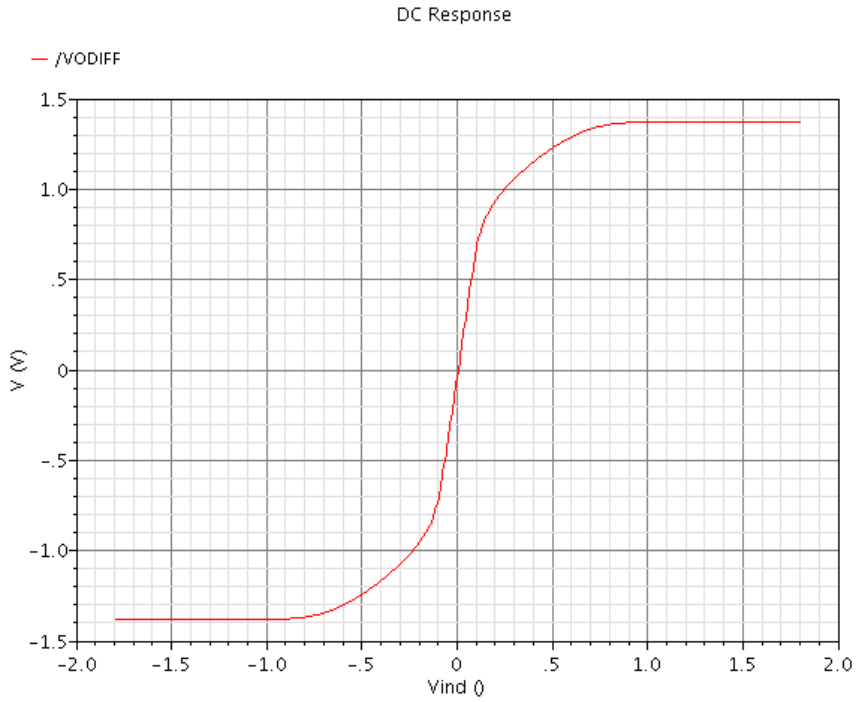
	AVCM	**AVD**
Gain	-61.4 m	7.442

Justify the variation of Avd/Avcm with frequency.

the same reason for the variations of AVCM because the system faces dominant pole then it faces a zero which slightly increase the slope then face another pole which continue to the end.

4) Diff large signal ccs:

Report diff large signal ccs (VODIFF vs VIDIFF)



Compare the extreme values with hand analysis in a table.

@Vid=-1.5V

Left branch is off , Id=0

Right branch is on , Id=Iss=40 uA

Vout=-IssRd=-1.5 V

@Vid=1.5V

Left branch is on , Id=Iss=40 uA

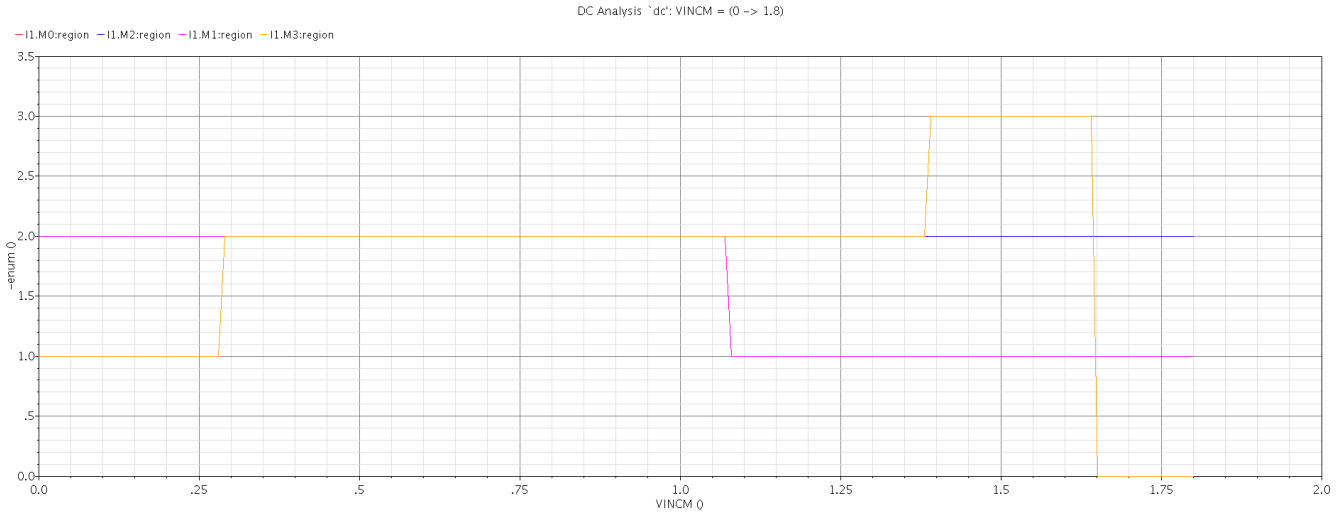
Right branch is off , Id=0

Vout=-IssRd=1.5 V

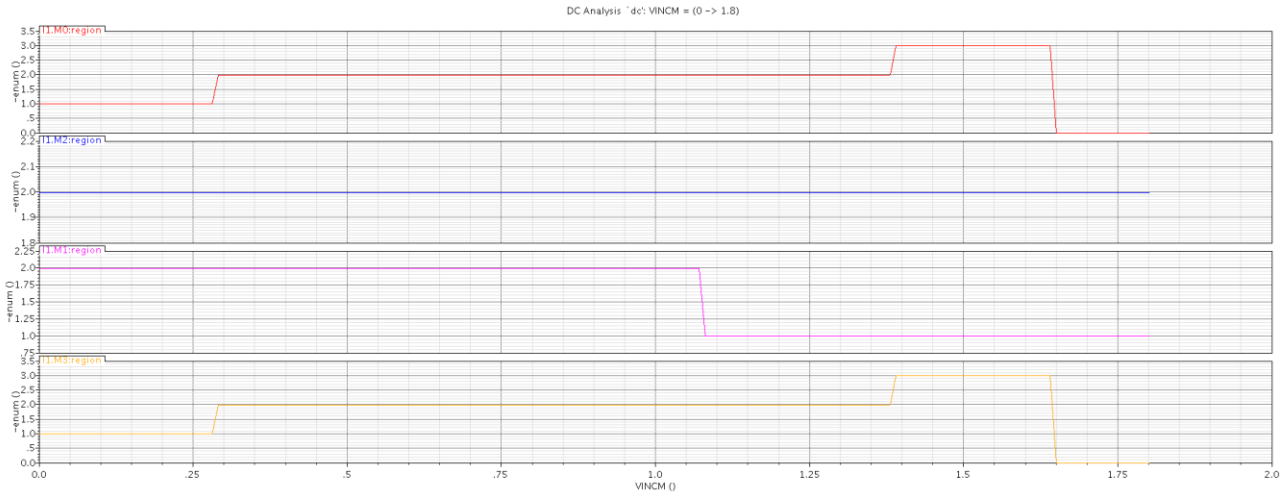
	Vout
@Vid=-1.5V	-1.5
@Vid=1.5V	1.5

5) CM large signal ccs (region vs VICM):

Plot "region" OP parameter vs VICM for the input pair and the tail current source



Here is another snapshot if this one is not clear.



Find the CM input range (CMIR). Compare with hand analysis in a table

For the tail CS (M1) and input pair (M0 , M3)
the input CM range is from 0.28 -> 1.05 V

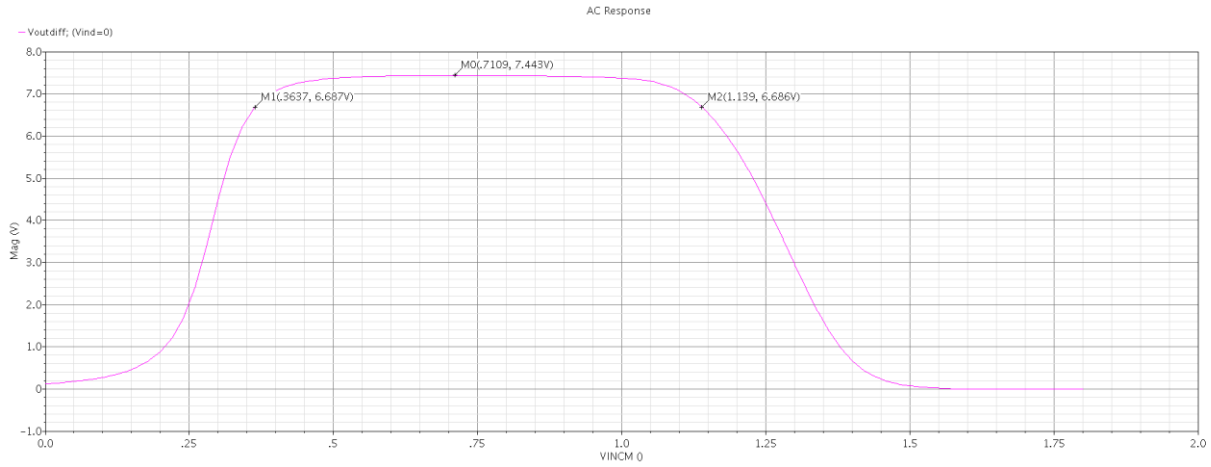
	Hand analysis	Simulation
CMIR	1.0556-0.2888=0.7668V	1.05-0.28=0.77V

6) CM large signal ccs (GBW vs Vicm):

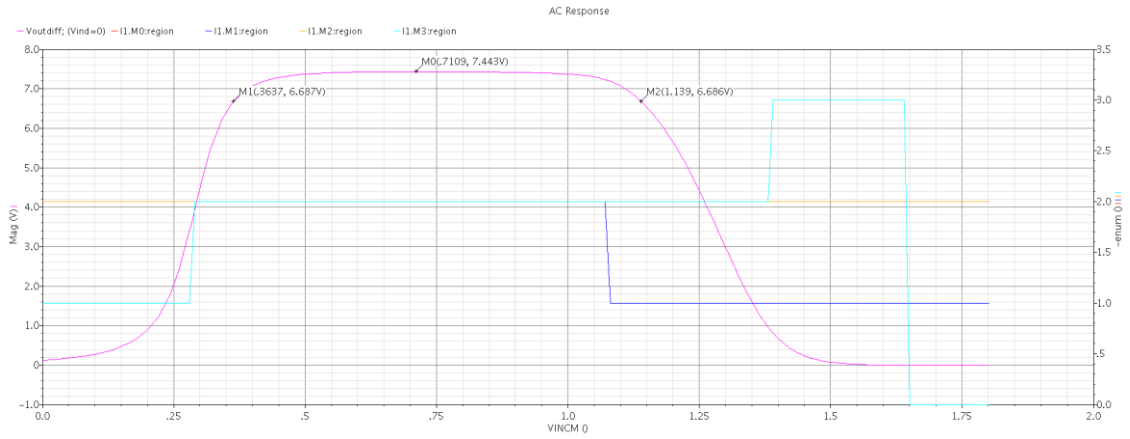
Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain

Test	Output	Nominal	Spec	Weight	Pass/Fa
AIC_Training:lab_06_diff_amp_TB:1	Voutdiff				
AIC_Training:lab_06_diff_amp_TB:1	ymax(mag(VF("/VODIFF")))	7.443			
AIC_Training:lab_06_diff_amp_TB:1	none				

the max output is 7.443V so 90% of it is 6.687V



Plot the results overlaid on the results of the previous method (region parameter). Find the CM input range. Compare with the previous method in a table.



From the previous graph.

The CMIR=1.139-0.3637=0.7682 V

	CMIR
Regions	0.77
GBW	0.7682

The GBW is way more better than the regions as the regions first is a simulation parameter only and second has a very sharp edged between transitions while the GBW is a logical and experimental way to tell the valid range and leaves the designer to his own estimation whether he accepts 90% of the output or maybe less