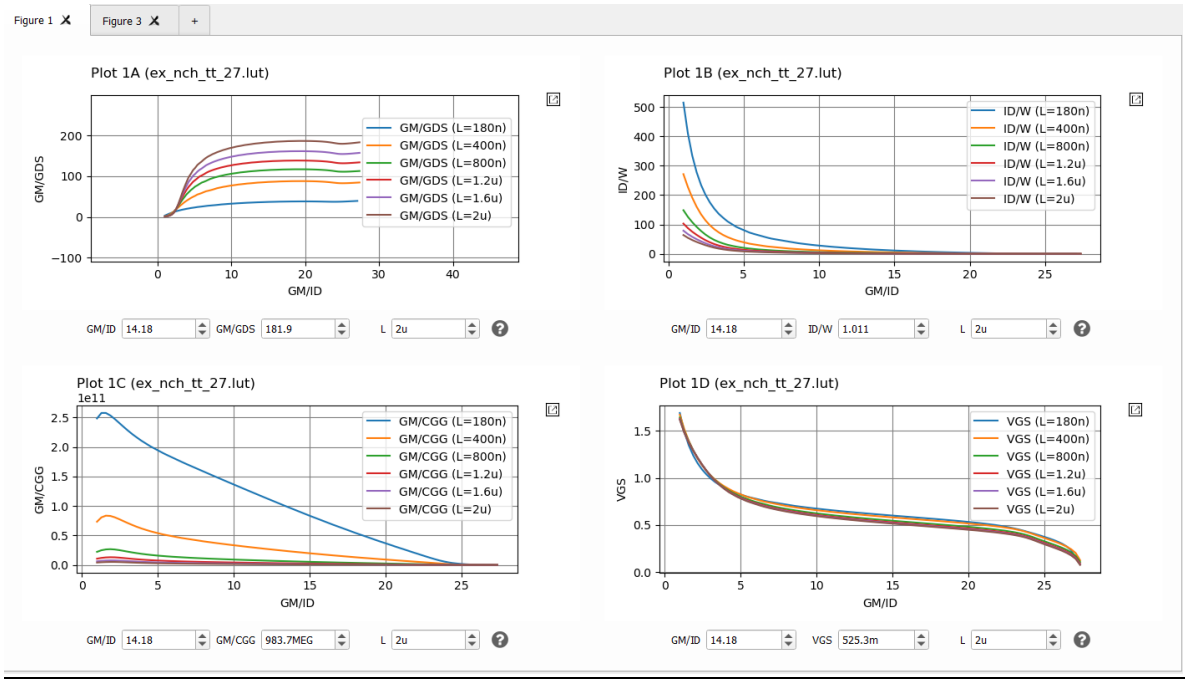
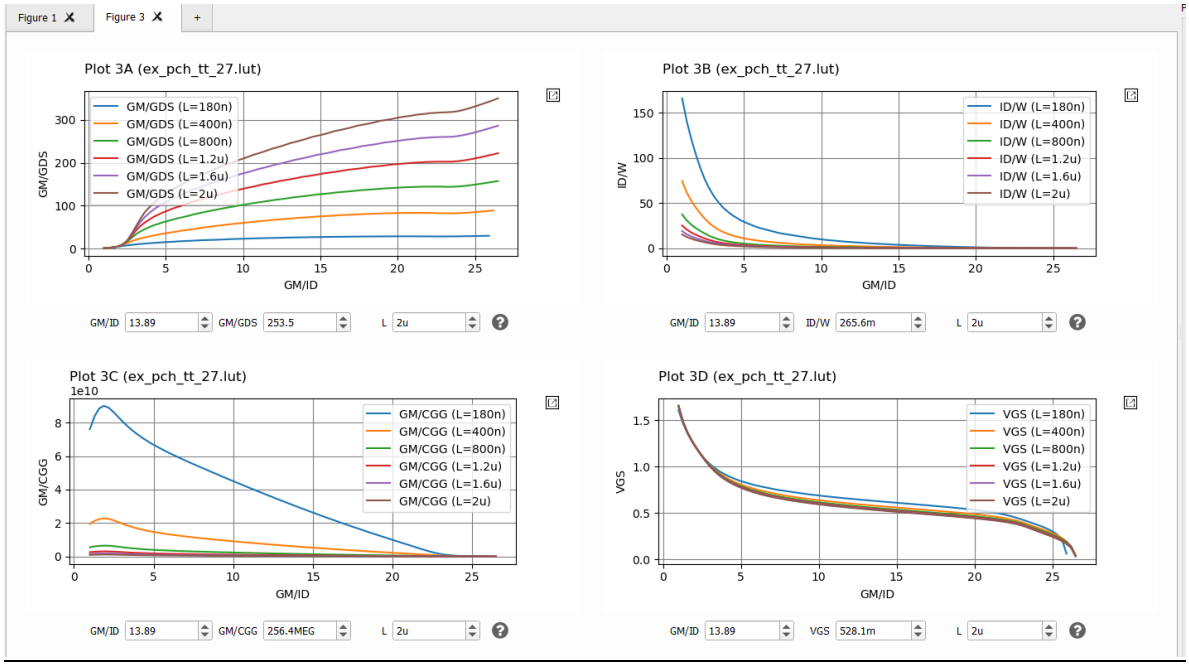
Analog IC Design
Lab 07
gm/ID Design Methodology

PART 1: gm/ID Design Charts

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 and L = 0.18u,0.4u:0.4u:2u



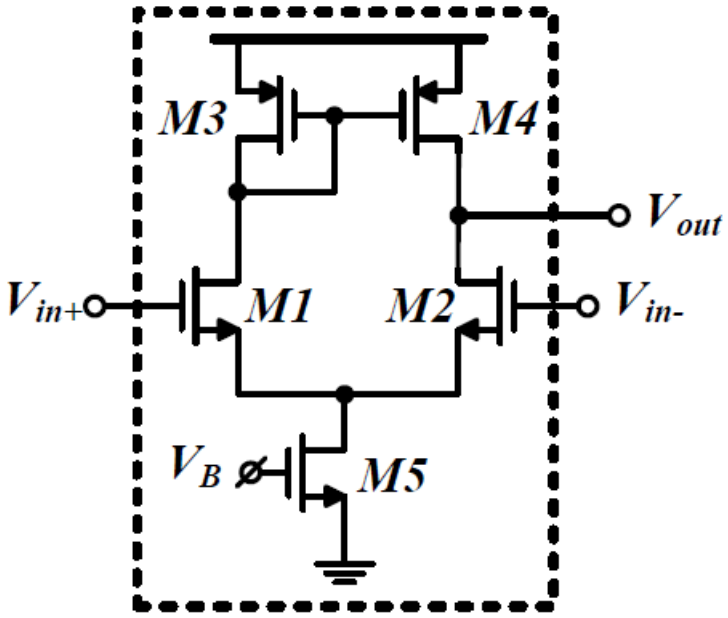


PART 2: OTA Design

Design specs

Iref=10Ua	Vdd=1.8V	Cl=5pF	DC gain=34 dB=50	CMRR=74 dB
Iss=20uA	CMIR_low=0.8V	CMIR_high=1.5V	GBW=5MHz	

-The gain is not very high so it can be implemented by a **ota-5T**
-since CMIR is closer to the VDD rail , so I will use **NMOS input pair**
-current Iss is 10uA and I need 20 uA Iss to flow 10uA in each branch so I will put a current mirror to double the reference current



This is the topology that I will design except that there is another mostef M6 will mirror the current to M5.

Design of the input NMOS pair:

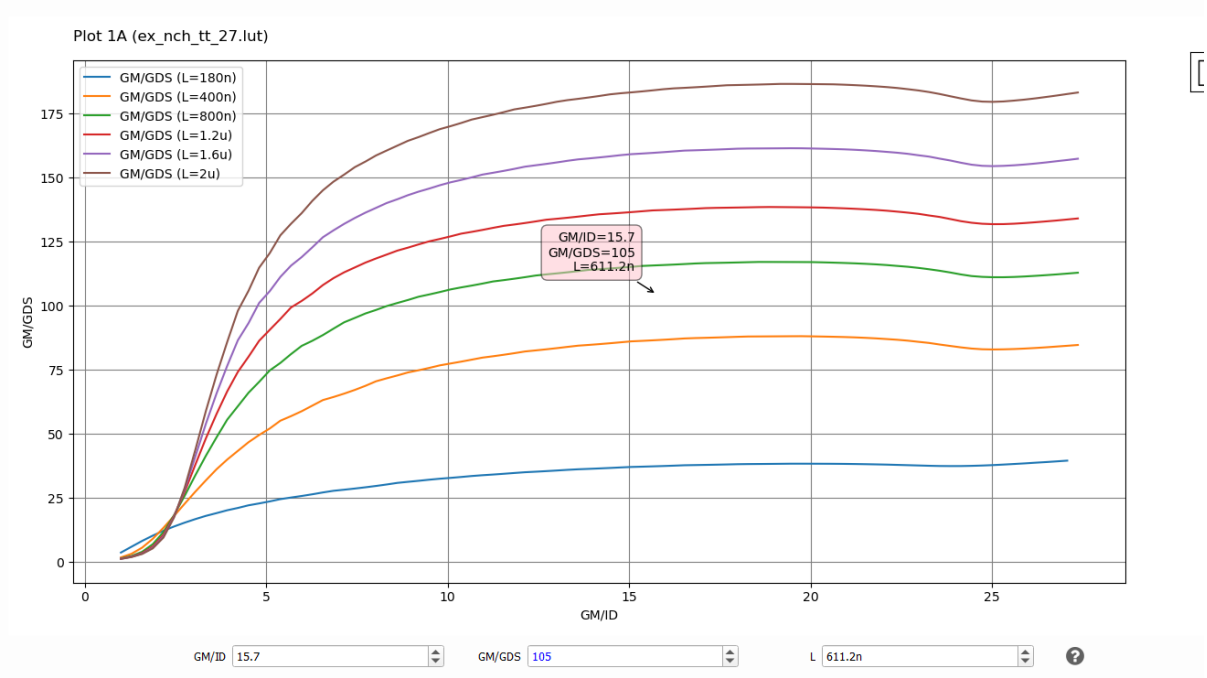
$$\text{GBW} = \frac{g_{m1,2}}{2 * pi * C_L} \rightarrow g_{m1,2} = 157.07uS$$

$$I_D = \frac{I_{ss}}{2} = 10uA \rightarrow \left(\frac{g_{m1}}{I_D}\right)_{1,2} = 15.7$$

$$A_v = g_{m1,2} * \frac{r_o}{2} \geq 50 \rightarrow \frac{g_{m1,2}}{g_{ds2,4}} \geq 100$$

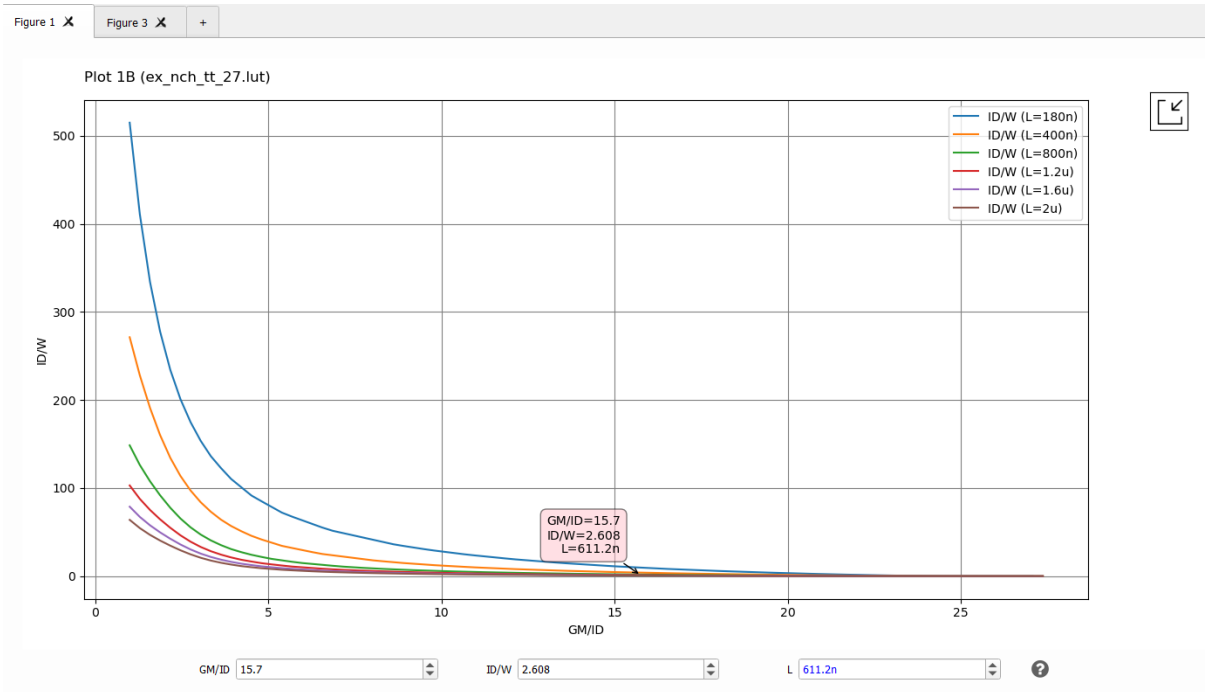
$$g_{ds2,4} \leq 1.57\ uS$$

Take $\frac{gm}{gds} = 105$



From here, length of M1,2

$$L_{1,2} = 611.2nm$$



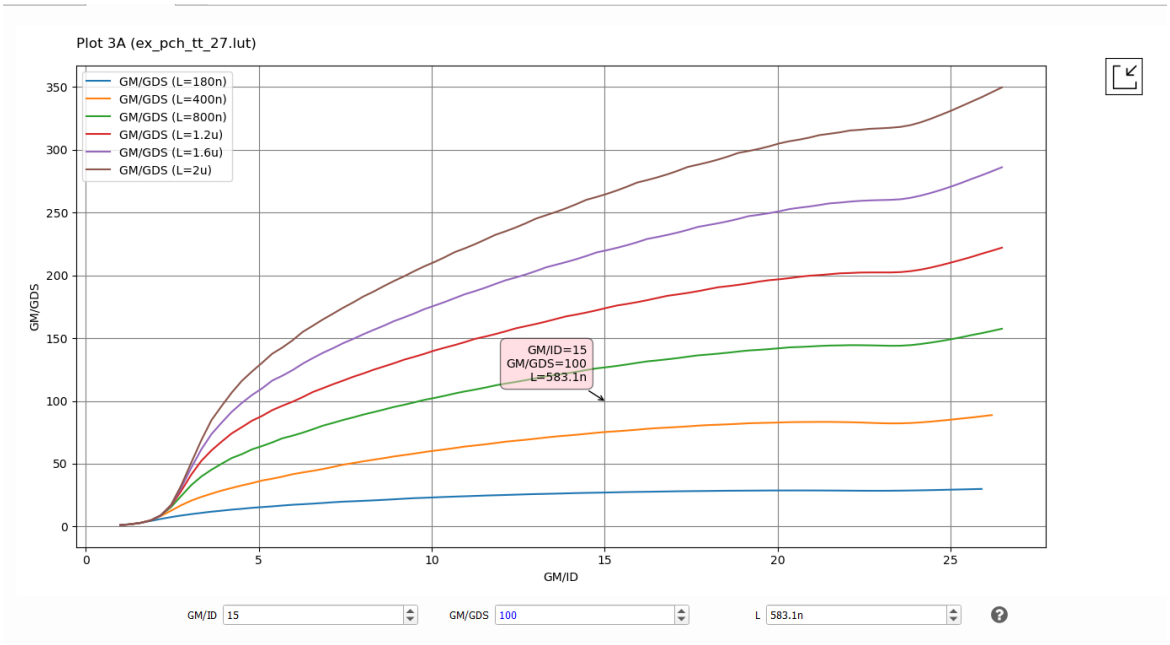
At gm/Id =15.7 , L=661.2nm

$$\frac{I_D}{W} = 2.68 \rightarrow W_{1,2} = 3.834um$$

Design of the PMOS Current mirror load:

Assume $\frac{g_{m3,4}}{ID} = 15 \rightarrow g_{m3,4} = 150uS$

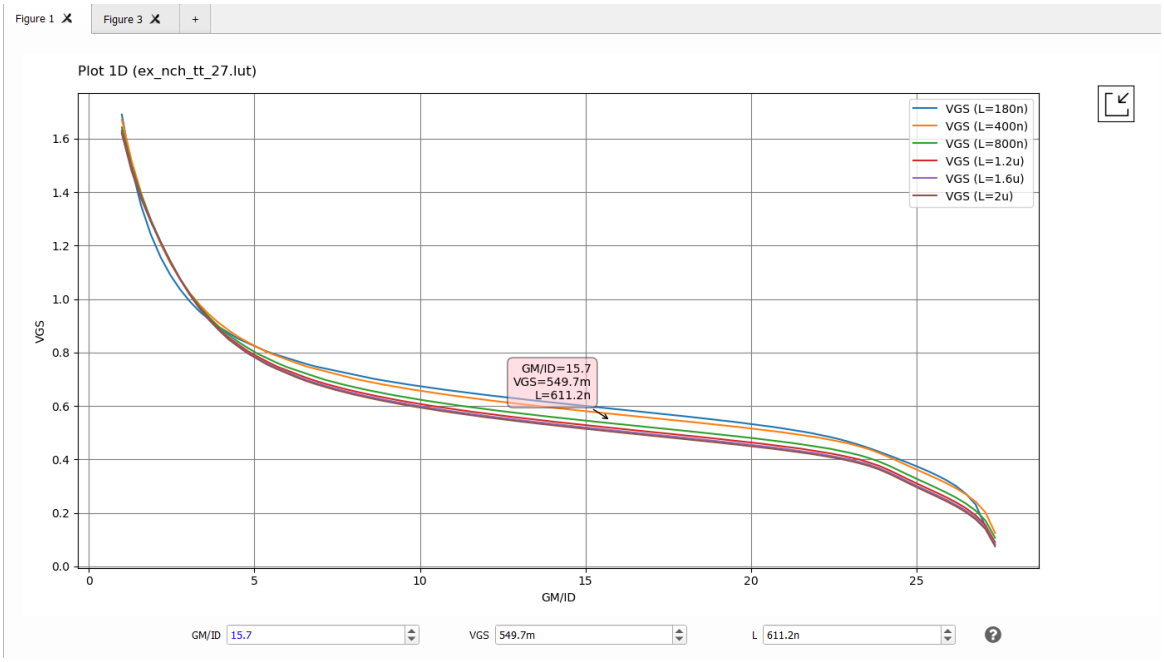
Therefore $\frac{g_{m3,4}}{g_{ds3,4}} = \frac{150u}{1.57u} = 95.54 \rightarrow take\ it\ 100$



$L_{3,4} = 583.1nm$

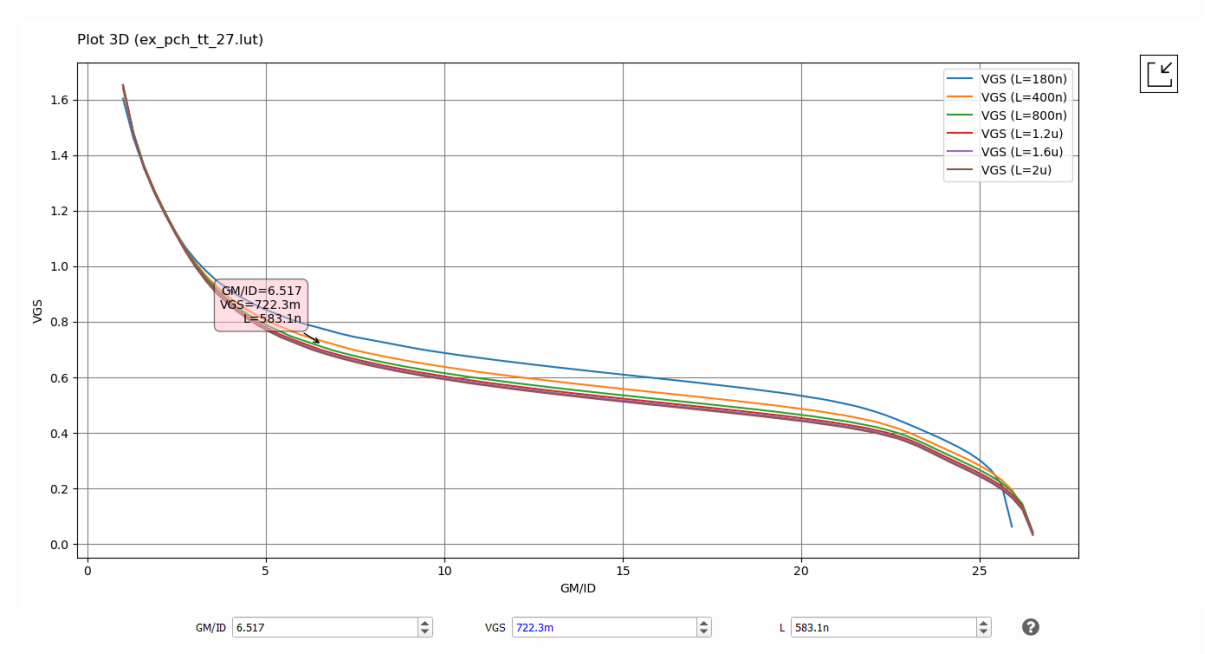
$CMIR_{high} = V_{gs1} - V_{dsat1} - V_{gs3} + V_{DD} \geq 1.5$

Let $V_{dsat1} = V^* = 2 * \frac{I_D}{g_{m1,2}} = 127\ mV$



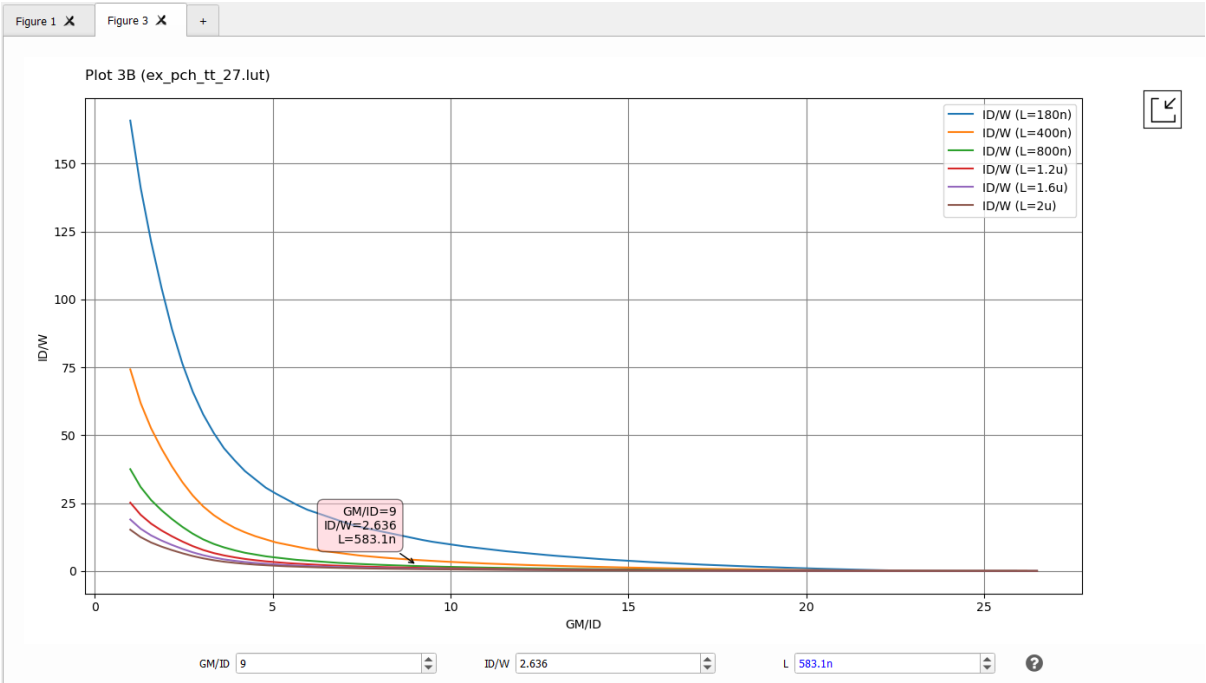
We have all properties for M1,2 so get VGS1=549.7 mV

So from the inequality above I can get $V_{gs3max} = 722.32\ mV$



$$(\frac{g_{m3,4}}{I_D})\_\min = 6.517 \rightarrow take \frac{g_{m3,4}}{I_D} = 9$$

Therefore $g_{m3,4} = 90\ uS$



From this graph we can see

$$\frac{I_D}{W} = 2.636 \rightarrow W_{3,4} = 3.79\ um$$

Design of the tail Current source:

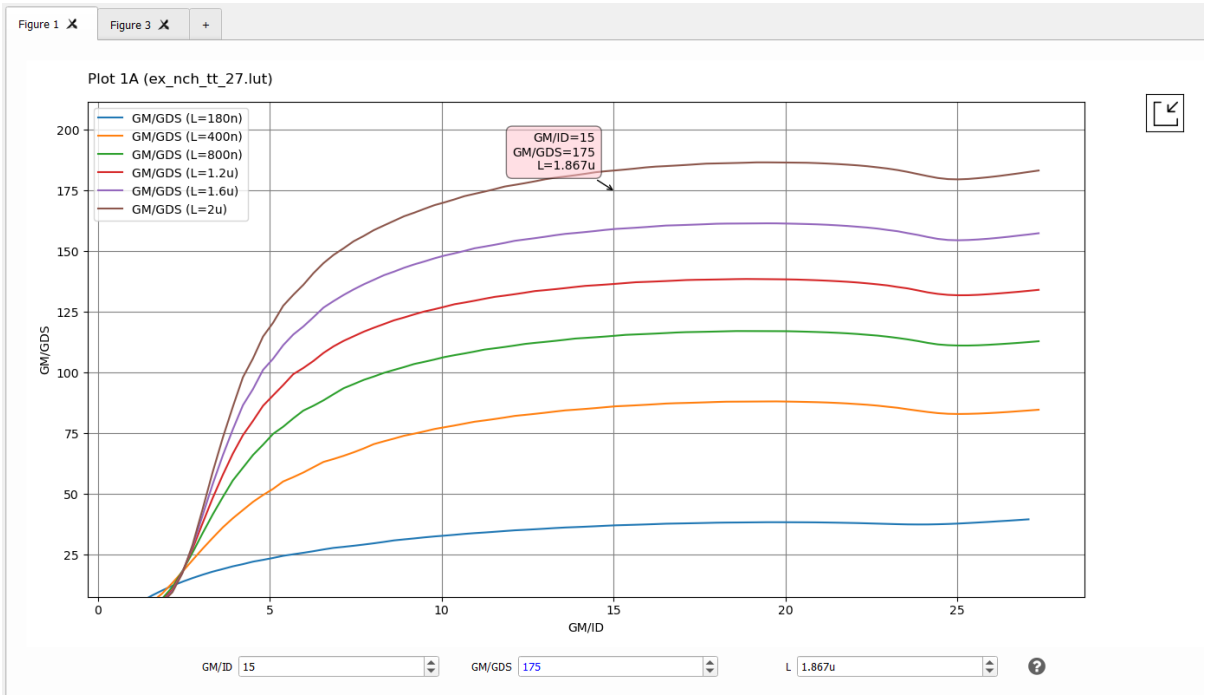
$$CMRR = \frac{A_v}{A_{vcm}} \Longrightarrow A_{vcm} = -40\ db$$

$$A_{vcm} = -\frac{1}{2 * g_{m3,4}R_{ss}} = 0.01$$

$$g_{ds5} \leq 1.8\ uS$$

$$let\ \left(\frac{g_{m5}}{I_D}\right)_5 = 15 \rightarrow g_{m5} = 300uS$$

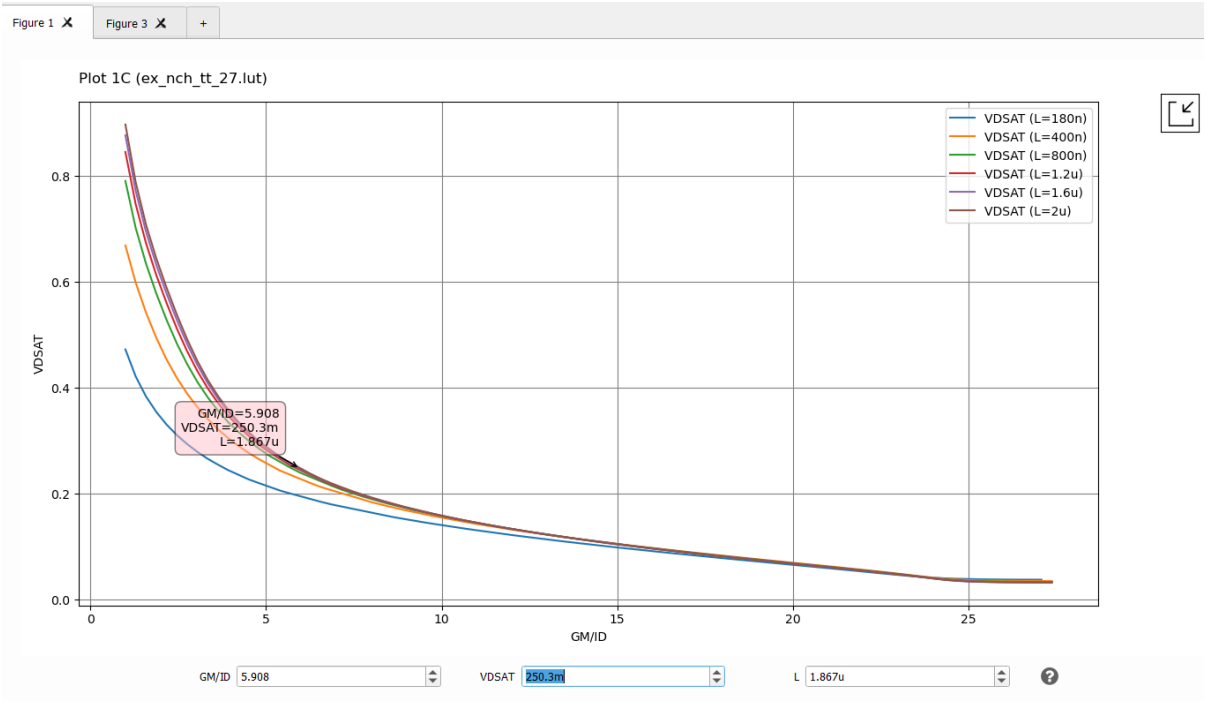
$$\frac{g_m}{g_{ds}} \geq 166.67 \rightarrow take \frac{g_m}{g_{ds}} = 175$$



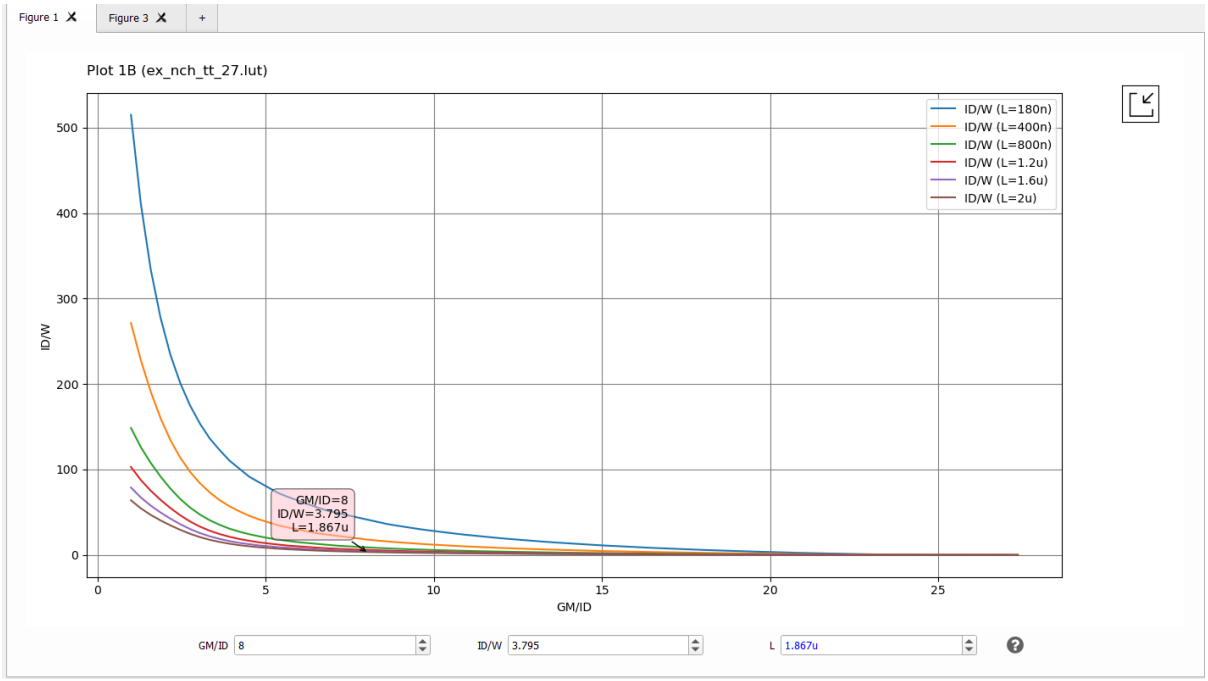
$$L_5 = 1.867\ um$$

$$CMIR_{low} = V_{gs1} + V_{dsat5} \geq 80$$

$$V_{dsat5} \geq 250.3\ mV$$



$$\left(\frac{g_m}{I_D}\right)_{5\text{min}} = 5.9 \rightarrow take \left(\frac{g_m}{I_D}\right)_5 = 8$$



$$\frac{I_D}{W_5} = 3.795 \rightarrow g_{m5} = 160uS$$

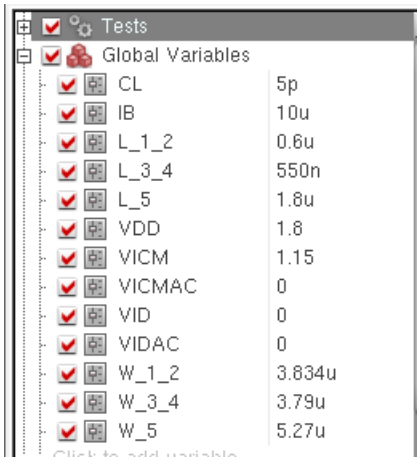
$$W_5 = 5.27\ um$$

Everything for M6 is the same except that $W_6 = 2.635\ um$

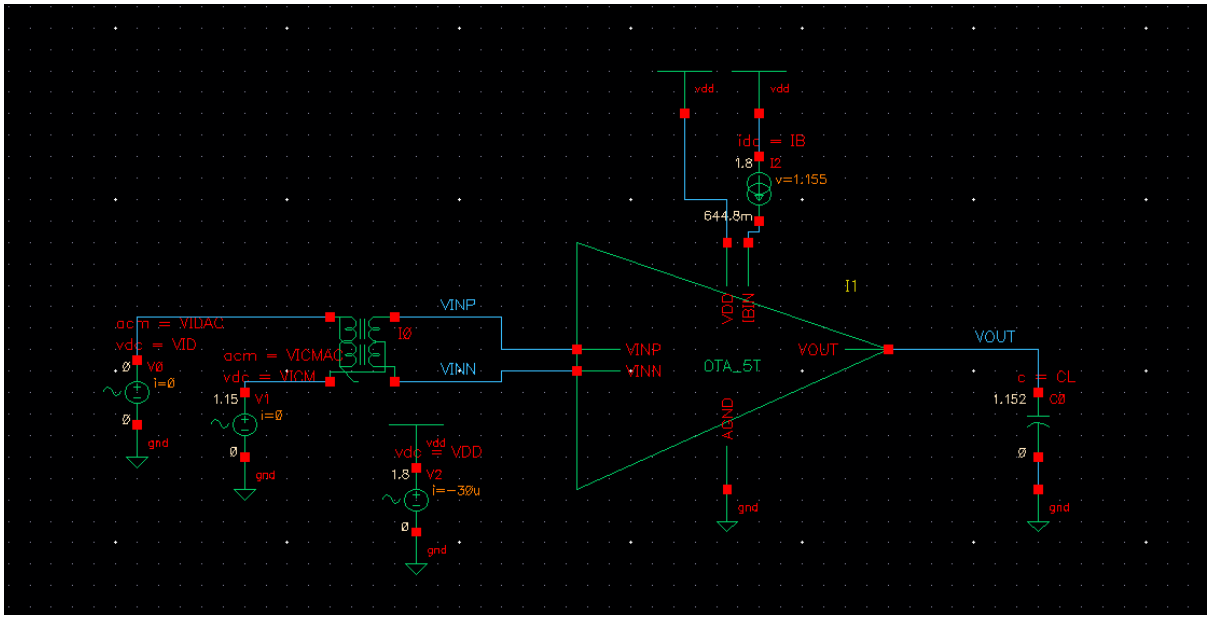
	M1	M2	M3	M4	M5	M6
W	3.834u	3.834u	3.79u	3.79u	5.27u	2.635u
L	0.6112u	0.6112u	583.1m	583.1n	1.867u	1.867u
Gm	157u	157u	90u	90u	160u	80u
Id	10u	10u	10u	10u	20u	10u
Gm/Id	15.7	15.7	9	9	8	8
V*	127m	127m	222.2m	222.2m	0.25	0.25
Vov	117.4m	117.4m	-210.3m	-210.3m	254.8m	255.1m
Vds	558m	558m	-642.2m	-642.2m	599.8m	641m
Vdsat	99m	99m	-175m	-175m	189m	188.9m

PART 3: Open-Loop OTA Simulation

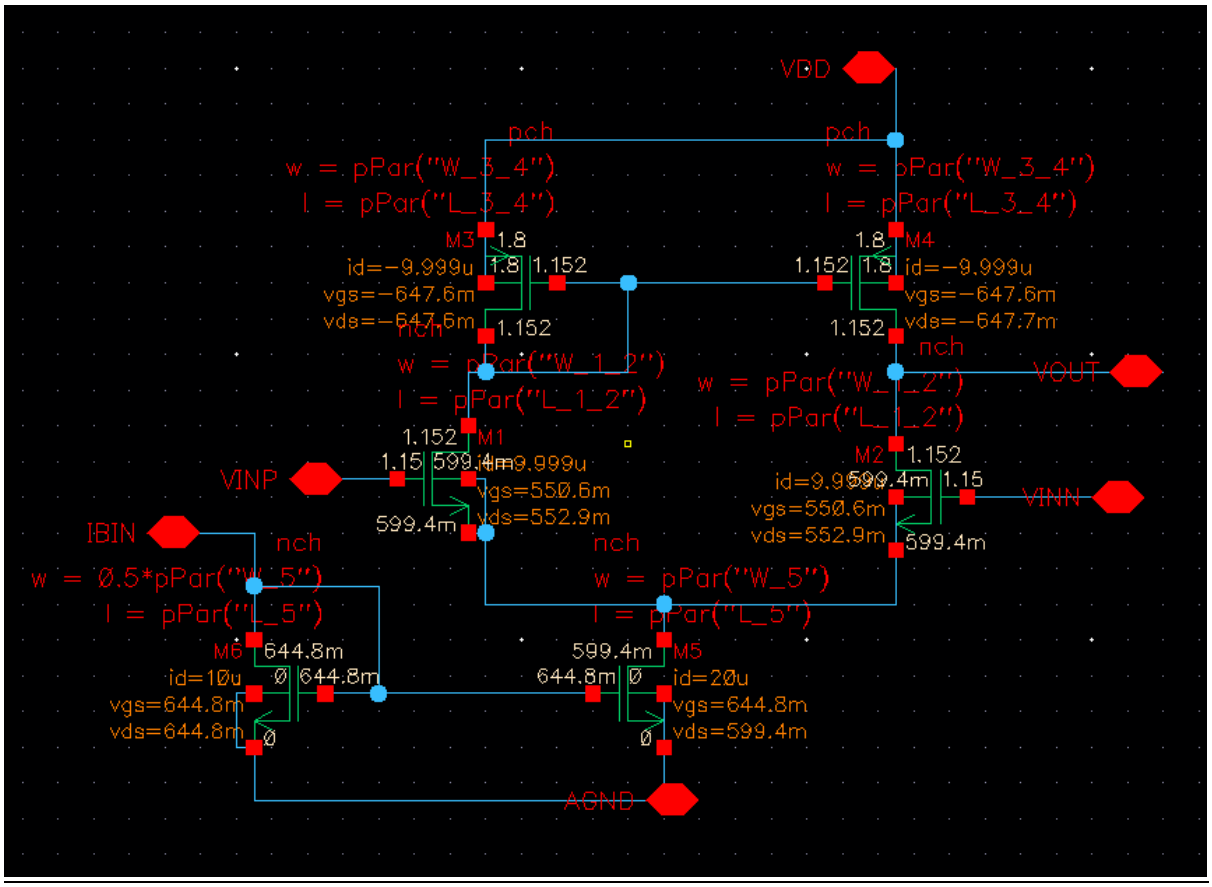
After the simulation I had to do some fine tunings to the design to meet the specs.



Slightly changed some values of the lengths of the mosfets to get better GBW.



1) Schematic of the OTA with DC node voltages clearly annotated



here is a screenshot for the DC operating point which I will need to calculate the hand analysis.

Any hand analysis , I will be using the numbers from the figure below and substitute in the formulas.

	A						
1							
2							
3	Name	/I1/M1	/I1/M2	/I1/M3	/I1/M4	/I1/M5	/I1/M6
4	cgd	-1.808f	-1.808f	-2.488f	-2.488f	-2.441f	-1.213f
5	cgs	-15.83f	-15.83f	-14.72f	-14.72f	-63.74f	-31.81f
6	gds	1.539u	1.539u	1.227u	1.227u	1.091u	532.9n
7	gm	157.4u	157.4u	92.56u	92.56u	162.7u	81.26u
8	gmoverid	15.74	15.74	9.257	9.257	8.13	8.123
9	id	9.999u	9.999u	-9.999u	-9.999u	20.01u	10u
10	region	2	2	2	2	2	2
11	type	0	0	1	1	0	0
12	vds	558m	558m	-642.2m	-642.2m	599.8m	641m
13	vdsat	99.02m	99.02m	-175.7m	-175.7m	189.4m	188.9m
14	vgs	550.2m	550.2m	-642.2m	-642.2m	641m	641m
15	vth	432.6m	432.6m	-431.9m	-431.9m	386.2m	385.9m
16							
17							
18	Region 0 is cutoff.						
19	Region 1 is linear.						
20	Region 2 is saturation .						
21	Region 3 is subthreshold.						
22	Region 4 is breakdown.						
23							
24	Type 0 is nMOS.						
25	Type 1 is pMOS.						

Is the current (and gm) in the input pair exactly equal?

Table Window (XL)

File View Tools Help

Names	I1.M1:gm	I1.M1:id	I1.M2:gm	I1.M2:id
Value	156.4E-6	9.999E-6	156.4E-6	9.999E-6

Yes, they are exactly the same.

What is DC voltage at VOUT? Why?

Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:Lab_07_Gm_ID_ota_tb:1	VDC("/VOUT")	1.152			

The DC voltage of Vout is exactly the same as VICM node Vf (the node of the diode connection). that's because Vout follows the Vf

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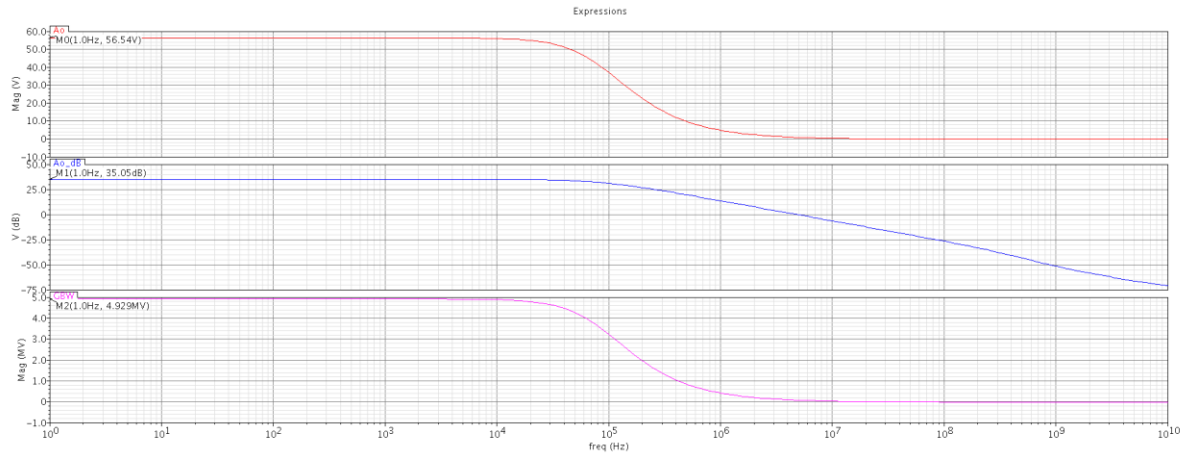
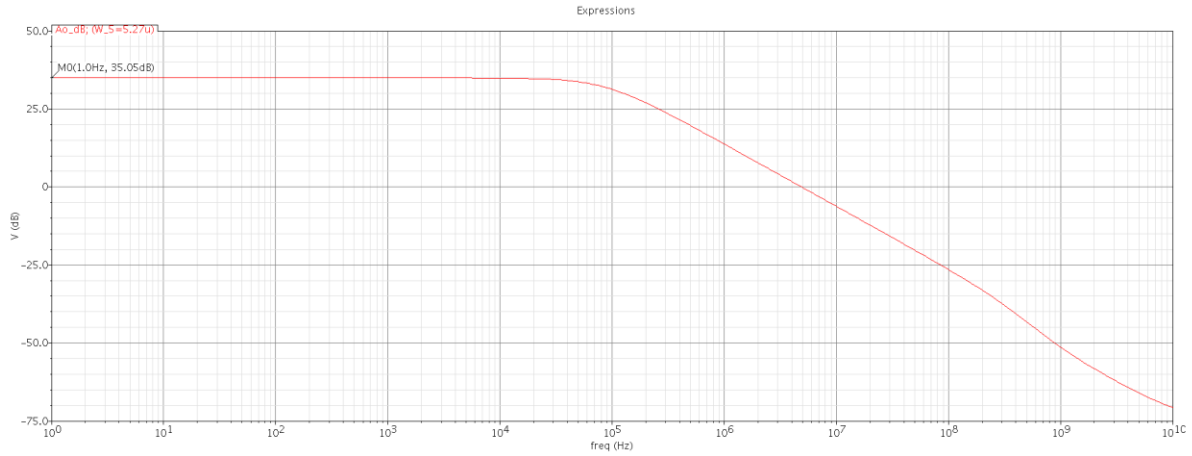
2) Diff small signal ccs:



Plot diff gain (in dB) vs frequency.



Test	Output	Nominal	Spec	Weight	Pass/Fail
AIC_Training:Lab_07_Gm_ID_ota_tb:1	Ao				
AIC_Training:Lab_07_Gm_ID_ota_tb:1	Ao_dB				
AIC_Training:Lab_07_Gm_ID_ota_tb:1	GBW				
AIC_Training:Lab_07_Gm_ID_ota_tb:1	BW	87.18k			
AIC_Training:Lab_07_Gm_ID_ota_tb:1	UGF	4.94M			

Compare simulation results with hand calculations in a table

$$\text{gain} = g_{m1} * (r_{o2} \backslash\backslash r_{o4}) = 157.4\text{u} * (649\text{ k} \backslash\backslash 824\text{ k}) = 56.9$$

$$GBW = gain * BW = \frac{g_{m1}}{2 * pi * C_l} = 5.01\ MHz$$

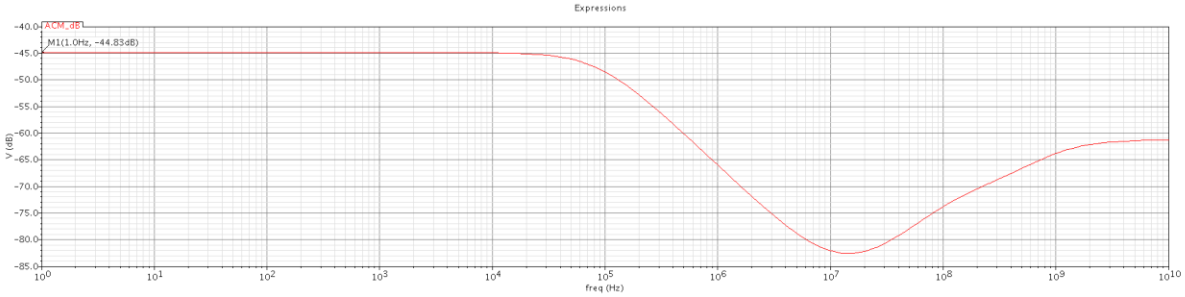
$$BW = \frac{GBW}{gain} = 88.05\ KHz$$

	Simulation	analytical
Gain	56.54	56.9
BW	87.18 KHz	88.05 kHz
GBW	4.929 MHz	5.1 MHz

here the GBW is very close to the design spec but not accurate to about (1.42%) if I want to increase the GBW a little bit to compensate that 1.4% I can slightly increase the lengths of the mosfets which will decrease the area of the mostef which will decrease the parasitic capacitances that will end up increasing the Bandwidth of the circuit thus increase GBW. (It will decrease the gain but I do have a gain margin above the specs to work around).

3) CM small signal ccs:

Plot CM gain in dB vs frequency.



Compare simulation results with hand calculations in a table.

$$A_{VCM} = -\frac{1}{2 * g_{m3,4} * R_{ss}} = -\frac{1}{22 * g_{m3,4} * r_{o5}} = -5.89\,m = -44.59\,dB$$

	Simulation	analytical
AVCM	-44.83 dB	$-44.59\ dB$

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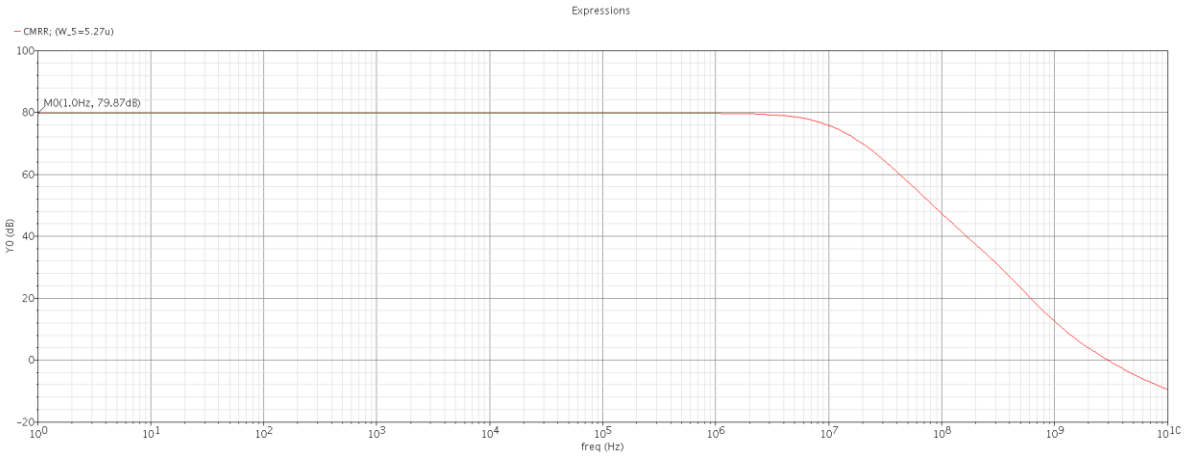
4) CMRR:

Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



Compare simulation results with hand calculations in a table

$$\text{CMRR} = \frac{\text{gain}}{\text{A}_{\text{VCM}}} = \frac{56.9}{-5.89m} = -9660.44 = 79.699\ dB$$

	Simulation	analytical
CMRR	79.87 dB	79.699

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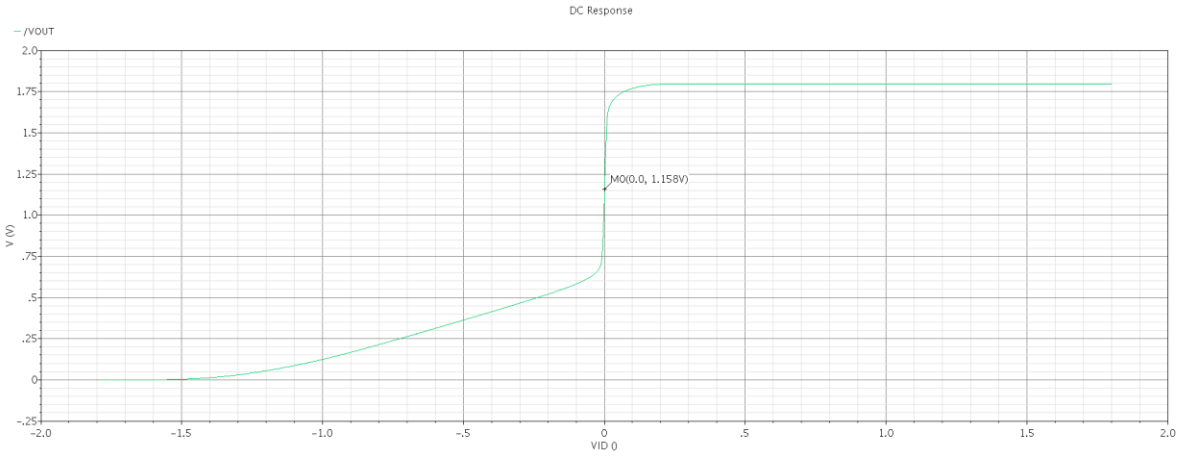
5) Diff large signal ccs:

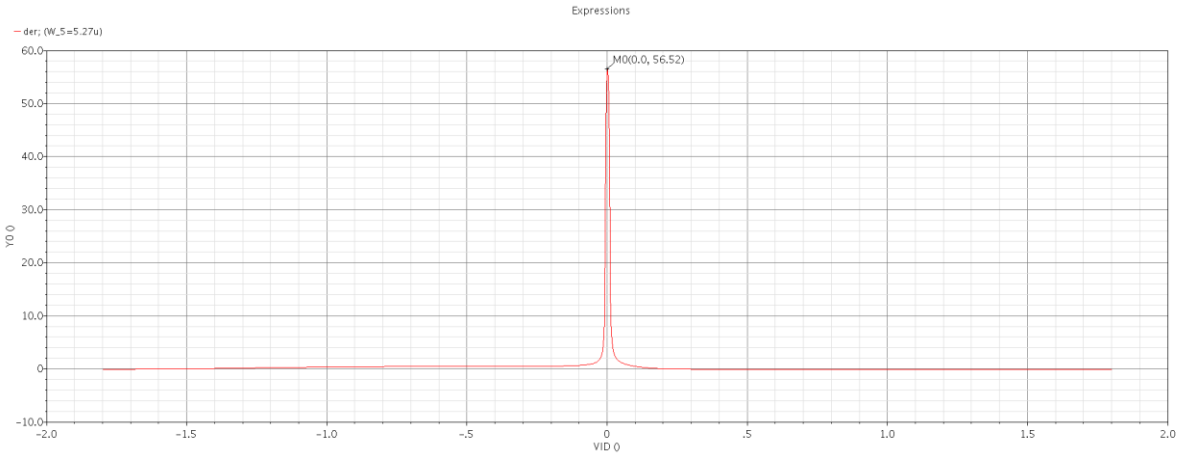
Plot VOUT vs VID.

From the plot, what is the value of Vout at VID = 0? Why?



From the plot, the value of Vout at Vid=0 is equal to VICM because that means that we doesn't inject any differential signal and we are only running a DC simulation with Vdc=VICM so Vf =VICM so it's exactly the same as in requirement (1) that Vout follow Vf.

Plot the derivative of VOUT vs VID. Compare the peak with Avd.

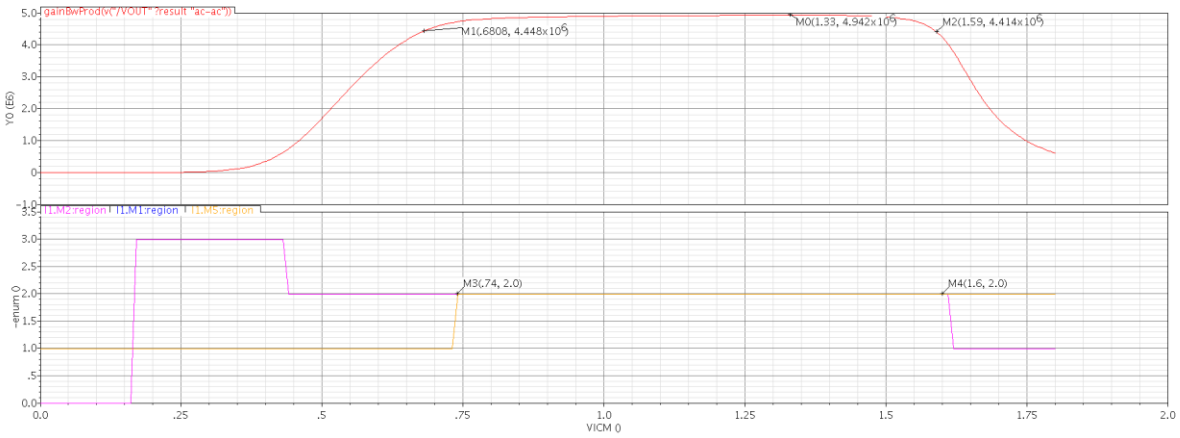


The derivative of Vout vs Vid is the differential gain , the peak of the curve is almost exactly equal to the differential gain Ao of the circuit.

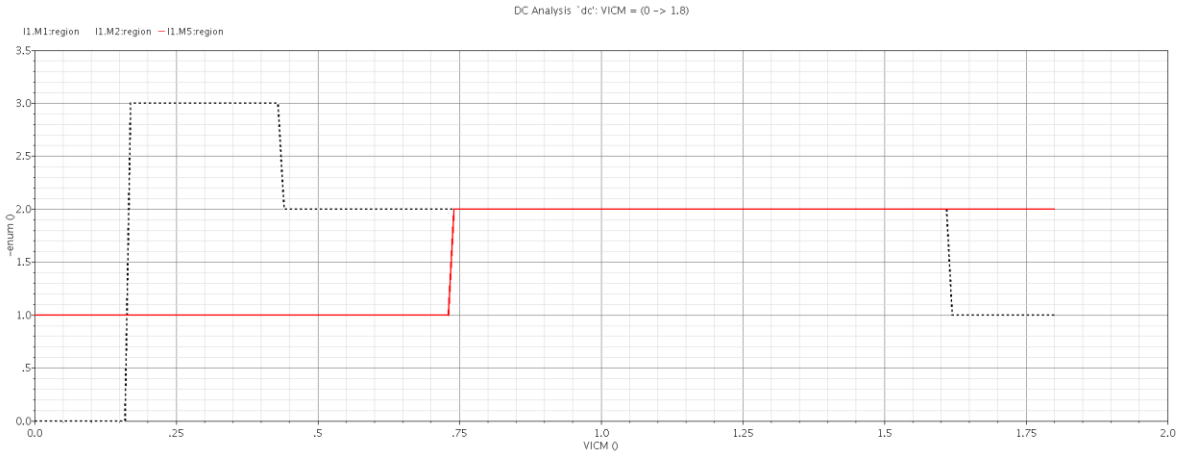
Derivative	Avd
56.52	56.54

6) CM large signal ccs (region vs VICM):

Plot "region" OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown). Plot the results overlaid on the results of the previous method (10% reduction of GBW).



Plot "region" OP parameter vs VICM for the input pair and the tail current source.



Find the CM input range (CMIR). Compare with hand analysis in a table

$$\mathrm{CMIR}_{\mathrm{low}} = V_{gs1} + V_{dsat5} = 739.6\,mV$$

$$CMIR_{high} = V_{gs1} - V_{dsat1} - V_{gs3} + V_{DD} = 1.608\,V$$

Note: CMIR_low means this is the lowest voltage than will maintain all mosfets just on the edge of saturation, so here I have 0.73 V so anything above that will be fine, the specs was to achieve 0.8 so CMIR low is satisfied.

CMIR_high means this is the highest voltage I can apply in the CMIR, the spec to meet was to achieve 1.5 V so here CMIR high is satisfied.

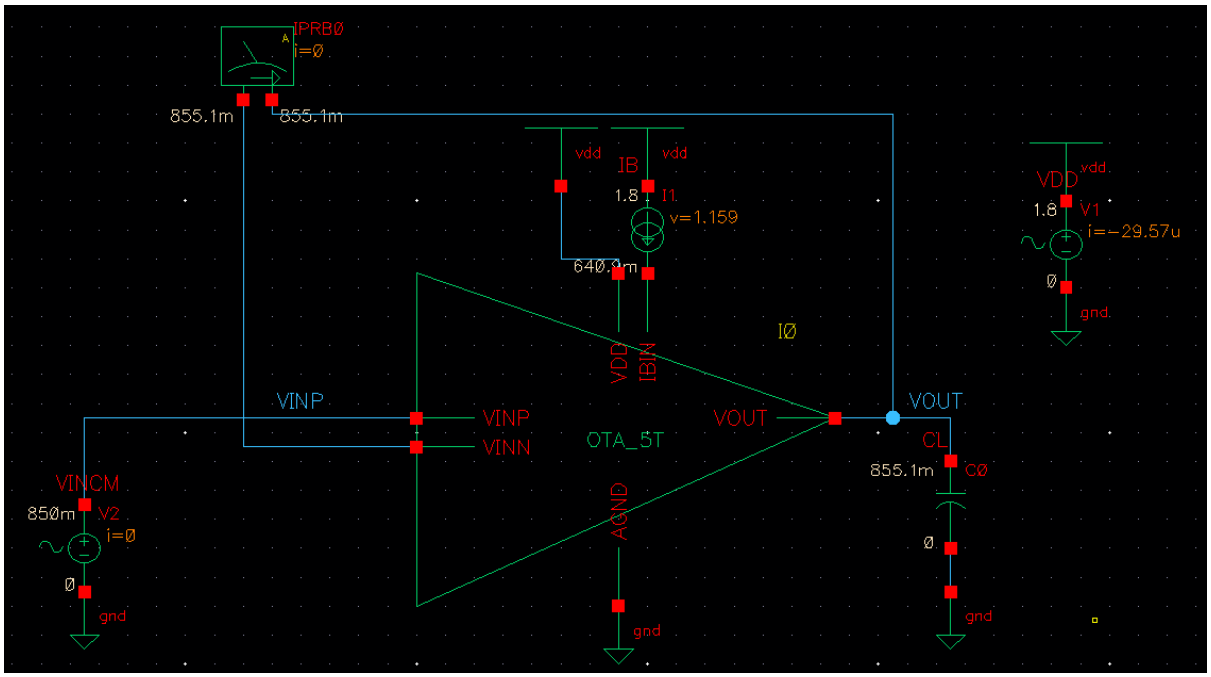
The range where the ota-5T will operate properly is when the mosfets all are in saturation.

M3,4 are diode connected so they are always in saturation.

The common range where M1,2,5 are in saturation is when VICM is between 0.75V to 1.6 V

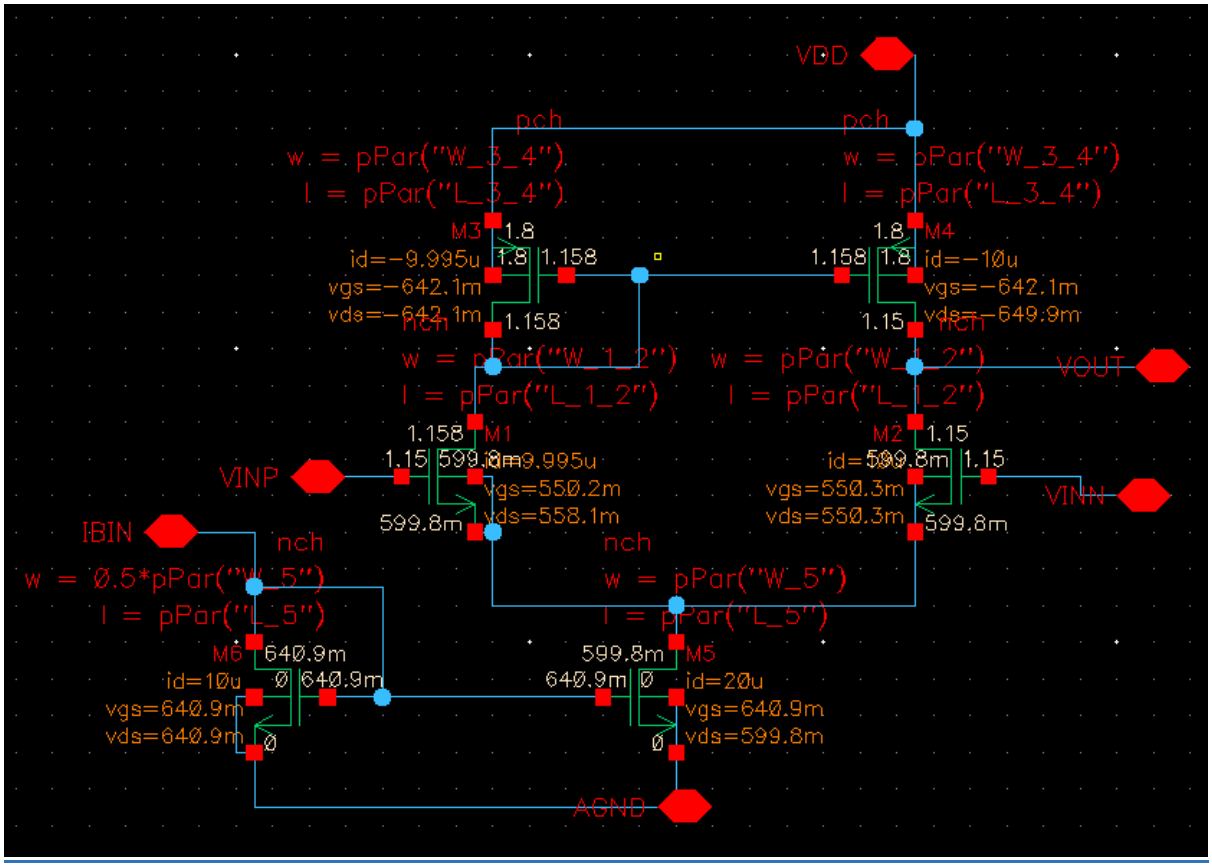
	Simulation-regions	Simulation-GBW	analytical
CMIR_low	0.74	0.68	0.7396
CMIR_high	1.6	1.59	1.608

PART 4: Closed-Loop OTA Simulation



Create a testbench as shown above

1) **Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration. Use VIN = CMIR-low + 50mV.**



Is the current (and gm) in the input pair exactly equal? Why?

	A					
1						
2						
3	Name	/I0/M1	/I0/M2	/I0/M3	/I0/M4	/I0/M5	/I0/M6
4	cgd	-1.808f	-1.808f	-2.488f	-2.488f	-2.441f	-1.213f
5	cgs	-15.83f	-15.83f	-14.72f	-14.72f	-63.74f	-31.81f
6	gds	1.538u	1.544u	1.226u	1.222u	1.091u	532.8n
7	gm	157.3u	157.4u	92.54u	92.61u	162.6u	81.24u
8	gmoverid	15.74	15.74	9.259	9.257	8.132	8.124
9	id	9.995u	10u	-9.995u	-10u	20u	10u
10	region	2	2	2	2	2	2
11	type	0	0	1	1	0	0
12	vds	558.1m	550.3m	-642.1m	-649.9m	599.8m	640.9m
13	vdsat	99m	99.05m	-175.6m	-175.6m	189.4m	188.9m
14	vgs	550.2m	550.3m	-642.1m	-642.1m	640.9m	640.9m
15	vth	432.6m	432.7m	-431.9m	-431.9m	386.2m	385.9m
16							
17							
18	Region 0 is cutoff.						
19	Region 1 is linear.						
20	Region 2 is saturation .						
21	Region 3 is subthreshold.						
22	Region 4 is breakdown.						
23							
24	Type 0 is nMOS.						
25	Type 1 is pMOS.						

NO, the current and gm of the input pair is not exactly equal

The 5T-OTA in a closed-loop unity gain buffer, the output voltage will change a little bit from the input common mode level just to match the input voltage.

The non-zero differential input voltage will cause the imbalance of the two sides of the differential pair. This imbalance is just like the mismatch, it will make a small mismatch in the gm and current of the sides of the differential pair which we will calculate in the next step.

Calculate the mismatch in I_D and gm.

Mismatch in M1: current mismatch= $\frac{10-9.995}{10} * 100 = 0.5\%$

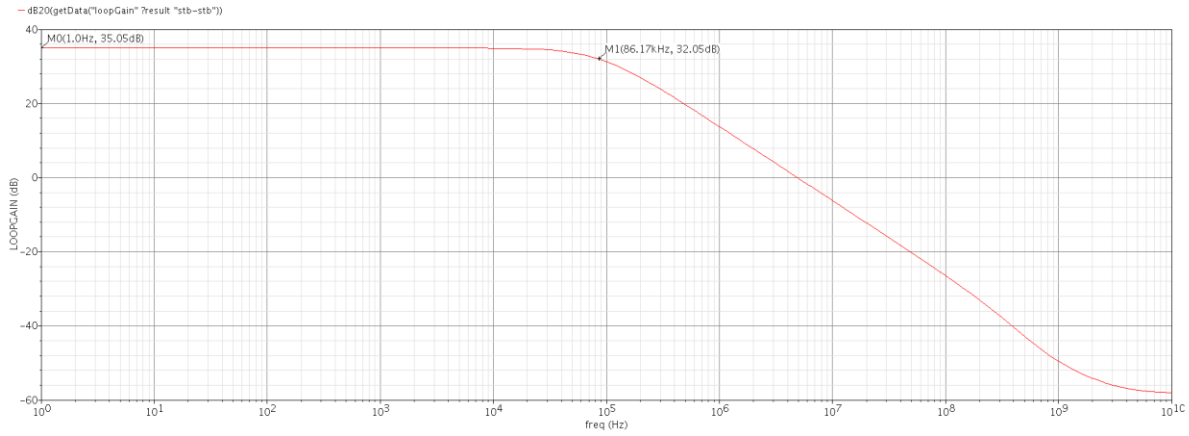
gm mismatch = $\frac{157.4-157.3}{157.4} * 100 = 0.063\%$

Mismatch in M2: current mismatch= $\frac{10-10}{10} * 100 = 0\%$

gm mismatch = $\frac{157.4-157.4}{157.4} * 100 = 0\%$

2) Loop gain:

Plot loop gain in dB and phase vs frequency



Compare DC gain and GBW with those obtained from open-loop simulation. Comment

	Open-loop	Loop gain
DC gain	56.54	56.558
GBW	4.929 MHz	4.873 MHz

The DC gain and GBW is almost the same in the closed loop as the open loop as the feedback network is just a wire (buffer) so the loop gain is equal to B*Aol and B=1 so the results are almost the same.

Compare simulation results with hand calculations in a table.

	Analytical	Simulation
DC gain	56.54	56.558
GBW	4.9429 MHz	4.873 MHz

The loop gain should be exactly equal to the open loop as B=1 ,here in the simulation it's very close to that result but it has a slight change.