# Lab 02
# Common Source Amplifier

## PART 1: Sizing Chart

We would like to design a resistive loaded CS amplifier that meets the specifications below.

- Use DC gain = -6 and ID = 200uA.
- Generic 0.18um model file (VDD = 1.8V)
- Assume we will choose $L=2\mu m$
- Use $W=10\mu m$

The design process involves selecting the sizing of the transistor ($W$ and $L$), the bias point ($V_{GS}$), and the resistive load ($R_D$).

$$|A_v| \approx g_m R_D = (2I_D/V_{ov}) \times R_D = 2V_{RD}/V_{ov}$$

$$V^* = 2I_D g_m \leftrightarrow g_m = 2I_D/V_*$$

$$|A_v| \approx 2V_{RD}/V_*$$

From the above equations we can determine:

$$V_{RD} = \frac{V_{DD}}{2} = 0.9\,V = V_{DS}$$

$$V^* = 0.3\,V$$

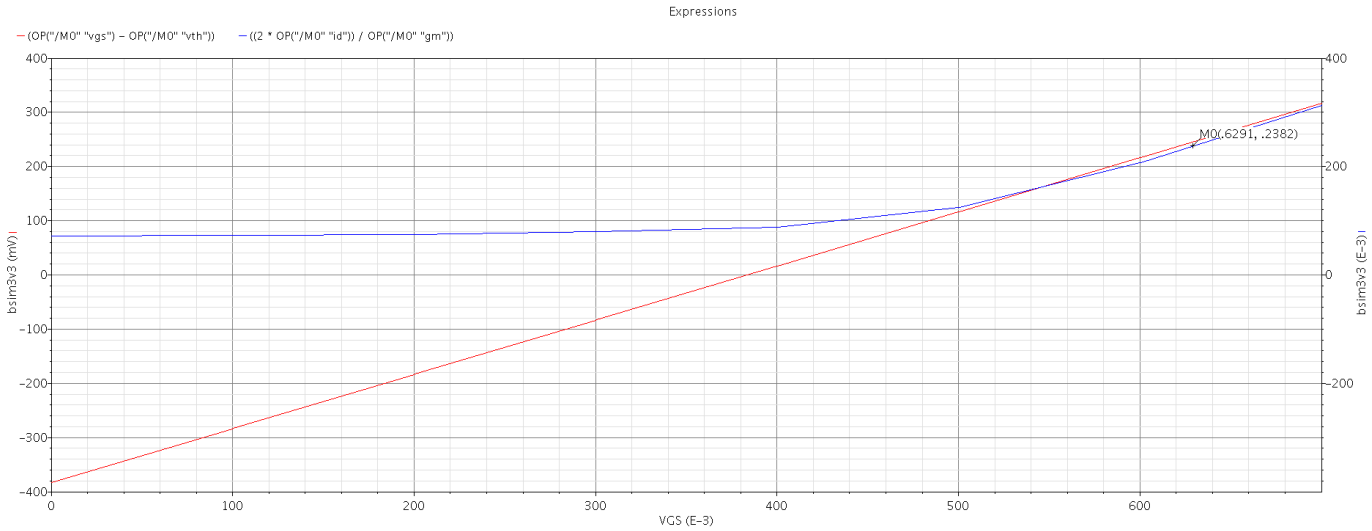
$$g_m = 1.33\,mS$$

$$R_D = 4.5\,k\Omega$$

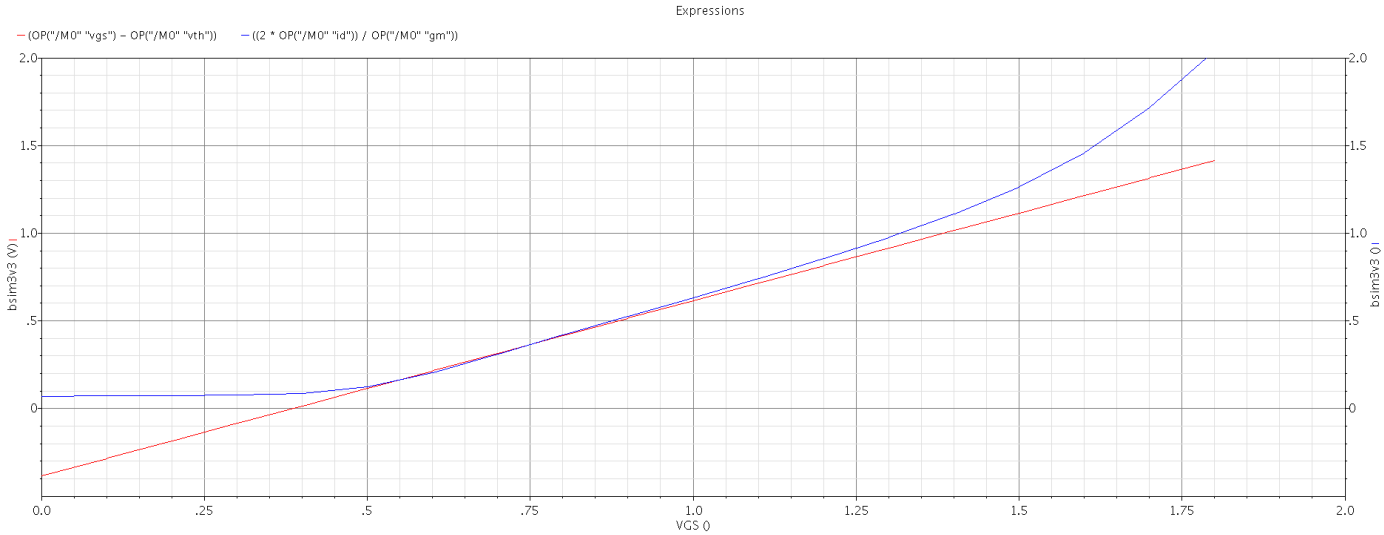
# Then the simulations:

We want to compare $V_*=2I_D/g_m$ and $V_{ov}=V_{GS}-V_{TH}$ by plotting them overlaid:

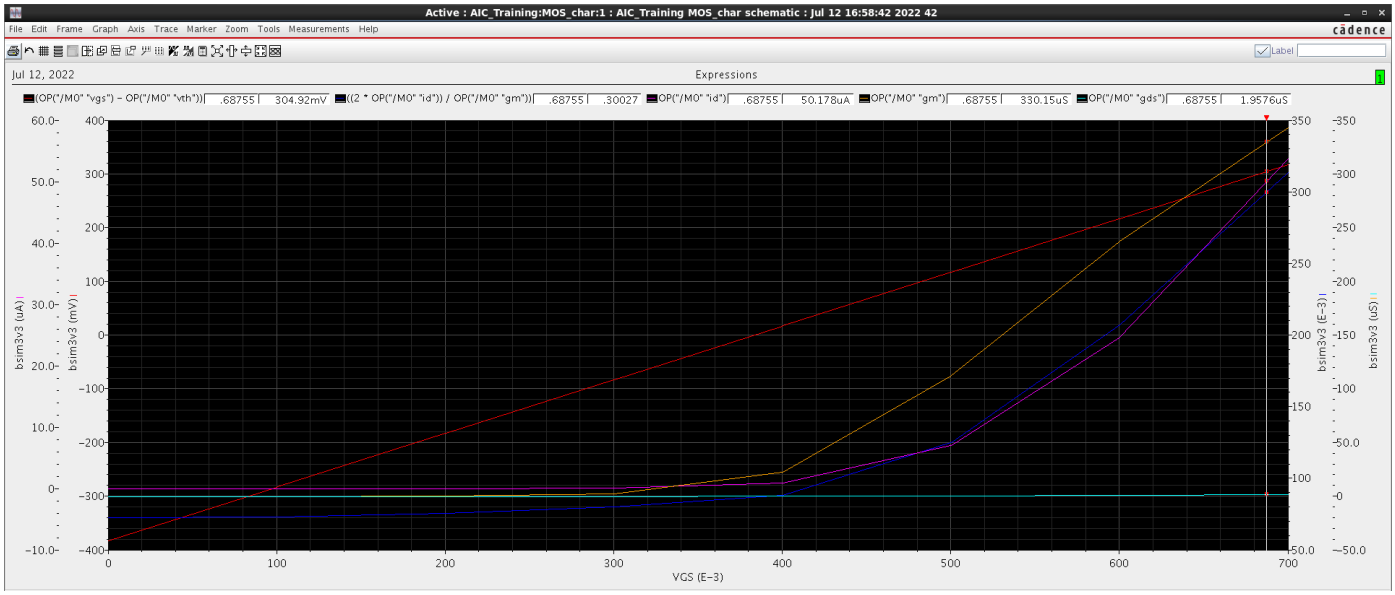
## This graph is at the range of Vgs from 0 to 0.4+Vth




## This graph is at the range of Vgs from 0 to Vdd to show the full regions of inversions.



From this graph we will get out operating point where is V*=0.3 V and hence will find the value of Vgs which corresponds to V*=0.3 V and this will be our operating point.

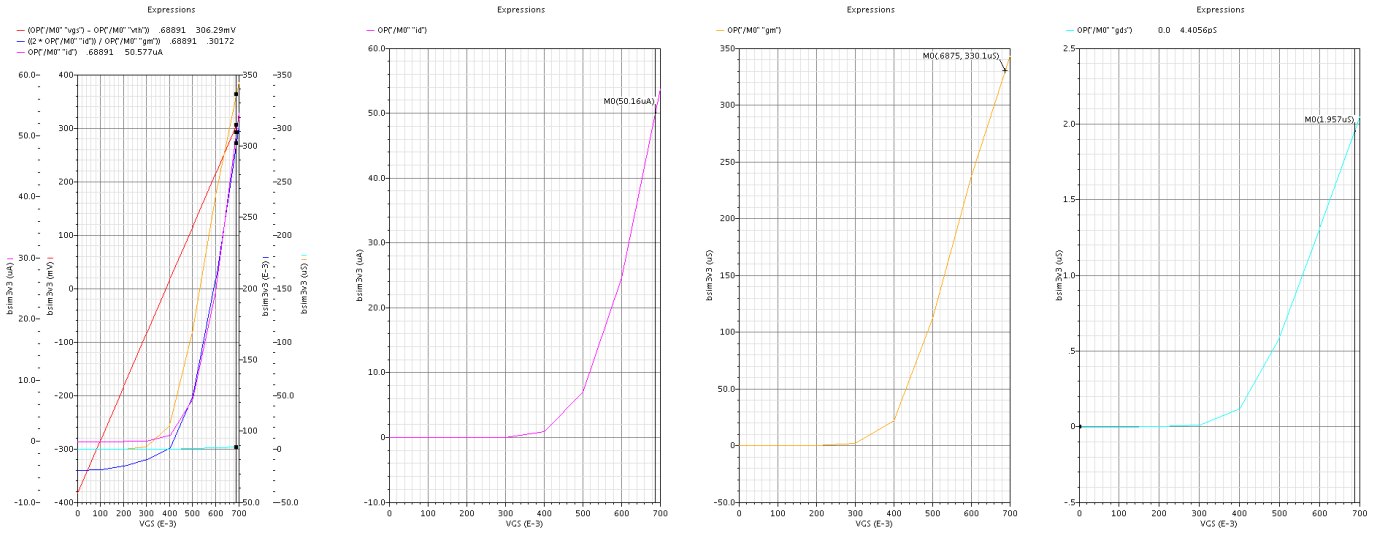



Here we found that at V*=0.3 V

Vgs=687.5 mV

Id=50.178 uA

## Plot $I_D$, $g_m$, and $g_{ds}$ vs $V_{GS}$.



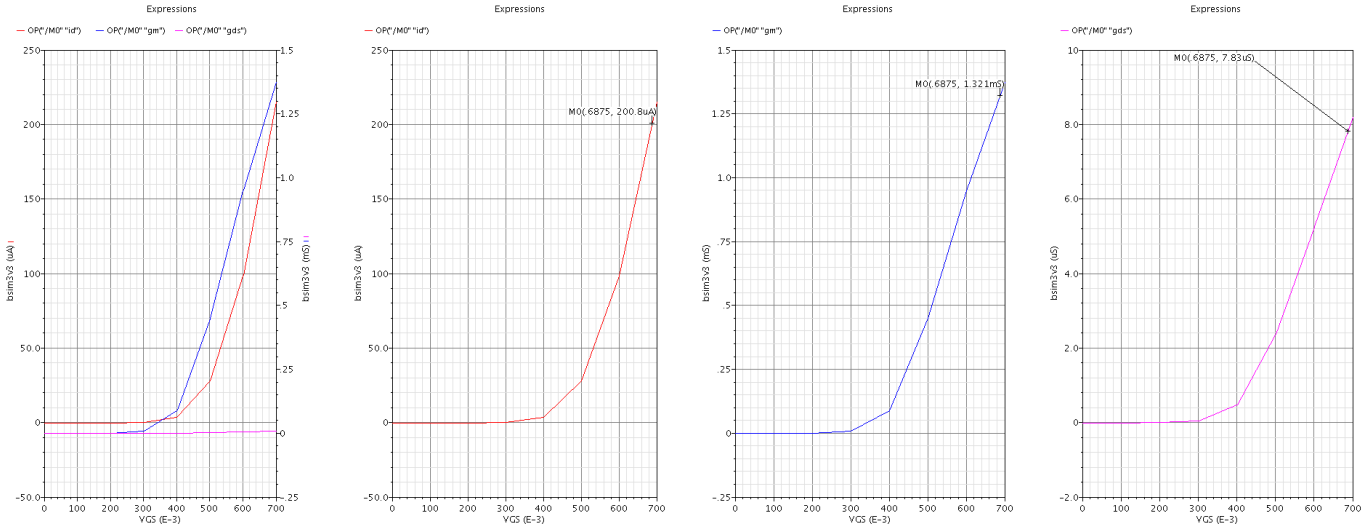

The above graph shows the values of gm,id,gds at the operating points

Now we will use the table to find W and hence find the values of the rest of the parameters that will achieve our design.

| W | Id |
|---|---|
| W=10u M | Id=50.178 uA |
| W_new | Id=200 u A |

Therefore W_new=39.858u M

Hence I can get the rest of the values of gm,gds the same way by substituting in the table above or also can get it by simulating results at W=39.858u M




Here we can find that

gm=1.321 mS // same as calculated analytically using the given formulas

gds=7.83u S

$r_o = 1/g_{ds} = 127.71\ \text{k}\Omega$

Now we can double check the gain to guarantee that our design is correct.

$A_v = -g_m(R_D || r_o)$

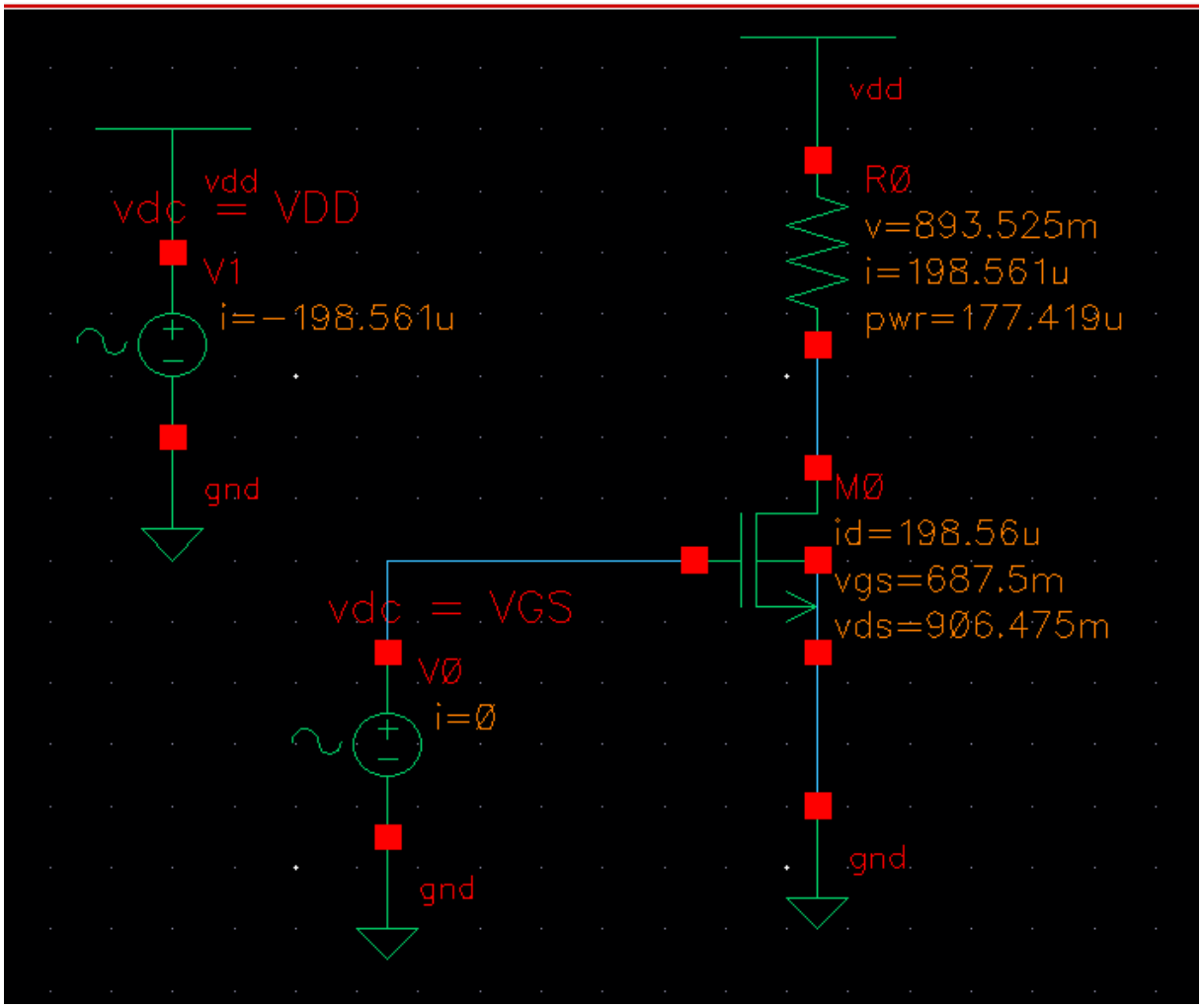
So $A_v = -5.9445$ $if\ not\ taking\ r_o\ into\ consideration$

And $A_v = -5.742$ with $taking\ r_o$ into consideration

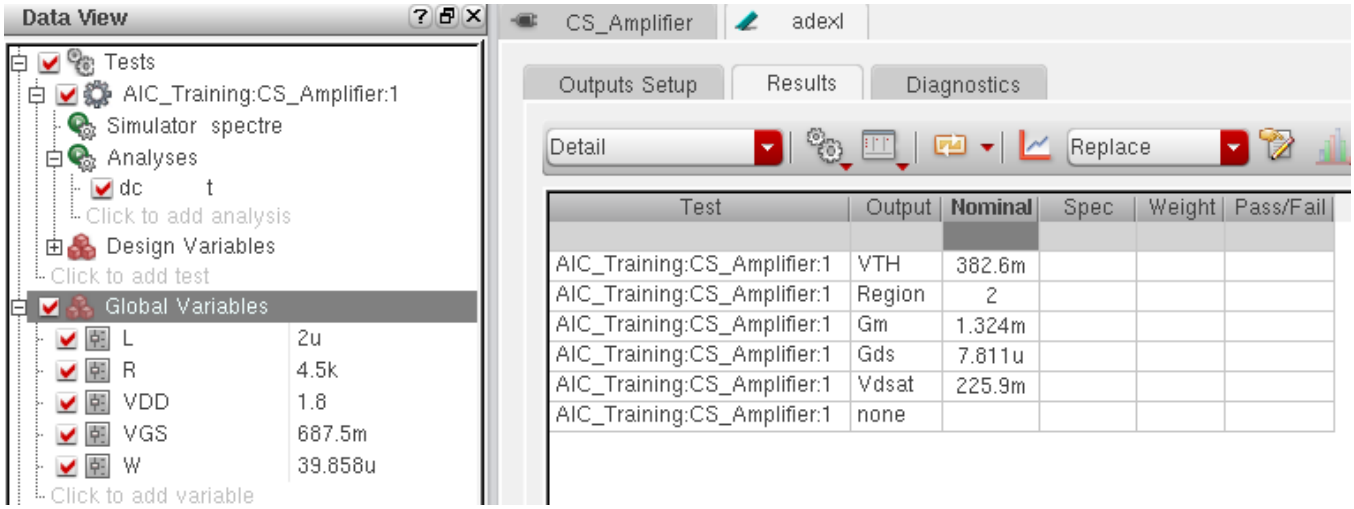
# PART 2: CS Amplifier

## OP and AC Analysis:

**Simulate the DC OP. Report a snapshot for the key operating point (OP) parameters.**




And here are the rest of the operating points and the values used for the simulation.




As seen from the above shots the Values of All the parameters agree with what we got in part 1

**Compare $r_o$ and $R_D$. Is the assumption of ignoring $r_o$ justified in this case? Do you expect the error to remain the same if we use min $L$?**

Gds=7.811 uS

$r_o = 128.02\ k\Omega$

$R_D = 4.5\ k\Omega$

So, the assumption of ignoring $r_o$ is justified as $R_D$ is much smaller than $r_o$ so it will be neglected compared to it in the parallel combination of the gain.

If we use min L, the assumption may not be justified as there are secondary effects that will decrease the output resistance and also that the output resistance is directly proportional to the output resistance so as the length decrease the output resistance decrease so it might reach a point where it won't be negligible compared to Rd.

## Calculate the intrinsic gain of the transistor.

$$\mathrm{A_{intrinsic}} = g_m * r_o = 169.49$$

**Calculate the amplifier gain analytically. What is the relation (≪,<,≈,>,≫) between the amplifier gain and the intrinsic gain?**

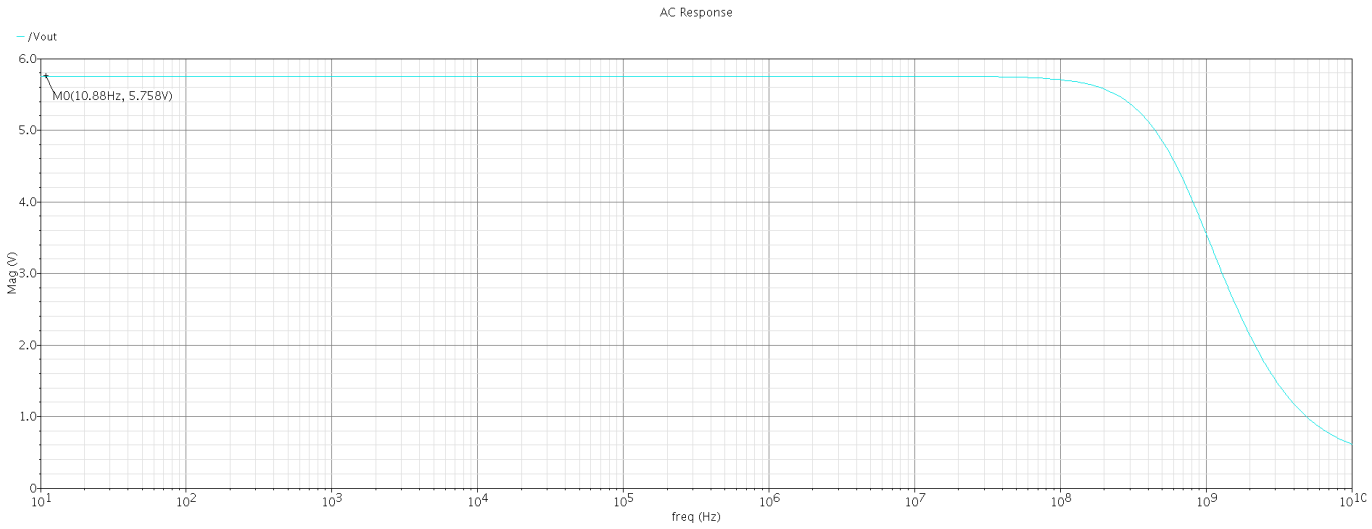
$A_o = g_m * (R_d // r_o) = 5.96$

$A_o \ll \mathrm{A_{intrinsic}}$

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| AIC_Training:CS_Amplifier:1 | VTH | 382.6m | | | |
| AIC_Training:CS_Amplifier:1 | Gm | 1.324m | | | |
| AIC_Training:CS_Amplifier:1 | Region | 2 | | | |
| AIC_Training:CS_Amplifier:1 | Gds | 7.811u | | | |
| AIC_Training:CS_Amplifier:1 | Vdsat | 225.9m | | | |
| AIC_Training:CS_Amplifier:1 | Intrinsic gain | 169.6 | | | |
| AIC_Training:CS_Amplifier:1 | Ao | 5.96 | | | |

and these are the values from cadence

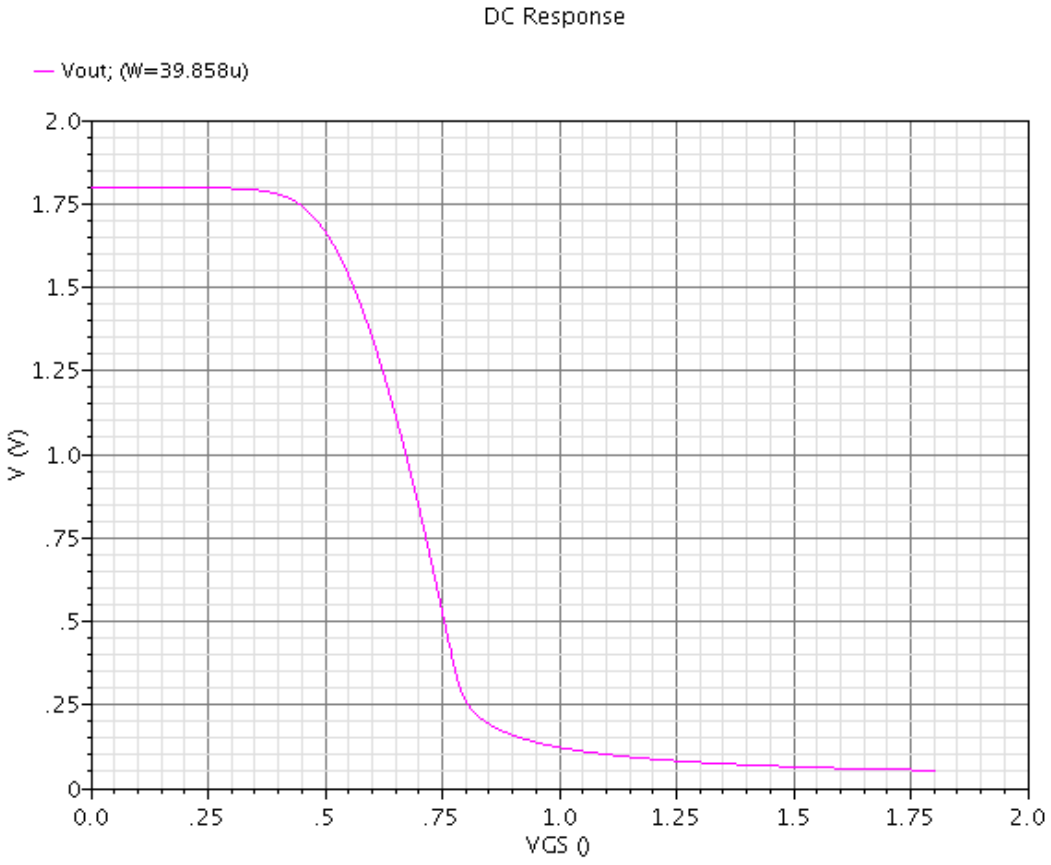
**Run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec**




## Gain Non-Linearity:

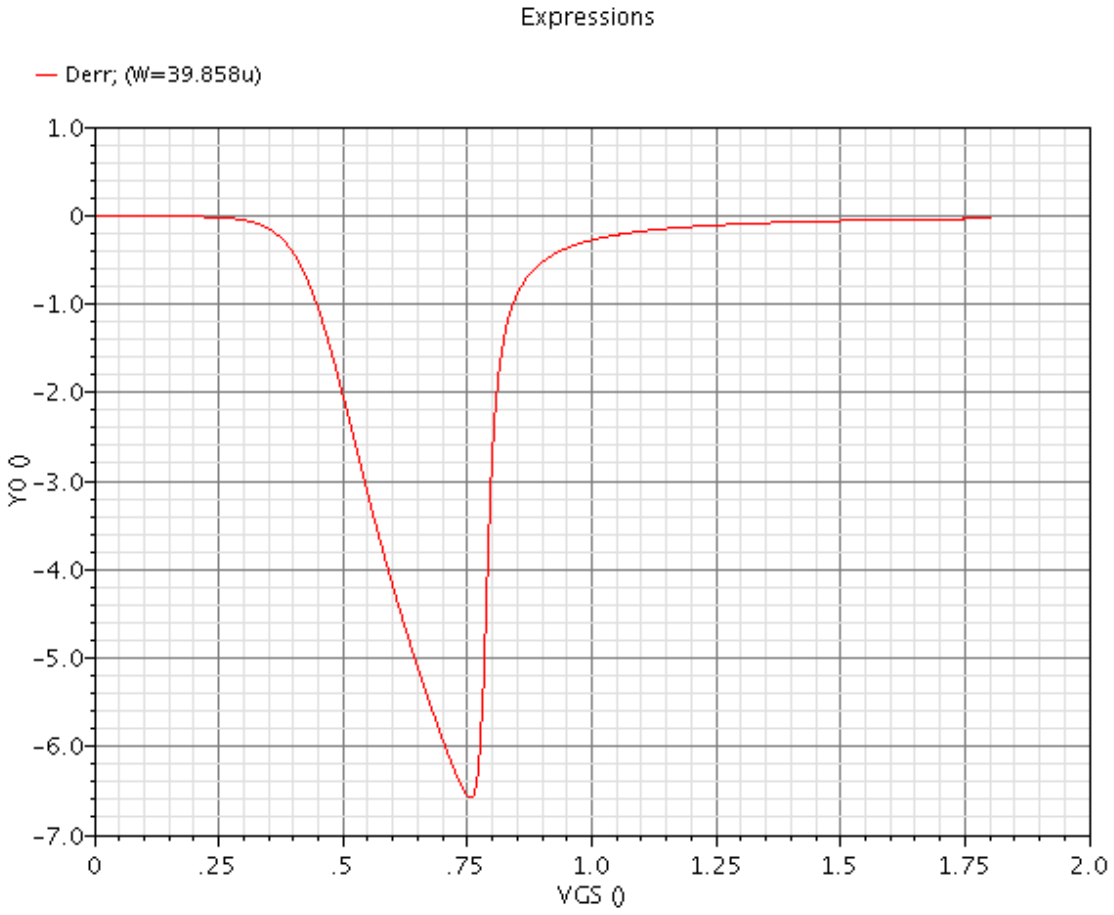
Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to $V_{DD}$ with 2mV step

**Report VOUT vs VIN. Is the relation linear? Why?**



The relation is quadratic because of the quadratic relation between $I_D$ and $V_{GS}$. So it's a non-linear relation.

**Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?**

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The gain is linear while $V_{DS} > V_{ov}$ i.e. (saturation region) because that,
$V_{out} = V_{DD} - I_D R_D$
If we differentiate $V_{out}$ W.R.T $V_{GS}$ the relation will be a linear relation.
But, when $V_{DS} < V_{ov}$, the relation between Vout and VGS will be linear and if we differentiate a linear relation, it will give a constant.
Therefore, the gain is dependent on the input (**non-linear gain)**

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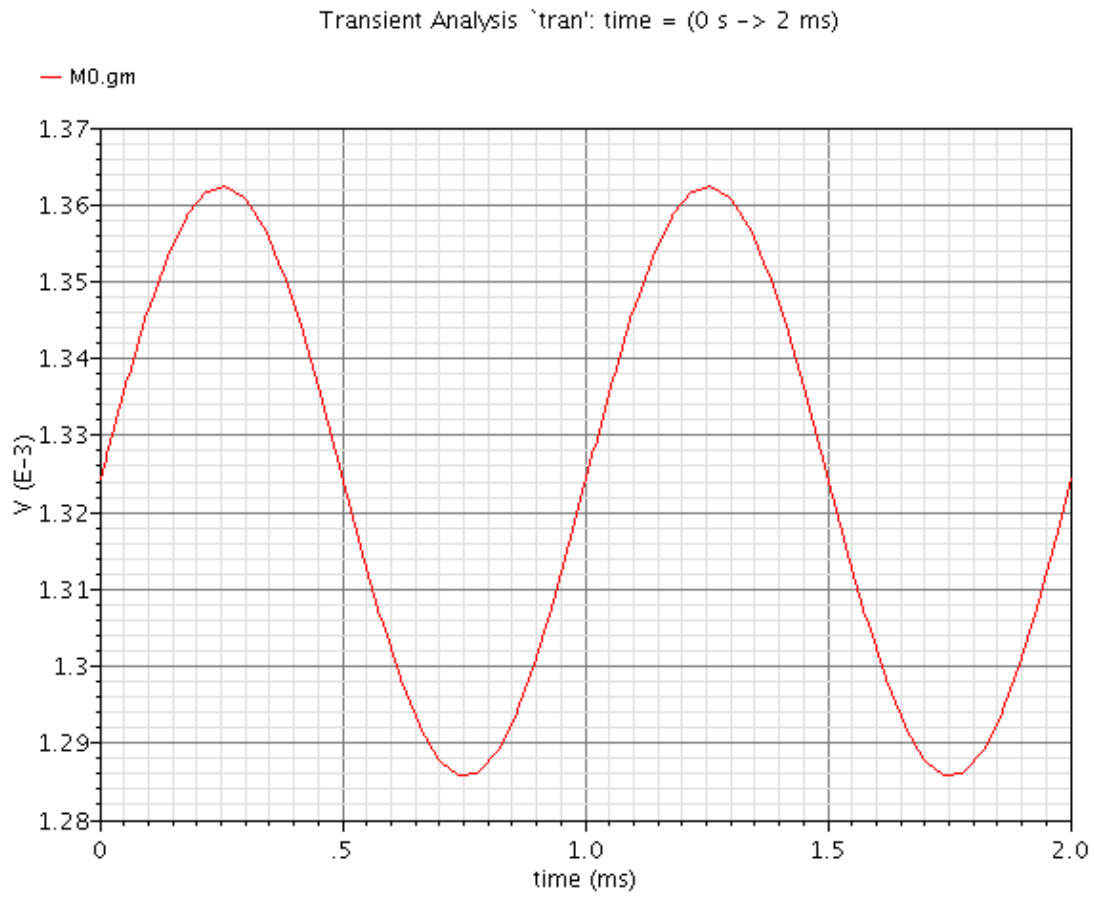
Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage)

**Run transient simulation for 2ms. Plot gm vs time.**

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**Does gm vary with the input signal? What does that mean?**

Yes, gm changes with the input signal, which means that gm is linearly proportional to the input signal VGS.

## Is this amplifier linear?

This amplifier is linear, although we used a nonlinear element in our design the amplifier acts as a linear device, but this linearity is only valid if the signal is "small".

So, we can say that the amplifier is linear as long as we keep the transistor biased in the saturation region and the input signal << $2Vov$