Analog IC Design
Lab 09 (Mini Project 01)
Two-Stage Miller OTA

PART 2: OTA Design

The OTA specs:

Technology	180 nm
Supply voltage	1.8 V
Static gain error	<= 0.05%
CMRR @ DC	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70 degrees
OTA current consumption	<= 60uA
CMIR – high	>= 1V
CMIR – low	<= 0.2V
Output swing	0.2 – 1.6V
Load	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns
Slew rate (SR)	**5** V/us

Use an ideal external 10uA DC current source in your test bench.

Report the following:

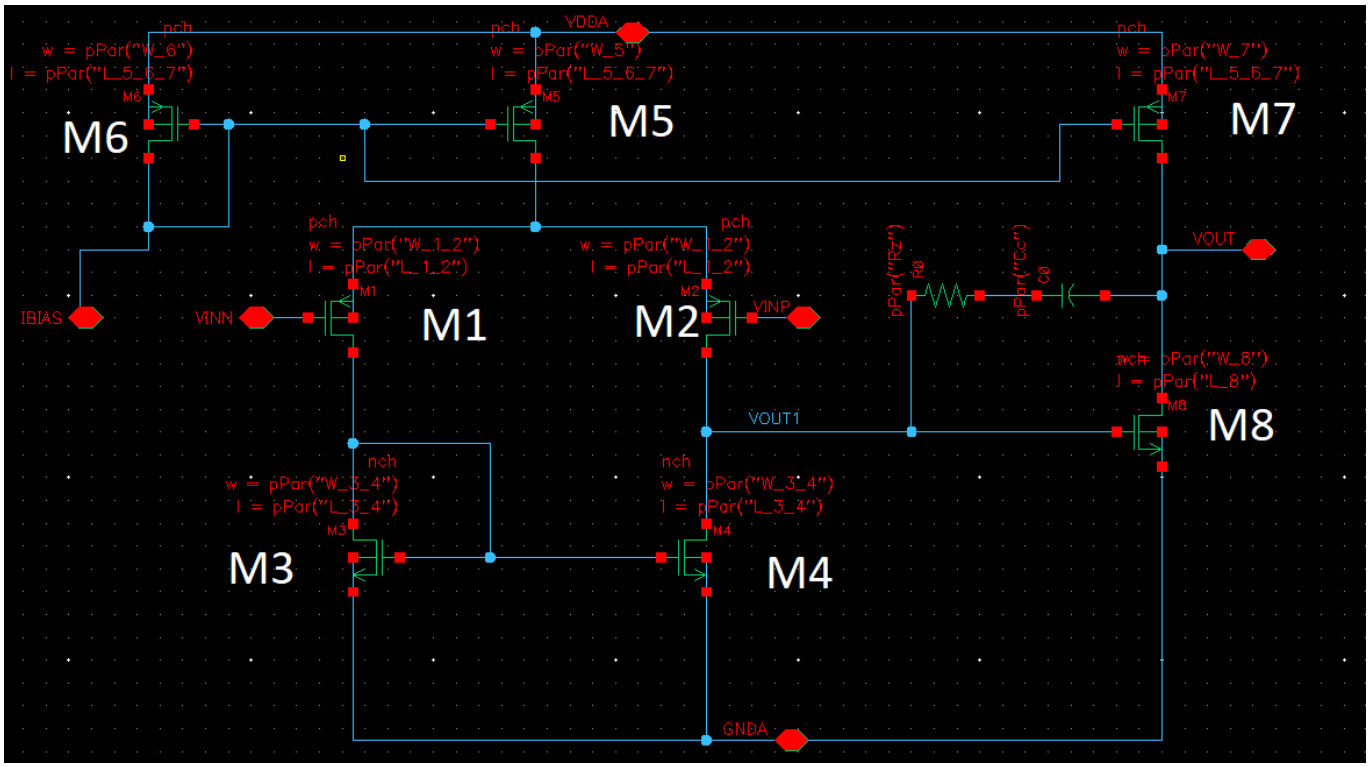
1) Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage.

Since that the CMIR is closer to the ground rail, therefore I will use a PMOS input stage for the first stage.

Since I used a PMOS input stage for the first stage, the bias current will be a sourcing current source from upwards. Note that this bias current will also be biasing the second stage.

So, the second stage input transistor will be a NMOS transistor to give me a common source stage and amplify the gain.

The following figure will show the design I implemented and the numbering or each MOSFET that will be very important because from now on I will be calling them by their numbers.



Suggested Design Procedure (you may create your own!):

1) Use a single 10uA DC current source and a single DC voltage source in your test bench. Design your own current mirrors and bias circuitry.

Here I will use a dc ideal current source then mirror the current for the first stage and the second stage with different widths for the mirror MOSFETS.

2) A reasonable starting point for Cc is $0.5C_L$. You may refine this choice by doing sweeps in simulation.

$$C_c = 0.5 * C_L = 2.5\ \text{pF}$$

3) Calculate the unity gain frequency (UGF) from the rise time requirement (t_{rise}=2.2τ). Hence, calculate $g_{m1,2}$.

$$t_{rise} = 2.2 * \tau \rightarrow \tau = \frac{70\text{n}}{2.2} = 31.81n$$

$$UGF = \frac{1}{\tau} = 31.428 \text{ Mrad/sec}$$

$$UGF = \frac{g_{m1,2}}{C_c} \qquad \rightarrow \qquad \boldsymbol{g_{m1,2} = 78.57\ uS}$$

4) From the SR requirement, calculate the current required in the first stage (I_{B1}): $SR=I_{B1}C_C$. Given the total current budget, calculate the current of the second stage.

$$SR = \frac{I_{B1}}{C_c} \qquad \rightarrow \qquad I_{B1} = 12.5\ uA$$

I_{B1} will be the bias current for the first stage and it will be divided equally between the two branches of the OTA.

$$I_{B2} = I_{Total} - I_{B1} = 47.5\ uA$$

5) Calculate gm/ID of the first stage.

$$\left(\frac{g_m}{I_D}\right)_{1,2} = \left(\frac{78.57u}{\frac{12.5u}{2}}\right) = 12.57$$

Take some margin in $\frac{g_m}{I_D}$ $\boldsymbol{so}$ $\boldsymbol{\left(\frac{g_m}{I_D}\right)_{1,2} = 15 \rightarrow g_{m1,2} = 93.75uS}$

6) Show that the closed-loop gain for a buffer is $A_{vCL}\approx 1-\frac{1}{A_{vOL}}$, where A_{vOL} is the open-loop gain. Given A_{vCL} gain error spec ($\%error=\left|\frac{actual-ideal}{ideal}\right|\times 100$), calculate the required DC gain in dB.

$$error = \frac{0.05}{100} = \left(\frac{1 - \frac{1}{A_{ol}} - 1}{1}\right) \rightarrow \qquad A_{ol} = 2000 = 66.02\ dB$$

$$A_{vcl} = 1 - \frac{1}{A_{ol}} = 0.9995 = -4.344 * 10^{-3}\ dB$$

7) Assign larger gain for the first stage (why?). Do not split the gain equally between the two stages. You may assume the first stage gain is twice that of the second stage (6dB difference).

$$A_{ol} = Gain_1 * Gain_2$$

$$let\ Gain_1 = 2 * Gain_2$$

$$A_{ol\,dB} = X + 6 + X$$

$$Gain_1 = 36\ dB = \ 63.09$$

$$Gain_2 = 30\ dB = 31.623$$

8) Given the 1st stage gain, calculate L (channel length) of the 1st stage input. You may assume input and load have the same gds.

$$Gain_1 = \frac{g_{m1,2}}{2 * g_{ds2,4}} \qquad \rightarrow \qquad \frac{g_{m1,2}}{g_{ds2,4}} = 126.18$$

Take some margin in the intrinsic gain so

$$\frac{g_{m1,2}}{g_{ds2,4}} = 130 \rightarrow \quad g_{ds2,4} = 721.15\ nS$$

By using the ADT sizing assistant

$$L_{1,2} = 828.2\ nm \quad W_{1,2} = 11.477\ um$$

Now M1 & M2 are fully specified, here are some values I got from ADT that will help me further more in the design.

$$V_{gs1,2} = 534.38\ mV\ , V_{dsat1,2} = 108.02\ mV$$

9) Given gds/ID of the first stage current mirror load, select L. Note that gds/ID slightly increases with gm/ID, which is not known yet. To get an estimate for L, you may ignore this dependence and assume a relatively large gm/ID for the load at this point (e.g., gm/ID = 15).

$$let\ \left(\frac{g_m}{I_D}\right)_{3,4} = 15 \rightarrow I_D\ is\ the\ current\ in\ the\ branch = \frac{I_{B1}}{2} = 6.25\ uA$$

$$g_{m3,4} = 93.75\ uS\ \rightarrow \frac{g_{m3,4}}{g_{ds3,4}} = 130$$

Take a 5% margin in the intrinsic gain so I will take $\frac{g_{m3,4}}{g_{ds3,4}} = 138$

By using ADT sizing assistant $L_{3,4} = 1.2276\ um$

10) Given the PM spec, calculate gm/ID of the second stage input transistor (Hint: assume $\omega_{p2}=4\omega_u$).

$$PM = 70\ degree\ , w_u = UGF = 31.428\ M\ rad/sec$$

$$w_{p2} = 4 * w_u = 125.712\ M\ rad/sec$$

$$\frac{G_{m2}}{C_L} = \frac{4 * G_{m1}}{C_c}$$

$$\frac{G_{m2}}{G_{m1}} = 4 * 2 = 8$$

$$G_{m2} = g_{m8} = 8 * g_{m1,2} = 750\ uS$$

$$\left(\frac{g_m}{I_D}\right)_8 = 15.789$$

This is the gm/Id of the second stage input transistor.

11) Given the CMIR-high and Swing-high specs, calculate max vdsat for tail current source and output load. Take the lower value and assume V*= vdsat. Note that always V* > vdsat; thus, this assumption already adds some margin to make sure they are driven a little more into saturation. Now you have gm/ID of these two transistors. Note that these two transistors are identical (they form a current mirror; thus, they have same L and same gm/ID) except for the current (and width).

All of the top 3 transistors which will bias the stages will have the same (V*) same gm/Id and same L

The only difference will be in their widths that will set the mirroring ratio to flow the desired current in each branch from the 10 uA reference current.

So here we want to get a condition on V* (Vdsat) but with some margin that will satisfy all the specs for the 3 transistors.

The first condition from the CMIR- high:

$$CMIR_{high} = V_{DD} - V_{gs1} - V_{dsat5} \geq 1\ V$$

$$V_{dsat5} \leq 265.62\ mV$$

The second condition from the swing-high spec:

$$Swing - high = V_{DD} - V_{dsat7} = 1.6\ V$$

$$V_{dsat7} \leq 200\ mV$$

I will take the lower value which will satisfy both conditions which is V*=200 mV

$$therefore \left(\frac{g_m}{I_D}\right)_{5,6,7} = \frac{2}{V^*} = 10$$

12) Use the CMRR spec to find gds of the tail current source (note that the second stage does not affect the CMRR). However, to complete this step you need gm of the current mirror load. This is not known yet, because we want VGS of 1st stage load = VGS of 2nd stage input. To break this deadlock, assume a relatively low gm/ID (e.g., gm/ID = 10) for first stage current mirror load1. Thus, get gds of tail current source.

$$CMRR = \frac{A_{vd}}{Avcm} \rightarrow A_{vcm} = -38\ dB$$

Assume $\left(\frac{g_m}{I_D}\right)_{3,4} = 10 \quad \rightarrow g_{m3,4} = 62.5\ uS$

$$A_{vcm} = -\frac{1}{2 * g_{m3,4} * r_{o5}} = -\frac{g_{ds5}}{2 * g_{m3,4}} \rightarrow g_{ds5} = 1.573\ uS$$

13) Tail current source and 2nd stage load must have the same L (they form a current mirror). Thus, get gds of the 2nd stage load (note that both gm and gds are proportional to ID).

$$since \left(\frac{g_m}{I_D}\right)_{5,6,7} = 10 \rightarrow g_{m5} = 125\ uS$$

$$g_{m7} = 475\ uS\ , g_{m6} = 100\ uS$$

$$g_{ds6} = 1.2584\ uS \quad g_{ds7} = 5.9774\ uS$$

Since $g_{ds5} = 1.573\ uS \rightarrow using\ ADT\ sizing\ assistant$

$$L_5 = 572.44\ nm \quad W_5 = 5.6825\ um$$

Since all of the top 3 mirroring transistors have the same L and same gm/Id

So again, by using ADT sizing assistant I can get the values of W and L of both M6 & m7

$$L_5 = L_6 = L_7 = 572.44\ nm\ W_6 = 4.546\ um \quad W_7 = 21.59\ um$$

14) Given the 2nd stage gain, calculate gds and L of the 2nd stage input transistor. This transistor is now fully specified; thus, calculate its VGS.

$$Gain_2 = g_{m8} * (r_{o7} \backslash\backslash r_{o8})$$

$$Gain_2 = \frac{g_{m8}}{g_{ds7} + g_{ds8}} \rightarrow \quad g_{ds8} = 17.739\ uS$$

By using ADT sizing assistant

$$V_{gs} = 588.53\,mV \qquad L_8 = 197.54\,nm \qquad W_8 = 5.413\,um$$

15) Note that you need to avoid systematic offset. Use VGS charts to guarantee that 1st stage current mirror load and 2nd stage input transistor have the same VGS. Use this condition to determine the gm/ID of the current mirror load in the first stage. Check that the calculated gm/ID is larger than the one you assumed before (to guarantee that the CMRR is satisfied). Otherwise, re-iterate with the new gm/ID value (if the difference is large). If this step is not done properly, you will find that VOUT goes towards VDD or GND and one of the output transistors is out of saturation. In order to make sure that the systematic offset is cancelled, you can sweep the width of the current mirror load with fine step till VOUT is around VDD/2.

$$g_{ds3,4} = 721.15\,nS$$

Using ADT sizing assistant
first by setting I=6.25 uA , Vgs=588.53 mV , gds=721.15 nS

$$\left(\frac{g_m}{I_D}\right)_{3,4} = 12.27 \quad L_{3,4} = 706.59\,nm \qquad W_{3,4} = 1.47\,um$$

The gm/Id is between 10 and 15 so I didn't iterate anymore. And also, I did set the Vgs of the load current mirror to be equal the Vgs of the input transistor the second stage to cancel the systematic offset.

16) Verify that your gm/ID choices do not violate the CMIR and the peak-to-peak output swing.

$$CMIR_{low} = -V_{gs1} + V_{dsat1} + V_{gs3} = 194.84\,mV < 200\,mV$$
$$CMIR_{high} = V_{DD} - V_{gs1} - V_{dsat5} = 1.099\,V > 1\,V$$

The CMIR and peak-to-peak output swing is satisfied.

17) Choose Rz to place the zero at infinity (some designers may move the LHP zero to the vicinity of the non-dominant pole to improve the PM). Do NOT place the LHP zero at a frequency less than $\omega p2$.

$$R_z = \frac{1}{G_{m2}} = \frac{1}{g_{m8}} = 1333.333\,\Omega$$

2) A table showing W, L, g_m,I_D, g_m/I_D, $vdsat$, $V_{ov}=V_{GS}-V_{TH}$, and $V_*=2I_D/g_m$ of all transistors (as calculated from gm/ID curves).

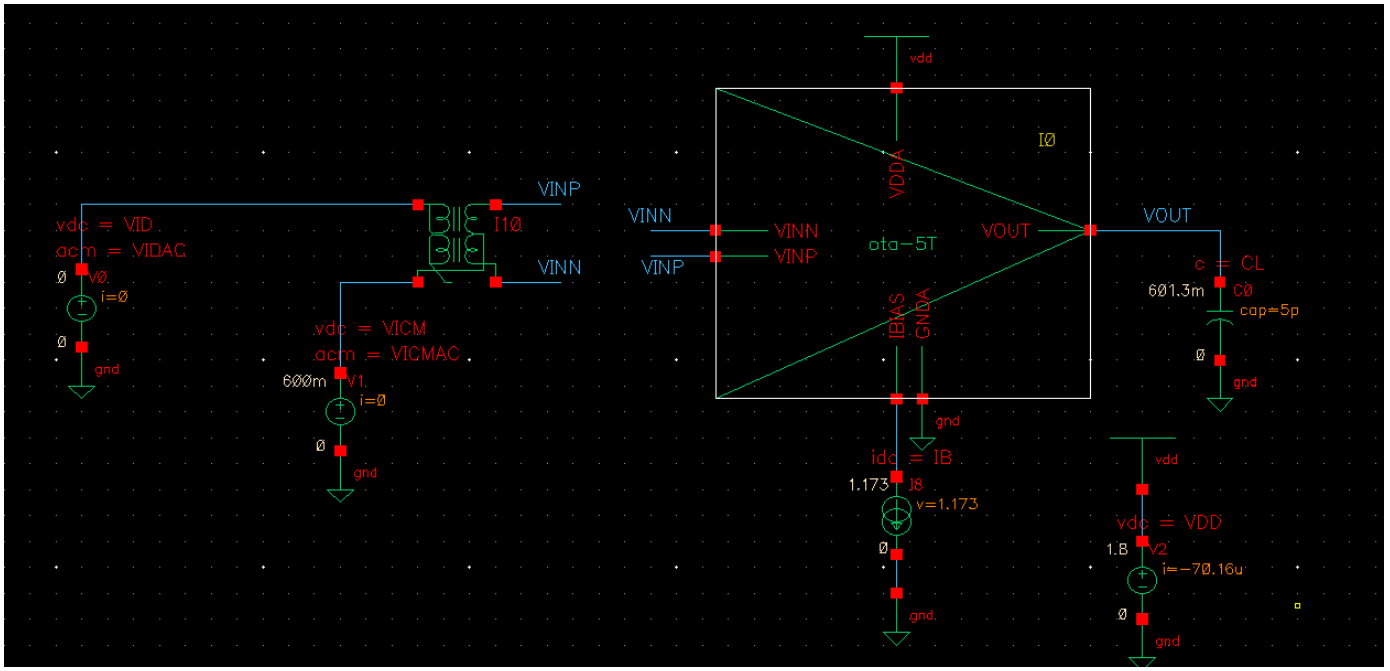
	M1, M2	M3, M4	M5	M6	M7	M8
W	11.477 um	1.47 um	5.6825 um	4.546 um	21.59 um	5.413 um
L	828.2 nm	706.59 nm	572.44 nm	572.44 nm	572.44 nm	197.54 nm
gm	93.25 uS	76.7 uS	124.51 uS	124.51 uS	124.51 uS	744.24 uS
Id	6.25 uA	6.25 um	12.5 uA	10 uA	47.5 uA	47.5 uA
gm/Id	15	12.27	10	10	10	15.668
Vdsat	108.02 mV	129.79 mV	166 mV	166 mV	166 mV	94.473 mV
Vov	116.99 mV	165.1 mV	290.08 mV	290.08 mV	290.08 mV	104.27 mV
V*	134.08 mV	162.9 mV	200.78 mV	200.78 mV	200.78 mV	127.65 mV

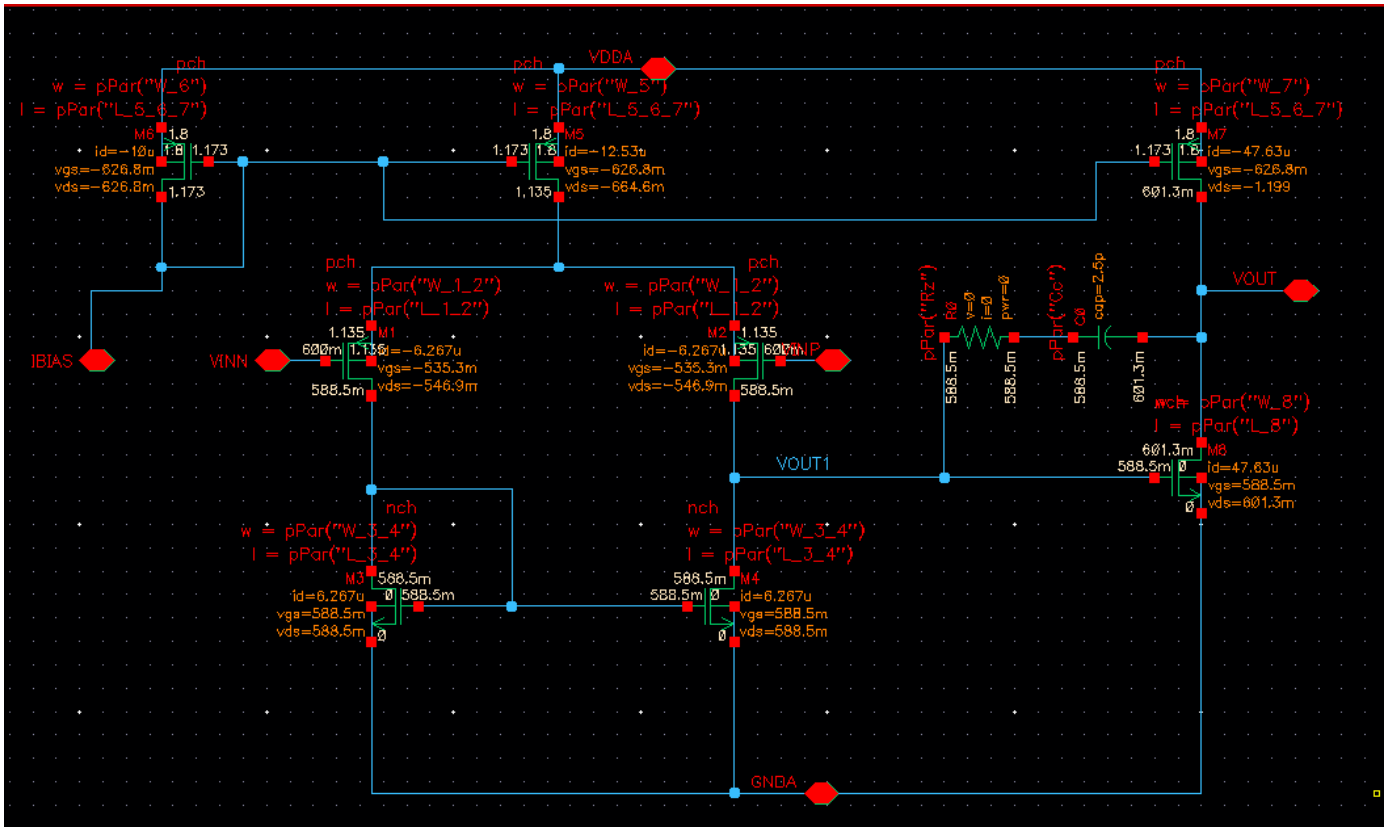
PART 3: Open-Loop OTA Simulation

1) Schematic of the OTA and bias circuit with DC node voltages clearly annotated.

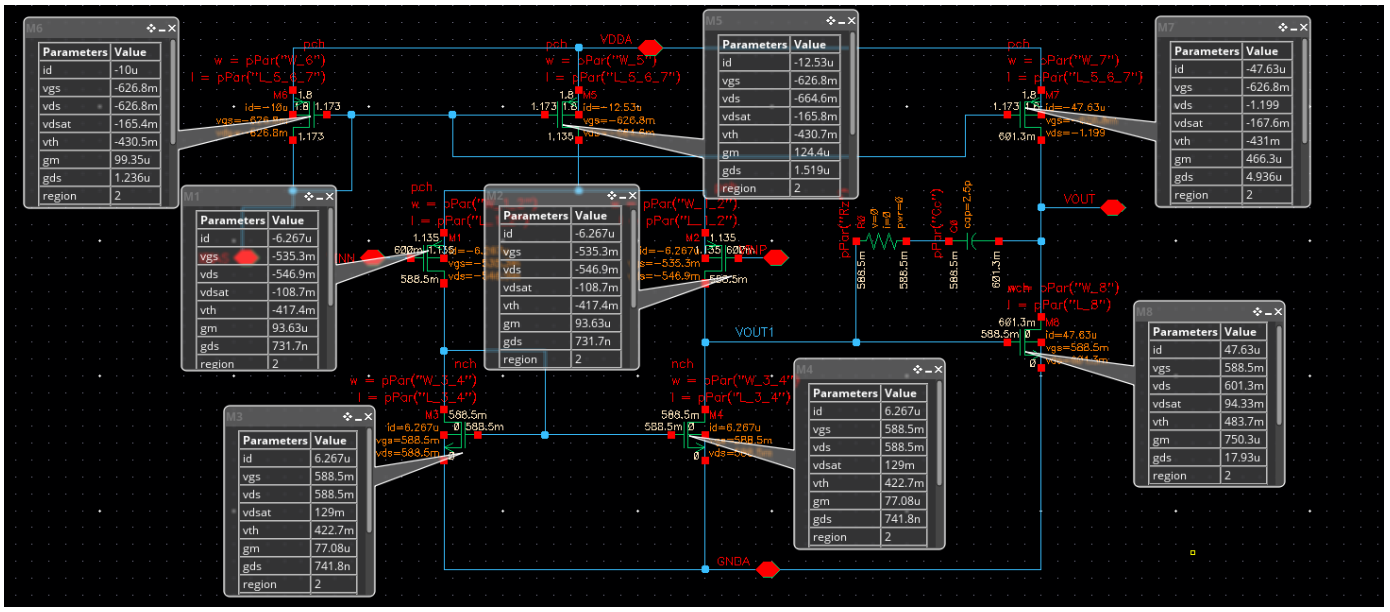
I did some fine changes to the widths of some transistors to flow the required current and this is the final values I used for simulation

CDF Parameter	Value	Display
Cc	2.5p	off
L_1_2	828.2n	off
L_3_4	706.59n	off
L_5_6_7	572.44n	off
L_8	197.54n	off
Rz	1333.333	off
W_1_2	11.477u	off
W_3_4	1.47u	off
W_5	5.66u	off
W_6	4.546u	off
W_7	20.1u	off
W_8	5.413u	off





Operating point:



Is the current (and gm) in the input pair exactly equal?

Yes, they are exactly equal.

What is DC voltage at the output of the first stage? Why?

588.5 mV, because it follow the current mirror diode connection node .

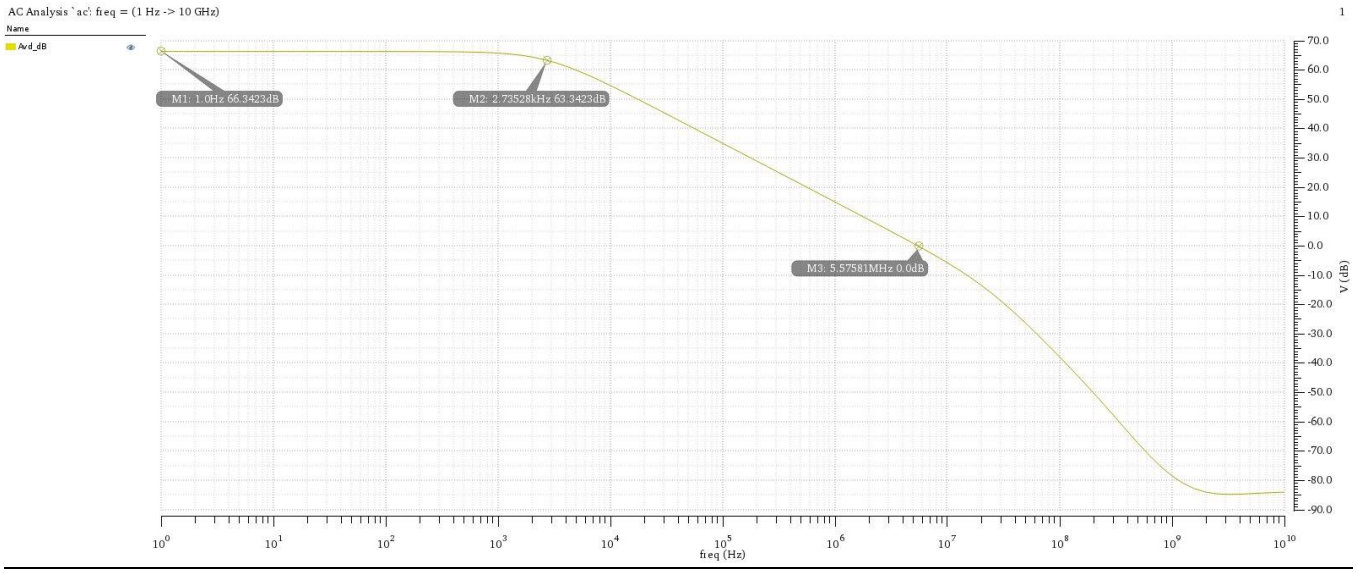
What is DC voltage at the output of the second stage? Why?

601.3 mV , because I set vds=600 mV

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_09:part_3:1	VOUT2	601.3m			
Lab_09:part_3:1	VOUT1	588.5m			

1) Diff small signal ccs:

Plot diff gain (in dB) vs frequency



Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_09:part_3:1	Ao	2.075k			
Lab_09:part_3:1	Ao_dB	66.34			
Lab_09:part_3:1	BW	2.744k			
Lab_09:part_3:1	UGF	5.615M			
Lab_09:part_3:1	GBW	5.695M			

Compare simulation results with hand calculations in a table.

$$A_o = gain1 * gain2 = \frac{g_{m1}}{gds_2 + gds4} * \frac{g_{m8}}{gds7 + gds8} = 63.54 * 32.81 = 2084.93 = 66.38dB$$

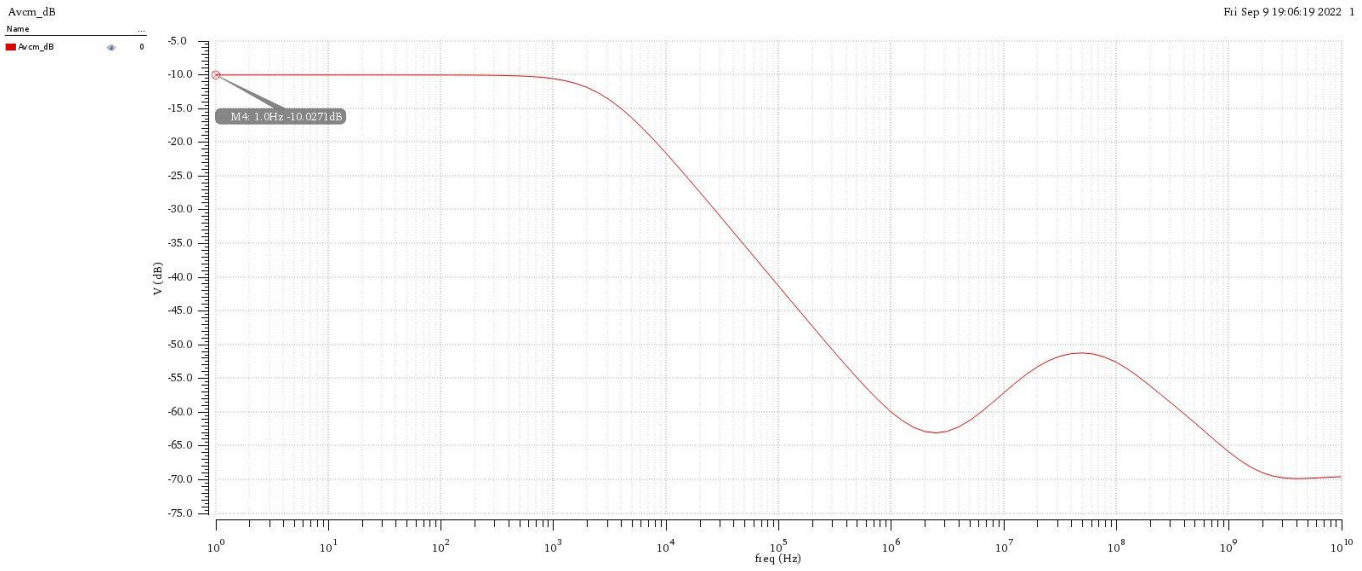
$$BW = \frac{1}{2 * pi * Rout1(G_{m2} * R_{out2}) * C_c} = 2856.13\ Hz$$

$$GBW = 5.954\ MHz$$

	Simulation	Analytical
Gain	2075=66.34 dB	2084.8=66.38 dB
BW	2.744 K	2856.13 Hz
GBW	5.695 M	5.954 MHz

2) CM small signal ccs:

Plot CM gain in dB vs frequency.



Compare simulation results with hand calculations in a table.

$$A_{vcm} = -\frac{1}{2 * g_{m34} * r_{o5}} = 9.85\ m = -40.12\ dB$$

$$A_{vcm_{tot}} = A_{vcm} * Gm2 * Rout2 = -40.12\ dB + 30dB = -10.12\ dB$$

	Simulation	Analytical
A_VCM in dB	-10.00271 dB	-10.12 dB

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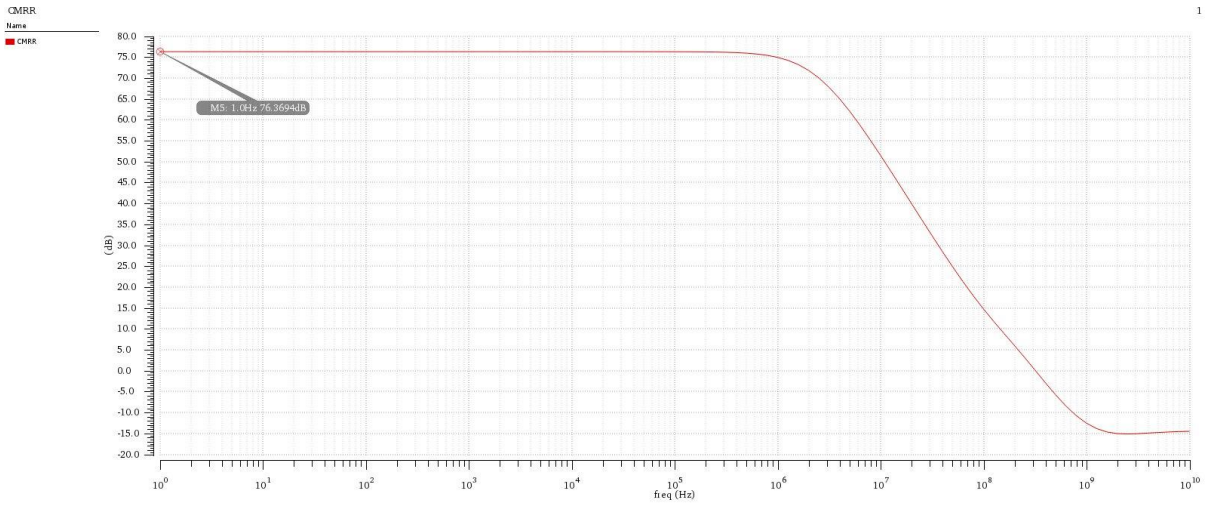
3) (Optional) CMRR:

Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



Compare simulation results with hand calculations in a table.

$$CMRR = A_{vd_{dB}} - A_{vcm_{dB}} = 66.38 - -10.12 = 76.5\ dB$$

	Simulation	Analytical
CMRR in dB	76.4694 dB	76.5 dB

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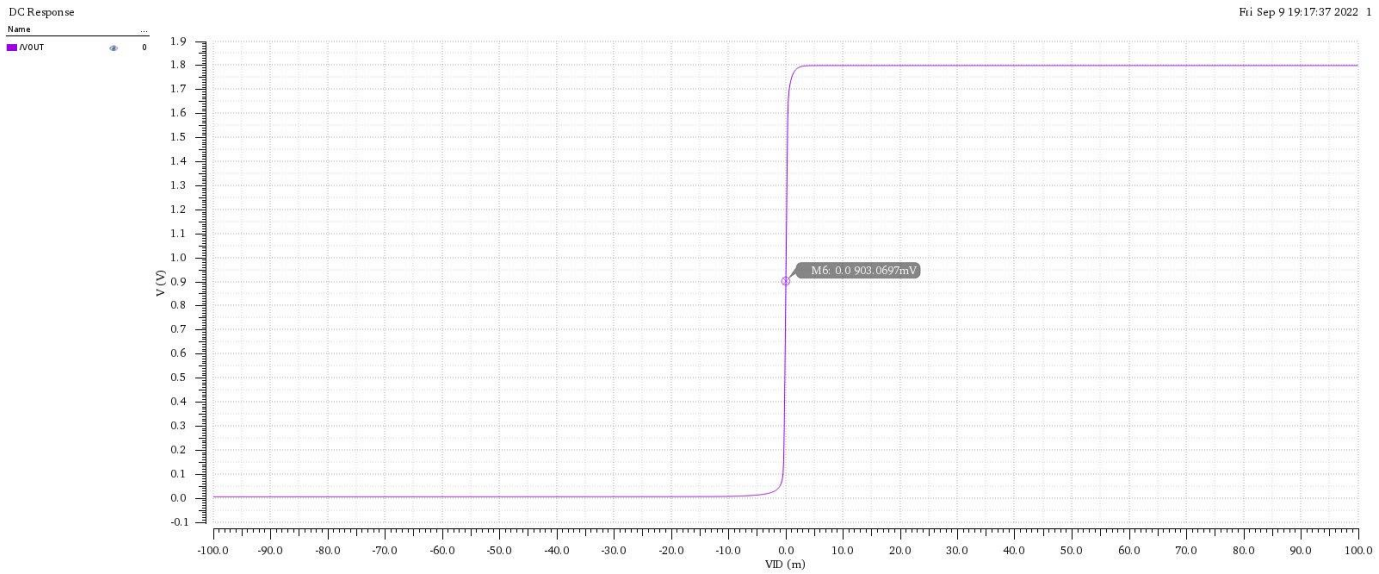
2) (Optional) Diff large signal ccs:

Plot VOUT vs VID.

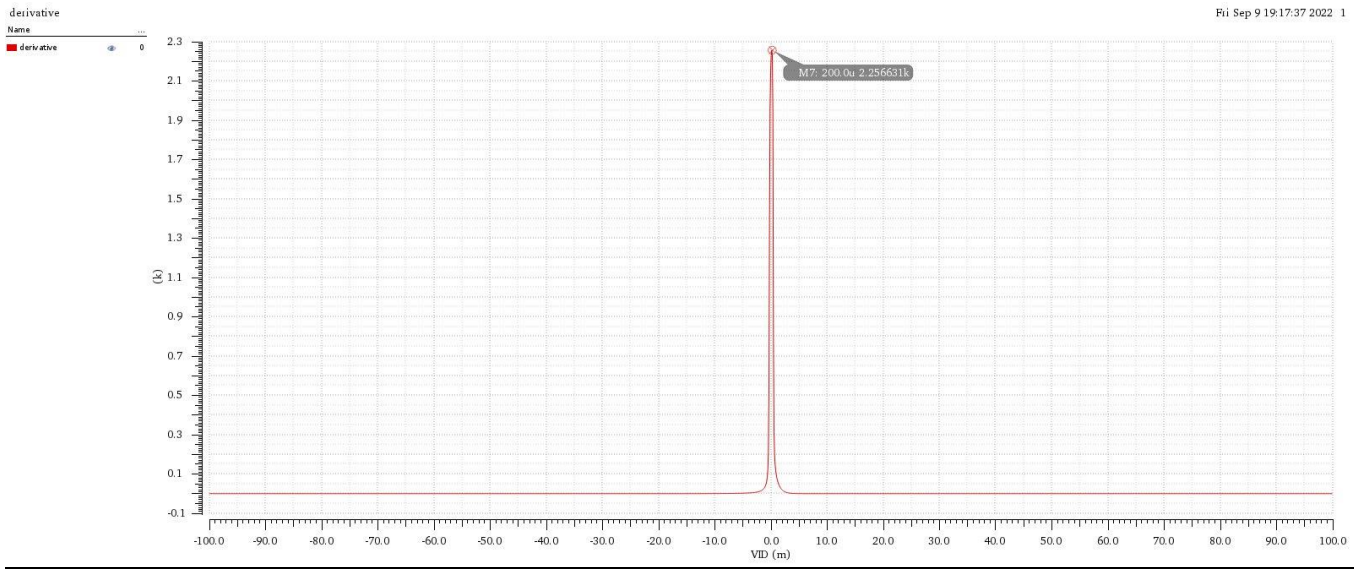


From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.

Vout at Vind=0 = 903.0697 mV

Here I used Vicm=0.9 so the output follows the common mode
in the dc I used Vicm =0.6 and the output followed it also and was 603.3 mV

Plot the derivative of VOUT vs VID. Compare the peak with Avd from ac analysis. Comment on the result.



	Derivative	Avd
Peak	2.25K=67 dB	2.078K=66.34 dB

Comment:

the value of the derivative of the output signal at its peak is almost equal to the gain in dB.

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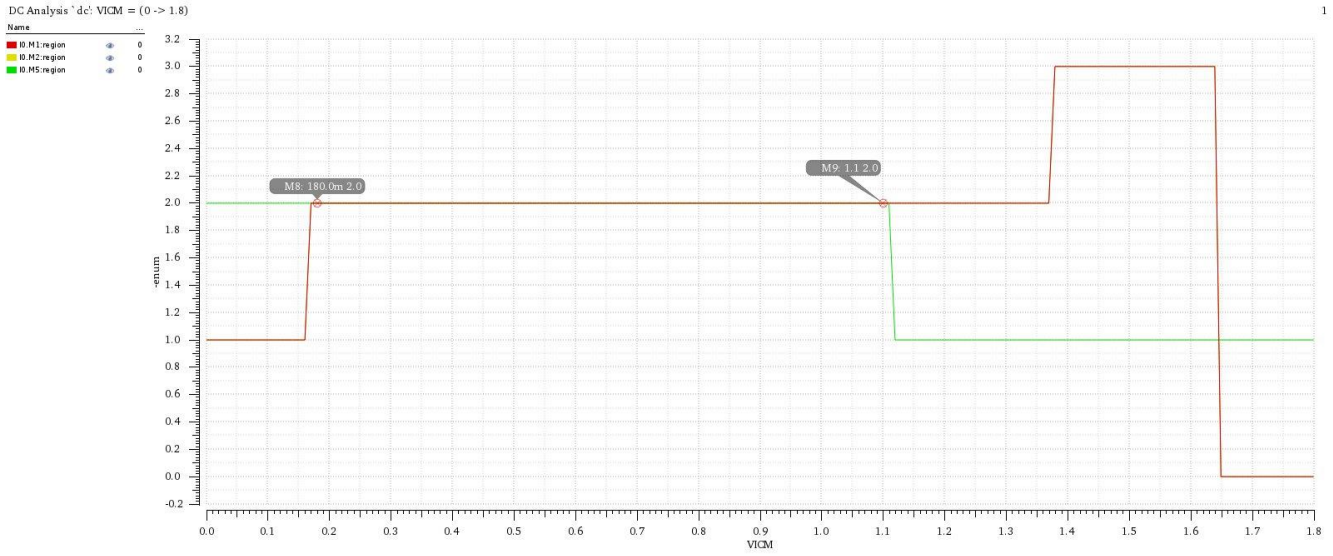
4) CM large signal ccs (region vs VICM):

Plot "region" OP parameter vs VICM for the input pair and the tail current source.



Find the CM input range (CMIR). Compare with hand analysis in a table.

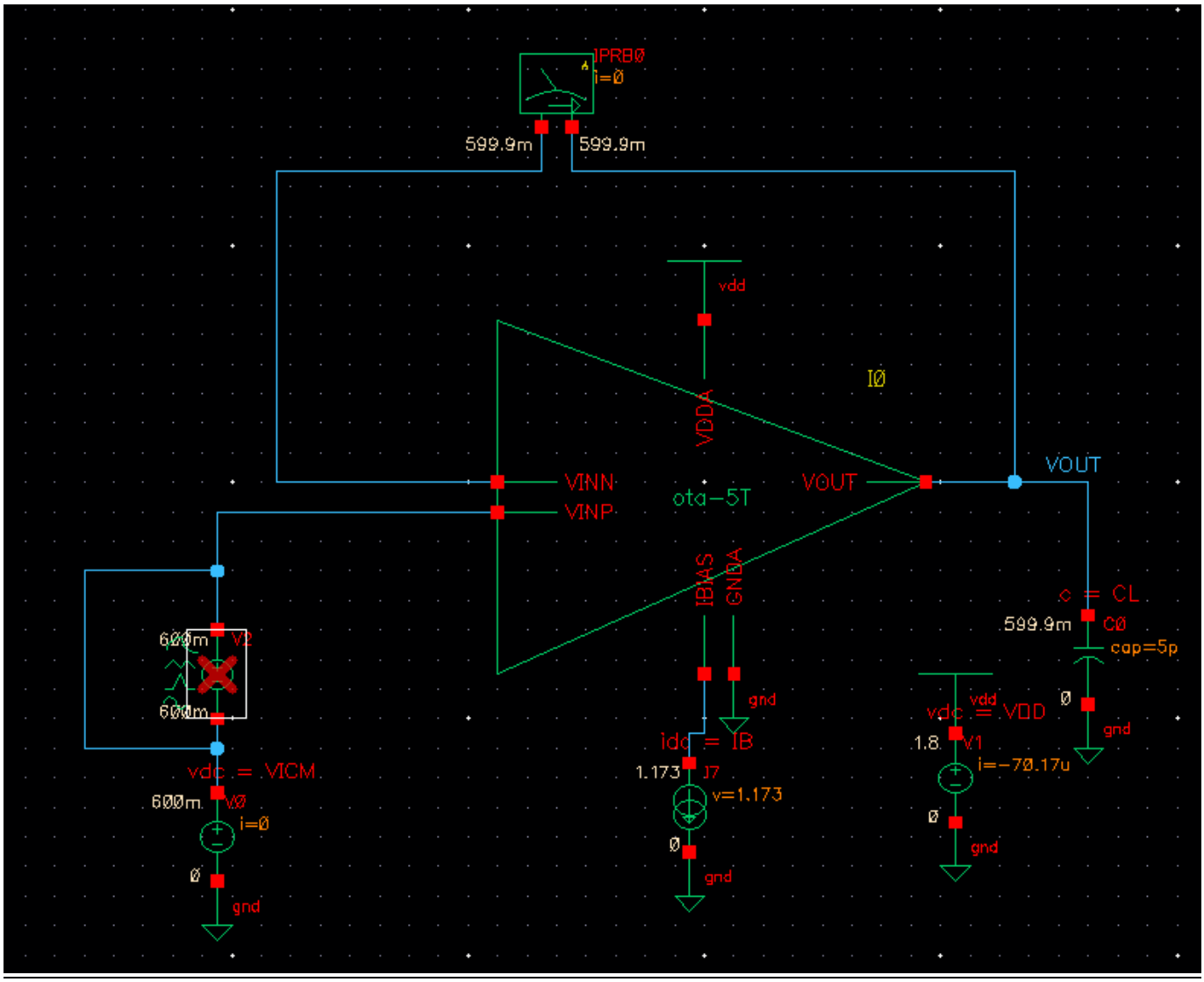
$$CMIR_{low} = -V_{gs1} + V_{dsat1} + V_{gs3} = 161.9\,mV < 200\,mV$$

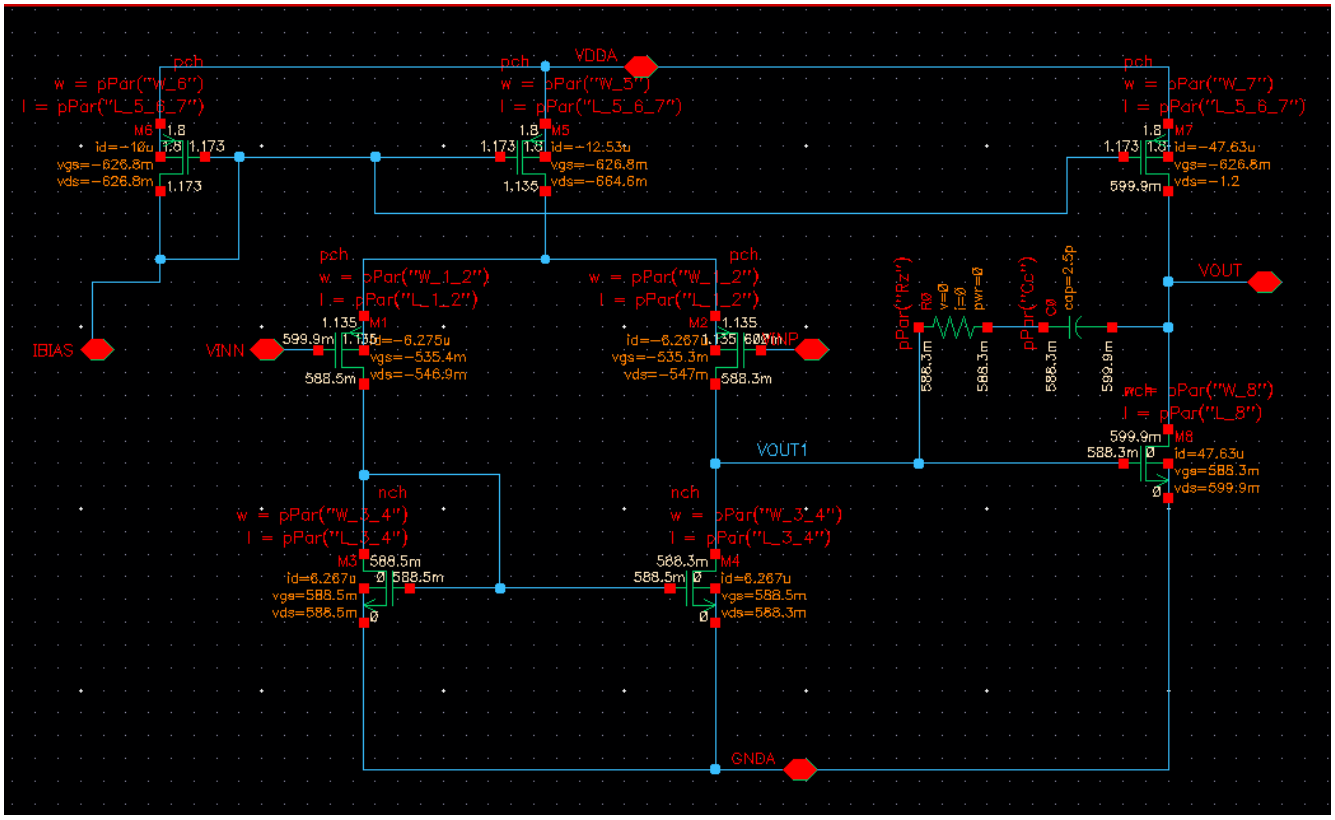
$$CMIR_{high} = V_{DD} - V_{gs1} - V_{dsat5} = 1.0989\,V > 1\,V$$

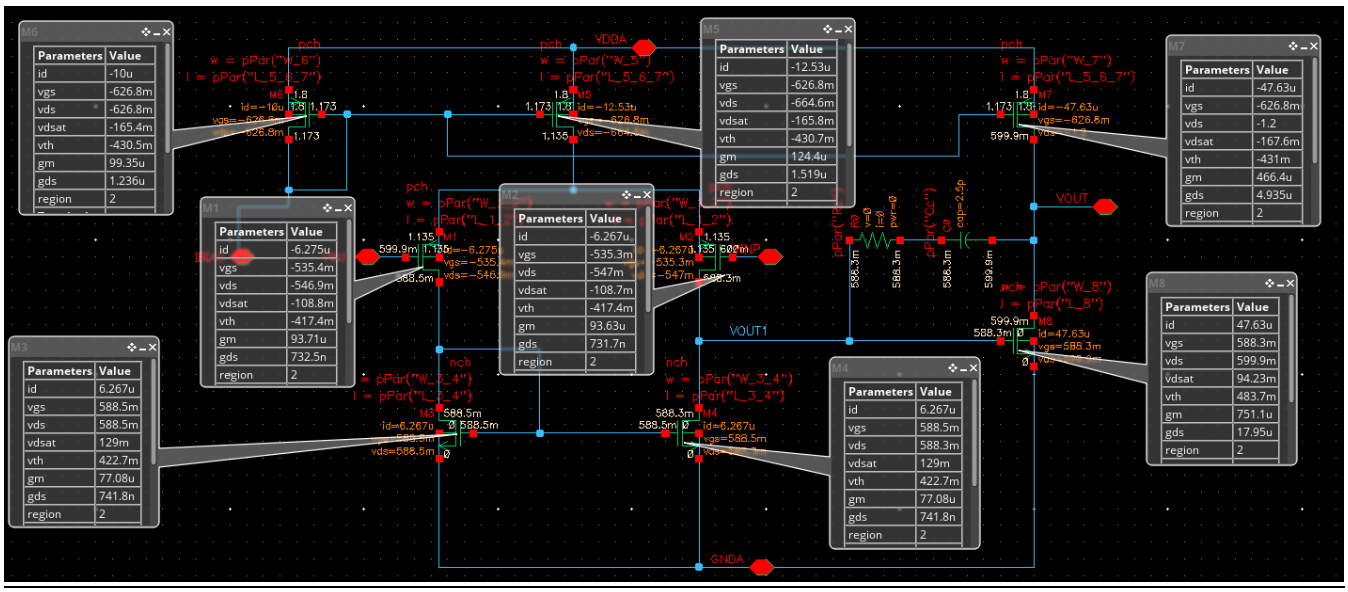
	Simulation	Analytical
CMIR_low	180 mV	161.9 mV
CMIR_high	1.1 V	1.0989 V

PART 4: Closed-Loop OTA Simulation

1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.







Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

$$V_{INP} = 600\,mV \;, V_{INN} = V_{OUT} = 599.9\,mV$$

So, they are not exactly equal and that's due to the static error introduced by the loop gain.

Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

In the closed loop: Vout1 = 588.3 mV
In the open loop: Vout1=588.5 mV

They are not exactly equal but they are very close to each other and that's due to the feedback that did the mismatch

Is the current (and gm) in the input pair exactly equal? Why?

No, they are not exactly equal but very close to each other and that's due to the feedback network

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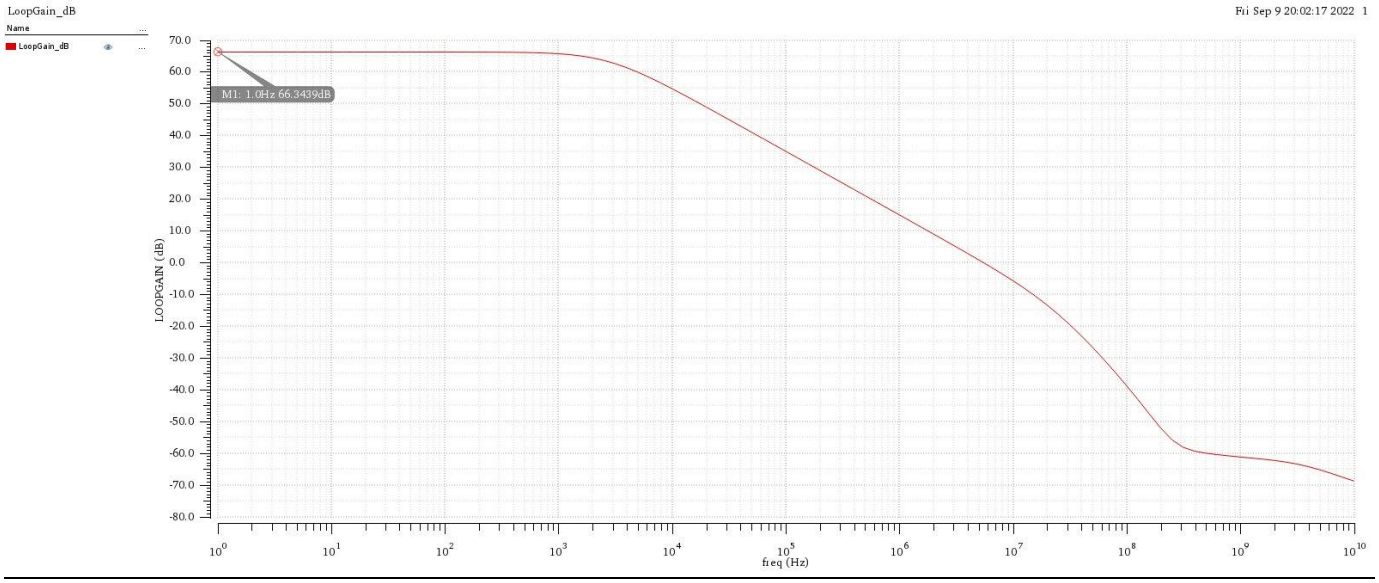
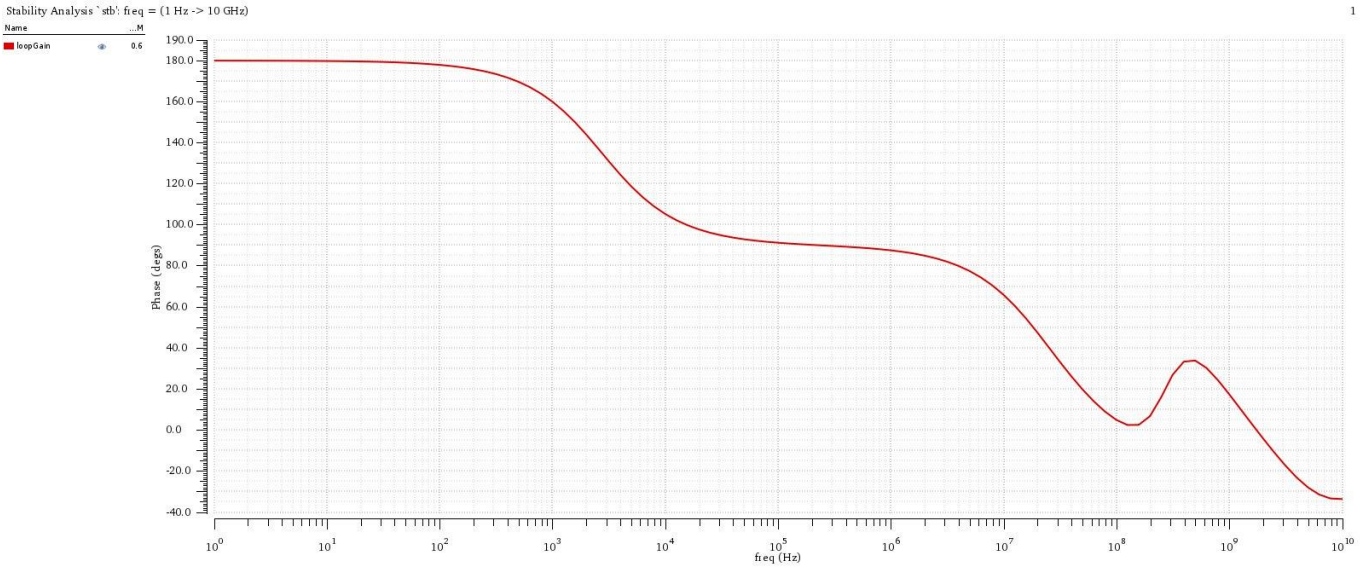
2) Loop gain:

Plot loop gain in dB and phase vs frequency.



Phase vs frequency



Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment

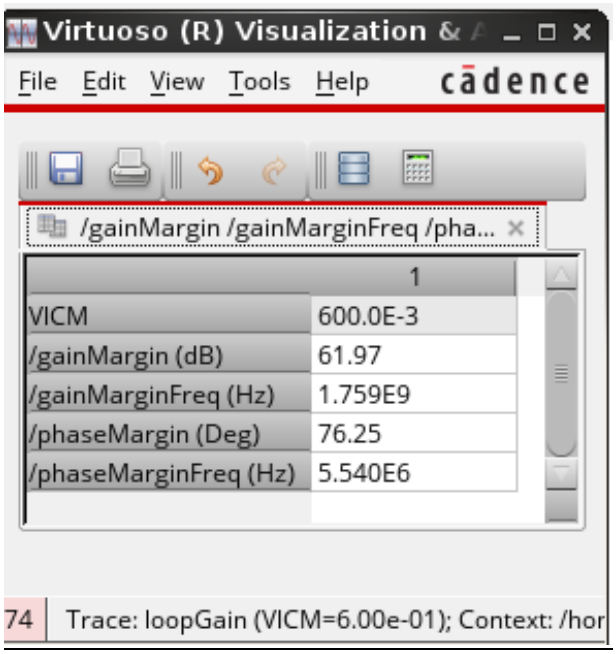
Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_09:part_4:1	LoopGain_dB				
Lab_09:part_4:1	Ao	2.076k			
Lab_09:part_4:1	BW	2.744k			
Lab_09:part_4:1	UGF	5.612M			
Lab_09:part_4:1	GBW	5.697M			
Lab_09:part_4:1	Ao_dB	66.34			

	Open-Loop	Closed-Loop
Gain in dB	66.34 dB	66.34 dB
UGF	5.615 M	5.612 M
GBW	5.695 M	5.697 M

Comment:

All of the parameters are almost the same as the feedback network is a buffer and has B ideally=1 that's why the values are almost the same.

Report PM. Compare with hand calculations. Comment.



$$\mathrm{GX} = UGF = 5.612 * 2\mathrm{pi} = 35.261 \ \ \mathrm{Mrad/sec}$$

$$\mathrm{w_{p2}} = 4 * w_u = \ 125.712 \ M \ rad/sec$$

$$PM = 90^0 - \tan^{-1}\left(\frac{GX}{w_{p2}}\right) = 74.33^0$$

Comment:

The phase margin in the simulation and the hand analysis is very close to each other and it's equal to 76 degrees.

First of all, it met the design spec needed

Secondly 76 degrees means critical damped response and it means fastest settling time and without overshoot.

Compare simulation results with hand calculations in a table.

$$\mathrm{Gain} = \mathrm{Gain_1} * Gain_2 = 63.596 * 32.82 = 2087.26 = 66.39 \ dB$$

$$BW = \frac{1}{2 * pi * Rout1(G_{m2} * R_{out2}) * C_c} = 2858.19 \ Hz$$

$$\mathrm{GBW} = \mathrm{Gain} * \mathrm{BW} = 5.965 \ \mathrm{M}$$

	Simulation	Analytical
PM	76.25 degree	75.9637 degree
Gain	66.34 dB	66.39 dB
BW	2.744 K	2.858 K
GBW	5.697 M	5.965 M

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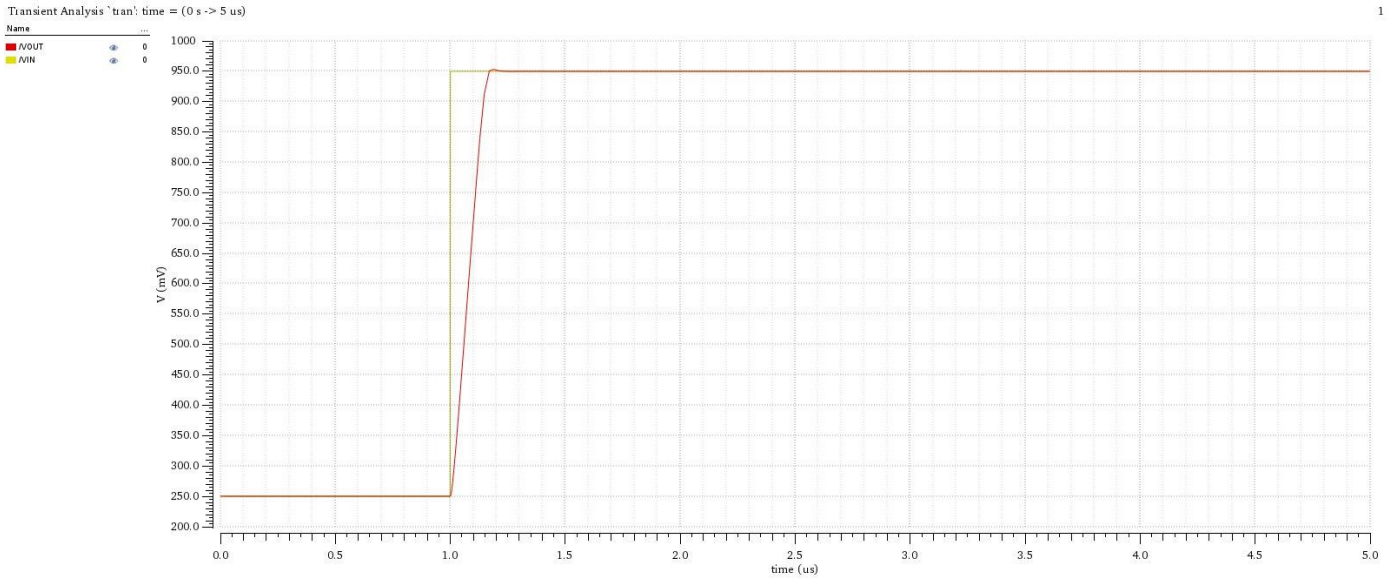
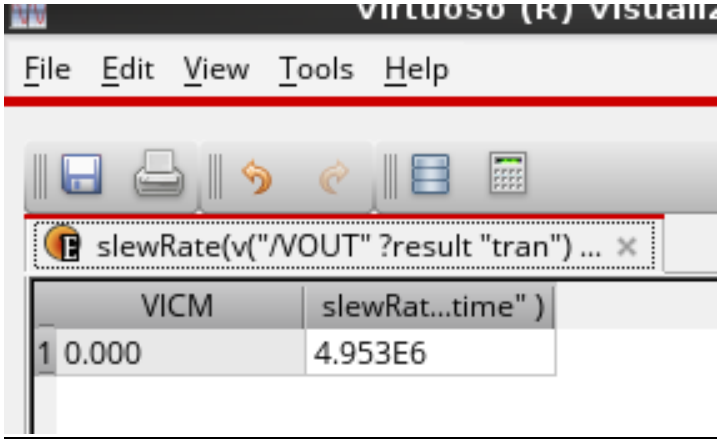
3) Slew rate:

Report Vin and Vout overlaid.



Report the slew rate.



Compare simulation results with hand calculations in a table

$$SR = \frac{I_{B1}}{C_c} = 5\ M$$

	Simulation	Analytical
Slew Rate	4.953 M	5 M

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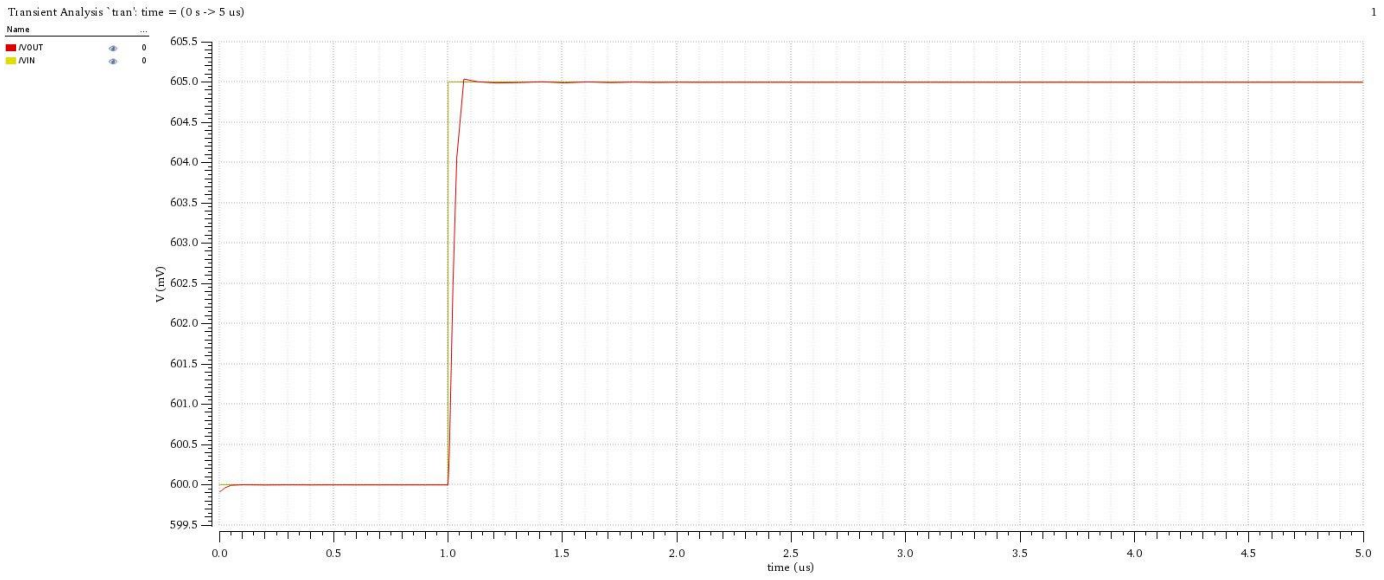
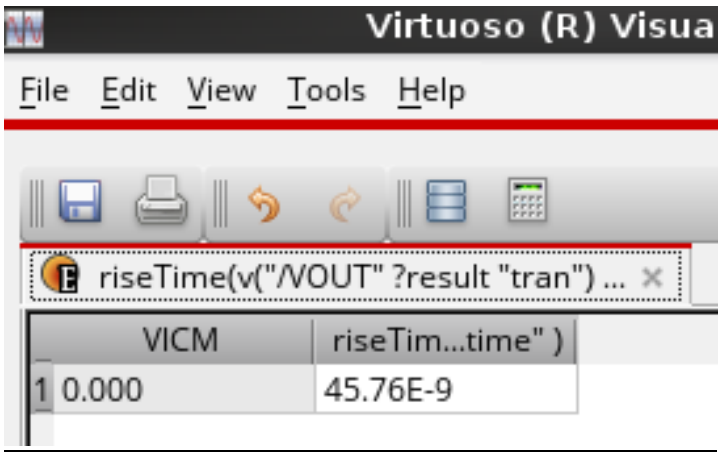
4) Settling time:



Do you see any ringing? Why?

No, there is no ringing as the system has a critical damped response.

Calculate the output rise time from simulation.



Compare simulation results with hand calculations in a table.

$$UGF = 35.261\ M\ rad/sec$$

$$UGF = \frac{1}{tao} \rightarrow tao = 28.359\ n\ sec$$

$$T_{rise} = 2.2 * tao = 62.39\ nsec$$

	Simulation	Analytical
Trise	45.76 n	62.39 n