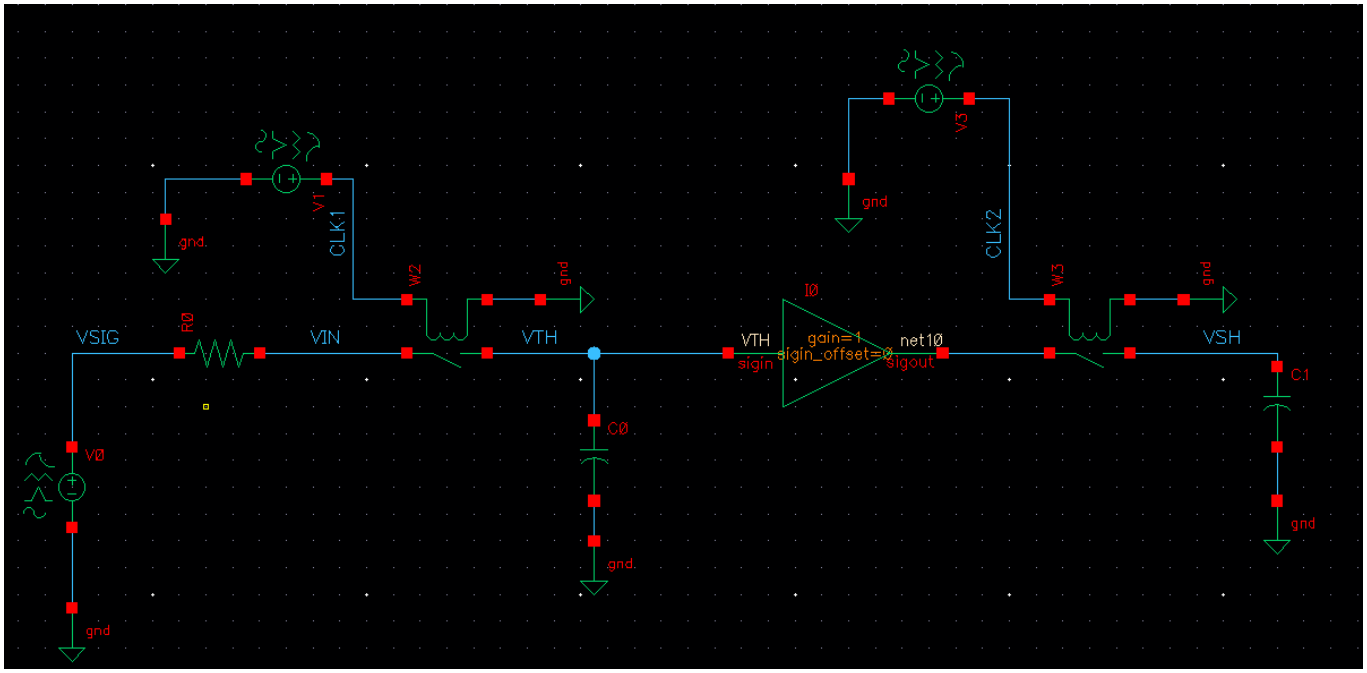
Analog Integrated System Design – Cadence Tools
Lab 02
Sampling and Quantization

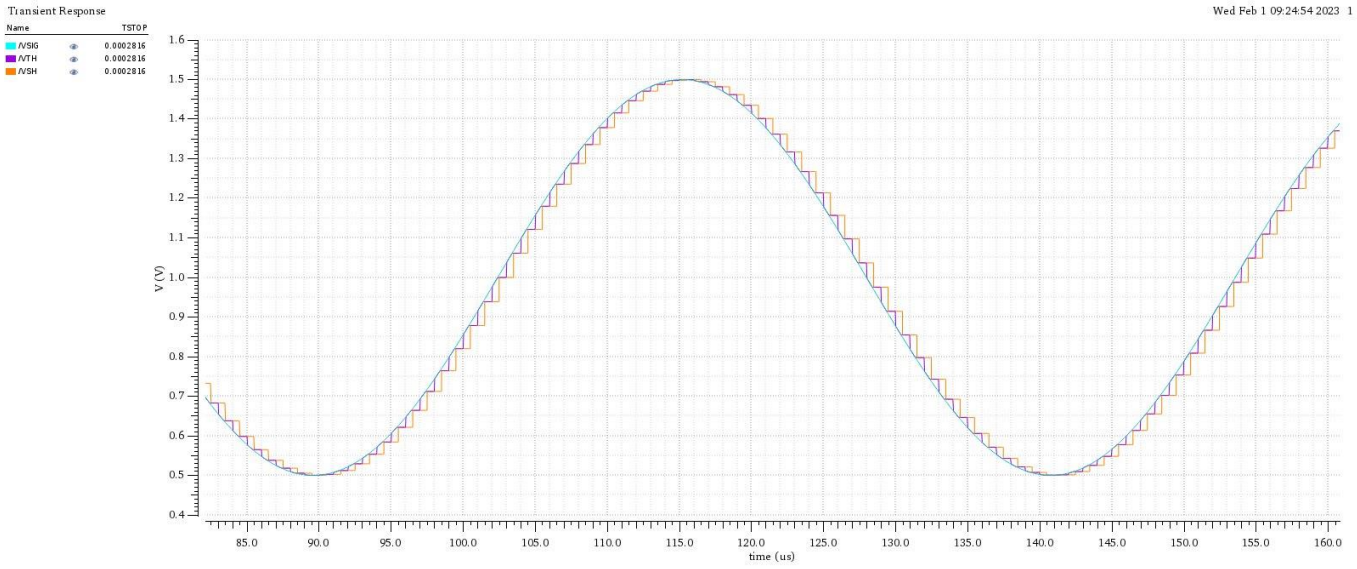
PART 1: Ideal Track & Hold and Sample & Hold

Schematic:

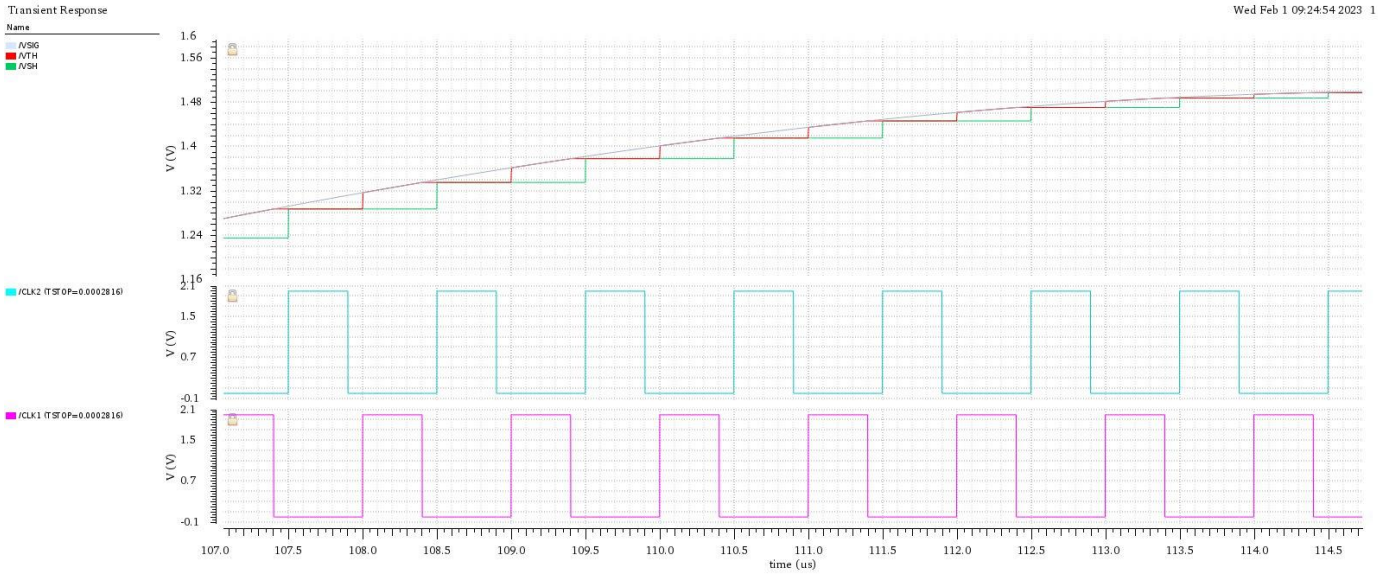


Run transient analysis. Plot VSIG, VTH, and VSH overlaid. Zoom in to observe the difference between T&H (VTH) and S&H (VSH).

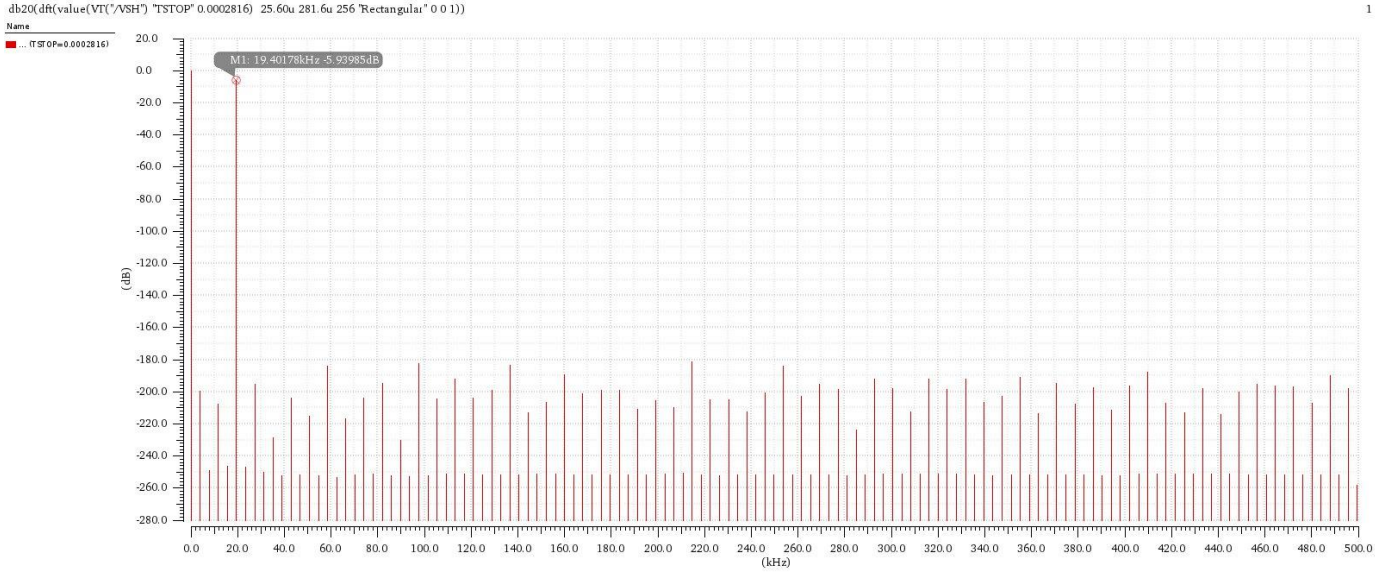
Output not zoomed in:



Zoom in version:



Use the Spectrum Assistant to plot FFT.



Outputs

Measurement	Value
value(VT("/VSH") "TSTOP" ...	
ENOB	27.614814 (bits)
SINAD	168.00418 (dB)
SNR	169.95287 (dB)
SFDR	175.28804 (dBc)
THD	2.4896655e-07 (%)
THD	-172.07718 (dB)
Signal Power	-6.0206 (dB)
DC Power	7.020304e-13 (dB)
Noise Floor/Bin	-197.04557 (dB)
Noise Floor/rtHz	-232.9291 (dB)
Total Harmonic Power	-178.09778 (dB)
Peak Harmonic Power	-181.9635 (dB)

What is the power of the peak signal (in dB)? Why?

>>Power of the peak is -5.9 dB

$P_{signal} = 20\log_{10}(amplitude) = 20\log_{10}(0.5) = -6\ dB$

• How many bins are occupied by the test signal?

>>1 bin

• What is the noise floor (in dBFS)?

>> -197.04 dBFS

• What is the relation between the SNR, NFFT, Signal Power, and Noise Floor?

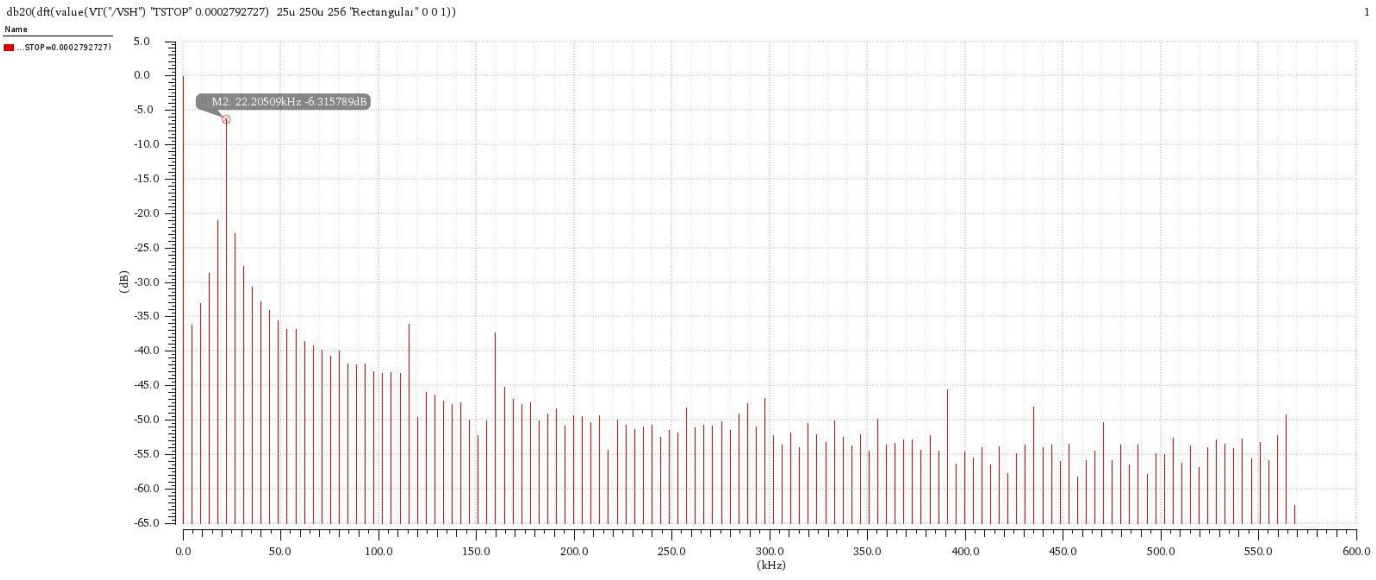
>>When signal power increases, SNR increases

When NFFT increases, the noise floor decrease

• If the sampling is ideal, what is the source of error that causes the noise floor?

>>It's due to the quantization errors

Change NCYC to 5.5 and re-simulate. Note that the start and stop time in the DFT will change from the previous case. Plot the new FFT. Observe the spectral leakage.

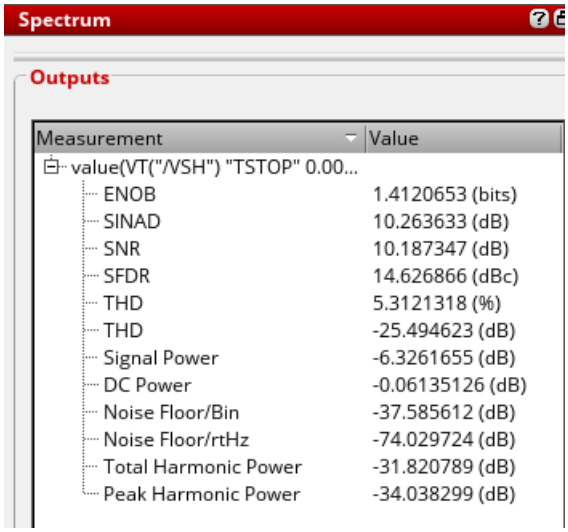


Comment:

Notice how the spectrum is showing a skirt effect.

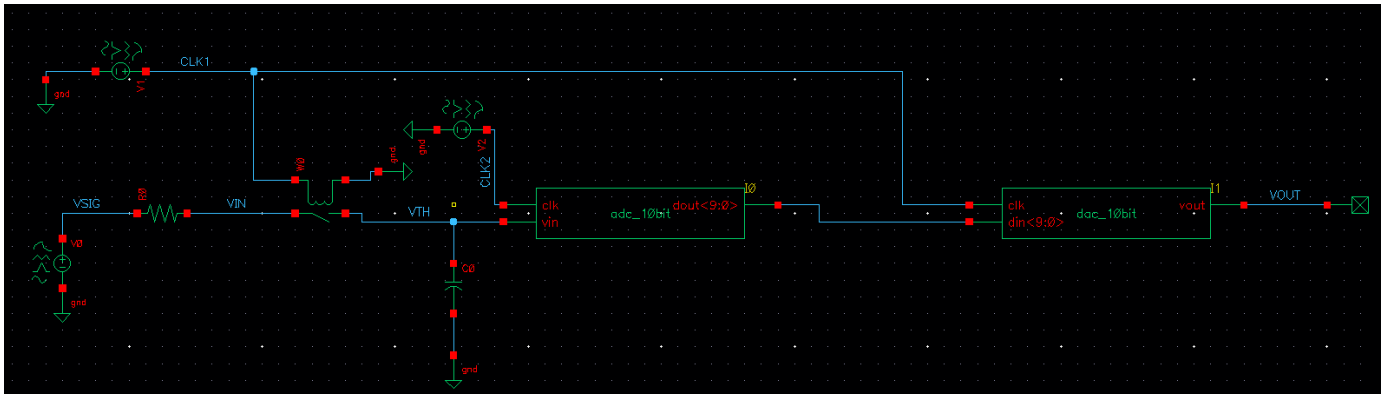
also note that the signal occupies around 3 or 5 bins.

also it's noticed that the noise floor increased than the previous case.

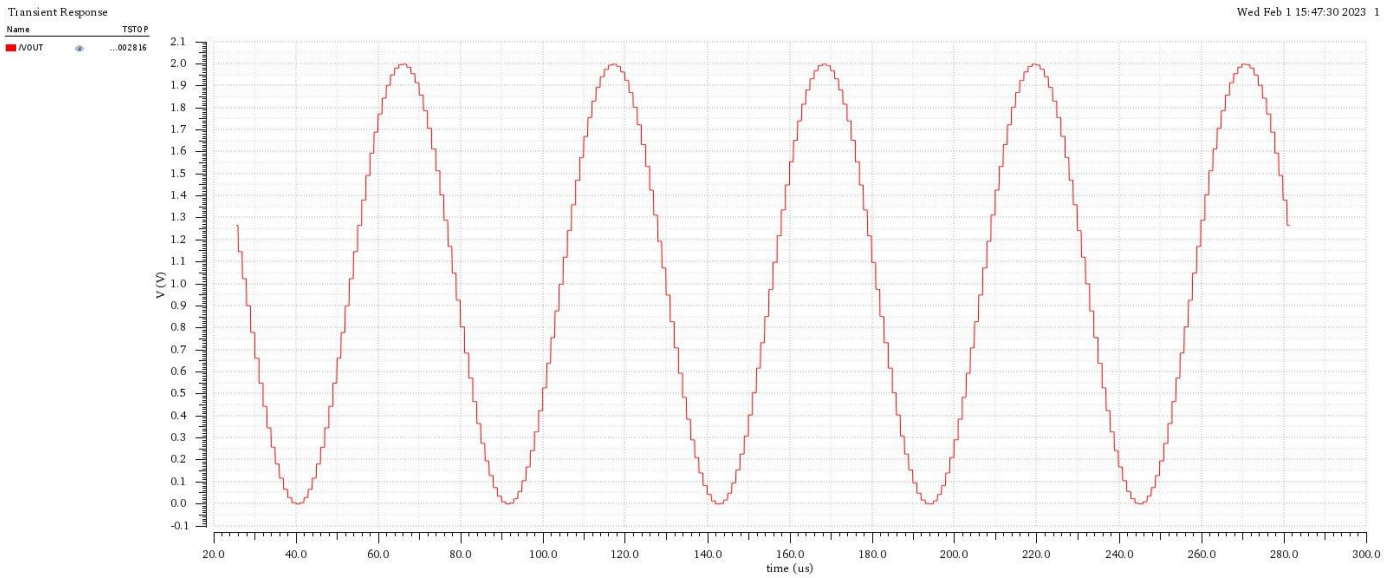

Spectrum
Outputs
Measurement
Value
value(VT("/VSH") "TSTOP" 0.00...
ENOB
1.4120653 (bits)
SINAD
10.263633 (dB)
SNR
10.187347 (dB)
SFDR
14.626866 (dBc)
THD
5.3121318 (%)
THD
-25.494623 (dB)
Signal Power
-6.3261655 (dB)
DC Power
-0.06135126 (dB)
Noise Floor/Bin
-37.585612 (dB)
Noise Floor/rtHz
-74.029724 (dB)
Total Harmonic Power
-31.820789 (dB)
Peak Harmonic Power
-34.038299 (dB)

PART 2: Quantization

Schematic:



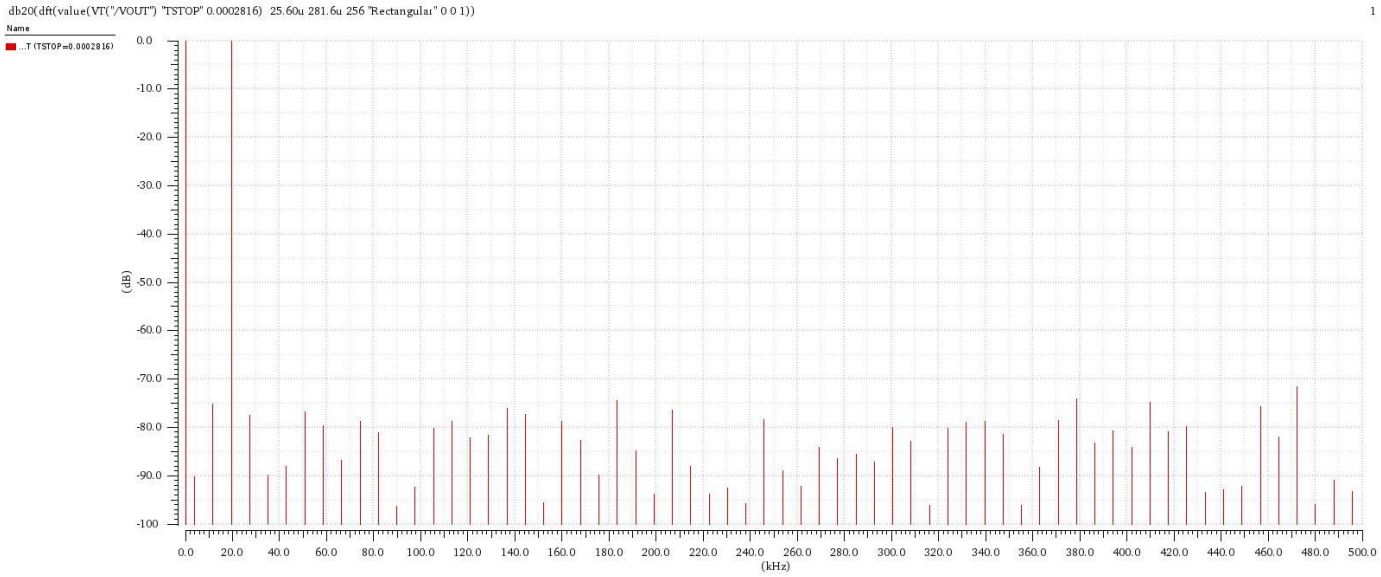
Plot the transient waveforms and study the timing relations between different signals.



You will need to increase the input signal amplitude, otherwise, the ENOB will be one bit less than the expected ideal value (why?).

>>Because when input amplitude is 0.5 volt here we are using half of the scale of the adc so we will have effective number of bits less by 1 (9 bits) so I increased the Vpeak to 1 volt.

Analyse the DAC output using the spectrum assistant. The result will be as shown below (zoom in y-axis from 0 to -100dB). Compare the SNR, ENOB, Signal Power, DC Power, and Noise Floor with the expected theoretical values.



Spectrum

Outputs

Measurement	Value
value(VT("/VOUT") "TSTOP" ...	
ENOB	10.039464 (bits)
SINAD	62.200573 (dB)
SNR	62.268259 (dB)
SFDR	71.520956 (dBc)
THD	0.019266953 (%)
THD	-74.303739 (dB)
Signal Power	-0.00012581537 (dB)
DC Power	-0.0084864586 (dB)
Noise Floor/Bin	-83.340485 (dB)
Noise Floor/rtHz	-119.22402 (dB)
Total Harmonic Power	-74.303865 (dB)
Peak Harmonic Power	-75.967938 (dB)

$$P_{signal} = 20\log_{10}(amplitiude) = 20\log_{10}(1) = 0\ dB$$

$$P_{dc} = 20\log_{10}(amplitiude) = 20\log_{10}(1) = 0\ dB$$

$$SNDR = 10\log_{10}\left(\frac{signal\ power}{Power\ of\ all\ unwanted\ signals}\right) = 61.96dB$$

$$ENOB = \frac{SNDR - 1.76}{6.02} = 10.0011\ bits$$

$$SNR = 6.02 * N + 1.76 = 61.96\ dB$$

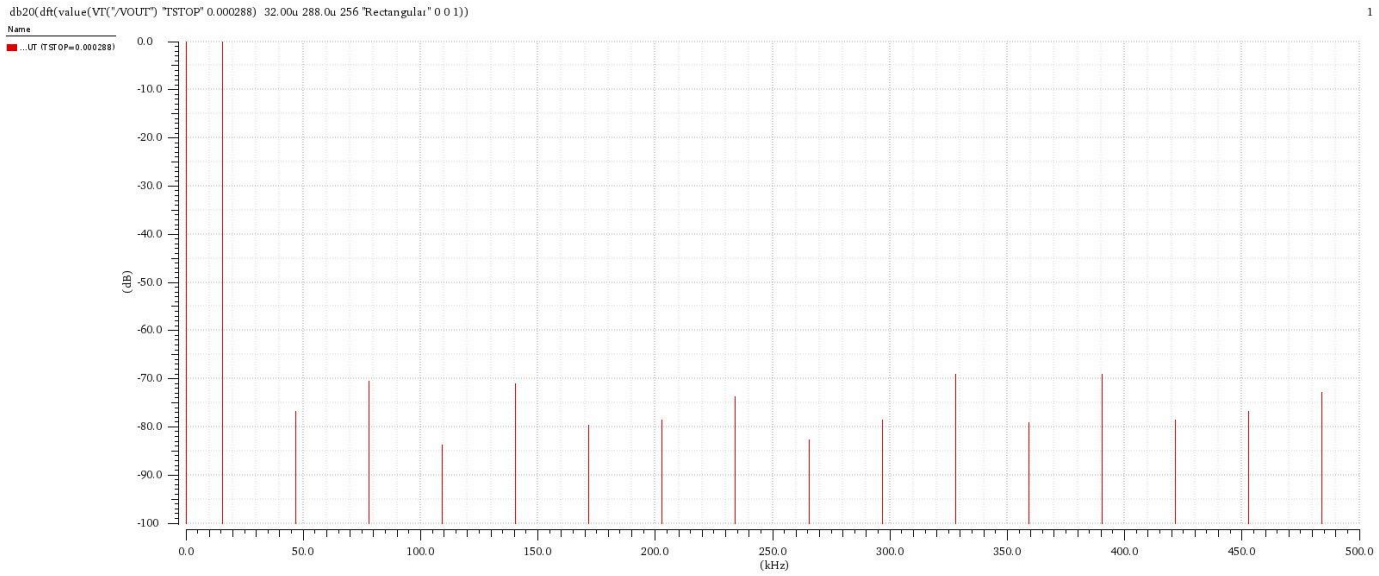
$$Noise\ floor = 10\log_{10}\left(\frac{V_{LSB}^2}{12}\right) - 10\log_{10}\left(\frac{M}{2}\right) = -86\ dB$$

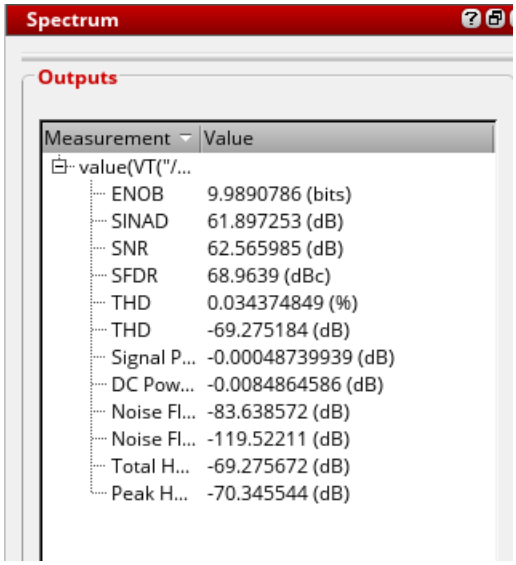
	SIMULATION	THEORETICAL
SNR	62 dB	$61.96\ dB$
ENOB	10.03 bits	10.0011 bits
SIGNAL POWER	-0.0001258 dB	0 dB
DC POWER	-0.00848 dB	0 dB
NOISE FLOOR	-83.3 dB	-86 dB

Record the value of the SFDR.

SFDR = 71.52 dBc

Change NCYC to 4 and re-simulate (now NFFT/NCYC = integer). Plot the new FFT (zoom in y-axis from 0 to -100dB). Note that the start and stop time in the DFT will change from the previous case. Compare the new SFDR with the previous one. Comment.





SFDR old	SFDR new
71.52 dBc	68.96 dBc

Comment:

When the NCYC = 4 then NFFT/NCYC = integer so now the harmonic noise is periodic and not random so the harmonic powers are higher than the first case therefore the noise floor is higher than the first case.