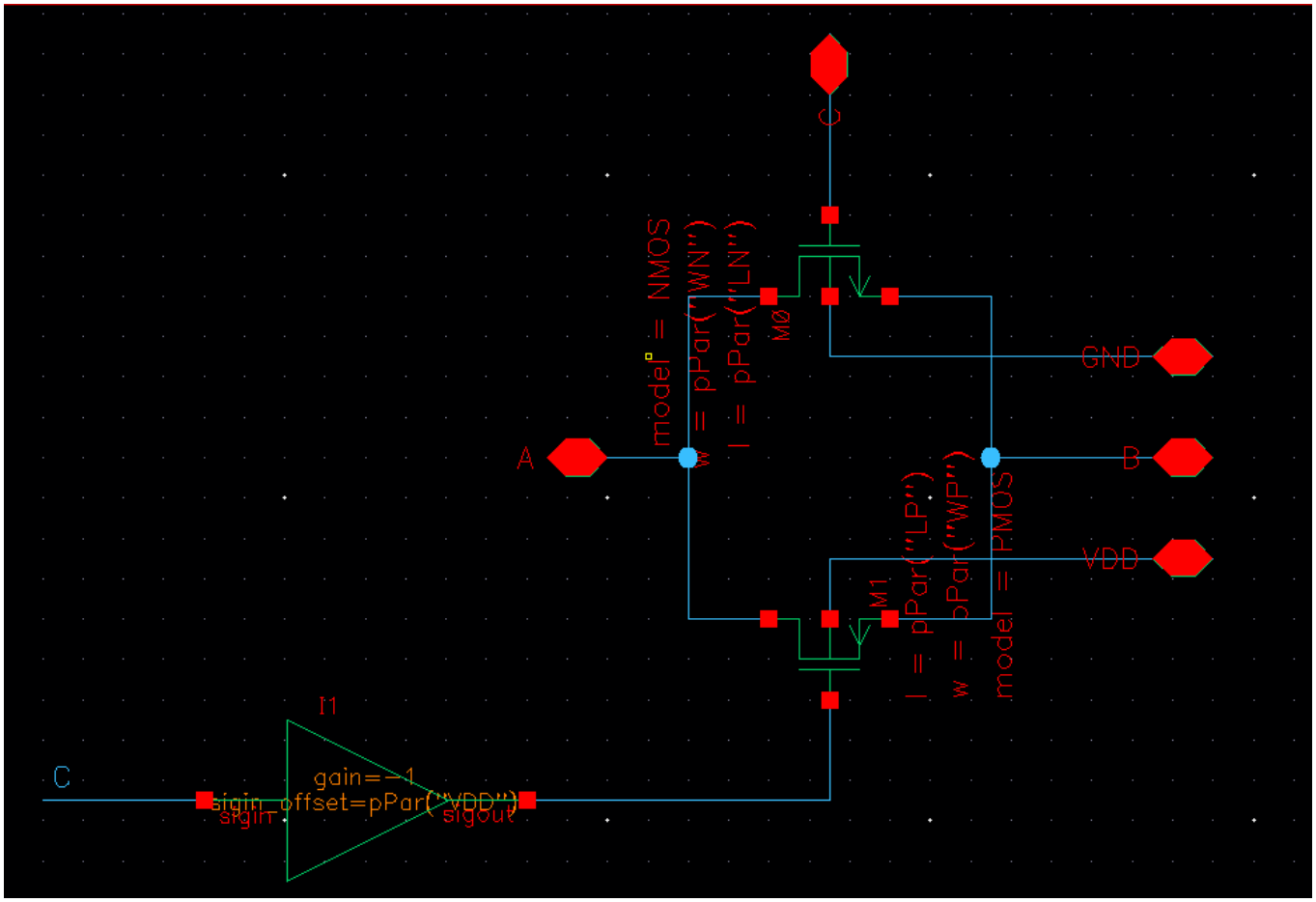
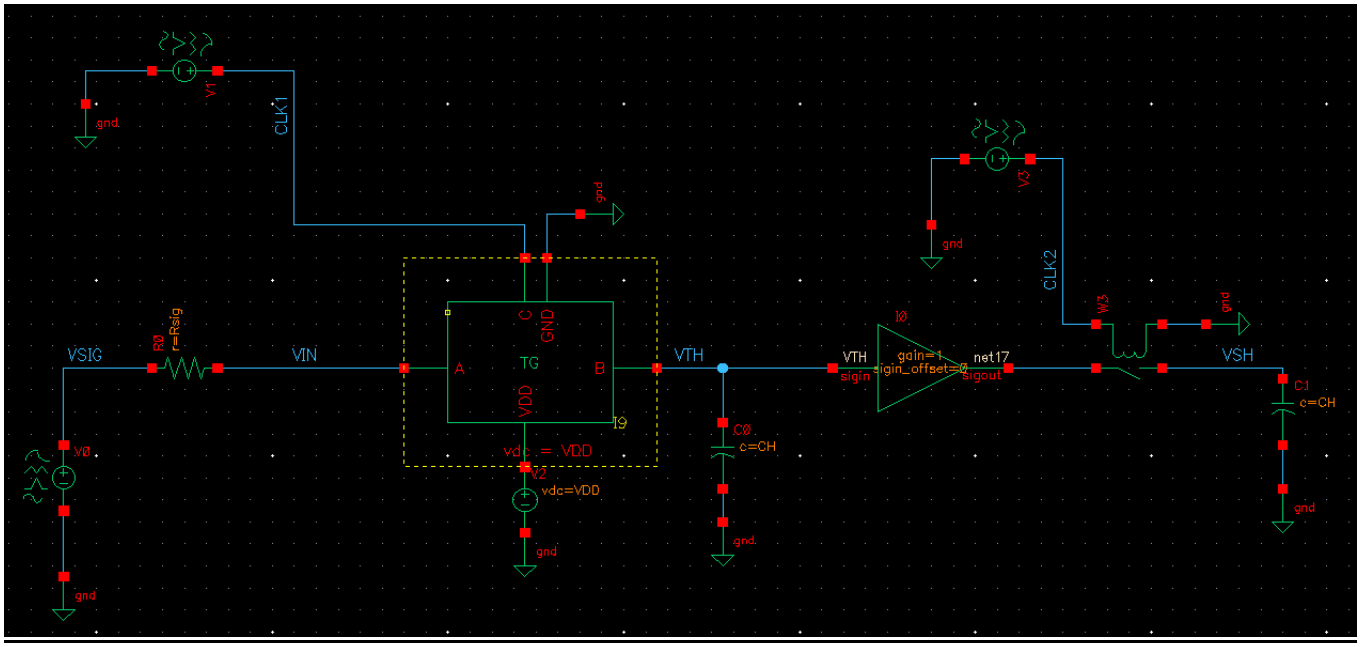
Analog Integrated System Design – Cadence Tools
Lab 04
Sample & Hold Circuits

PART 1: S&H Artifacts

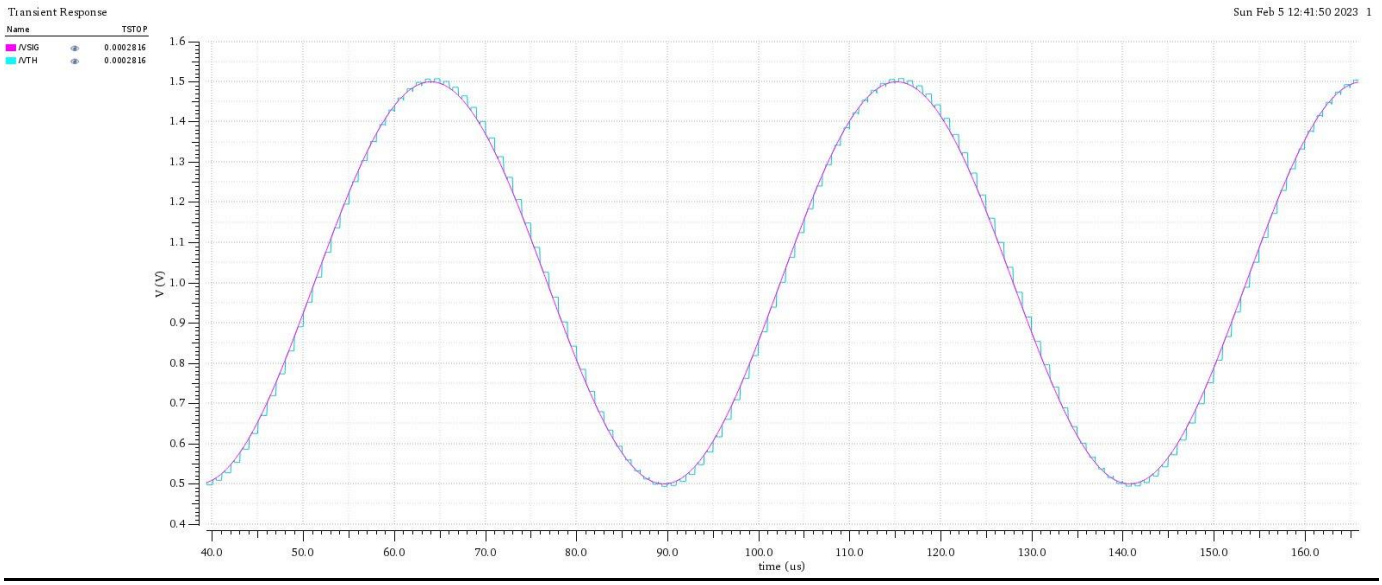
Create a new cell "tg" for a CMOS transmission gate (TG). Create schematic and symbol as shown below.



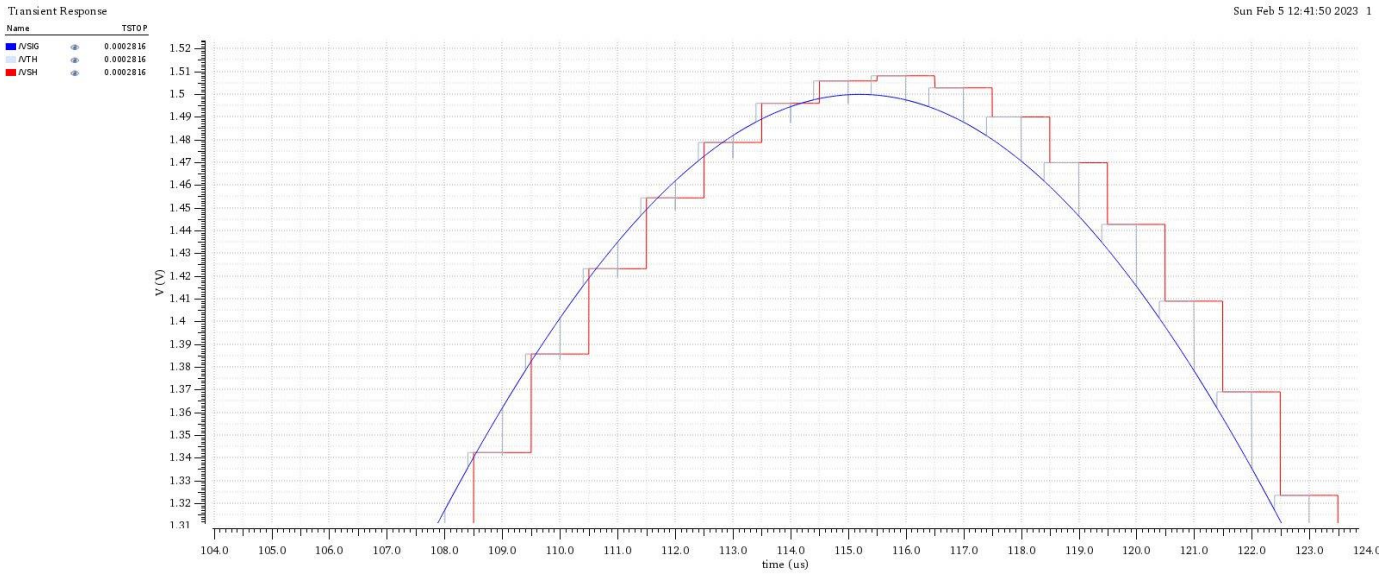
Schematic:



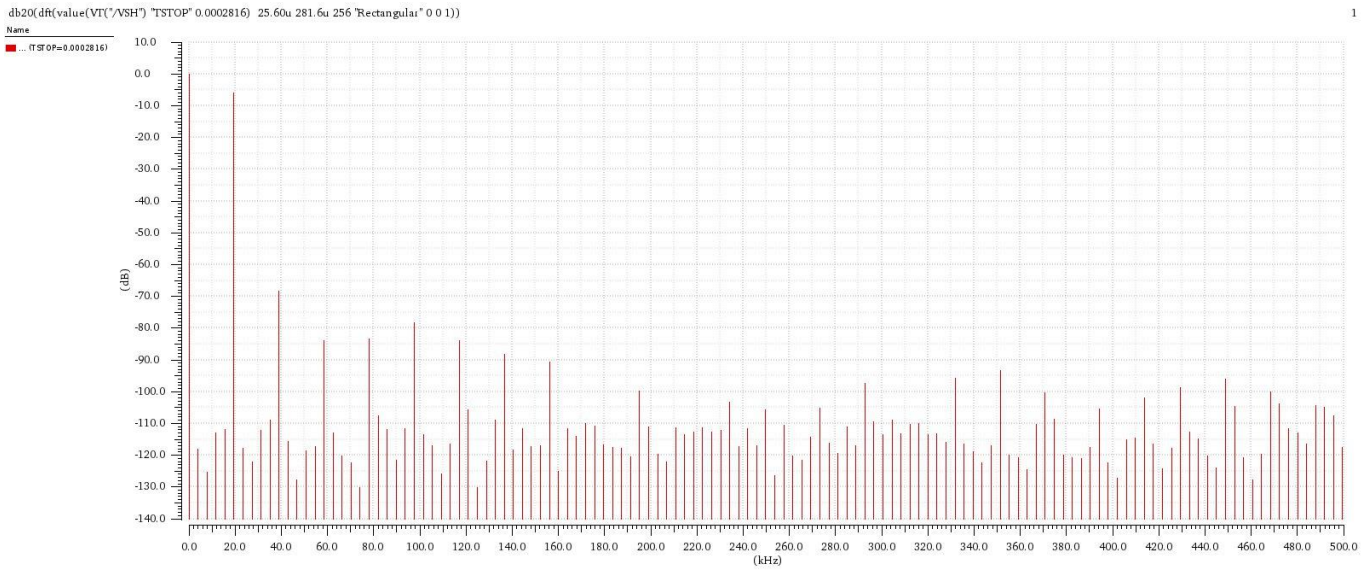
Run transient analysis. Plot VSIG and VTH overlaid. Zoom in to observe the S&H artifacts.



Zoomed in version:

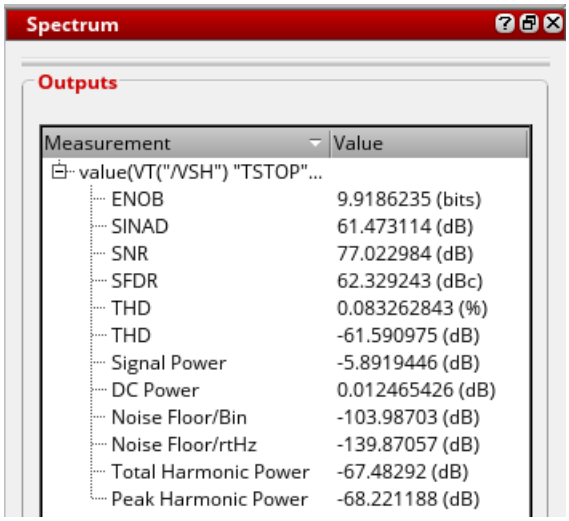


Use the Spectrum Assistant to plot FFT for VSH.

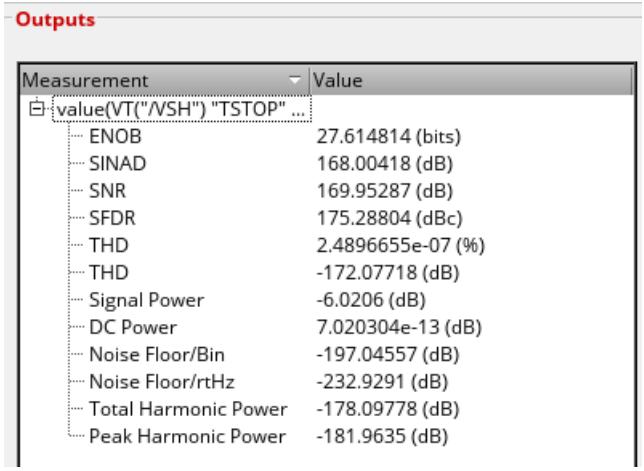


Compare the results below with Lab 02 Part 1 results in a table. Comment on the differences.

The results of this run are as shown below:



The results of lab 2 part 1 are here as shown below:



Comparison:

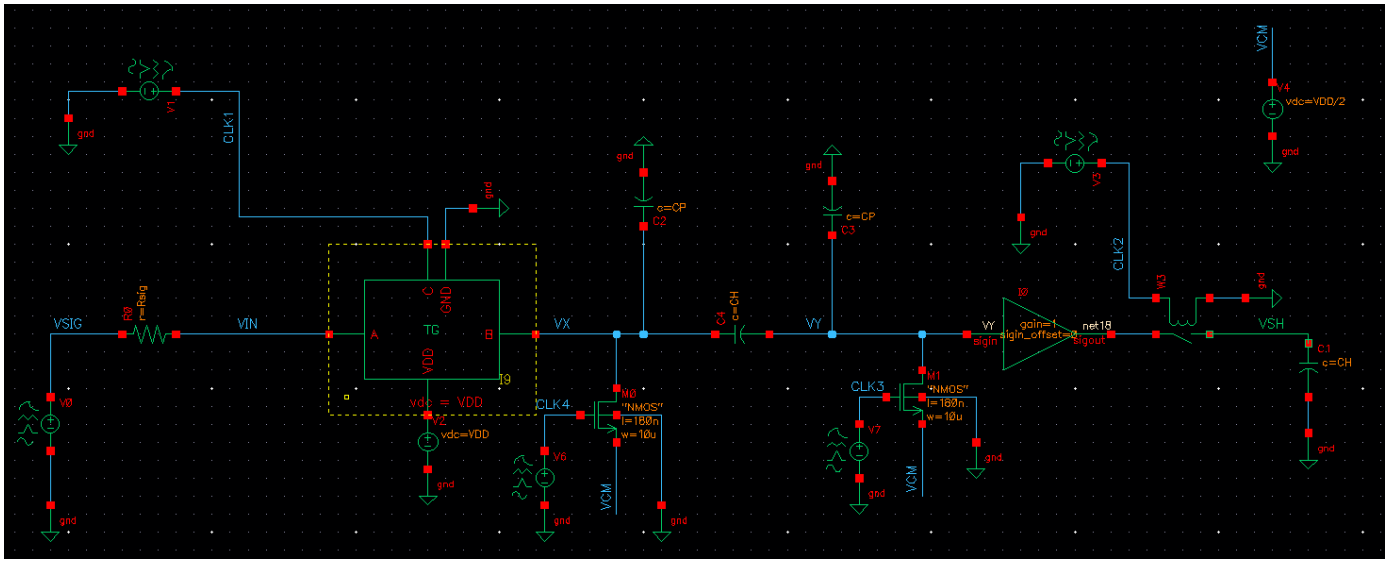
	Lab 4-part 1	Lab 2-part 1
ENOB	9.918 bits	27.6148 bits
SINAD	61.47 dB	168 dB
SNR	77 dB	169.95 dB
SFDR	62.32 dBc	175.288 dBc
THD	-61.59 dB	-172 dB
Signal power	-5.89 dB	-6.02 dB
DC power	0.012465 dB	$7.02 * 10^{-13}$ dB

Comment on the differences:

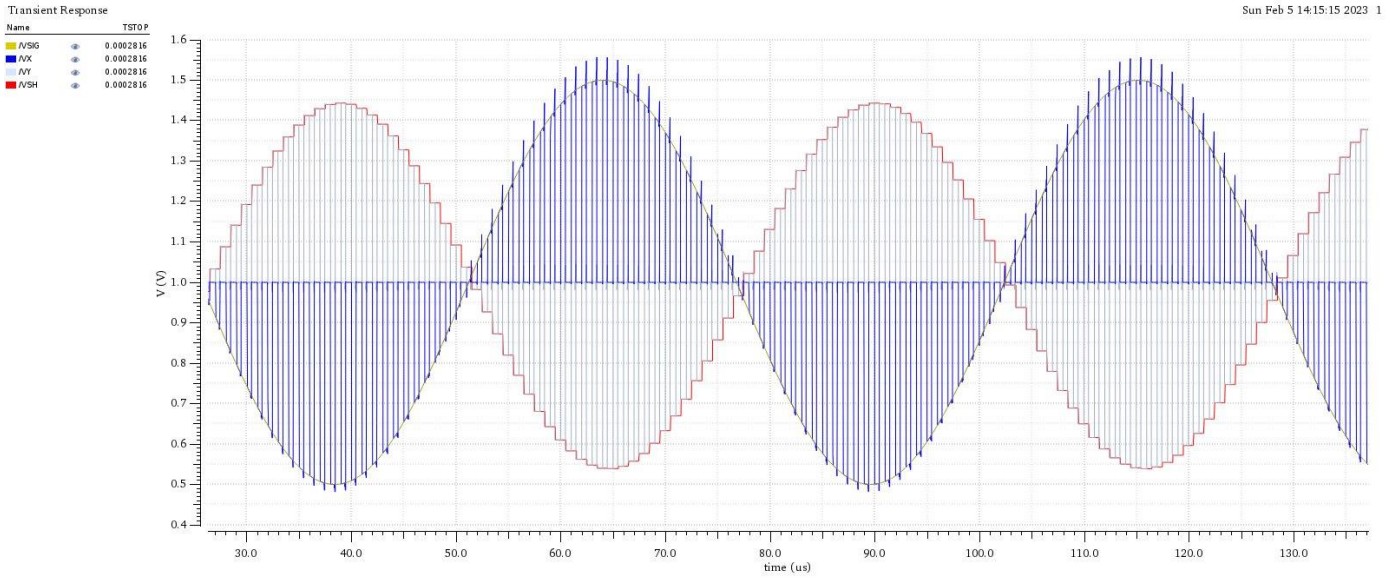
It's very clear that the ideal switch has way better efficiency in all specs where this is something quite not achievable, when we replaced the ideal switch with the TG the specs degraded.

PART 2: Bottom Plate Sampling

Schematic:

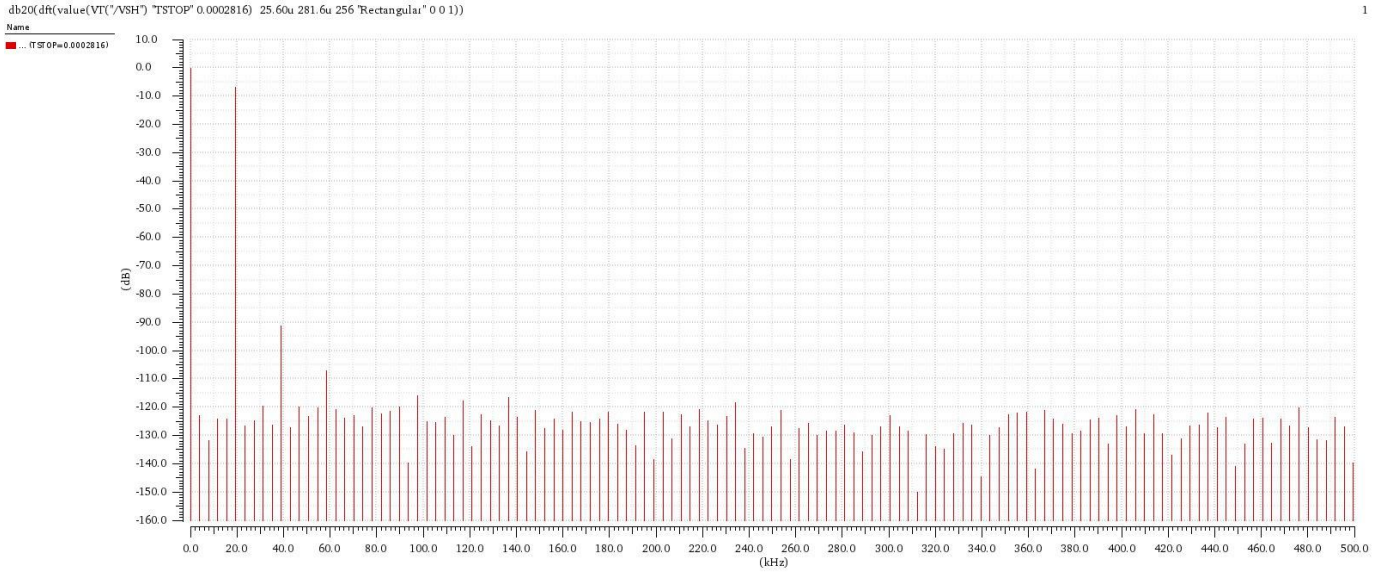


Run transient analysis. Observe the timing relations between different signals.



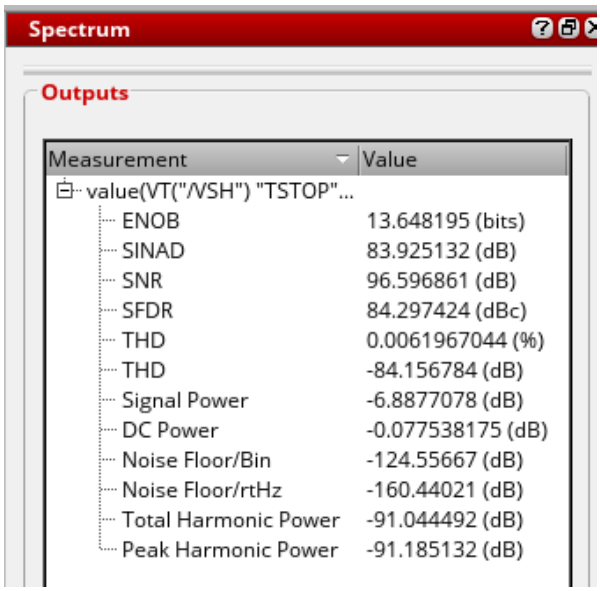
There is 180 phase shift (-ve) between VSIG and VSH, charge injection still is less independent on input signal (i.e., less non-linear) due to bottom-plate sampling.

Use the Spectrum Assistant to plot FFT.



Compare the results below with Part 1 results in a table.

The results of this run are as shown below:



	Lab 4-part 1	Lab 4-part 2
ENOB	9.918 bits	13.648195 bits
SINAD	61.47 dB	83.92 dB
SNR	77 dB	96.59 dB
SFDR	62.32 dBc	84.297 dBc
THD	-61.59 dB	-84.156 dB
Signal power	-5.89 dB	-6.88 dB
DC power	0.012465 dB	-0.0775 dB

Comment:

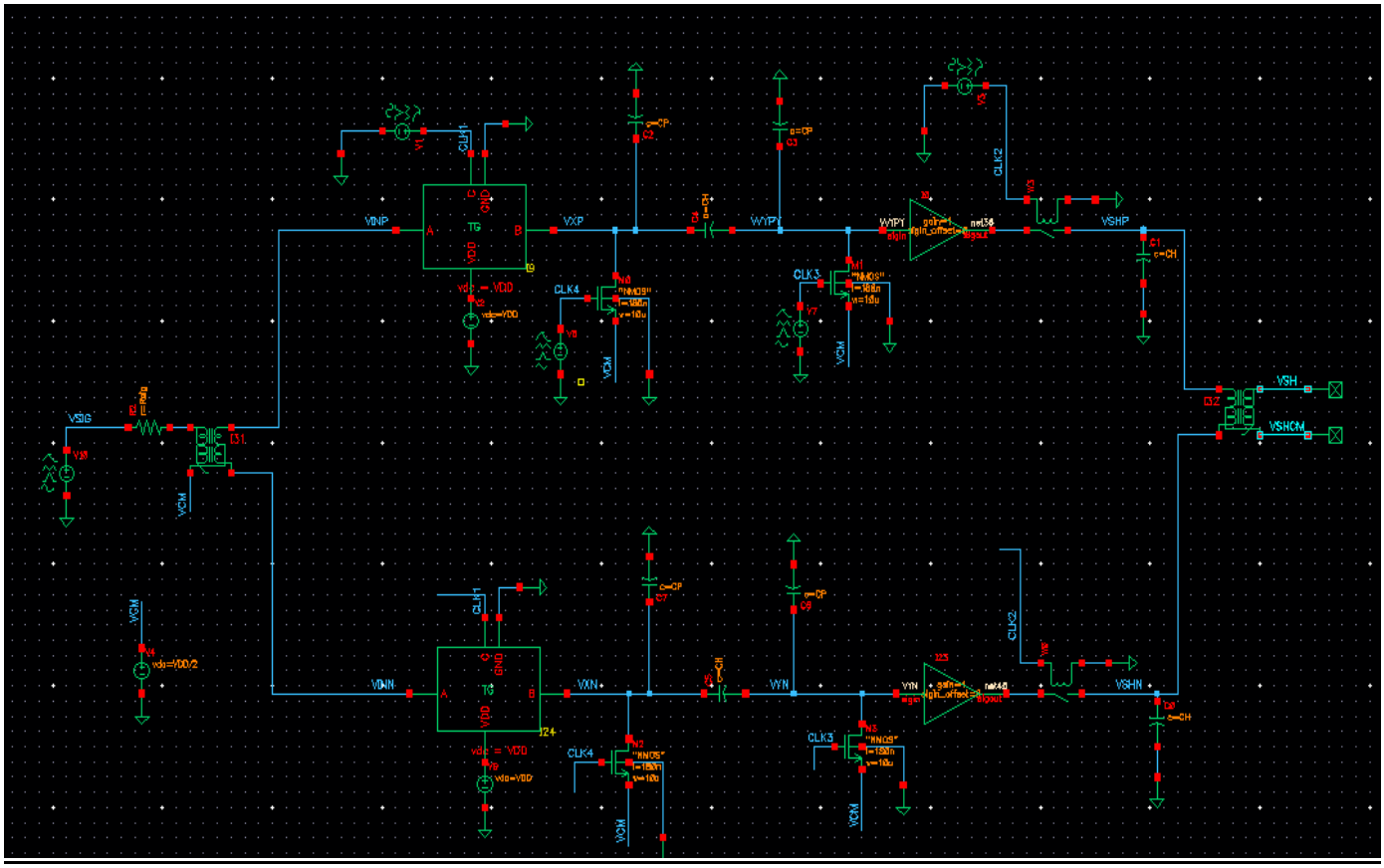
The ENOB,SINAD,SNR,SFDR and THD parameters are all improved in the bottom sampling technique.

Due to the bottom plates sampling all of the distortion is now depending on the bottom transistor which is connected to CLK3 and as the transistor Vsb is constant and equal to VDD/2 which is due to Vcm (so it's not dependent on the input voltage)

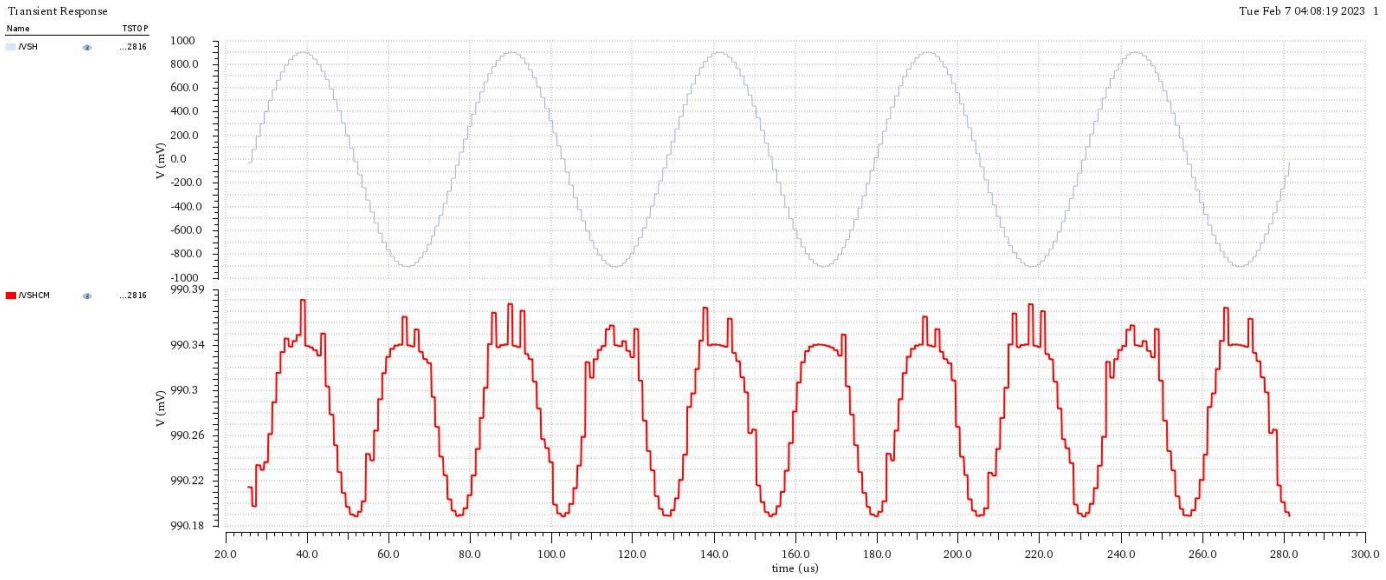
So, most of the errors will be in the form or offset errors and gain errors which are all linear errors can be easily solved and will not cause distortion to the output that's why we have lower THD and SNDR and SFDR.

PART 3: Fully Differential Operation

Schematic:



Plot the differential output and the common mode output vs time. Comment on the peak-to-peak differential output. Comment on the common output waveform

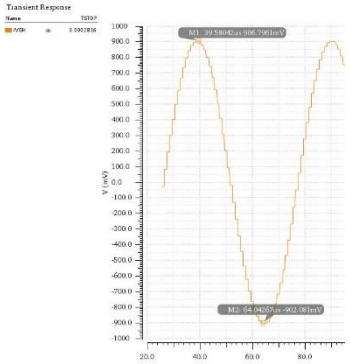


The peak to peak of the differential output is ideally 2 volts

as the Vpeak is now 1 volt however the peak-to-peak voltage

is around 1.8 V not 2 volt and this is due to the parasitic Cp

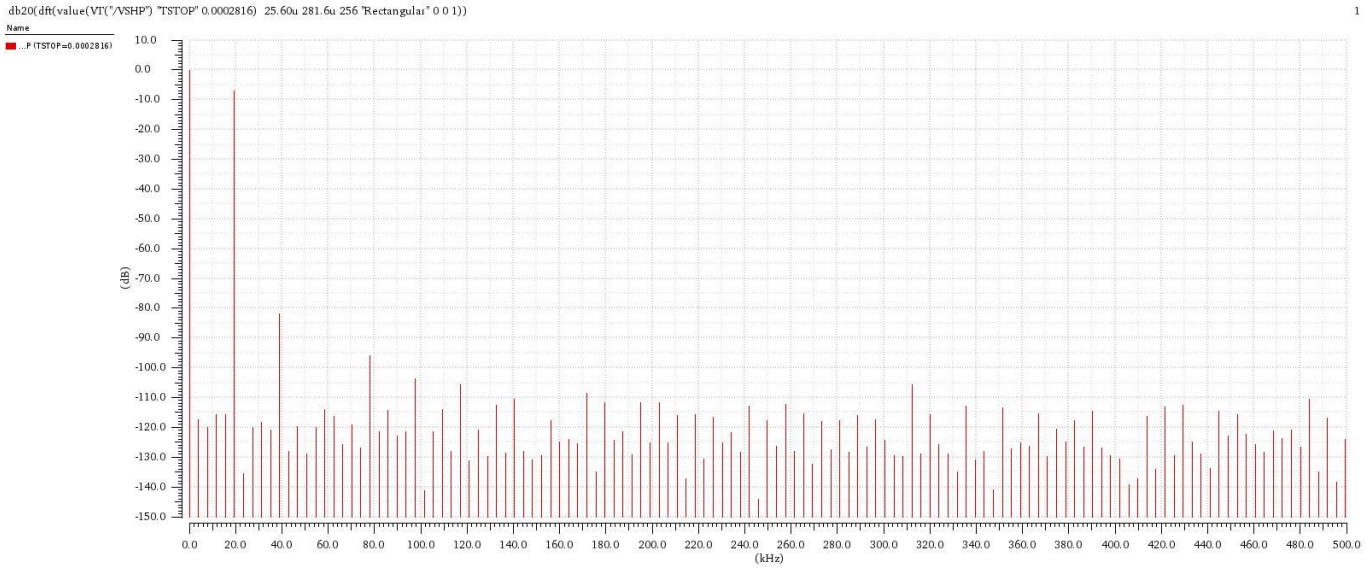
it's less than 2 volts due to attenuation.



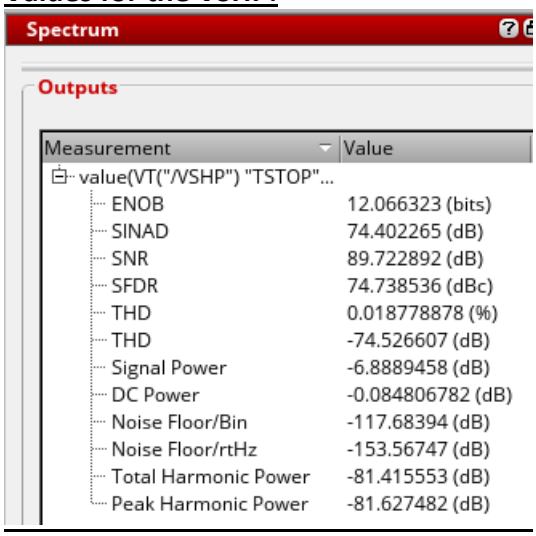
The common mode output is almost a dc 1 volt as it has very small variations

This 1 volt is due to the common mode dc voltage at the transistors at clock 3 and 4 which makes to common mode voltage at 1 volt.

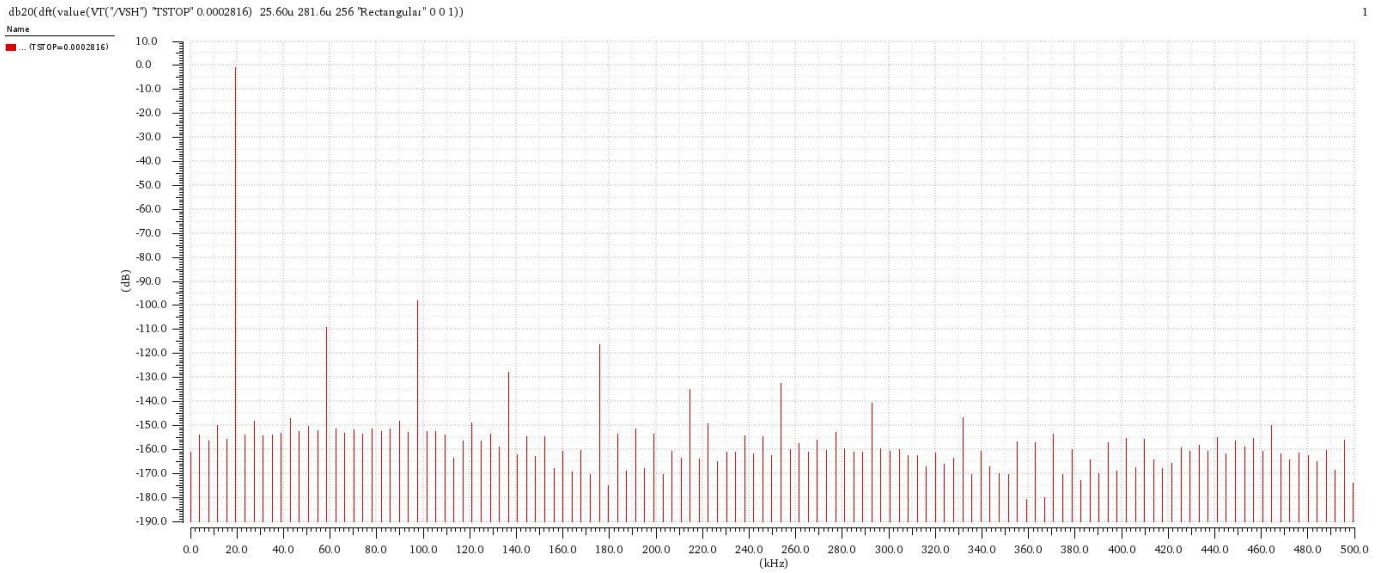
Use the Spectrum Assistant to plot FFT of the positive half output VSHP.



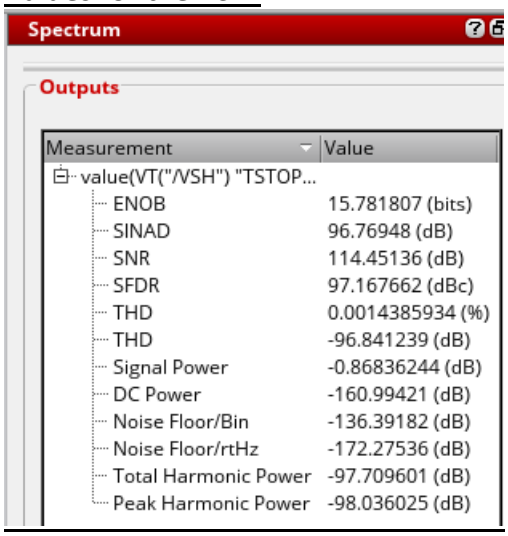
Values for the VSHP:



Use the Spectrum Assistant to plot FFT of the VSH.



Values for the VSH:



Compare the 2nd harmonic power in VSHP and VSH spectrum. Compare the results below for VSHP and VSH in a table. Comment on the differences.

	VSHP	VSH
ENOB	12.06 bits	15.7818 bits
SINAD	74.4 dB	96.769 dB
SNR	89.72 dB	114.45 dB
SFDR	74.738 dBc	97.167 dBc
THD	-74.52 dB	0.0014 dB
Signal power	-6.8889 dB	-0.868 dB
Dc power	-0.0848 dB	-160.99 dB

Second harmonic power in VSHP is large where it's around -80 dB
while the second harmonic power in VSH is very low which is around -150 dB

Comment:

The effective number of bits in VSH is larger than VSHP

It has better SFDR and better SNR and SINAD