Analog Integrated System Design
Lab 03
Data Converters Specifications

ADCs Specifications

No. of bits >> 12 bits

Sample rate >> more than 1Msps

No. of channels >> 1

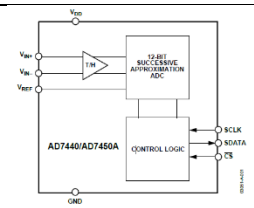
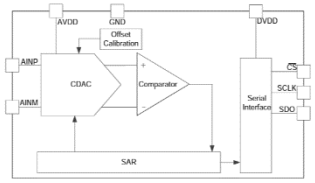
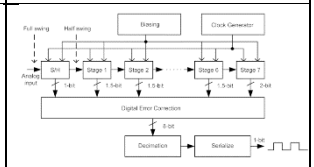
Input type >> Differential

Max DNL >> less than 1 LSB

Max INL >> less than 1 LSB

Power consumption >> minimum

ADCs Comparison:

#	Name	ADI (AD7440 Version B)	TI(ADS7044)	JSSC Paper
1	Architecture	SAR	SAR	pipelined
2	Block diagram			
3	Price ($)	2.61	2.19	-
4	Min power supply (V)	3 v	1.8 v but for INL spec we will use 3 v	1.8
5	Peak-to-peak input range (V)	4	6	2.4
6	Power consumption at 1 MSps (mW)	4	0.9	18.4
7	Max DNL (LSB)	0.5	0.5	0.26

8	Max INL (LSB)	0.5	0.7	0.72
9	ENOB (bit)	9.841	11.502	10.399
10	SNR (dB)	61.4	71	64.245
11	SINAD (dB)	61	71	64
12	SFDR (dB)	76	85	76.6
13	Digital output format (parallel, serial, etc.)	Serial	Serial	parallel
14	Internal reference (Yes/No)?	No	Yes	No
15	Internal sampling clock (Yes/No)?	Yes	Yes	-
16	Walden FoM (pJ/step)	4.361378	0.31	13.627
17	Schreier FoM (dB)	142.369	158.44	138.586

For the FoM

$$FoM_w = \frac{P_{adc}}{2^{ENOB} * f_s}$$

$$FoM_{sc} = SNR + 10\log_{10}(\frac{\frac{f_s}{2}}{P_{adc}})$$