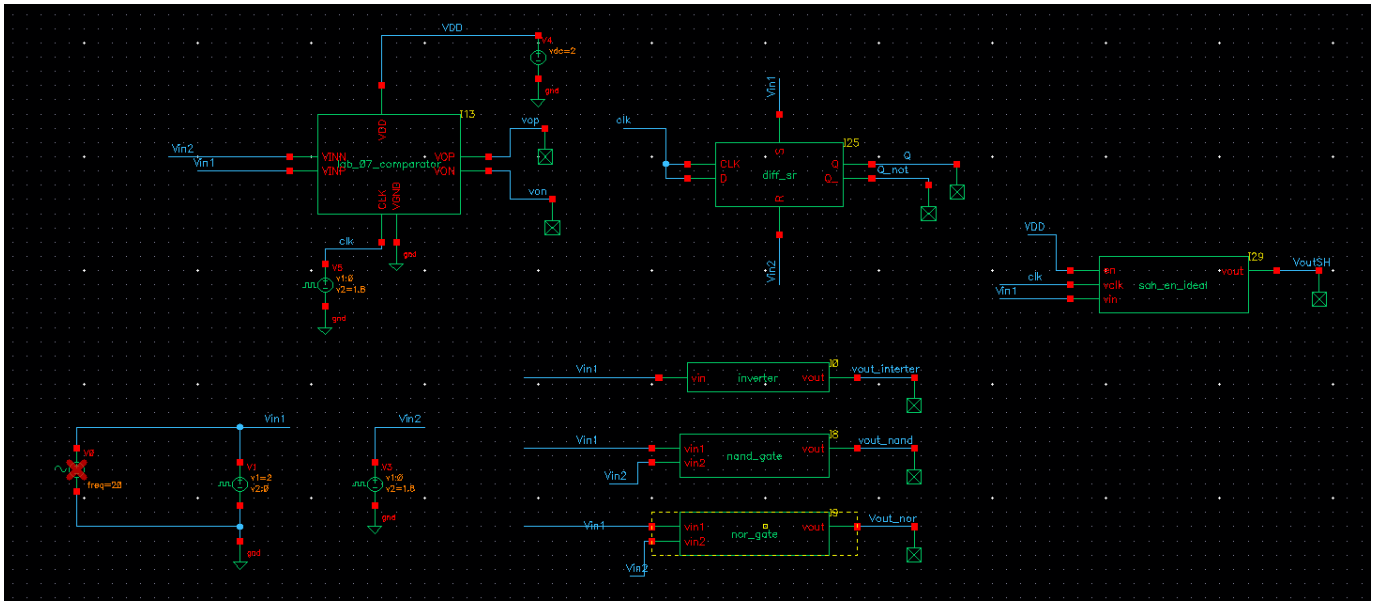
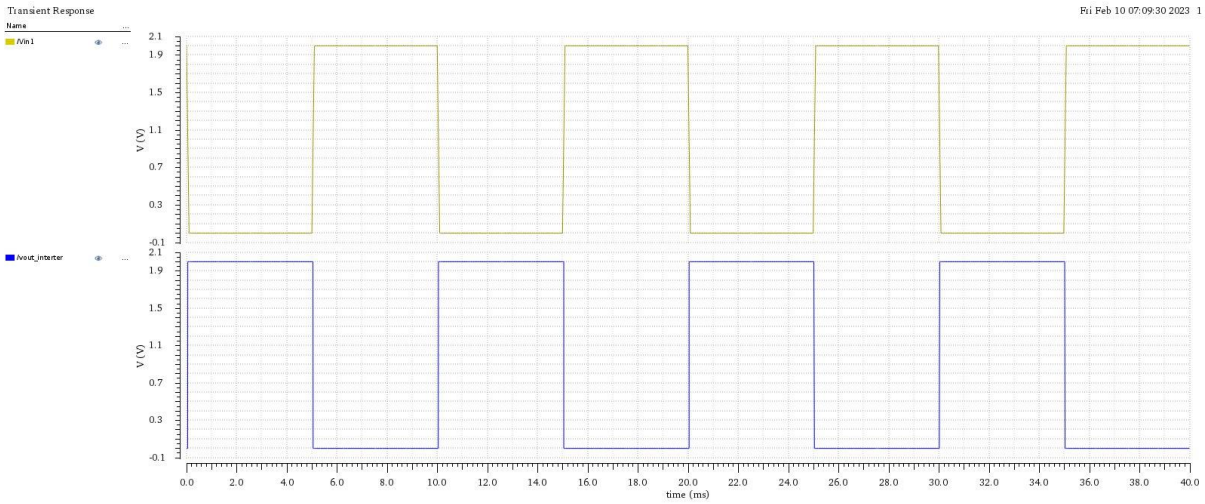
Analog Integrated System Design – Cadence Tools
Lab 08 (Final-Project)
SAR ADC

PART 1: Verilog-A Behavioural Models

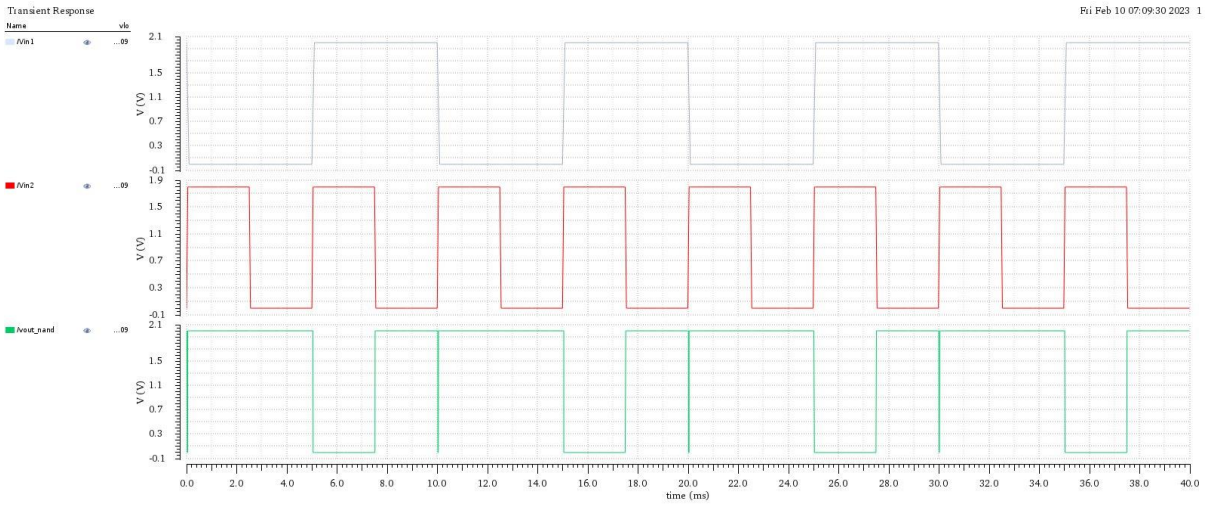
Create appropriate testbenches to verify the operation of the Verilog-A models. Report transient simulation results showing proper operation of each block.



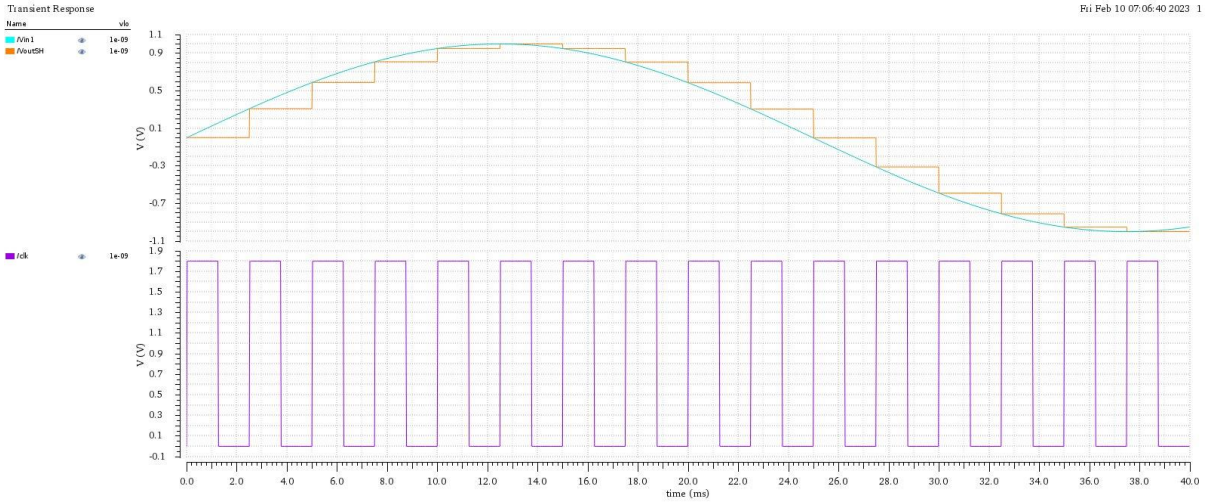
Inverter:



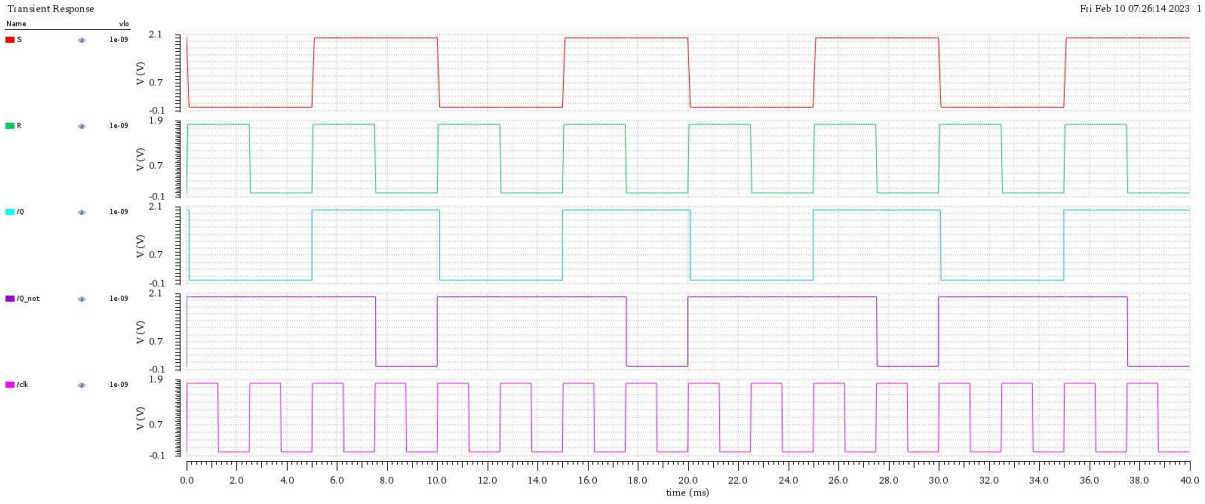
NAND:


Transient Response
Fri Feb 10 07:09:30 2023 1
Name
/Vin1
/Vin2
/Vout_nand
V (V)
time (ms)

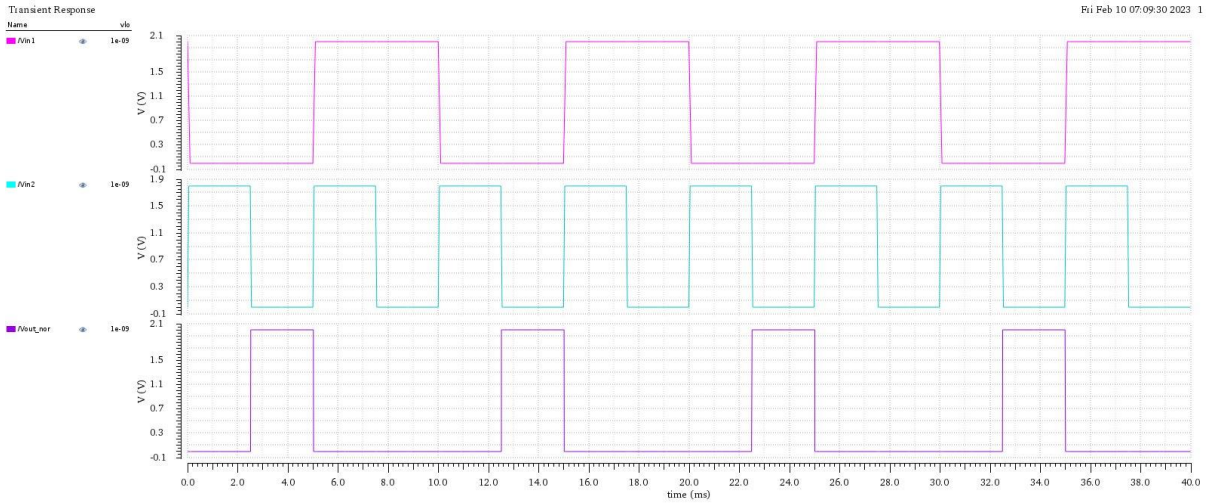
SAH:


Transient Response
Fri Feb 10 07:06:40 2023 1
Name
/Vin1
/VoutSH
/clk
V (V)
time (ms)

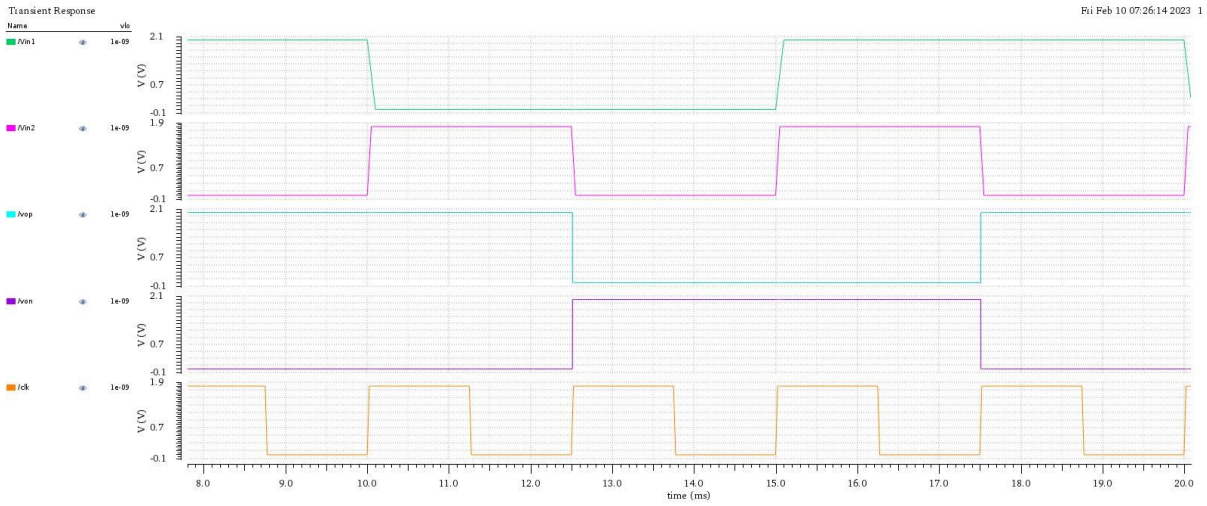
SR:


Transient Response
Fri Feb 10 07:26:14 2023 1
Name
S
R
/Q
/Q_not
/clk
V (V)
time (ms)

NOR:

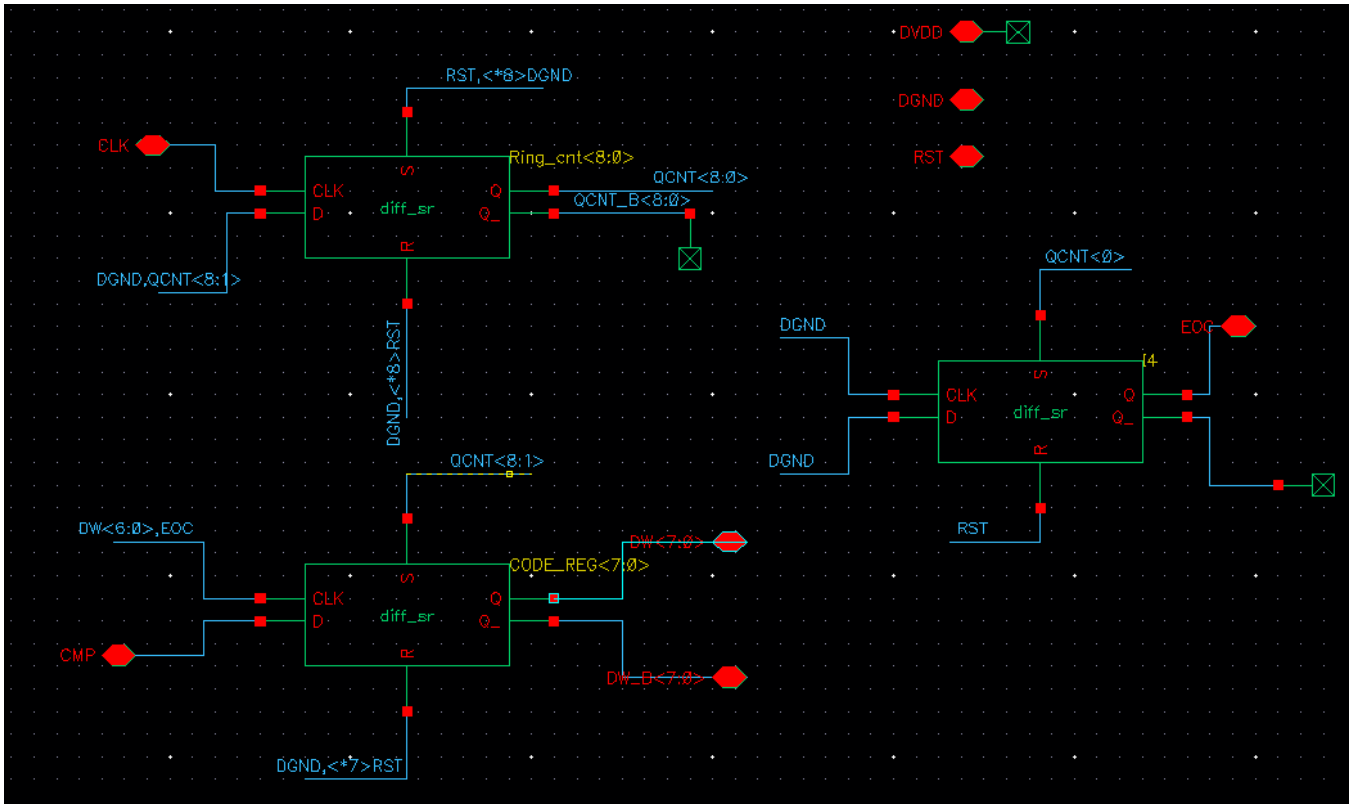


COMP:

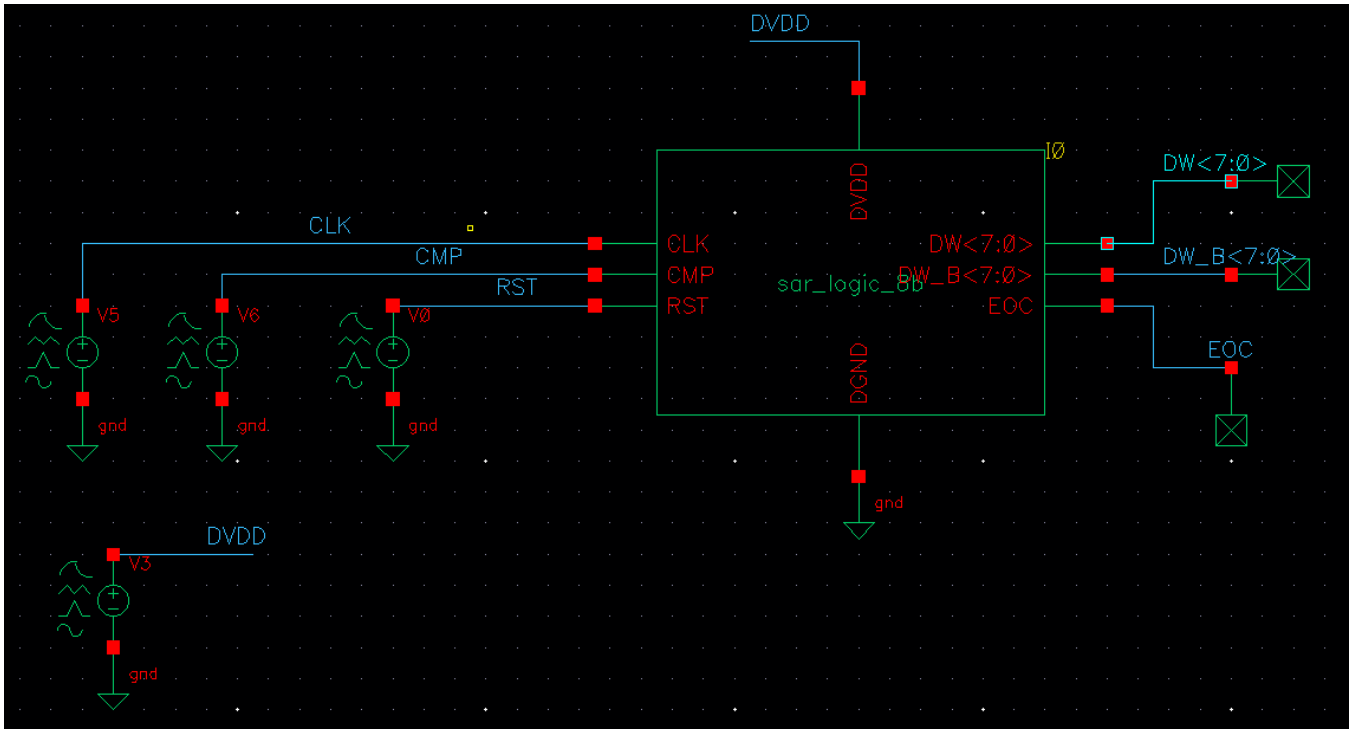


PART 2: SAR Logic

Create the schematic of SAR logic as shown below

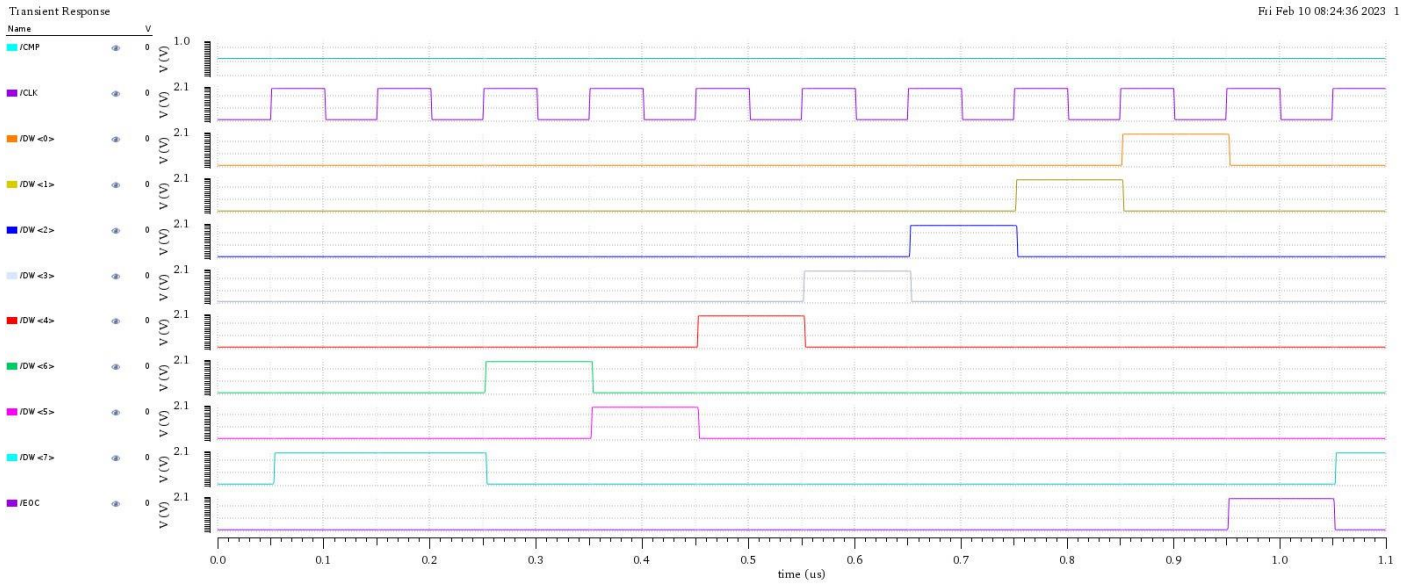


Create a testbench to verify SAR logic operation. Set FCLK = (NBIT + 2) * FS, where NBIT = 8 and FS = 1MHz.



Report transient simulation results for the ring counter output, the code register output, and the EOC signal for the following cases:

a. CMP is all zeros

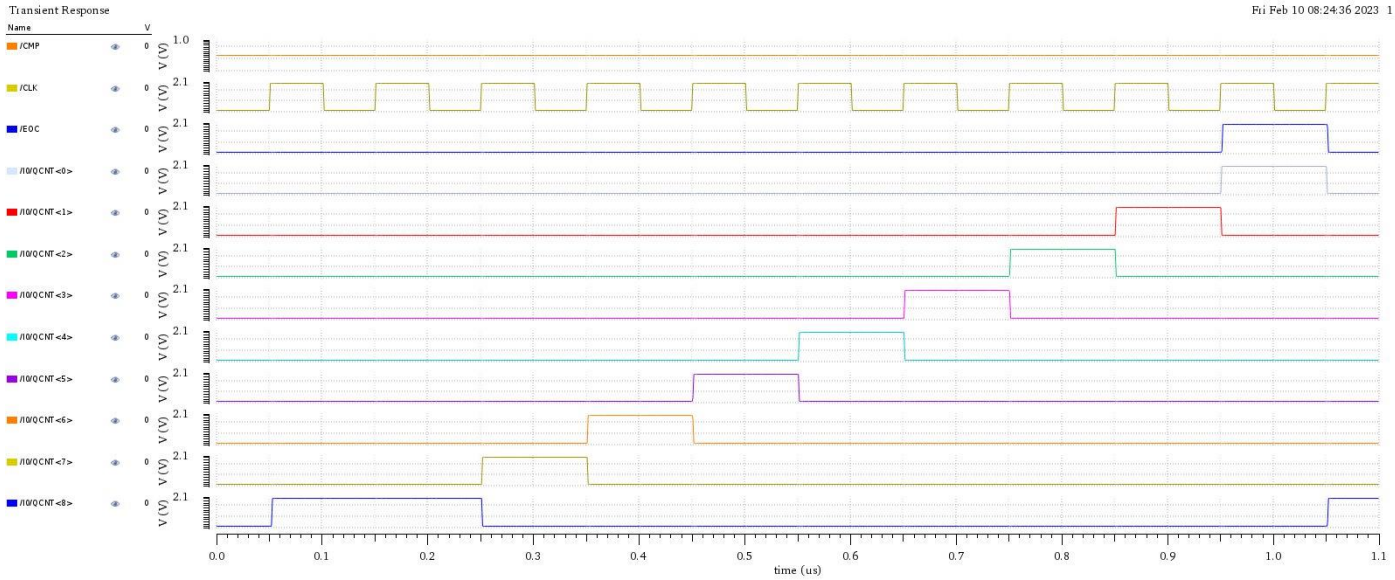


note that at the end of conversion all outputs are to zero because the compare is zero

the above photo is exactly the same as the table required to fill as it shows the value of each DW signal in each clock

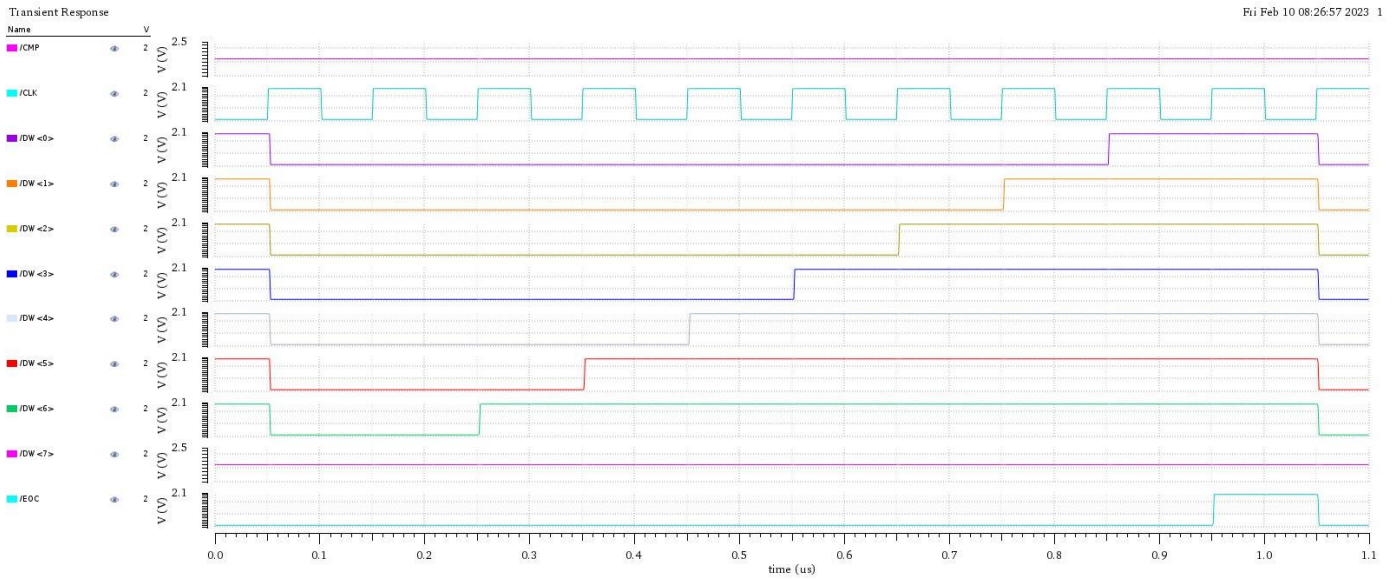
Support your explanation by filling the state table below.

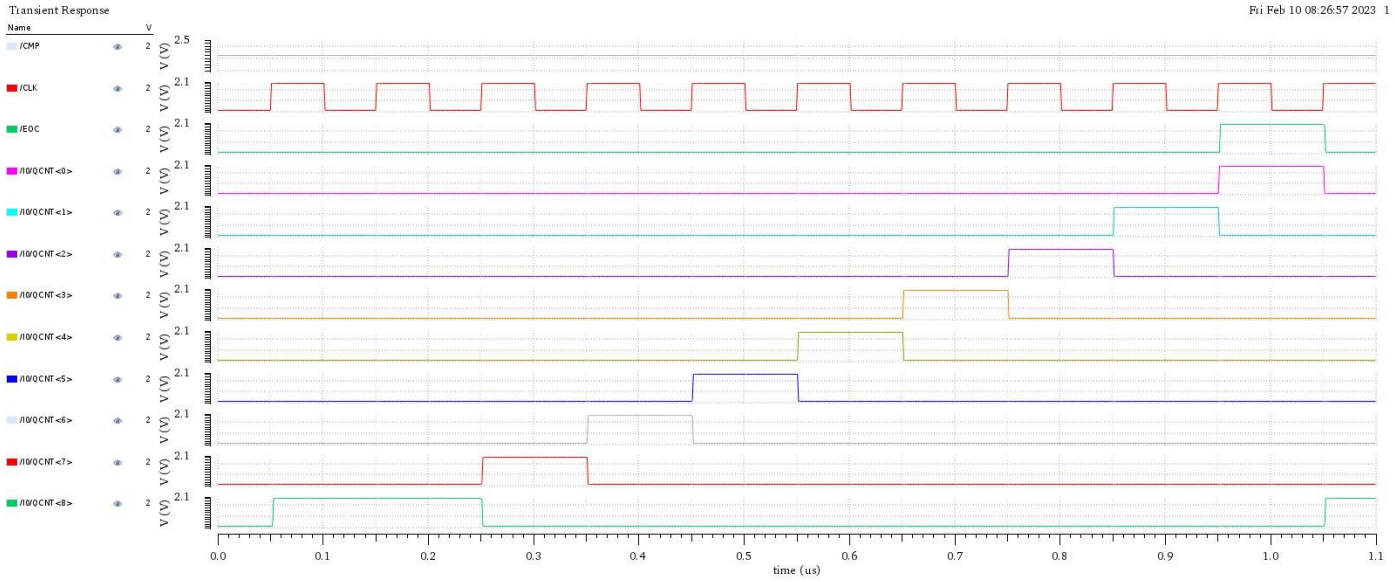
CLK	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	CMP
1)Reset	0	0	0	0	0	0	0	0	-
2	1	0	0	0	0	0	0	0	B7
3	0	1	0	0	0	0	0	0	B6
4	0	0	1	0	0	0	0	0	B5
5	0	0	0	1	0	0	0	0	B4
6	0	0	0	0	1	0	0	0	B3
7	0	0	0	0	0	1	0	0	B2
8	0	0	0	0	0	0	1	0	B1
9	0	0	0	0	0	0	0	1	B0
10	0	0	0	0	0	0	0	0	-



Notice that QCNT is independent on the input.

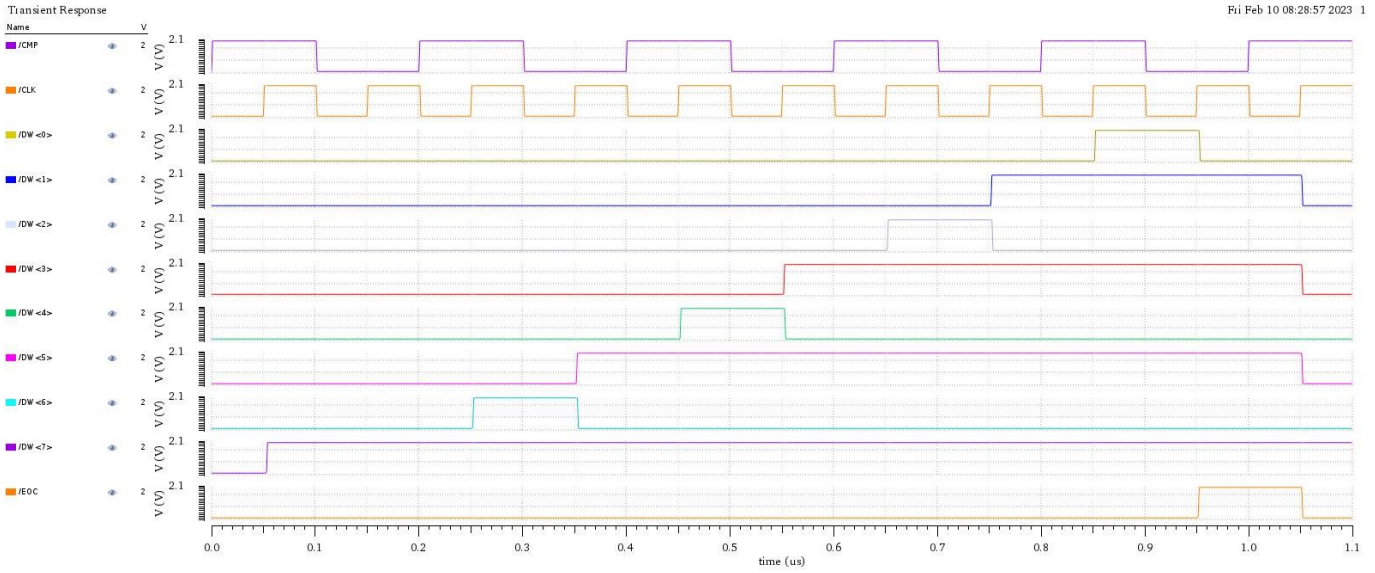
b. CMP is all ones



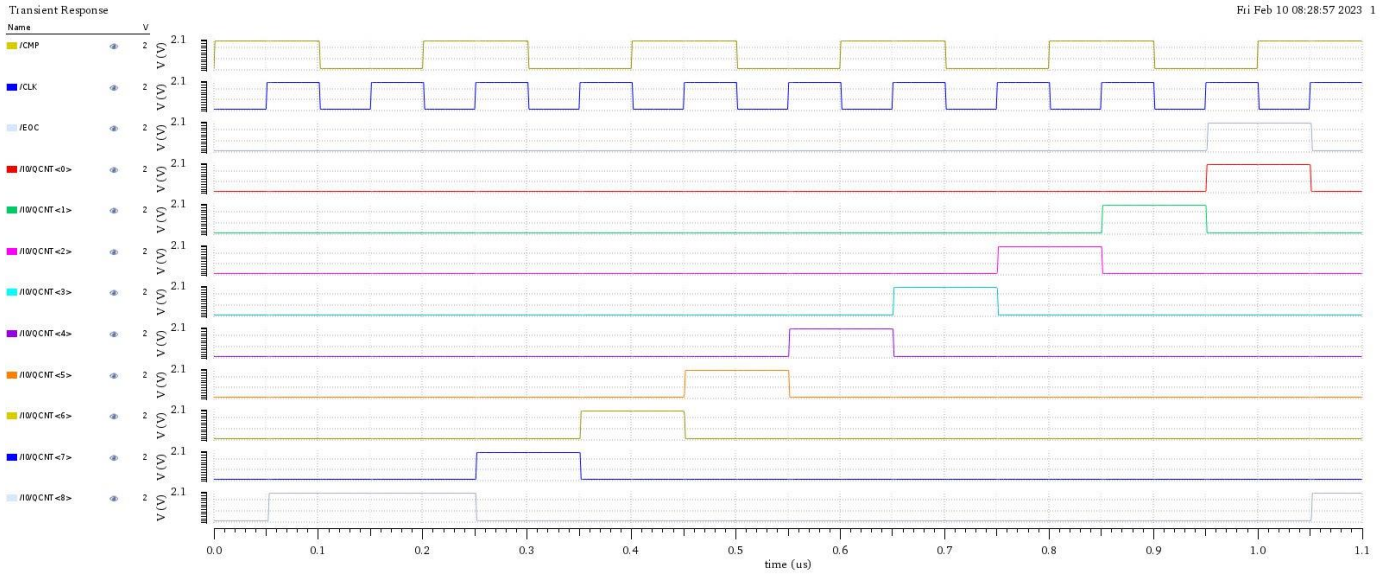


CLK	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	CMP
1)Reset	0	0	0	0	0	0	0	0	-
2	1	0	0	0	0	0	0	0	B7
3	1	1	0	0	0	0	0	0	B6
4	1	1	1	0	0	0	0	0	B5
5	1	1	1	1	0	0	0	0	B4
6	1	1	1	1	1	0	0	0	B3
7	1	1	1	1	1	1	0	0	B2
8	1	1	1	1	1	1	1	0	B1
9	1	1	1	1	1	1	1	1	B0
10	1	1	1	1	1	1	1	1	-

c. CMP is alternating ones and zero



CLK	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DW0	CMP
1)Reset	0	0	0	0	0	0	0	0	-
2	1	0	0	0	0	0	0	0	B7
3	1	1	0	0	0	0	0	0	B6
4	1	0	1	0	0	0	0	0	B5
5	1	0	1	1	0	0	0	0	B4
6	1	0	1	0	1	0	0	0	B3
7	1	0	1	0	1	1	0	0	B2
8	1	0	1	0	1	0	1	0	B1
9	1	0	1	0	1	0	1	1	B0
10	1	0	1	0	1	0	1	0	-

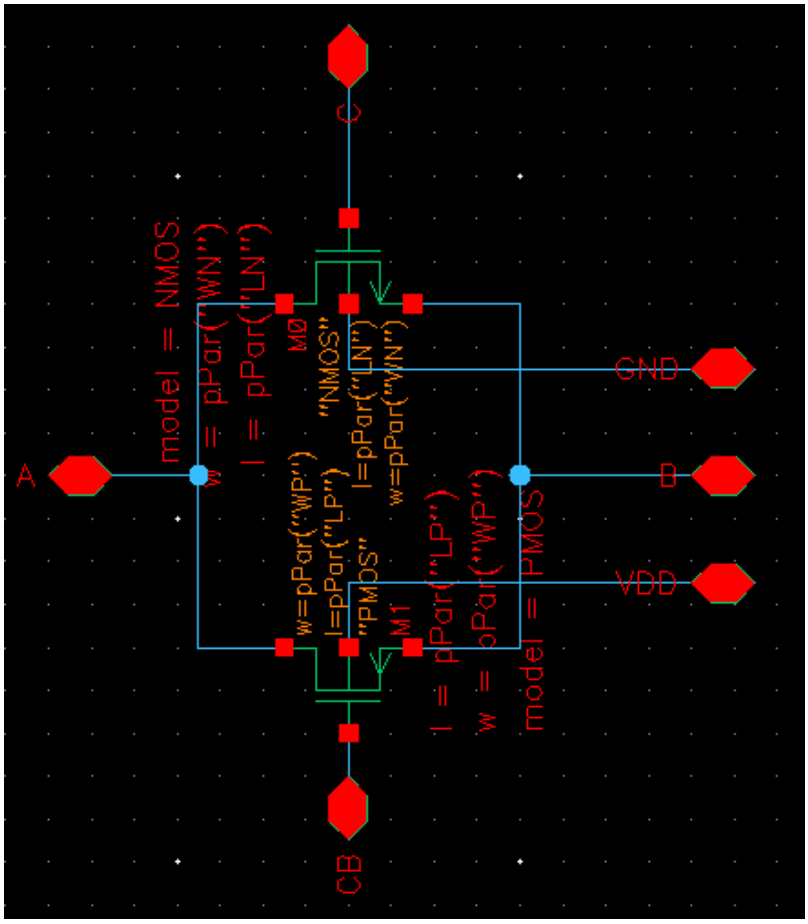


Briefly explain in your own words how does this design work and how does it implement the successive approximation algorithm

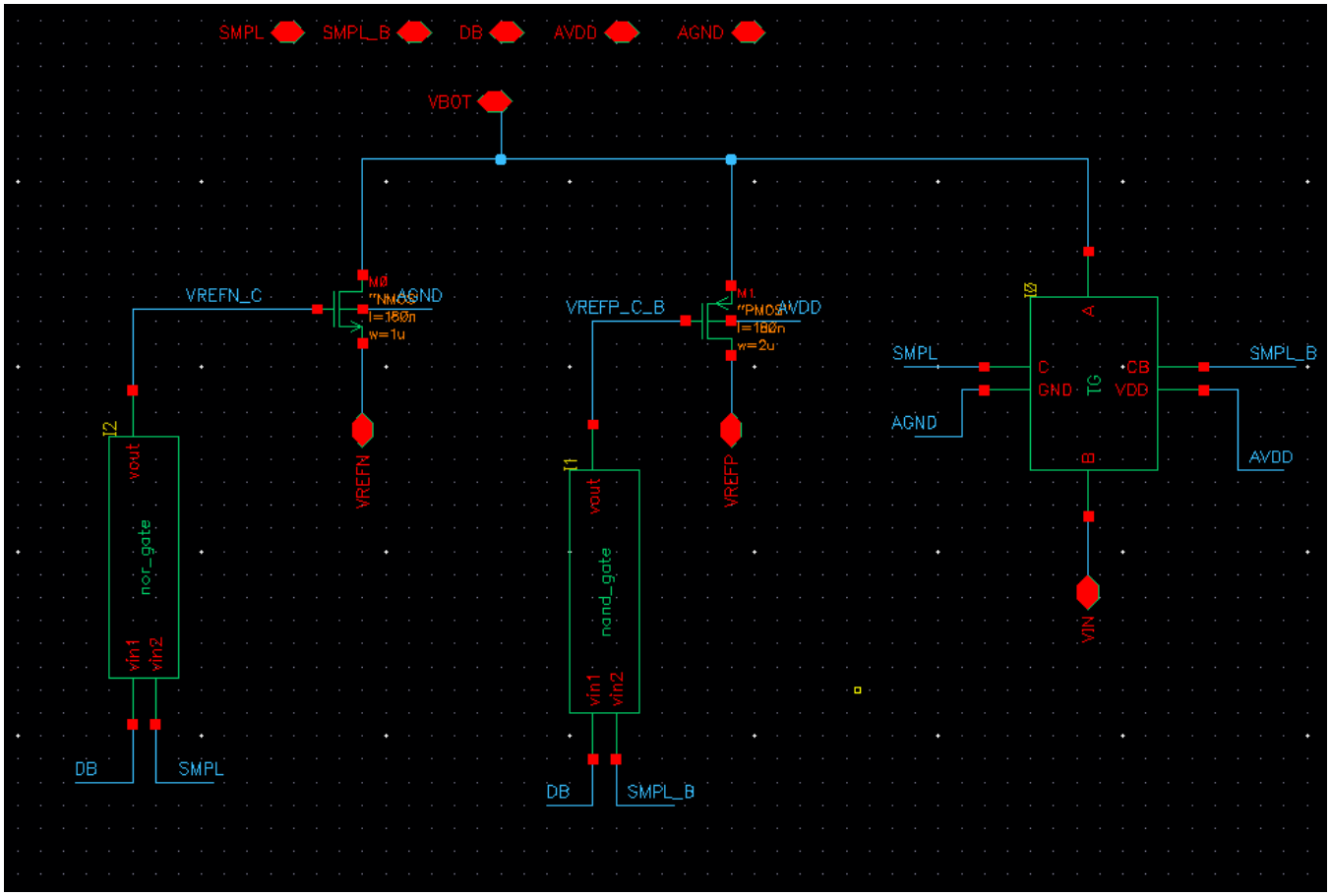
We used a sample and hold circuit to capture the input voltage of the ADC and hold it as long as needed , The input voltage then compared to the DAC output if te voltages is equal then the counter value corresponds the analog input voltage if not , the counter (connected to the DAC input) value is changed and compared again and so on , the SAR algorithm is just like the binary search algorithm as the initial value of the counter is half the range of the ADC and the value is changed by half the weight each bit added or removed

PART 3: SAR ADC Testbench

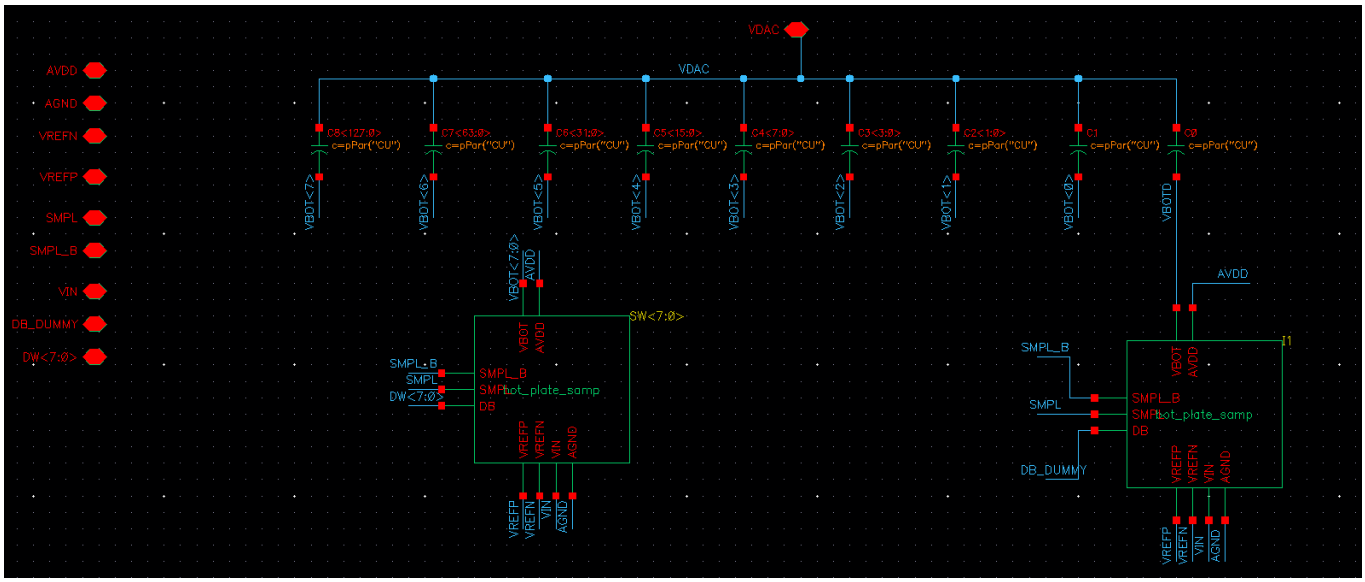
Transmission gate schematic.



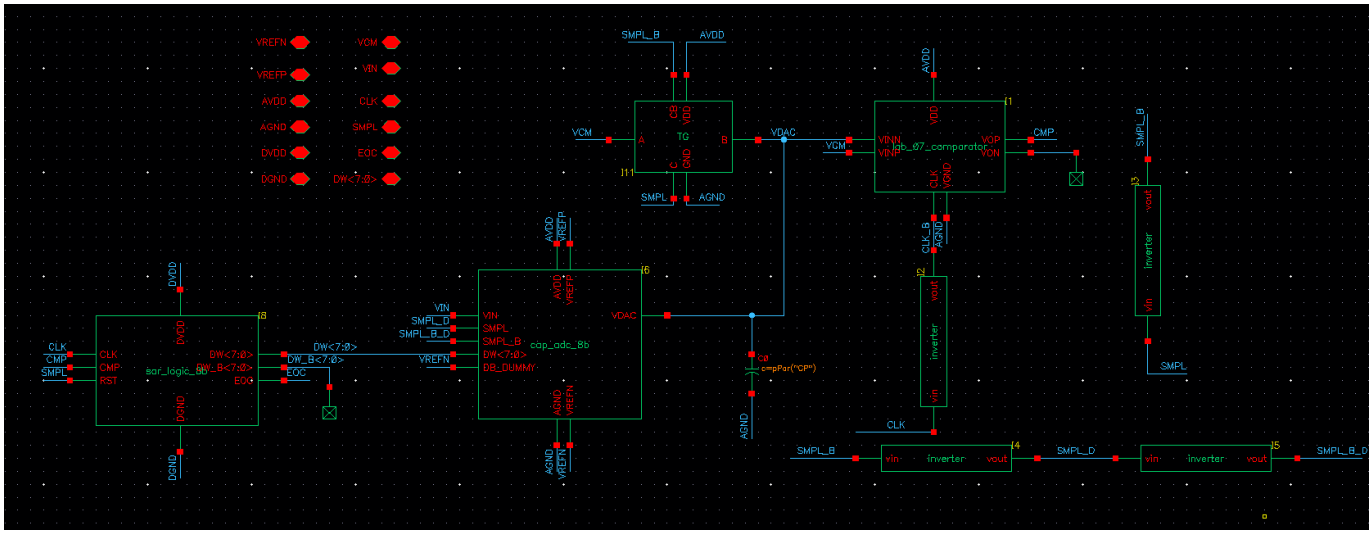
Bottom-plate switch schematic.



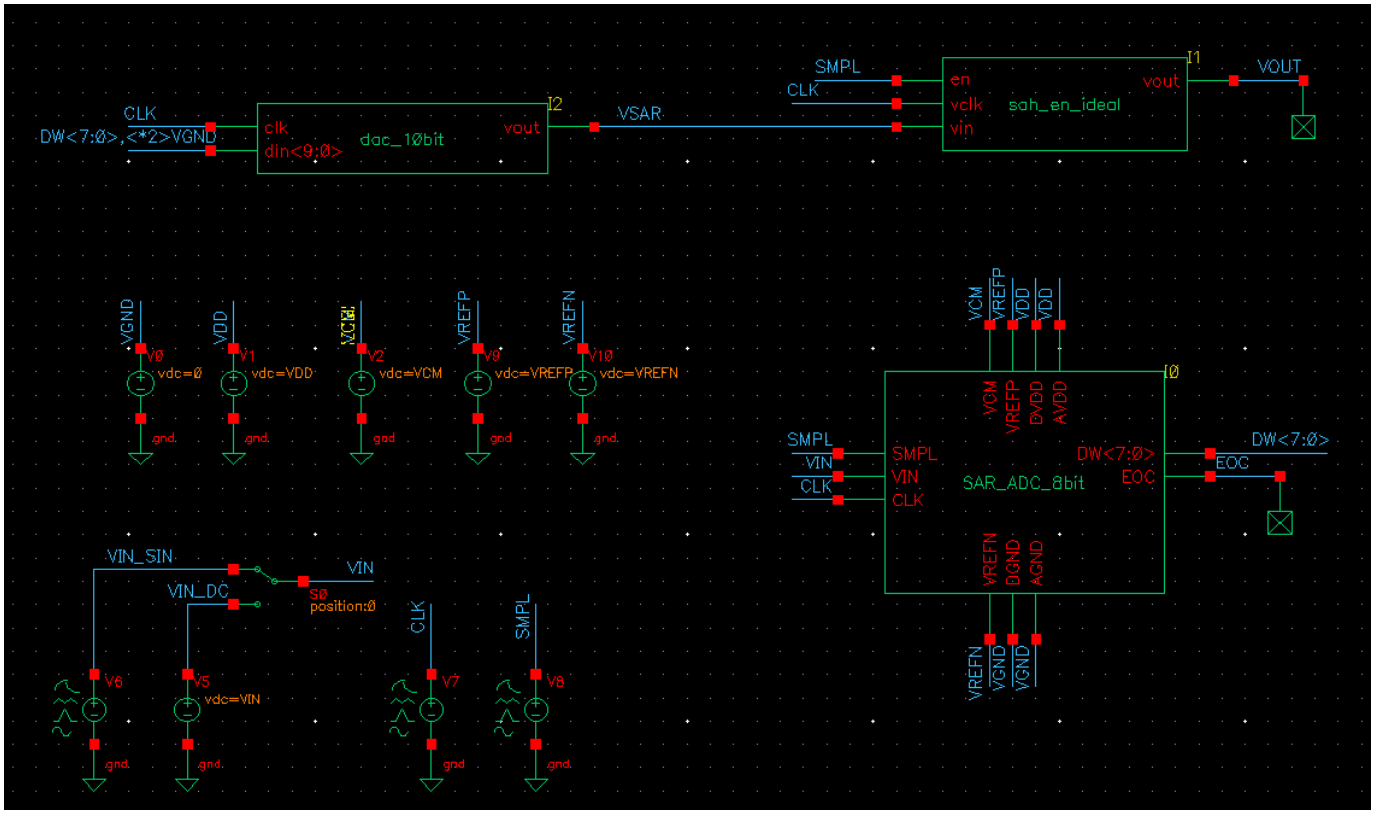
Capacitive DAC schematic.



SAR ADC schematic.



SAR ADC testbench.



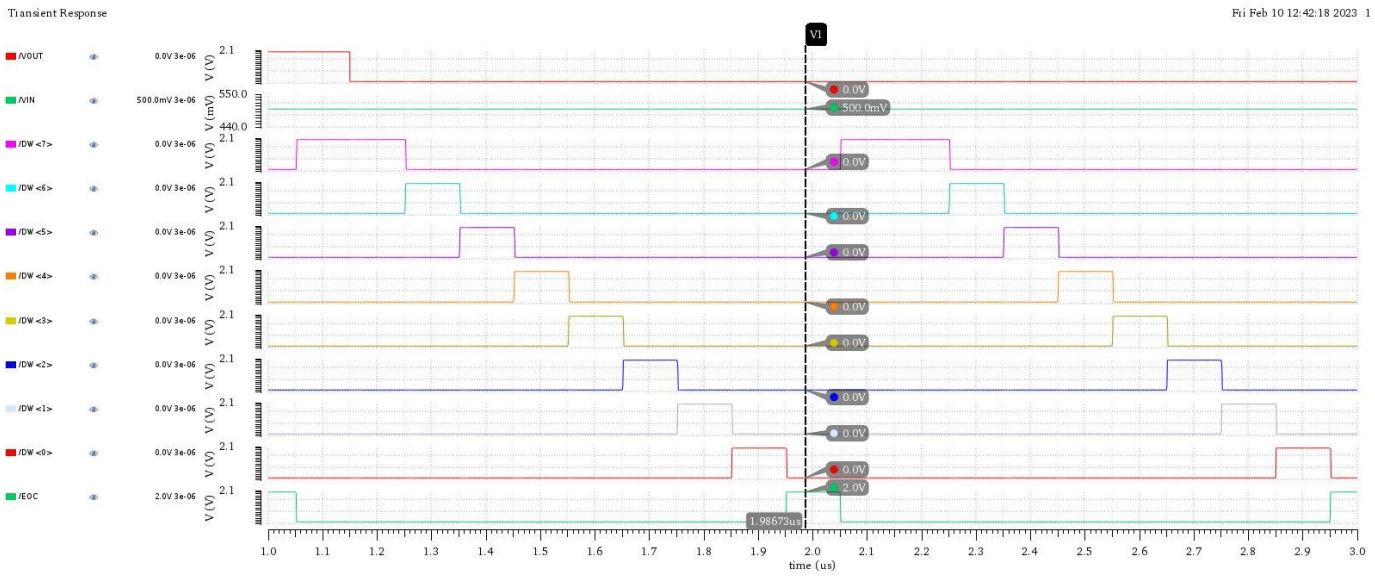
PART 4: DC Functional Test

The values which I simulated with:

Global Variables	
SW_POS	2
tcphlq	1n
tcplhq	1n
VCM	0.5*(VREFP + VREFN)
VDD	2
vhi	2
VIN	VREFN
vlo	0
VREFN	0.25*VDD
VREFP	0.75*VDD
TCLK	100n
TRF	100p
TS	(NBIT+2)*TCLK
CP	12.8*CU
CU	20f
NBIT	8
VLSB	(VREFP-VREFN)/256
TDROP	TS
TSTOP	3*TS

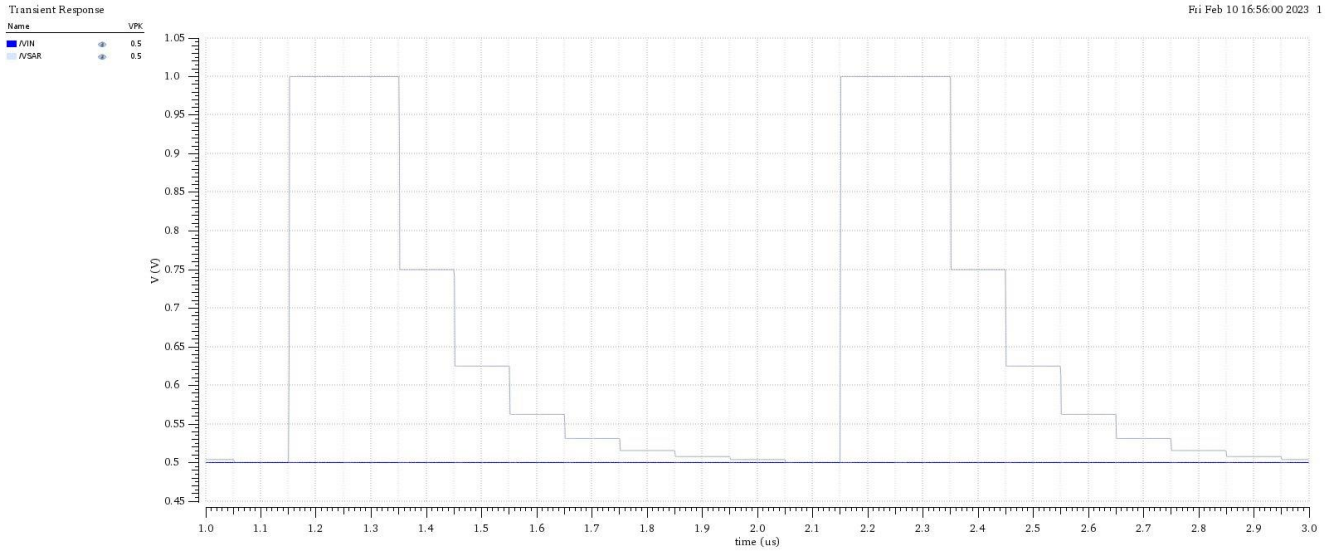
Run transient simulation for three cases of VIN:

a. VIN = VREFN → output will be all zeros

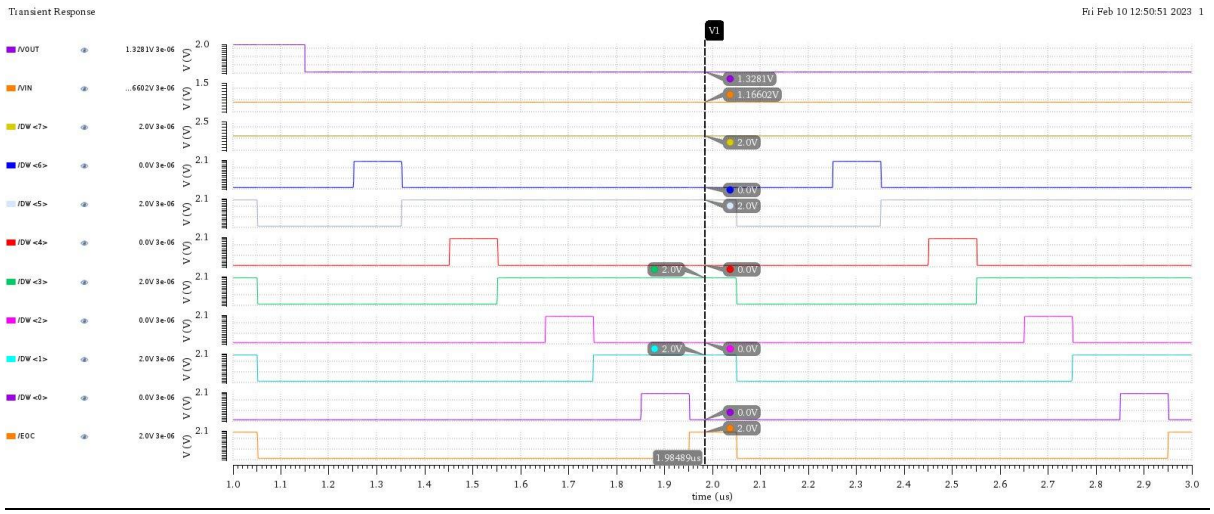


Notice that the output at the end of conversion is all zeros as expected

Report the waveforms of VIN and VSAR overlaid

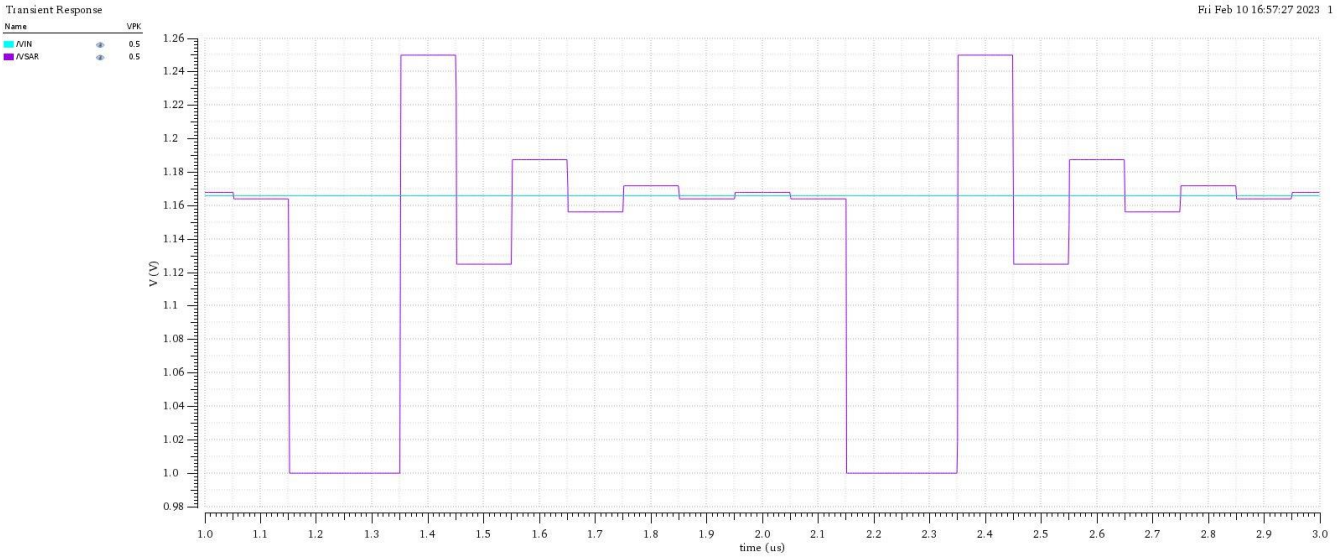


b. VIN = VREFN + (128+32+8+2+0.5)*VLSB → output will be alternating zeros and ones

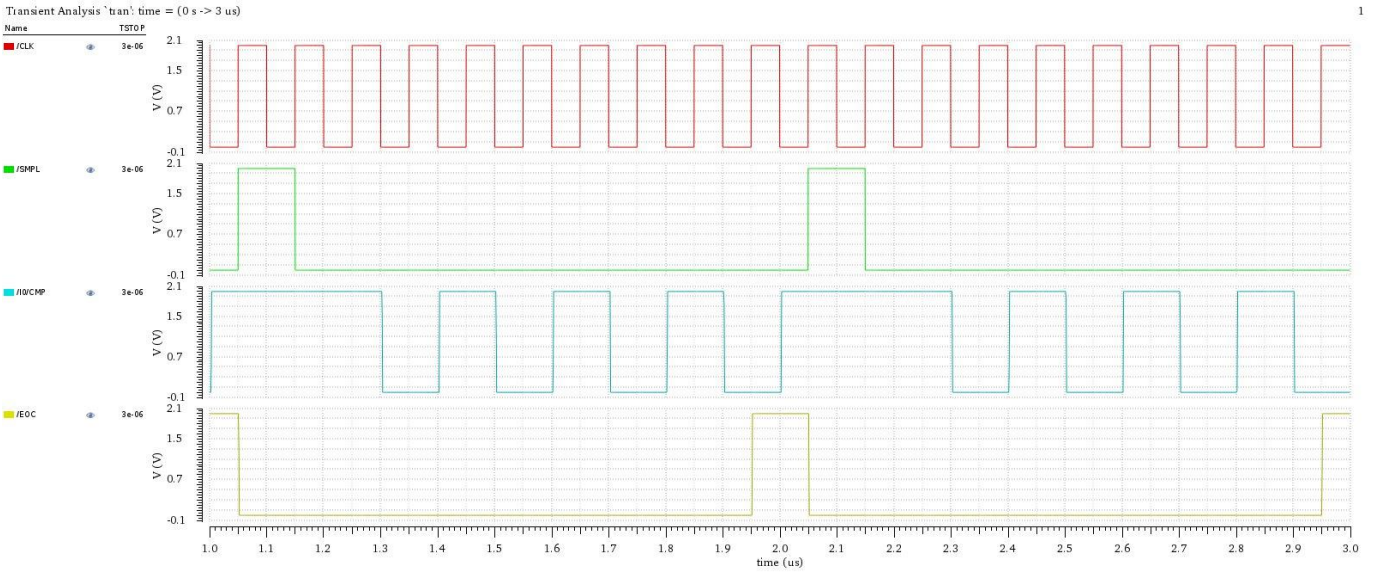


Notice how the output at the end of conversion is alternating between 1 and 0 as expected

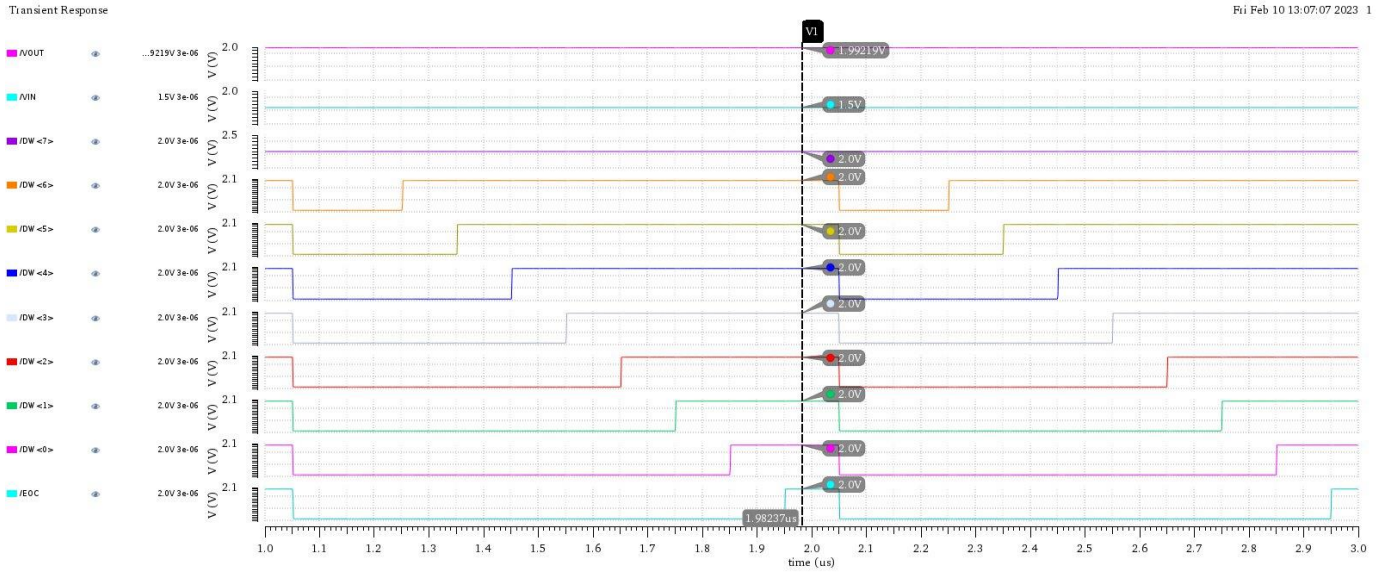
Report the waveforms of VIN and VSAR overlaid



Report the waveforms of SMPL, CLK, CMP, and EOC

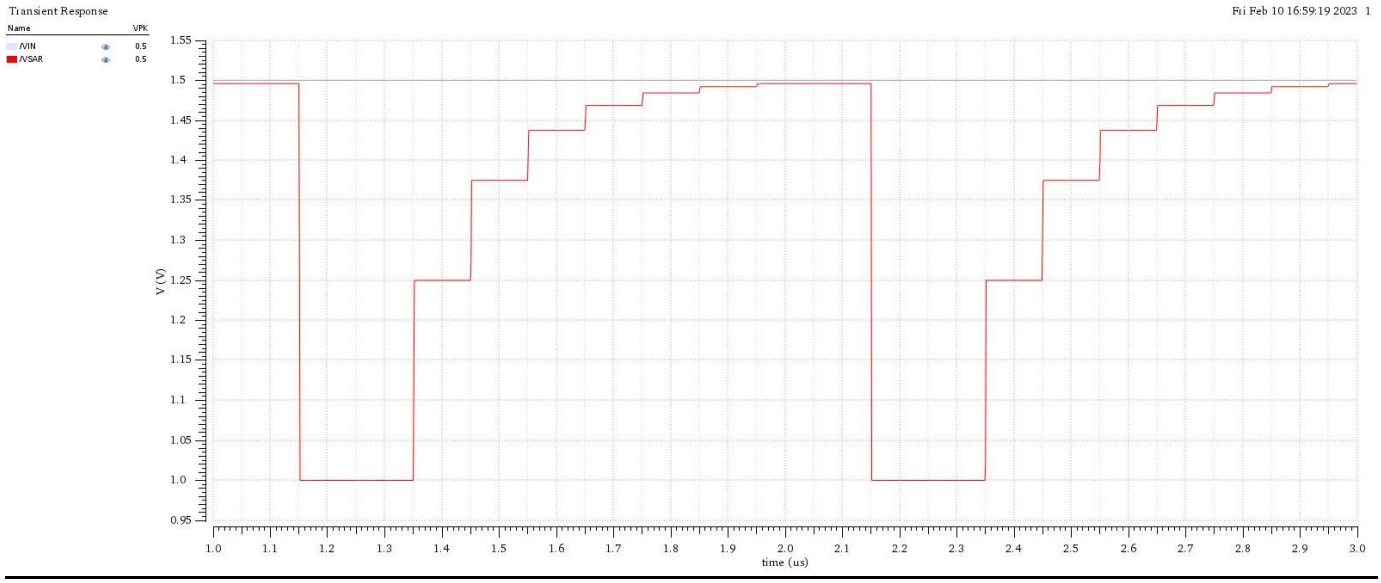


c. VIN = VREFP → output will be all ones



Notice that the output at the end of conversion is all ones as expected

Report the waveforms of VIN and VSAR overlaid



PART 5: Sine Wave Test

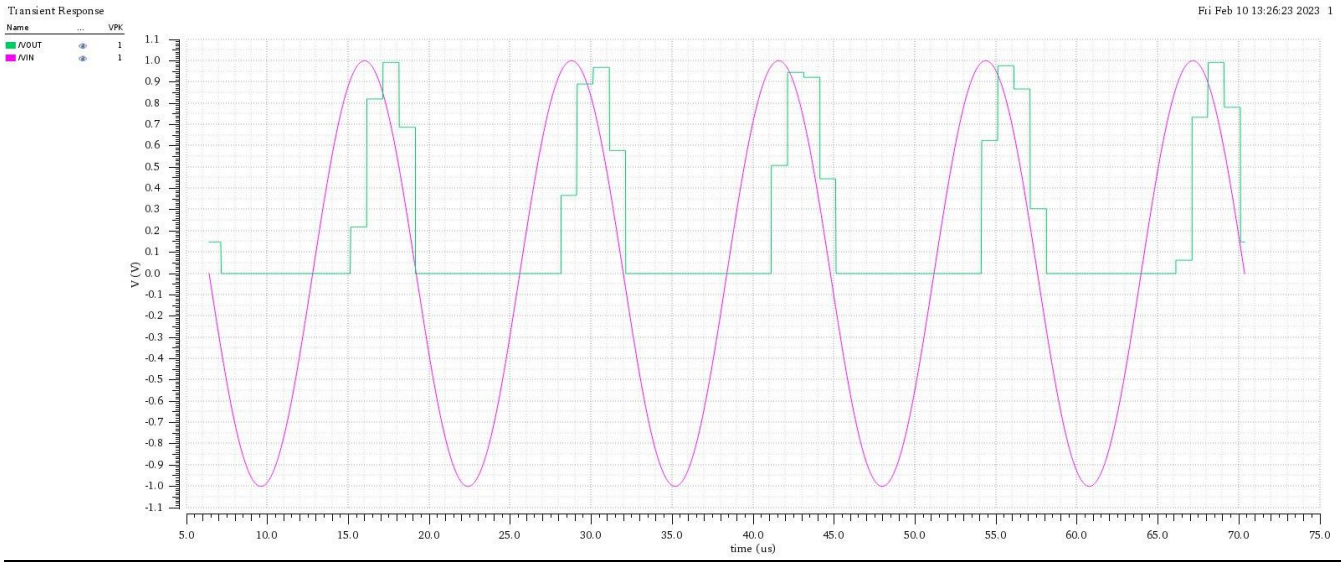
The values I used for this simulation:

Data View

Global Variables	
SW_POS	1
tcphlq	1n
tcplhq	1n
VCM	0.5*(VREFP + VREFN)
VDD	2
vhi	2
VIN	VREFP
vlo	0
VREFN	0.25*VDD
VREFP	0.75*VDD
TCLK	100n
TRF	100p
TS	(NBIT+2)*TCLK
CP	12.8*CU
CU	20f
NBIT	8
VLSB	(VREFP-VREFN)/256
TDROP	0.5/FIN
TSTOP	NCYC/FIN + TDROP
NFFT	64
NCYC	5
FIN	(NCYC/NFFT)/TS
VPK	VDD/4

Click to add variable

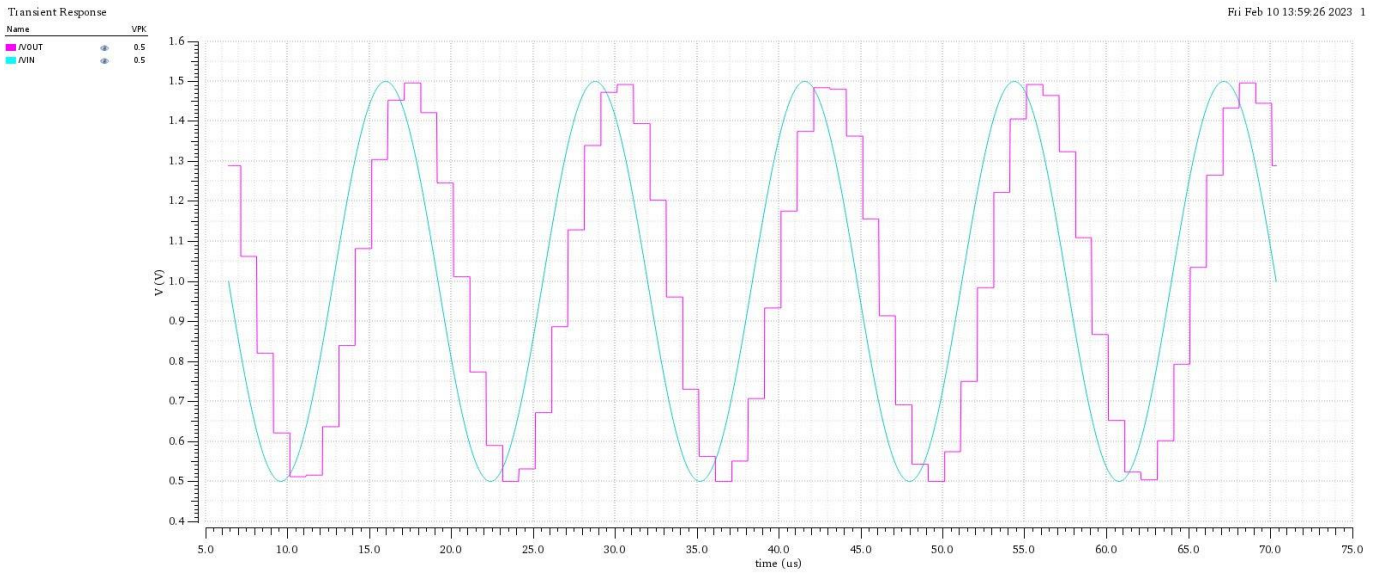
Plot transient waveforms of VIN and VOUT



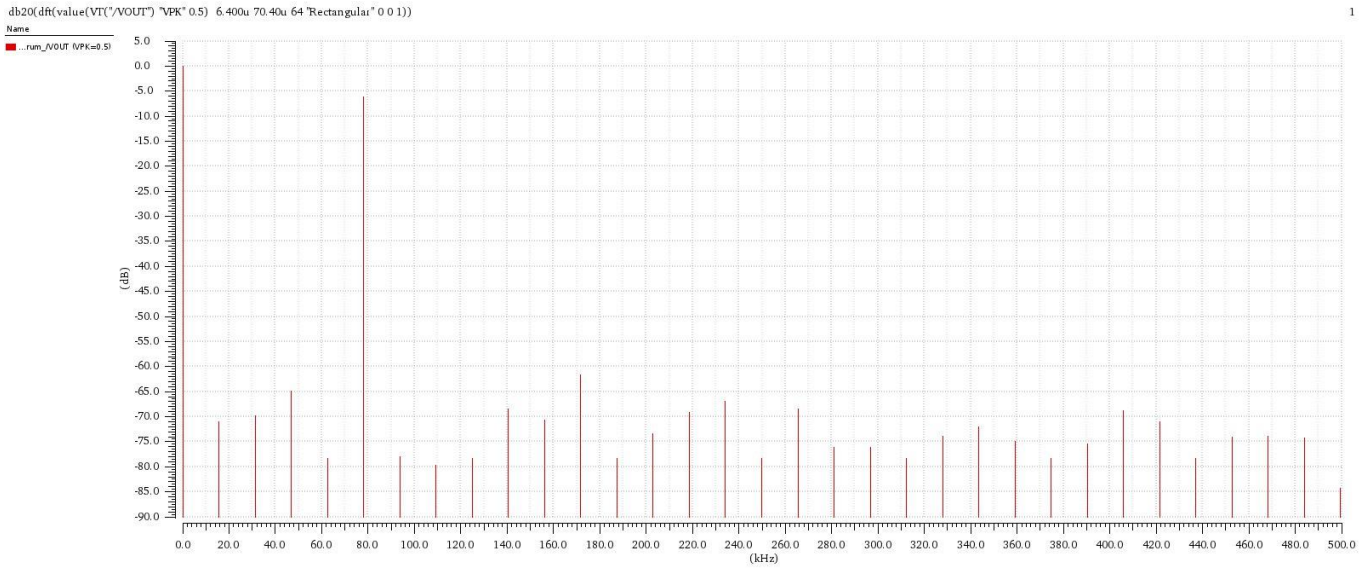
This is what the lab manual required

But here is another version where I put a dc voltage of 1 volt to the input sine wave

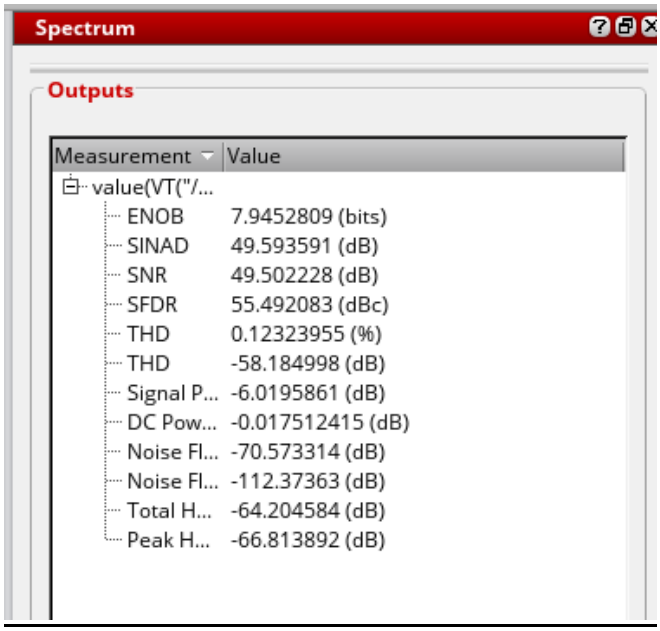
Plot transient waveforms of VIN and VOUT



Plot the FFT of the VOUT to measure the ENOB and other performance parameters.

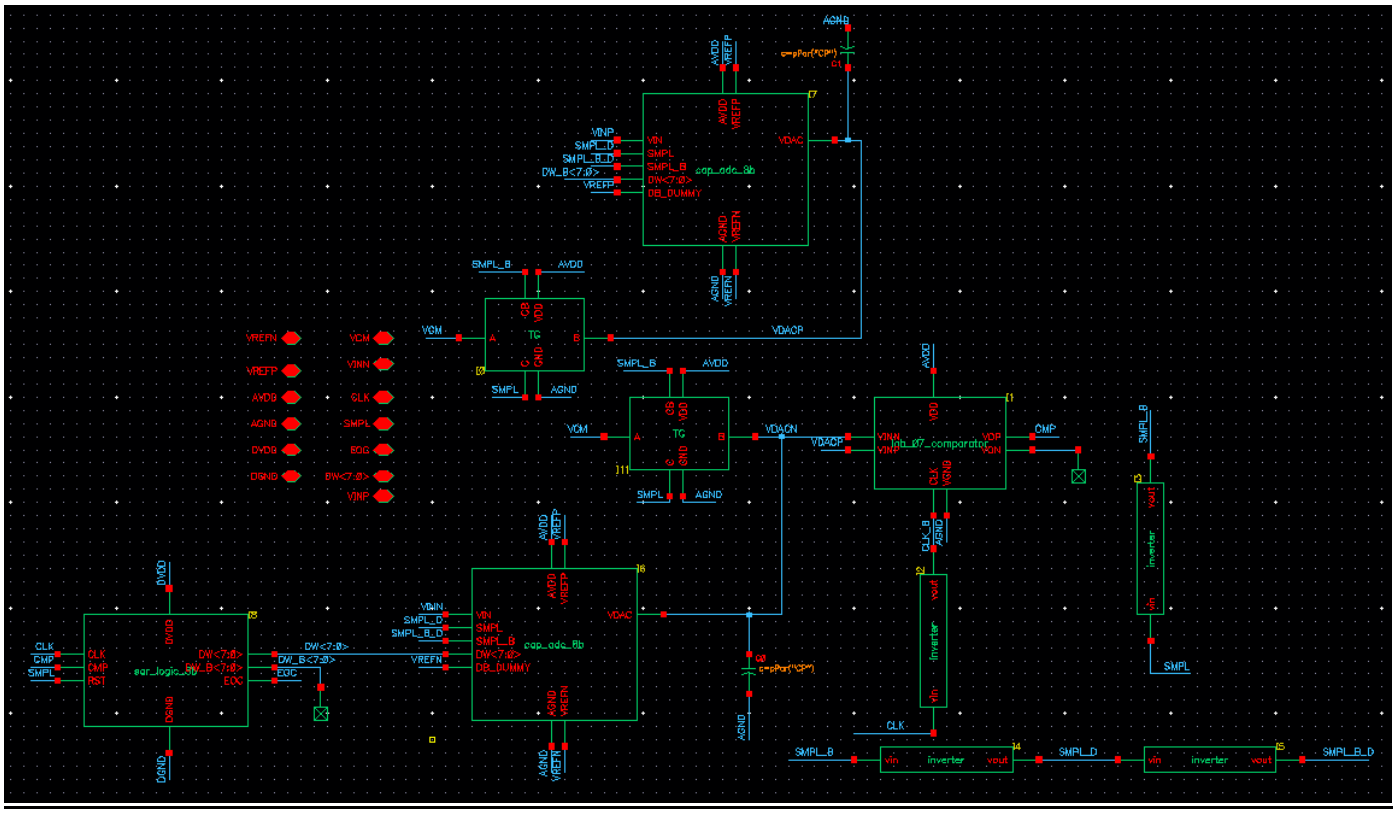


Here are the spectrum performance parameters.

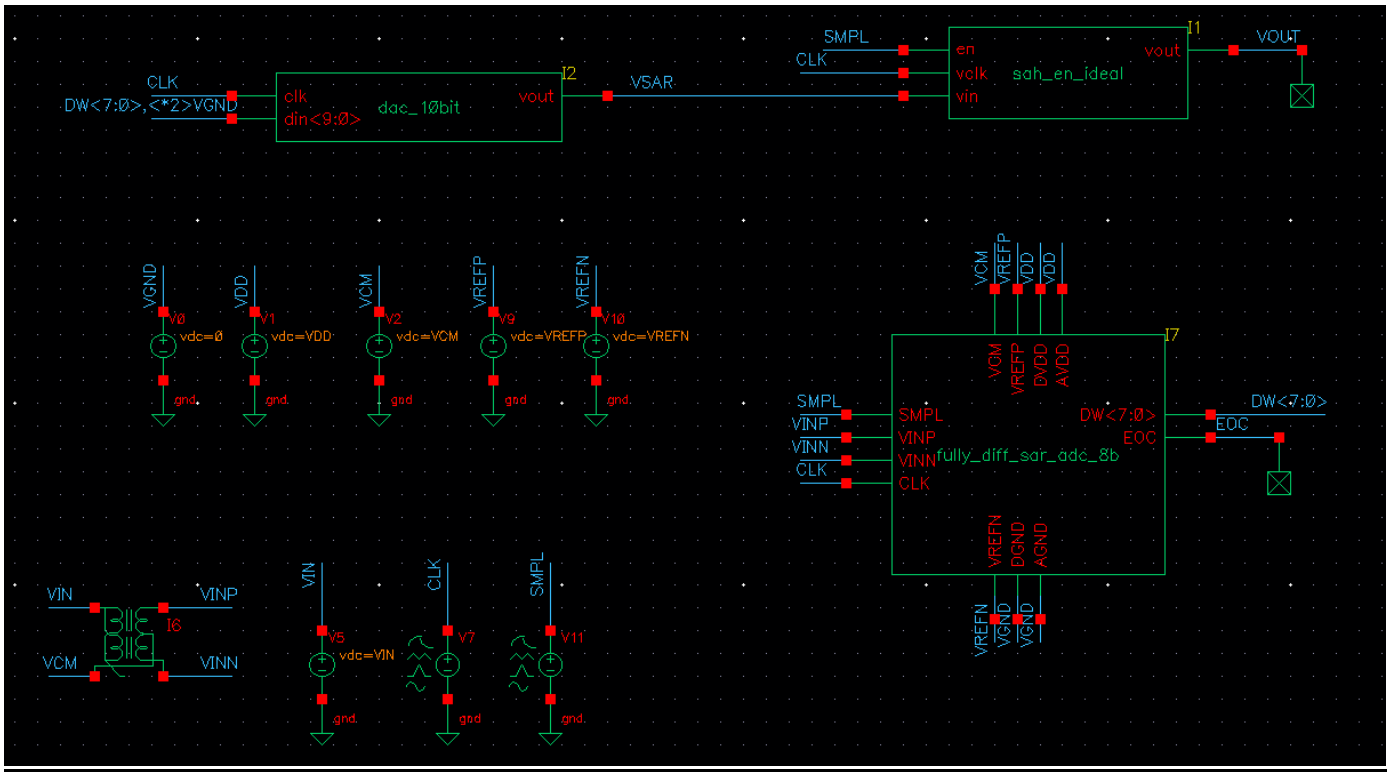


PART 6: Fully-Differential SAR ADC

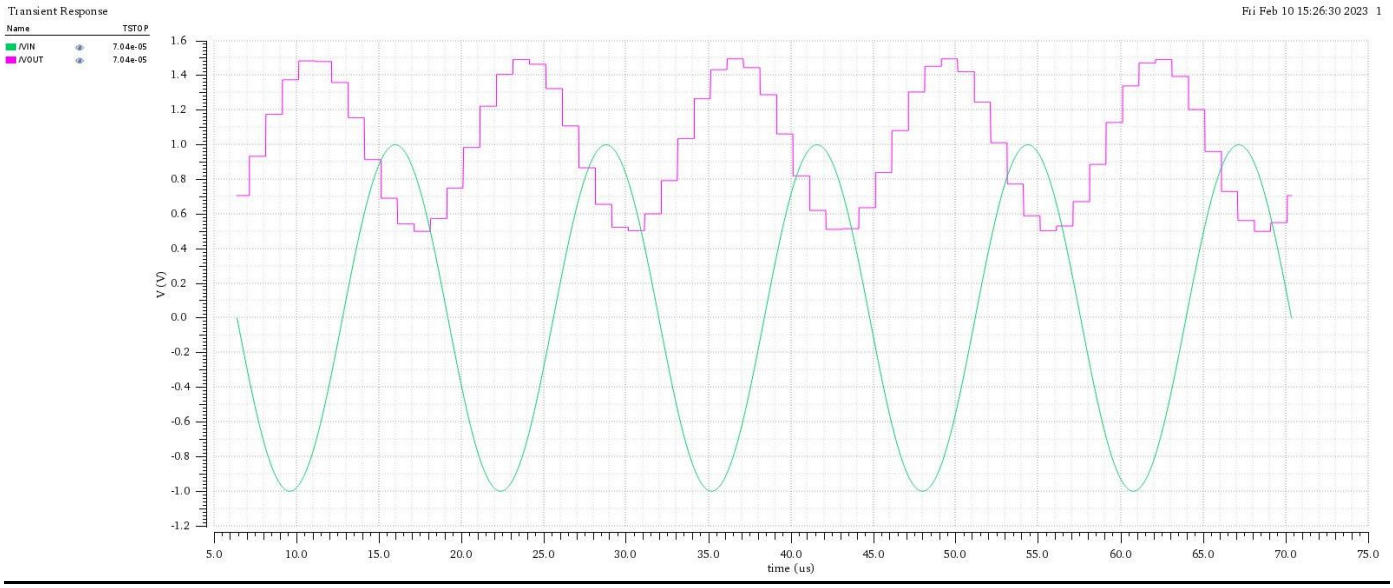
Create a new schematic for fully-differential SAR ADC



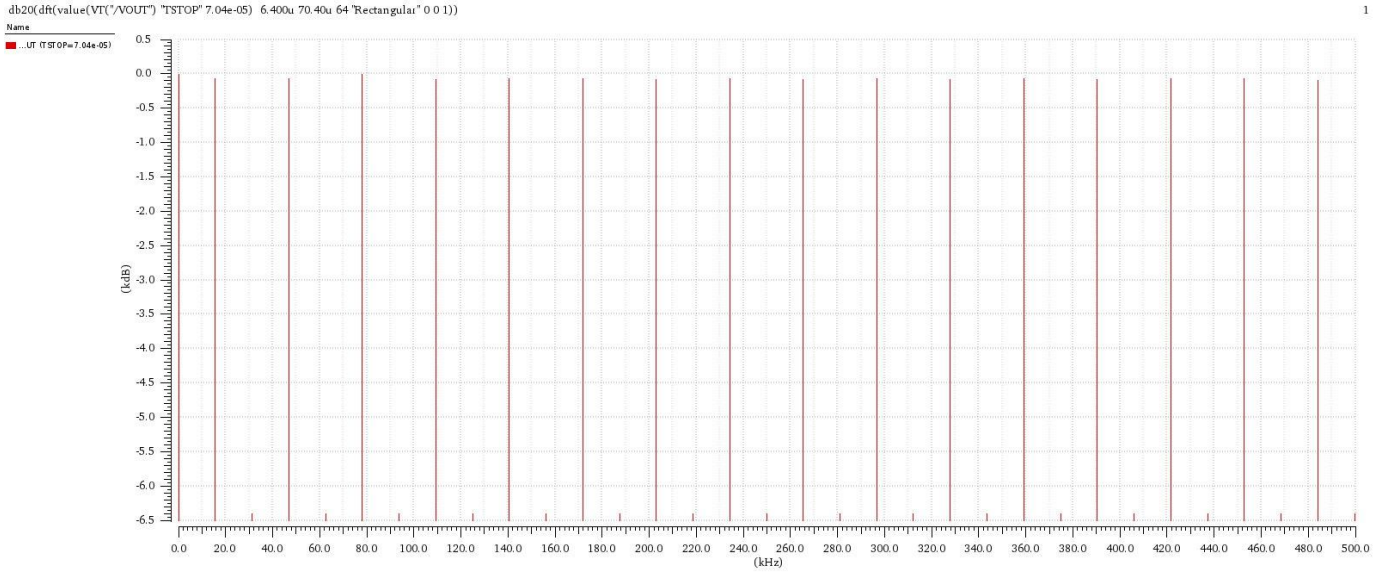
Create a new schematic for fully-differential SAR ADC testbench



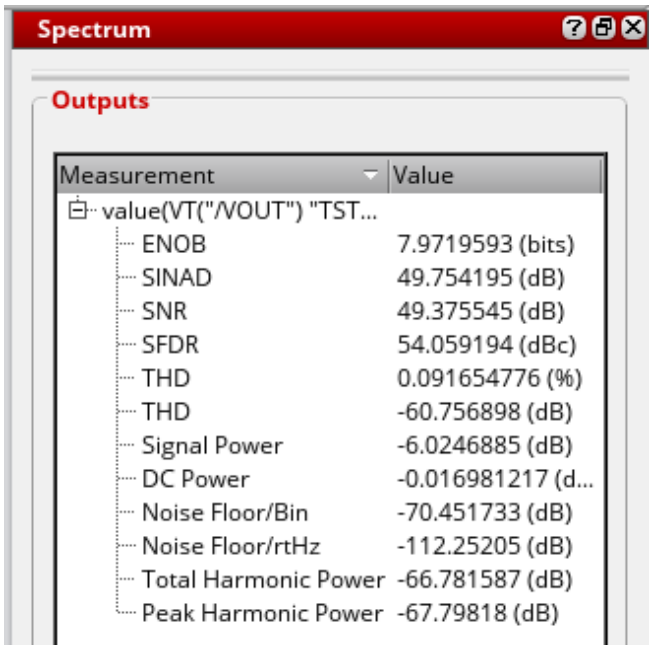
Plot transient waveforms of VIN and VOUT.



Plot the FFT of the VOUT to measure the ENOB and other performance parameters.



Here are the spectrum performance parameters.



notice that the differential architecture gave better ENOB,THD.