Project: Using Tcl to manipulate modelsim/Questasim

Introduction:

Questasim (previously known as modelsim) is one of the most common used simulators for RTL designs. It is almost integrated with all FPGA IDEs. The task of tool is to compile and simulate RTL designs. In real world, RTL designers usually write regression test as a collection of testbenches. Each testbench should run and provide a result. We can use TCL to automate this testing process and get a final statistic.

Objective:

- To learn how to write a script to compile and simulate designs in modelsim using tcl
- To build a test suite to automate testing

```
vlib work

vlog half_adder.v .\anotherfoler\full_adder.v

vsim -batch full_adder  -do "run -all ; run -all ;"
```

```
vlib work

vcom half_adder.vhd .\anotherfoler\full_adder.vhd

vsim -batch full_adder  -do .\dofile.do
```