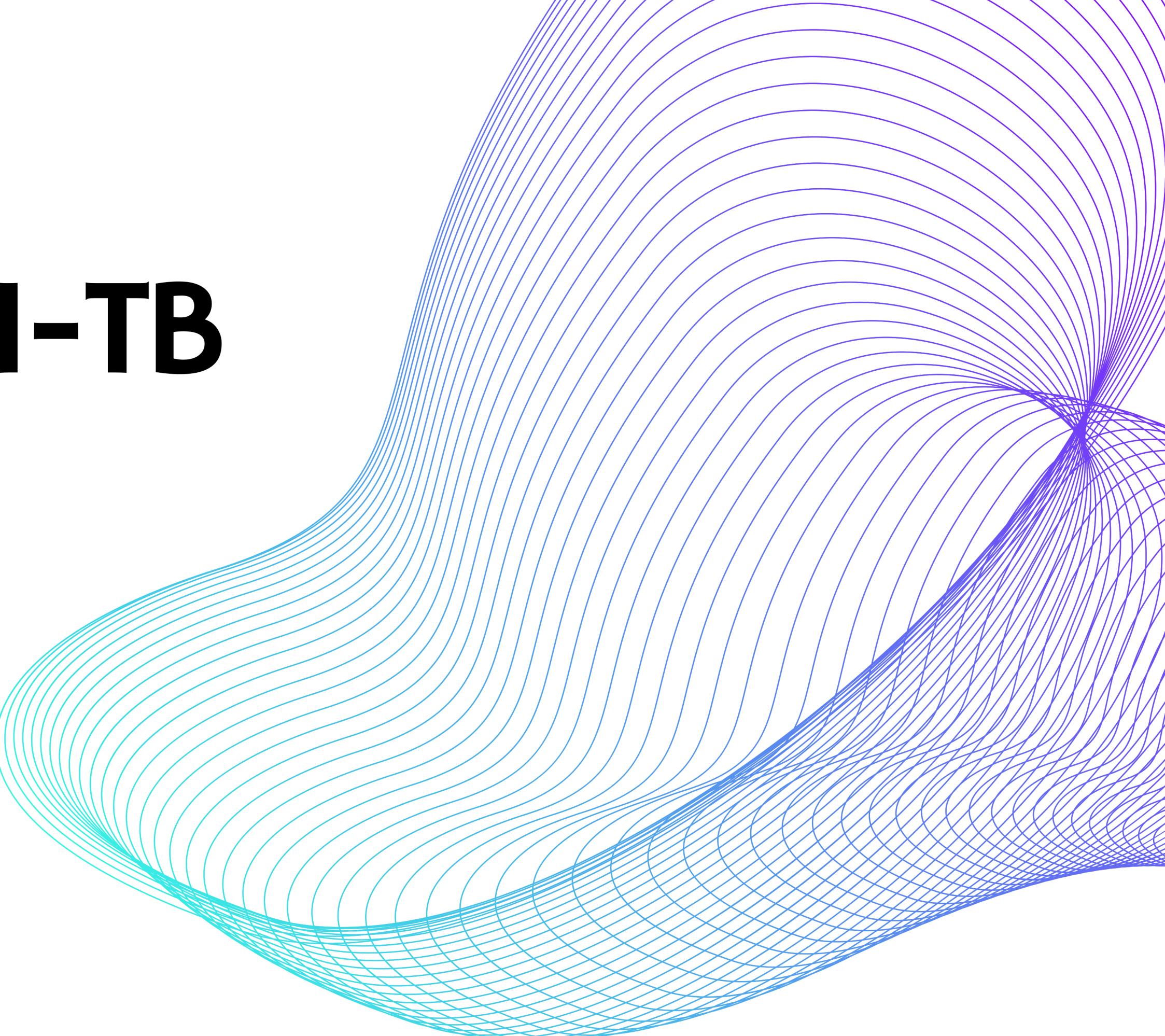


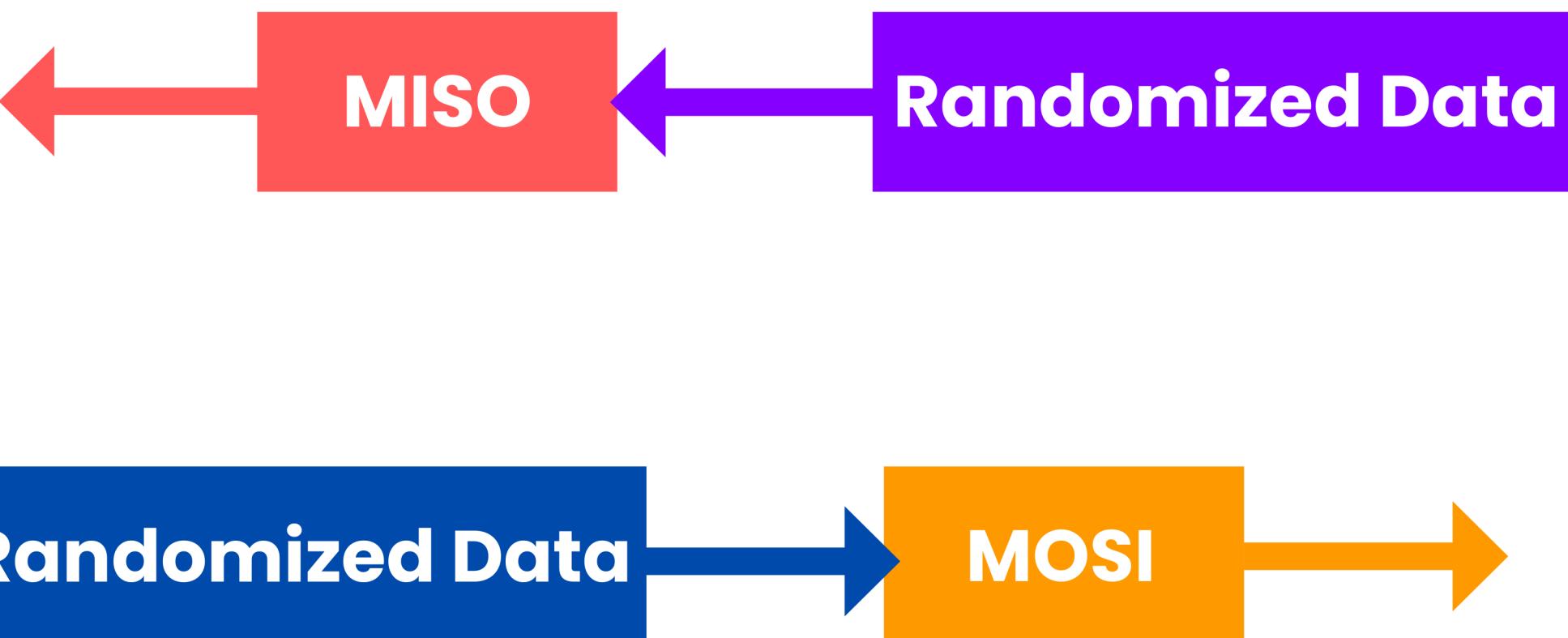
Design & UVM-TB of SPI Master

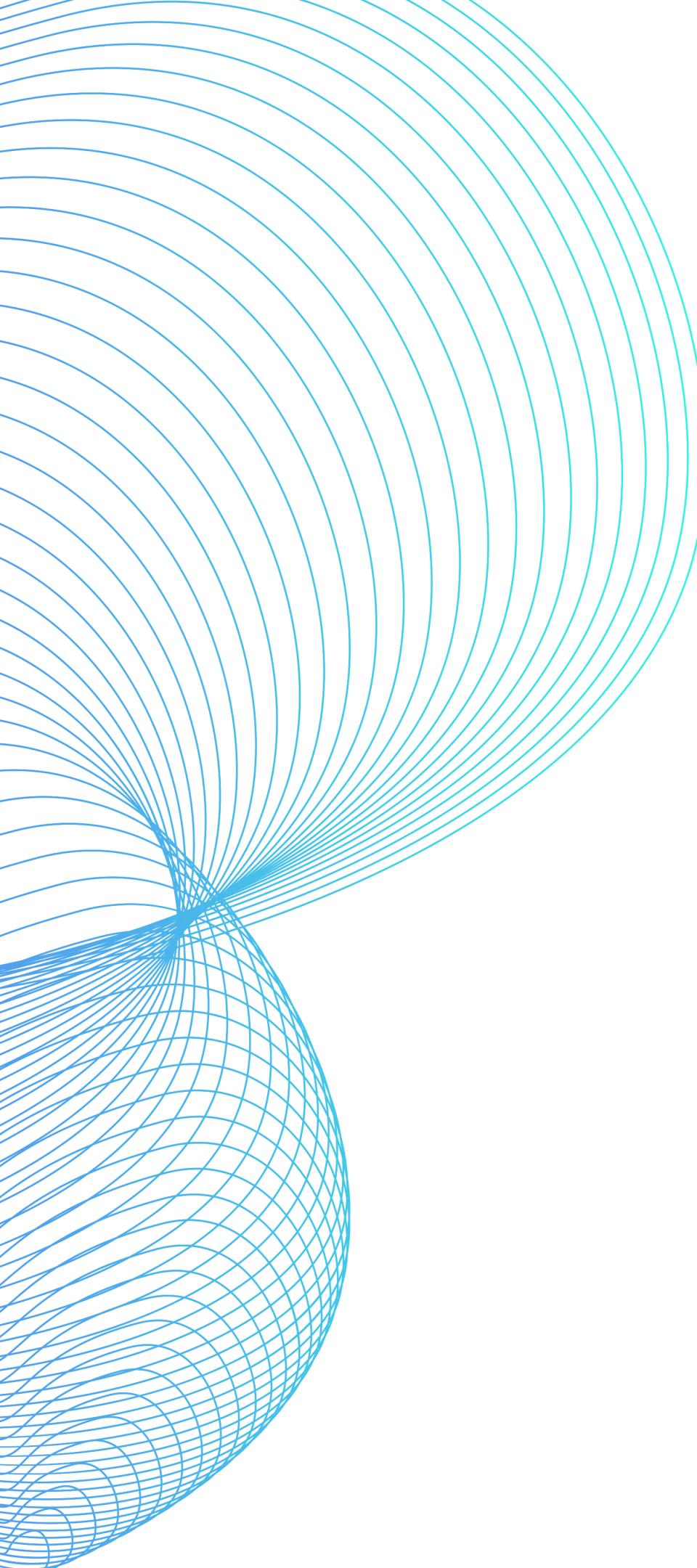


Youssef Ahmed



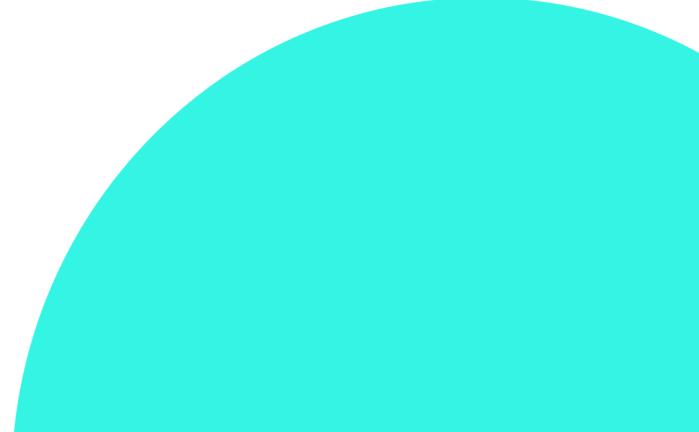
The design is configured in a way that MOSI transmits randomized data, and similarly, MISO also receives randomized data. However, it's important to note that the randomized data for MISO may not be the same randomized data.





UVM Architecture



- Top
 - Environment
 - Agent
 - Monitor
 - Driver
 - Sequencer
 - Coverage
 - Collector
- 

Top

Test

Env

Agent

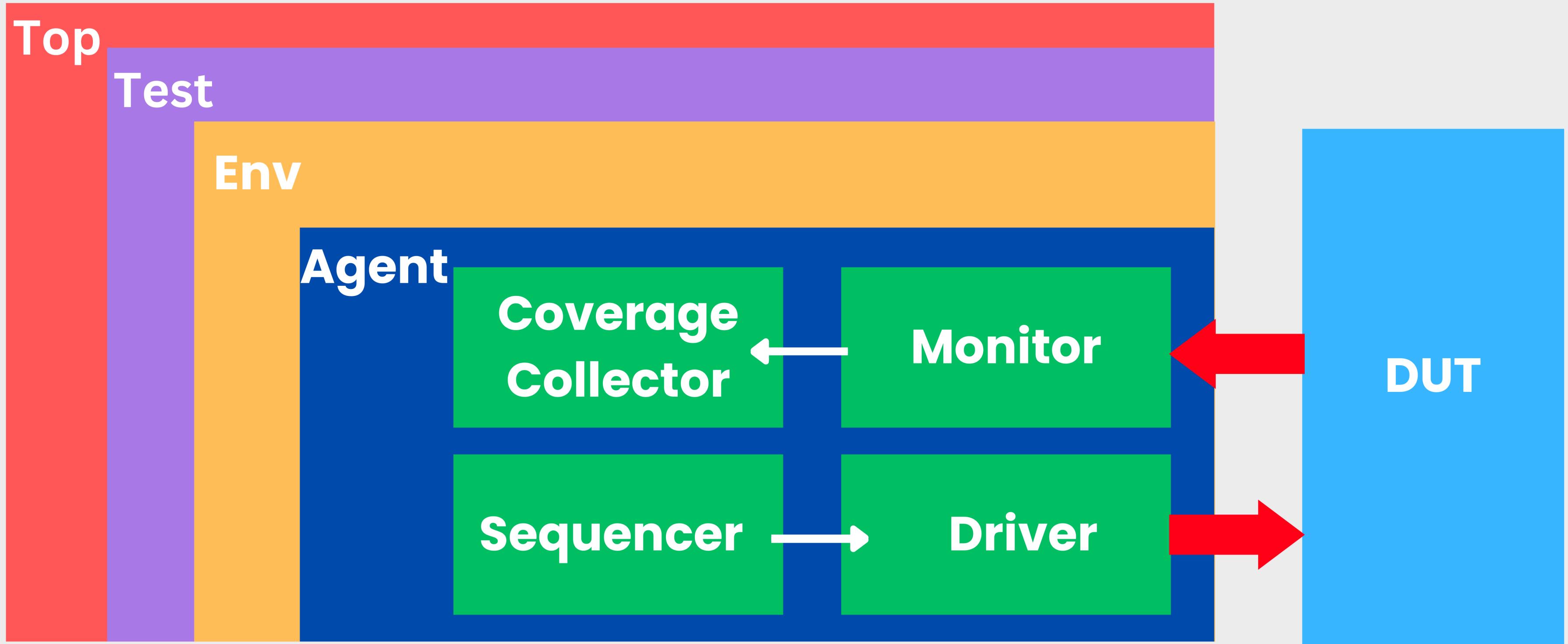
Coverage
Collector

Sequencer

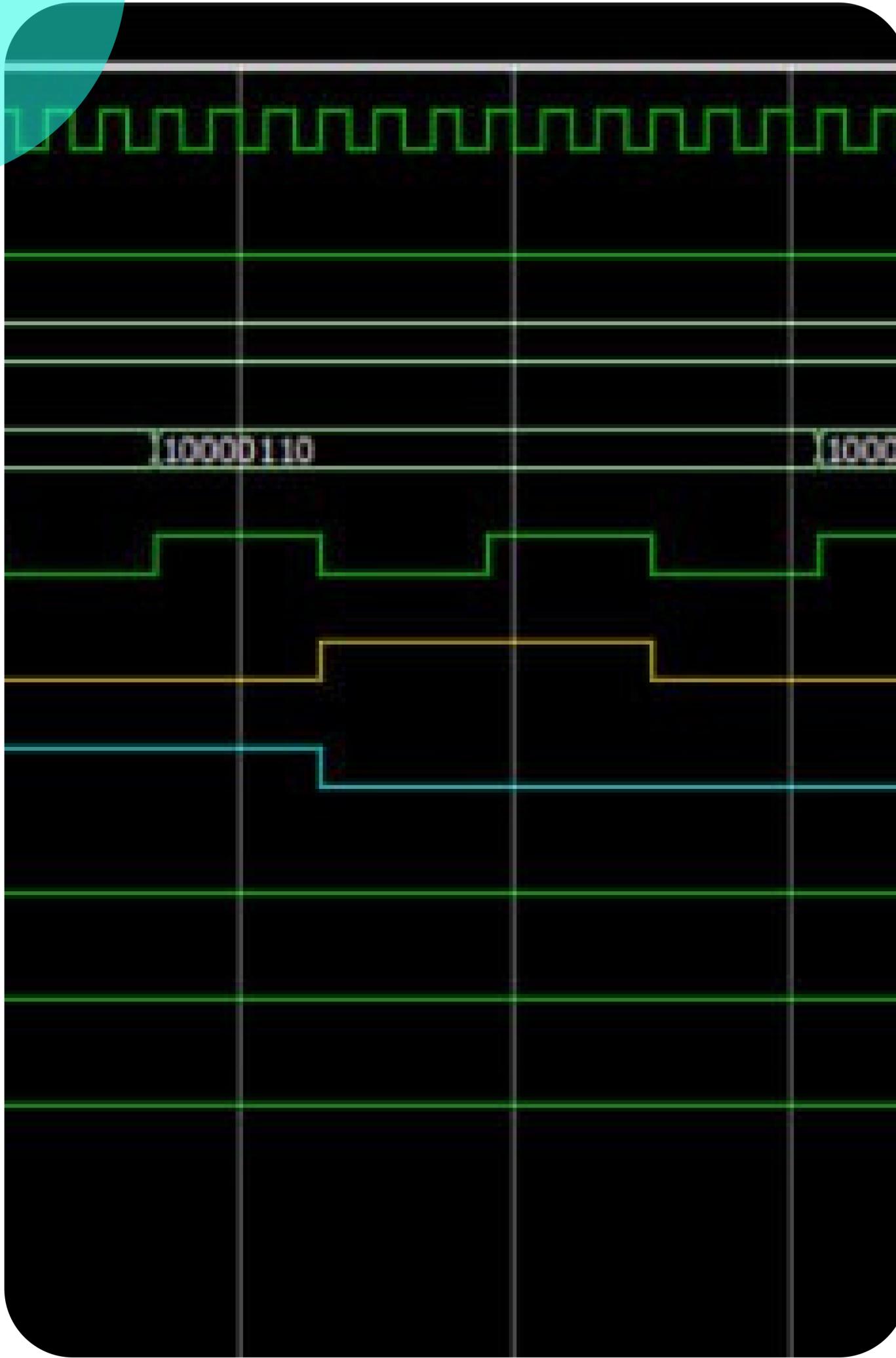
Monitor

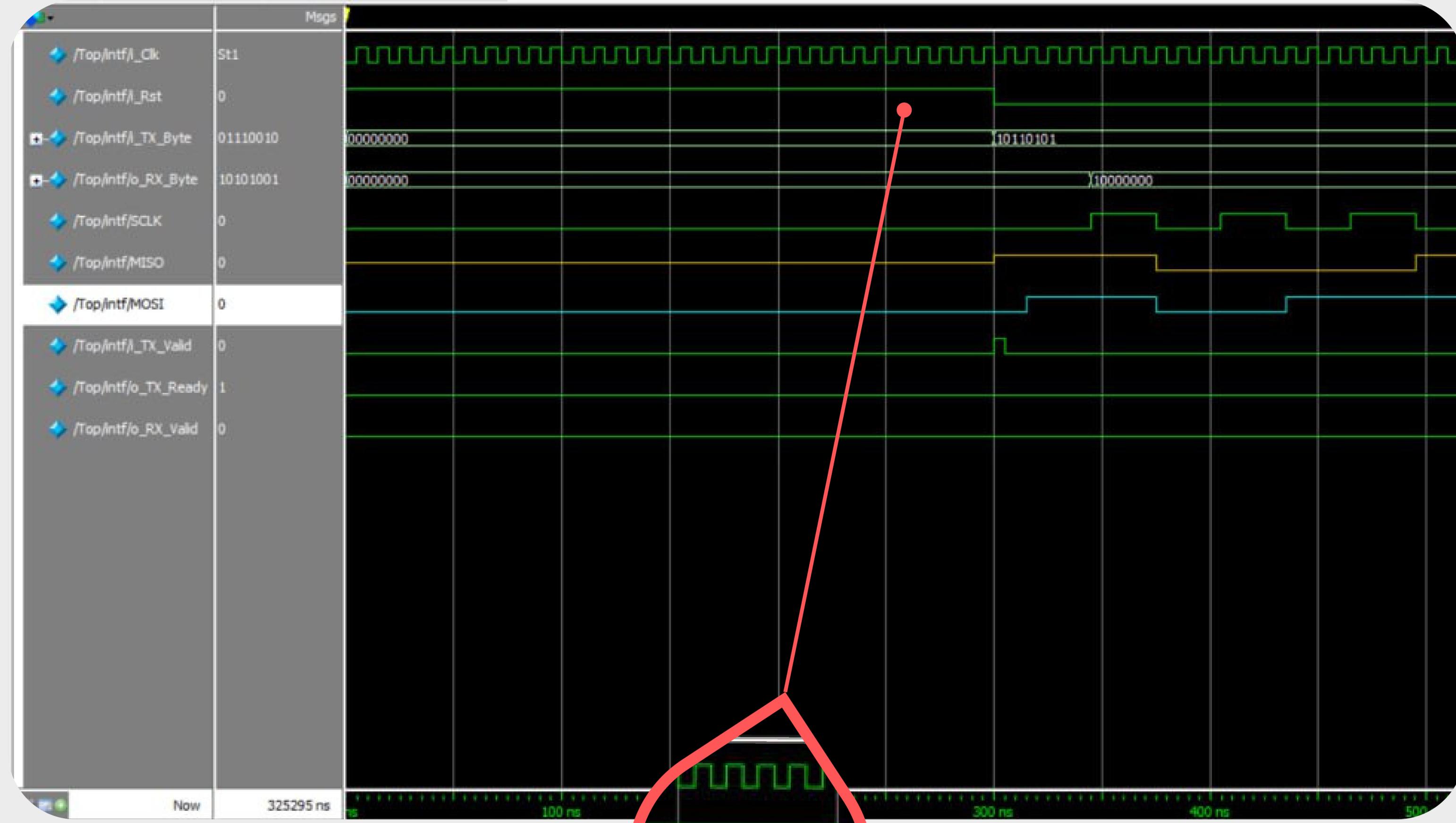
Driver

DUT

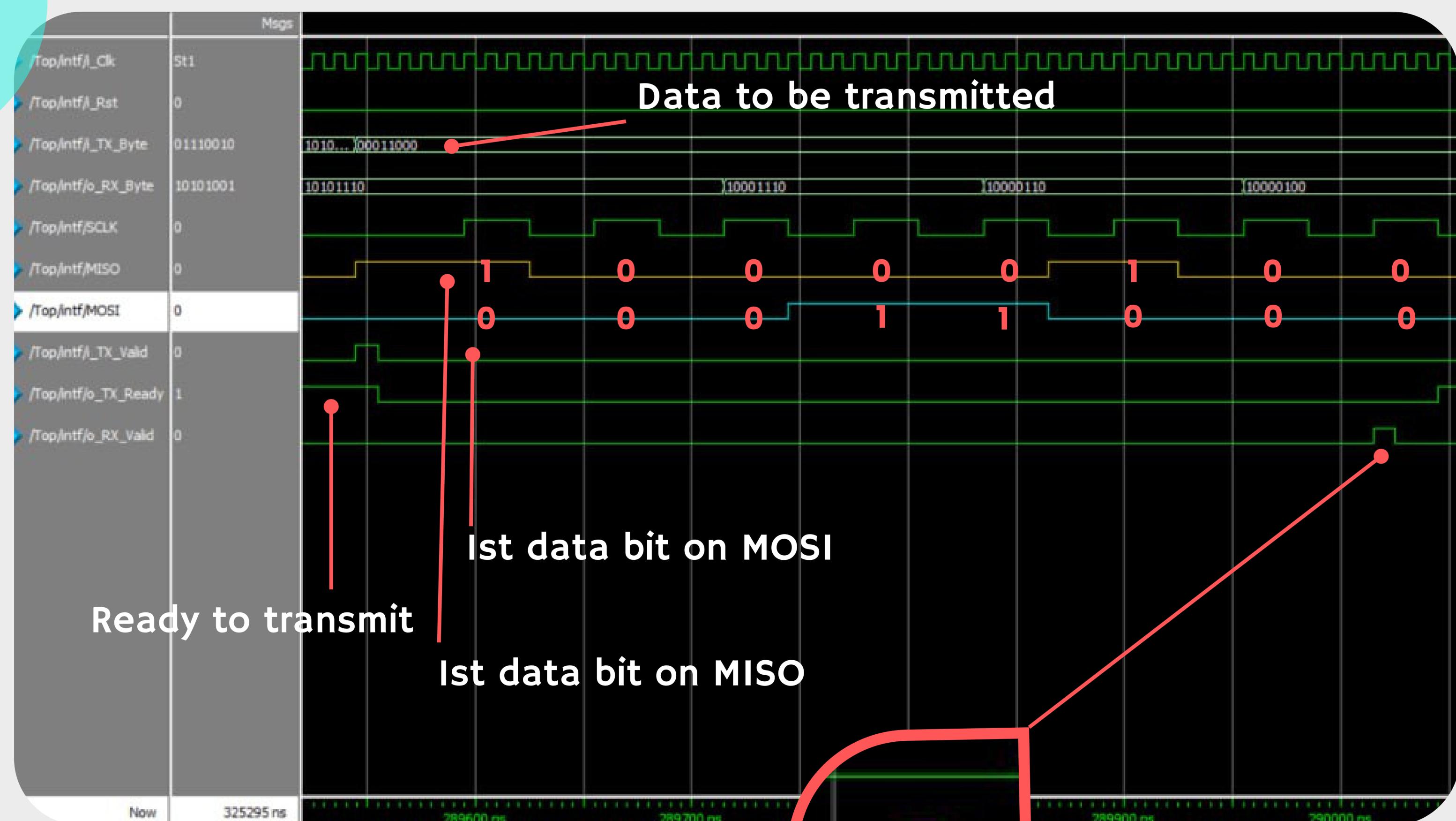


Simulation Results

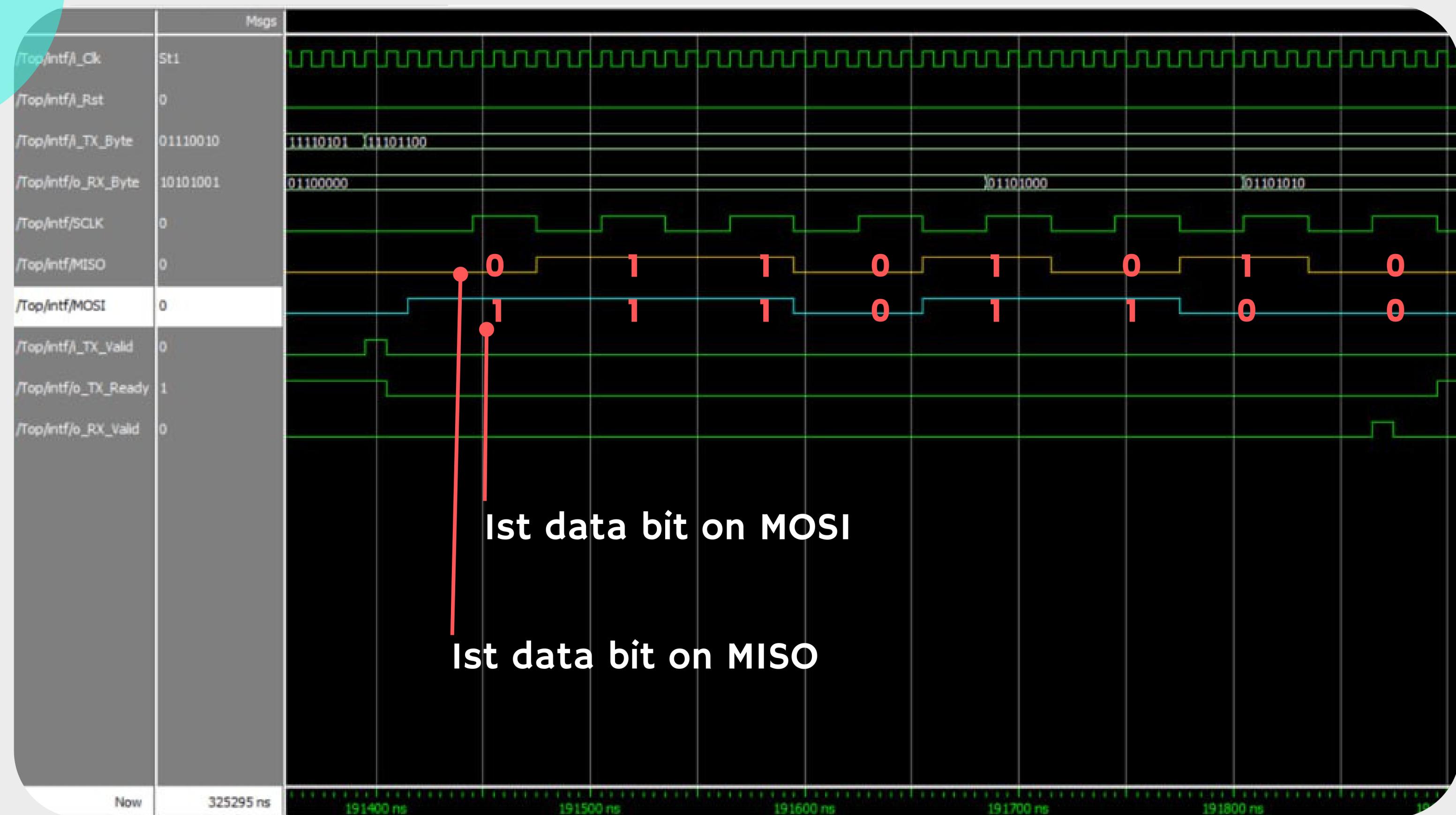




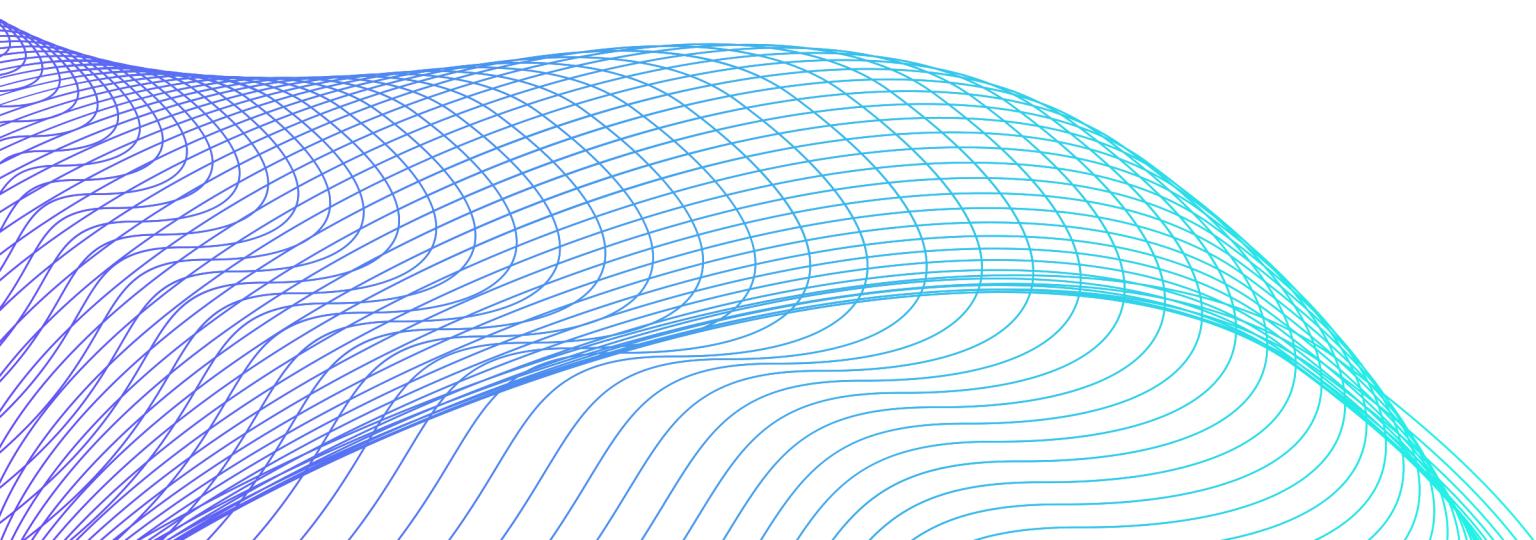
Resetting the system



Was successfully received



Coverage report



Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

code coverage is excluded

[List of tests included in report...](#)

Coverage Summary by Structure:		Coverage Summary by Type:				
Design Scope	Coverage (%)	Weighted Average:			100.00%	
Top	100.00%					
uvm_pkg	100.00%					
uvm_callbacks	100.00%					
uvm_phase	100.00%					
uvm_component	100.00%					
SPL_pkg	100.00%					
Coverage_collector	100.00%					
		Coverage Type	Bins	Hits	Misses	Coverage (%)
		Covergroup	66	66	0	100.00%
		Directive	4	4	0	100.00%
		Assertion Attempted	22	22	0	100.00%
		Assertion Failures	22	0	-	0.00%
		Assertion Successes	22	22	0	100.00%

Questa Covergroup Coverage Report

Scope: /SPI_pkg/Coverage collector

Show All

Show Covered

Show Missing

Covergroups / Instances	Total Bins	Covered Bins	Coverage
Covergroup <u>SPI_cover_signals</u>	66	66	100.00%

Covergroup type: <u>SPI_cover_signals</u>	100.00%			
Coverpoints / Bins	At Least	Hits	Goal	Coverage
Coverpoint: <u>TX_Byte_cov</u>			100.00%	100.00%
Coverpoint: <u>MISO_cov</u>			100.00%	100.00%

Questa Coverage Summary

Scope: /Top

code coverage is included

Coverage Summary By Instance:

Scope	TOTAL	Cvg	Cover	Statement	Branch	UDP Expression	UDP Condition	FEC Expression	FEC Condition	Toggle	FSM State	FSM Trans	Assertion Attempted	Assertion Passes	Failure
TOTAL	94.56%	--	100.00%	98.27%	100.00%	--	--	--	80.00%	--	--	--	--	--	--
Top	93.75%	--	100.00%	87.50%	--	--	--	--	--	--	--	--	--	--	--
DUT	93.33%	--	--	100.00%	100.00%	--	--	--	80.00%	--	--	--	--	--	--

Local Instance Coverage Details:

Weighted Average:	93.75%			
Coverage Type	Bins	Hits	Misses	Coverage (%)
Directive	4	4	0	100.00%
Statement	8	7	1	87.50%

Recursive Hierarchical Coverage Details:

Weighted Average:	94.56%			
Coverage Type	Bins	Hits	Misses	Coverage (%)
Directive	4	4	0	100.00%
Statement	58	57	1	98.27%
Branch	29	29	0	100.00%
FEC Condition	10	8	2	80.00%

Questa Coverage Summary

Scope: /Top/DUT

Local Instance Coverage Details:

Weighted Average:				93.33%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	50	50	0	100.00%
Branch	29	29	0	100.00%
FEC Condition	10	8	2	80.00%

Scope Details:

Instance Path:

/Top/DUT

Design Unit Name:

[work.SPI_Master](#)

Language:

SystemVerilog

Source File:

[Top.sv](#)

It is not covered 100% because
the design is configured to work
on one mode, which is mode 0
where CPHA=0

Questa Condition Coverage Report

Scope: /Top/DUT

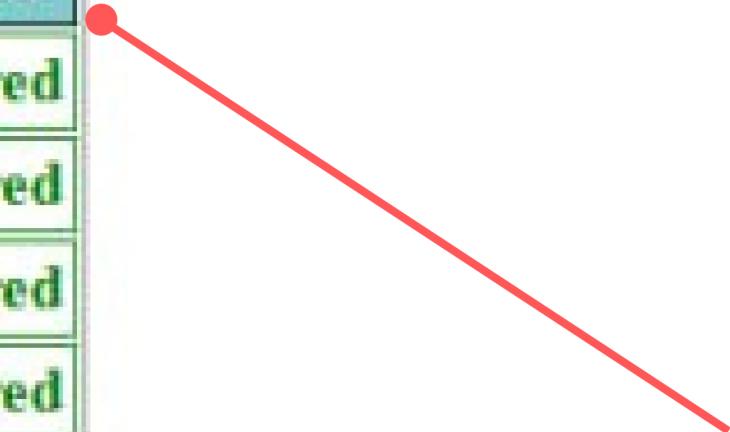
Show All	Show Covered	Show Missing	
FEC Condition: SPI_Master.sv:163		100.00%	
Input Term	Covered	Reason For No Coverage	Hint
I_TX_Valid	Yes		
w_CPHA	No	'_I' not hit	Hit '_I'
FEC Target	Hits	Matching Input Patterns	
I_TX_Valid_0	24001	{ 00 }	
I_TX_Valid_1	500	{ 10 }	
w_CPHA_0	500	{ 10 }	
w_CPHA_1	0	{ 11 }	

Questa Cover Directive Report

Scope: /[Top](#)

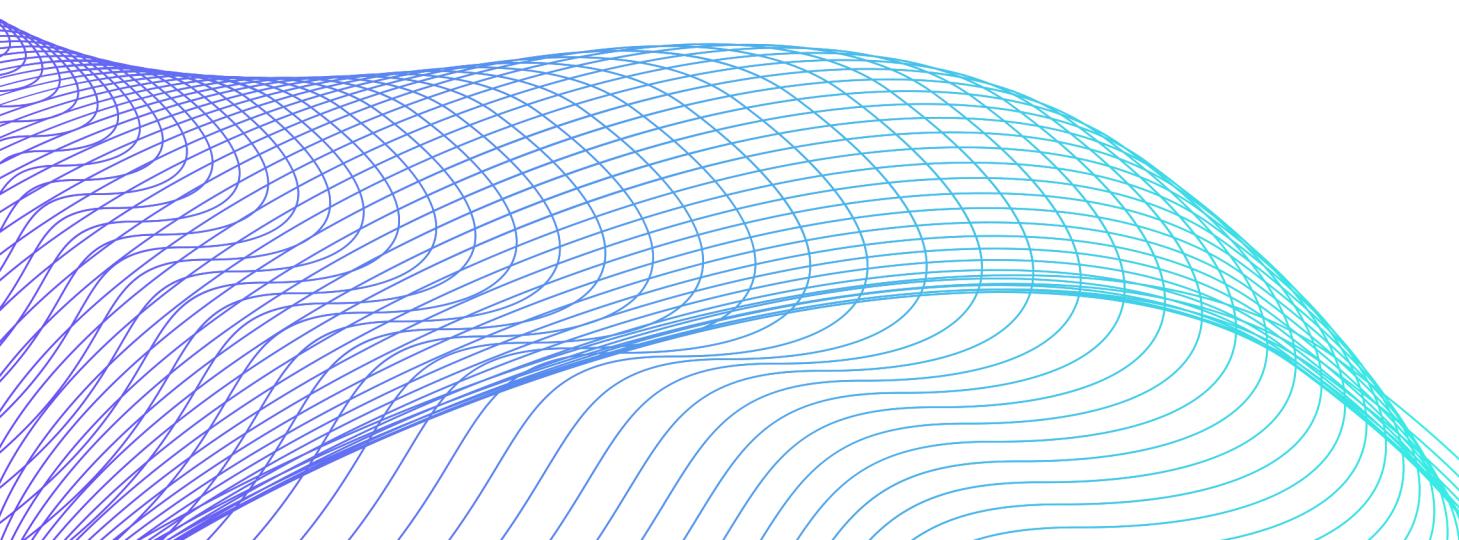
[Show All](#) [Show Covered](#) [Show Missing](#)

Cover Directive	Hits	Status
cover_Valid_Receiving	500	Covered
cover_Not_Ready	4000	Covered
cover_End_Of_SCLK	7998	Covered
cover_Start_Of_SCLK	500	Covered



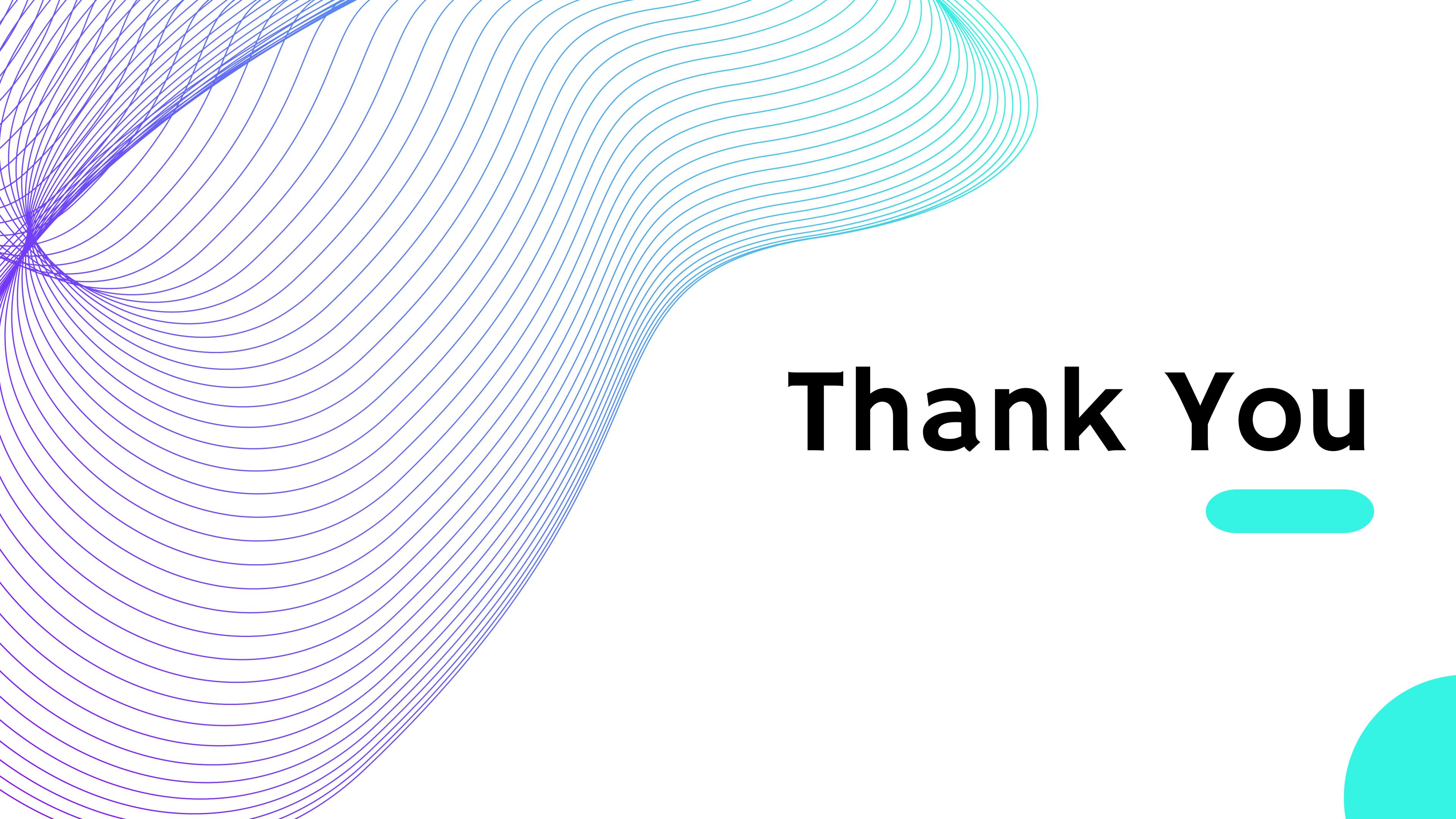
covered assertions in top design

Simulation Log Results



```
UVM-1.0pl
# (C) 2007-2011 Mentor Graphics Corporation
# (C) 2007-2011 Cadence Design Systems, Inc.
# (C) 2006-2011 Synopsys, Inc.
#
# UVM_INFO SPI_Test.sv(26) @ 0: uvm_test_top [SPI_Test] Inside constructor of SPI Test Class
# UVM_INFO @ 0: reporter [RNTST] Running test SPI_Test...
# UVM_INFO SPI_Test.sv(45) @ 0: uvm_test_top [SPI_Test] Inside build phase of SPI Test Class
# UVM_INFO Environment.sv(22) @ 0: uvm_test_top.SPI_environment [Environment] Inside constructor of Environment Class
# UVM_INFO Environment.sv(39) @ 0: uvm_test_top.SPI_environment [Environment] Inside build phase of Environment Class
# UVM_INFO Agent.sv(23) @ 0: uvm_test_top.SPI_environment.SPI_Agent [Agent] Inside constructor of Agent Class
# UVM_INFO Agent.sv(40) @ 0: uvm_test_top.SPI_environment.SPI_Agent [Agent] Inside build phase of Agent Class
# UVM_INFO Monitor.sv(31) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_monitor [Monitor] Inside constructor of Monitor Class
# UVM_INFO Driver.sv(25) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_driver [Driver] Inside constructor of Driver Class
# UVM_INFO Sequencer.sv(16) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_sequencer [Sequencer] Inside constructor of Sequencer Class
# UVM_INFO Coverage_collector.sv(45) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_coverage_collector [Coverage_collector] Inside const
# UVM_INFO Coverage_collector.sv(64) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_coverage_collector [Coverage_collector] Inside build
# UVM_INFO Driver.sv(42) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_driver [Driver] Inside build phase of Driver Class
# UVM_INFO Monitor.sv(50) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_monitor [Monitor] Inside build phase of Monitor Class
# UVM_INFO Sequencer.sv(33) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_sequencer [Sequencer] Inside build phase of Sequencer Class
# UVM_INFO Coverage_collector.sv(82) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_coverage_collector [Coverage_collector] Inside connec
# UVM_INFO Driver.sv(67) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_driver [Driver] Inside connect phase of Driver Class
# UVM_INFO Monitor.sv(78) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_monitor [Monitor] Inside connect phase of Monitor Class
# UVM_INFO Sequencer.sv(51) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_sequencer [Sequencer] Inside connect phase of Sequencer Class
# UVM_INFO Agent.sv(67) @ 0: uvm_test_top.SPI_environment.SPI_Agent [Agent] Inside connect phase of Agent Class
# UVM_INFO Environment.sv(61) @ 0: uvm_test_top.SPI_environment [Environment] Inside connect phase of Environment Class
# UVM_INFO SPI_Test.sv(67) @ 0: uvm_test_top [SPI_Test] Inside connect phase of SPI Test Class
# UVM_INFO SPI_Test.sv(86) @ 0: uvm_test_top [SPI_Test] Inside run phase of SPI Test Class
# UVM_INFO Environment.sv(79) @ 0: uvm_test_top.SPI_environment [Environment] Inside run phase of Environment Class
# UVM_INFO Agent.sv(88) @ 0: uvm_test_top.SPI_environment.SPI_Agent [Agent] Inside run phase of Agent Class
# UVM_INFO Sequencer.sv(68) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_sequencer [Sequencer] Inside run phase of Sequencer Class
# UVM_INFO Monitor.sv(96) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_monitor [Monitor] Inside run phase of Monitor Class
# UVM_INFO Driver.sv(84) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_driver [Driver] Inside run phase of Driver Class
# UVM_INFO Coverage_collector.sv(99) @ 0: uvm_test_top.SPI_environment.SPI_Agent.SPI_coverage_collector [Coverage_collector] Inside run r
# UVM_INFO verilog_src/uvm-1.0pl/src/base/uvm_objection.svh(1116) @ 325295: reporter [TEST_DONE] 'run' phase is ready to proceed to the
```

```
+---- UVM Report Summary ----  
+  
+ ** Report counts by severity  
+ UVM_INFO : 30  
+ UVM_WARNING : 0  
+ UVM_ERROR : 0  
+ UVM_FATAL : 0  
+ ** Report counts by id  
+ [Agent] 4  
+ [Coverage_collector] 4  
+ [Driver] 4  
+ [Environment] 4  
+ [Monitor] 4  
+ [RNTST] 1  
+ [SPI_Test] 4  
+ [Sequencer] 4  
+ [TEST_DONE] 1
```



A large, bold, black sans-serif font text "Thank You" is centered in the middle-right area of the image. The text is partially overlaid by a teal-colored rounded rectangle at the bottom right corner. The background features a dynamic, abstract pattern of numerous thin, curved lines in shades of purple and blue, which curve from the left side towards the center and right side of the frame.

Thank You