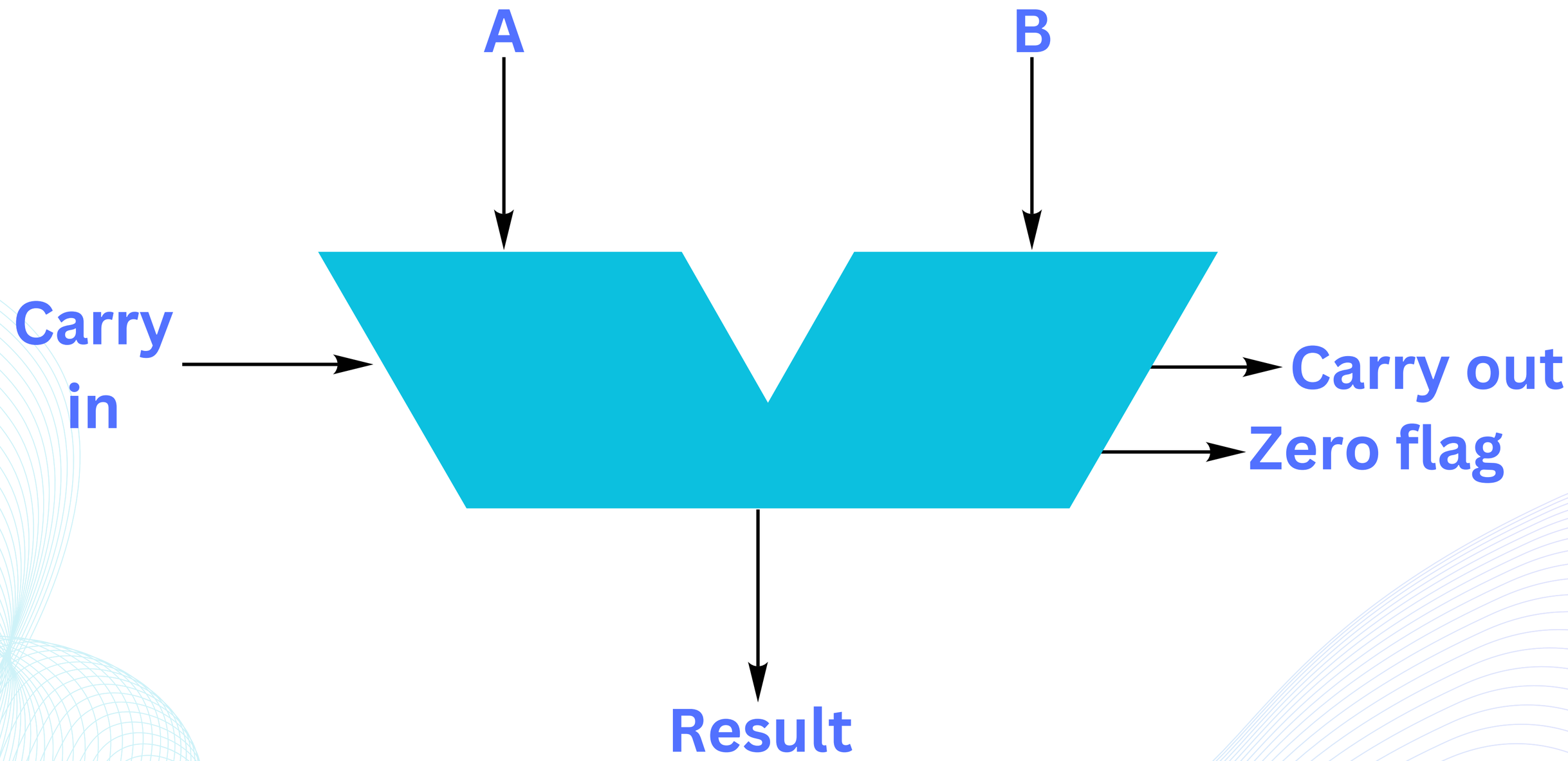
Youssef Ahmed

Design and UVM Verification of an ALU

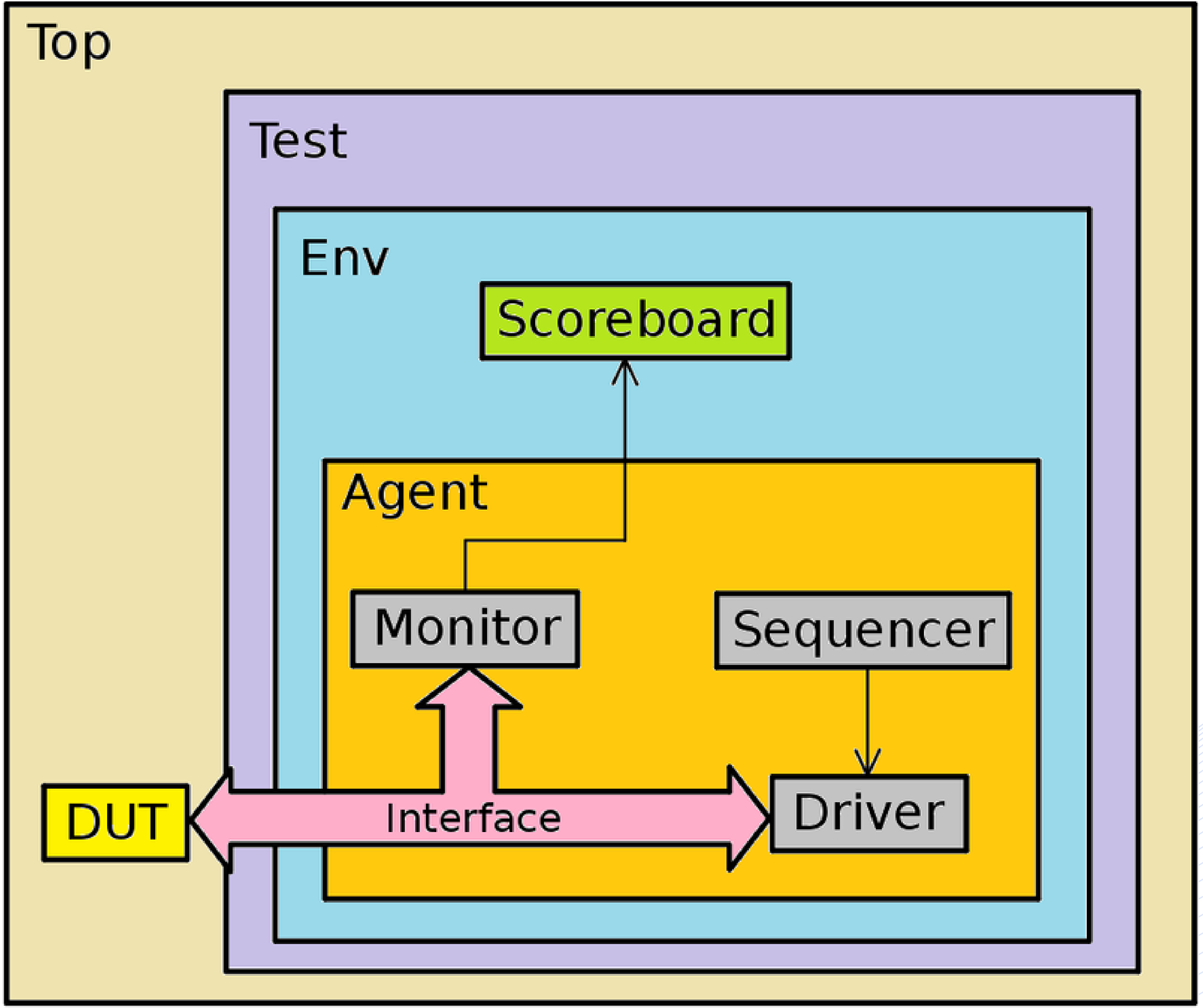
ALU

it stands for Arithmetic and Logic Unit. It is a digital circuit or a functional block within a central processing unit (CPU) that performs arithmetic and logical operations on binary data. The ALU is responsible for carrying out basic arithmetic operations such as addition, subtraction, multiplication, and division, as well as logical operations like AND, OR, XOR, and bit shifting.

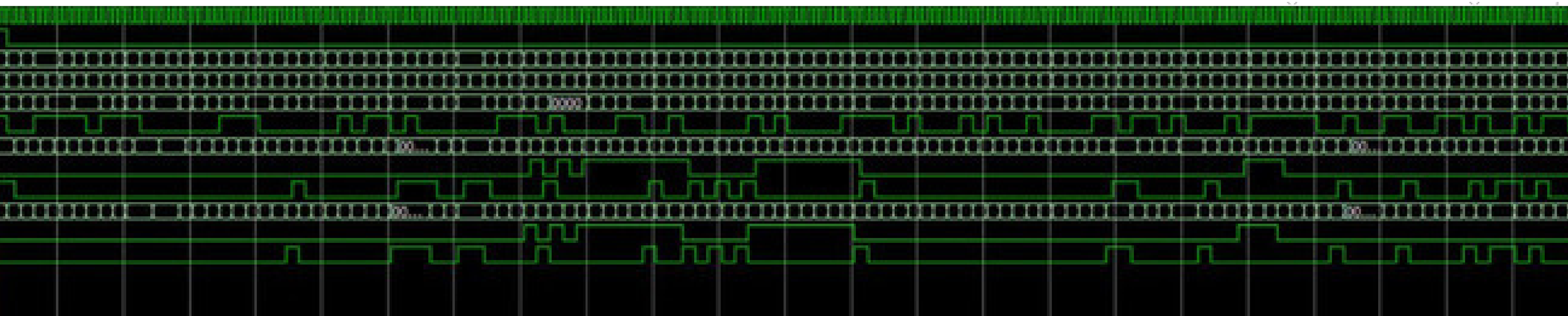
THE DESIGN SCHEMATIC OF THE ALU

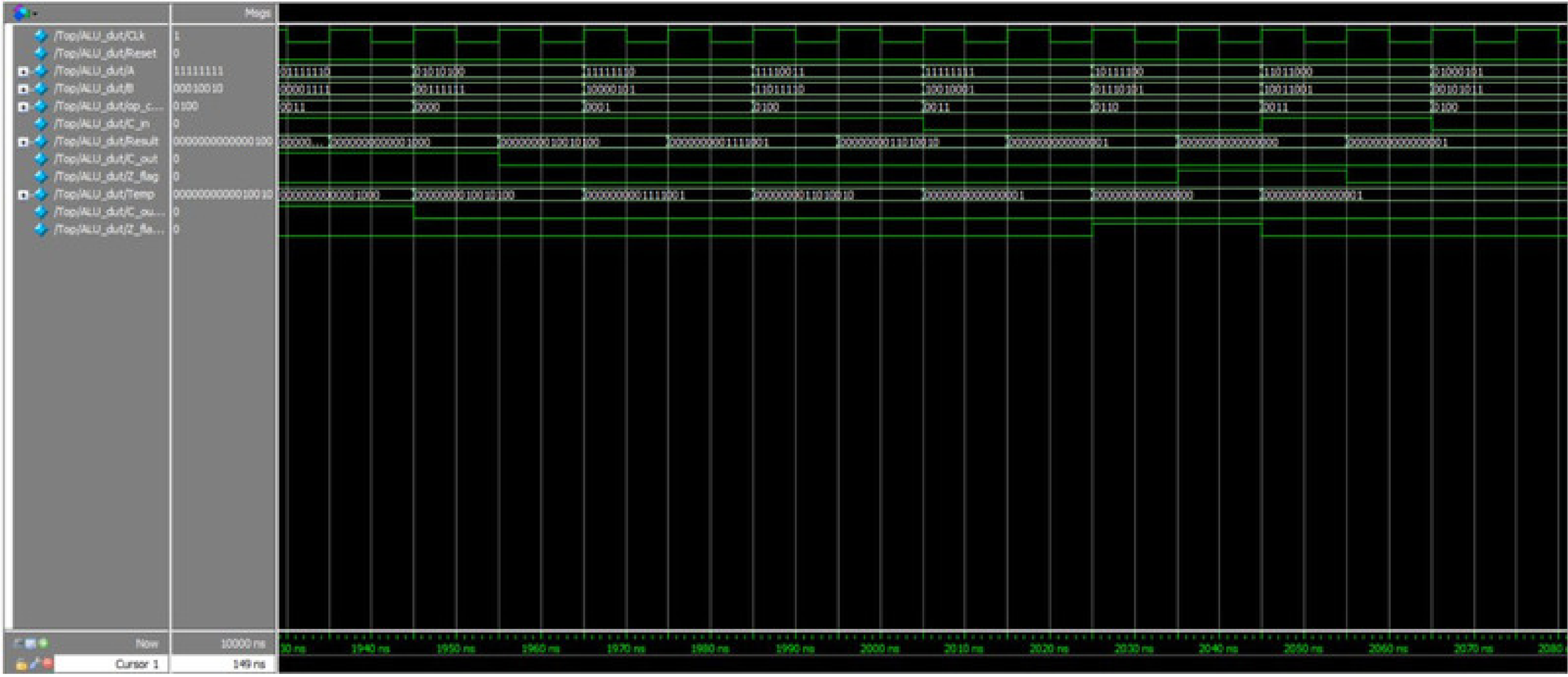

A
B
Carry in
Carry out
Zero flag
Result

UVM TESTBENCH ARCHITECTURE


Top
Test
Env
Scoreboard
Agent
Monitor
Sequencer
DUT
Interface
Driver

THE SIMULATION RESULTS




Msgs
/Top/ALU_dut/Clk
/Top/ALU_dut/Reset
/Top/ALU_dut/A
/Top/ALU_dut/B
/Top/ALU_dut/op_c...
/Top/ALU_dut/C_in
/Top/ALU_dut/Result
/Top/ALU_dut/C_out
/Top/ALU_dut/Z_flag
/Top/ALU_dut/Temp
/Top/ALU_dut/C_ou...
/Top/ALU_dut/Z_fla...
Now
10000 ns
Cursor 1
149 ns
1940 ns
1950 ns
1960 ns
1970 ns
1980 ns
1990 ns
2000 ns
2010 ns
2020 ns
2030 ns
2040 ns
2050 ns
2060 ns
2070 ns

THE LOG RESULTS OF THE TEST

```
VSIM 33> vsim -voptargs=+acc work.Top
# vsim -voptargs=+acc work.Top
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
#           File in use by:   Hostname:   ProcessID: 3
#           Attempting to use alternate WLF file "./wlft33gf9a".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
#           Using alternate file: ./wlft33gf9a
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading sv_std.std
# Loading mtiUvm.uvm_pkg
# Loading work.ALU_pkg
# Loading work.Top(fast)
# Loading work.ALU_interface(fast)
# Loading work.DUT(fast)
# Loading C:\questasim_10.0b\uvm-1.0p1\win32\uvm_dpi.dll
add wave \
/Top/ALU_dut/CLk \
/Top/ALU_dut/Reset \
/Top/ALU_dut/A \
/Top/ALU_dut/B \
/Top/ALU_dut/op_code \
/Top/ALU_dut/C_in \
/Top/ALU_dut/Result \
/Top/ALU_dut/C_out \
/Top/ALU_dut/Z_flag \
/Top/ALU_dut/Temp \
/Top/ALU_dut/C_out_t \
/Top/ALU_dut/Z_flag_t
VSIM 35> run -all
```

```
# ----------------------------------------------------------------
# UVM-1.0p1
# (C) 2007-2011 Mentor Graphics Corporation
# (C) 2007-2011 Cadence Design Systems, Inc.
# (C) 2006-2011 Synopsys, Inc.
# ----------------------------------------------------------------
# UVM_INFO ALU_Test.sv(27) @ 0: uvm_test_top [ALU_Test]  Inside constructor of ALU_Test class
# UVM_INFO @ 0: reporter [RNTST] Running test ALU_Test...
# UVM_INFO ALU_Test.sv(39) @ 0: uvm_test_top [ALU_Test]  Inside build phase of ALU_Test class
# UVM_INFO Environment.sv(25) @ 0: uvm_test_top.ALU_environment [Environment]  Inside constructor of Environment Class
# UVM_INFO Environment.sv(39) @ 0: uvm_test_top.ALU_environment [Environment]  Inside build_phase of Environment Class
# UVM_INFO Agent.sv(27) @ 0: uvm_test_top.ALU_environment.ALU_agent [Agent]  Inside constructor of Agent Class
# UVM_INFO Scoreborad.sv(25) @ 0: uvm_test_top.ALU_environment.ALU_scoreborad [Scoreborad]  Inside constructor of Scoreborad class
# UVM_INFO Agent.sv(41) @ 0: uvm_test_top.ALU_environment.ALU_agent [Agent]  Inside build_phase of Agent Class
# UVM_INFO Monitor.sv(23) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_monitor [Monitor]  Inside constructor of Monitor Class
# UVM_INFO Driver.sv(20) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_driver [Driver] Inside constructor of Driver class
# UVM_INFO Sequencer.sv(18) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_sequencer [Sequencer]  Inside constructor of Sequencer Class
# UVM_INFO Driver.sv(32) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_driver [Driver] Inside build phase of Driver class
# UVM_INFO Monitor.sv(37) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_monitor [Monitor]  Inside build_phase of Monitor Class
# UVM_INFO Sequencer.sv(32) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_sequencer [Sequencer]  Inside build_phase of Sequencer Class
# UVM_INFO Scoreborad.sv(39) @ 0: uvm_test_top.ALU_environment.ALU_scoreborad [Scoreborad]  Inside build phase of Scoreborad class
# UVM_INFO Driver.sv(51) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_driver [Driver] Inside connect phase of Driver class
# UVM_INFO Monitor.sv(59) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_monitor [Monitor]  Inside connect_phase of Monitor Class
# UVM_INFO Sequencer.sv(47) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_sequencer [Sequencer]  Inside connect_phase of Sequencer Class
# UVM_INFO Agent.sv(62) @ 0: uvm_test_top.ALU_environment.ALU_agent [Agent]  Inside connect_phase of Agent Class
# UVM_INFO Scoreborad.sv(54) @ 0: uvm_test_top.ALU_environment.ALU_scoreborad [Scoreborad]  Inside connect phase of Scoreborad class
# UVM_INFO Environment.sv(59) @ 0: uvm_test_top.ALU_environment [Environment]  Inside connect_phase of Environment Class
# UVM_INFO ALU_Test.sv(56) @ 0: uvm_test_top [ALU_Test]  Inside connect phase of ALU_Test class
# UVM_INFO ALU_Test.sv(73) @ 0: uvm_test_top [ALU_Test]  Inside run phase of ALU_Test class
# UVM_INFO Environment.sv(75) @ 0: uvm_test_top.ALU_environment [Environment]  Inside run_phase of Environment Class
# UVM_INFO Scoreborad.sv(85) @ 0: uvm_test_top.ALU_environment.ALU_scoreborad [Scoreborad]  Inside run phase of Scoreborad class
# UVM_INFO Agent.sv(78) @ 0: uvm_test_top.ALU_environment.ALU_agent [Agent]  Inside run_phase of Agent Class
# UVM_INFO Sequencer.sv(60) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_sequencer [Sequencer]  Inside run_phase of Sequencer Class
# UVM_INFO Monitor.sv(73) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_monitor [Monitor]  Inside run_phase of Monitor Class
# UVM_INFO Driver.sv(64) @ 0: uvm_test_top.ALU_environment.ALU_agent.ALU_driver [Driver] Inside run phase of Driver class
# 1
# Break in Module Top at C:/questasim_10.0b/examples/Top.sv line 74
```

FOR MORE DETAILS CHECK MY GITHUB REPO

THANK YOU

FOR WATCHING