

ITI Summer Training

LAB Spyglass



Results

1- Lint RTL

Goal: lint/rtl

```
1 module mips(  
2     input  clk,reset,  
3     output [15:0] pc_out, alu_result  
4     //,reg3,reg4  
5 );  
6  
7  
8 // [15:0] pc_out_m, alu_result_m;  
9 // logic0, clk_m, reset_m, logic1;  
10  
11 // Core Instantiation  
12 mips_16 mips_core(.clk(clk), .reset(reset), .pc_out(pc_out), .alu_result(alu_result));  
13 /*  
14  
15 XMHA in1(.SMT(logic0), .PU(logic0), .PD(logic0), .O(clk_m), .I(clk));  
16 XMHA in2(.SMT(logic0), .PU(logic0), .PD(logic0), .O(reset_m), .I(reset));  
17  
18
```

Message Tree (Total: 20, Displayed: 4, Waived: 16)

- Design Read (3)
 - DetectTopDesignUnits (1) : Identify the top-level design units in user design.
 - ElabSummary (1) : Generates Elaborated design units Summary data
 - SYNTH_5143 (1) : Initial block is ignored for synthesis
- lint/rtl (1)
 - STARCO5-1.3.1.3 (1) : Asynchronous reset/preset signals must not be used as non-reset/preset or synchronous reset/preset signals

2- Lint RTL enhanced

File Edit View Tools Help Design Setup Goal Setup Analyze Results Reports

Run Goal: lint/lint_rtl_enhanced ☐ Incremental Mode MS IS Waiver Design

Instances

- mips
 - + mips_core

Modules Instances Files Constraints

```

1
2 module mips(
3     input  clk,reset,
4     output [15:0] pc_out, alu_result
5     //,reg3,reg4
6 );
7
8 // [15:0] pc_out_m, alu_result_m;
9 // logic0, clk_m, reset_m, logic1;
10
11 // Core Instantiation
12 mips_16 mips_core(.clk(clk), .reset(reset), .pc_out(pc_out), .alu_result(alu_result));
13 /*
14
15 XMHA in1(SMT(logic0), .PU(logic0), .PD(logic0), .O(clk_m), .I(clk));
mips.v

```

Group By: Goal by Rule

Message	File	Line
Message Tree (Total: 44, Displayed: 7, Waived: 37)		
Design Read (4)		
CMD_overloadrule01 (1) : Overload ignored as rule not registered in run language		
DetectTopDesignUnits (1) : Identify the top-level design units in user design.		
ElabSummary (1) : Generates Elaborated design units Summary data		
SYNTH_5143 (1) : Initial block is ignored for synthesis		
lint/lint_rtl_enhanced (3)		
ReportPortInfo-ML (1) : Generate a report of all ports of top level block and black-box instances.		
STARC05-1.3.1.3 (1) : Asynchronous reset/preset signals must not be used as non-reset/preset or synchronous reset/preset signals		
W240 (1) : An input has been declared but is not read		

Violations

3- RTL Turbo

Run Goal: **lint/lint_turbo_rtl** ☐ Incremental Mode MS IS Waiver Design

Instances

- mips
 - + mips_core

Modules Instances Files Constraints

```

1
2 module mips(
3     input  clk,reset,
4     output [15:0] pc_out, alu_result
5     //,reg3,reg4
6 );
7
8 // [15:0] pc_out_m, alu_result_m;
9 // logic0, clk_m, reset_m, logic1;
10
11 // Core Instantiation
12 mips_16 mips_core(.clk(clk), .reset(reset), .pc_out(pc_out), .alu_result(alu_result));
13 /*
14
15 XMHA in1(.SMT(logic0), .PU(logic0), .PD(logic0), .O(clk_m), .I(clk));
mips.v

```

Group By: **Goal by Rule**

Message	File	Line
Message Tree (Total: 6, Displayed: 5, Waived: 17, Secondary Waived: 16)		
Design Read (4)		
DetectTopDesignUnits (1) : Identify the top-level design units in user design.		
ElabSummary (1) : Generates Elaborated design units Summary data		
SYNTH_5143 (1) : Initial block is ignored for synthesis		
TurboModeStatus (1) : Reports if turbo_struct license feature is successfully checked out or not.		
lint/lint_turbo_rtl (1)		
STARCO5-1.3.1.3 (1) : Asynchronous reset/preset signals must not be used as non-reset/preset or synchronous reset/preset signals		

Violations

4- Lint Functional RTL

Run Goal: **lint/lint_functional_rtl** ☐ Incremental Mode MS IS Waiver Design

Instances

- mips
 - + mips_core

Modules Instances Files Constraints

```

1
2 module mips(
3     input  clk,reset,
4     output [15:0] pc_out, alu_result
5     //,reg3,reg4
6 );
7
8 // [15:0] pc_out_m, alu_result_m;
9 // logic0, clk_m, reset_m, logic1;
10
11 // Core Instantiation
12 mips_16 mips_core(.clk(clk), .reset(reset), .pc_out(pc_out), .alu_result(alu_result));
13 /*
14
15 XMHA in1(.SMT(logic0), .PU(logic0), .PD(logic0), .O(clk_m), .I(clk));
mips.v

```

Group By: **Goal by Rule**

Message	File	Line
Message Tree (Total: 4, Displayed: 4, Waived: 0)		
Design Read (3)		
DetectTopDesignUnits (1) : Identify the top-level design units in user design.		
ElabSummary (1) : Generates Elaborated design units Summary data		
SYNTH_5143 (1) : Initial block is ignored for synthesis		
lint/lint_functional_rtl (1)		
Av_init01 (1) : Reports initial setup issues of the design.		

Violations

5- Lint abstract

The screenshot displays the Lint tool interface during a linting operation. The top toolbar contains icons for File, Edit, View, Tools, Help, Design Setup, Goal Setup, Analyze Results, and Reports. The 'Run Goal' dropdown is set to 'lint/lint_abstract', and the 'Incremental Mode' checkbox is unchecked. The tabs at the top right are MS, IS, Waiver, and Design.

The left pane, labeled 'Instances', shows a tree structure with 'mips' as the root and 'mips_core' as a sub-instance. The right pane displays the Verilog code for 'mips.v'.

```
1
2 module mips(
3     input clk,reset,
4     output [15:0] pc_out, alu_result
5     //,reg3,reg4
6 );
7
8 // [15:0] pc_out_m, alu_result_m;
9 // logic0, clk_m, reset_m, logic1;
10
11 // Core Instantiation
12 mips_16 mips_core(clk(clk), .reset(reset), .pc_out(pc_out), .alu_result(alu_result));
13 /*
14
15 XMHA in1(.SMT(logic0),.PU(logic0),.PD(logic0),.O(clk_m),.I(clk));
16 mips.v
```

The bottom pane, labeled 'Violations', shows the 'Message Tree' with 4 messages. The messages are:

- Design Read (3)
 - DetectTopDesignUnits (1) : Identify the top-level design units in user design.
 - ElabSummary (1) : Generates Elaborated design units Summary data
 - SYNTH_5143 (1) : Initial block is ignored for synthesis
- Lint/lint_abstract (1)
 - LINT_abstract01 (1) : Generates relevant base policy constraints for block abstraction