

ITI Summer Training

LAB Spyglass



Code after editing

```

16 //----- Internal Wires -----
17 //wire [1:0] Inernal_wire1 ; //not read
18 //wire [2:0] Inernal_wire2 ;//not read
19 //wire [3:0] Inernal_wire3 ; //not read

21 //----- Internal Reg -----
22 reg [1:0] Inernal_reg1 ;
23 // [2:0] Inernal_reg2 ; //not read
24 reg [3:0] Inernal_reg3 ;
25

34 else begin
35 Inernal_reg1 <= Data_in1;
36 //Inernal_reg2 <= Data_in2; //not read
37 Inernal_reg3 <= Data_in3;
38 end

60 /* always @(posedge clk)
61 begin
62 Data_out3 <= Data_in3 & Data_out3 ; //multiple drivers
63 end */
64

66 always @(posedge clk, negedge rst_n)
67 begin
68 if (!rst_n)
69 Data_out2 <= 0; //need a reset signal
70 else
71 Data_out2 <= Data_out2 & Data_in2 ;
72 end
73

77 always @( posedge clk, negedge rst_n )
78 begin
79 if (!rst_n)
80 Data_out1 <= 0;
81 //need a reset signal
82 else if (check)
83 begin
84 Data_out1 <= Data_in1 & Inernal_reg1;
85 end

89 always @(*)
90 begin
91 case(Data_in1)
92 2'b00: Data_out3 = Data_in3 & Inernal_reg3 ;
93 2'b01: Data_out3 = Inernal_reg3 ;
94 default : Data_out3 = 0; //default case was missed
95 endcase
96 end

```

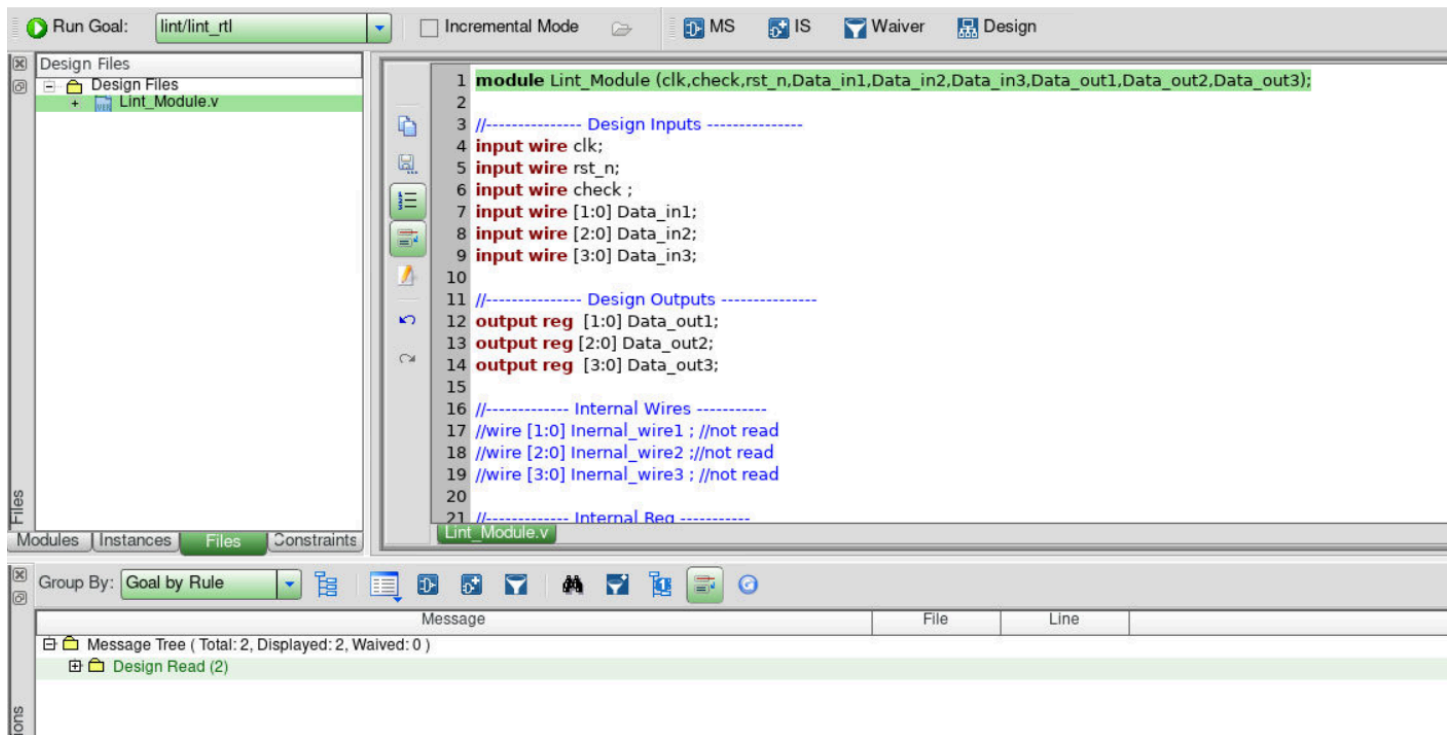
```

100 /*always @(posedge clk)
101 begin|
102 Data_out1 <= Data_in1 & Inernal_reg1;    multiple drivers to the same signal
103 Data_out1 <= Data_in1 | Inernal_reg1;    multiple drivers to the same signal
104 end */
105
106 // Data_out2 = Data_in2 & Inernal_reg2;    multiple drivers to the same signal
107 //assign Data_out2 = Data_in2 | Inernal_reg2;    multiple drivers to the same signal
108
112 //assign Inernal_wire1 = Data_in2 ; not read
113 //assign Inernal_wire2 = Data_in3 ; not read
114 //assign Inernal_wire3 = Data_in1 ; not read
115
118 /* always @(posedge clk )
119 begin
120 Data_out1 <= Data_in1 | Inernal_reg1; multiple drivers
121 Data_out3 <= Data_in3 | Inernal_reg3; multiple drivers
122 end */

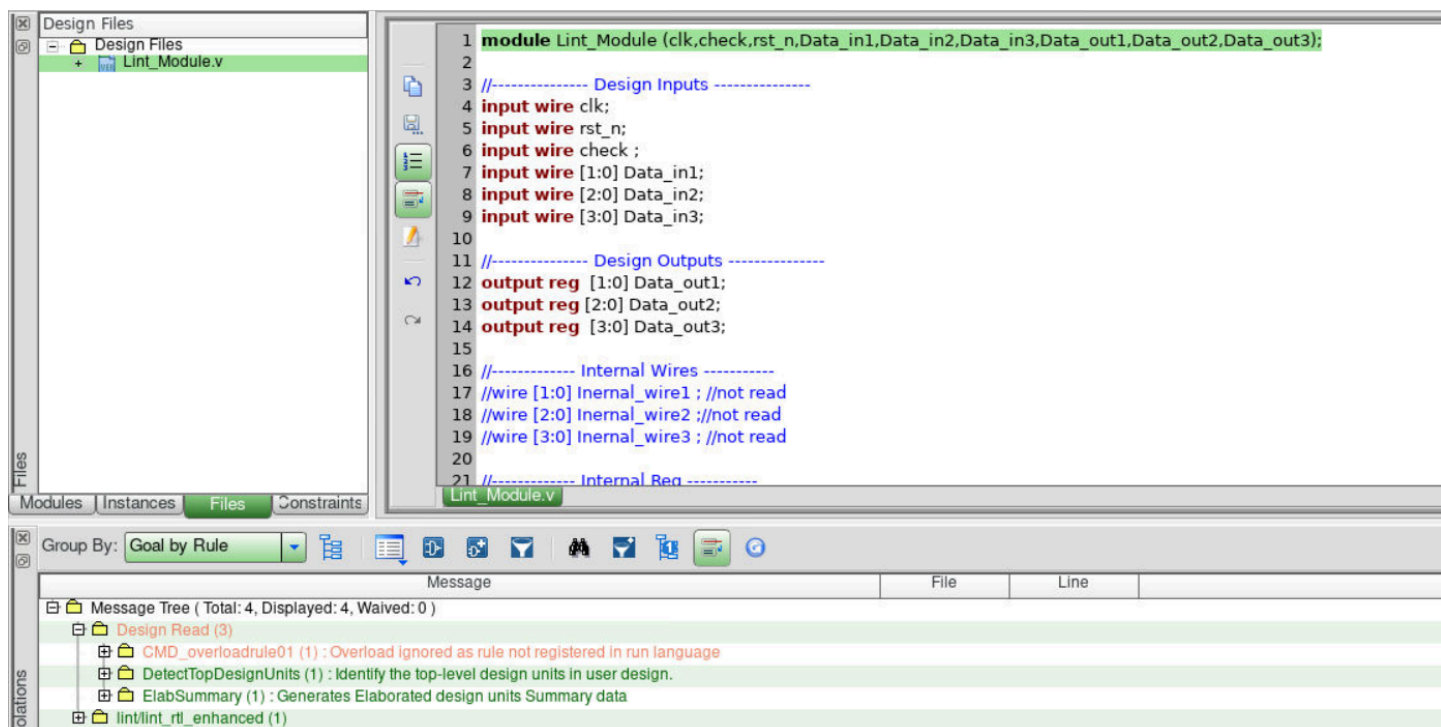
```

Results

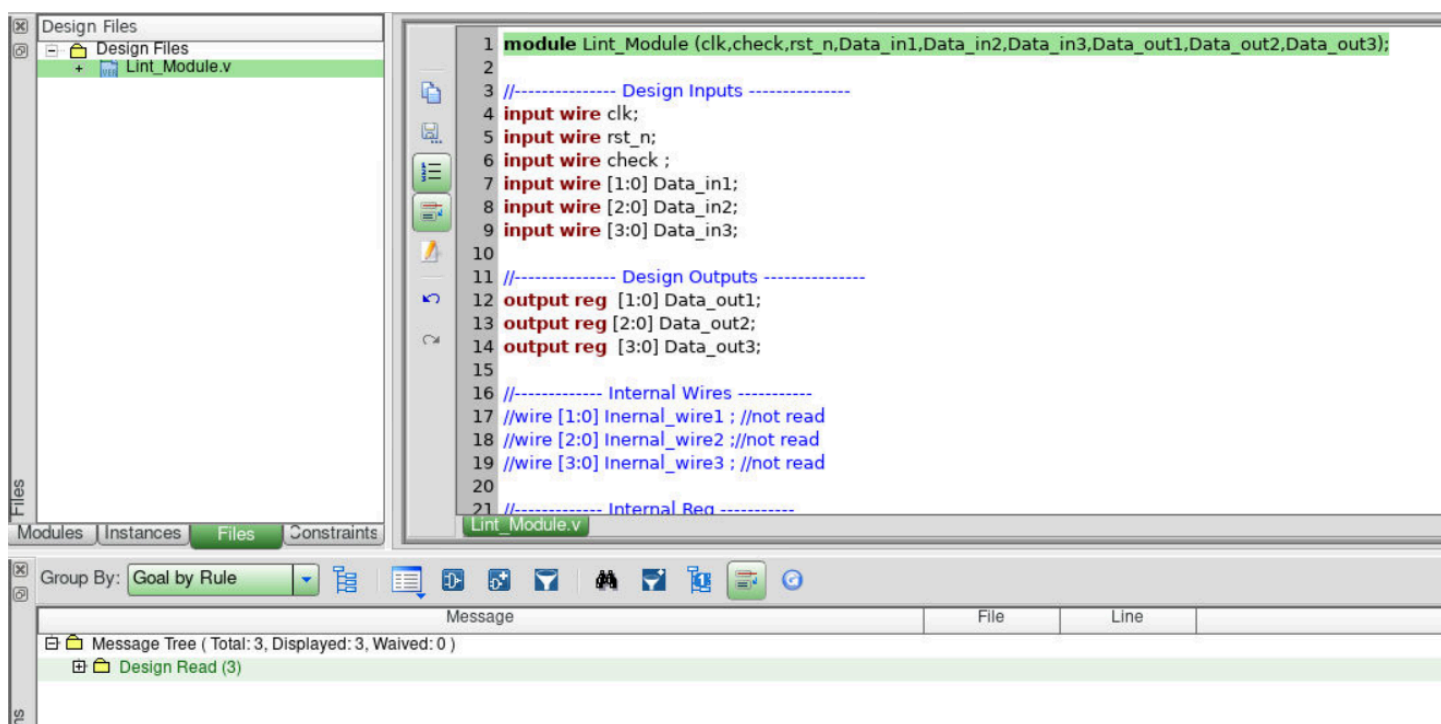
1- Lint RTL



2- Lint RTL enhanced



3- RTL Turbo



4- Lint Functional RTL

The screenshot shows the Lint Module V HDL Editor. The Design Files pane on the left lists 'Lint_Module.v'. The main editor displays the Verilog code for the 'Lint_Module' module, which includes design inputs, outputs, and internal wires. The Message Tree on the bottom left shows a warning from the 'Av_init01' rule: 'Could not find clocks for all the flops. Please add clock SGDC constraint to the design'. The message is associated with 'Lint_Module.v' at line 1.

```

1 module Lint_Module (clk,check,rst_n,Data_in1,Data_in2,Data_in3,Data_out1,Data_out2,Data_out3);
2
3 //----- Design Inputs -----
4 input wire clk;
5 input wire rst_n;
6 input wire check ;
7 input wire [1:0] Data_in1;
8 input wire [2:0] Data_in2;
9 input wire [3:0] Data_in3;
10
11 //----- Design Outputs -----
12 output reg [1:0] Data_out1;
13 output reg [2:0] Data_out2;
14 output reg [3:0] Data_out3;
15
16 //----- Internal Wires -----
17 //wire [1:0] Inernal_wire1 ; //not read
18 //wire [2:0] Inernal_wire2 ;//not read
19 //wire [3:0] Inernal_wire3 ; //not read
20
21 //----- Internal Reg -----

```

Message Tree (Total: 3, Displayed: 3, Waived: 0)

- Design Read (2)
- lint/lint_functional_rtl (1)
 - Av_init01 (1) : Reports initial setup issues of the design.
 - Could not find clocks for all the flops. Please add clock SGDC constraint to the design

Lint_Module.v 1

5- Lint abstract

This screenshot shows the same Lint Module V HDL Editor interface, but the Message Tree now displays a different lint rule: 'lint/lint_abstract (1)'. The Verilog code in the main editor remains the same as in the previous screenshot.

```

1 module Lint_Module (clk,check,rst_n,Data_in1,Data_in2,Data_in3,Data_out1,Data_out2,Data_out3);
2
3 //----- Design Inputs -----
4 input wire clk;
5 input wire rst_n;
6 input wire check ;
7 input wire [1:0] Data_in1;
8 input wire [2:0] Data_in2;
9 input wire [3:0] Data_in3;
10
11 //----- Design Outputs -----
12 output reg [1:0] Data_out1;
13 output reg [2:0] Data_out2;
14 output reg [3:0] Data_out3;
15
16 //----- Internal Wires -----
17 //wire [1:0] Inernal_wire1 ; //not read
18 //wire [2:0] Inernal_wire2 ;//not read
19 //wire [3:0] Inernal_wire3 ; //not read
20
21 //----- Internal Reg -----

```

Message Tree (Total: 3, Displayed: 3, Waived: 0)

- Design Read (2)
- lint/lint_abstract (1)