2. Question 2

2.1. Design code “Moore FSM gray counter”

```verilog
module gray_counter_Moore_FSM (
    input  clk,  /* clock signal input */
    input  arst, /* Active high asynchronous */
    output reg [1:0]y
);
  parameter A = 2'b00;
  parameter B = 2'b01;
  parameter C = 2'b10;
  parameter D = 2'b11;


reg [1:0]CS,NS;     /* CS -> current state  NS -> next state */

// state memory
always @(posedge clk or posedge arst) begin
    if(arst)
        CS <= A;
    else
        CS <= NS;
end

//next state logic
always @(CS) begin
    case(CS)
        A:  NS = B;
        B:  NS = C;
        C:  NS = D;
        D:  NS = A;
    endcase
end

// output logic depends only on Current state
always @(CS) begin
    case(CS)
        A:  y = 2'b00;
        B:  y = 2'b01;
        C:  y = 2'b11;
        D:  y = 2'b10;
    endcase
end

endmodule //gray_counter_Moore_FSM
```

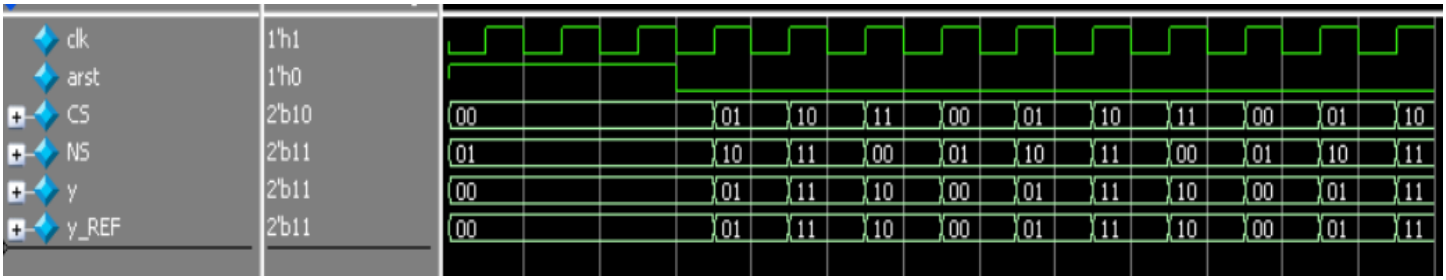
2.2. Reference code “behavioral gray counter”

```
module gray_counter (clk,rst,gray_out);
 input  clk,rst;
 output reg[1:0]gray_out;

 reg [1:0]binary_counter;

 always @(posedge clk or posedge rst) begin
    if(rst)begin
        binary_counter = 0;
        gray_out =0;
    end
    else begin
        binary_counter  = binary_counter +1;
        gray_out[0] = binary_counter[0]^binary_counter[1];
        gray_out[1] = binary_counter[1];
    end
 end
endmodule
```

2.3. Testbench

```
module gray_counter_moore_FSM_tb();
    /*--------------Inputs--------------*/
    reg clk;
    reg arst;
    /*--------------outputs-------------*/
    wire [1:0]y;
    wire [1:0]y_REF;
    /*---Instantiation of DUT and Ref---*/
    gray_counter_Moore_FSM DUT (.*);
    gray_counter REF (clk,arst,y_REF);
    // Clock generation
    initial begin
        clk = 0;
        forever #5 clk = ~clk; // 10 ns period
    end
    /*--------Stimulus process---------*/
    initial begin
        $display("start Simulation");
        //test the reset signal
        arst=1;
        #30;
        arst= 0;

        // wait 100ns to check the functionality
        #100;
        $display("End Simulation");
        $stop;
    end
    /*--------Monitor testing--------*/
    initial begin
        $monitor("Y_DUT = %b --- Y_REF = %b ",y,y_REF);
    end

endmodule

```

2.4. QuestaSim Waveform



2.5. Transcript

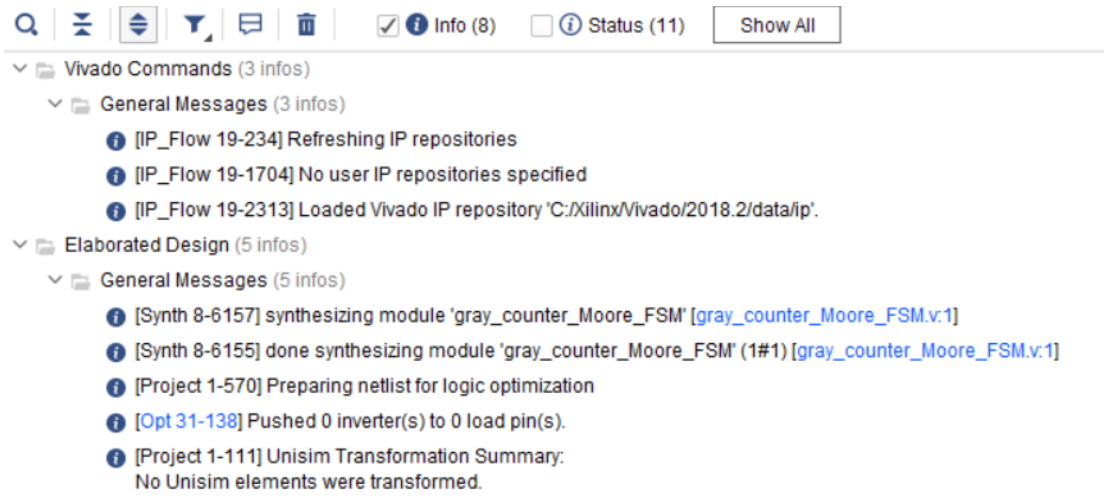
```
# start Simulation
# Y_DUT = 00 --- Y_REF = 00
# Y_DUT = 01 --- Y_REF = 01
# Y_DUT = 11 --- Y_REF = 11
# Y_DUT = 10 --- Y_REF = 10
# Y_DUT = 00 --- Y_REF = 00
# Y_DUT = 01 --- Y_REF = 01
# Y_DUT = 11 --- Y_REF = 11
# Y_DUT = 10 --- Y_REF = 10
# Y_DUT = 00 --- Y_REF = 00
# Y_DUT = 01 --- Y_REF = 01
# Y_DUT = 11 --- Y_REF = 11
# End Simulation
```

2.6. Constrains File

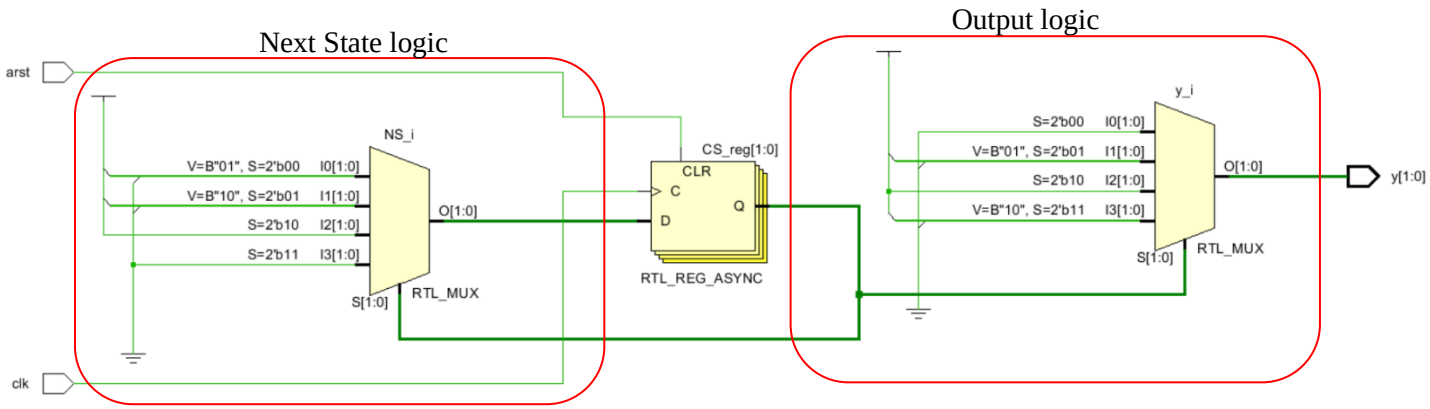
```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name clk -period 10.00 -waveform {0 5} [get_ports clk]

## LEDs
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {y[0]}]
set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {y[1]}]

##Buttons
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports arst]

## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

2.7. Elaboration

2.7.1. Messages Tab

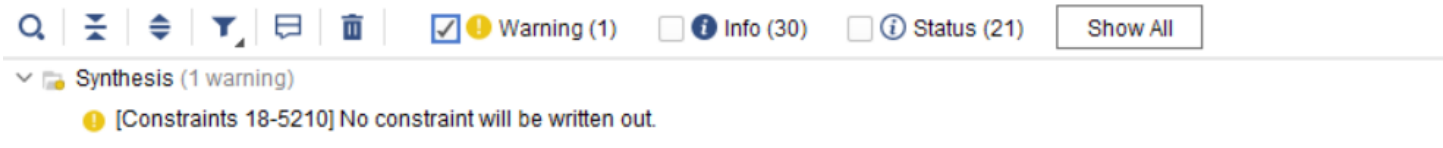


2.7.2. Schematic

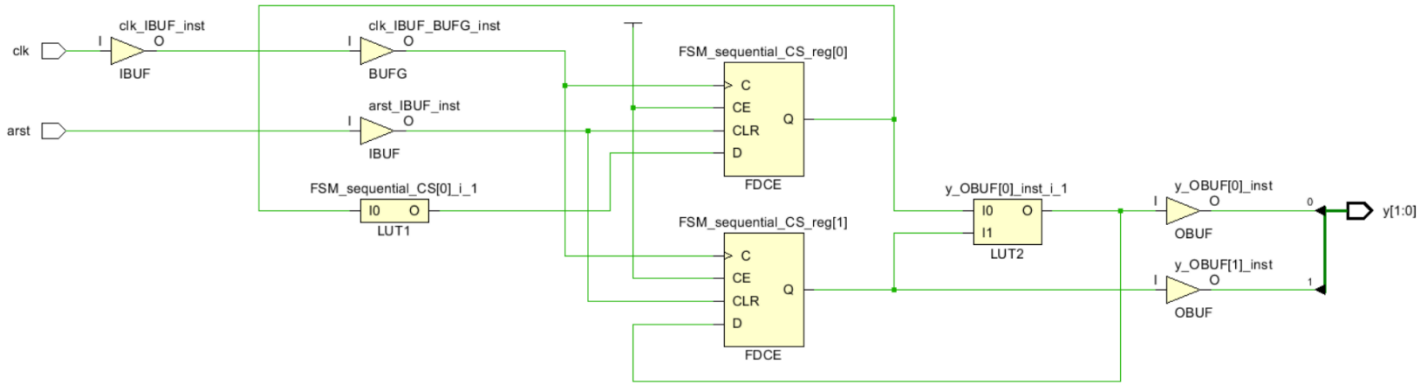


2.8. Synthesis

2.8.1. Messages Tab



2.8.2. Schematic



2.8.3. Report Timing summary

Design Timing Summary

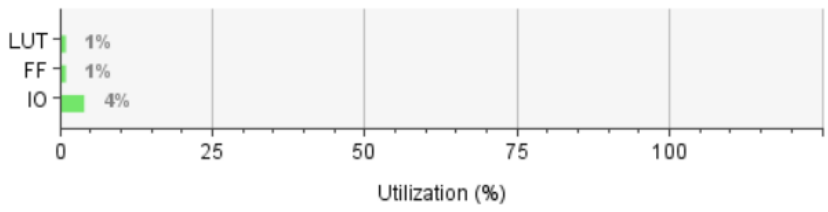
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.617 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2	Total Number of Endpoints:	2	Total Number of Endpoints:	3

All user specified timing constraints are met.

2.8.4. Utilization Report Summary

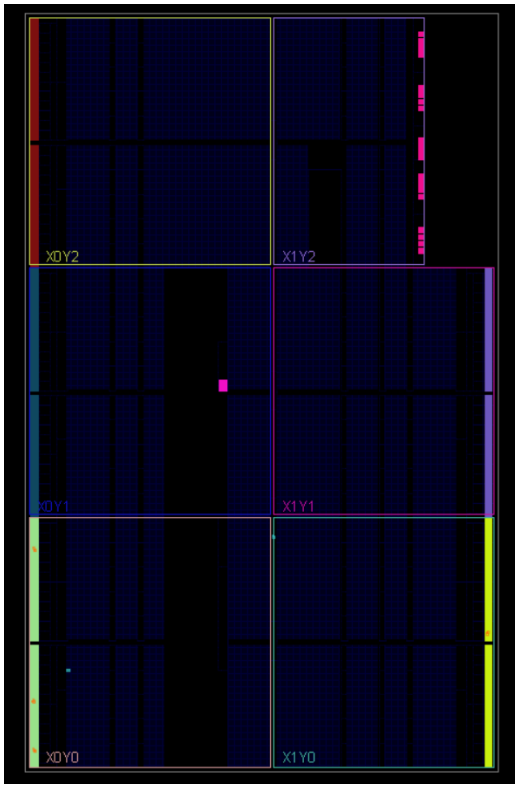
Summary

Resource	Utilization	Available	Utilization %
LUT	2	20800	0.01
FF	2	41600	0.00
IO	4	106	3.77



2.9. Implementation

2.9.1. Device Schematic



2.9.2. Report Timing Summary

Design Timing Summary

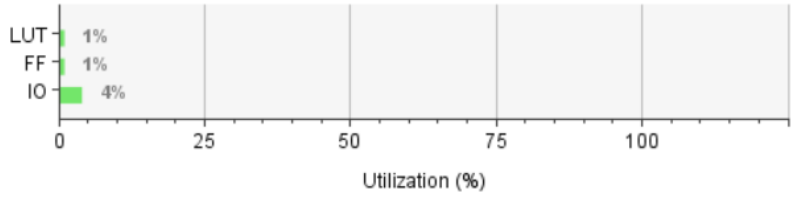
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.019 ns	Worst Hold Slack (WHS):	0.367 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2	Total Number of Endpoints:	2	Total Number of Endpoints:	3

All user specified timing constraints are met.

2.10. Utilization Report Summary

Summary

Resource	Utilization	Available	Utilization %
LUT	2	20800	0.01
FF	2	41600	0.00
IO	4	106	3.77



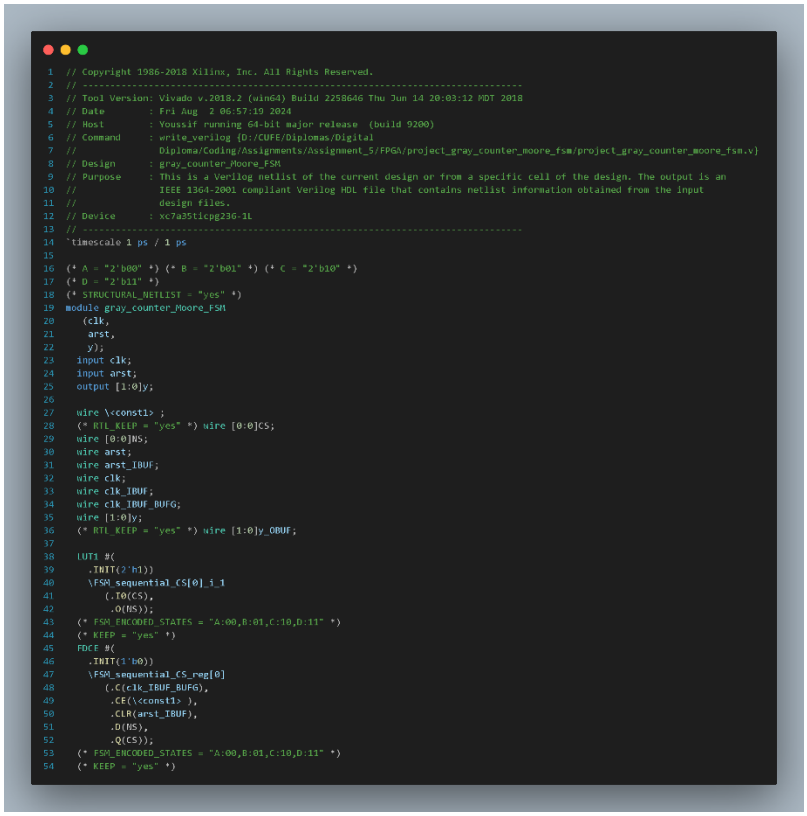
2.11. Generate Bitstream

Implementation				
impl_1				
Design Initialization (init_design)				
Opt Design (opt_design)				
Power Opt Design (power_opt_design)				
Place Design (place_design)				
impl_1_place_report_io_0	Report information about all the IO sites on the device (report_io)		8/2/24 5:45 AM	72.1 KB
impl_1_place_report_utilization_0	Report on utilization of resources on the targeted device (report_utilization)		8/2/24 5:45 AM	8.5 KB
impl_1_place_report_control_sets_0	Report the unique control sets in design (report_control_sets)		8/2/24 5:45 AM	2.9 KB
impl_1_place_report_incremental_reuse_0	Report on achievable incremental reuse for the given design-checkpoint (report_incremental_reuse)			
impl_1_place_report_incremental_reuse_1	Report on achievable incremental reuse for the given design-checkpoint (report_incremental_reuse)			
impl_1_place_report_timing_summary_0	Report timing summary (report_timing_summary)			
Post-Place Power Opt Design (post_place_power_opt_design)				
Post-Place Phys Opt Design (phys_opt_design)				
Route Design (route_design)				
impl_1_route_report_drc_0	Report on error or violations against a set of design rule checks (report_drc)		8/2/24 5:45 AM	1.4 KB
impl_1_route_report_methodology_0	Report on error or violations against a set of methodology checks (report_methodology)		8/2/24 5:45 AM	2.1 KB
impl_1_route_report_power_0	Report power analysis details (report_power)		8/2/24 5:45 AM	7.6 KB
impl_1_route_report_route_status_0	Report on status of the routing. (report_route_status)		8/2/24 5:45 AM	0.6 KB
impl_1_route_report_timing_summary_0	Report timing summary (report_timing_summary)		8/2/24 5:45 AM	25.3 KB
impl_1_route_report_incremental_reuse_0	Report on achievable incremental reuse for the given design-checkpoint (report_incremental_reuse)			
impl_1_route_report_clock_utilization_0	Report information about clock nets in design (report_clock_utilization)		8/2/24 5:45 AM	10.5 KB
impl_1_route_report_bus_skew_0	Report on calculated bus skew among the signals constrained by set_bus_skew (report_bus_skew)		8/2/24 5:45 AM	1.0 KB
impl_1_route_implementation_log_0	Vivado Implementation Log		8/2/24 5:50 AM	28.8 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Write Bitstream (write_bitstream)				
impl_1_bitstream_report_webtalk_0	Webtalk Report		8/2/24 5:50 AM	20.4 KB
impl_1_bitstream_implementation_log_0	Vivado Implementation Log		8/2/24 5:50 AM	28.8 KB

2.12. Netlist generation

project_gray_counter_moore_fsm.edn	8/2/2024 6:57 AM	Extensible Data N...	7 KB
project_gray_counter_moore_fsm.v	8/2/2024 6:57 AM	V File	3 KB

2.12.1. Snippet from netlist file



```
// Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
// ----------------------------------------------------------------------------
// Tool Version: Vivado v.2018.2 (win64) Build 2258646 Thu Jun 14 20:03:12 MDT 2018
// Date        : Fri Aug  2 06:57:19 2024
// Host        : Youssif running 64-bit major release  (build 9200)
// Command     : write_verilog {D:/CUFE/Diplomas/Digital
//               Diploma/Coding/Assignments/Assignment_5/FPGA/project_gray_counter_moore_fsm/project_gray_counter_moore_fsm.v}
// Design      : gray_counter_Moore_FSM
// Purpose     : This is a Verilog netlist of the current design or from a specific cell of the design. The output is an
//               IEEE 1364-2001 compliant Verilog HDL file that contains netlist information obtained from the input
//               design files.
// Device      : xc7a35ticpg236-1L
// ----------------------------------------------------------------------------
`timescale 1 ps / 1 ps

(* A = "2'b00" *) (* B = "2'b01" *) (* C = "2'b10" *)
(* D = "2'b11" *)
(* STRUCTURAL_NETLIST = "yes" *)
module gray_counter_Moore_FSM
   (clk,
    arst,
    y);
  input clk;
  input arst;
  output [1:0]y;

  wire \<const1> ;
  (* RTL_KEEP = "yes" *) wire [0:0]CS;
  wire [0:0]NS;
  wire arst;
  wire arst_IBUF;
  wire clk;
  wire clk_IBUF;
  wire clk_IBUF_BUFG;
  wire [1:0]y;
  (* RTL_KEEP = "yes" *) wire [1:0]y_OBUF;

  LUT1 #(
    .INIT(2'h1))
    \FSM_sequential_CS[0]_i_1
       (.I0(CS),
        .O(NS));
  (* FSM_ENCODED_STATES = "A:00,B:01,C:10,D:11" *)
  (* KEEP = "yes" *)
  FDCE #(
    .INIT(1'b0))
    \FSM_sequential_CS_reg[0]
       (.C(clk_IBUF_BUFG),
        .CE(\<const1> ),
        .CLR(arst_IBUF),
        .D(NS),
        .Q(CS));
  (* FSM_ENCODED_STATES = "A:00,B:01,C:10,D:11" *)
  (* KEEP = "yes" *)
```