

5. Question 5

5.1. Snippet after instantiation of IP modules

```
1 wire [5:0]adder_out,multiplier_out;
2 /* Adder IP Instantiation */
3 generate
4     if(FULL_ADDER = "ON")
5         c_addsub_0 adder_mod (
6             .A(A_r),          // input wire [2 : 0] A
7             .B(B_r),          // input wire [2 : 0] B
8             .C_IN(cin_r),      // input wire C_IN
9             .S(adder_out)      // output wire [3 : 0] S
10        );
11     else if(FULL_ADDER = "OFF")
12         c_addsub_0 adder_mod (
13             .A(A_r),          // input wire [2 : 0] A
14             .B(B_r),          // input wire [2 : 0] B
15             .C_IN(cin_r),      // input wire C_IN
16             .S(adder_out)      // output wire [3 : 0] S
17        );
18 endgenerate
19
20 /* Multiplication IP Instantiation */
21 mult_gen_0 your_instance_name (
22     .A(A_r), // input wire [2 : 0] A
23     .B(B_r), // input wire [2 : 0] B
24     .P(multiplier_out) // output wire [5 : 0] P
25 );
26
27 /* always block for storing the inputs value to D-FF with rising edge of clock if rst is LOW */
28 always @(posedge clk or posedge rst) begin : INPUTS_REGISTRATION
29     if(rst)begin
30         A_r <= 0;
31         B_r <= 0;
32         opcode_r <=0;
33         cin_r <= 0;
34         serial_in_r <= 0;
35         red_op_A_r <= 0;
36         red_op_B_r <= 0;
37         bypass_A_r <= 0;
38         bypass_B_r <= 0;
39         direction_r <= 0;
40         out_r <= 0;
41     end
42     else begin
43         A_r <= A;
44         B_r <= B;
45         opcode_r <= opcode;
46         cin_r <= cin;
47         serial_in_r <= serial_in;
48         red_op_A_r <= red_op_A;
49         red_op_B_r <= red_op_B;
50         bypass_A_r <= bypass_A;
51         bypass_B_r <= bypass_B;
52         direction_r <= direction;
53     end
54     if(bypass_A_r && bypass_B_r)
55         out_r <= First_priority;
56     else if (bypass_A_r)
57         out_r <= A_r;
58     else if (bypass_B_r)
59         out_r <= B_r;
60     else if(~invalid_case)begin
61         case (opcode_r)
62             3'b000 : begin
63                 /* AND operation */
64                 if(red_op_A_r && red_op_B_r) out_r <= &First_priority;
65                 else if(red_op_A_r) out_r <= &A_r;
66                 else if(red_op_B_r) out_r <= &B_r;
67                 else out_r <= A_r & B_r;
68             end
69             3'b001 : begin
70                 /* XOR operation */
71                 if(red_op_A_r && red_op_B_r) out_r <= ^First_priority;
72                 else if(red_op_A_r) out_r <= ^A_r;
73                 else if(red_op_B_r) out_r <= ^B_r;
74                 else out_r <= A_r ^ B_r;
75             end
76             3'b010 :begin
77                 /* addition */
78                 out_r <= adder_out;
79             end
80         endcase
81     end
82 end
```

```

80         3'b011 : begin
81             /* multiplication */
82             out_r <= multiplier_out;
83         end
84         3'b100 : begin
85             /* shift output by 1 */
86             if(direction_r) begin
87                 /* left shift */
88                 out_r <= {out_r[4:0],serial_in_r};
89             end
90             else begin
91                 /* right shift */
92                 out_r <= {serial_in_r,out_r[5:1]};
93             end
94         end
95         3'b101 :
96             /* Rotate output by one */
97             if(direction_r) begin
98                 /* left rotation */
99                 out_r <= {out_r[4:0],out_r[5]};
100             end
101             else begin
102                 /* right rotation */
103                 out_r <= {out_r[0],out_r[5:1]};
104             end
105     endcase
106 end
107 end
108
109 end

```

5.2. 7-Segment Code

```

1 reg [3:0] nibble1, nibble0; // divid the out_r[5:0] into two internal signal
2 reg [1:0] digit_select; // first segment or second or ...
3 reg [18:0] refresh_counter; // 19-bit counter for refreshing the display
4
5 // Clock divider for refreshing the display at ~1kHz (assuming 100MHz input clock)
6 always @(posedge clk or posedge rst) begin
7     if (rst) begin
8         refresh_counter <= 0;
9         digit_select <= 0;
10    end
11    else begin
12        refresh_counter <= refresh_counter + 1;
13        digit_select <= refresh_counter[18:17]; // Digit select based on the refresh counter
14    end
15 end
16
17 always @(*) begin : Seven_Segment
18     nibble0 =out_r[3:0];
19     nibble1 ={2'b00,out_r[5:4]};
20     if(invalid_case)begin
21         case(digit_select)
22             2'b00:
23                 anode = 4'b1110;
24                 // activate LED1 and Deactivate LED2, LED3, LED4
25                 cathode = 7'b1001100; // "4"
26             2'b01:
27                 anode = 4'b1101;
28                 // activate LED2 and Deactivate LED1, LED3, LED4
29                 cathode = 7'b0000001; // "0"
30             2'b10: begin
31                 anode = 4'b1011;
32                 // activate LED3 and Deactivate LED2, LED1, LED4
33                 cathode = 7'b1001100; // "4"
34             end
35             2'b11: begin
36                 anode = 4'b0111;
37                 // activate LED4 and Deactivate LED2, LED3, LED1
38                 cathode = 7'b0110000; // "E"
39             end
40         endcase

```

```

41     end else begin
42         case(digit_select)
43             2'b00:
44                 anode = 4'b1110;
45                 // activate LED1 and Deactivate LED2, LED3, LED4
46                 case(nibble0)
47                     4'b0000: cathode = 7'b0000001; // "0"
48                     4'b0001: cathode = 7'b1001111; // "1"
49                     4'b0010: cathode = 7'b0010010; // "2"
50                     4'b0011: cathode = 7'b0000110; // "3"
51                     4'b0100: cathode = 7'b1001100; // "4"
52                     4'b0101: cathode = 7'b0100100; // "5"
53                     4'b0110: cathode = 7'b0100000; // "6"
54                     4'b0111: cathode = 7'b0001111; // "7"
55                     4'b1000: cathode = 7'b0000000; // "8"
56                     4'b1001: cathode = 7'b0000100; // "9"
57                     4'b1010: cathode = 7'b0001000; // "A"
58                     4'b1011: cathode = 7'b0000000; // "B"
59                     4'b1100: cathode = 7'b0110001; // "C"
60                     4'b1101: cathode = 7'b1000010; // "d"
61                     4'b1110: cathode = 7'b0110000; // "E"
62                     4'b1111: cathode = 7'b0111000; // "F"
63                     default: cathode = 7'b1111110; // "-"
64                 endcase
65             2'b01:
66                 anode = 4'b1101;
67                 // activate LED2 and Deactivate LED1, LED3, LED4
68                 case(nibble1)
69                     4'b0000: cathode = 7'b0000001; // "0"
70                     4'b0001: cathode = 7'b1001111; // "1"
71                     4'b0010: cathode = 7'b0010010; // "2"
72                     4'b0011: cathode = 7'b0000110; // "3"
73                     4'b0100: cathode = 7'b1001100; // "4"
74                     4'b0101: cathode = 7'b0100100; // "5"
75                     4'b0110: cathode = 7'b0100000; // "6"
76                     4'b0111: cathode = 7'b0001111; // "7"
77                     4'b1000: cathode = 7'b0000000; // "8"
78                     4'b1001: cathode = 7'b0000100; // "9"
79                     4'b1010: cathode = 7'b0001000; // "A"
80                     4'b1011: cathode = 7'b0000000; // "B"
81                     4'b1100: cathode = 7'b0110001; // "C"
82                     4'b1101: cathode = 7'b1000010; // "d"
83                     4'b1110: cathode = 7'b0110000; // "E"
84                     4'b1111: cathode = 7'b0111000; // "F"
85                     default: cathode = 7'b1111110; // "-"
86                 endcase
87             2'b10: begin
88                 anode = 4'b1011;
89                 // activate LED3 and Deactivate LED2, LED1, LED4
90                 cathode = 7'b1111110; // "-"
91             end
92             2'b11: begin
93                 anode = 4'b0111;
94                 // activate LED4 and Deactivate LED2, LED3, LED1
95                 cathode = 7'b1111110; // "-"
96             end
97         endcase
98     end
99 end
100 endmodule

```

5.3. Constrains File

```
1  ## This file is a general .xdc for the Basys3 rev B board
2  ## To use it in a project:
3  ## - uncomment the lines corresponding to used pins
4  ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
8  create_clock -add -name clk -period 10.00 -waveform {0 5} [get_ports clk]
9
10 ## Switches
11 set_property -dict { PACKAGE_PIN V17    IOSTANDARD LVCMOS33 } [get_ports {opcode[0]}]
12 set_property -dict { PACKAGE_PIN V16    IOSTANDARD LVCMOS33 } [get_ports {opcode[1]}]
13 set_property -dict { PACKAGE_PIN W16    IOSTANDARD LVCMOS33 } [get_ports {opcode[2]}]
14 set_property -dict { PACKAGE_PIN W17    IOSTANDARD LVCMOS33 } [get_ports {A[0]}]
15 set_property -dict { PACKAGE_PIN W15    IOSTANDARD LVCMOS33 } [get_ports {A[1]}]
16 set_property -dict { PACKAGE_PIN V15    IOSTANDARD LVCMOS33 } [get_ports {A[2]}]
17 set_property -dict { PACKAGE_PIN W14    IOSTANDARD LVCMOS33 } [get_ports {B[0]}]
18 set_property -dict { PACKAGE_PIN W13    IOSTANDARD LVCMOS33 } [get_ports {B[1]}]
19 set_property -dict { PACKAGE_PIN V2     IOSTANDARD LVCMOS33 } [get_ports {B[2]}]
20 set_property -dict { PACKAGE_PIN T3     IOSTANDARD LVCMOS33 } [get_ports {cin}]
21 set_property -dict { PACKAGE_PIN T2     IOSTANDARD LVCMOS33 } [get_ports {red_op_A}]
22 set_property -dict { PACKAGE_PIN R3     IOSTANDARD LVCMOS33 } [get_ports {red_op_B}]
23 set_property -dict { PACKAGE_PIN W2     IOSTANDARD LVCMOS33 } [get_ports {bypass_A}]
24 set_property -dict { PACKAGE_PIN U1     IOSTANDARD LVCMOS33 } [get_ports {bypass_B}]
25 set_property -dict { PACKAGE_PIN T1     IOSTANDARD LVCMOS33 } [get_ports {direction}]
26 set_property -dict { PACKAGE_PIN R2     IOSTANDARD LVCMOS33 } [get_ports {serial_in}]
27
28
29 ## leds
30 set_property -dict { PACKAGE_PIN U16    IOSTANDARD LVCMOS33 } [get_ports {leds[0]}]
31 set_property -dict { PACKAGE_PIN E19    IOSTANDARD LVCMOS33 } [get_ports {leds[1]}]
32 set_property -dict { PACKAGE_PIN U19    IOSTANDARD LVCMOS33 } [get_ports {leds[2]}]
33 set_property -dict { PACKAGE_PIN V19    IOSTANDARD LVCMOS33 } [get_ports {leds[3]}]
34 set_property -dict { PACKAGE_PIN W18    IOSTANDARD LVCMOS33 } [get_ports {leds[4]}]
35 set_property -dict { PACKAGE_PIN U15    IOSTANDARD LVCMOS33 } [get_ports {leds[5]}]
36 set_property -dict { PACKAGE_PIN U14    IOSTANDARD LVCMOS33 } [get_ports {leds[6]}]
37 set_property -dict { PACKAGE_PIN V14    IOSTANDARD LVCMOS33 } [get_ports {leds[7]}]
38 set_property -dict { PACKAGE_PIN V13    IOSTANDARD LVCMOS33 } [get_ports {leds[8]}]
39 set_property -dict { PACKAGE_PIN V3     IOSTANDARD LVCMOS33 } [get_ports {leds[9]}]
40 set_property -dict { PACKAGE_PIN W3     IOSTANDARD LVCMOS33 } [get_ports {leds[10]}]
41 set_property -dict { PACKAGE_PIN U3     IOSTANDARD LVCMOS33 } [get_ports {leds[11]}]
42 set_property -dict { PACKAGE_PIN P3     IOSTANDARD LVCMOS33 } [get_ports {leds[12]}]
43 set_property -dict { PACKAGE_PIN N3     IOSTANDARD LVCMOS33 } [get_ports {leds[13]}]
44 set_property -dict { PACKAGE_PIN P1     IOSTANDARD LVCMOS33 } [get_ports {leds[14]}]
45 set_property -dict { PACKAGE_PIN L1     IOSTANDARD LVCMOS33 } [get_ports {leds[15]}]
46
47
48 ##7 Segment Display
49 set_property -dict { PACKAGE_PIN W7     IOSTANDARD LVCMOS33 } [get_ports {cathode[0]}]
50 set_property -dict { PACKAGE_PIN W6     IOSTANDARD LVCMOS33 } [get_ports {cathode[1]}]
51 set_property -dict { PACKAGE_PIN U8     IOSTANDARD LVCMOS33 } [get_ports {cathode[2]}]
52 set_property -dict { PACKAGE_PIN V8     IOSTANDARD LVCMOS33 } [get_ports {cathode[3]}]
53 set_property -dict { PACKAGE_PIN U5     IOSTANDARD LVCMOS33 } [get_ports {cathode[4]}]
54 set_property -dict { PACKAGE_PIN V5     IOSTANDARD LVCMOS33 } [get_ports {cathode[5]}]
55 set_property -dict { PACKAGE_PIN U7     IOSTANDARD LVCMOS33 } [get_ports {cathode[6]}]
56
57 #set_property -dict { PACKAGE_PIN V7     IOSTANDARD LVCMOS33 } [get_ports dp]
58
59 set_property -dict { PACKAGE_PIN U2     IOSTANDARD LVCMOS33 } [get_ports {anode[0]}]
60 set_property -dict { PACKAGE_PIN U4     IOSTANDARD LVCMOS33 } [get_ports {anode[1]}]
61 set_property -dict { PACKAGE_PIN V4     IOSTANDARD LVCMOS33 } [get_ports {anode[2]}]
62 set_property -dict { PACKAGE_PIN W4     IOSTANDARD LVCMOS33 } [get_ports {anode[3]}]
63
64
65 ##Buttons
66 set_property -dict { PACKAGE_PIN U18    IOSTANDARD LVCMOS33 } [get_ports rst]
67
68 ## Configuration options, can be used for all designs
69 set_property CONFIG_VOLTAGE 3.3 [current_design]
70 set_property CFBVSS VCCO [current_design]
71
72 ## SPI configuration mode options for QSPI boot, can be used for all designs
73 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
74 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
75 set_property CONFIG_MODE SPIx4 [current_design]
```

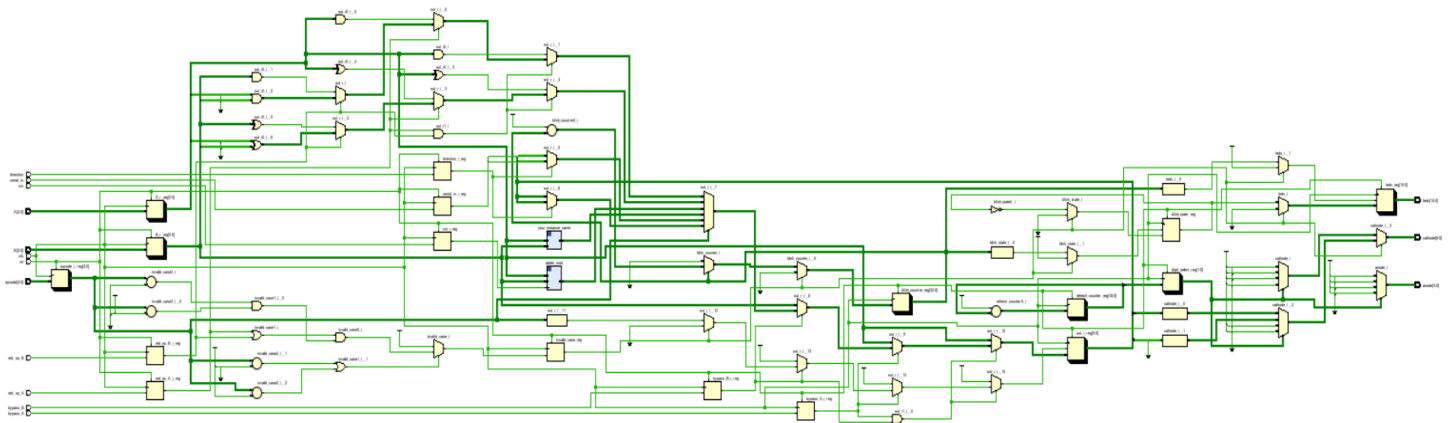
5.4. Elaboration

5.4.1. Messages Tab

☒ Warning (300)
 ☐ Info (84)
 ☐ Status (33)
 Show All

- ▼ Synthesis (150 warnings)
 - ▼ Out-of-Context Module Runs (150 warnings)
 - ▼ c_addsub_0_synth_1 (45 warnings)
 - > [Synth 8-3331] design xbp_dsp48e1_wrapper_v3_0 has unconnected port CE (42 more like this)
 - > [Constraints 18-5210] No constraint will be written out. (1 more like this)
 - ▼ mult_gen_0_synth_1 (105 warnings)
 - > [Synth 8-5640] Port 'zero_detect' is missing in component declaration [[mult_gen_0.vhd:70](#)] (1 more like this)
 - > [Synth 8-5974] attribute "use_dsp48" has been deprecated, please use "use_dsp" instead
 - > [Synth 8-3331] design delay_line has unconnected port CLK (99 more like this)
 - > [Constraints 18-5210] No constraint will be written out. (1 more like this)

5.4.2. Schematic



5.5. Synthesis

5.5.1. Messages Tab

Warning (256)

Info (168)

Status (58)

Show All

Synthesis (128 warnings)

synth_1 (1 warning)

[Constraints 18-5210] No constraint will be written out.

Out-of-Context Module Runs (127 warnings)

c_addsub_0_synth_1 (22 warnings)

[Synth 8-3331] design c_addsub_v12_0_12_lut6_legacy has unconnected port clk (19 more like this)

[Constraints 18-5210] No constraint will be written out. (1 more like this)

mult_gen_0_synth_1 (105 warnings)

[Synth 8-5640] Port 'zero_detect' is missing in component declaration [mult_gen_0.vhd:70] (1 more like this)

[Synth 8-5974] attribute "use_dsp48" has been deprecated, please use "use_dsp" instead

[Synth 8-3331] design delay_line has unconnected port CLK (99 more like this)

[Constraints 18-5210] No constraint will be written out. (1 more like this)

5.5.2. Schematic

5.5.3. Report Timing Summary

Design Timing Summary					
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS): 2.507 ns		Worst Hold Slack (WHS): 0.131 ns		Worst Pulse Width Slack (WPWS): 4.500 ns	
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns		Total Pulse Width Negative Slack (TPWS): 0.000 ns	
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	
Total Number of Endpoints: 70		Total Number of Endpoints: 70		Total Number of Endpoints: 80	
All user specified timing constraints are met.					

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5.6. Implementation

5.6.1. Messages Tab

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5.7. Snippet from the Netlist file

```
1 // Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
2 // -----
3 // Tool Version: Vivado v.2018.2 (win64) Build 2258646 Thu Jun 14 20:03:12 MDT 2018
4 // Date       : Sat Aug  3 23:35:35 2024
5 // Host       : Youssif running 64-bit major release (build 9200)
6 // Command    : write_verilog {D:/CUFE/Diplomas/Digital
7 //             : Diploma/Coding/Assignments/Assignment_5/FPGA/project_ALSU_IP_Catalog/project_ALSU_IP_Catalog.v}
8 // Design     : ALSU
9 // Purpose    : This is a Verilog netlist of the current design or from a specific cell of the design. The output is an
10 //             : IEEE 1364-2001 compliant Verilog HDL file that contains netlist information obtained from the input
11 //             : design files.
12 // Device     : xc7a35t1cp236-1L
13 // -----
14 `timescale 1 ps / 1 ps
15
16 (* FULL_ADDER = "ON" *) (* INPUT_PRIORITY = "A" *)
17 (* STRUCTURAL_NETLIST = "yes" *)
18 module ALSU
19     (clk,
20      rst,
21      A,
22      B,
23      cin,
24      serial_in,
25      red_op_A,
26      red_op_B,
27      opcode,
28      bypass_A,
29      bypass_B,
30      direction,
31      leds,
32      anode,
33      cathode);
34     input clk;
35     input rst;
36     input [2:0]A;
37     input [2:0]B;
38     input cin;
39     input serial_in;
40     input red_op_A;
41     input red_op_B;
42     input [2:0]opcode;
43     input bypass_A;
44     input bypass_B;
45     input direction;
46     output [15:0]leds;
47     output [3:0]anode;
48     output [6:0]cathode;
49
50     wire \<const0> ;
51     wire \<const1> ;
52     wire [2:0]A;
53     wire [2:0]A_IBUF;
54     wire [2:0]A_r;
55     wire [2:0]B;
56     wire [2:0]B_IBUF;
57     wire [2:0]B_r;
58     wire [3:0]adder_out;
59     wire [3:0]anode;
60     wire [3:0]anode_OBUF;
61     wire \blink_counter[0]_i_1_n_0 ;
62     wire \blink_counter[10]_i_1_n_0 ;
63     wire \blink_counter[11]_i_1_n_0 ;
64     wire \blink_counter[12]_i_1_n_0 ;
65     wire \blink_counter[13]_i_1_n_0 ;
66     wire \blink_counter[14]_i_1_n_0 ;
67     wire \blink_counter[15]_i_1_n_0 ;
68     wire \blink_counter[16]_i_1_n_0 ;
69     wire \blink_counter[17]_i_1_n_0 ;
70     wire \blink_counter[18]_i_1_n_0 ;
71     wire \blink_counter[19]_i_1_n_0 ;
72     wire \blink_counter[1]_i_1_n_0 ;
73     wire \blink_counter[20]_i_1_n_0 ;
74     wire \blink_counter[21]_i_1_n_0 ;
75     wire \blink_counter[22]_i_1_n_0 ;
76     wire \blink_counter[23]_i_1_n_0 ;
77     wire \blink_counter[24]_i_1_n_0 ;
```

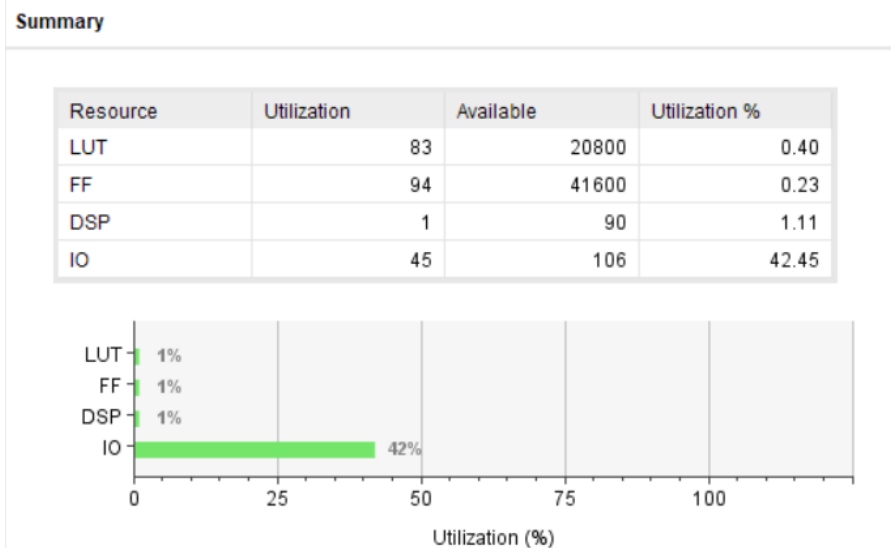

5.8. Utilization Report summary

5.8.1. Hierarchy

Q [] [] [] [] Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	DSP s (90)	Bonded IOB (106)	BUFGCTRL (32)
▼ N ALSU	83	94	47	83	42	1	45	1
> [] adder_mod (c_addsub...	3	0	1	3	0	0	0	0
> [] mult_mod (mult_gen_0)	0	0	0	0	0	1	0	0

5.8.2. Summary



5.9. Bitstream generation

▼ Write Bitstream (write_bitstream)				
[] impl_1_bitstream_report_webtalk_0	Webtalk Report		8/3/24 10:33 PM	25.6 KB
[] impl_1_bitstream_implementation_log_0	Vivado Implementation Log		8/3/24 10:34 PM	29.4 KB