Analog Readout Methods for CMOS (Complementary metal-oxide-semiconductor) Image Sensors Utilizing a Global Feedback

By

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Curriculum Vitae

The author was born in Changchun, Jilin Province, P.R. China on July 23th, 1981. She attended the University of Rochester from 2004 to 2006 as a transfer student from Monroe Community College, and graduated with a Bachelor of Science degree in Electrical and Computer Engineering in 2006. She began graduate studies in the Department of Electrical and Computer Engineering at the University of Rochester from 2006, and received a Master of Science degree in Electrical Engineering in 2008. She has received a research assistantship since then. She pursued her research in CMOS image sensor design under the direction of Professor Zeljko Ignjatovic, where she mainly focused on analog integrated circuit design, simulation and layout, and conducted chip level characterization on the fabricated CMOS image sensor prototype.

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Abstract

Ever since the invention of Charged Coupled Devices (CCD) and CMOS image sensors, there have been tremendous development efforts towards the creation of digital cameras, which rapidly replaced traditional analog and film cameras. Despite their leading role in the market today, most digital cameras still exhibit worse image quality than film cameras. Many efforts have been made to improve the performance of digital images, such as increased dynamic range and reduced readout noise.

As one of the fastest growing industries worldwide, CMOS imaging ranges from high quality digital still cameras to low quality consumer end products. Compared to CCD image sensors, CMOS image sensors allow low power, low cost and on-chip signal processing, which allow them to become more and more prominent. However, the demand for low noise, high readout speed and high dynamic range is still a big concern for CMOS imagers. The goal of this work is to improve the readout time while decreasing the readout noise by employing a modification to the standard Active Pixel Sensor (APS) design to retain high fill factor.

The first part of this work focused on a new design named Current Sensing Active Pixel (CSAP) sensor. The design was an analog CMOS image sensor readout architecture implemented in a standard 0.35 μm CMOS process, operating from a 3.3 V power supply with faster readout settling times than the standard APS design. The standard APS source follower configuration is used in the pixel part of the CSAP

design to obtain a high fill factor. The CSAP design also employed an out-of-pixel readout amplifier in the negative feedback topology with respect to the pixel unit to increase the pixel's current driving capabilities and thereby reduce the settling time at the output. As a result of improved settling time, the 1/f noise contributed by the in-pixel source follower transistor may be significantly reduced by the correlated double sampling (CDS) operation commonly used in analog image sensor readout methods. The fabricated CSAP chip prototype was successfully tested and some of the performance improvements were also demonstrated.

The other part of this thesis was a new design named Reconfigurable Active Pixel Sensor (RAPS). It was also an analog CMOS image sensor readout architecture implemented in a standard 0.35 μm CMOS process operating from a 3.3 V power supply. This design eliminated the need for the external correlated double sampling (CDS) circuit that is used in traditional APS designs. It employed a reconfigurable differential-input readout amplifier that may be used in both the reset and the readout phases of the image sensor operation. As a result, the DC offset was removed, the flicker noise was differentiated, and the reset noise was greatly reduced by employing the amplifier in an active reset configuration. Gain related fixed pattern noise (FPN) was also reduced by the higher open-loop gain of the differential amplifier. This design retained a high fill factor since the pixel unit utilized the same number and size of transistors as the standard APS design.

Table of Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 CCD Image Sensors vs. CMOS Image Sensors

The Nobel Prize winners Willard Boyle and George Smith from Bell Laboratory co-invented the CCD solid state imager in 1969. This invention made it possible to utilize the photoelectric effect to transform light into electrical signals for subsequent measurement. The challenge when designing a CCD image sensor is to gather and read out the signals from a large number of pixels in a short time. This invention has revolutionized imaging applications by allowing light to be captured electronically instead of on film. Digital photography has then become an irreplaceable tool in many fields of research. In the early 1990s, CMOS image sensors have emerged as an alternative technology to CCD, and since then have become the prevalent technology for consumer imaging applications due to their low power, cost effectiveness, and relative ease of integration into other CMOS based electronic products [1].

CCD and CMOS image sensors are two technologies presently used for capturing images digitally. Each has unique strengths and weaknesses having advantages in

different applications. Both types of imagers convert light into electrical charge that is then processed by the readout circuitry and converted to digital values by an analog-to-digital converter (ADC). Figure 1.1 shows a block diagram of a typical CMOS imaging system. In this figure, a scene is focused by a lens through a color filter array onto an image sensor; the image sensor then converts light into electrical signals [2]. These signals then go through analog signal processing such as correlated double sampling (CDS), automatic gain control (AGC), and then are digitized by an on-chip ADC. The digitized electrical signal further goes through the digital processing steps for color processing, image enhancement, and compression.

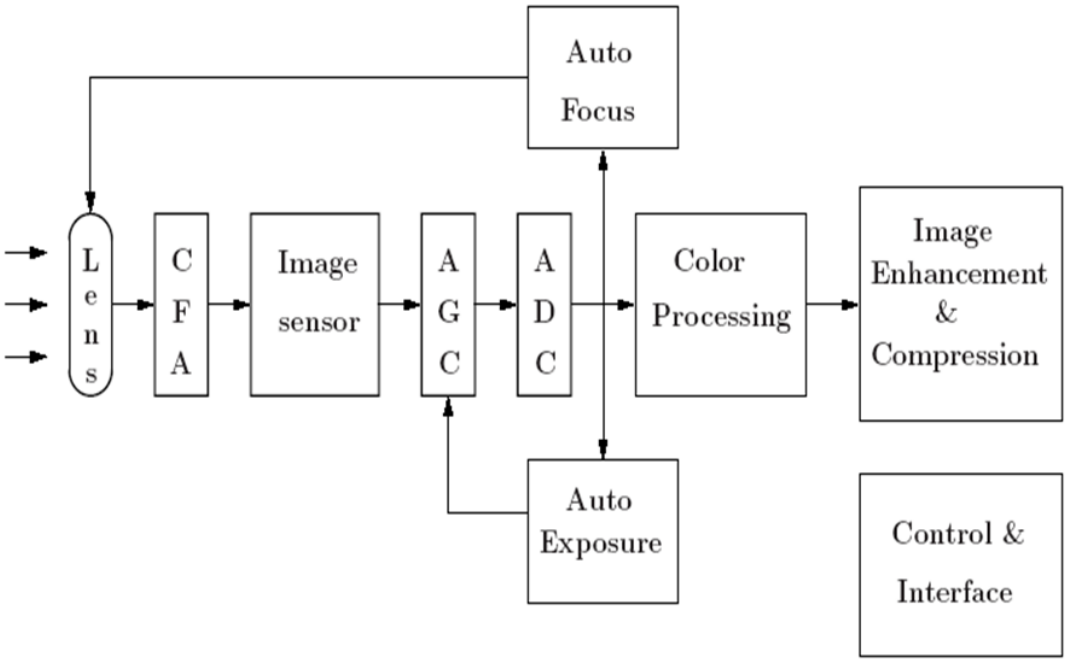

Figure 1.1 Typical CMOS imaging system pipeline

In a CCD sensor, every pixel's charge is transferred through a very limited number of output nodes (often just one) to be converted to voltage, buffered, and sent off-chip as an analog signal. All of the pixel area can be devoted to light capture, and the output's uniformity is high. As opposed to CCD, each pixel in a CMOS image sensor has its own charge-to-voltage conversion circuit, and the sensor often also includes amplifiers, noise-correction, and digitization circuits, so that the chip outputs digital bits. These additional functions increase the design complexity and reduce the area available for light capture. With each pixel performing its own conversion, uniformity is lower. However, the CMOS image sensor usually requires less off-chip circuitry to perform basic imaging operations.

Both CCD and CMOS imagers can offer excellent imaging performance when designed properly. CCDs have traditionally provided the performance benchmarks in the photographic, scientific, and industrial applications that demand the highest image quality at the expense of larger system size and higher cost [3]. On the other hand, CMOS imagers offer more on-chip functionality, lower power dissipation, and the possibility of smaller system size. However, they have often required tradeoffs between higher image quality and lower fabrication cost. CCD technology not only leads to large devices but also consumes high power and costs more than CMOS imagers. The most important advantage of CMOS imaging systems over CCDs is the capability to integrate readout circuits within the pixel arrays, allowing for the most robust design with respect to image performance.

The most significant design challenge in CMOS imagers lies in simultaneously achieving high dynamic range, high fill factor, and high linearity. As battery-powered devices such as the “mobile phone – MP3 player – Internet Appliance – Camera” add more and more features, low power consumption has also emerged as a critical constraint for each subsystem. This factor, combined with the move to higher resolution imagers (more pixels), makes fast low-power pixel readout circuits more important than ever, and in response there has been a great deal of modeling and analysis of CMOS pixel readout circuits to optimize them for readout speed and noise [4].

The principles of converting light [2] are more or less the same in CCD and CMOS imagers, as shown in Figure 1.2. This figure represents the signal path for an image sensor from the incident photon flux to the output voltage. This conversion is almost linear and is represented with three parameters: quantum efficiency, exposure or integration time, and conversion gain. The photo-detector is used to convert incident photons into photocurrent. At the end of the exposure time, photocurrent is integrated into charge, and then charge is converted into voltage for readout using a linear amplifier.

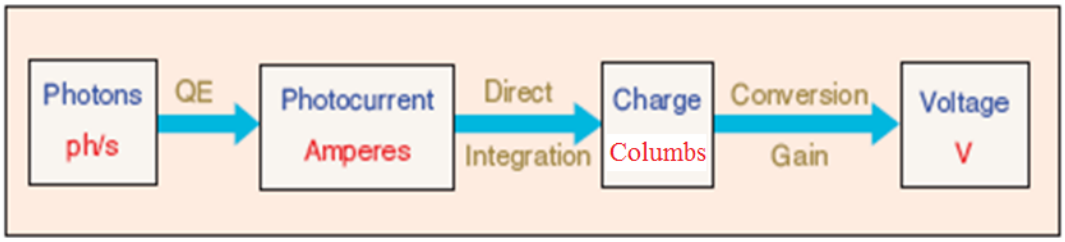

Figure 1.2 Typical image sensor signal path

The image capturing devices in digital cameras are all solid state image sensors. An image sensor array consists of $n \times m$ pixels. Each pixel contains a photo-detector and circuits for reading out the electrical signal. Different types of image sensors have different readout architectures. The pixel size is usually chosen with respect to required dynamic range and fabrication cost. In the following, the difference between CCD and CMOS image sensors is briefly described.

1.1.1 Brief Overview of CCD Image Sensors

CCD image sensors are the most widely used solid state image sensors in the digital camera market today. A CCD is basically an array of closely-spaced metal-oxide-semiconductor (MOS) capacitors that can store and transfer information using packets of electric charge [3]. Applying the proper sequence of clock signals to a CCD biases the array of MOS capacitors into a deep depletion region where the charge packets may be moved in a controlled manner across the semiconductor substrate. The semiconductor substrate of a CCD may be of n or p type. A simplified cross-section of a CCD sensor is shown in Figure 1.3.

In a p-type CCD, grounding the substrate and applying a positive voltage V1 to all the closely-spaced metal electrodes will create a depletion region in the substrate right beneath the oxide layer. If a more positive voltage V2 is now applied at one of the electrodes while maintaining the other electrodes at V1, the depletion region beneath the more positive electrode will extend more deeply into the substrate. This deeper depletion region creates a potential well where minority carriers (electrons) can be accumulated. By applying proper voltage signals at the electrodes, the accumulated charge can now be transferred to the next adjacent electrode. This is done by applying more positive voltage V2 at the adjacent electrode, while returning the voltage of the current electrode back to V1. The potential well underneath the current electrode becomes shallower, and all the trapped charge is transferred to the deeper potential well of the adjacent electrode. This charge transfer from one electrode to the next is called dynamic charge shift register.

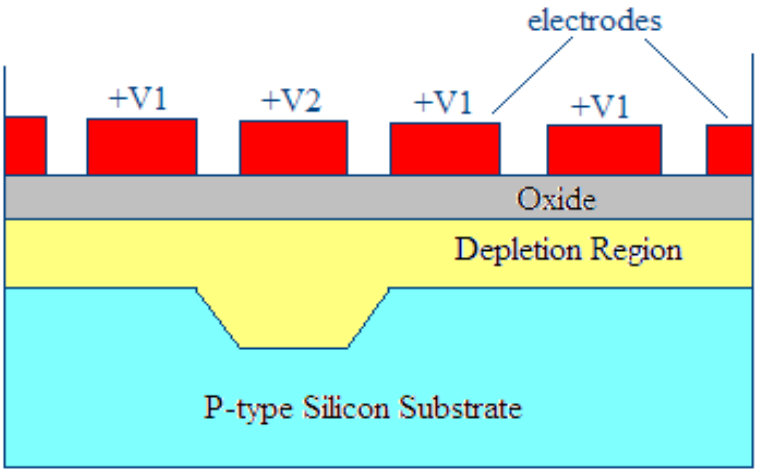

Figure 1.3 Cross section of a simplified CCD sensor

There are several types of CCD image sensors, such as full frame CCD, frame transfer CCD, and interline transfer CCD. The most commonly used CCD imager nowadays utilizes the interline transfer method [5]. Figure 1.4 shows the readout architecture of the interline transfer CCD image sensor. It consists of an array of photo-detectors and vertical and horizontal CCDs for readout. During exposure, the charge is integrated in each photo-detector, and it is simultaneously transferred from all of the pixels to vertical CCDs at the end of the exposure. The charge is then sequentially transferred out of the pixel array through the vertical and horizontal CCDs by charge transfer mechanism, and converted into voltage by a single on-chip output amplifier, and then serially read out of the chip.

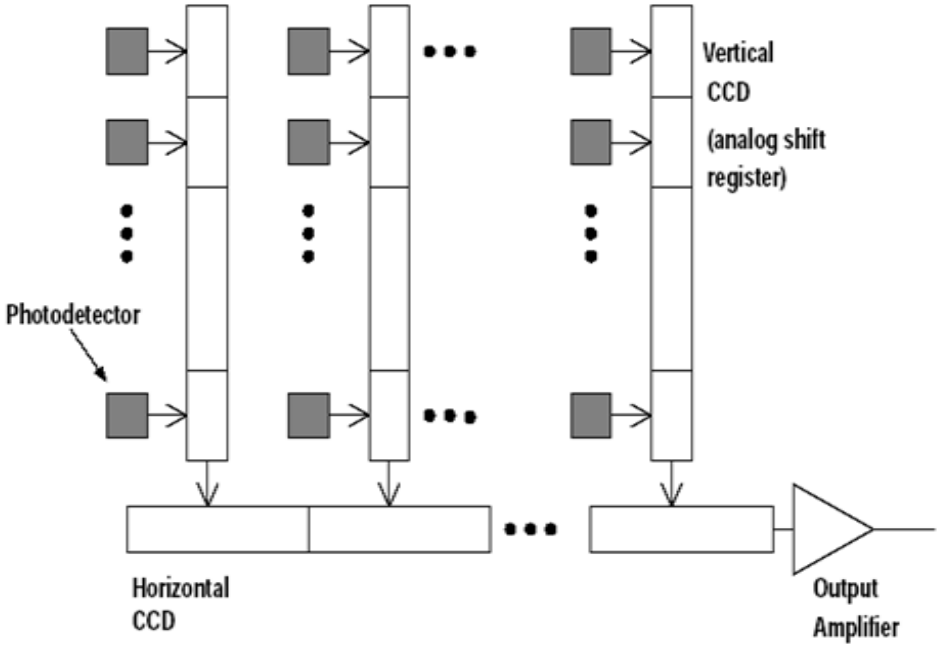

Figure 1.4 Interline transfer CCD image sensor architecture

The charge transfer must occur at high enough rates to avoid charge loss due to leakage, but slow enough to ensure high charge transfer efficiency. Therefore, the CCD image sensor readout speed is limited mainly by the array size and the charge transfer efficiency requirement. This type of readout allows CCDs to have low noise and high uniformity; however, it limits the readout speed and consumes a lot of power [3].

The previously described charge transfer principle leads to some advantages and disadvantages of using CCD image sensors.

Advantages:

- CCD cameras can be up to 100 times more sensitive than film, leading to a much greater dynamic range. They can readily capture both faint and bright details in a single exposure.
- CCD has higher image quality than other solid-state imagers.
- CCD has very low noise, low dark current noise and low fixed pattern noise (FPN).

Disadvantages:

- CCD technology is unable to integrate other analog or digital circuits on chip, such as clock generation, control circuits, and A/D converter circuit.
- CCD cameras are expensive due to specialized fabrication technology.
- CCD consumes high power.
- Random access of pixels is not possible.

- CCD cameras have limited frame rate determined by the charge transfer efficiency.

1.1.2 Brief Overview of CMOS Image Sensors

By the late 1990s, CMOS image sensors had begun to replace CCD image sensors in consumer end imaging applications. One contributing factor to this success was that the CMOS technology had became the dominant technology for VLSI design due to its favorable power-speed tradeoff, high level of integration possibility, and relatively inexpensive fabrication. In addition, the CMOS technology has allowed implementations of a variety of on-chip mixed signal designs, so that both analog preprocessing, such as filters, amplifiers, and analog to digital converters, and digital post processing can be combined on a single chip [1].

The CMOS image sensors are fabricated using standard CMOS processes with no or minor modifications to the process. Figure 1.5 shows the overall architecture of a CMOS image sensor. A CMOS image sensor consists of an array of pixels. Each pixel in the array is addressed through a horizontal word line and the voltage signal is read out through a vertical bit line. The readout is performed one row at a time by sampling the voltage signals onto the column storage capacitors and then reading out the stored values using the column decoders and multiplexers. This readout mechanism allows a random access to the pixel array through row and column addressing and is similar to a memory structure. The column amplifiers provide the

bias current for the pixel array and perform functions such as sample and hold, correlated double sampling, and variable gain control.

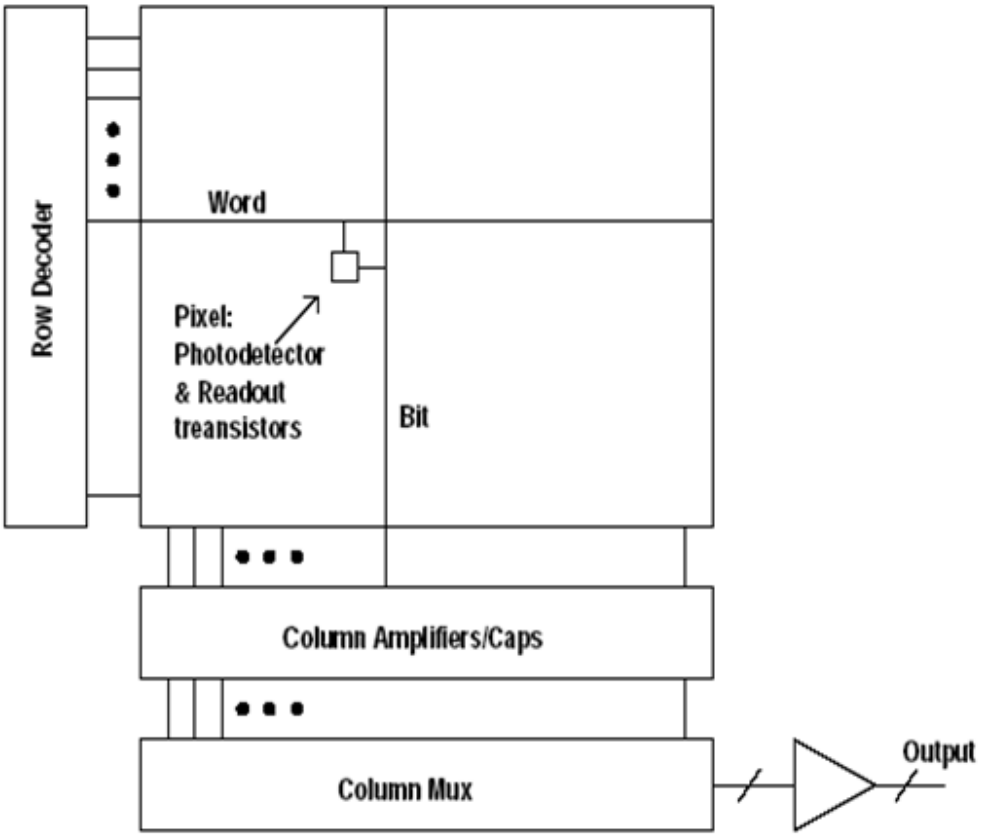

Figure 1.5 CMOS image sensor readout architecture

Since the readout of the CMOS image sensor is not limited by the charge transfer mechanism, the readout speed of the CMOS imager can be much greater than the speed of the interline transfer CCD image sensors with very low power consumed. However, the overall readout noise of the CMOS image sensors is usually higher than the CCD image sensors [2].

The described operating principles of the CMOS image sensors have led to some advantages and disadvantages over the CCD imagers, as listed below.

Advantages:

- Lower power consumption
- Inexpensive fabrication
- On-chip integration of digital signal processing modules
- Random access to individual pixels within the imager array
- Faster readout speed

Disadvantages:

- Medium sensitivity and image quality due to lack of design optimization
- Lower fill factor
- Higher noise
- Lower dynamic range

The basic implementation of any CMOS image sensor consists of a photo-detector, readout electronics, and signal processing circuitry. The design and optimization of the readout circuitry is an important aspect of the overall imager design and has to be carried out with great care to obtain the desired performance, such as power, pixel size, dynamic range, and linearity.

1.2 Motivation

As multi-megapixel image sensors are developed in more aggressive CMOS technologies, the size of the in-pixel source-follower transistor of the APS design is reduced, which in turn diminishes its current driving capability [6]. At the same time, the substantial parasitic capacitances of the long readout lines do not scale down as quickly, so that the small size in-pixel source-follower transistor slows down the voltage transients on the readout lines, increases the settling time, and limits the achievable frame rate of the imager. The limited speed problem becomes more prominent as the pixel count of the image sensor increases; especially as more pixels must be read while maintaining the same number of frames per second; therefore each pixel must be read faster.

The limitation of settling time also reduces the noise attenuation performance of the CDS circuit, since the two consecutive samples taken by the CDS circuit are not sufficiently close together in time to efficiently reduce 1/f noise (i.e., the sampling speed becomes lower than the 1/f noise corner frequency, which results in 1/f noise power leaking into the signal band [7]). It has been shown that the 1/f noise power that "leaks" through in the CDS circuit is becoming one of the major sources of readout noise in modern CMOS imagers [8].

In this dissertation, two new CMOS image sensor readout methods are developed. The Current Sensing Active Pixel (CSAP) sensor is proposed to increase the readout

speed of the pixel output by applying a high gain amplifier in the negative feedback loop of the pixel unit. Therefore, the current driving capability of the sensor is increased and the settling time between the two CDS samples is decreased, which significantly reduces the 1/f noise contributed by the in-pixel source follower transistor. In addition, an improved active reset utilizing the current sensing method is presented. A sensor prototype using the current sensing readout architecture was designed and manufactured using the TSMC 0.35 μm CMOS process.

Another design proposed to eliminate the need for an external CDS circuit is the Reconfigurable Active Pixel Sensor (RAPS). This design employs a reconfigurable differential-input readout amplifier that may be used in both the reset and the readout phases of the image sensor operation. As a result, the DC offset is removed, the flicker noise is differentiated, and the reset noise is greatly reduced by employing the amplifier in an active reset configuration. Gain related fixed pattern noise (FPN) is also reduced by the higher open-loop gain of the differential amplifier.

1.3 Dissertation Organization

In this thesis, a brief overview of different imaging systems is presented, followed by the description of two new CMOS image sensor readout techniques.

Chapter 2 introduces the design theory and concept, which include the basic knowledge of the MOS transistor and its different sources of noise. The fundamental

operating principles of photodiodes and related noise sources are described. Last, the pixel design techniques are also described.

Chapter 3 presents a detailed description of the CSAP readout circuit and its different modes of operation. The proposed design is analyzed and simulated in the Cadence design tool. The performance comparison in terms of speed and settling time between the proposed CSAP design and the standard CMOS APS design is also presented.

Chapter 4 presents a detailed description of the RAPS readout circuit and its different modes of operation. The proposed design is analyzed and simulated in the Cadence design tool. The performance comparison among the proposed RAPS design, the standard CMOS APS design, and the CMOS Active Column Sensor (ACS) design is also presented.

Chapter 5 provides test results of the proposed CSAP design. The CSAP sensor contains a pixel array of 3 rows by 128 columns, was fabricated using the 1-poly 4-metal CMOS 0.35 μm process through MOSIS and the testing was performed to validate the design. It has been shown that the use of negative feedback with the additional row amplifier increases the imager's current driving capabilities and thereby allows faster speed during the readout phase of the image sensor operation. The CSAP circuit fabricated in 0.35-μm CMOS technology with a standard photodiode demonstrates readout root-mean-square (rms) noise levels of 95 μV or 50 electrons at room illumination levels. A single pixel occupies 15*15 μm^2 and

measured conversion gain is 1.88 μV per electron. The power dissipation of the entire CSAP sensor (including the supporting circuitry) is 132 μW. The test results of the proposed RAPS design will be provided after the prototype is successfully fabricated and experimentally verified.

Finally, chapter 6 concludes the thesis and gives suggestions for future research directions.

Chapter 2

Fundamentals of CMOS Image Sensor

2.1 Photodiode Operations

When a semiconductor is illuminated, some of the photons are absorbed if the photon energy is greater than the semiconductor's bandgap energy Eg. The absorbed photons stimulate the electrons to move from the valence energy band to the conduction band. As a result, electron-hole pairs are created. The number of photons absorbed is proportional to the photon flux through the semiconductor, and it's determined by the absorption coefficient α, which differs with different semiconductor materials and wavelength of the incident photons. As the wavelength increases, α is a decreasing function. The irradiance of light (photon flux) traveling though the semiconductor material can be expressed as [9],

$$I_X = I_0 \mathrm{e}^{-\alpha\chi} \tag{2.1}$$

where I_0 is the photo flux at the surface of the material and χ is the distance from the surface

A photo-detector converts the absorbed photon flux, first into electron-hole pairs and then into photocurrent. There are several types of photo-detectors. The most commonly used photo-detector is the photodiode, which is a reversed biased p-n junction. Since we employed photodiodes in the CSAP pixel design, a detailed description is provided next.

In a standard CMOS process, there are three types of photodiodes available. They can be built either between an n-type diffusion and a p-type substrate or an n-type well and a p-type substrate as shown in Figure 2.1, they can also be built between p-type diffusion and an n-type well [9]. The area between $0 < x < x_n$ is the n-type cathode (well or diffusion) and $x_j < x < x_p$ is the p-type anode (substrate). The area enclosed $x_n < x < x_j$ is the depletion region of the pn junction often referred to as the space charged region since it lacks free charges as opposed to quasi neutral regions..

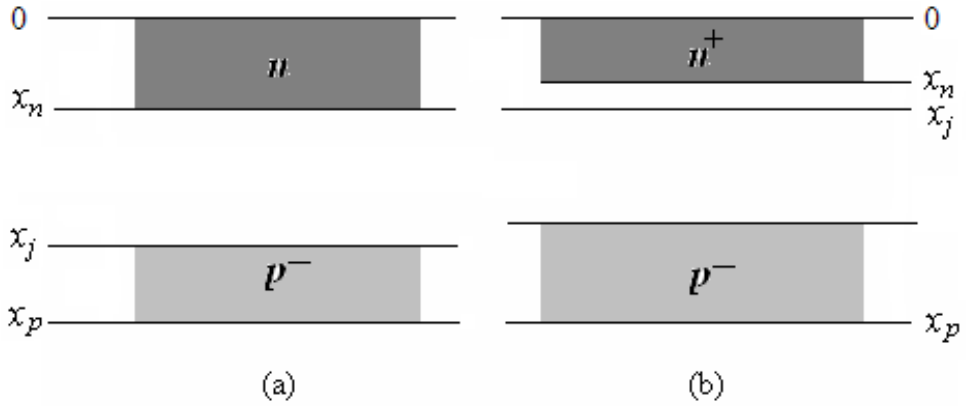

Figure 2.1 PN junctions (a) n-Diff and p-Substrate (b) n-Well and p-Substrate

Figure 2.2 shows the energy band diagram of the photodiode and the movement of generated electron-hole pairs under the reverse biased p-n junction [9].

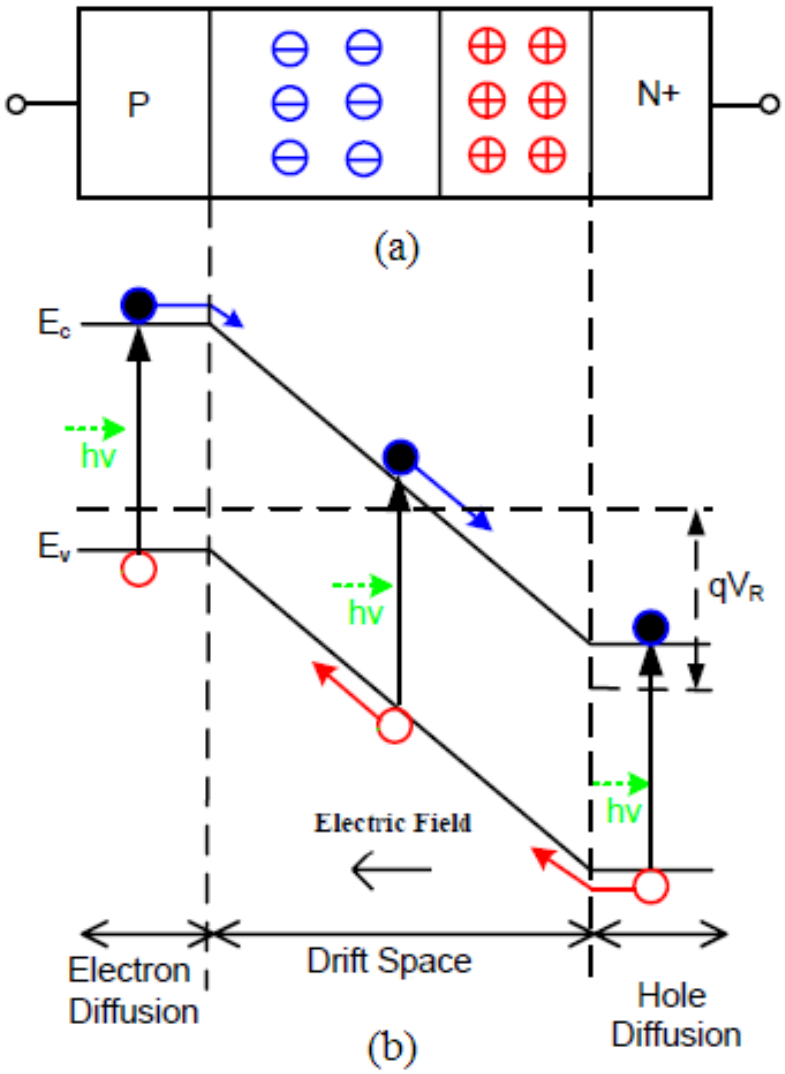

Figure 2.2(a) Cross-section view and (b) Energy band diagram of photodiode

Carriers that are photo-generated in the quasi-neutral regions (bulk n or p regions) can either recombine in the bulk region or diffuse through the bulk region to the

depletion region, and then add to the photocurrent. In a standard CMOS process carriers photo-generated in the bulk region typically do not recombine before they can enter the depletion region. This implies that the light sensitive portion of the photodiode can be larger than the depletion region of the p-n junction and that the total photocurrent generated in the photodiode comes from both the depletion region and the quasi-neutral regions. The current generated in the depletion region is carried by both types of charge carriers (electrons and holes) that are separated after the generation by the strong electric field. On the other hand, the currents generated in the quasi-neutral regions are due to holes generated in the n-type quasi-neutral region and electrons generated in the p-type quasi-neutral region. Only the carries that successfully diffuse to the depletion region are collected after the random recombination in these quasi-neutral regions. The number of electron-hole pairs generated for each incident photon is measured as quantum efficiency η [2].

$$\eta = \frac{number\ of\ collected\ electron\ hole\ pairs}{number\ of\ incident\ photon\ at\ wavelength\ \nu} \tag{2.2}$$

In order for a reverse biased p-n junction to maintain electrical equilibrium, the diffusion of carriers across the junction and the reverse bias voltage must be balanced by a strong electric field in the depleted quasi-neutral region. If photo-generation occurs within the depleted quasi-neutral region, then the built-in electric field will quickly separate and collect the electron-hole pairs. This will form a photo-leakage current through the diode that is proportional to the incident light intensity and can be expressed as [9].

$$I_{photo} = \frac{\eta q P_s}{h\nu} \tag{2.3}$$

where η is the quantum efficiency of the photodiode as is defined in equation 2.2, *Ps* is the incident optical power, *h* is the Planck's constant, and υ is the wavelength of the light.

The steady-state current density of an N+/P-substrate photodiode is described in [9].

$$J_{total} = J_{drift} + J_{diffusion} = qI_0\left[1 - \frac{e^{-\alpha W}}{1+\alpha L_n}\right] + \frac{qD_n n_{p0}}{L_n} \tag{2.4}$$

where W is the depletion width, $L_n = \sqrt{D_n \tau_n}$ is the diffusion length, D_n is the diffusion constant for electrons, τ_n is the minority carrier lifetime and n_{p0} is the electron density at equilibrium.

Since the photocurrent is very small, normally on the order of tens to hundreds of fA [10], it is typically integrated into a charge, and the accumulated charge (or converted voltage) is then read out. This type of operation is called direct integration, the most commonly used mode of operation in an image sensor, where the photocurrent and the dark current are directly integrated over the diode capacitance.

The direct integration operation is shown in Figure 2.3, where the capacitance C_D is the junction capacitance of the photodiode. The photodiode is reset to the reverse biased voltage V_D at the start of the image capture integration time. During the integration, the photocurrent discharges the photodiode capacitance C_D for an integration time t_{int}, causing the photodiode voltage to drop at a rate that is

proportional to the photocurrent. At the end of the integration time, the accumulated (negative) charge $Q(t_{int})$ or voltage $Vo(t_{int})$ is sampled and read out by the readout circuitry. The pixel is then reset again, and the process repeats for the next frame. Assuming that the photo current, dark current, and C_D do not change with the reverse biased voltage, the charge and the voltage relations are obtained as shown in equation 2.5 and 2.6 [10].

$$Q(t_{int}) = (i_{ph} + i_{dc})t_{int} \tag{2.5}$$

$$V_O(t_{int}) = V_D - \frac{(i_{ph}+i_{dc})t_{int}}{C_D} \tag{2.6}$$

The maximum non-saturating photocurrent is thus given by the following equation, where Q_{max} is called the well capacity.

$$i_{ph}^{max} = \frac{Q_{max}}{t_{int}} - i_{dc} \tag{2.7}$$

To avoid blooming — the overflowing of charges from one photodiode in a pixel to the photodiode of a neighboring pixel in an image sensor — the photodiode must remain reversed biased during the light integration so that $Vo(t_{int}) > 0$ V. It is very often that the output voltage swing is lower than V_D to maintain good linear response, which causes the well capacity to be lower than $V_D \times C_D$.

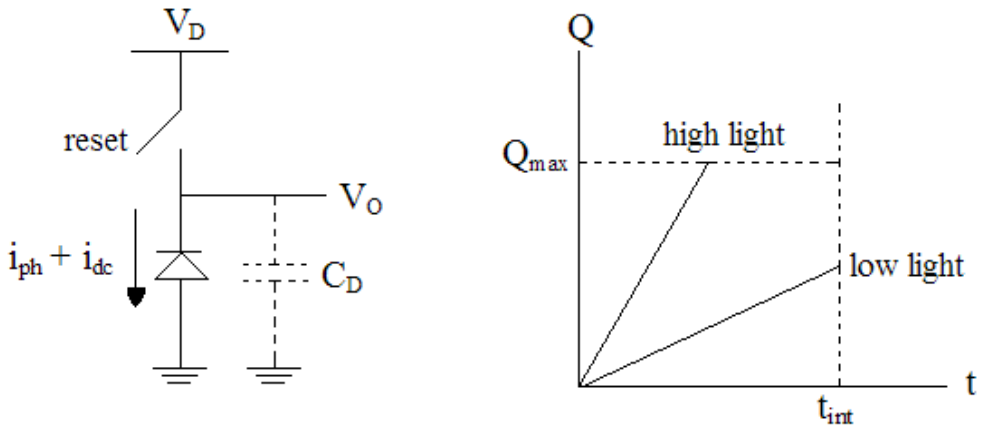

Figure 2.3 Direct integration operation of photodiode

2.2 Types of CMOS Image Sensors

There are two groups of CMOS image sensors that have been successfully implemented in the market today: Passive Pixel Sensors (PPS) and Active Pixel Sensors (APS). An APS contains an active amplifier at the pixel which does not exist in the PPS. We mainly focus on describing the operating principles of the APS design (the most popular architectures in today's market), which utilized a photodiode and a pinned-photodiode as photodetector. The Active Column Sensor (ACS) model is also introduced, because the proposed RAPS design presented in the Chapter 4 is derived from this model. The Digital Pixel Sensor (DPS) is another type of the CMOS image sensor, which also facing design challenges.

2.2.1 CMOS Passive Pixel Sensor

The photodiode PPS image sensor consists of a photodiode and a single pass transistor in each pixel [11] as shown in Figure 2.4. The fill factor, which is the ratio of the photosensitive area to the pixel size, can be very large due to only one transistor in a single pixel. When the pass transistor is activated, the photodiode is connected to a vertical column bus line.

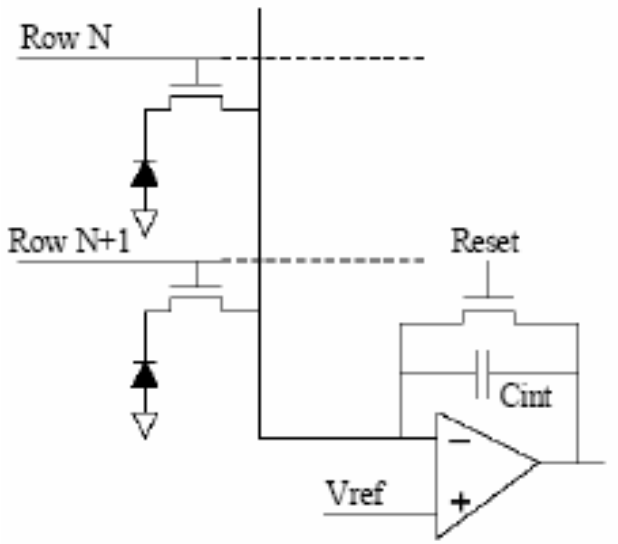

Figure 2.4 CMOS PPS with common readout circuit for each column

The charge amplifier readout circuit is located at the bottom of each column bus line. Prior to each light exposure, each pixel is selected to reset the voltage on the photodiode to the column bus voltage V_{ref}. Following the reset, the pixels are disconnected from the bus line for a period of integration time T_{int}. During this period, the photodiode discharges at a rate approximately proportional to the amount of

incident illumination. When the transistor switch is closed again to reset the photodiode, a current supplied by a charge amplifier flows via the resistance of the column bus due to replenish the charge lost during the light exposure. (i.e., the total charge that flows to reset the pixel is equal to that discharged during the integration period). This charge is integrated on the capacitor C_{int} and converted to a voltage by the charge amplifier. Then the integration process starts again.

The column charge amplifier keeps the voltage on the column bus line constant and reduces KT/C noise. The PPS structure has a major problem due to its large capacitive load. Since the long bus line is directly connected to each pixel during the readout, the RC time constant is very high and the time of transferring a row to the output is long, resulting in a slow overall readout speed. In addition, the readout noise is typically high — on the order of 250 electrons rms compared to less than 10 electrons rms for commercial CCDs [3] — since the signal path is directly connected to the column bus without a buffer. Because of these disadvantages, the PPS does not scale well to larger array sizes or faster pixel readout rates. Furthermore, difference between the individual column-level amplifiers will cause fixed pattern noise (FPN).

2.2.2 Photodiode Active Pixel Sensor

The APS imager design was proposed in [1] and is commonly used in the commercial CMOS image sensor market. The APS design places a buffer into each pixel to drive the readout bus line and improve the image performance. Therefore, the

photo-detector is isolated from the readout line reducing cross talk and charge loss, which is a significant drawback of previously described PPS image sensor design. The basic schematic of the photodiode APS is shown in Figure 2.5. It consists of three-transistor (3T) in each pixel: a reset (RST) transistor Q_1, source-follower (SF) transistor Q_2 and a column select (CS) transistor Q_3. The photodiode is normally a reverse biased p-n junction and is fabricated by n-type diffusion or well in a p-type substrate.

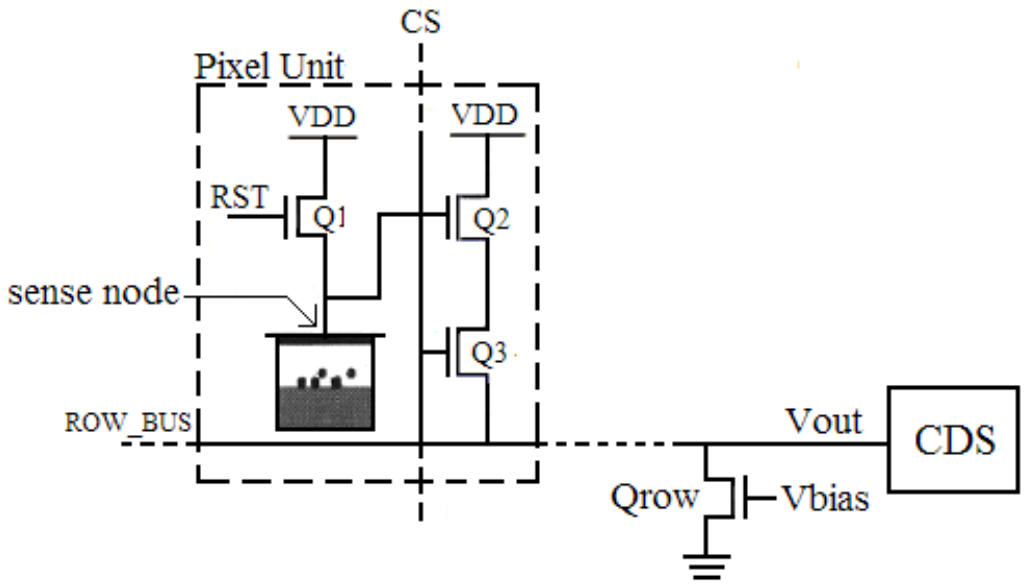

Figure 2.5 Standard three-transistor photodiode APS with CDS unit

The charge-to-voltage conversion occurs at the sense node capacitance, which comprises the photodiode capacitance and all other junction capacitances connected to that node. In this case, these are the source capacitance of the reset transistor Q_1 and the gate capacitance of the source follower transistor Q_2. The large junction

capacitance results in a smaller conversion gain and lower sensitivity. The photodiode is isolated by the readout transistor Q_2, which is connected through the column select switch Q_3 to a common current source Q_{row} outside the pixel area to reduce pixel-to-pixel variations. When the selecting switch Q_3 is asserted, the transistors Q_2 and Q_{row} form a source-follower type amplifier. This in-pixel amplifier provides output buffering to increase the readout speed and SNR. Transistor Q_1 is used to reset the photodiode to an initial voltage level and to control the integration time. It is usually implemented with an NMOS transistor since no additional well is required, thus allowing a higher fill factor. Transistor Q_3 is used to accommodate multiplexing. The APS designs suffer from relatively high dark current and lower fill factor with respect to traditional CCD imagers and PPS designs. The APS designs are commonly implemented with column-level Correlated Double Sampling (CDS) circuits to remove offset and reset noise and column-level ADCs to convert sampled signal to digital. Low speed ADCs are sufficient but consume significant area and power.

In the APS operation, each pixel is read in two phases; reset phase and integration phase [12]. During the reset phase, the photodiode connects to the power supply through the reset transistor Q_1 and the photodiode capacitance is charged to a reset voltage. This reset voltage is sampled and stored into one of the sample-and-hold (S/H) capacitors in the CDS circuit [13]. In the integration phase, the photo-element accumulates photo-generated charge, and the voltage across the photodiode decreases. Switch transistor Q_3 turns on to connect the amplifier transistor Q_2 to the external current source $Q_{row.}$ The output voltage is then sampled and stored into the second

S/H capacitor in the CDS circuit [2]. The CDS circuit is then used to subtract these two stored voltages at two different samples S_1 and S_2 to obtain the final output value as shown in Figure 2.6.

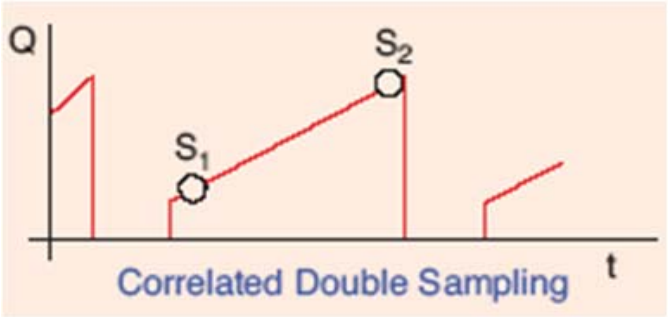

Figure 2.6 Correlated double sampling circuit

The CDS circuit is usually located at the end of each column and its main purpose is to eliminate the DC offset FPN and reset noise. However even though 1/f noise is differentiated, it is poorly attenuated because 1/f noise samples are weakly correlated due to the relatively large time interval between the samples. Another disadvantage of this approach is that it requires a separate capacitive element for each pixel. The capacitive elements could be placed inside the pixel units at the expense of significantly reducing the effective area that might otherwise be used for light gathering. The capacitive elements could also be placed externally to the pixel area but may be prohibitively expensive in terms of silicon area. It has been shown that the CDS circuits may require as much area as the imaging region itself.

Another sampling approach called delta-reset sampling (DRS) has been proposed to reduce capacitance area and to better differentiate the 1/f noise [2]. It is just the reverse sampling procedure of the CDS. The voltage at the end of the integration phase is sampled first, followed by sampling the photo-detector voltage after the reset phase. These two sampling values are then subtracted to obtain the final output voltage as shown in Figure 2.7. This method requires only one capacitive element per column, which consumes much less silicon area than the CDS method. Since the time difference between these two sampled voltages is much smaller than in the CDS approach, 1/f noise samples are highly correlated and can be greatly attenuated. However, this sampling method does not remove the reset noise, and in fact it has been shown that the reset noise power may be increased by a factor of two. The reset noise problem becomes more prominent with technology scaling; as the size of the photo-detector capacitance C_{pd} decreases, the reset noise power kT/C_{pd} increases.

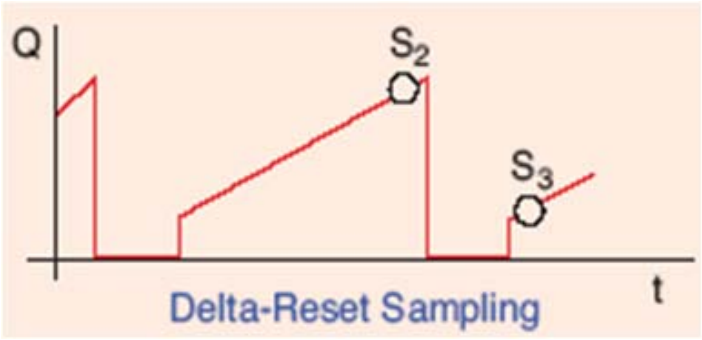

Figure 2.7 Delta-reset sampling circuit

Figure 2.8 shows the comparison of the readout timing signals of the photodiode APS using different sampling approaches, CDS and DRS. In the CDS, the pixel

output signal is sampled first after the reset phase and is stored in one memory after SHR is turned on, and then the signal is sampled after the integration phase and is stored in another memory after SHS is turned on. The difference of these two signals $V_{SIG} - V_{RST}$ represents the integrated signal during this particular time period. In DRS, the pixel output signal is sampled first after the integration phase and is stored in one memory after SHS is turned on, and then the signal is sampled after the reset phase and is stored in another memory after SHR is turned on. The difference of these two signals $V_{RST} - V_{SIG}$ represents the integrated signal during this particular period.

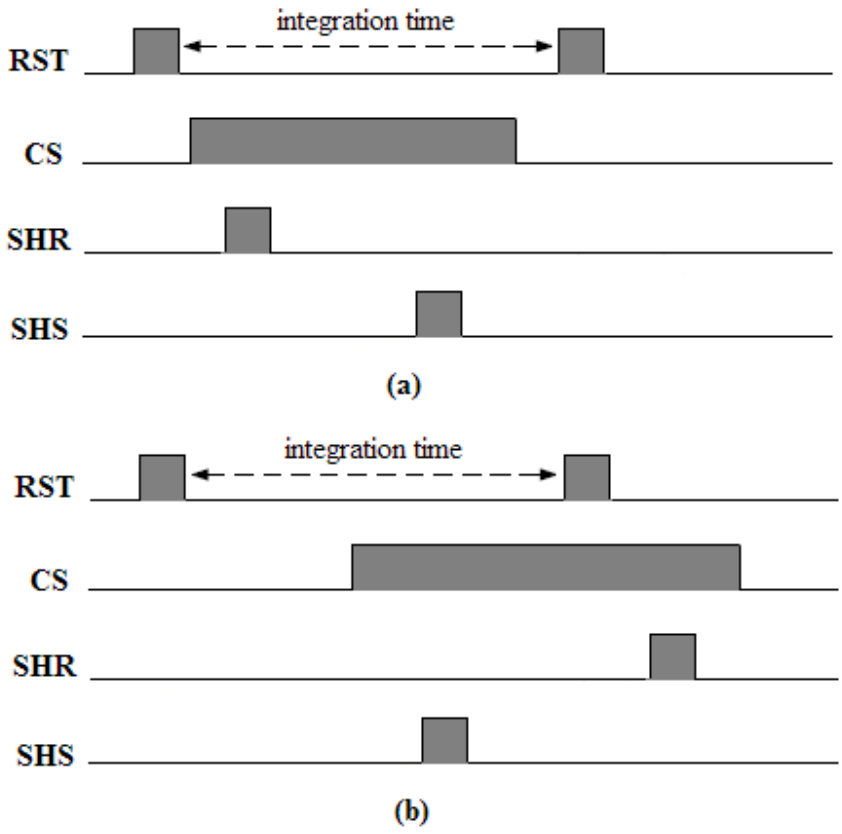

Figure 2.8 Photodiode APS readout timing diagram with (a) CDS and (b) DRS

Another important disadvantage of the photodiode APS image sensor based on the source follower amplifier at each pixel site is the relatively large gain error among the pixels of the imager. The APS design employs the source follower structure that has a voltage closed-loop gain given by equation 2.8,

$$A = \frac{g_m r_{load}}{1+g_m r_{load}} \tag{2.8}$$

where g_m is the transconductance of Q_2 and r_{load} is the load resistance driven by Q_2 during the readout phase. It has been experimentally demonstrated that the closed-loop gain A is somewhat close to 0.8, which means that the open-loop gain $g_m r_{load}$ is equal to 4. This value for the open-loop gain is not large enough to stabilize the closed-loop gain A (i.e., variation of either the transconductance g_m or the equivalent load resistance r_{load} may change the closed loop gain significantly). As a result, the CMOS APS structure suffers from the gain related FPN problem.

2.2.3 Pinned Photodiode Active Pixel Sensor

The pinned photodiode is also commonly used in sensor market nowadays. A pinned photodiode has better photosensitivity than a standard pn junction photodiode, but suffers from incomplete charge transfer reducing the readout speed. The schematic is shown in Figure 2.9. The pixel unit contains a pinned photodiode and 4 transistors: a transfer gate (TX), a reset transistor (RST), a source follower transistor (SF) and a column select transistor (CS). The transfer gate is used to transfer the

collected charge to a floating diffusion (FD) node. The pinned PD is a p^+-n^+-p structure, where the n^+ region is pulled away from the silicon surface in order to reduce the surface defect noise (most likely due to dark current) [14]. As the voltage applied to the n^+ layer is increased, the depletion regions of both p-n junctions grow toward each other. At a certain pinned voltage V_{pin}, the depletion regions meet.

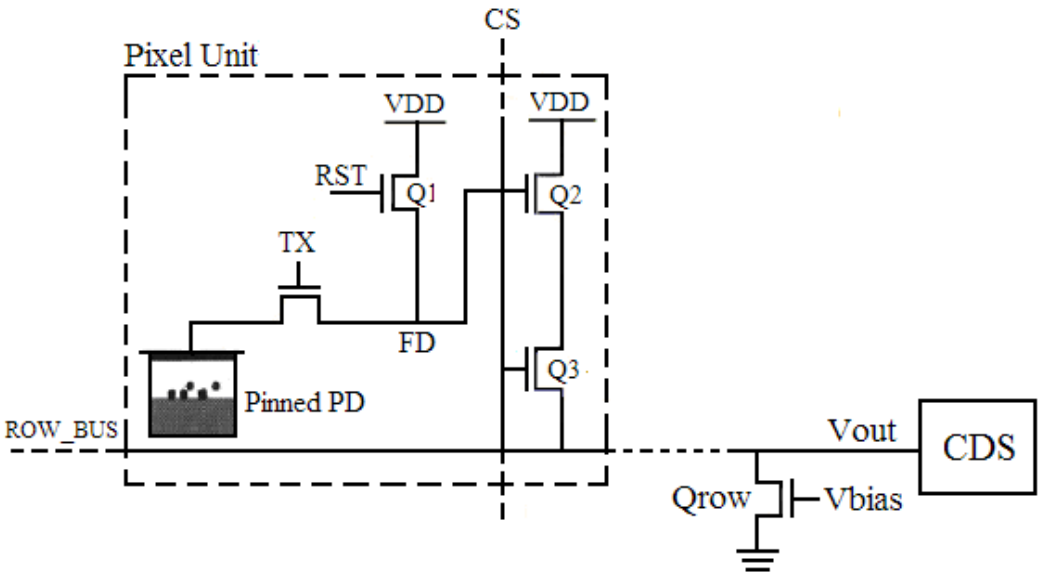

Figure 2.9 Schematic of a pinned photodiode APS (4T APS)

Unlike the photodiode 3T APS structure, the pinned photodiode 4T APS structure uses a transfer gate to separate the photodiode and the floating diffusion node, so the capacitance of the FD node can be optimized. This capacitance needs to be minimized to increase the conversion gain, but it also needs to be large enough to hold all charges transferred from the photodiode. The readout timing signal using the CDS sampling approach is shown in Figure 2.10. A pixel is reset when both the RST

gate and the TX gate are turned on at the same time, so the VDD voltage level is set to both the photodiode and the FD node. Next, the RST gate and the TX gate are turned off and the integration phase is started. The photo-generated electrons are stored in the n+ region of the pinned photodiode thus lowering the potential across the photodiode. During the readout phase, the RST gate is turned on and off again to reset the FD node. Immediately after that, the FD voltage is sampled and stored in one memory after SHR is turned on. Next, the TX gate is turn on and off, which allows charge stored on the photodiode to transfer to the FD node. Then the FD voltage is sampled and stored again in another memory after SHS is turned on. The difference between these two signals $V_{SIG} - V_{RST}$ represents the integrated signal during this particular integration period.

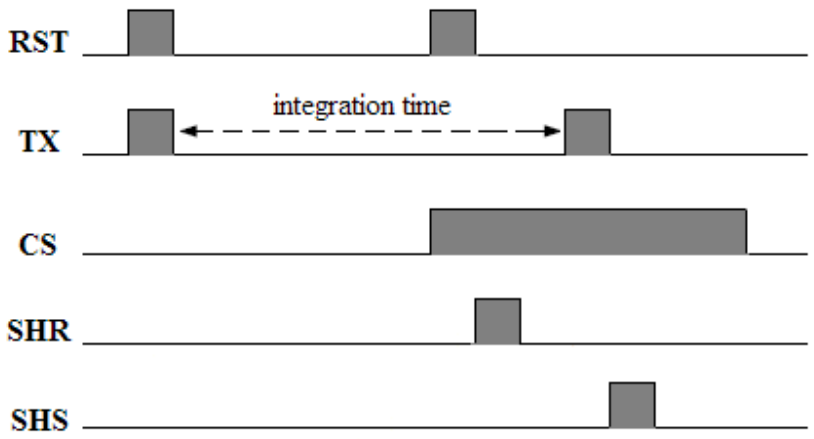

Figure 2.10 Readout timing diagram of a pinned photodiode APS Using CDS

The use of the pinned photodiode APS reduces dark current and surface recombination. It also helps to decrease the read noise in the image and reduce image lag [14].

2.2.4 CMOS Active Column Sensor

In order to improve the gain related FPN problem arising in the APS design, an Active Column Sensor (ACS) design has been proposed in [15]. The ACS readout architecture is depicted in Figure 2.11. The main difference between the APS and the ACS approaches lies in the design of the amplifier. The APS employs a source-follower amplifier design, while the ACS employs a differential-input amplifier in a unity gain buffer topology.

The pixel unit contains three transistors; a reset transistor Q_1, a column selector transistor Q_2 and a source follower transistor Q_3. Q_1 connects the photo-detector to the reset voltage value during the reset operation, Q_2 serves as a switch to assert connection of Q_3 to the common amplifier circuit shared among the pixels of one row. The amplifier circuit is placed outside the pixel area. The in-pixel amplification transistor Q_3 together with the external transistor Q_4 constitutes an input differential pair of a unity gain amplifier (UGA). The current mirror Q_5 and Q_6 provides an active load to the differential pair and the transistor Q_7 provides current biasing to the amplifier. The output of the amplifier is tied to the negative input providing negative feedback, thus creating a unity gain buffer circuit topology.

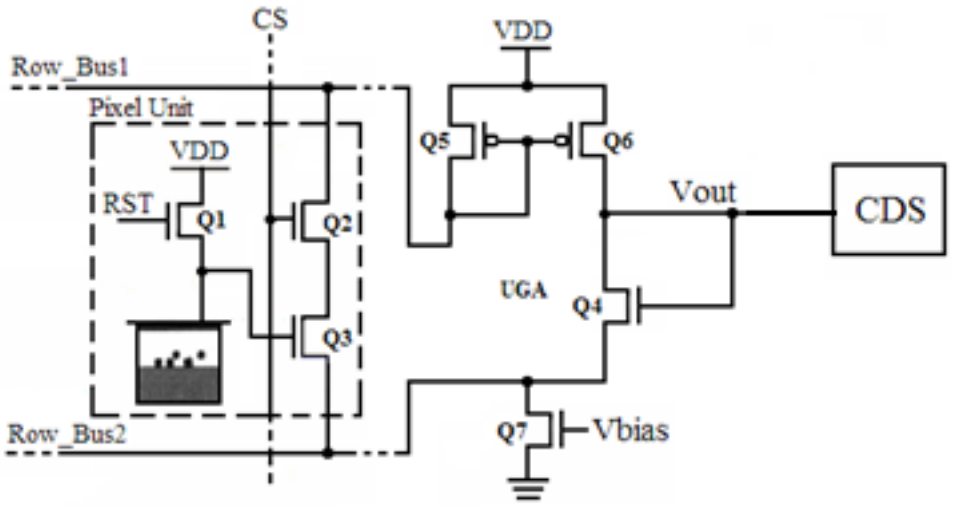

Figure 2.11 ACS architecture with Correlated double sampling unit

The main advantage of the ACS design over the APS design is that the open-loop gain can be increased significantly without increasing the size of the in-pixel transistors. This can be achieved by biasing transistors Q_2 and Q_4 to act as cascade devices and boost open-loop gain in the UGA structure. By increasing the open-loop gain, device parameter variations do not affect the closed-loop gain associated with each pixel as much as in the APS design. A significant reduction of the gain related FPN has been demonstrated in [16] by employing a current-mode ACS with unity gain amplifier feedback system.

However, similar to the APS design, an additional CDS circuit is required for the ACS design to remove the DC offset and the flicker noise. The CDS circuit operation is described below. During the reset phase, both switches Q_1 and Q_2 are turned on. The transistor Q_1 connects the photo-detector to the reset voltage value. The transistor

Q_3 is connected to the amplifier's body through the bus lines. As a result, a UGA is formed that outputs value V_{out_reset}, which ideally is equal to the reset voltage value. This output voltage value is stored in an external capacitance. After the reset phase concludes, the pixel is disconnected from the reset voltage and bus lines, and begins the integration phase. Incident light creates charge that reduces the voltage at the photo-detector terminal. After the integration phase concludes, the pixel is selected by turning on transistor Q_2. A corresponding output voltage value $V_{out\text{-}integration}$ from the unity-gain buffer is then stored in the CDS circuit and subtracted from the initial sample $V_{out\text{-}reset}$. As a result, the DC offset and the reset noise are eliminated and the flicker noise is reduced.

It has been shown that in addition to reduced gain related FPN, the ACS structure exhibits faster settling times than the APS due to higher current capabilities of the differential amplifier structure [15]. The speed of the APS structure is limited by the current driving capabilities of the in-pixel source-follower transistor, which is usually chosen to be a minimum size transistor due to high fill factor requirements. Therefore, the small in-pixel transistor of the APS limits the speed of the positive voltage swings on the bus lines. Unlike the APS design, the active load transistor Q_5 of the ACS design — provides current for the positive voltage swings on the Row_Bus1 line — does not have to be a minimum size transistor because it is external to the pixel area, thereby it allows faster settling times and increased readout speed. Hence, the speed of the ACS design may be improved by increasing the size of the active load transistor. Due to the higher current driving capabilities of the ACS design, it is

advantageous for larger (multi-megapixel) image sensor applications. However, the overall speed improvement of ACS design is rather modest, because the parasitic capacitance of the Row_Bus2 line is still driven by the small size transistor Q_4 that has to match the in-pixel transistor Q_3. The Row_Bus2 line — heavily loads the transistor Q_4 — slows down the overall response since it has to follow output value changes. Therefore, as the CMOS technology continue to scale, the ACS design is facing the same speed limitation problem as the standard APS design. Same as in the APS design, a row level ADC is usually utilized to convert pixel signals to digital values.

2.2.5 CMOS Digital Pixel Sensor

Unlike designs of the PPS, the 3T and the 4T APS, and the ACS, where the Analog to Digital Conversion (ADC) is performed at the chip level or the column level; the DPS design integrates ADC into each pixel [17] as shown in Figure 2.12.

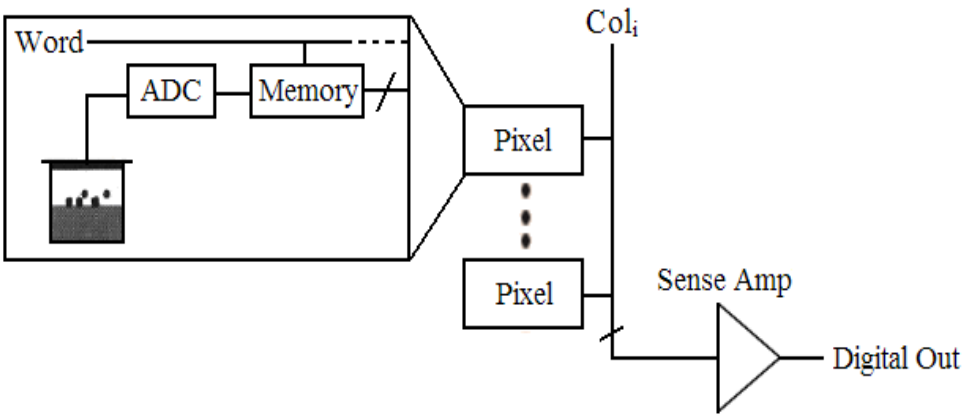

Figure 2.12 DPS architecture with ADC in each pixel

A very low speed and a low power ADC is good enough to provide required performance at the pixel level. This highly paralleled pixel level A/D conversion approach and the digital readout provides very high readout speed, low cross talk and power reduction. The DPS exhibits better scaling with the CMOS technology due to its reduced performance demands on the analog circuitry, which helps to eliminate the column FPN and the column readout noise. The main drawback is relatively large pixel size due to the increased number of transistors per pixel, resulting in lower fill factor and lower light sensitivity.

2.3 The MOS Transistor

The MOS transistor theory and its device models used for small signal analysis are described, followed by the noise analysis. Different types of noises in a CMOS image sensor will be discussed in the next section.

The equations [18] used for hand calculations are presented in equations 2.9-2.11. K is the transconductance parameter, W and L are the channel width and length respectively, V_T is the threshold voltage, and λ is the channel-length modulation parameter. λ is often taken to be zero since it is rather small, which leads to a simplification of the equation in the saturation region shown in equation 2.12 [18].

$$I_D = 0 \qquad V_{GS} < V_T \qquad (2.9)$$

$$I_D = K\frac{W}{L}((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}) \qquad V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \qquad (2.10)$$

$$I_D = \frac{K}{2}\frac{W}{L}((V_{GS} - V_T)^2(1 + \lambda V_{DS})) \qquad V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \qquad (2.11)$$

The threshold voltage V_T depends on the source-to-bulk voltage V_{SB}. Equation 2.13 [18] is often used to calculate V_T when V_{SB} is not zero. V_{T0} is the threshold voltage at zero V_{SB}, Φ_F is the Fermi potential and γ is the substrate bias coefficient.

$$I_D = \frac{K}{2}\frac{W}{L}(V_{GS} - V_T)^2 \qquad (2.12)$$

$$V_T = V_{TO} + \gamma(\sqrt{|2\Phi_F + V_{SB}| - |2\Phi_F|}\,) \qquad (2.13)$$

The equations presented here are valid for NMOS transistors, but they can also be used for PMOS transistors by taking the absolute value of the parameters in the formulas. However, these equations are not very accurate in the short-channel region (or rather high-field region). When the electric field E in silicon reaches 10^5-10^6 V/m, the electron velocity starts to saturate, which leads to many effects that make the equations presented less useful. There are also other effects due to the small dimensions that further divert the calculated values from those actually measured. These equations are used in hand calculations so that the result obtained from them could be used as a guide in the design process. Therefore, it is necessary to validate the function of a circuit in the Cadence simulation environment for modern processes.

2.3.1 Small Signal Model

A small signal model is a linearization of the equations at a quiescent point of the device. This implies that the MOS transistor must have different models, depending on which region of operation it is currently working within [19]. The models shown in Figure 2.13 are often good enough and valid both for NMOS and PMOS transistors. It is possible to add more to these models, such as the resistance of the substrate and other parameters. However, it is not necessary to include additional parameters into the model, since the model accuracy is usually limited by the short-channel effects. The parameters g_m, g_s, and r_{ds} used in these models are defined by equations 2.14 - 2.16 [19].

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.14}$$

$$g_s = \frac{\partial I_D}{\partial V_{SB}} \tag{2.15}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{r_{ds}} \tag{2.16}$$

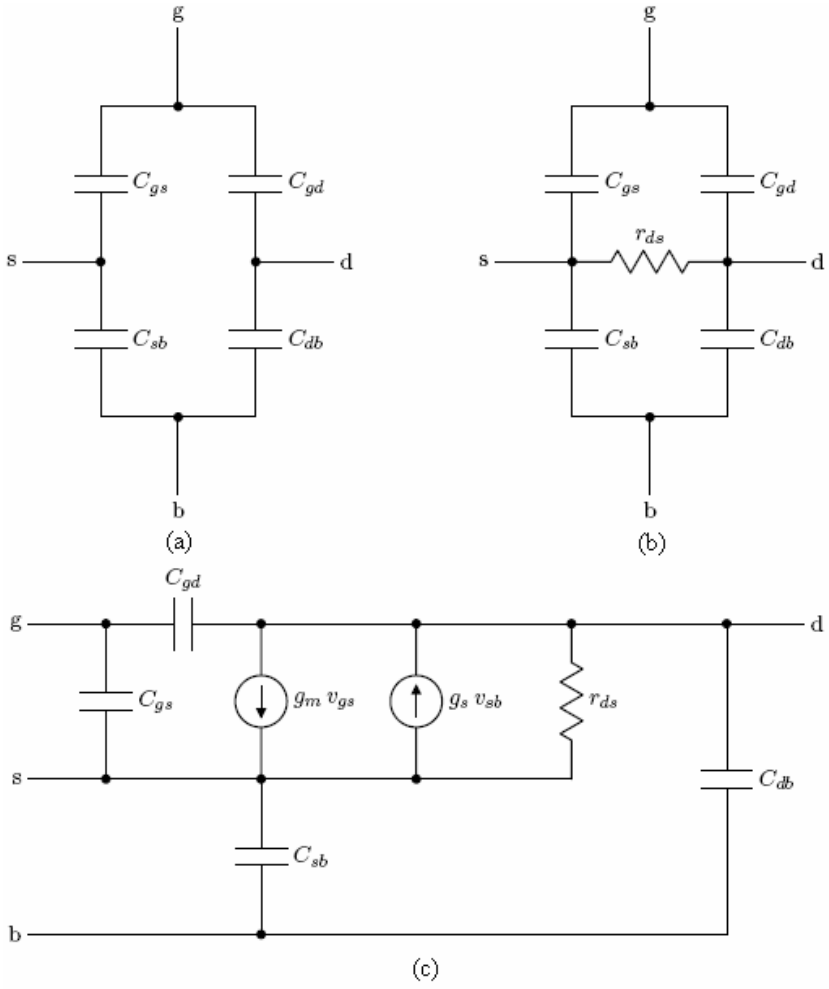

Figure 2.13 Small signal models of MOS transistor (a) Cutoff (b) Triode (c) Saturation

2.3.2 Noise Fundamentals

The noise signals are modeled as weakly stationary processes; for example, the mathematical expectation $\overline{x(t)}$ of a stationary process $x(t)$ is a constant. This condition also establishes that the Auto Correlation Function (ACF) of $x(t)$ only depends on the time difference τ, and is given by equation 2.17 [20].

$$R_x(t+\tau, t) = R_x(\tau) = \overline{x(t+\tau)x(t)} \tag{2.17}$$

Since the Power Spectral Density (PSD) is an even function, only positive frequencies need to be taken into account if the PSD is doubled and this doubled PSD is referred to as single sided PSD. The PSD $S_x(f)$ is given by the Fourier transform of the ACF. The total average noise power is then given by equation 2.18 [20].

$$\overline{x^2} = R_X(0) = \int_{-\infty}^{\infty} S_x(f)df \tag{2.18}$$

If *y*(t) denotes the output when *x*(t) is filtered by a linear filter with the transfer function *H*(f), then equations 2.19 and 2.20 hold true for R_Y and S_Y. When several uncorrelated noise sources are present, the total average noise power can be obtained by summing the contribution from the different noise sources given by equation 2.21 [20].

$$R_Y(t) = \int_{-\infty}^{\infty} \int h(\tau_1)h(\tau_2)R_X(\tau - \tau_1 + \tau_2)d\,\tau_1\tau_2 \tag{2.19}$$

$$S_Y(f) = |H(f)|^2 S_X(f) \tag{2.20}$$

$$\overline{x_{tot}^2} = \overline{x_1^2} + \overline{x_2^2} + \ldots + \overline{x_n^2} \tag{2.21}$$

2.4 Noise analysis of CMOS image sensors

Noise sources in an image sensor can be grouped into two different categories: those that change with time are called “temporal noise” and those that are constant with time but change across the array are called “fixed pattern noise” [2].

Temporal noise is a time dependent noise of an image and is also called random noise. It is the most important non-ideal behavior in an image sensor. It is independent from pixel to pixel and varies from frame to frame. It includes photon shot noise, dark current shot noise, pixel reset noise, quantization noise, and readout related thermal noise and flicker noise [2]. All these noise sources can be treated as uncorrelated sources, and superposition can be used when the total random noise is calculated. The variance of the total random noise voltage can be written as:

$$\overline{v_{pixel}^2} = \overline{v_{shot-photon}^2} + \overline{v_{shot-dark}^2} + \overline{v_{reset}^2} + \overline{v_{thermal}^2} + \overline{v_{1/f}^2} + \overline{v_{quantization}^2} \quad (2.22)$$

The noise can be calculated as the number of electrons n_{noise} or the voltage v_{noise} referenced to the sensing node. The conversion between the two units is called conversion gain (CG) and is represented in the equation 2.23.

$$\overline{v_{noise}^2} = CG^2 \times \overline{n_{noise}^2} \quad (2.23)$$

2.4.1 Shot Noise

A necessary condition for shot noise to occur in a device is if a DC current I_{DC} flows through the device and this current is subjected to a potential barrier. Shot noise is due to discontinuous pulses of current every time an electron charge jumps across the barrier, and the randomness of the arrival times at the potential barrier makes the shot noise white [21]. So the power spectral density of the shot noise can be calculated as shown in equation 2.24 [21]. In an MOS transistor, it is only the gate leakage current that generates shot noise and it is normally so small that it can be ignored.

$$S_{In,s}(f) = 2qI_{DC} \quad [\text{A}^2/\text{Hz}] \tag{2.24}$$

There are two types of shot noise in CMOS image sensors, photon shot noise and dark current shot noise. When the light is incident on an image sensor, the scene is illuminated with an average flux that arrives at a given area of the sensor. There are some fluctuations around the average value and the fluctuations are visible in images and are called photon shot noise [22]. Photon shot noise is a typical Poisson process; the mean of the noise is equal to the variance of the noise. As the signal grows, the photon shot noise also grows, but more slowly; and the signal-to-noise (SNR) ratio increases with the square root of the number of photons collected. The higher the illumination, the less apparent the photon shot noise; the lower the illumination, the more apparent it is [22].

Dark current is a relatively small leakage current flow within the photodiode under no illumination. The major sources of dark current are interface defects, surface defects and bulk defects [23]. Dark current of the image sensor reduces the signal swing of the output voltage and introduces an unavoidable noise source to the entire system, which is called dark current shot noise. The dark current features of the image sensor limit the overall dynamic range.

2.4.2 Reset Noise

Reset noise is due to the noise injected when the pixels in CMOS image sensors are reset. This noise comes from the reset transistor in a pixel unit, which acts as a MOS switch as shown in Figure 2.14. The MOS switch can be modeled as a resistor in series with a voltage source V_R, which is the thermal noise of a resistor with the single-sided PSD equal to $4KTR_{on}$. So the reset noise voltage and noise charge are given by equation 2.25 [24] and 2.26, respectively.

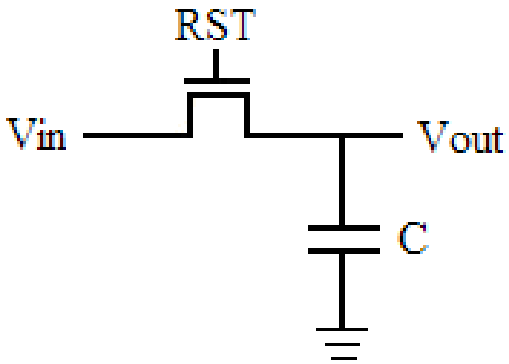

Figure 2.14 Reset transistor acts as a MOS switch

$$\overline{v_{n,reset}^2} = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C)^2} df = \frac{kT}{C} \quad (2.25)$$

$$\overline{n_{n,reset}^2} = C^2 \times \overline{v_{n,reset}^2} = kTC \quad (2.26)$$

where k is the Boltzman constant, T is the temperature, R_{on} is the channel resistance of the reset transistor, and C is the parasitic capacitance of the photodiode. We can see from the equation that the reset noise is only related to temperature and sensing node capacitance of the photodiode.

2.4.3 Thermal Noise

Thermal noise originates from the random motion of agitated electrons giving rise to a current. The thermal noise in resistors, transistors, and so on is white, meaning that its PSD is constant and independent of frequency. In an MOS transistor, the thermal noise $S_{th,in}$ is the drain current noise of the MOSFET and is given by equation 2.27 [21]. In this equation, k is the Boltzmann constant, T is the temperature, γ is a constant that is unity in the triode region and approaches 2/3 in the saturation region for a long-channel MOSFET and g_{ds0} is the drain-source conductance at zero V_{DS}. g_{ds0} can also be written as g_m which is the transconductance of a transistor in the saturation region.

$$S_{th,in}(f) = 4kT\gamma g_{ds0} \quad [A^2/Hz] \quad (2.27)$$

In a CMOS APS, the thermal noises come from the source follower transistor, the column select transistor, and the row bias transistor, which are important and can be calculated accordingly. Since the source follower and row bias transistor are always working in the saturation region, and the column select transistor is always working in the triode region, we can express the thermal noise PSD of the source follower, the column select and the row bias transistor as in equations 2.28, 2.29 and 2.30 respectively.

$$S_{th,SF}(f) = 4kT\frac{2}{3}\frac{1}{g_{m,SF}} \tag{2.28}$$

$$S_{th,CS}(f) = 4kT\frac{1}{g_{d,CS}} \tag{2.29}$$

$$S_{th,bias}(f) = 4kT\frac{2}{3}\frac{1}{g_{m,bias}} \tag{2.30}$$

where $g_{m,SF}$ and $g_{m,bias}$ are the transconductance of the source follower and row bias transistors, $g_{d,CS}$ is the channel conductance of the column select transistor. The thermal noise from the SF transistor is dominant and the thermal noise from the CS transistor is very small and can be neglected [25].

2.4.4 Flicker Noise (1/f) and Random Telegraph Signal (RTS) Noise

Flicker noise is a non-stationary noise that has a PSD in the form of function kf^{-n}, where n is an exponent that is usually close to unity. Flicker noise is more prominent in electrical devices that are sensitive to trapping of charges and other surface

phenomena [21]. Since flicker noise originates from the random trapping and releasing of charges, it is a function of the current flowing through the device. The PSD of the flicker noise is usually modeled as in equation 2.31 for a MOS transistor [21], where K is a device – specific parameter that normally is much larger for NMOS transistors than PMOS transistors. W and L are the gate width and length, respectively and C_{ox} is the gate oxide capacitance per unit width.

$$S_{f,in}(f) = \frac{K}{f}\frac{1}{WLC_{ox}} \qquad [\mathrm{A^2/Hz}] \tag{2.31}$$

Unlike shot noise and thermal noise, which have white-noise spectral properties, the frequency distribution of the flicker noise is non-white. Flicker noise is a low-frequency phenomenon and it is a dominant noise source in MOS transistors at low frequencies. On the other hand, at higher frequencies, the flicker noise is overshadowed by the white noise from other sources, such as thermal noise. Corner frequency is the important parameter of the flicker noise and it represents the transition from flicker noise region to thermal noise region.

A MOS transistor can be modeled by a noiseless transistor in parallel with a noise source as shown in Figure 2.15(a). Its PSD is given by equation 2.32. For low frequencies, the transistor noise model can be simplified to Figure 2.2(b) and characterized by equation 2.33.

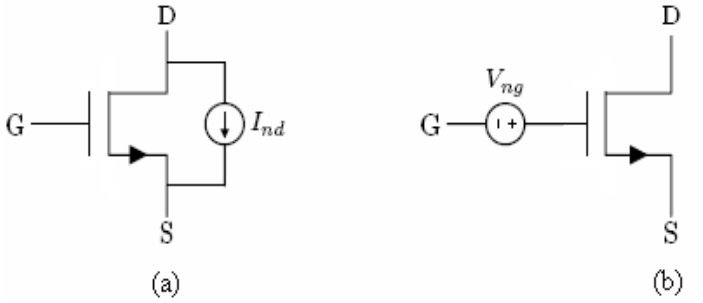

Figure 2.15(a) MOSFET noise model (b) MOSFET noise model for low frequencies

$$S_{Ind,tot}(f) = 4kT\gamma g_m + \frac{K}{f}\frac{g_m^2}{WLC_{ox}} \quad [A^2/Hz] \tag{2.32}$$

$$S_{Ing,tot}(f) = 4kT\gamma \frac{1}{g_m} + \frac{K}{f}\frac{1}{WLC_{ox}} \quad [A^2/Hz] \tag{2.33}$$

If we employ the CDS operation in the CMOS image sensors, we can subtract the two flicker noise samples stored in the CDS circuit taken at time instances separated by the interval τ as shown in equation 2.34. Then the transfer function can be expressed as in equation 2.35. Thus, the PSD of y is equal to the PSD of the flicker noise times the filter function $4sin^2(\omega\tau/2)$ as shown in equation 2.36.

$$y(t) = f(t) - f(t-\tau) \tag{2.34}$$

$$Y(j\omega) = F(j\omega) * H(j\omega) = F(j\omega) * (1 - e^{-j\omega\tau}) \tag{2.35}$$

$$|Y(j\omega)|^2 = F^2(j\omega) * 4sin^2\frac{\omega\tau}{2} \tag{2.36}$$

We can see that the time interval τ between the two noise samples of the CDS circuit determines the value of the flicker noise in a CMOS image sensor. Recent research has demonstrated that the flicker noise is becoming a dominant noise source of the image sensor's temporal noise [26]. As the pixel size and the source follower transistor size shrink, the random telegraph signal (RTS) noise is becoming another major factor that limits the image sensor's performance [27].

RTS consists of sudden step-like transitions between two or more discrete voltage or current levels at random and unpredictable times. The most common cause of the RTS is the random trapping and release of charge carriers at defect sites such as Si/SiO2 interface in the semiconductor device [28]. The noise voltage of the RTS can be modeled as in equation 2.37.

$$S_{RTS,in}(f) = \frac{K}{1+(f/f_c)^2} \tag{2.37}$$

2.4.5 Readout Noise

Readout noise refers to the noise generated at the pixel with noise voltage v_{pixel} plus the noise generated in the array amplifier with noise voltage v_{amp}, so the input referred readout noise voltage can be expressed as in equation 2.38.

$$v_{read}^2 = v_{pixel}^2 + \frac{v_{amp}^2}{A_v^2} \tag{2.38}$$

The readout noise does not include photon shot noise. It limits the image quality in the dark regions of an image and increases with exposure time due to the pixel's dark current shot noise [29].

2.4.6 Fixed Pattern Noise

In an image sensor array, parameters of the transistor and the photodiode, such as width, length, doping concentration, and so on vary slightly throughout the chip, which gives rise to different behaviors from pixel to pixel. This static spread in the readout values shows up as darker or lighter portions in the captured image, when the sensor is subjected to uniform illumination. This pattern of noise is known as Fixed Pattern Noise (FPN) which is constant with time but changes across the array [2]. Mathematically, the FPN is defined as the standard deviation of the voltages from all the pixels of the sensor when the sensor has uniform illumination, and can be estimated by equation 2.39. The summation is carried out over all the K pixels in the array and $\overline{V}$ is the mean value of the readout voltages and is given by equation 2.40.

$$\sigma_V = \sqrt{\frac{1}{K-1}\sum_{i=1}^{K}(V_i - \bar{V})^2} \tag{2.39}$$

$$\bar{V} = \frac{1}{K}\sum_{i=1}^{K} V_i \tag{2.40}$$

2.5 Pixel Theory

An image sensor consists of an array of pixels. To specify and analyze an image sensor, we start by modeling a single pixel. Once the pixel is specified, the sensor is formed by arranging a number of pixels together based on the area and resolution specifications. The sensor formation involves both positioning of the pixels as well as assigning appropriate color filters to form the desired color filter array pattern.

2.5.1 Implementing a Single Pixel

A pixel description includes the specifications of both electrical and geometrical properties. Geometrical properties of a pixel include the photo-detector size and its position within the pixel, the pixel size and its position relative to adjacent pixels. Electrical properties of a pixel include the dark current density and spectral response of the photo-detector, and the conversion gain and voltage swing of the pixel readout circuitry. However, both proposed CSAP and RAPS designs are focused more towards characterizing the performances of their readout circuitry.

We draw the single pixel layout as shown in Figure 2.16. It contains a single poly layer and three metal layers in this layout. The entire pixel size is measured as 15 μm by 15 μm. The photodiode is implemented as an n+ type diffusion in a p-type substrate, where the large red area in the center represents the n+ diffusion with area measuring 95.84 μm^2. There is an RPO layer (silicide block layer) in dark green on

top of the n+ diffusion to ensure a higher light absorption. In the vertical direction, there are three poly segments in the sharp blue representing the three APS transistors (reset transistor, source follower transistor and column select transistor).

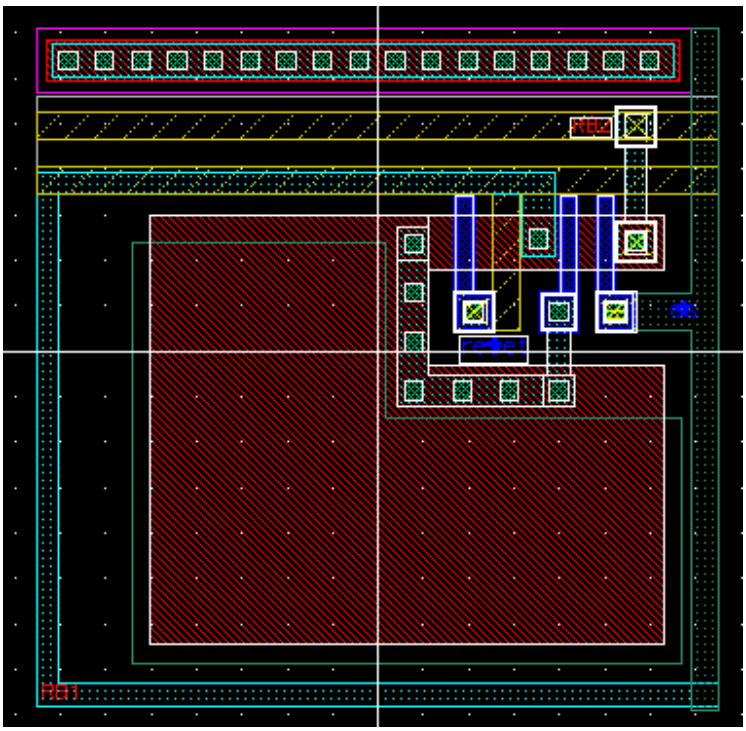

Figure 2.16 CMOS Image Sensor Single Pixel Layout

2.5.2 Fill Factor

Fill Factor (FF) is defined as A_s / A_{tot}, where A_s is the light sensitive area of the pixel and A_{tot} is the total area of the pixel [22]. In figure 2.16, the fill factor is 42.6%. A large FF is desired since the light sensitivity of the sensor increases with an increase in FF. The light sensitive area is calculated by removing the area that is

covered by metals and diffusions, which is not connected to the cathode of the photodiode. Calculations like this become somewhat approximate since:

- Reflections from different layers can cause light to end up in the light sensitive area even though it first hits a metal that is opaque.
- Diffusions do not collect incident light.
- Poly is opaque for short wavelengths, and in silicide processes poly is opaque for longer wavelengths too.

2.5.3 Optimal Pixel Size

In standard CMOS APS design, the transistors at the pixel site play a vital role in arriving at the optimal pixel size, and these transistors also decide the fill factor. As the CMOS technology scales down, the area occupied by the transistors decreases in a pixel unit, providing more freedom to increase the fill factor while maintaining an acceptably small pixel size. A small pixel size is desirable because it results in a higher spatial resolution and better Modulation Transfer Function (MTF) [22]. A large pixel size is desirable because it results in better dynamic range (DR) and SNR. Therefore, the tradeoff for designing a pixel is between high DR and SNR on the one hand, and high spatial resolution and MTF on the other. To date it has not yet become clear how to trade off DR and SNR with spatial resolution and MTF. More importantly, it is not clear how these measures relate to the image quality, which should be the ultimate objective of selecting the optimal pixel size.

Chapter 3

CSAP Design Theory and Concept

3.1 Introduction

As multi-megapixel image sensors are developed in more aggressive CMOS technologies, the size of the in-pixel source follower transistor of the APS design is reduced which in turn diminishes its current driving capability [6]. At the same time, the substantial parasitic capacitances of the long readout lines do not scale down as quickly, and the small size in-pixel source follower transistor limits the readout speed of the imager and slows down the voltage transients on the readout lines. The limited speed problem becomes more prominent as the pixel count of the image sensor increases (i.e., more pixels must be read while maintaining the same number of frames per second, therefore each pixel must be read faster). The shrinking factor of the in-pixel source follower transistor size limits the achievable frame rate of an image sensor.

The limitation of settling time also reduces the noise attenuation performance of the CDS circuit, since the two consecutive samples are not sufficiently close together

in time, so that the sampling speed becomes slower than 1/f noise corner frequency, which results in 1/f noise power leaking into the signal band [7]. As a result, the 1/f noise power is not reduced. It has been shown that the 1/f noise power that "leaks" through in the CDS circuit becomes one of the major sources of readout noise in modern CMOS imagers [8].

We propose a Current Sensing Active Pixel (CSAP) CMOS image sensor design that employs an in-pixel transistor current sensing to decrease the settling time of the pixel readout circuit. The objective of the design is to combine the small pixel size and low power dissipation of the standard APS configuration with faster settling times and correspondingly increased readout speed. By decreasing the settling time, the two consecutive samples in the CDS scheme are closer together in time, which in turn reduces the effective 1/f noise contribution of the source follower transistor. A further objective is to reduce the reset noise by utilizing an in-pixel amplifier in a negative feedback configuration.

3.2 CSAP Architecture

The general CSAP architecture is shown in Figure 3.1, which contains a pixel unit and a shared readout circuit configuration. On the left side is the in-pixel APS structure. The APS unit contains a photo-detector, an NMOS reset transistor Q_1, an NMOS readout transistor Q_2 and an NMOS column select transistor Q_3. On the right

side is the out-of-pixel readout circuit shared by pixels of a row, which contains a current amplifier in the current-sensing configuration, a bias current source and a CDS circuit.

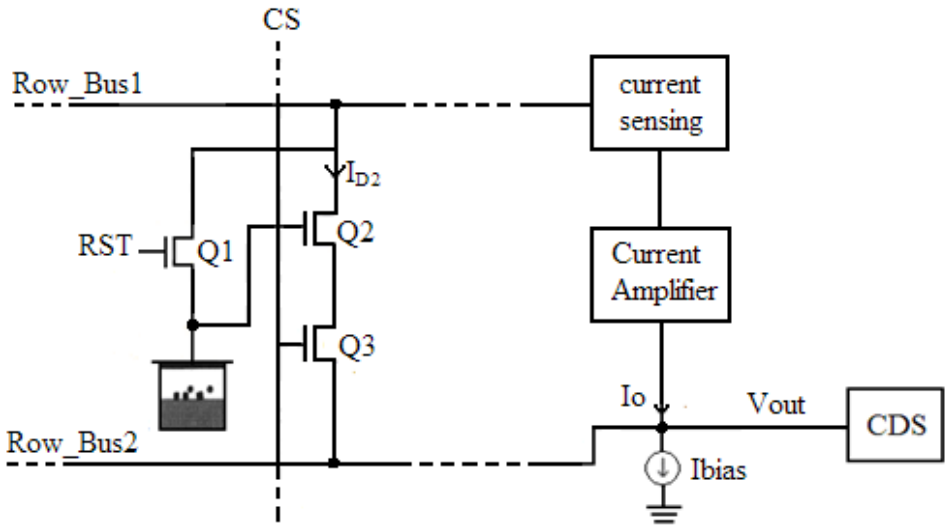

Figure 3.1 Schematic diagram of a general CSAP architecture

The proposed design employs a minimum number of transistors at the pixel level to maintain high fill factor and a readout architecture shared by a row of the pixels, leading to further reduced hardware complexity. The CSAP sensor design increases array readout speed for greater frame rates and decreases readout noise through external CDS circuitry. The CSAP technology may be integrated with existing APS pixel designs to provide substantial performance improvements with minimal design changes.

The current I_{D2} through the in-pixel readout transistor Q_2 is sensed by a circuit external to the pixel and shared among the pixels of a row. This external readout circuit amplifies current I_{D2} and feeds the amplified current I_O back to the pixel in order to charge the read-line (ROW_BUS2) parasitic capacitance. The in-pixel readout transistor Q_2 is in the source-follower configuration during the pixel readout operation, but it is in a common-source amplifier configuration during the pixel reset operation. During both the readout and reset operations, the in-pixel amplifier operates in conjunction with the external circuit that provides current sensing and feedback.

3.3 CSAP Operation Principles

3.3.1 CSAP Pixel Readout Operation

During the pixel readout operation, the in-pixel readout transistor Q_2 is in the source-follower configuration and the CSAP architecture is constructed as shown in Figure 3.2. The pixel is selected by asserting the transistor Q_3, which connects the amplification transistor Q_2 to the out-of-pixel part of the readout circuit. The reset transistor Q_1 is turned off during the readout operation. The drain terminal of the transistor Q_2 is connected through the Row_Bus1 line to the external current sensing circuit. The source terminal of Q_3 is connected through the Row_Bus2 line to the bias

current source I_{bias} and the output of the current amplifier circuit, which forms a negative feedback loop.

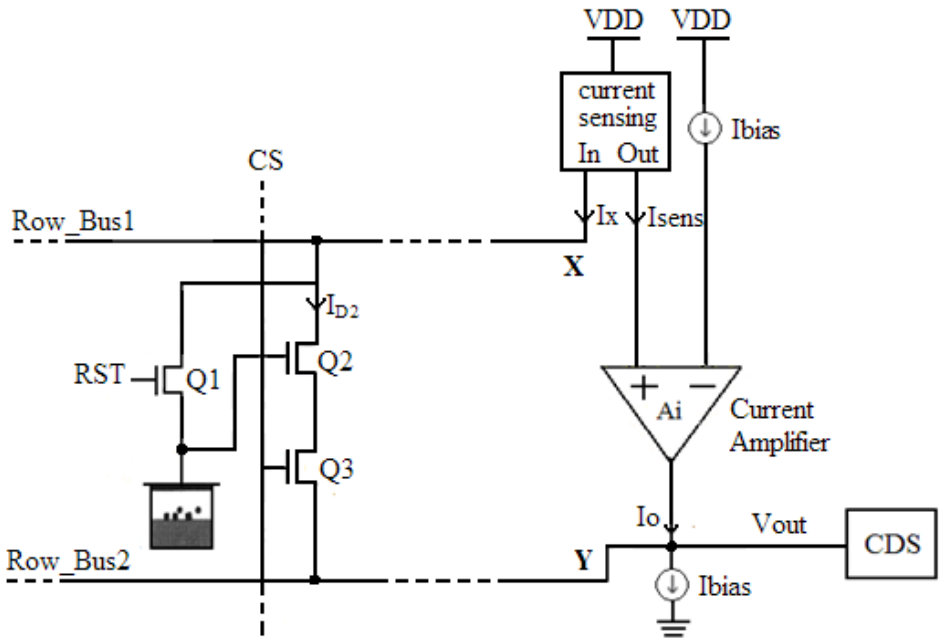

Figure 3.2 Schematic diagram of the CSAP architecture for the pixel readout operation

The current sensing circuit ideally holds the potential V_X of the Row_Bus1 line to a fixed value. Consequently, the parasitic capacitance C_X of the Row_Bus1 line does not influence the circuit speed. The current sensed by the sensing circuit is corresponding to the drain current of the transistor Q_2 as $I_X = I_{D2}$, while at the same time the sensing circuit outputs a current I_{sens} that is proportional to I_X. As a result, the output current I_{sens} is equal to the drain current of Q_2 as $I_{sens} = I_{D2}$, or equal to its scaled version as $I_{sens} = kI_{D2}$ in order to provide more current gain by the external feedback circuitry. The current feedback circuit finds the difference between the drain

current I_{D2} of Q_2 and the bias current $I_{bias,}$ and then multiplies the difference with a current gain A_i. This amplified current difference is then fed back to the Row_Bus2 line. If the sensing circuit provides a scaled version of the current I_{D2}, then the current feedback circuit would compare kI_{sens} and I_{bias}, resulting in a total current gain of kA_i. The CSAP readout configuration provides negative feedback that effectively forces the drain current of Q_2 to be equal to the biasing current I_{bias}. This feedback configuration results in a faster response time by a factor equal to the current gain A_i or kA_i.

The transfer function of the CSAP architecture during the readout operation is given by equation 3.1. The –3dB frequency determines the readout speed of the CSAP circuit and is given by equation 3.2. Hence, the unity gain frequency is increased by a factor proportional to the current gain A_i or kA_i with respect to the unity gain frequency of the standard APS design.

$$H_{readout}(j\omega) = \frac{g_{m2}r_{ds2}}{1+g_{m2}r_{ds2}} \frac{1}{1+j\omega\frac{C_Y r_{ds2}}{(1+A_i)(1+g_{m2}r_{ds2})}} \tag{3.1}$$

$$f_{-3dB} = \frac{(1+A_i)(1+g_{m2}r_{ds2})}{2\pi C_Y r_{ds2}} \tag{3.2}$$

The negative feedback operation of the CSAP readout may be described as follows. If the input voltage value at the gate of Q_2 increases, the gate-source voltage

V_{GS2} of Q_2 increases. As a result, the current I_{D2} of Q_2 increases, which is now larger than the bias current I_{bias}. The sensing circuit senses this current change and outputs a current I_{sens} that is equal to I_{D2}. The feedback circuit compares I_{sens} and I_{bias}, multiplies their difference, and supplies the Row_Bus2 line with the additional current $I_O = A_i*(I_{sens}-I_{bias}) = A_i*(I_{D2}-I_{bias})$. This additional current is positive, because $I_{sens} > I_{bias}$; hence it charges the parasitic capacitance of the Row_Bus2 line. As a result, the potential of the Row_Bus2 line increases which reduces the gate-source voltage V_{GS2} of Q_2, thereby reducing I_{D2} until it is equal to I_{bias}, at which point the feedback becomes zero. Similarly, if the input voltage value at the gate of Q_2 decreases, the additional current I_O becomes negative, thus it discharges the parasitic capacitance of the Row_Bus2 line. As a result, the potential of the Row_Bus2 line and source terminal of Q_2 decreases, thus giving rise to the gate-source voltage V_{GS2} of Q_2 and subsequently increases I_{D2} to a value that is equal to I_{bias}.

The current sensing circuit of Figure 3.2 can be implemented as one of the current mirror circuits shown in Figure 3.3. The possible circuit implementations are the simple current mirror as shown in (b), or some advanced current-mirrors such as the Wilson current mirror, the cascode current mirror and the wide-swing current mirror, shown in (c), (d) and (e) respectively [24].

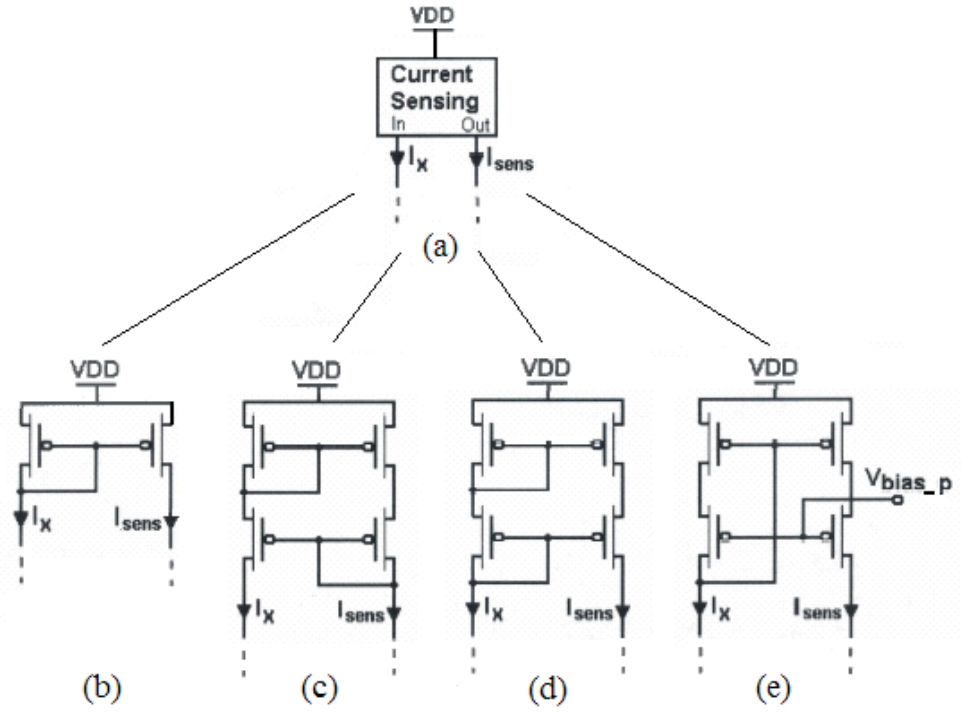

Figure 3.3 Current mirror implementations of the current sensing circuit

3.3.2 CSAP Pixel Reset Operation

During the pixel reset operation, the in-pixel readout transistor Q_2 is in the common-source type amplifier configuration and the CSAP architecture is constructed as shown in Figure 3.4. The current sensing approach can be used to extend the bandwidth of the common-source amplifier used for the active reset, thus reducing the reset noise that is injected by the reset transistor Q_1. The drain terminal of transistor Q_2 is connected through the Row_Bus1 line to the bias current source I_{bias} and the output of the current amplifier. The source terminal of transistor Q_2 is connected through the switch Q_3 to an external current sensing circuit.

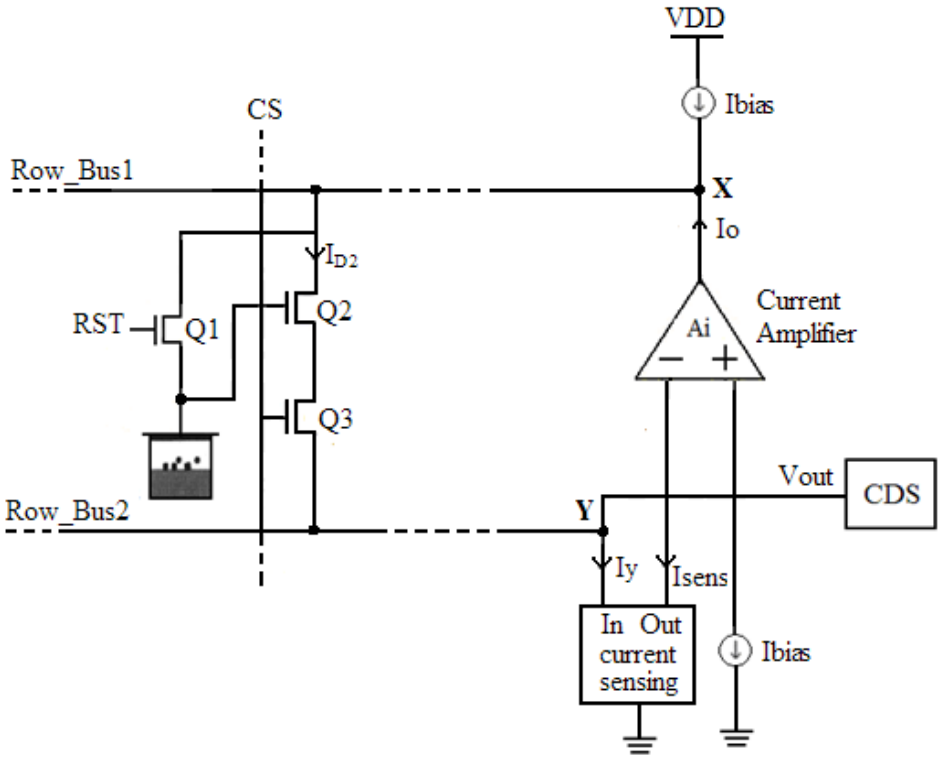

Figure 3.4 Schematic diagram of the CSAP architecture for the pixel reset operation

During the pixel reset operation, reset transistor Q_1 and column select transistor Q_3 are asserted. Transistor Q_2 is in a common-source configuration. The sensing circuit ideally holds the potential V_Y of the Row_Bus2 line to a fixed value; therefore the parasitic capacitance of the Row_Bus2 line does not influence the circuit speed. The current sensed by the sensing circuit corresponds to the drain current of transistor Q_2 as $I_Y = I_{D2}$, while at the same time the sensing circuit outputs a current I_{sens} that is proportional to I_Y. As a result, the output current I_{sens} is equal to the drain current of Q_2 as $I_{sens} = I_{D2}$, or equal to its scaled version as $I_{sens} = kI_{D2}$ to provide more current

gain by the external feedback circuitry. The current amplifier finds the difference between the drain current I_{D2} of Q_2 (or its k times scaled version) and the bias current I_{bias} and then multiplies the difference with a current gain A_i. This amplified current difference is then fed back to the Row_Bus1 line.

Similar to the readout configuration, the reset configuration provides negative feedback that effectively forces the drain current of Q_2 to be equal to the bias current I_{bias}. This feedback operation effectively increases the unity-gain frequency of the common-source amplifier. The transfer function of the equivalent common-source amplifier during the reset operation and its unity-gain frequency f_{ta} are given by equations 3.3 and 3.4 respectively [6].

$$H_{readout}(j\omega) = -\frac{g_{m2}r_{ds2}}{1+j\omega\frac{C_X r_{ds2}}{1+A_i}} \tag{3.3}$$

$$f_{ta} = \frac{(1+A_i)g_{m2}}{2\pi C_X} \tag{3.4}$$

Since the feedback operation of the CSAP architecture increases the unity-gain frequency and the bandwidth of the common-source amplifier by a factor of A_i (kA_i), then more reset noise power will fall within the amplifier's bandwidth and will be attenuated by the negative feedback of the common-source amplifier. Assuming that the cut-off frequency of the thermal noise is lower than the unity-gain frequency, then

the total reset noise would be reduced by the open loop DC gain of the amplifier as $(g_{m2} * r_{ds2})(1 + \frac{r_{ds2}}{r_{ds1}})$.

It has been shown in [8] that the in-pixel transistor Q_2 can be configured as a common-source amplifier in order to attenuate the reset noise injected by the reset transistor Q_1 into the photo-detector element. In this active reset configuration, the reset switch is placed in the negative feedback path of the amplifier. Ideally, assuming that the common-source amplifier has a bandwidth that is larger than the reset noise bandwidth, the total reset noise would be reduced by a factor of $(1 + A_{DC})(1 + \frac{r_{ds2}}{R_{on}})$; where $A_{DC} = g_{m2} * r_{ds2}$ is the open-loop DC gain of the common-source amplifier, R_{on} is the on-resistance of the reset transistor Q_1, and r_{ds2} is the equivalent resistance of the amplification transistor Q_2. However, the pixel-level common-source amplifier is heavily loaded by the parasitic capacitance C_X of the Row_Bus1 line, which significantly reduces its unity-gain bandwidth. The unity-gain bandwidth of such an amplifier is readily lower than the reset noise cut-off frequency, so that most of the reset noise power is still injected into the photo-detector without any attenuation. As a result, due to the reduced bandwidth of the in-pixel amplifier, the circuit reset noise attenuation capabilities are limited and only a modest noise reduction by a factor of 2 has been reported in [8].

3.3.3 CSAP Noise Analysis

During the pixel readout operation, the CSAP design decreases the settling time of the pixel readout circuit. By decreasing the settling time, the two consecutive samples in a CDS scheme are closer together in time, which in turn reduces the effective 1/f noise contribution of the source follower transistor.

By applying the CDS operation at the output of the CSAP design, we can clearly see the reduction of the flicker noise from the in-pixel source follower amplifier. If we subtract the two flicker noise samples of the CDS separated by the time interval τ as shown in equation 3.5, we can obtain the difference between the flicker noise samples in the frequency domain as shown in equation 3.6 and described in [20]. Then, the PSD of the resulting noise y can be calculated as shown in equation 3.7. If we decrease the settling time, the corresponding sampling frequency will increase, shown as filter 1 and filter 2 in Figure 3.5. As a result, the area enclosed between the PSD of the 1/f noise and filter 2 is smaller than the area enclosed between the PSD of the 1/f noise and filter 1, indicating a reduction of the resulting 1/f noise at the output of the CDS. Therefore, by providing faster readout and sufficiently decreasing the settling time, the CSAP readout method may attenuate the 1/f noise power down to the thermal noise level. Corner frequency is between 100 KHz and 200 KHz for a typical CMOS 0.35 μm process; however it is not an important factor here.

$$y(t) = f(t) - f(t-\tau) \tag{3.5}$$

$$Y(j\omega) = F(j\omega) * H(j\omega) = F(j\omega) * (1 - e^{-j\omega\tau}) \tag{3.6}$$

$$|Y(j\omega)|^2 = F^2(j\omega) * 4sin^2\frac{\omega\tau}{2} \tag{3.7}$$

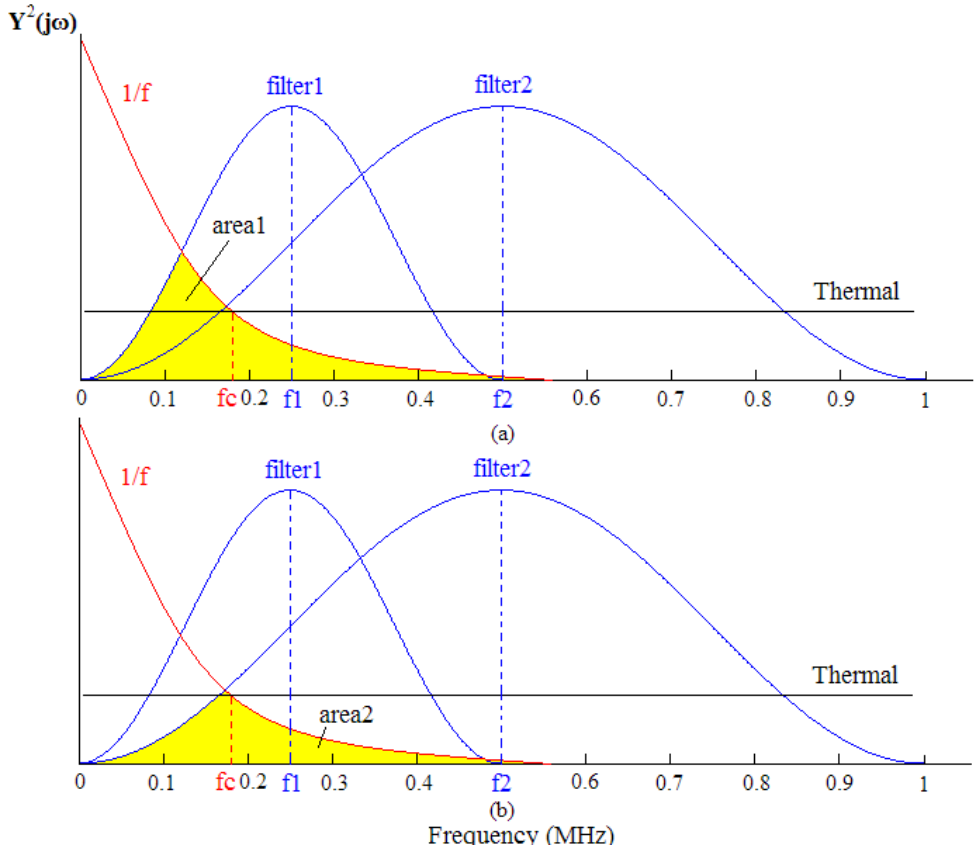

Figure 3.5 Flicker noise power reduction as a function of sampling frequency (i.e. readout circuit settling time). A decrease in the settling time results in a reduced area below the power spectral density curve and reduced flicker noise power at the output of the CDS.

Two major noise sources in the CSAP design come from the in-pixel source follower transistor and the shared current amplifier. Noises from the in-pixel source follower amplifier are the dominant components of the readout noise in the CSAP design. On the other hand, noise from the shared current amplifier can be neglected since it is attenuated by the amplifier's high open-loop gain, as studied in [30].

Overall, the CSAP sensor design increases array readout speed for greater frame rates and decreases flicker noise through the external CDS circuit and faster settling times.

3.4 CSAP Simulation Results

3.4.1 CSAP Simulation using a Ideal Amplifier

The CSAP design was first simulated in the Cadence design tool using an ideal OTA, which is essentially a voltage controlled current source (VCCS) in parallel with an output resistance R_{out}, as shown in Figure 3.6. The current sensing circuit in Figure 3.3 was implemented as a simple PMOS transistor in the triode region. Transistors Q_1, Q_2, and Q_3 are part of the standard pixel unit. Transistors Q_6 and Q_7 are NMOS transistors and each serves as a current source I_{bias}. Transistors Q_4 and Q_5 are PMOS transistors operating in the triode region and each has an equivalent resistance $R_{on,}$ which connects to the input of the ideal OTA.

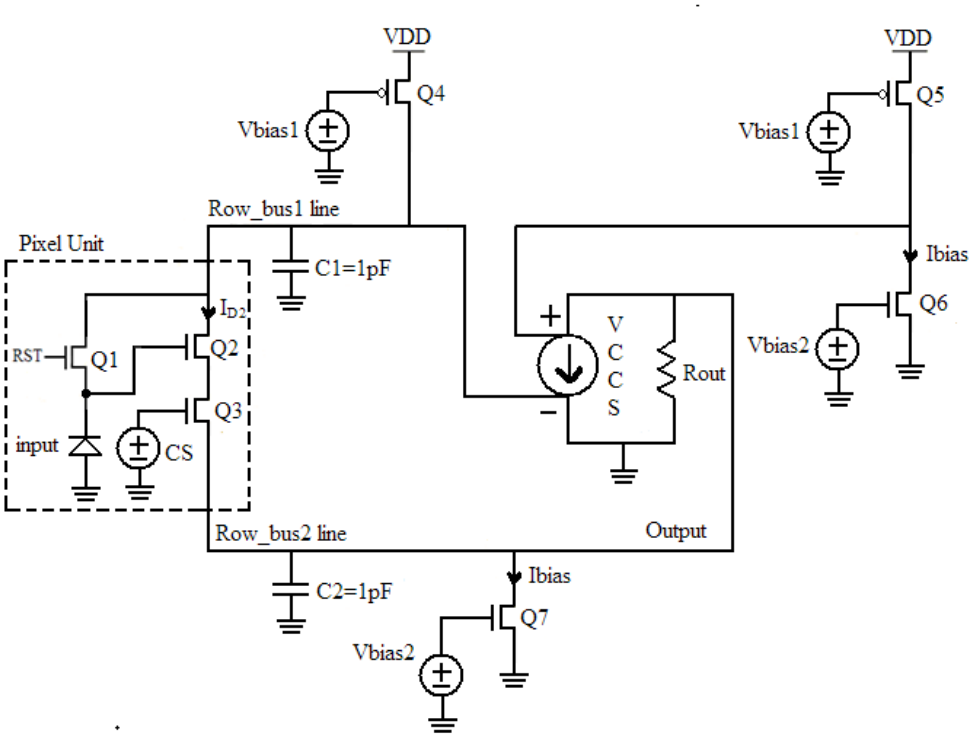

Figure 3.6 Simulated CSAP architecture with an ideal OTA

The VCCS component represents the instance parameter of transconductance G_m of the amplifier; therefore it sets the gain of the amplifier. With a current gain of 10, we obtained an output waveform of the proposed CSAP design and comparison to an output waveform of standard APS design, as shown in Figure 3.7.

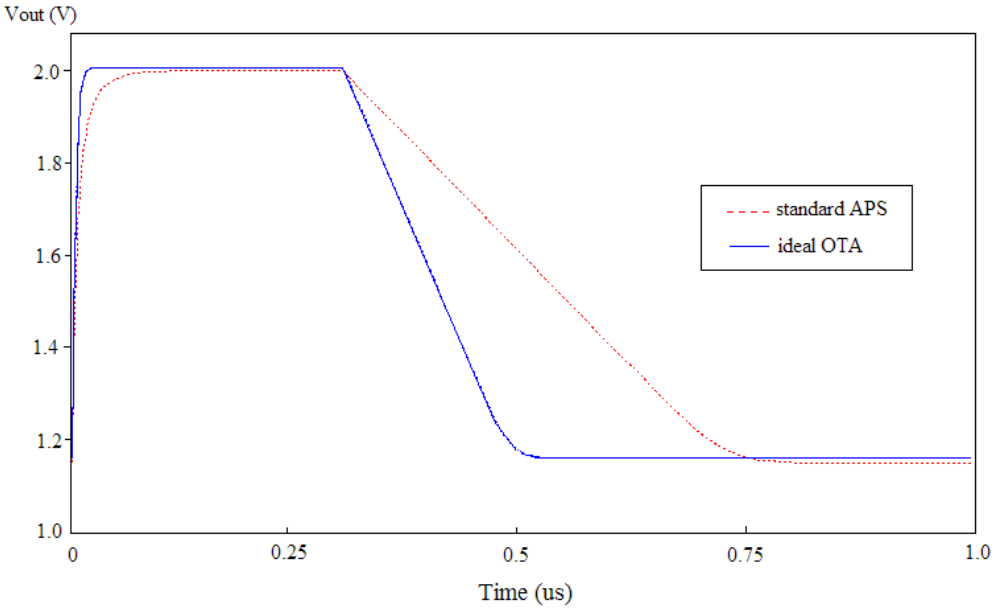

Figure 3.7 Comparison of the output waveforms of the standard APS and proposed CSAP design with an ideal OTA for a 0.35-um CMOS technology

By applying the settling accuracy of 1%, the readout speed measurements are as follows: the charging time T_c of the proposed CSAP design with a transconductance gain of 10 is measured to be 20 ns, as compared to the standard APS design with a measured charging time of 100 ns. These measurements show a speed improvement by a factor of 5 for charging time T_c. However, the measurements show a speed improvement by a factor of only 2.5 for discharging time T_d. T_d of the proposed CSAP design with a transconductance gain of 10 is measured to be 200 ns, as compared to the standard APS design with a measured discharging time of 500 ns.

3.4.2 CSAP Simulation using a Practical Amplifier

The OTA employed in Figure 3.6 is just an ideal case, which was used to verify the concept of the readout speed improvement by utilizing an out-of-pixel negative feedback. However, a practical OTA has to be designed and stability of the design must be analyzed. Therefore we implemented a practical OTA composed of CMOS transistors. We then simulated the CSAP design in the Cadence design tool using a practical OTA. The schematic is shown in Figure 3.8.

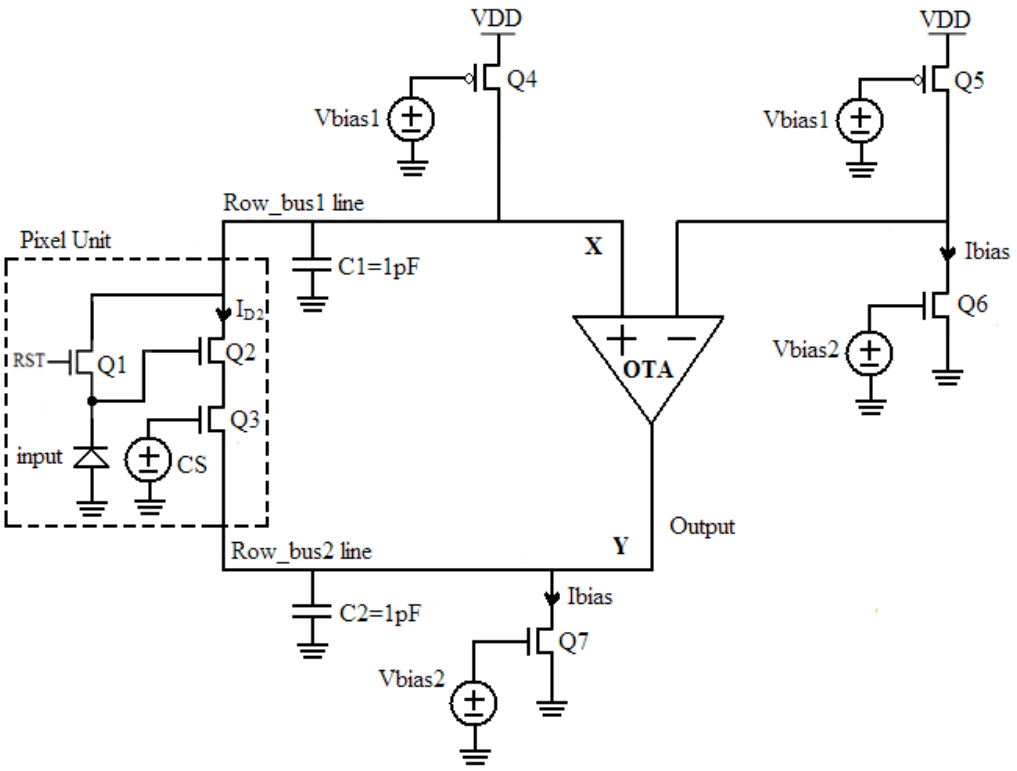

Figure 3.8 Simulated CSAP architecture with a practical OTA

Just as in Figure 3.6, simple PMOS transistors Q_4 and Q_5 operating in the triode region are employed as the current sensing circuit and each has an equivalent resistance $R_{on,}$ which connects to the input of the amplifier. Transistors Q_1, Q_2, Q_3 are part of the standard pixel unit. Q_6 and Q_7 are NMOS transistors and each serves as a current source I_{bias}. The amplifier has a transconductance G_m and an output resistance R_{out}. The total current gain of the current sensing circuit combined with the OTA is calculated as $A_i = G_m * R_{on}$.

The OTA shown in Figure 3.8 is implemented as a balanced OTA [31] and is shown in Figure 3.9 in detail. The OTA structure contains transistors M_1 through M_{15}. There are five PMOS transistors M_3, M_4, M_5, M_7 and M_8. The rest of the transistors are NMOS transistors.

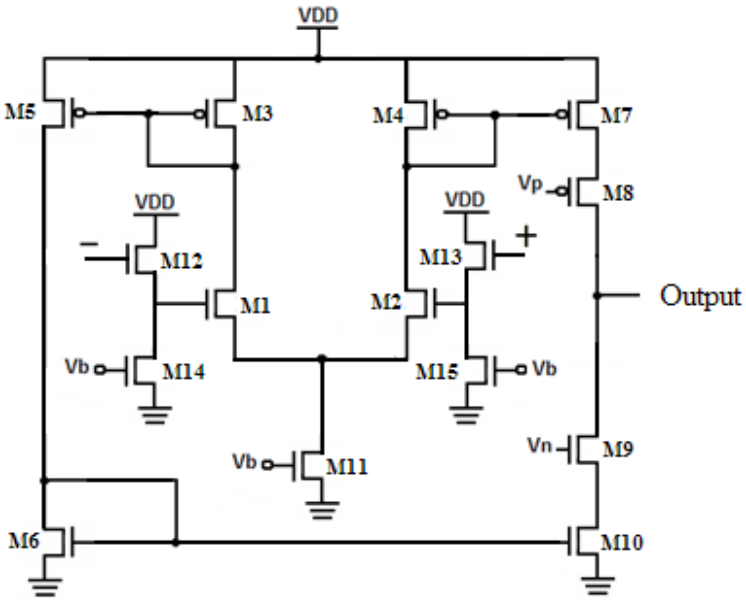

Figure 3.9 Balanced OTA implemented in CSAP design

This balanced OTA is an example of the two-stage amplifier with differential input and single-ended output. The OTA converts the two input voltages into a single output current and feeds the current back to the source follower transistors Q_2 of the pixel unit.

This balanced OTA contains three pairs of current mirrors; they are PMOS current mirrors M_3 and M_5, M_4 and M_7, and NMOS current mirror M_6 and M_{10}. It also contains three bias transistors M_{11}, M_{14} and M_{15}. Transistor M_{11} provides the bias current to the input differential pair M_1 and M_2. M_{14} and M_{15} are used to bias source-follower transistors M_{12} and M_{13}. The source-follower transistors M_{12} and M_{13} are required to reduce the common-mode voltage level going into the gate terminals of M_1 and M_2. The OTA also contains two cascade transistors M_8 and M_9, which are designed to boost the open loop gain of the OTA by enhancing the output resistance of the amplifier. Transistors M_3, M_4, M_5 and M_6 are designed to have width of 1 μm and minimum length of 0.35 μm, whereas output cascaded transistors M_7, M_8, M_9 and M_{10} are designed to boost the open loop gain of the OTA by enhancing the output impedance of the amplifier, and thus designed to have width of 10 μm and length of 0.35 μm. The design purpose is to boost the gain of the OTA and thus reduce the settling time of the CSAP sensor design.

Each gain stage of this two-stage OTA introduces at least one pole in the open-loop gain transfer function, making it difficult to guarantee stability in a feedback system [24]. The gain and phase plot of this balanced OTA is shown in Figure 3.10.

The DC gain of the OTA is measured to be 55 dB and the unity gain frequency is measured to be 70 MHz. Also, as shown in Figure 3.10, the gain crossover (GX) occurs well before phase crossover (PX), which results in a stable response of the OTA when applied in a negative feedback configuration.

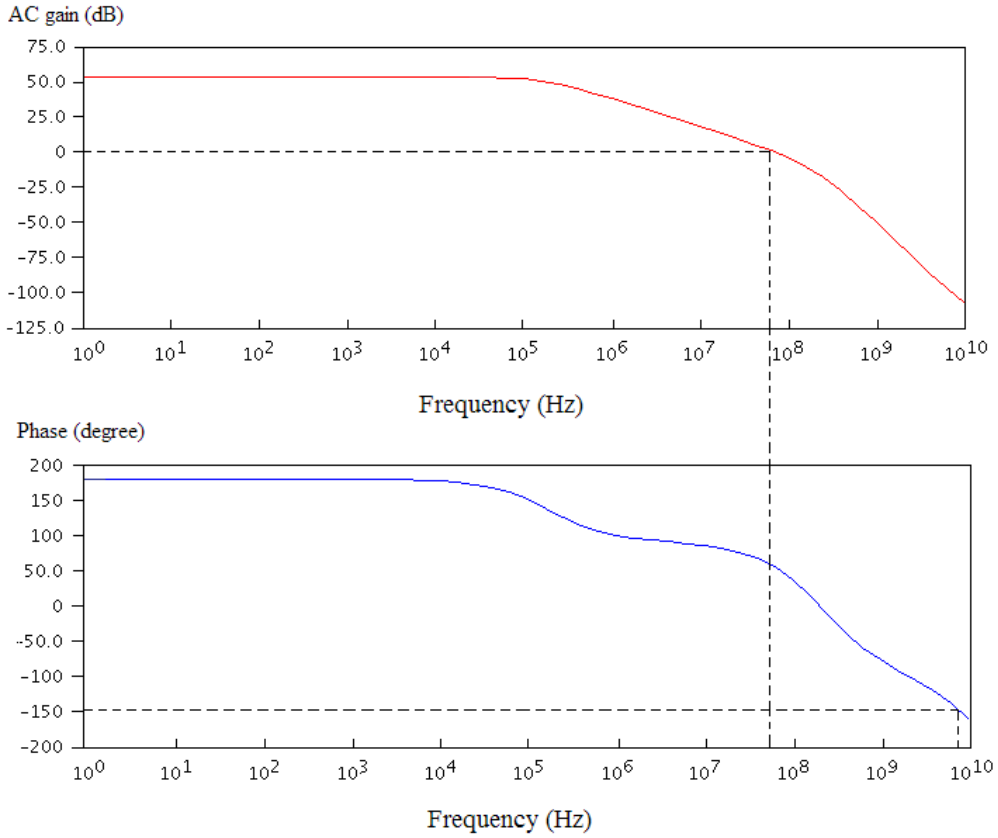

Figure 3.10 Gain and phase plot of the Balanced OTA

An output waveform of the proposed CSAP design with the balanced OTA was compared to the output waveform of the standard APS design, as shown in Figure 3.11. By applying the settling accuracy of 1%, the readout speed measurements are as

follows: the charging time T_c of the proposed CSAP design with balanced OTA is measured to be 20 ns, as compared to 100 ns for the standard APS. The discharging time T_d of the proposed CSAP design is measured to be 100 ns, as compared to 500 ns for the standard APS. Therefore, we proved that our proposed CSAP design has a total speed improvement of 5 when employing a practical balanced OTA.

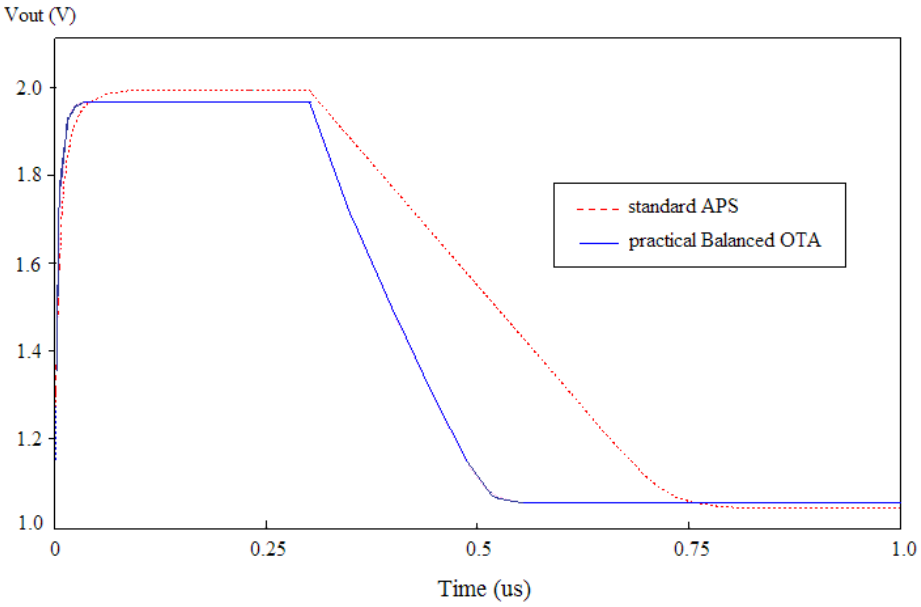

Figure 3.11 Comparison of the output waveforms of the standard APS and proposed CSAP design with practical balanced OTA for a 0.35-um CMOS technology

Since the CSAP architecture employs a negative feedback loop, the stability of the loop has to be carefully addressed. A relatively large parasitic capacitance C_1 is introduced on the Row_Bus1 line in addition to the main parasitic capacitance C_2 on the Row_Bus2 line. Therefore, appropriate values have to be chosen for g_m and R_{out} of the balanced OTA and the on-resistance R_{on} of the PMOS transistor M_4 operating

in the triode region. These values have to be chosen such that the output waveform does not exhibit oscillations and overshoot. Since the output voltage changes exponentially with time during charging and linearly during discharging [4], the disparity between the charging and discharging time exists.

3.5 CSAP Layout Design

Figure 3.12 shows the layout design of the out-of-pixel readout circuitry of the CSAP architecture in a 0.35µm single-poly four-metal process. It contains a balanced OTA in a current sensing configuration, NMOS bias current transistors, and a current sensing circuit implemented as a single PMOS transistor. The balanced OTA in the center of the figure is pointed out, and the rest of the layout represents two PMOS transistors and two NMOS bias current transistors.

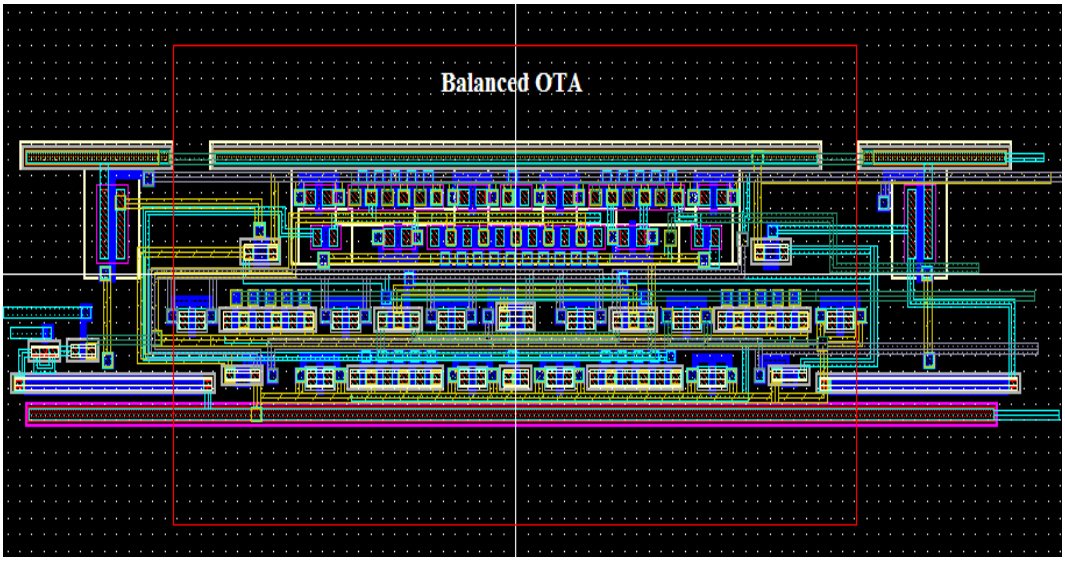

Figure 3.12 Layout of CSAP out-of-pixel readout circuit

To minimize the etch effect during fabrication, we use dummy transistors in the layout to achieve good matching of the devices (e.g., we add dummy transistors at the end of each transistor finger). We have also employed the common-centroid layout method to design the layout of the input differential pair of the balanced OTA; the purpose is to cancel the effect of long-range variations and reduce orientation mismatch of the two input transistors [32].

3.6 Summary

Since the bandwidth of the readout circuit in the proposed CSAP design increases by an order of magnitude, the thermal noise of the source follower transistor referred to the output increases and may limit the performance of the imager. To overcome this noise problem, the CSAP feedback amplifier can be used only for a fraction of the readout time and then can be disconnected when the output signal is expected to reach within one-half of the LSB of the ADC used for conversion [33]. At the end of the readout interval, the feedback amplifier is turned off, which lowers the noise bandwidth and reduces thermal noise contribution to the level that is comparable to the level in standard APS.

To eliminate both the reset and 1/f noise of the pixel readout, an on-chip full CDS will become inevitable [34]. Since the settling time of the CSAP design with a practical balanced OTA has improved by a factor of 5 compared to the standard APS design, the two consecutive samples of CDS circuit become closer to each other in

time. By reducing the time difference between the two CDS samples, the low frequency cut-off point will increase, and then attenuate the 1/f noise from the in-pixel source follower transistor 5 times more than in the standard APS designs.

Chapter 4

RAPS Design Theory and Concept

4.1 Introduction

As CMOS image sensor performance benefits become more and more prominent over CCD, the demands for low noise, low power, high readout speed, and high dynamic range have become important concerns in recent years [35]. In addition, the fixed pattern noise (FPN) is also becoming a very important noise source in the CMOS imager. To reduce offset related FPN, correlated double sampling (CDS) technique is required for both the voltage-mode APS and the current-mode APS [36].

Most of the CMOS imagers employ external correlated double sampling (CDS) circuitry to remove DC offset related FPN noise and 1/f noise. CDS is an analog memory element implemented as an external array of capacitors to store the initial voltages of the photodiodes immediately after the reset operation. After the light integration phase, the photodiode voltages are subtracted from the stored reset voltages, which effectively remove the offset related FPN and the reset (kTC) noise arising from the reset and amplification transistors [2]. The external array of

capacitors is either placed at the pixel site or outside the pixel area. The design in which the capacitor is placed at the pixel site reduces the fill factor, so the preferred CDS method employs a capacitor outside of the pixel area without compromising the pixel fill factor. However this CDS method still requires significant silicon area outside of the pixel array, which may take as much area as the imaging region itself. In addition, gain related FPN cannot be removed, but it is instead exacerbated by applying the CDS [2].

We propose a reconfigurable active pixel sensor (RAPS) design, where the amplifier structure used to read out the pixel is also employed to perform the reset operation. This method performs inherent CDS and effectively eliminates the need for external CDS circuits that are used in existing CMOS APS design. The underlying idea is to use the internal capacitance of the photo-detector to store samples of the DC offset and flicker noise from the amplifier structure. The amplifier, which is a differential-input amplifier, is reconfigurable such that the in-pixel source follower transistor acts as an inverting input device during the reset operation and it also acts as a non-inverting input device during the readout operation. The objective of the RAPS design is to combine the low cost, small pixel size, and low power consumption of the conventional APS design with low noise. It achieves reduced DC offset related FPN and flicker noise without an external array of storage capacitors, thus requiring less total silicon area than conventional APS design. RAPS design also reduces gain variation related FPN by incorporating a high open loop gain differential amplifier as opposed to the conventional APS structure, which employs a sub-unity

gain source follower amplifier. Finally, the RAPS design greatly reduces reset noise by placing the reset transistor in the feedback path of an inverting amplifier, which actively drives the photodiode reset voltage to the reference level.

This design can be implemented in a multiplexed configuration in which the neighboring photo-detectors can share a common amplification transistor, thus enabling designs with 1.5 transistors per pixel while still preserving the performance.

4.2 RAPS Architecture

The idea of RAPS design is derived from the Active Column Sensor (ACS) design as described in Section 2.24. The ACS design improves the gain related FPN problems of the standard APS design by applying a differential amplifier as a unity gain buffer, however additional CDS circuits are still required to remove the DC offset and flicker noise. We improve the ACS design with a reconfigurable idea, so that we do not need the CDS circuit to remove DC offset and flicker noise. The underlying idea is to use the internal capacitance of the photo-detector to store samples of the DC offset and the flicker noise from the amplifier structure. The readout differential amplifier can be reconfigured, such that its non-inverting (positive) and inverting (negative) terminals are reconfigured to act as its inverting and non-inverting terminals, respectively, in two different phases (reset and readout) of the operations.

The general RAPS architecture is shown in Figure 4.1, which contains a pixel unit and a shared reconfigurable current mirror readout circuit in a unity gain amplifier configuration.

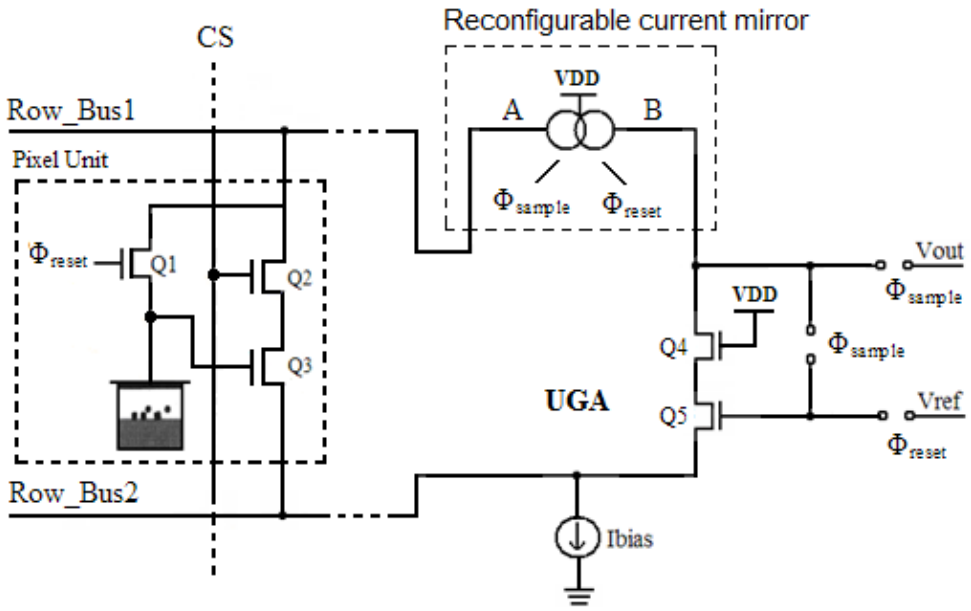

Figure 4.1 Schematic diagram of a general CSAP architecture

On the left side of the circuit is the in-pixel APS structure. It contains a photo-detector, an NMOS reset transistor Q_1, an NMOS column select transistor Q_2, and an NMOS readout transistor Q_3. The only difference between this APS structure and the standard APS is that the reset transistor Q_1 connects the photodiode to the Row_Bus1 line instead of the power supply line VDD. On the right side is the out-of-pixel readout circuit shared by pixels of one row, which is a reconfigurable amplifier in a

unity gain buffer topology. The output voltage value is then sampled with external circuitry. This differential amplifier is biased by the external current source I_{bias}.

The reconfigurable amplifier in the proposed RAPS design is a differential single-ended amplifier. The amplifier is reconfigured by reconfiguring an active-load of the differential amplifier. The active load of the differential single-ended amplifier is implemented as a current mirror, where a diode-connected current branch reflects its current into the driven current branch. During the pixel reset operation, the active-load is configured such that the diode-connected side of the current mirror supplies the inverting input of the differential input transistors of the amplifier and inputs reference voltage V_{ref}. During the pixel readout phase, the active-load is reconfigured such that the diode-connected side of the current mirror supplies the non-inverting input of the differential input transistors of the amplifier.

The reconfigurable PMOS current-mirror in Figure 4.1 is used as the active-load of the RAPS architecture. The possible implementations are shown in Figure 4.2, which includes the single transistor pair PMOS current mirror as shown in (b), or some advanced PMOS current mirrors such as the Wilson PMOS current mirror, the cascode PMOS current mirror and the wide-swing PMOS current mirror to enhance the output impedance of the mirror, as shown in (c), (d) and (e) respectively [24].

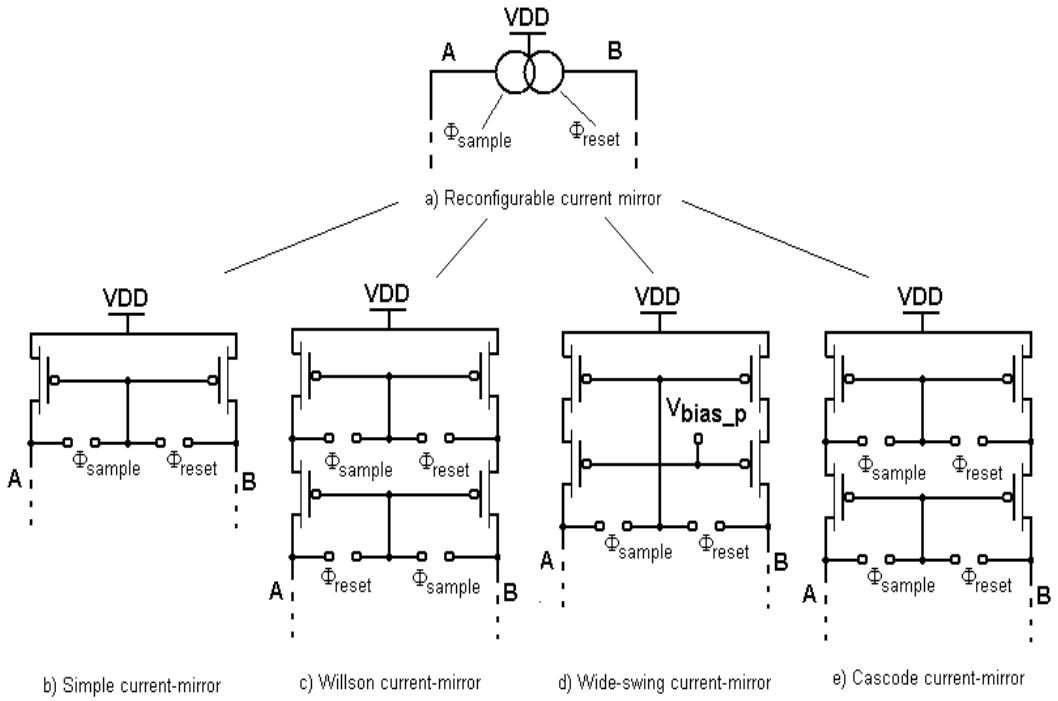

Figure 4.2 Possible implementations of Reconfigurable PMOS current-mirror

4.3 RAPS Operation Principles

4.3.1 RAPS Pixel Reset Operation

The photo-detector measurements are performed during two non-overlapping clock phases in the proposed RAPS design, which are called the reset phase and the readout phase.

During the reset phase, switches Q_1 and Q_2 of Figure 4.1 are turned on. The reference voltage V_{ref} is applied to the input transistor Q_5, and the current branch B of

the current mirror load forms a diode-connected branch. As a result, the differential-input amplifier is configured as a unity gain amplifier (UGA) such that the in-pixel input device (transistor Q_3) serves as the inverting input of the differential amplifier, and the out-of-pixel input device (transistor Q_5) serves as the non-inverting input of the differential amplifier. The output of the amplifier is connected through the in-pixel reset switch Q_1 to the photodiode terminal and the negative input of the amplifier, as shown in Figure 4.3 [35]. The photo-detector capacitance stores the reference voltage value V_{ref}.

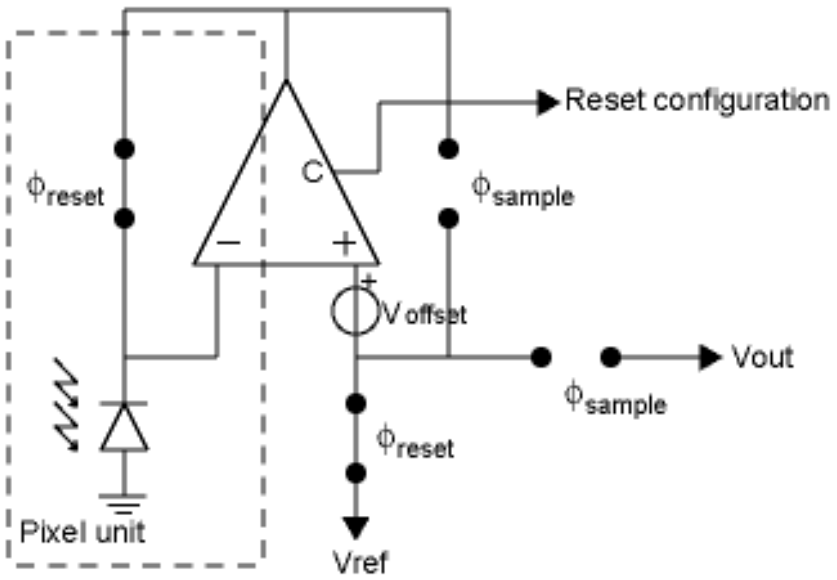

Figure 4.3 RAPS architecture configured for pixel reset operation

As a result, the output voltage from the amplifier V_{reset} which is equal to the sum of the reference voltage V_{ref}, the amplifier's DC offset voltage V_{offset}, and the amplifier's flicker noise voltage $e(t_1)$, is stored at the photodiode capacitance denoted by equation 4.1.

$$V_{reset} = V_{ref} + V_{offset} + e(t_1) \tag{4.1}$$

4.3.2 RAPS Pixel Readout Operation

After the reset phase, both switches Q_1 and Q_2 of Figure 4.1 are turned off, disconnecting the pixel from the bus-lines and starts the integration phase. The photodiode is exposed to light for an integration time T_1 during which it accumulates photo-generated charge. The voltage across the photodiode terminal decreases in proportion to the light intensity. When the integration phase is complete, the pixel is again selected by asserting switch Q_2.

During the readout phase, the amplifier is reconfigured as a unity gain amplifier (UGA) such that the current branch A of the current mirror forms a diode-connected branch, so the in-pixel input device (transistor Q_3) serves as the non-inverting input of the differential amplifier, and the out-of-pixel input device (transistor Q_5) serves as the inverting input of the differential amplifier. At the same time, the output node of the UGA (the drain terminal of Q_4) is connected to the inverting input Q_5 to form a negative feedback of the UGA with the photodiode connects to the non-inverting input of the amplifier as shown in Figure 4.4 [35].

After an integration time T_1, the output voltage at the end of the readout phase is sampled and denoted by equations 4.2 and 4.3.

$$V_{out} = V_{ref} + V_{offset} + e(t_1) - \left(\frac{I_{ph}T_1}{C_{diode}} + V_{offset} + e(t_1 + T_1)\right) \quad (4.2)$$

$$= V_{ref} - \frac{I_{ph}T_1}{C_{diode}} + (e(t_1) - e(t_1 + T_1)) \quad (4.3)$$

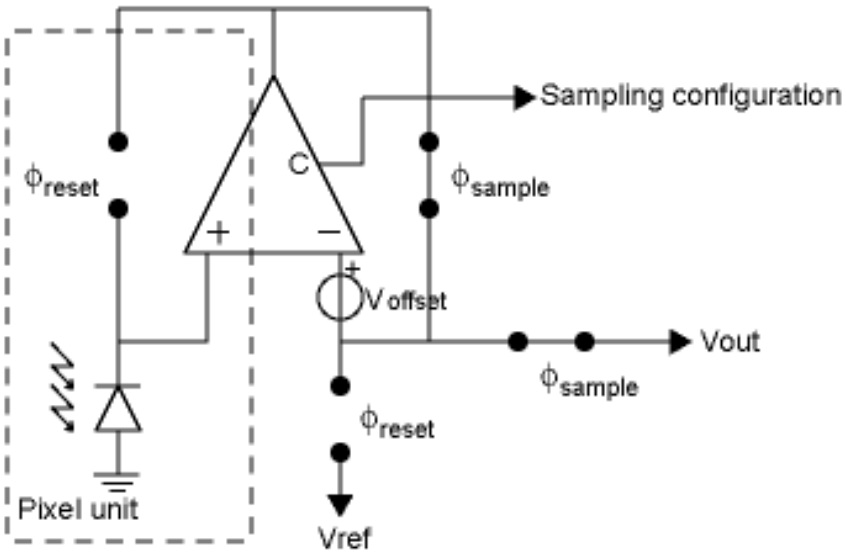

Figure 4.4 RAPS architecture configured for pixel readout operation

4.3.3 RAPS Noise Analysis

From equation 4.3, we notice that the DC offset voltage of the amplifier is cancelled completely and the flicker noise is differentiated as $e(t_1) - e(t_1+T_1)$, which

highly attenuates the noise power due to its low frequency nature. All these noise improvements are performed without applying the external CDS circuit.

Another significant benefit of the RAPS architecture is the reduction of the reset (kTC) noise. During the reset phase, the reset switch of the pixel is in the amplifier's negative feedback path. The reset noise voltage $V_n(t)$ is generated by the thermal noise in the channel of the reset switch, and it accumulates on the photodiode with a gain of -1 producing $-V_n(t)$ at the output of the amplifier. This output voltage is then fed back to the photodiode to cancel the reset noise voltage originally at the photodiode terminal. In this way the reset noise voltage is driven to zero by the negative feedback. It has been shown that the reset noise power is reduced by a factor equal to the product of the amplifier's open-loop gain and the ratio between the amplifier's output impedance and reset switch impedance (this ratio is in the range of 1000). Therefore, the reset noise cancellation depends on the amplifier's gain bandwidth product [37].

4.4 RAPS Simulation Results

4.4.1 ACS Simulation using a Ideal Amplifier

The ACS design [15] with an ideal OTA was simulated in the Cadence design tool. The schematic is shown in Figure 4.5.

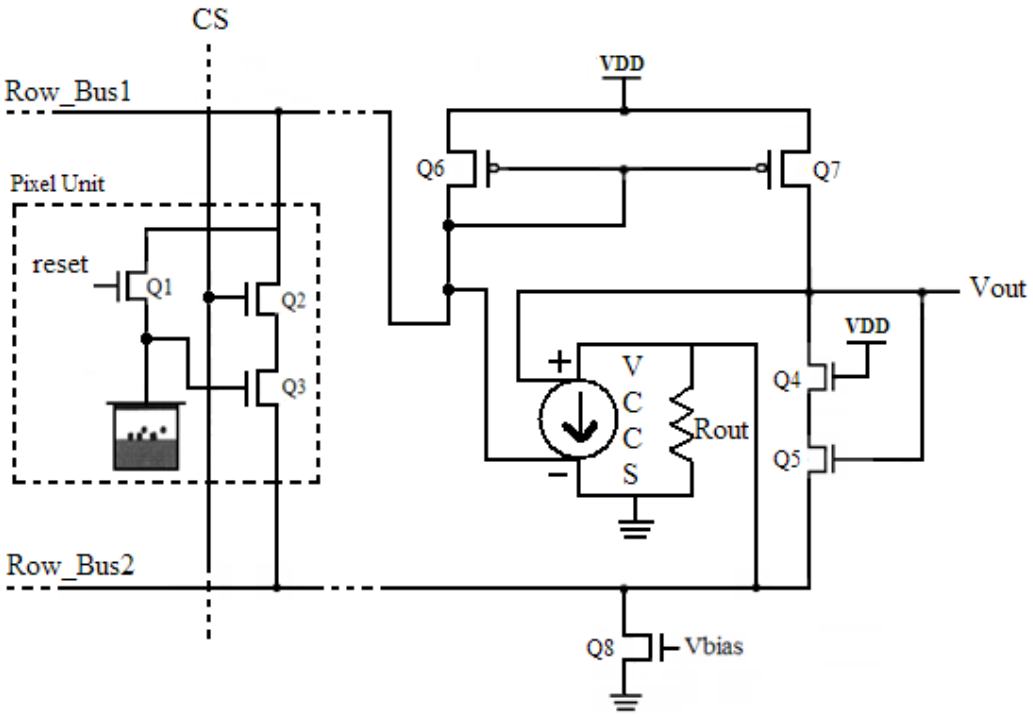

Figure 4.5 ACS architecture with an ideal OTA for settling time enhancement

Transistors Q_1, Q_2 and Q_3 are part of the standard pixel unit. Transistors Q_2 and Q_4 are cascaded to boost the open-loop gain of the ACS structure. NMOS transistor Q_8 provides a biasing current to the differential pair transistors Q_3 and Q_5. The ideal OTA is essentially a voltage controlled current source (VCCS) in parallel with an output resistance R_{out}.

Figure 4.6 shows the output waveform of the ACS design with an ideal OTA in comparison to the standard APS design.

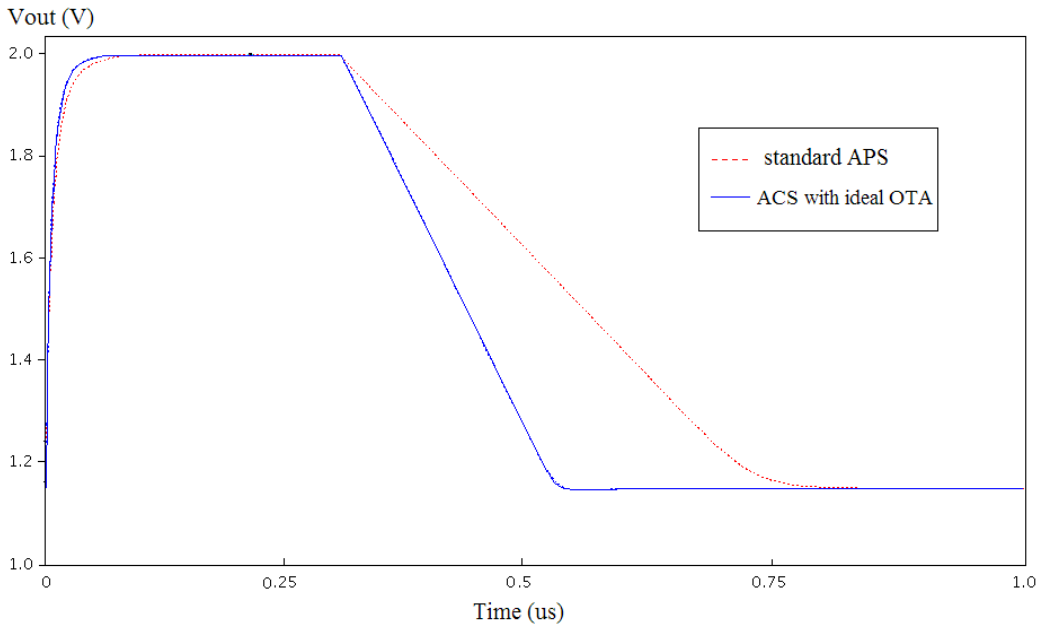

Figure 4.6 Comparison of the output waveforms of the standard APS and ACS design with an ideal OTA using 0.35-um CMOS technology

ACS design exhibits faster settling time than the standard APS design, because of the higher current capabilities of the differential amplifier structure. The speed of the APS structure is limited by the current driving capabilities of the in-pixel source-follower transistor, which is usually chosen to be a minimum size transistor due to high fill factor requirement. Therefore, the small in-pixel transistor of the APS design limits the speed of the positive voltage swings on the bus lines. In contrast, the transistor Q_5 of the ACS design provides the current for the positive voltage swing on the Row_Bus1 line, does not have to be a minimum size transistor since it's external

to the pixel area. Therefore, the ACS design allows faster settling time and increased readout speed.

4.4.2 RAPS Simulation using a Practical Amplifier

The RAPS design was then simulated using the standard single transistor pair (Q_6 and Q_7) as the PMOS current mirror, the schematic is shown in Figure 4.7.

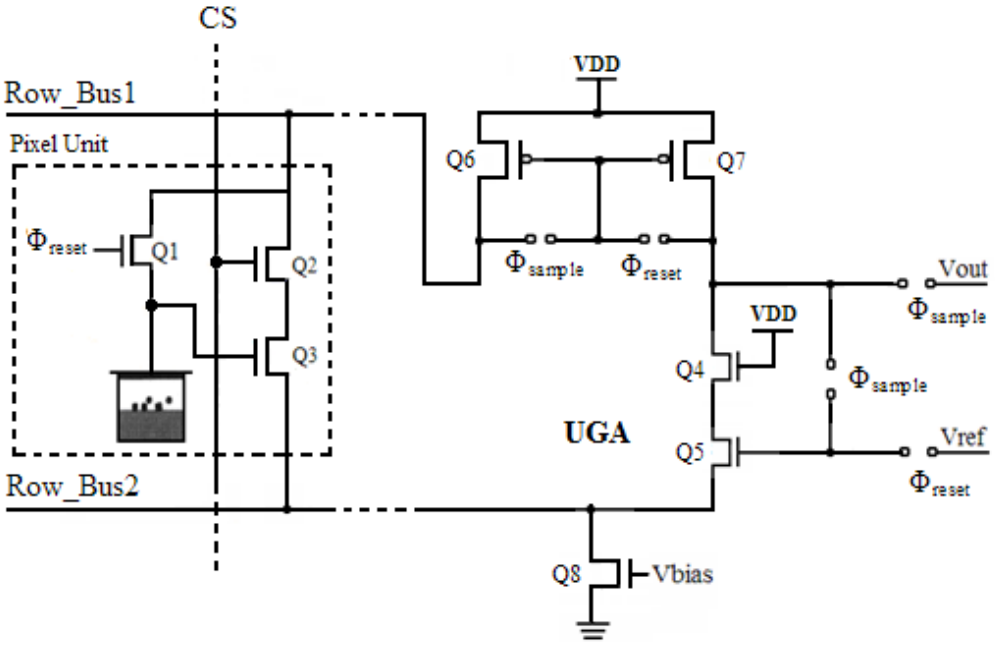

Figure 4.7 Transistor level implementation of the RAPS architecture

Transistors Q_1, Q_2 and Q_3 are part of the standard pixel unit. Transistors Q_2 and Q_4 are cascaded to boost the open-loop gain of the RAPS structure. NMOS transistor Q_8 provides a biasing current for the input differential pair Q_3 and Q_5 of the amplifier.

During the reset phase, transistors Q_1 and Q_2 are turned on. The reference voltage V_{ref} is applied to the input of Q_5, and the transistor Q_7 of the PMOS current mirror forms a diode-connected branch. As a result, the differential amplifier is configured such that Q_3 and Q_5 become the inverting and the non-inverting inputs, respectively, as shown in Figure 4.8.

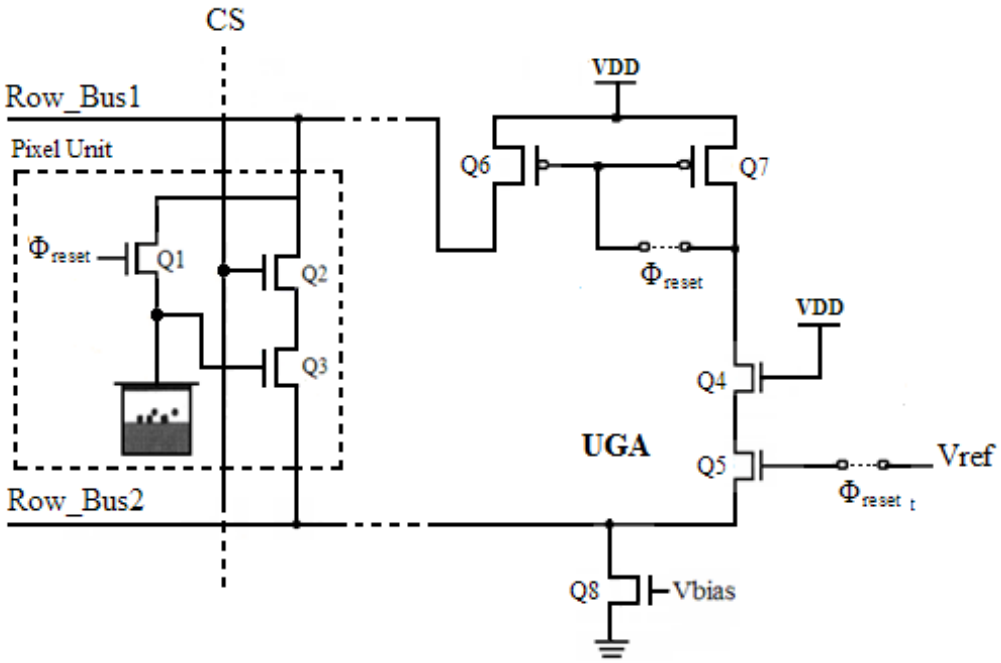

Figure 4.8 Transistor level implementation of the RAPS architecture during reset phase

The output of the amplifier is connected through the switch Q_1 to the photo-detector terminal and the negative input of the amplifier. At the end of reset phase, the photodiode capacitance stores the reference voltage value V_{ref}. Both switches Q_1 and Q_2 are turned off disconnecting the pixel from the bus lines, and the pixel begins the integration phase. After a specified integration time T_1, the pixel is selected again

by asserting the switch Q_2. During the readout phase, the amplifier is reconfigured as shown in Figure 4.9. Transistor Q_6 of the PMOS current mirror forms a diode-connected branch and the input transistor Q_3 is reconfigured as the non-inverting input. At the same time, the output node is connected to the negative input Q_5 of the amplifier, forming a unity gain amplifier structure. The output voltage value proportional to the integrated light intensity is then sampled with an external circuitry. At the end of the readout phase, the amplifier's DC offset noise is eliminated and the flicker noise is attenuated.

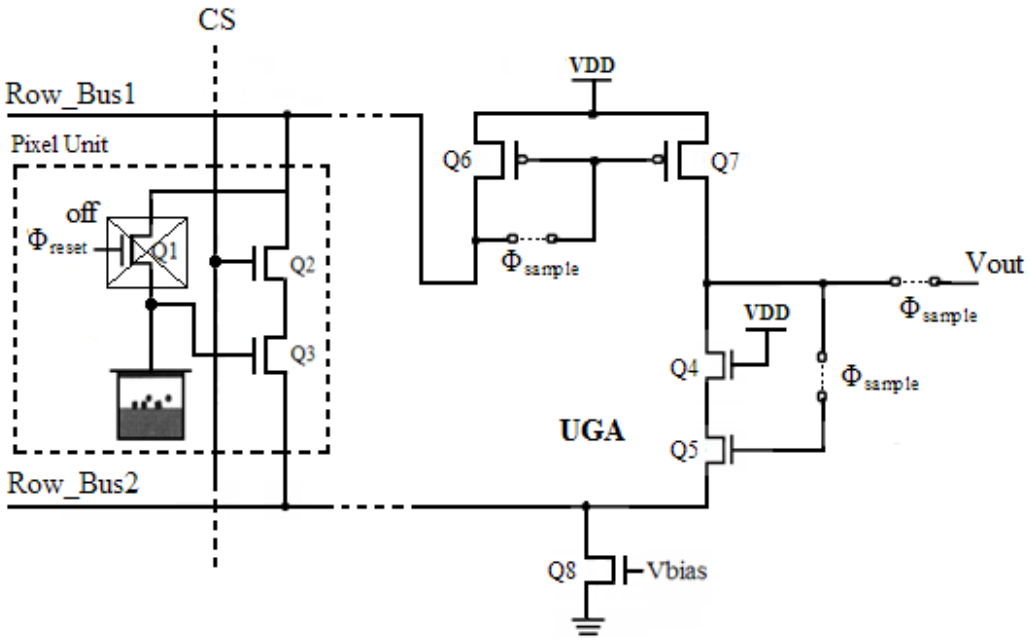

Figure 4.9 Transistor level implementation of the RAPS architecture during readout phase

The switches Φ_{sample} and Φ_{reset} are implemented as transmission gates (TG), the actual transistor level implementation [38] is shown in Figure 4.10. It is made by the

parallel combination of an NMOS transistor M_1 and a PMOS transistor M_2, with the input at the gate of M_1 being the complementary to the input at the gate of M_2. This complementary signal is made through a CMOS inverter that contains a PMOS transistor M_3 and an NMOS transistor M_4.

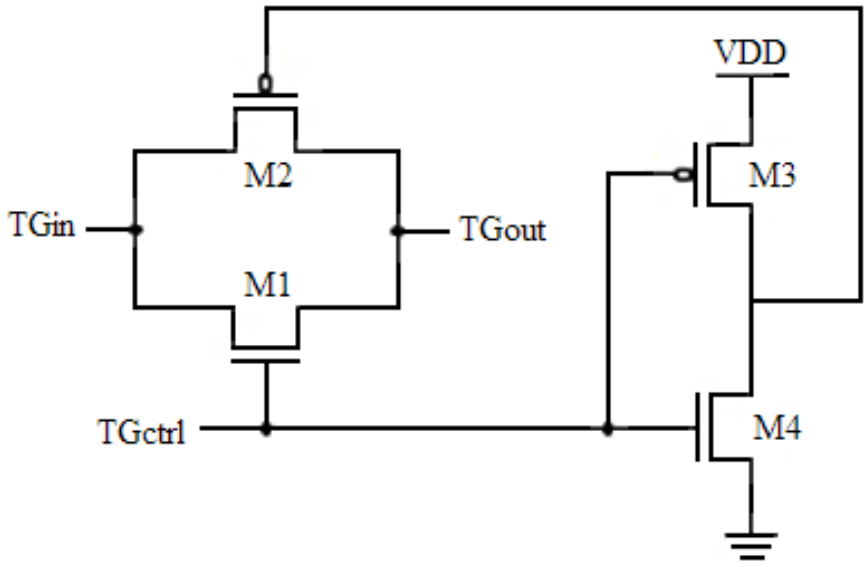

Figure 4.10 Transistor level implementation of transmission gate (TG)

When the gate input to the NMOS transistor is '0' and the complementary '1' is input to the PMOS gate, both gates are turned off. However, when the gate input to the NMOS is '1' and its complementary '0' is input to the PMOS gate, both gates are turned on and passes the input signal to the output without any degradation.

A good settling response with a high phase margin is the most important parameter for an amplifier implemented within a negative feedback loop [39]. However, the two most critical bus lines Row_Bus1 line and Row_Bus2 line of the

RAPS structure introduce relatively high capacitive loads to the amplifier. The capacitances denoted by C_1 and C_2 in Figure 4.11 are the parasitic capacitances, which tend to introduce additional poles to affect amplifier's settling performance. Parasitic capacitances C_1 and C_2 were both simulated using 1 pF capacitors for their actual effects on the amplifier. Figure 4.12 shows the output waveforms of the RAPS design with and without parasitic capacitances. An oscillatory settling response is illustrated in the output waveform of the RAPS design with parasitic capacitances C_1 and C_2.

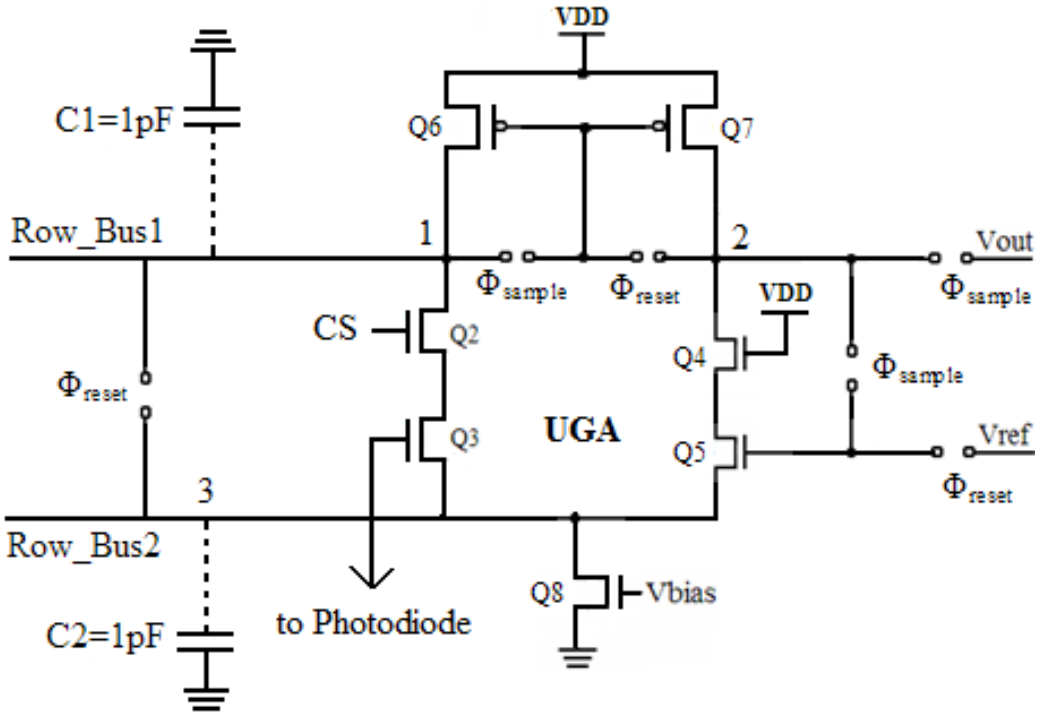

Figure 4.11 RAPS architecture showing the parasitic capacitance C_1 and C_2

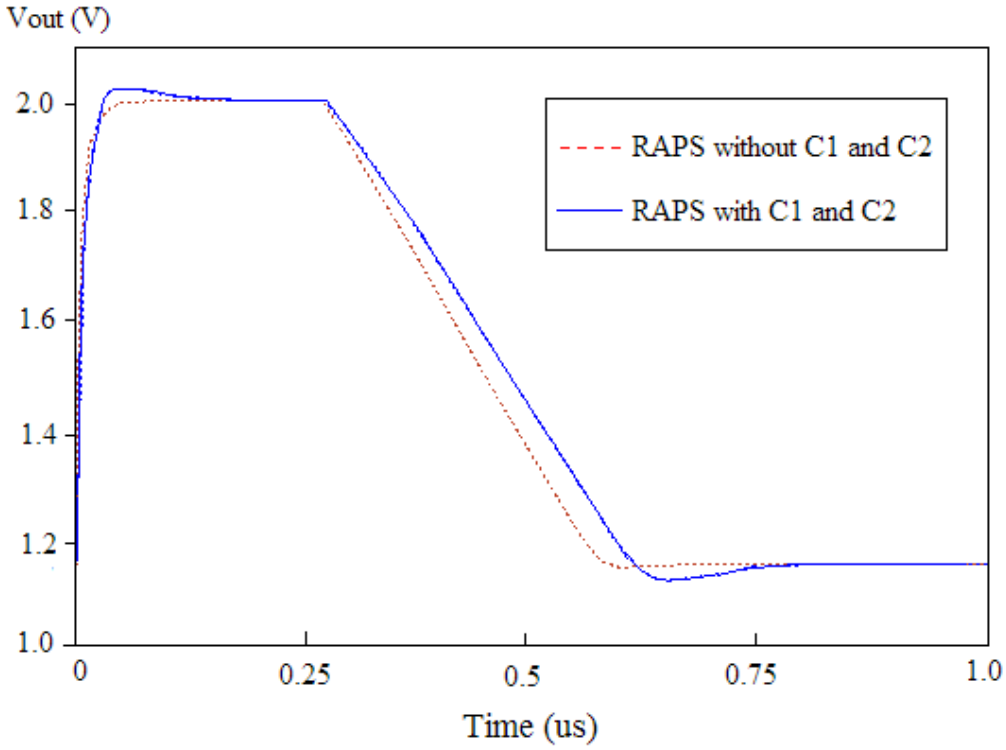

Figure 4.12 Output waveform comparison of RAPS design with and without the parasitic capacitance C_1 and C_2

In Figure 4.11, PMOS current mirror Q_6 and Q_7 can be large enough to drive the parasitic capacitance C_1, since the transistors are outside the pixel area. However, the in-pixel transistor Q_3 is designed to be a minimum size transistor to maintain high fill factor, it cannot provide enough current to drive the parasitic capacitance C_2. Therefore, C_2 must be driven by other support circuitry, in order to make sure it does not affect amplifier's settling response. One solution to overcome the speed degradation due to parasitic capacitances C_1 and C_2 is to utilize an additional CMOS amplifier. There are basically four types of operational amplifier (Opamp) we can

choose from; they are the Telescopic Opamp, the Folded-cascode Opamp, the Two-stage Opamp and the Gain-boosted Opamp [24]. In order to overcome the oscillatory settling response of the output waveform, we are targeting at two-stage Opamp since it can provide a high gain with faster setting time, higher output swing and lower readout noise. This amplifier could be used to monitor the difference between nodes 1 and 2, and supply additional current proportional to the difference to the node 3.

The complete schematic of RAPS design with an OTA is shown in Figure 4.13 (a). The ideal small signal equivalent model of the CMOS OTA is shown in Figure 4.13 (b) [18]. Transistors Q_1, Q_2 and Q_3 are part of the standard pixel unit. PMOS transistors Q_6 and Q_7 form a single transistor pair PMOS current mirror, which is designed to have large W/L ratio since they are outside of the pixel unit. Transistors Q_2 and Q_4 are cascoded to boost the open-loop gain of the RAPS structure. NMOS transistor Q_8 provides a biasing current to the input differential pair Q_3 and Q_5 of the amplifier. The switches Φ_{sample} and Φ_{reset} are implemented as transmission gates (TG) as shown in Figure 4.10, where the input signal to the Φ_{reset} switch is complemented to the input signal of the Φ_{sample} switch. The voltage difference between nodes 1 and 2 is amplified and is converted into an output current by the CMOS OTA in order to drive the node 3.

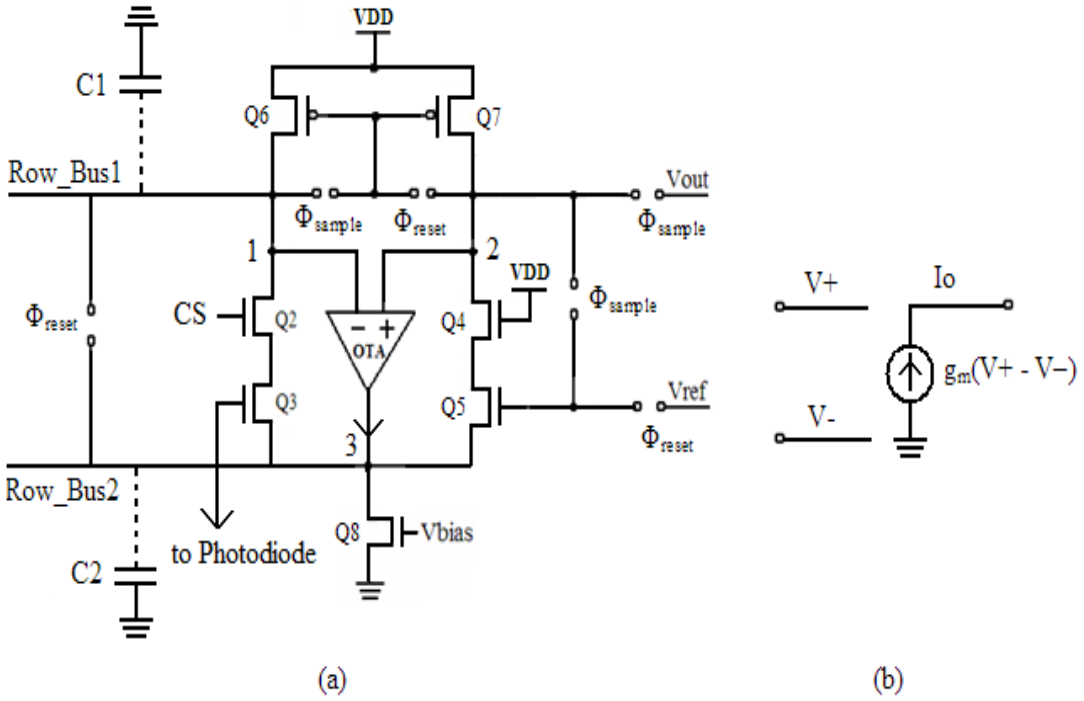

Figure 4.13 (a) RAPS architecture with an OTA, (b) ideal small signal equivalent of OTA

The two stage amplifier utilized in this design is a differential input – single ended balanced OTA [31]. This OTA contains three current mirrors as shown in Figure 4.14. They are PMOS current mirrors M_3 and M_5, M_4 and M_6, and NMOS current mirror M_7 and M_8. Transistors M_3 – M_6 are PMOS transistors. All other transistors are NMOS transistors. Transistor M_9 provides the bias current for the input differential pair M_1 and M_2. Transistors M_3, M_4, M_5 and M_7 are designed to have minimum W/L ratio, whereas transistors M_6 and M_8 are designed to have multiple fingers of the minimum W with same L. All of the transistors must operate in the saturation region to ensure a stable operation. The design goal is not only to avoid the oscillatory

settling response of the output waveform, but also to boost the gain of the OTA which in turn reduces the settling time of the RAPS design.

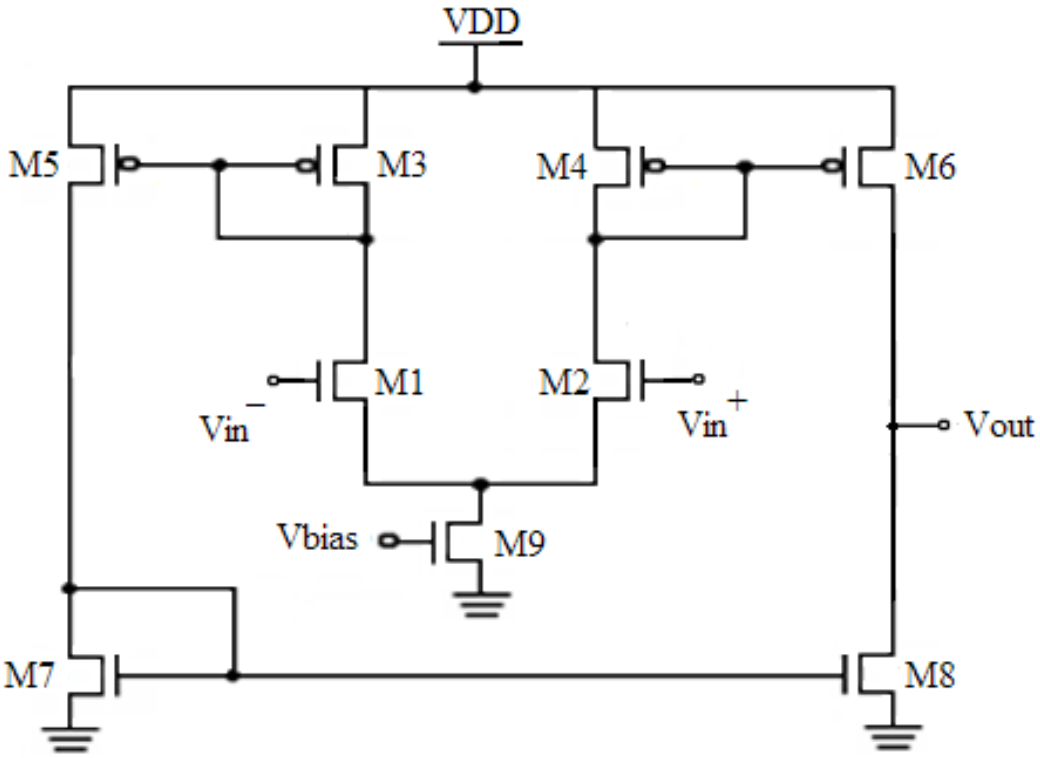

Figure 4.14 Balanced OTA implemented in RAPS design

In Figure 4.15, we compared the readout speed of the standard APS design to the RAPS design with a balanced OTA. By applying the settling accuracy of 1%, the speed measurements are as follows. The charging time T_c of the proposed RAPS design with an OTA is measured to be 25 ns, as compared to the charging time T_c of the standard APS with 100 ns. The discharging time T_d of the proposed RAPS design with an OTA is measured to be 125 ns, as compared to the discharging time T_d of the

standard APS with 500 ns. Therefore, we demonstrated that the RAPS design when employing a balanced OTA provides an overall speed improvement by a factor of four with respect to the standard APS.

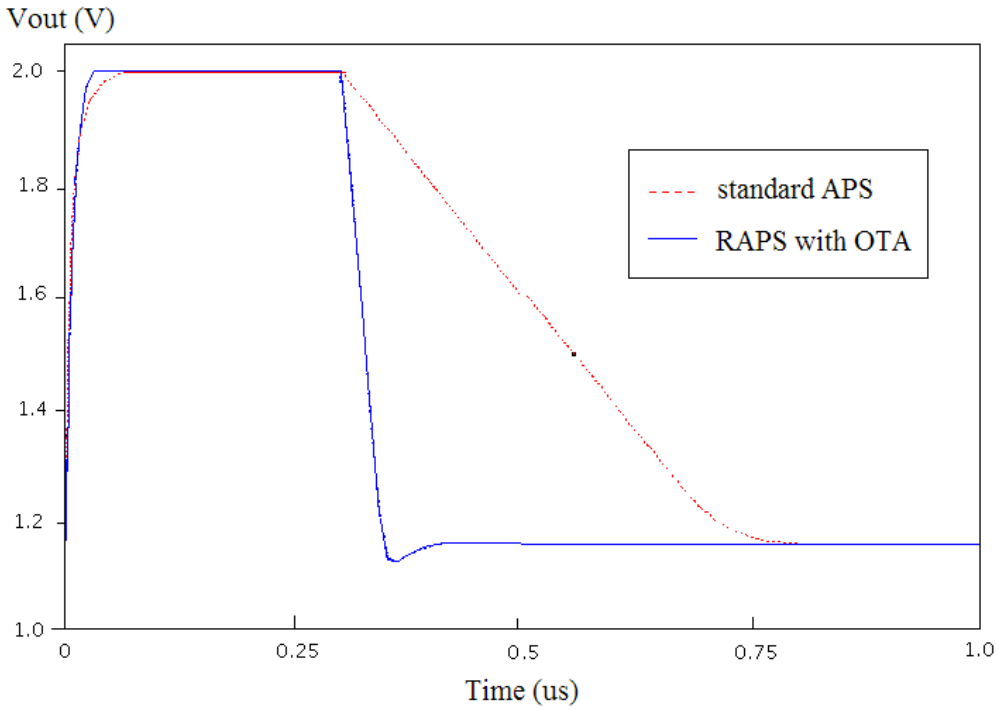

Figure 4.15 Comparison of the output waveforms of the standard APS and RAPS design with OTA using 0.35-um CMOS technology

We mentioned earlier in this chapter that more reset noise reduction is achieved with a higher gain bandwidth (GBW) product [37]; it is confirmed with the actual measurements from the simulations.

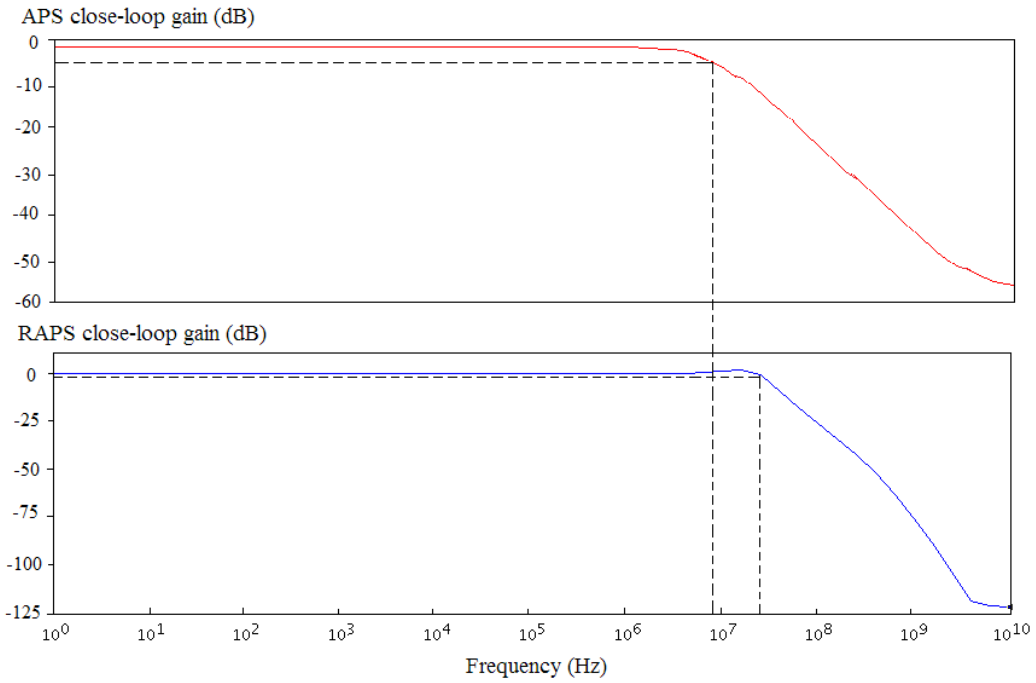

Figure 4.16 Comparison of the close loop gain of APS and RAPS design

As shown in Figure 4.16, the closed-loop gain of the RAPS design is measured to be 0.96 (1 dB), which is very close to the unity gain amplifier. In comparison, the APS design has a measured closed-loop gain of 0.85 (-1.4 dB). Therefore pixel to pixel gain related FPN can be greatly reduced in the RAPS design.

The -3dB bandwidth of the RAPS design is roughly measured to be 38 MHz, as compared to 900 KHz of the APS design. Therefore the GBW product of the RAPS design is 38 MHz as compared to 765 KHz of the APS design, which effectively reduces the reset noise caused by the reset transistor Q_1 in the RAPS design.

4.5 Summary

The proposed RAPS image sensor design utilizes a reconfigurable differential input readout amplifier, so that the correlated double sampling operation can be implemented without external capacitive elements as opposed to the conventional APS design, which in turn reduces overall silicon area and power consumption. In addition, the differential input amplifier allows higher open-loop gain and larger -3 dB bandwidth than the conventional source follower readout amplifier, which may effectively increases readout speed, decreases the reset noise if utilized in an active reset implementation, and reduces the gain related FPN. We have verified that the settling time of the RAPS design with a balanced OTA is reduced by a factor of four as compared to the standard APS design through simulations. The effective gain error reduction is also verified through simulations in a standard 0.35 μm CMOS process.

Chapter 5

CSAP Fabrication and Testing Results

5.1 Introduction

CMOS imagers have experienced rapid development due to their significant advantages over CCD. Besides low power, low cost and ease of integration into other consumer products [1], high frame rate is another big improvement allowed by the CMOS image sensors. In order to obtain higher frame rates, an image sensor has to be able to read out the pixel values fast enough. With a faster readout image sensor, an image can be captured with clear details even in high light intensity or captured without blurring in the presence of motion blur conditions. The faster readout improves the dynamic range of the imager at both high signal levels, by allowing the photodiode to capture higher illumination levels without saturation, and at low signal levels, by decreasing the effects of 1/f noise.

The readout speed of the CMOS active pixel sensor (APS) readout circuits has been briefly discussed in [4]. It was observed that the readout time can be shortened by reducing the bias current of the access transistor. However, the smaller bias

current only shortens the APS readout time during charging; it prolongs the APS readout time during discharging by a huge amount. Therefore, we designed our access transistor to have a constant bias current of 2 μA, in order to balance readout times between the charging and the discharging phases.

5.2 CSAP Fabrication Details

5.2.1 Fabricated CSAP Structure

The fabricated CSAP image sensor architecture is shown in Figure 5.1. It is a test chip with array of 128 columns by 3 rows of pixels. A column selector is used to control the select signals of pixel units in each column, which is a 128-bit shift register containing 128 D flip-flops. One column of pixels is selected from the array by controlling three input signals to the column selector circuit: reset_CS, D_CS, and clk_CS. Each row of pixels has its own readout OTA amplifier located at the end of the row.

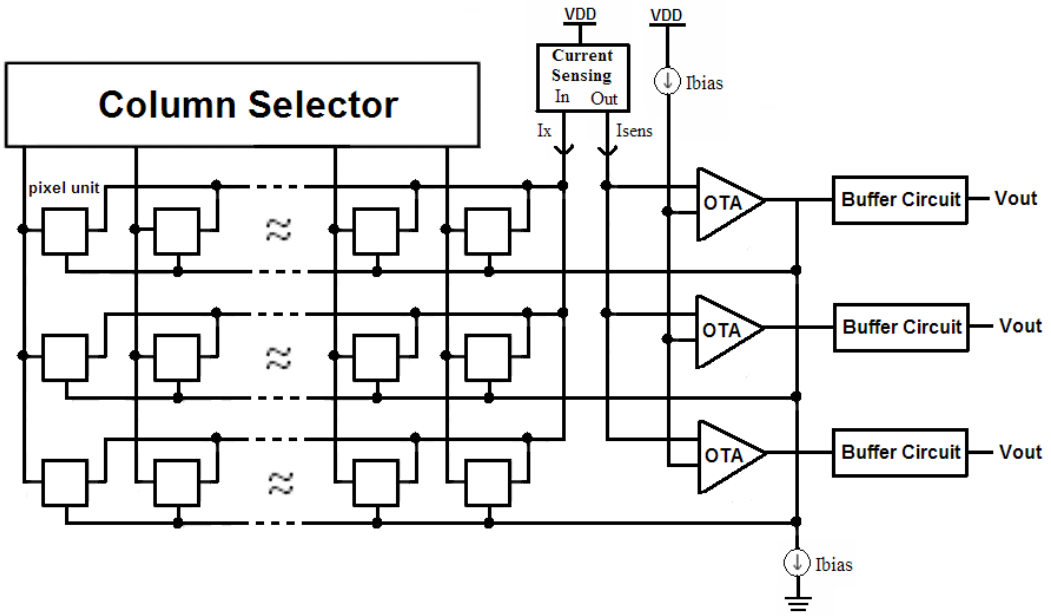

Figure 5.1 Building blocks of our proposed CSAP image sensor

During both readout and reset operations, the in-pixel readout transistor is always connected to the external circuit that provides current sensing and feedback. The current sensing circuit is designed to sense the current through the in-pixel readout transistor and to supply the resulting current I_{sens} to one input terminal of the OTA. The bias current I_{bias} equal to the biasing current of the in-pixel readout transistor is applied to the other input terminal of the OTA. The OTA circuit finds the difference between the current I_{sens} and the bias current I_{bias}, and amplifies the difference with a gain A_i. This amplified current difference is then fed back to the pixel unit in order to charge the read-line parasitic capacitance. In addition, the output of the OTA is

supplied to the input of a buffer amplifier that drives the pad frame and sends the signal off-chip. The shared OTA is designed so that its area fits the pixel pitch.

The detailed circuit schematic of our designed CSAP design is shown in Figure 5.2. It illustrates a single pixel unit and a readout amplifier shared by an entire row of pixels. The pixel unit employs standard APS design, which contains a photo-detector, NMOS reset transistor Q_1, source follower transistor Q_2, and column select transistor Q_3. The photo-detector is implemented as a standard photodiode in order to obtain high fill factor. The photodiode is implemented as an n-type diffusion in a p-type substrate as illustrated in Figure 2.16. The area of the photodiode is measured to be 95.84 μm^2, with the total area of the pixel unit measured to be 15 × 15 μm^2, therefore the entire 128 by 3 pixel array is measured to be 45 μm by 1920 μm. We used three metal layers and one poly layer in the single-pixel layout. The only difference between the standard APS pixel unit and our designed pixel unit is that we connect the drain terminal of the reset transistor Q_1 and the drain terminal of the source follower transistor Q_2 to the Row_Bus1 line instead of the power line VDD.

The readout amplifier outside the pixel unit contains an OTA and four bias transistors to provide desired currents. NMOS transistors Q_6 and Q_7 serve as the current sources I_{bias}. The current sensing circuit in Figure 5.1 is implemented with PMOS transistors Q_4 and Q_5 that provide active loads for the bias current sources I_{bias}. Both Q_4 and Q_5 are designed to operate in the triode region and each has an

equivalent resistance R_{on} of 2.5 KΩ. The drain terminal of Q_4 and Q_5 connects to the negative input terminal and positive input terminal of the amplifier, respectively.

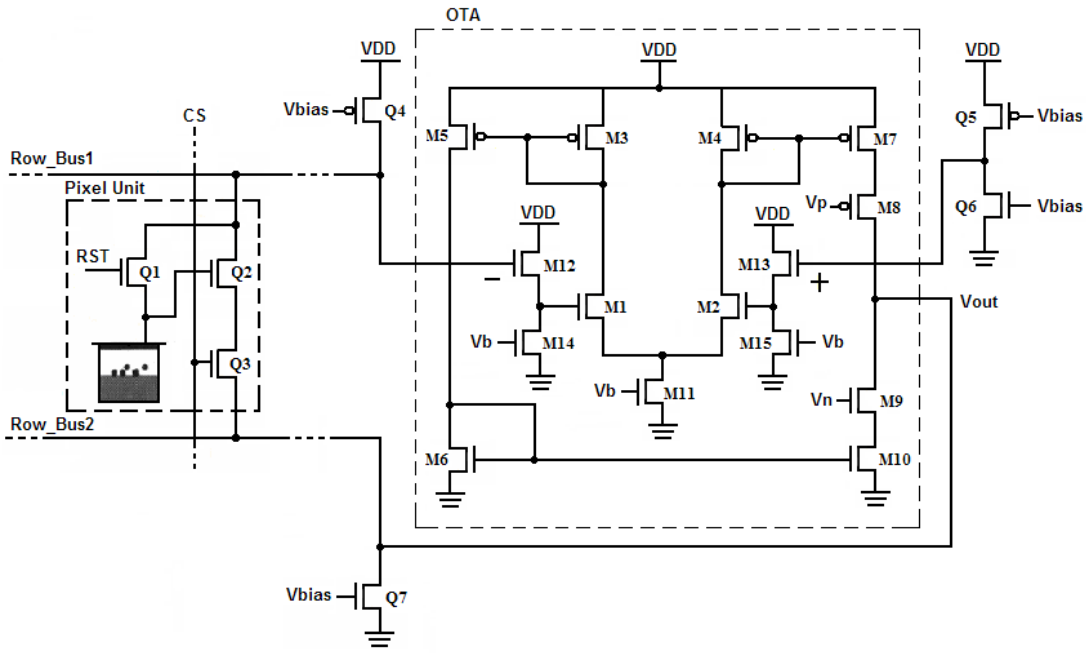

Figure 5.2 The proposed CSAP circuit schematic is shown in detail. To the left is one of the in-pixel APS structure and to the right is the out-of-pixel amplifier structure shared by 128 pixels of a row

The OTA structure contains transistors M_1 through M_{15}. There are five PMOS transistors M_3, M_4, M_5, M_7 and M_8. The rest of the transistors are NMOS transistors. The OTA is designed to have three pairs of current mirrors; they are PMOS current mirrors M_3 and M_5, M_4 and M_7, and NMOS current mirror M_6 and M_{10}. The OTA also contains two cascode transistors M_8 and M_9 designed to boost the open loop gain of the OTA by enhancing the output resistance of the amplifier. The transistor M_{11} provides the bias current for the input differential pair M_1 and M_2. Transistors M_{12}

and M_{13} act as voltage level shifters. They are required in the design to lower the common-mode voltage level provided to the input differential pair M_1 and M_2 of the OTA. Transistors M_3, M_4, M_5 and M_6 are designed to have width of 1 μm and minimum length of 0.35 μm, whereas transistors M_7, M_8, M_9 and M_{10} are designed to have width of 10 μm and length of 0.35 μm. The design goal was to provide a gain of 10 in order to reduce the settling time of the CSAP design.

5.2.2 Fabricated CSAP Bias Levels

In order to achieve the best circuit performance, the bias levels of both the pixel unit and the readout circuit need to be optimized. All bias levels are summarized in Table 5.1. There are 2 bias voltages in the pixel unit: V_{RST} and V_{CS}. V_{RST_HI} is set to 3.3V to reset the photodiode to the same potential as the power supply VDD. V_{CS_HI} is also set to 3.3V to make the column select transistor Q_3 work in the linear region, which can be used to reduce FPN. There are 4 more bias voltages in the out-of-pixel readout circuit: V_{bias}, V_b, V_p and V_n. V_{bias} controls four identical bias voltages supplied to two PMOS transistors Q_4 and Q_5, and two NMOS transistors Q_6 and Q_7. V_b controls the bias voltage supplied to the transistor M_{11} which provides the bias current for the input differential pair M_1 and M_2 of the CMOS OTA. V_p and V_n control the bias voltages supplied to the PMOS transistor M_8 and NMOS transistor M_9 of the OTA circuit, respectively.

Table 5.1 Summary table of fabricated CSAP circuit bias voltages

V_{RST_HI}	**3.3 V**	V_{RST_LO}	**0 V**
V_{CS_HI}	**3.3 V**	V_{CS_LO}	**0 V**
V_{bias}	**1.5 V**	V_b	**0.7 V**
V_p	**0.6 V**	V_n	**0.7 V**

5.2.3 Fabricated CSAP operation

During the readout operation, the reset transistor Q_1 is turned off. The drain terminal of the transistor Q_2 is connected through the Row_Bus1 line to the external amplifier circuit. The source terminal of Q_3 is connected to the Row_Bus2 line, the drain terminal of the bias transistor Q_7, and the output of the OTA circuit. The pixel is selected by asserting the column select transistor Q_3. The in-pixel readout transistor Q_2 is in the source-follower configuration during the pixel readout operation, but it is in the common-source amplifier configuration during the pixel reset operation. The current through Q_2 is sensed by the out-of-pixel PMOS transistor Q_4. Since the currents I_{D4} and I_{D2} are equal and the transistor Q_4 is in a linear operating region, the drain voltage of the transistor Q_4 is linearly proportional to the current. This voltage is fed to the inverting input of the amplifier. The transistor Q_6 provides the same bias current as Q_7, which is passed through the PMOS transistor Q_5. The drain voltage of

the transistor Q_5 is supplied to the non-inverting input of the amplifier. Since the transistors Q_4 and Q_5 are identical they will provide equal drain voltages to the input of the amplifier if the equilibrium is established (i.e., if the currents through the transistor Q_2 and Q_6 are identical the negative feedback is in the equilibrium). Since we get $I_{D6} = I_{D7} = I_{D4}$, we obtain balanced currents between the PMOS transistors Q_4 and Q_5 as $I_{D4} = I_{D5}$. Because the transistors Q_4 and Q_5 have the same design parameters, the voltages supplied to the negative and positive terminals of the OTA are identical. These two identical voltages effectively make the currents through the input differential pair M_1 and M_2 equal, where the current is provided by the bias current source M_{11}. Therefore, the negative feedback will effectively force the current through the transistor Q_2 to be equal to the biasing current from Q_7. Transistors M_3, M_4, M_5 and M_6 are designed to have identical minimum size, and transistors M_7, M_8, M_9 and M_{10} are designed to have identical size but 10 times larger than the minimum size transistor. Therefore, the currents through transistors M_5 and M_6 are equal to the current through M_3 because of the current mirror effect with M_3, and the currents through the PMOS transistors M_7 and M_8 as the upper output path are 10 times larger because of the current mirror effect with M_4. We also obtain 10 times larger currents through the NMOS transistors M_9 and M_{10} as the lower output path because of the current mirror effect with M_6. The output current of the OTA can be calculated as $I_{out} = (V_{in+} - V_{in-}) * g_m$ and it equals zero in the equilibrium ($V_{in+} = V_{in-}$). The output current is then fed back to the Row_Bus2 line to provide a negative feedback and ensure a stable current flow of 2 μA through the in-pixel readout transistors Q_2.

The proposed readout operation is in the negative feedback configuration that effectively forces the drain current of the transistor Q_2 to be equal to the biasing current through the transistor Q_5. This feedback configuration results in a faster response time by a factor equal to the current gain of the feedback circuit $A_i = g_m * R_{ON}$, where g_m is the transconductance of the OTA and R_{ON} is the resistance of the transistor Q_4. The feedback circuit is designed to provide a current gain of $A_i = 10$.

The negative feedback operation of the CSAP readout circuit may be described as follows. If the input voltage at the gate of transistor Q_2 increases, the gate-source voltage V_{GS2} increases, and the current through Q_2 also increases. As a result, the current I_{D4} through the transistor Q_4 increases. This increase of the current I_{D4} results in a decrease of the input voltage going into the negative input terminal of the OTA, which in turn increases the output current of the OTA. This increased output current is then fed back to the Row_Bus2 line and charges the parasitic capacitance of the Row_Bus2 line. As a result, the potential of the Row_Bus2 line is increased reducing the gate-source voltage V_{GS2} of Q_2 and reducing the current I_{D2} until it is equal to I_{D5}. At this point the feedback enters the equilibrium and the output OTA current becomes zero. Similarly, if the input voltage at the gate of Q_2 decreases, the output current of the OTA becomes negative and then is fed back to the Row_Bus2 line to discharge the parasitic capacitance. As a result, the potential of the Row_Bus2 line is decreased and reduces the voltage at the source terminal of Q_2, thus giving rise to the gate-source voltage V_{GS2} that subsequently increases I_{D2} to a value that is equal to I_{D5}.

5.2.4 Fabricated CSAP Timing Diagram

The timing diagram of the fabricated CSAP design during the readout operation is shown in Figure 5.3. The input of the reset transistor in the pixel unit is represented by the reset_Pixel signal. Before the photodiode integration, the photodiode is reset for a small period of time by applying a high potential to the reset_Pixel signal. The column selector circuit contains three input signals: reset_CS, D_CS and clk_CS. The column selector circuit operates as a 128-bit shift register and consists of 128 D flip-flops. It controls the column selection transistors Q_3 inside the pixel units such that only one pixel column is selected at a time and multiplexed to the feedback circuit at the end of the rows. The signal reset_CS acts like an active low input to reset all D flip-flop circuits in the shift register after resetting the photodiode. The signal D_CS is the data input to the first D flip-flop and it goes to high potential at the same time as signal reset_CS for a small period of time. The signal clk_CS is the clock signal provided to the shift register with a rising edge clock trigger. The signals column1, column2 to column128 are the output signals from the shift register, which represent the actual column select signals from the first column to the last column. As a result, any pixel can be multiplexed to the feedback circuit at the end of the row. The output voltage of the OTA is then fed back to the Row_Bus2 line and is shown as signals Vout1 to Vout128 in Figure 5.3 with CDS operation (output sampled twice), where the voltage changes exponentially with time during charging and linearly during discharging [4].

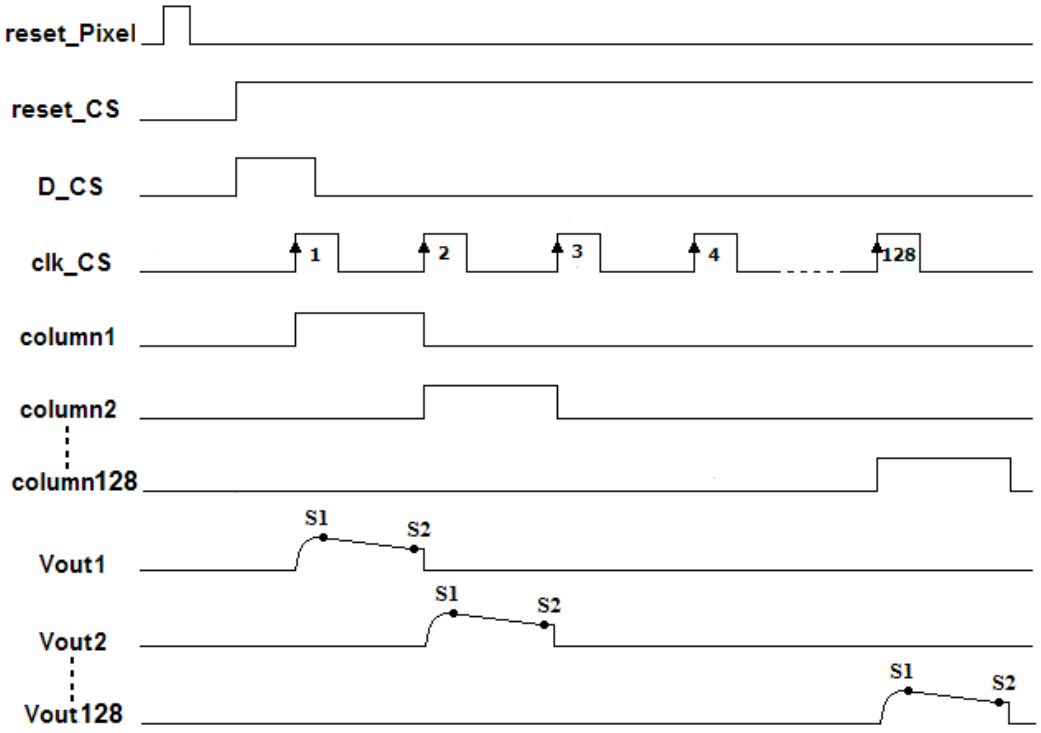

Figure 5.3 Fabricated CSAP Timing diagram during readout operation

5.2.5 Fabricated CSAP Layout and Chip Photograph

Figure 5.4 depicts the entire layout of the proposed CSAP sensor design with bonding pad frame. It includes 3 by 128 pixel units, 128-bit column selector circuit and three readout OTA circuits where each OTA is multiplexed to the pixels of the corresponding row.

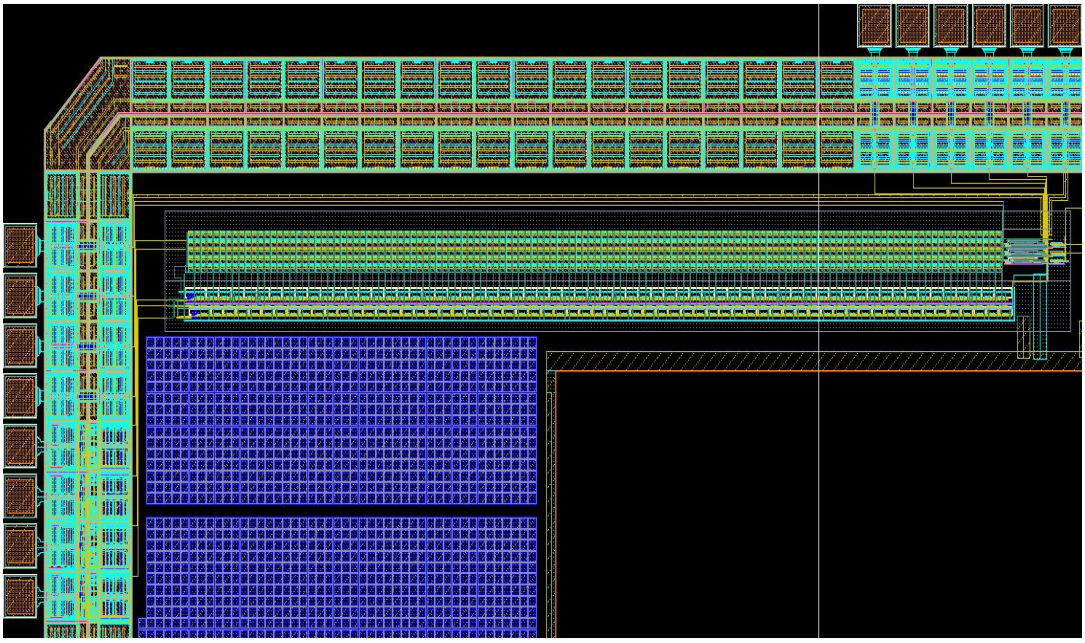

Figure 5.4 Layout of entire CSAP design in TSMC 0.35 µm CMOS technology

Figure 5.5 shows a photograph of the fabricated sensor chip in the 0.35 µm CMOS technology with single poly layer and four metal layers. The entire pixel array is shielded by the forth metal layer to remove light induced transistor currents, which may create a parasitic light contribution at the output signal [40]. By shielding the readout area, we can also avoid additional undesirable noise sources from the outer circuitry, such as noises from row amplifiers and pad frames. The chip measures 3.84 mm × 2.58 mm and is packaged in DIP40.

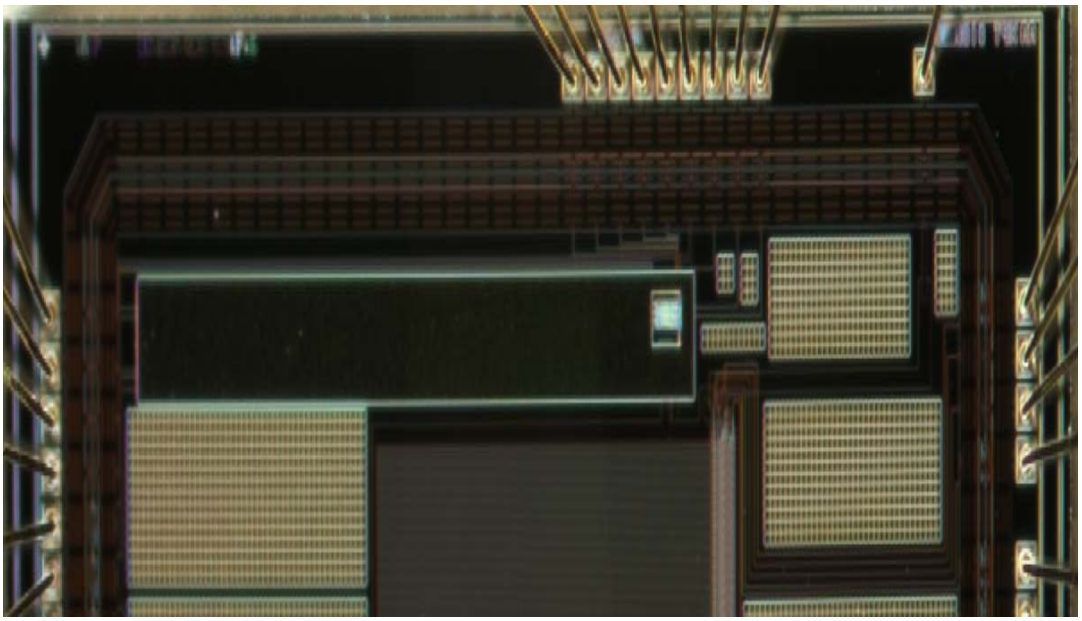

Figure 5.5 Photograph of the fabricated sensor chip.

In order to characterize and test this chip prototype, we implemented the Printed Circuit Board (PCB), and the detail is shown in the next section.

5.3 CSAP Characterization Setup

Both chip level characterization and imaging experiments have been carried out on the fabricated image sensor. A logic analyzer is used to provide digital signals to the image sensor chip. An NI DAQ USB-6221 box is used for data acquisition with a built-in 12-bit analog to digital Converter (ADC) used to convert analog signal to digital for further processing. A custom made LABVIEW program and a MATLAB program were both used to obtain the measured results.

5.3.1 Characterization Setup

The characterization setup is shown in Figure 5.6. In order to characterize the chip prototype and conduct measurements, an experimental platform was designed with the chip and other supporting parts mounted on a Printed Circuit Board (PCB). The power supply supplies VDD and GND to the sensor on the PCB. The optical part of the experimental setup comprises a light source and a digital light meter.

We used a logic analyzer to provide digital signals to the sensor on the PCB. During the reset phase, the logic analyzer inputs a reset signal to reset the pixel array. During this phase, the array is disconnected from the readout amplifiers and the control signals of the column selector circuit are turned off. Then the reset signal is turned off and the array enters the integration phase. The logic analyzer turns on three control signals of the column selector circuit, which enables the shared OTA to serially scan throughout the entire pixel array. After a 50 ms integration time, the pixel values are read out as analog values at the output node.

The analog output of the sensor on the PCB is then connected to the analog input node on the DAQ box. The National Instrument DAQ box with an internal 12-bit ADC is used to convert the analog voltages from its input to the digital numbers, and then output to a PC. An external clock signal from the DAQ box is used to trigger the data acquisition and acquire the correct signal with synchronous time, which is controlled by the logic analyzer. We use LABVIEW on the PC to receive the acquired digital values and then save to a text file to allow further data processing in

MATLAB. An oscilloscope is used to obtain the output waveforms from the sensor on the PCB and then further processed by MATLAB.

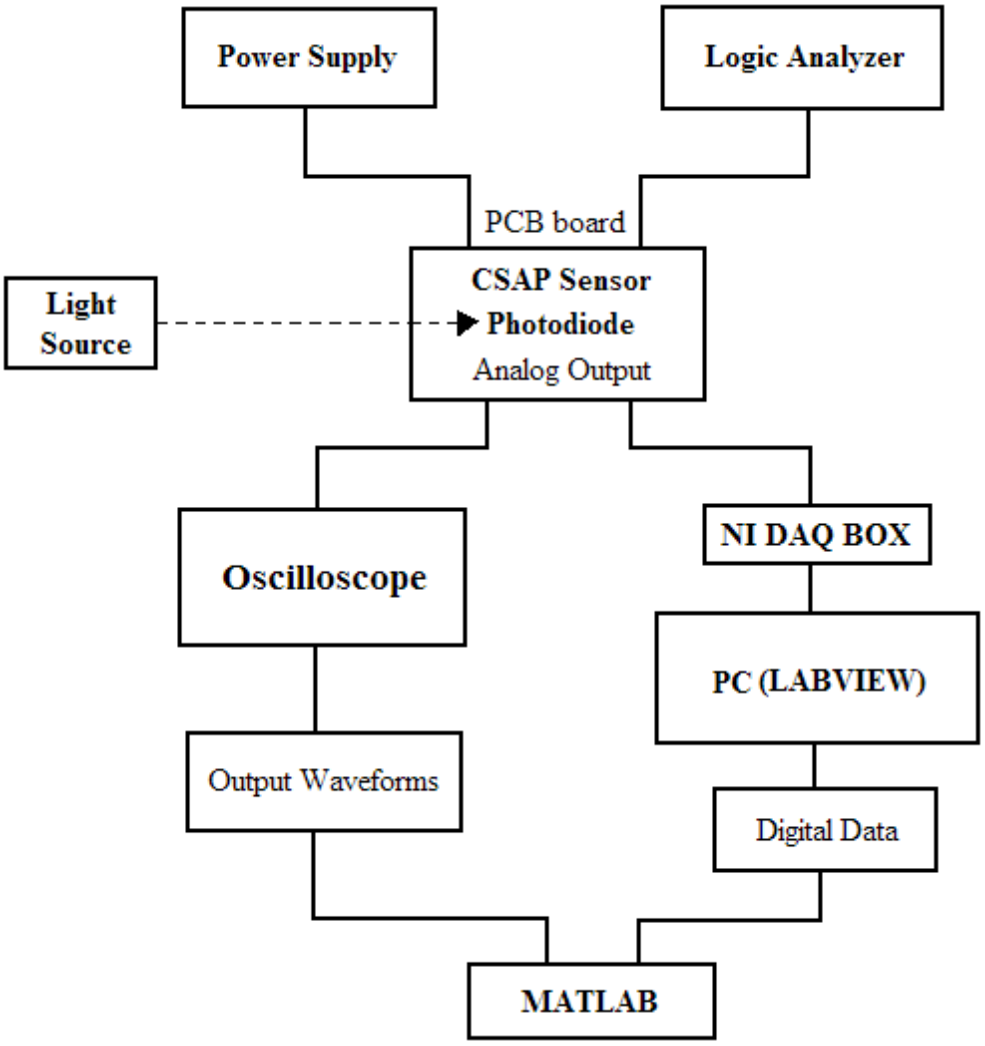

Figure 5.6 CSAP Characterization setup

5.3.2 Characterization Methodology

The external CDS technique is used to characterize the sensor. We read two sets of digital numbers at the same light intensity separated by integration time of 50 ms. Then we subtract these two sets of digital numbers to obtain a single set of digital numbers, which effectively reduces the DC offset and the flicker noise of the CSAP image sensor.

Noise sources in an image sensor can be grouped into two different categories: those that change with time are called “temporal noise” and those that are constant with time but change across the array are called “fixed pattern noise” [41]. Temporal noise is the most important non-ideality in an image sensor. It includes photon shot noise, pixel reset noise, quantization noise and readout related thermal and flicker noise [2]. Two major noise sources to be considered in the CSAP design are the in-pixel source follower transistor and the shared OTA. Noise from the in-pixel source follower amplifier is the primary component of readout noise in a sensor. The higher gain of the shared OTA can attenuate noise generated from the row amplifier and the output buffer circuit. It is demonstrated in [30] that by increasing the gain of the readout amplifier, noise from the amplifier itself is reduced. Therefore, noise from the shared readout OTA can be negligible.

In order to separate the temporal noise from the total noise, 50 frames of the measurements are taken under the same measurement condition. Since the sensor array contains 3 rows and 128 columns, we took the measurements row by row. The

measurement data can be expressed by the notation $P_n(x, y)$, where x is the row number, y is the column number and n represents the number of frames. For example, the mean signal and the random temporal noise, which is the variance for pixel $P_n(1, 1)$ can be calculated as shown in equation 5.1 and 5.2 [42].

$$M(1,1) = \frac{1}{50}\sum_{n=1}^{50} P_n(1,1) \tag{5.1}$$

$$\sigma(1,1) = \sqrt{\frac{1}{50}\sum_{n=1}^{50}(P_n(1,1) - M(1,1))^2} \tag{5.2}$$

The total mean signal and temporal noise are given by equation 5.3 and 5.4 [42].

$$M_{total} = \frac{1}{3\times128}\sum_{x=1}^{3}\sum_{y=1}^{128} M(x,y) \tag{5.3}$$

$$\sigma_{temporal} = \frac{1}{3\times128}\sum_{x=1}^{3}\sum_{y=1}^{128} \sigma(x,y) \tag{5.4}$$

The total fixed pattern noise can then be expressed in equation 5.5.

$$\sigma_{FPN} = \sqrt{\frac{1}{3\times128}\sum_{x=1}^{3}\sum_{y=1}^{128}(M(x,y) - M_{total})^2} \tag{5.5}$$

5.4 CSAP Testing Results

Main parameters of the CSAP image sensor were obtained, including photon transfer curve, conversion gain, dark current, sensitivity, electrical response curve, signal to noise ratio (SNR) and dynamic range (DR) performance. The noise measurements include dark current shot noise, photon shot noise, ADC quantization noise, reset noise, and readout noise.

5.4.1 Mean-Variance Plot

We obtained the mean, variance and standard deviation of the CSAP sensor by applying the corresponding MATLAB functions. A variance versus mean plot is an important parameter to determine whether the sensor is functioning in the desirable manner. The slope of this plot provides the conversion gain of the sensor, and the intercept point provides the temporal readout noise [41]. Figure 5.7 shows the variance versus mean plot of the CSAP sensor prototype. We can clearly see that the variance of the sensor increases linearly with the mean. The slope is measured to be 1.88 μV, indicating that the conversion gain is 1.88 μV/electrons. The intercept is measured to be 0.9 $(mV)^2$, indicating that the readout noise (noise floor) is 95 μV or 50 electrons (dividing the measured readout noise of 950 μV from the intercept by the OTA current gain of 10), which includes dark current shot noise, reset noise, quantization noise, and transistor thermal and flicker noise.

The error bar of the sample data point is shown in the small box. The error w in the x-axis direction is determined by $V_{LSB}/2$ and the error h in the y-axis direction is determined by $V^2_{LSB}/12$, where the V_{LSB} is the voltage corresponding to 1 LSB of the 12-bit ADC in the DAQ box and is calculated to be 0.5 mV.

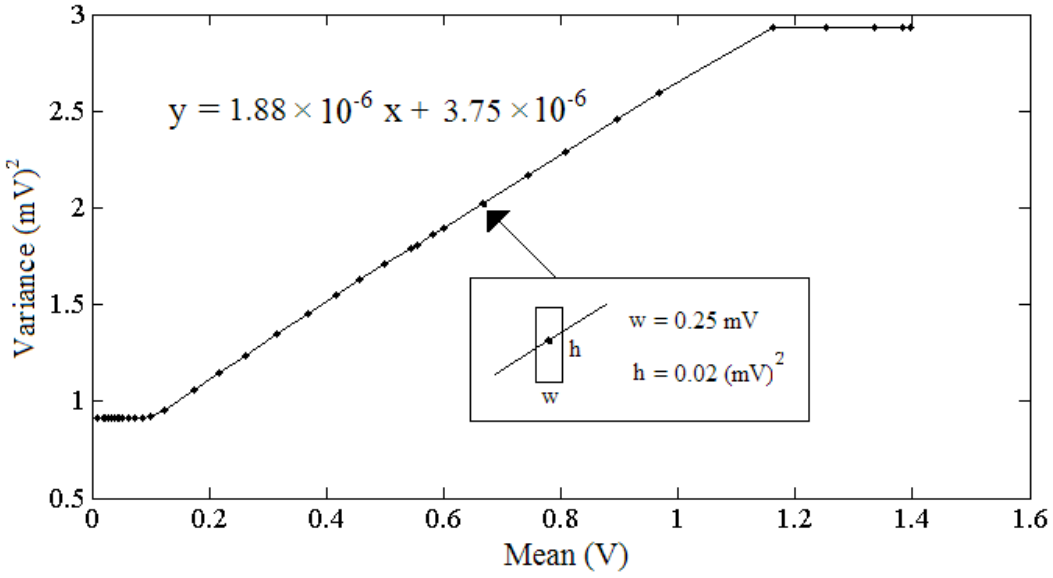

Figure 5.7 Mean-variance plot with linear increase in sensor noise

Now, we are able to estimate the parasitic capacitance of the integration node including the junction capacitance of the photodiode, gate capacitance of the source follower transistor Q_2, capacitance of the source diffusion of the reset transistor Q_1, and metal interconnect capacitances. The capacitance of the integration node is in an inverse relation with conversion gain as shown in equation 5.6.

$$C_{pd} = \frac{q}{\text{conversion gain}} = 85\ fF \tag{5.6}$$

5.4.2 Dark current

The dark current measurement result is shown in Figure 5.7. It is obtained by sweeping the integration time from 1 ms to 250 ms, while the sensor array is completely shielded from the external light [43]. The integrated dark signal is measured to be 300 mV/s, which corresponds to a dark current of 25.5 fA since the capacitance of the integration node C_{pd} is calculated as 85 fF. The error bar indicates that the output voltage is measured with a 5mV fluctuation.

Dark current components depend on doping concentration, band gap and temperature of the reverse-biased diode. The work in [44] indicates that dark current shot noise increases severely with higher temperature.

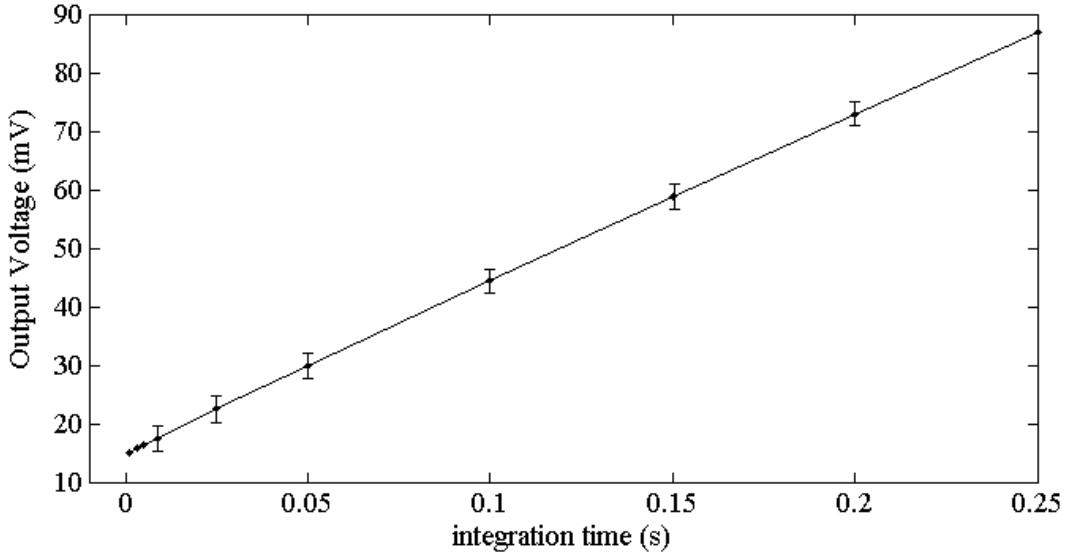

Figure 5.8 Dark current measurement result

The dark current shot noise is calculated to be 17 μV_{rms}. The ADC quantization noise comes from the external NI-DAQ box and is measured to be 15 μV or 8 electrons. We employed the "hard reset" method to the reset transistor Q_1 in the pixel design, and the reset noise was calculated as 22 μV_{rms} or 12 electrons from the following equation [25].

$$N_{rms}^{reset} = \sqrt{\frac{kT}{C_{pd}}} \tag{5.7}$$

5.4.3 Electrical Response Curve

Figure 5.9 shows the measured electrical response curve. The integration time is chosen to be 50 ms to target the frame rate of 20 Hz. It shows the linear fitting characteristic of the output voltage with uniform light intensity swept from 1 lm/m^2 to 340 lm/m^2 for the corresponding output range of 1.4 V. The slope of the response curve is measured to be 4.5 mV/(lm/m^2). For an integration time of 50 ms, this corresponds to 90 μV/((lm/m^2)·ms).

The error bar of the sample data point is shown in the small box. The output voltage error in the y-axis direction is determined by $V_{LSB}/2$, which is equal to 0.25 mV and is applied to every data point in this figure.

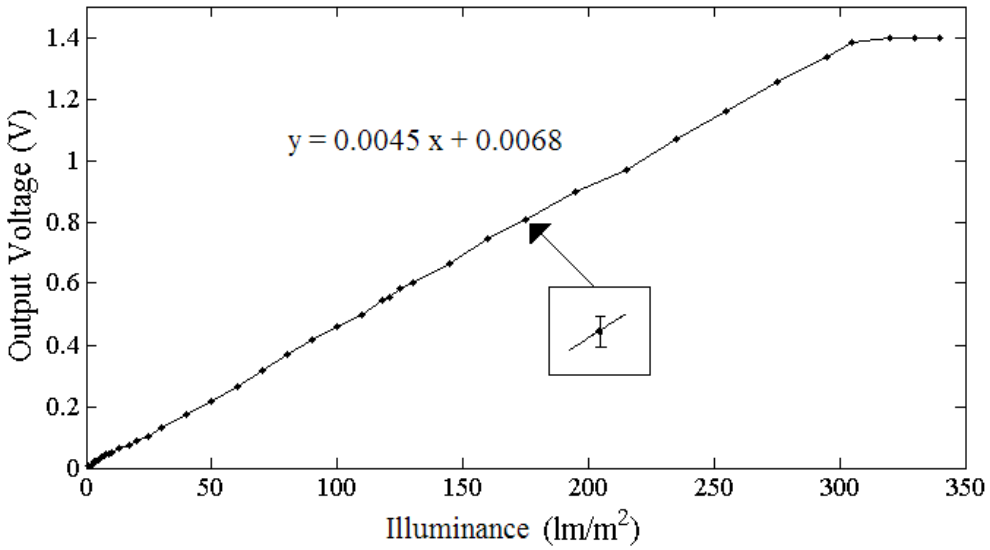

Figure 5.9 Output voltage of the pixel as a function of input light level for a 50 ms integration time

5.4.4 Signal to Noise Ratio (SNR)

Signal to noise ratio (SNR) is defined as the ratio of the signal power to the total noise power [39]. The noise power at the end of the integration can be expressed as the sum of three independent components: readout noise, photon shot noise and gain related FPN. Figure 5.10 shows the SNR plot of the CSAP design for the range of photocurrents from 15 fA to 12 pA.

We can see that there are three distinct regions in the SNR plot. It exhibits 20 dB per decade slope in the region where the read noise is dominant. Then, as the photocurrent increases, photon shot noise becomes the dominant noise source with 10 dB per decade. However, at high signal levels the curve is nearly flat, which indicates

the dominant noise source is fixed pattern noise (FPN) caused by the spatial variations from the transistors and the amplifiers both inside the pixels and at the end of the rows. We noticed that the SNR improves with higher illumination levels, as well as increased integration time.

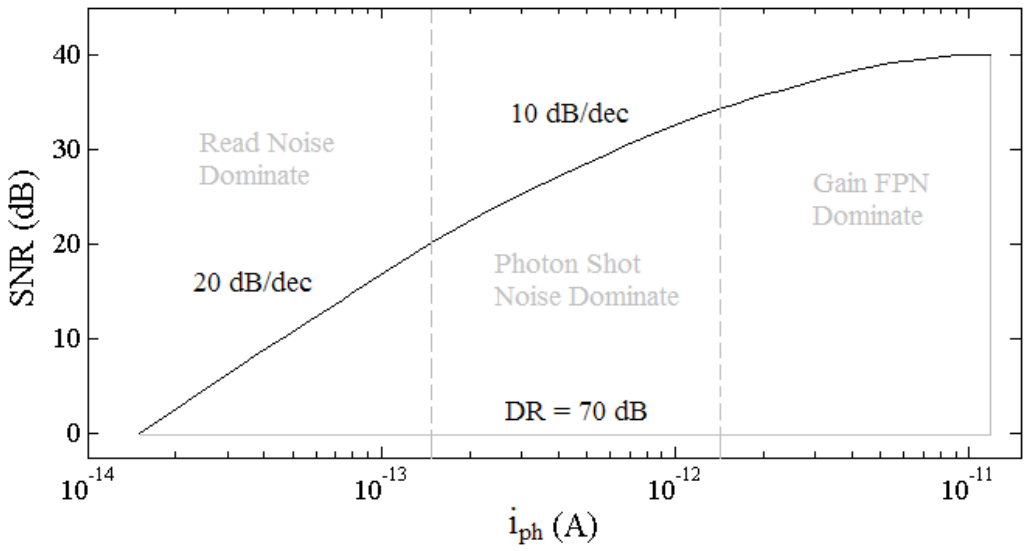

Figure 5.10 Signal to noise ratio measurement of the sensor

5.4.5 Dynamic Range (DR)

DR performance is defined by equation 5.8, which is the ratio of the largest signal to the smallest simultaneously detectable signal (or noise floor) [2].

$$DR = 20log_{10}\frac{max}{min} = 20log_{10}\frac{MAX_{DN}}{\sigma_{DS}} \quad (5.8)$$

It can be expressed as the ratio of MAX_{DN} to σ_{DS} in our measurements, where MAX_{DN} is the maximum non-saturating signal in digital number. The maximum non-saturating signal includes the dark current, which has to be subtracted from the maximum detectable signal. σ_{DS} is the smallest detectable random (readout) noise, which is measured in the dark condition. So the *DR* of the CSAP sensor is calculated to be 70 dB. We are targeting the frame rate at 20 frames/s, so the minimum read-out frequency is 20 Hz, which sets the lower bound of the dynamic range to a fixed value. If we increase the frame rate to a higher value, the minimum detectable signal will also increase, which reduces the dynamic range at the lower end of the illumination range and in turn reduces the overall dynamic range.

5.4.6 Readout Speed

The faster readout of an image sensor can result in a higher frame rate for large pixel arrays and a faster electronic shutter. In addition, increasing the readout speed reduces readout noise by decreasing the interval between the successive measurements in the CDS method.

We measured the readout speed of the CSAP design and the standard APS design during the readout operations of both image sensors. The comparisons of the readout time during charging and discharging of the imagers are shown in Figure 5.11 and 5.12, respectively.

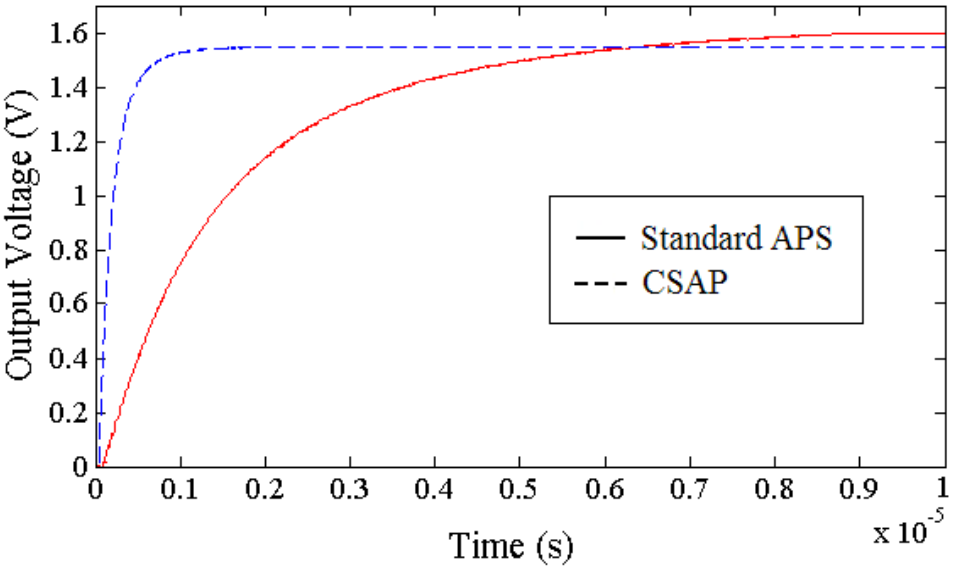

Figure 5.11 Comparison of measured readout speeds during charging between standard APS and CSAP design

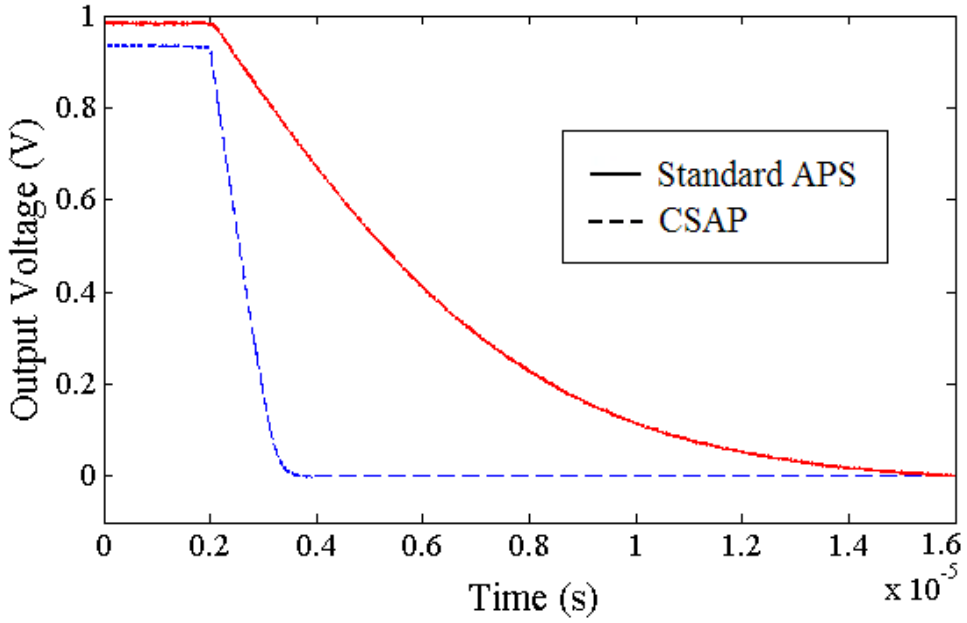

Figure 5.12 Comparison of measured readout speeds during discharging between standard APS and CSAP design

The charging time T_c of the CSAP design is measured to be 1 μs, as compared to 8 μs of the standard APS design. The discharging time T_d of the CSAP design is measured to be 1.5 μs, as compared to 12 μs of the standard APS design. Therefore, we demonstrate that the CSAP design has a nearly 8-fold speed improvement both during charging phase and discharging phase.

The speed measurements of the chip prototype are consistent with the simulation results in Chapter 3. However the charging and discharging times of both CSAP design and standard APS design of the chip prototype are slower than the simulation results, which is due to the additional capacitive loads of the PAD frame. The faster readout of an image sensor can result in a higher frame rate for large pixel arrays and faster electronic shutter. In addition, increasing readout speed reduces readout noise by decreasing the interval between the successive measurements in the CDS method.

5.4.7 1/f Noise Reduction

In order to demonstrate the 1/f noise power reduction in the CSAP design, we have to demonstrate that the total output noise is decreased when the time interval between the two consecutive samples of the CDS is shortened. Figure 5.13 shows the total noise comparison of the CSAP design and the standard APS design as we sweep the time interval between the two consecutive samples in the CDS from 1 μs to 1 ms. For a given time interval between the two CDS samples, the CSAP design exhibits a slightly higher total noise power than the APS design because of its larger bandwidth.

The total noise power of both designs is decreasing in the same trend as the time interval between the two CDS samples is shortened. However, when the time interval drops down to 40 μs, further decrease of the noise power in the APS design cannot be accomplished because it becomes limited by the settling time of the APS design. In contrast, the total noise power of the CSAP design can still be decreased after the 40 μs time interval since the CSAP can handle faster settling times. These measurements demonstrate the CSAP design's ability to reduce readout noise to levels that are 4 times lower than in the APS design and these measured noise levels are dominated by the 1/f noise of the in-pixel source follower transistor. Therefore, we demonstrate that with the faster settling time provided by the CSAP design, the time interval between the two CDS samples has decreased, so that more 1/f noise can be reduced.

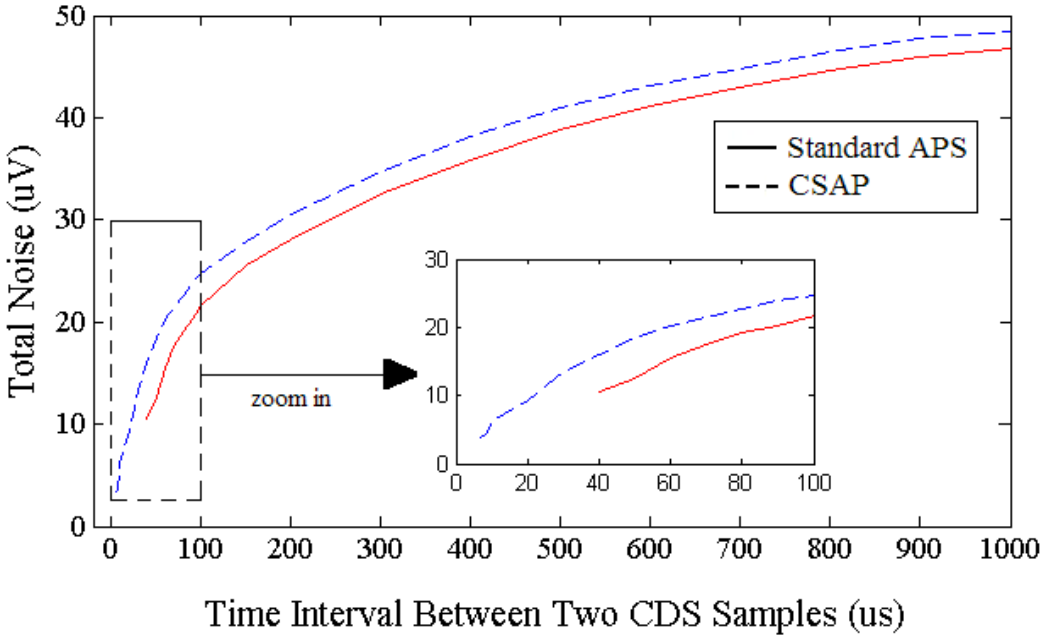

Figure 5.13 Comparison of the total noises of the CSAP design and APS design when applying CDS with different time intervals between two conservative samples

Figure 5.14 shows the noise spectrum comparison of the standard APS design and our developed CSAP design during the dark illumination condition. The noise spectrum of both designs shows a 10 dB/decade decreasing rate. Overall, for a given time interval between the two CDS samples, the CSAP design demonstrates more 1/f noise than the standard APS design and similar thermal noise levels.

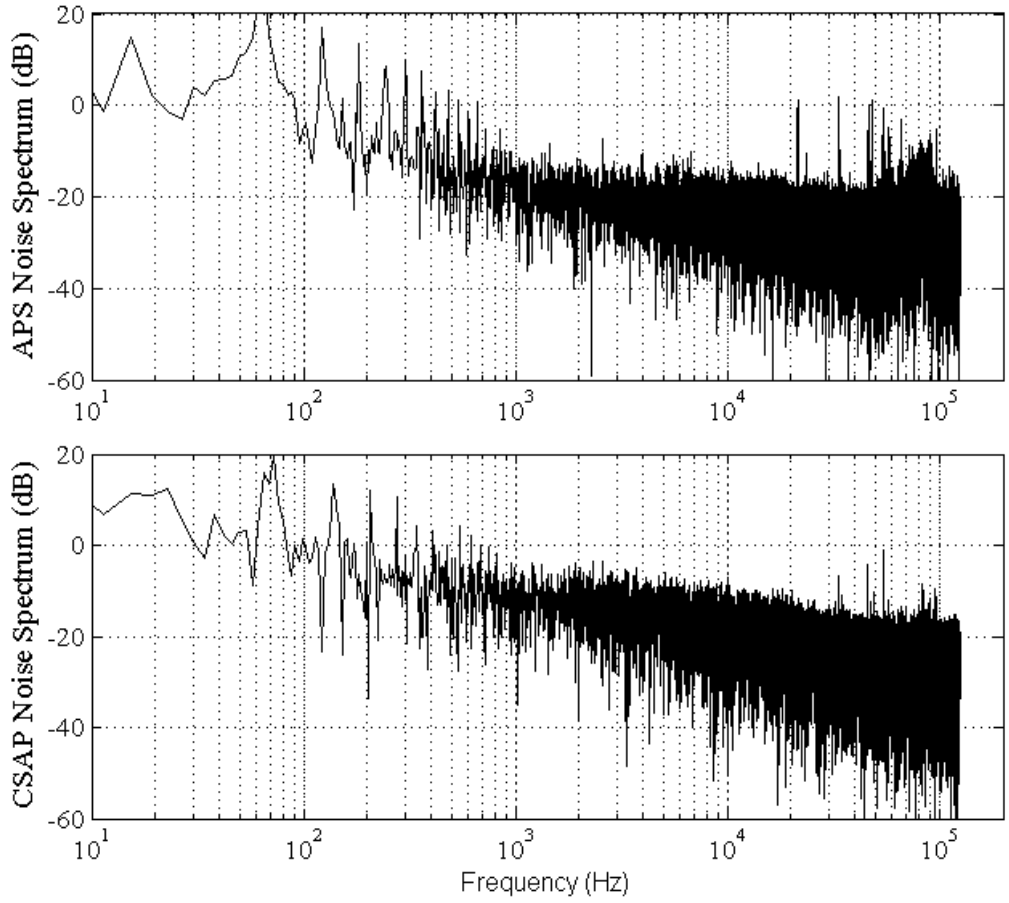

Figure 5.14 Noise spectrum comparison between the standard APS design and the proposed CSAP design in the frequency range of 250 KHz

Table 5.2 summarizes the measured performance of the CSAP sensor. The pixel fill factor is 42.6%. The sensitivity is measured to be 0.25 V/lux•s; however, this value shows that our pixel is not as sensitive as the typical 0.35μm CMOS image sensor in [22] with a sensitivity of 1.1 V/lux•s.

Table 5.2 Measured CSAP Sensor Performance Summary

Technology	0.35μm 4M 1P CMOS
Power supply	3.3 V
Chip size	3.84mm × 2.58mm
Pixel array	128 × 3
Pixel size	15μm × 15μm
Photo element	N diff/P sub Photodiode
Photodiode area	95.84 μm^2
Fill factor	42.6%
Conversion gain	1.88 μV/e-
Sensitivity	0.25 V/lux•s
Dark current	27 nA/ cm^2
Readout noise	95 μV

Dark current shot noise	17 μV
Reset noise	22 μV
Transistor thermal and flicker noise	90 μV
Dynamic range	70 dB
Frame rate	20 fps
OTA power consumption	85 μW
Total Power consumption	132 μW

5.5 Summary

The fabricated chip has been successfully implemented using 0.35 μm CMOS technology with standard photodiode. The chip has been tested and it has been demonstrated that the readout speed can be nearly an order of magnitude faster than the standard APS design, thus more 1/f noise can be reduced as we decrease the time interval between the two CDS samples. We achieved a measured dynamic range of 70 dB by applying a readout amplifier with a current gain of 10 in the negative feedback path of the pixel unit.

Chapter 6

Conclusions

6.1 Conclusions

In this work, we developed two different analog readout methods for a CMOS image sensor. One is the current sensing active pixel (CSAP) sensor and another is the reconfigurable active pixel sensor (RAPS). We provided detailed descriptions and circuit simulations for both designs and tested the fabricated CSAP chip by validating its noise performance and readout improvement as compared to the standard active pixel sensor (APS) design. The CSAP design is built using the standard 0.35 μm CMOS process with 1 poly and 4 metal layers. The design operates from a 3.3 V power supply.

The CSAP image sensor is an analog CMOS image sensor readout architecture designed to have faster settling time and readout speed than the standard APS design. In our design, we employ the standard source follower amplifier configuration in the pixel part of the CSAP design to obtain a high fill factor. Negative feedback is applied to the readout of the pixel unit from a row-shared operational transconductance amplifier to increase its current driving capabilities. This reduces

the settling time between the two conservative samples in the Correlated Double Sampling (CDS) circuit. As a result, the low frequency cut-off point is increased, which attenuates the pixel's 1/f noise contributed by the in-pixel source follower transistor. Typically, the performance of the CDS circuits in standard APS designs degrades as the technology scales down, due to increased parasitic capacitances of the readout lines and correspondingly longer settling time [2]. However, the settling time of the CSAP architecture can be significantly shortened, so that the CDS circuit may continue to benefit the CSAP design in more advanced technologies. Simulations and fabricated chip test results of the CSAP design indicate that the readout speed is almost an order of magnitude faster than the standard APS design. The CSAP design also increases the effectiveness of the active reset amplifier by increasing its unity-gain bandwidth.

The RAPS imager is another analog CMOS image sensor readout architecture that is designed to operate without the need for external CDS circuits used in standard APS designs. The pixel transistor count of the RAPS design is equal to the standard APS design, thereby retaining a high fill factor. Our design employs a reconfigurable differential input readout amplifier, which is used in both the reset and readout phases of the image sensor operation. Therefore, the CDS operation can be implemented without using external capacitive elements, which saves silicon area power and makes image sensor designs more compact. Thus, in our design, the DC offset is removed, flicker noise is differentiated, and reset noise is greatly reduced by employing the amplifier in an active reset configuration. Our differential input amplifier allows a

higher open-loop gain and unity-gain bandwidth over the conventional source follower readout amplifier in the APS design. These performance improvements reduce gain related Fixed Pattern Noise. Furthermore, the settling time is decreased by a factor of four, proven through simulations of the RAPS design with a balanced OTA. Finally, the effective gain error reduction has been verified through Cadence simulations.

6.2 Future Work

After the successful testing and performance characterization of the CSAP prototype sensor implemented as a 3 by 128 pixel array, we plan to fabricate larger arrays such as 256 by 128, or even larger, to fully exploit the speed improvement benefits of the CSAP design. The CSAP design proves to be more valuable for larger arrays with increased numbers of pixels and longer readout lines where faster readout speeds are crucial for capturing quality images.

We are also looking forward to working on the layout design and fabrication of the RAPS readout circuit. The testing and characterization procedure is important to verify the idea and architecture of the design. Finally, we plan to compare the imaging performances of the CSAP design and the RAPS design, such as silicon area and fabrication costs, noise, speed, and power consumption.

Publications by the Author

1. Z. Ignjatovic, Y. Zhang and M. Bocko, “CMOS image sensor readout employing in-pixel transistor current sensing,” in *Proc. IEEE ISCAS*, May. 2008.

2. Y. Zhang and Z. Ignjatovic, “Reconfigurable CMOS image sensor design with built-In correlated double sampling,” *in Proc. IEEE ISCAS*, May. 2009.

3. Y. Zhang, Z. Ignjatovic, D. Maricic and M. Bocko, “Low noise CMOS image sensor employing current sensing readout amplifier,” prepare to submit to IEEE Sensor Journal 2011

Bibliography

[1] E. Fossum, "CMOS Image Sensor: electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, Vol. 44, no. 10, pp.1689-1698, Oct. 1997.

[2] A. El Gamal and H. Eltoukhy, "CMOS image sensors," *IEEE Circuits Devices Mag*., vol.21, no.3, pp. 6-20, 2005.

[3] E. Fossum, "Active pixel sensors: Are CCD's dinosaurs?," *in Proc. SPIE, Charged-Coupled Devices and Solid State Optical Sensors III,* vol. 1900, 1993, pp, 30-39.

[4] K. Salama and A. El. Gamal, "Analysis of active pixel sensor readout circuit," *IEEE Trans. Circuits and Systems-I: fundamental theory and applications*, vol.50, no.7, pp. 941-944, July. 2003.

[5] T. Nobusada, M. Azuma, H. Toyoda, T. Kuroda, K. Horii, T. Otsuki and G. Kano, "Frame interline transfer CCD sensor for HDTV camera," *in Proc. IEEE ISSCC,* 1989.

[6] Z. Ignjatovic, Y. Zhang and M. Bocko, "CMOS image sensor readout employing in-pixel transistor current sensing," in *Proc. IEEE ISCAS*, May. 2008.

[7] K. Findlater, et al., "SXGA pinned photodiode CMOS image sensor in 0.35um technology," *in Proc. IEEE ISSCC,* 2003.

[8] Y. Jungwook, et al., "A 3Mpixel low-noise flexible architecture CMOS image sensor," *in Proc. IEEE ISSCC,* 2006.

[9] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley and Sons, 1981.

[10] X. Liu and A. El Gamal, "Photocurrent estimation for a self-reset CMOS image sensor," *in Proc. SPIE, Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications III*, vol. 4669, 2002, pp, 304-312.

[11] B. Fowler, D. Yang, H. Min and A. El Gamal, "Single pixel test structures for characterization and comparative analysis of CMOS image sensors," At *1997 IEEE Workshop on Charge Coupled Devices*, Brugge, Belgium, June 1997.

[12] A. Dickinson, B. Ackland, E. Eid, D. Inglis and E. Fossum, "Standard CMOS active pixel image sensors for multimedia applications," *in Proc. IEEE Advanced Research in VLSI*, 1995.

[13] S. Mendis, S. Kemeny, R. Gee, B. Pain and E. Fossum, "Progress in CMOS active pixel image sensors," *in Proc. SPIE, Charged-Coupled Devices and Solid State Optical Sensors IV,* vol. 2172, pp. 19-29, 1994.

[14] F. Chu, R.M. Guidash, J. Compton, S. Coppola and W, Hintz, "Improving low-light CMOS performance with four-transistor four-shared pixel architecture and charge-domain binning", *Proc. of SPIE-IS$T Electronic imaging, SPIE Vol. 6069*

[15] J.J. Zarnowski, M. Pace and M. Joyner, "1.5 FET-per-pixel standard CMOS active column sensor," *Proceedings of SPIE*, vol.3649-27, Jan. 1999.

[16] T. Das and P. R. Mukund, "A low noise current-mode readout circuit for CMOS image sensor applications," in *Proc. IEEE 17th International Conference on VLSI Design*, pp. 653-658, 2004.

[17] D. Maricic, Z. Ignjatovic and M. Bocko, "An oversampling digital pixel sensor with a charge transfer DAC employing parasitic capacitances," in *Proc. IEEE MWSCAS*, pp. 415-418, 2009.

[18] Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuits, 5th Edition, Oxford University Press, 2004.

[19] David A. John and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997.

[20] Henry Stark and John W. Woods, Probability and Random Processes with Applications to Signal Processing, 3rd Edition, Prentice-Hall, 2001.

[21] Thomas H. Lee, The design of CMOS Radio-Frequency Integrated Circuits, 2nd Edition, Cambridge University Press, 1998.

[22] O. Yadid-Pecht and R. Etienne- Cummings, CMOS Imagers: From Phototransduction to Image Processing. Boston: Kluwer Academic Publishers, 2004.

[23] Paul R.Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th Edition, John Wiley & Sons, 2001.

[24] Behzad Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.

[25] H. Tian, B. Fowler, and A. El Gamal, "Analysis of Temporal Noise in CMOS Photodiode Active Pixel Sensor," IEEE, J. Solid State Circuits, vol.36, no. 1, pp.92-101, January 2001.

[26] X. Wang, P. R. Rao, A Mierop, A. J. P. Theuwisssen, "Random Telegraph Signal in CMOS Image Sensor Pixels," International Electron Device Meeting (IEDM'06), pp. 1 – 4, Dec. 2006.

[27] C. Leyris; F. Martinez; M. Valenza; A. Hoffmann; J.C. Vildeuil; F. Roy, "Impact of Random Telegraph Signal in CMOS Image Sensors for Low-Light Levels," Solid-State Circuits Conference, pp. 376 – 379, Sept. 2006.

[28] http://en.wikipedia.org/wiki/Burst_noise

[29] Hewlett-Packard Components Group, "Noise Sources in CMOS Image Sensors", available: http://www.stw.tu-ilmenau.de/~ff/beruf_cc/cmos/cmos_noise.pdf

[30] M. Sakakibara, S. Kawahito, D. Handoko, N. Nakamura, H, Satoch, M. Higashi, K. Mabuchi and H. Sumi, "A high-sensitivity CMOS image sensor with gain-adaptive column amplifiers," IEEE J. Solid-State Circuits, Vol. 40, no.5, pp. 1147-1156, May. 2005.

[31] E. Sanchez Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," in Proc. IEE Circuits Devices and Systems, vol.147, no.1, pp. 3-12, Feb. 2000.

[32] Alan Hastings, The Art of Analog Layout, 1st Edition, Prentice-Hall, 2001.

[33] D. Yang, B. Fowler and A. El. Gamal, "A nyquist rate pixel level ADC for CMOS image sensors ," in Proc. IEEE Custom Integrated Circuits Conference, pp. 237–240, May. 1998.

[34] T. Lule, S. Benthien, H. Keller, F. Mutze, P. Rieve, K. Seibel, M. Sommer and M. Bohm, "Sensitivity of CMOS based imagers and scaling perspectives," IEEE Trans. Electron Devices, Vol. 47, no.11, pp. 2110-2122, November. 2000.

[35] Y. Zhang and Z. Ignjatovic, "Reconfigurable CMOS image sensor design with built-In correlated double sampling," in Proc. IEEE ISCAS, May. 2009.

[36] Z. Yang, V. Gruev, and J. Van der Spiegel, "A CMOS linear voltage/current dual-mode imager," in Proc. IEEE ISCAS, May. 2006.

[37] K. Lee and E. Yoon, "A CMOS image sensor with reset level control using dynamic reset current source for noise suppression," in ISSCC Dig. Tech. Papers, Feb. 2004, pp 114-516.

[38] J.M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice-Hall, 2003.

[39] David A. John and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997.

[40] C. Shoushun, F. Boussaid and A. Bermak, "Robust intermediate read- out for deep submicron technology CMOS image sensors", IEEE Sensor Journal, vol. 8, no.3, pp. 286-294, March. 2008.

[41] S. Bohndiek, A. Blue, A. Clark, M. Prydderch, R. Turchetta, G. Royle and R. Speller, "Comparison of methods for estimating the conversion gain of CMOS active pixel sensors", IEEE Sensor Journal, vol. 8, no.10, pp. 1734-1744, Oct. 2008.

[42] Sheldon Ross, A First Course in Probability, 6th Edition, Prentice-Hall, 2001.

[43] J. Guo and S. Sonkusale, "A high dynamic range CMOS image sensor for scientific imaging applications", IEEE Sensor Journal, vol. 9, no.10, pp. 1209-1218, Oct. 2009.

[44] I. Shcherback, A. Belenky, O. Yadid-Pecht, "Empirical Dark Current Modeling for CMOS Active Pixel Sensors (APS)," Optical Engineering, Special issue on Focal Plane Arrays, Vol. 41, No. 6, pp. 1216-1219, June 2002.