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Connectors
Connectors.SchDoc

MCU
MCUtop.SchDoc

LEDs
LED.SchDoc

UART-USB
UART_connect.SchDoc

FPGA
XC7A35TFTG256.SchDoc

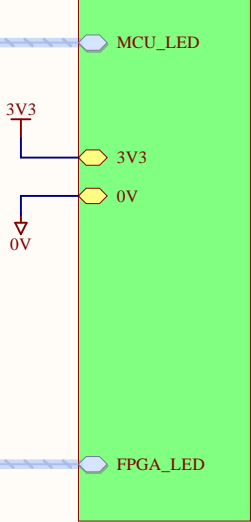
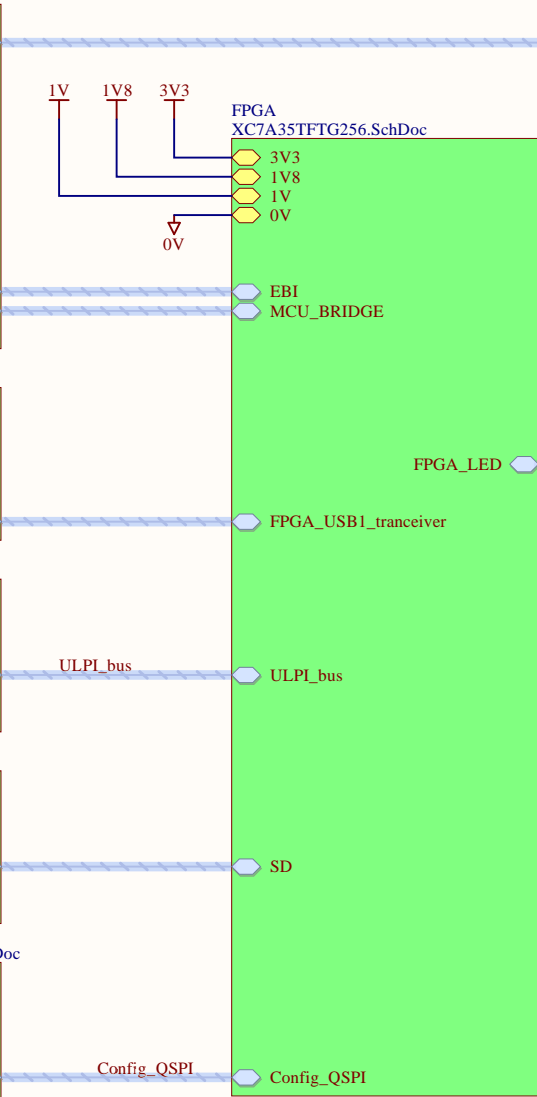
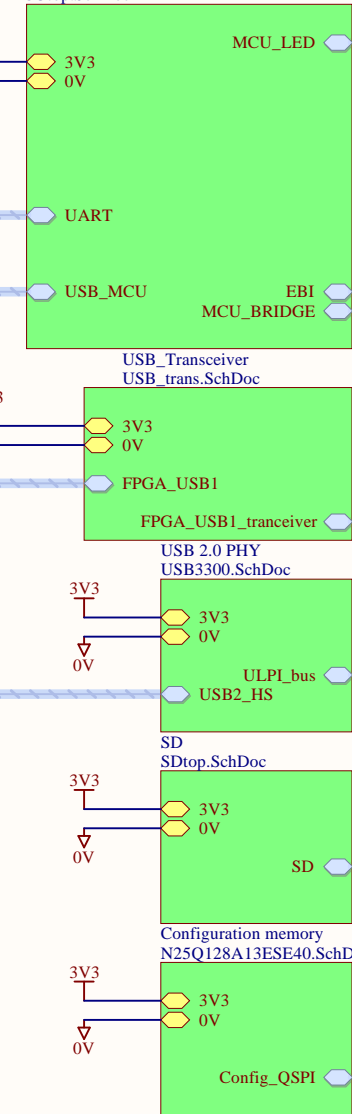
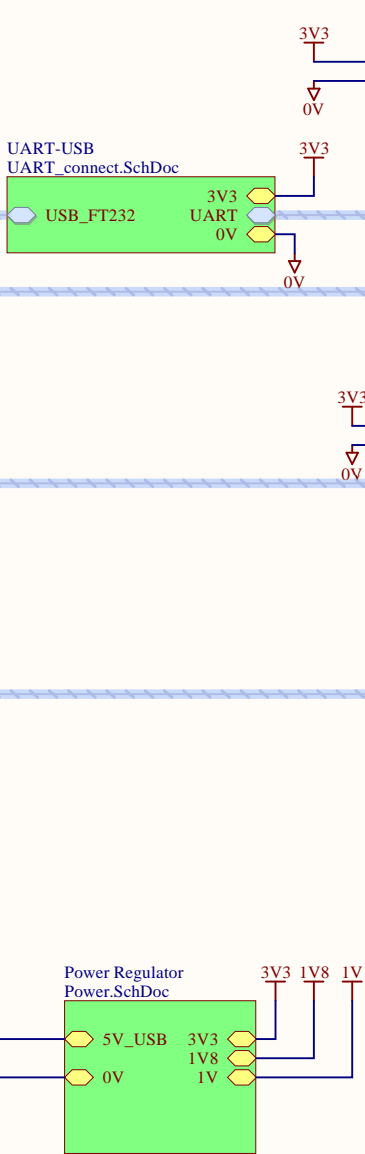
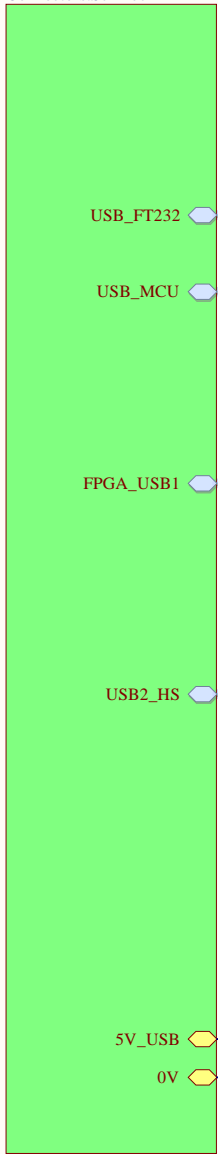
USB_Transceiver
USB_trans.SchDoc

USB 2.0 PHY
USB3300.SchDoc

SD
SDtop.SchDoc

Configuration memory
N25Q128A13ESE40.SchDoc

Power Regulator
Power.SchDoc



Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Top level	Sheet	1 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	main.SchDoc		



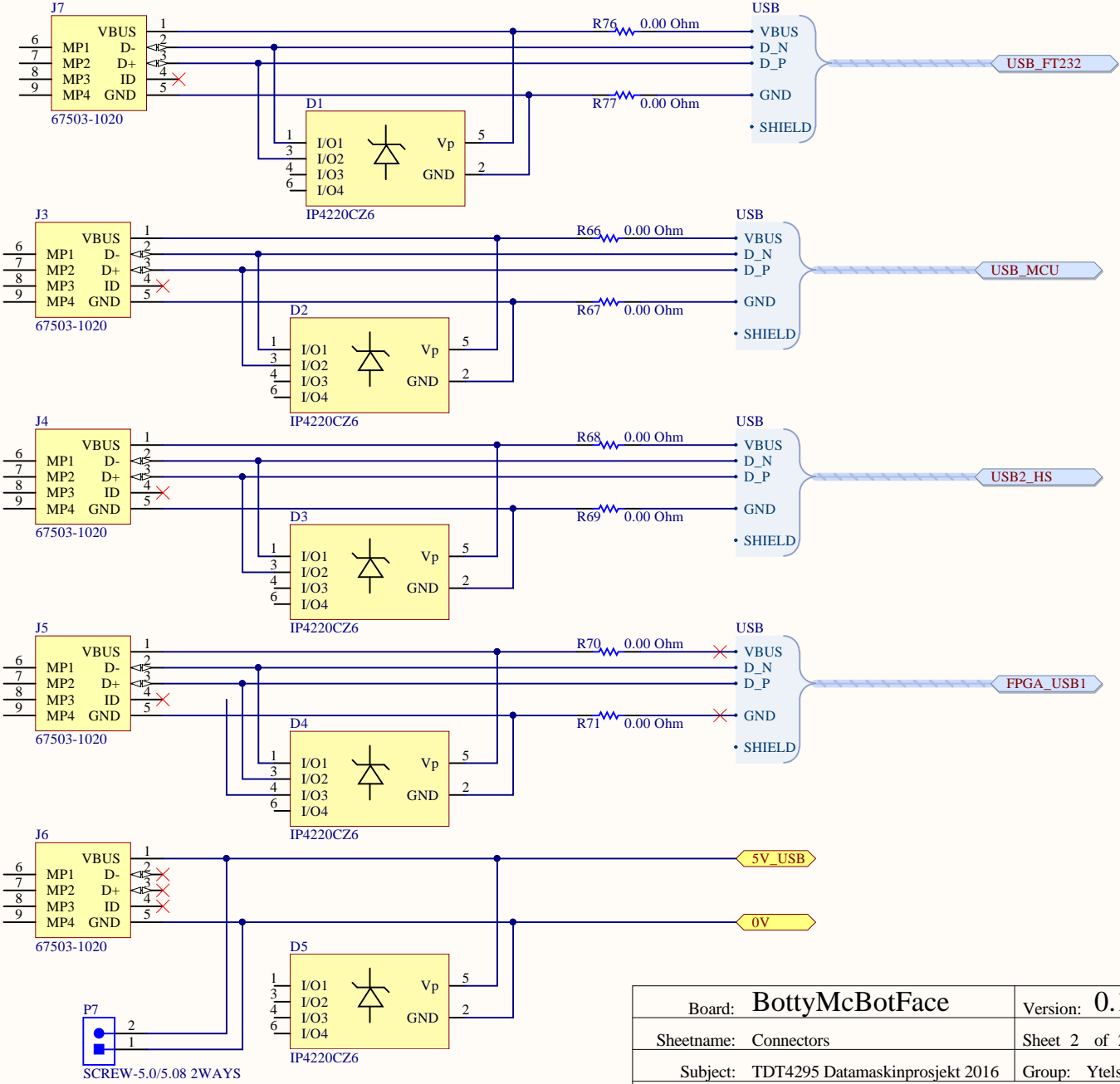
Do not connect to 0V, grounding only on host side

Do not connect to 0V, grounding only on host side

Do not connect to 0V, grounding only on host side

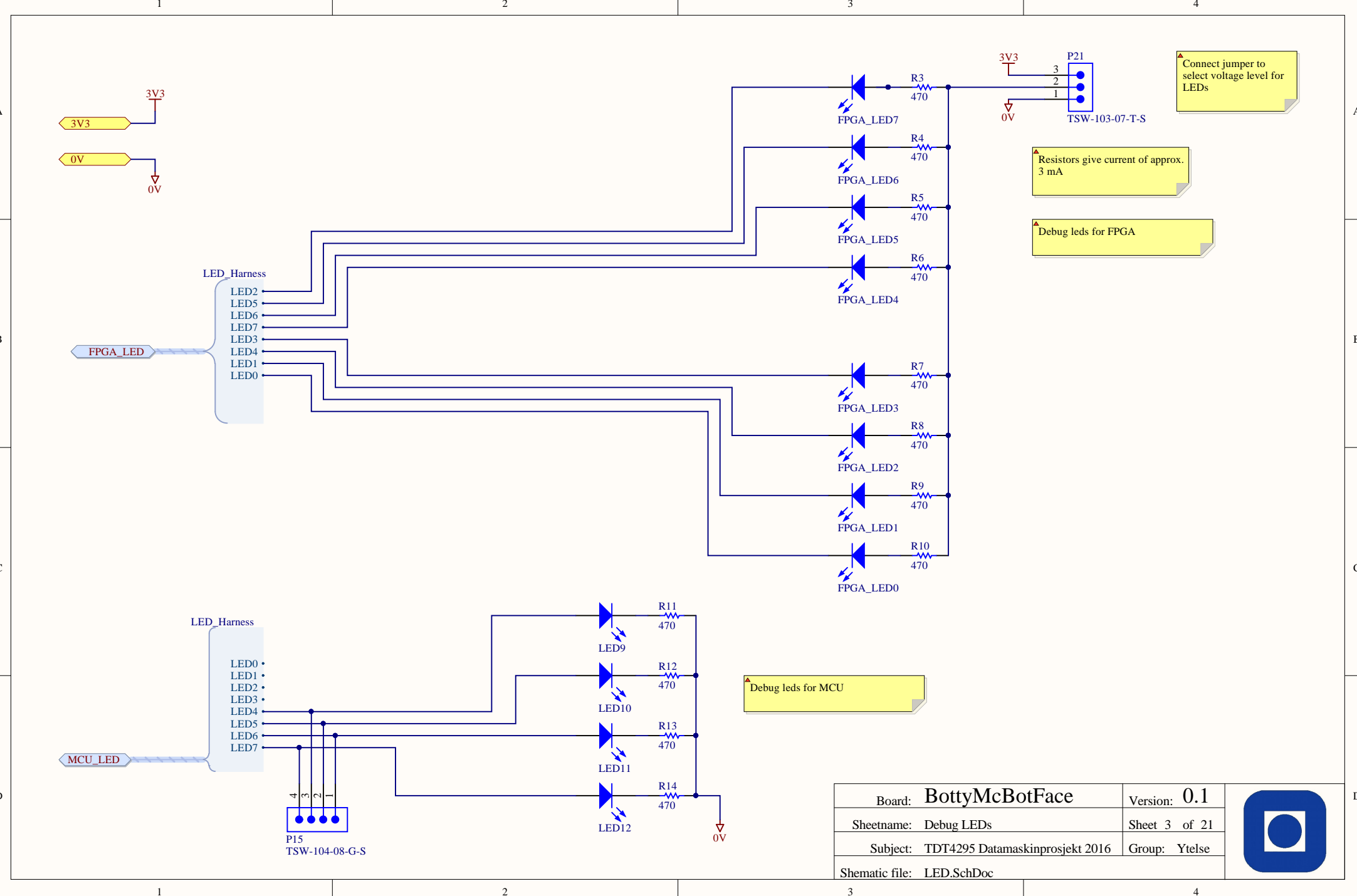
Do not connect to 0V, grounding only on host side

Do not connect to 0V, grounding only on host side



Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Connectors	Sheet	2 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	Connectors.SchDoc		





Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Debug LEDs	Sheet	3 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	LED.SchDoc		



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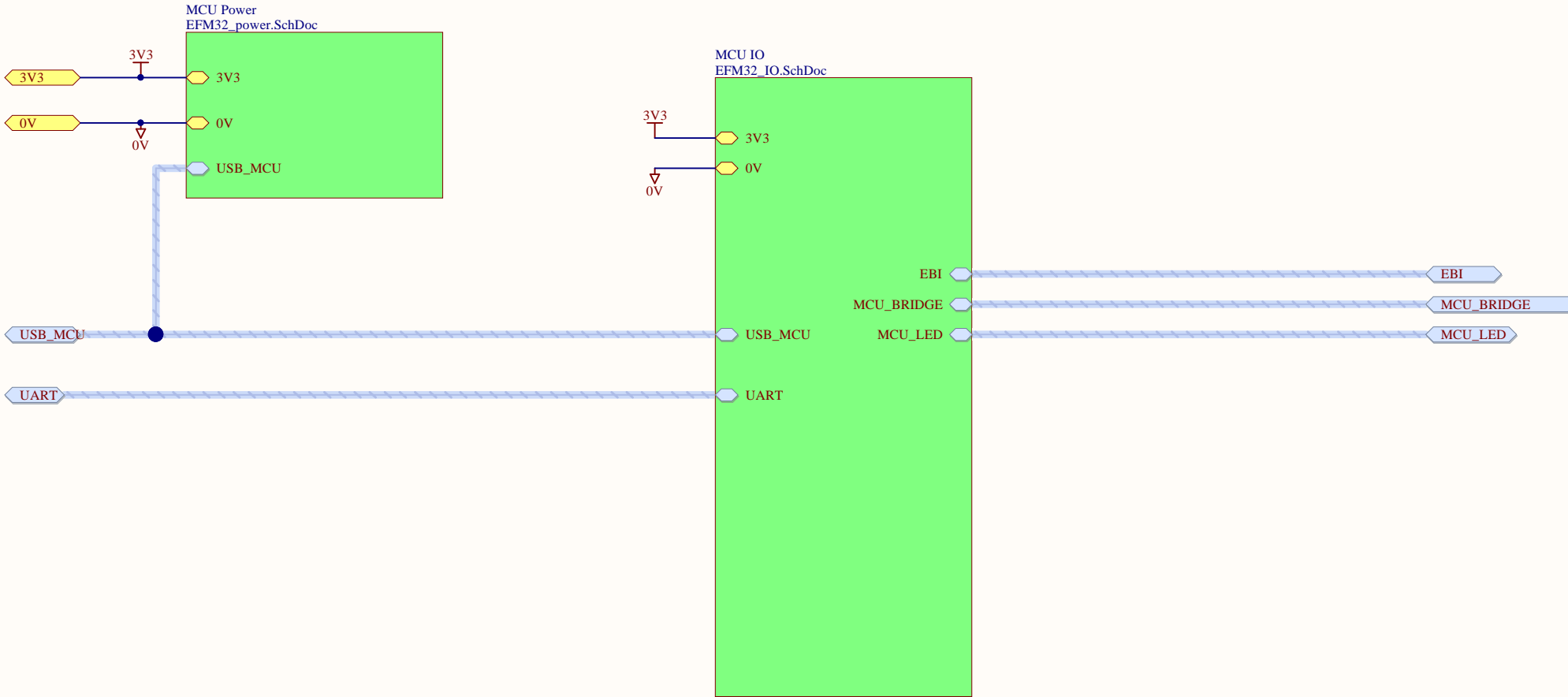
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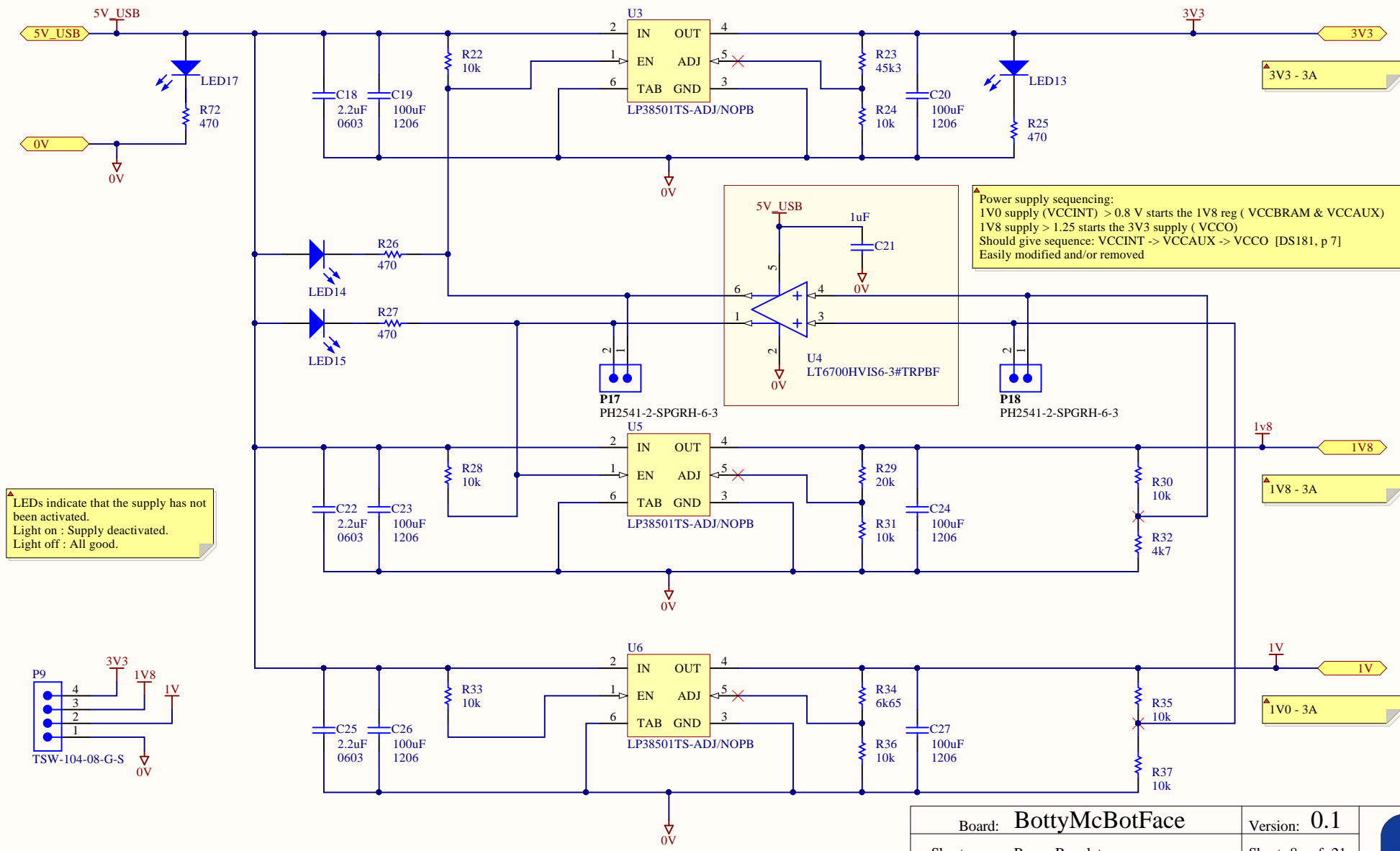
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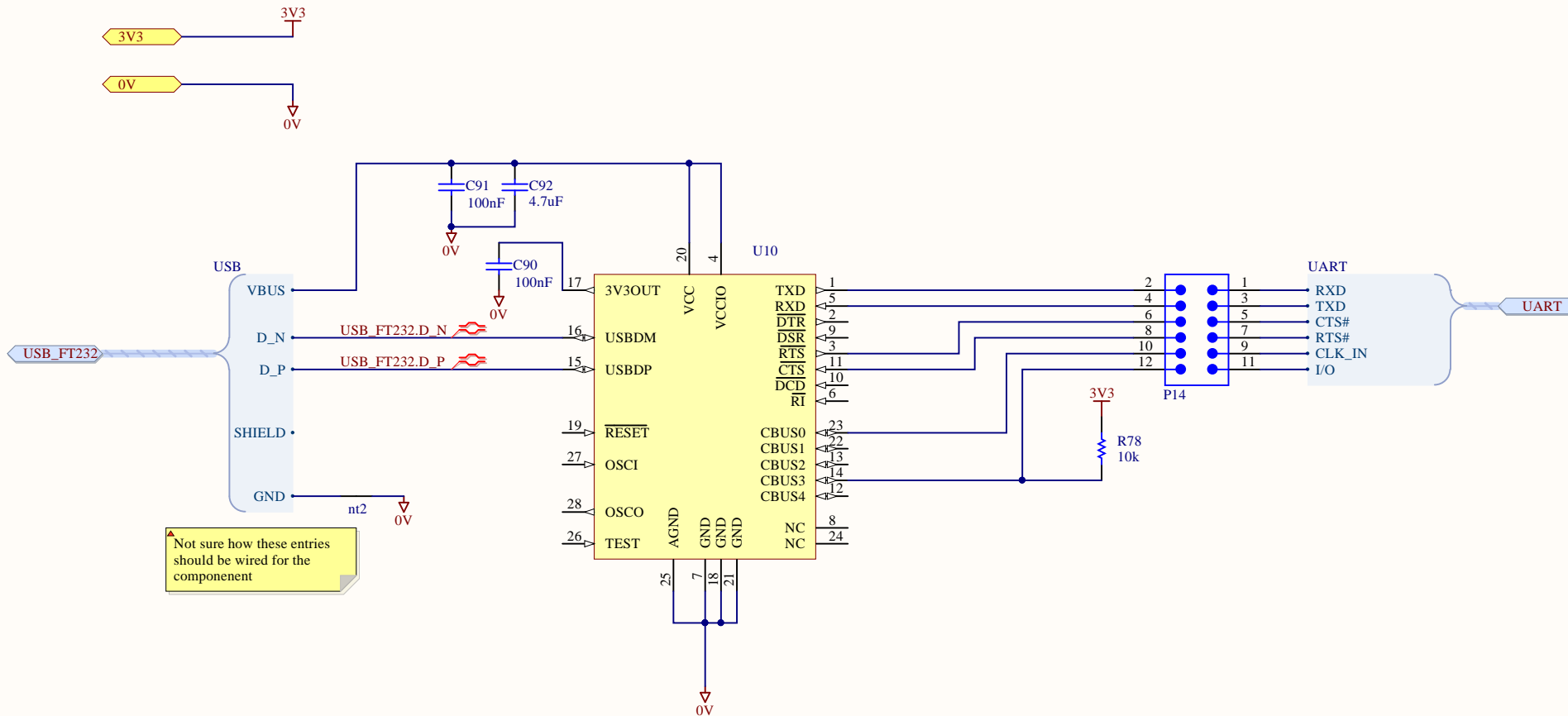
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Board:	BottyMcBotFace	Version:	0.1	
Sheetname:	Microcontroller Top Level	Sheet	4 of 21	
Subject:	TDT4295 Datamaskinprojekt 2016	Group:	Ytelse	
Schematic file:		MCUtop.SchDoc		



Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Power Regulators	Sheet	8 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	Power.SchDoc		



Board:	BottyMcBotFace	Version:	0.1	
Sheetname:	UART to USB Bridge	Sheet	10 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Shematic file:	UART_connect.SchDoc			

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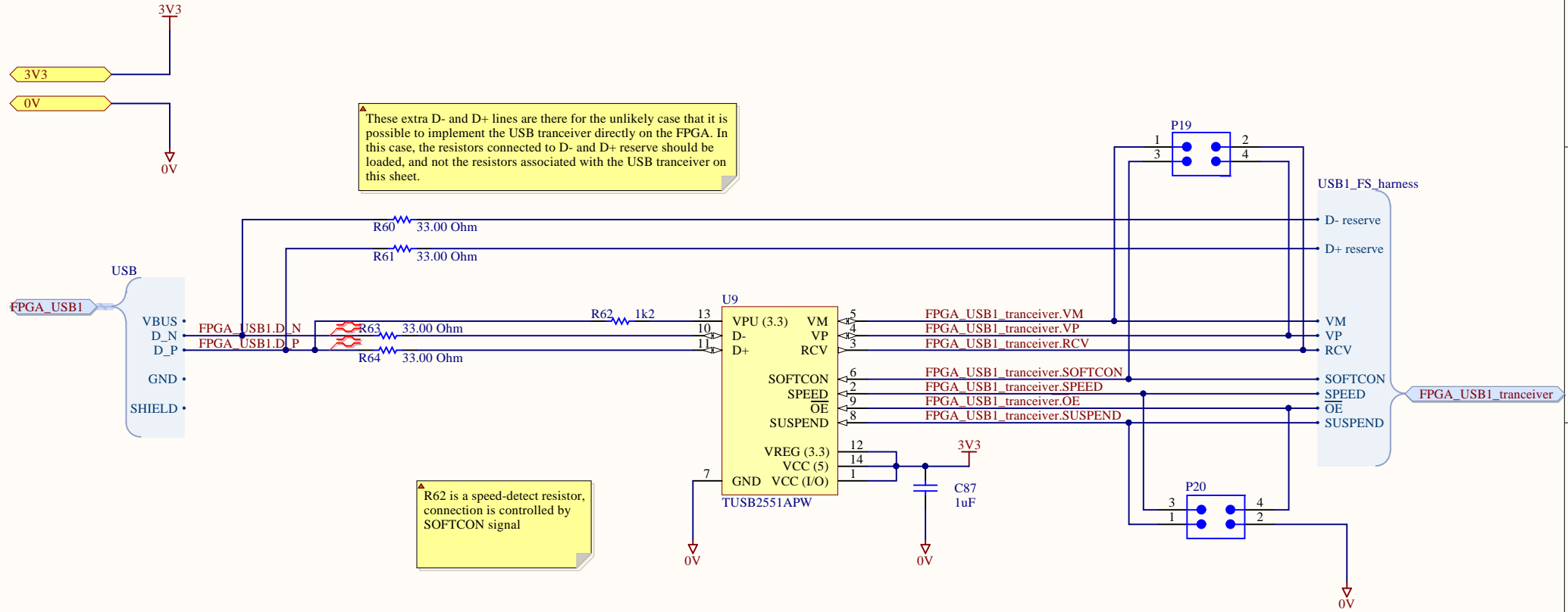
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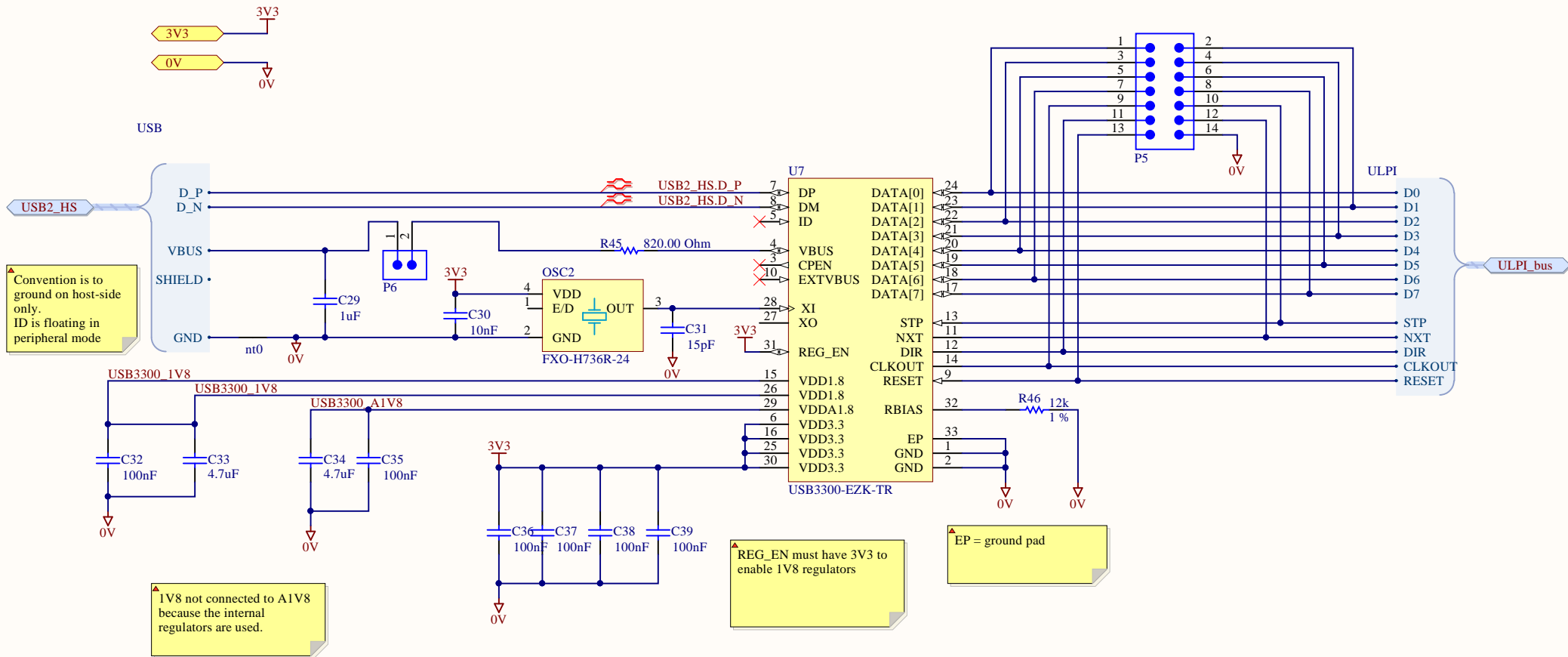
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Board:	BottyMcBotFace	Version:	0.1	
Sheetname:	USB Full Speed transceiver	Sheet	11 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Shematic file:	USB_trans.SchDoc			



USB3300 - Silicon Labs USB 2.0 High speed transceiver
- Connected in peripheral mode

Board: BottyMcBotFace	Version: 0.1	
Sheetname: USB 2.0 HS PHY	Sheet 12 of 21	
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse	
Schematic file: USB3300.SchDoc		

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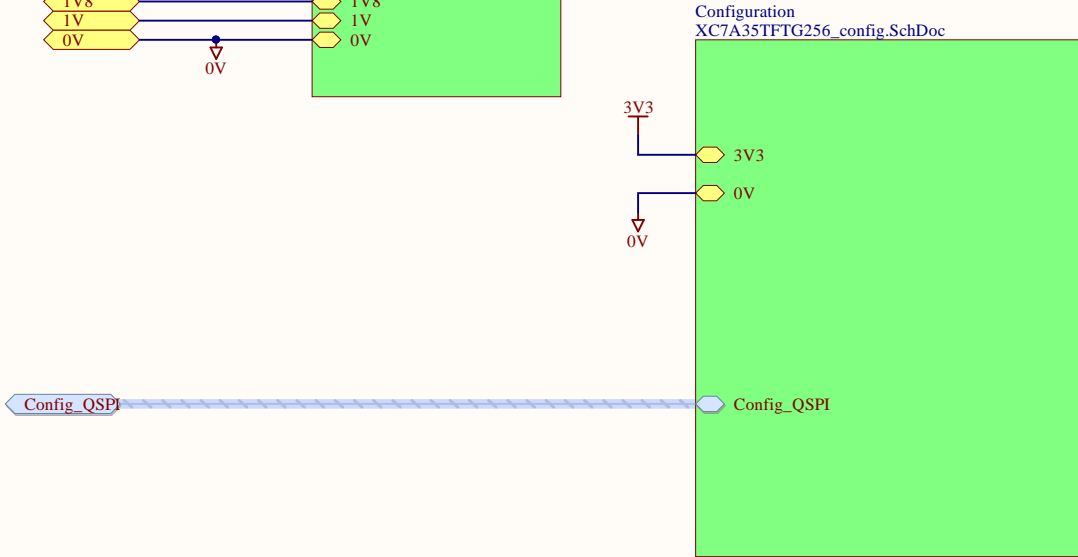
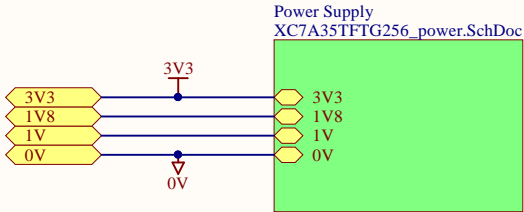
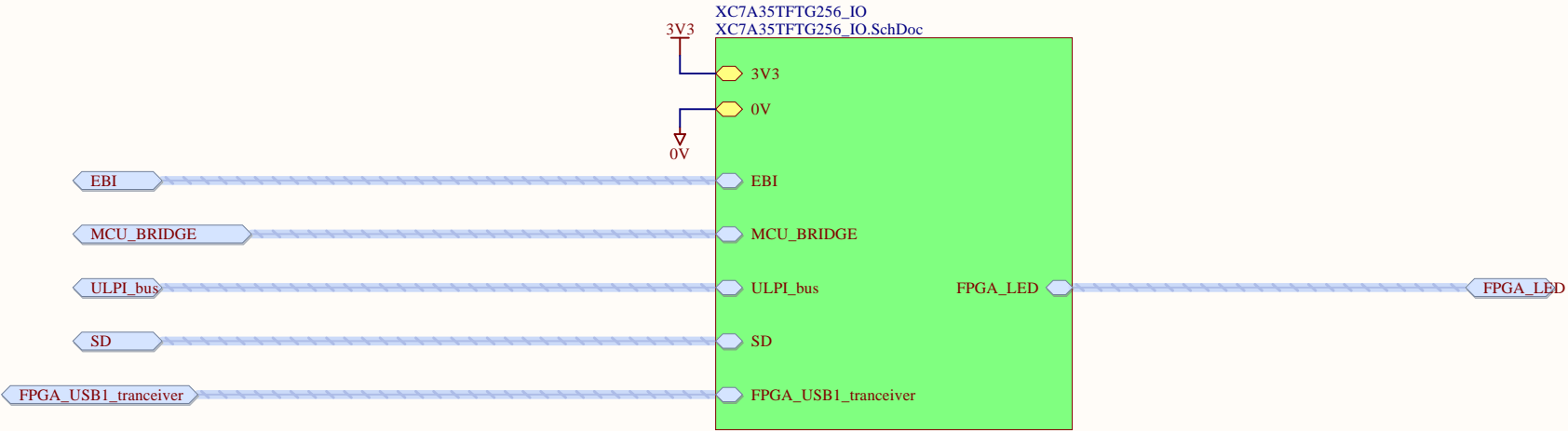
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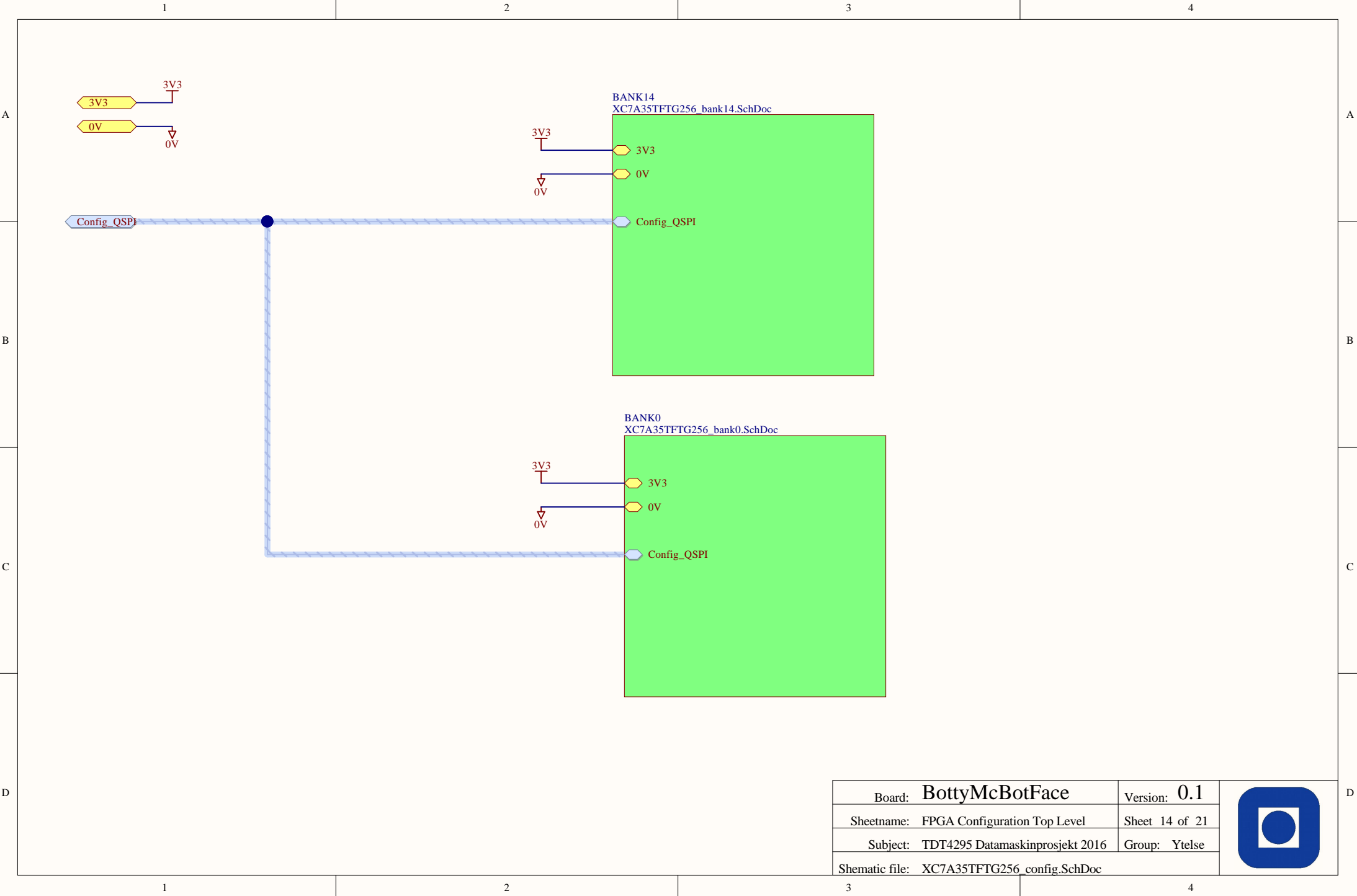
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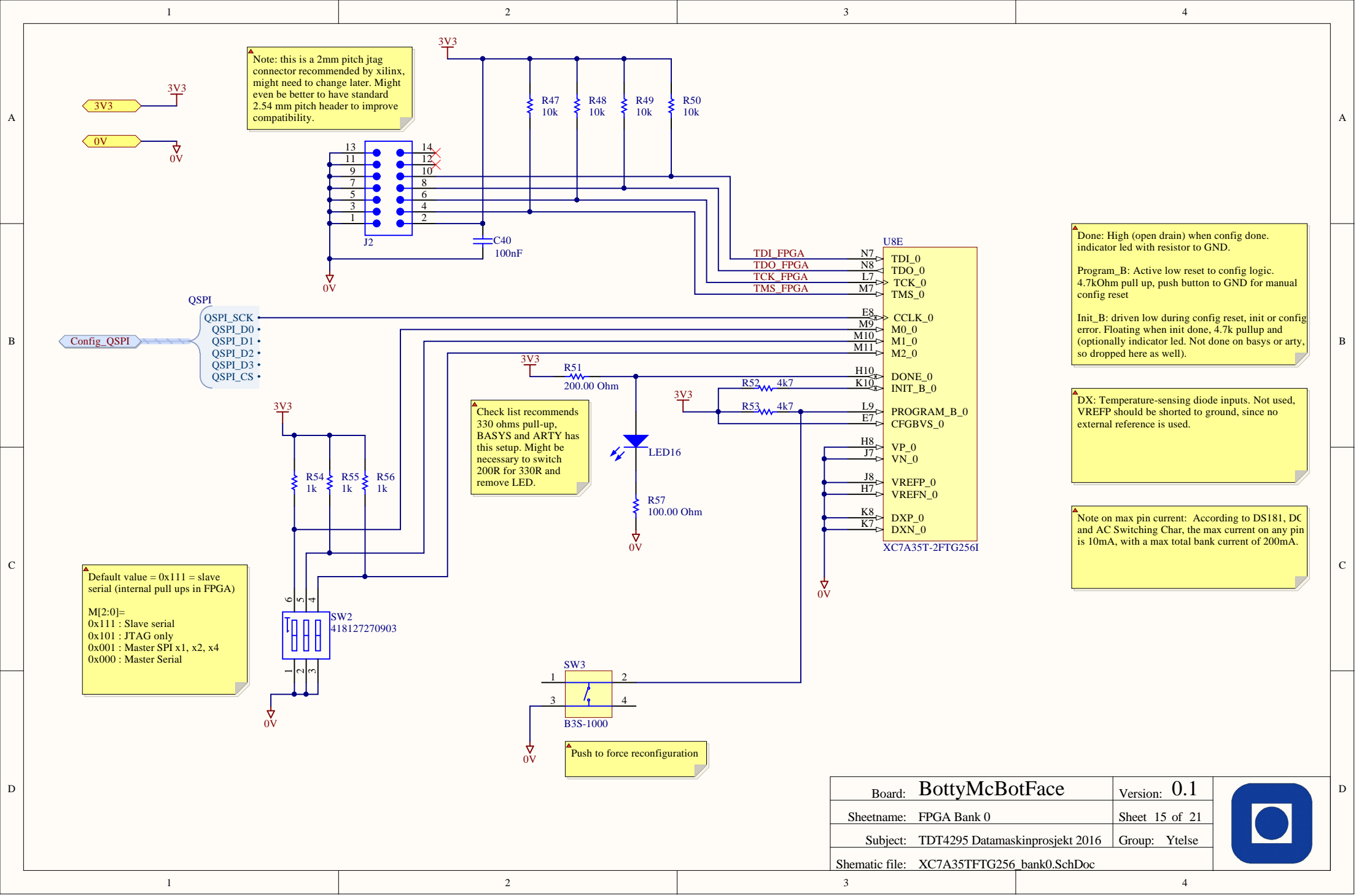
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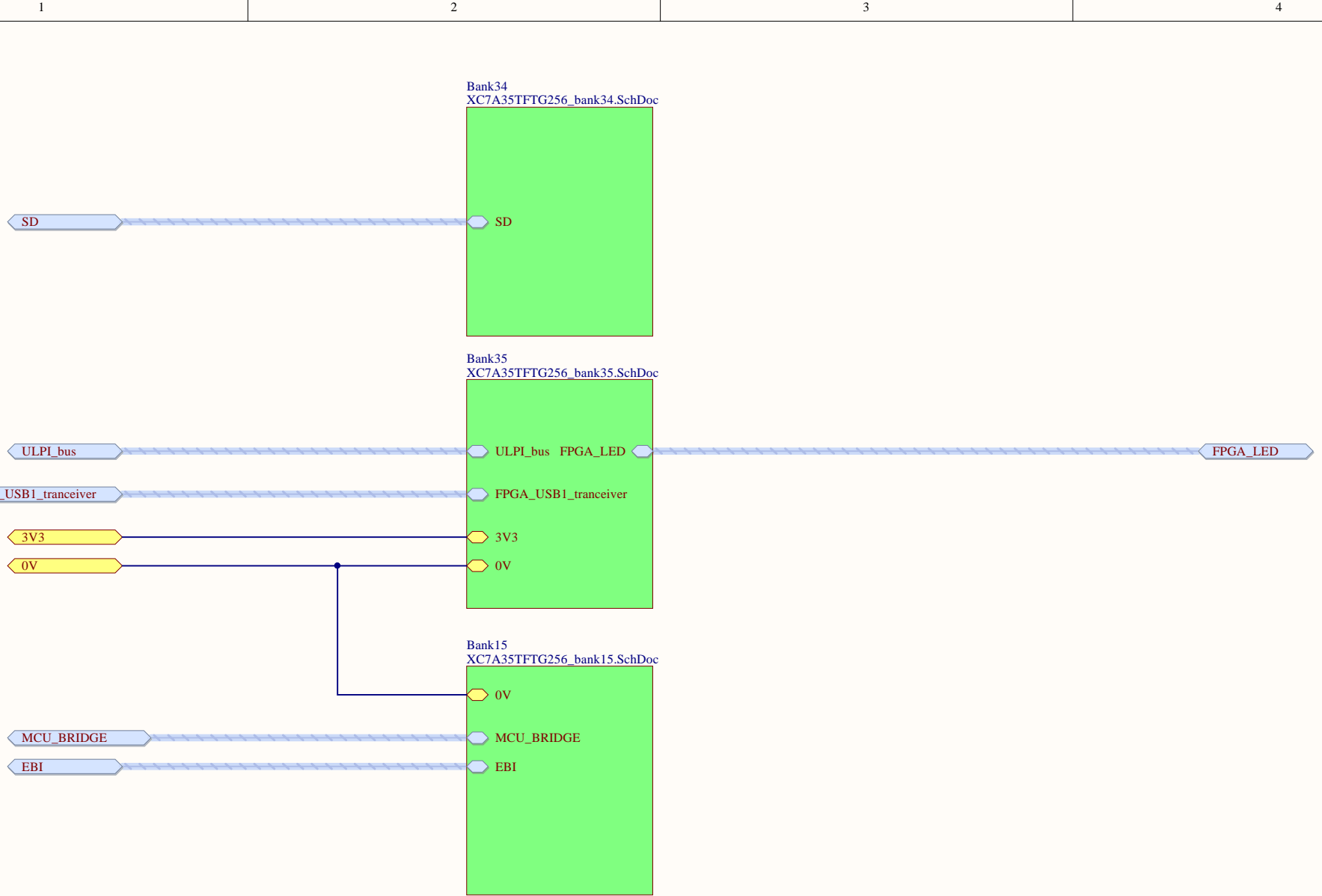


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Top level	Sheet	13 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256.SchDoc		

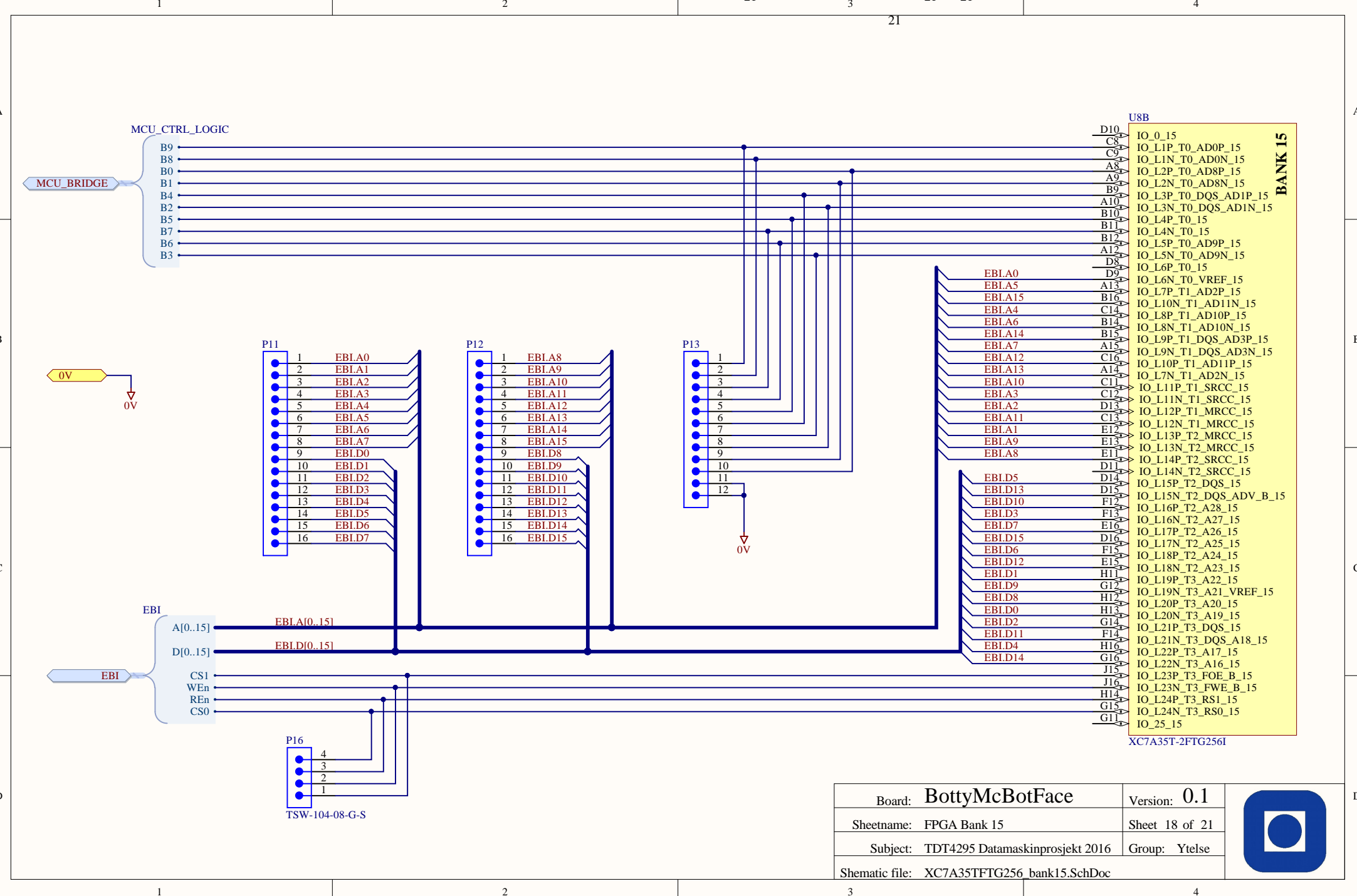








Board:	BottyMcBotFace	Version:	0.1	
Sheetname:	FPGA IO Top level	Sheet	17 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_IO.SchDoc				



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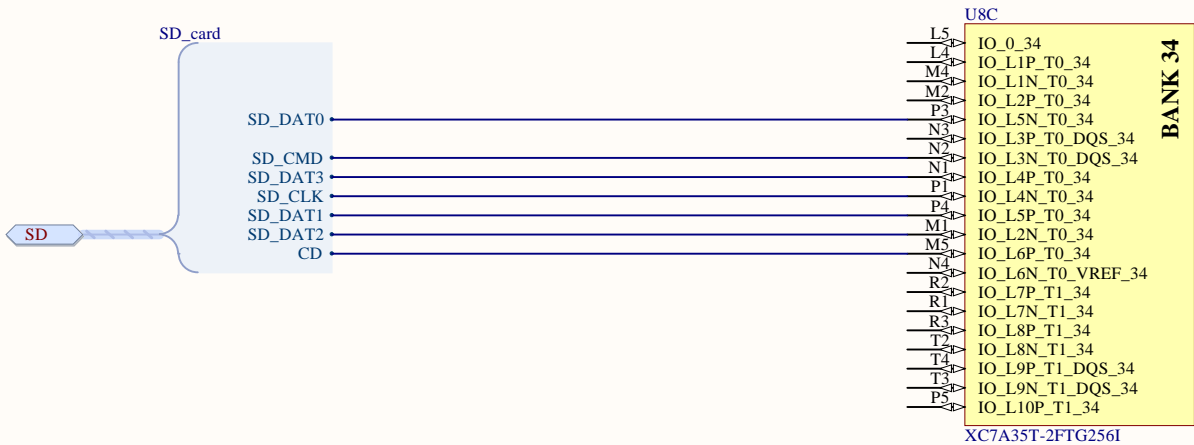
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Board:	BottyMcBotFace	Version:	0.1	
Sheetname:	FPGA Bank 34	Sheet	19 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_bank34.SchDoc				

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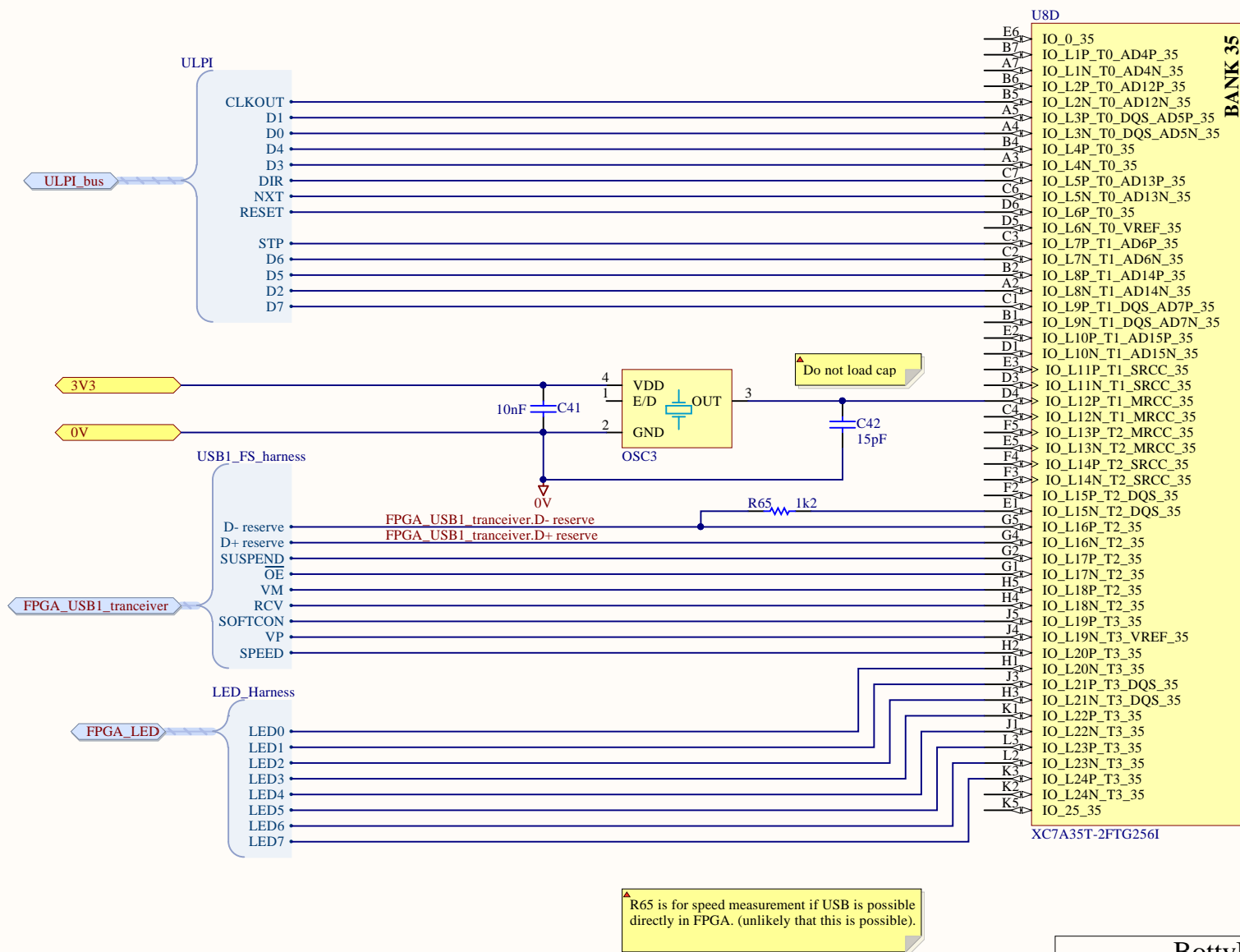
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Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Bank 35	Sheet	20 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank35.SchDoc		



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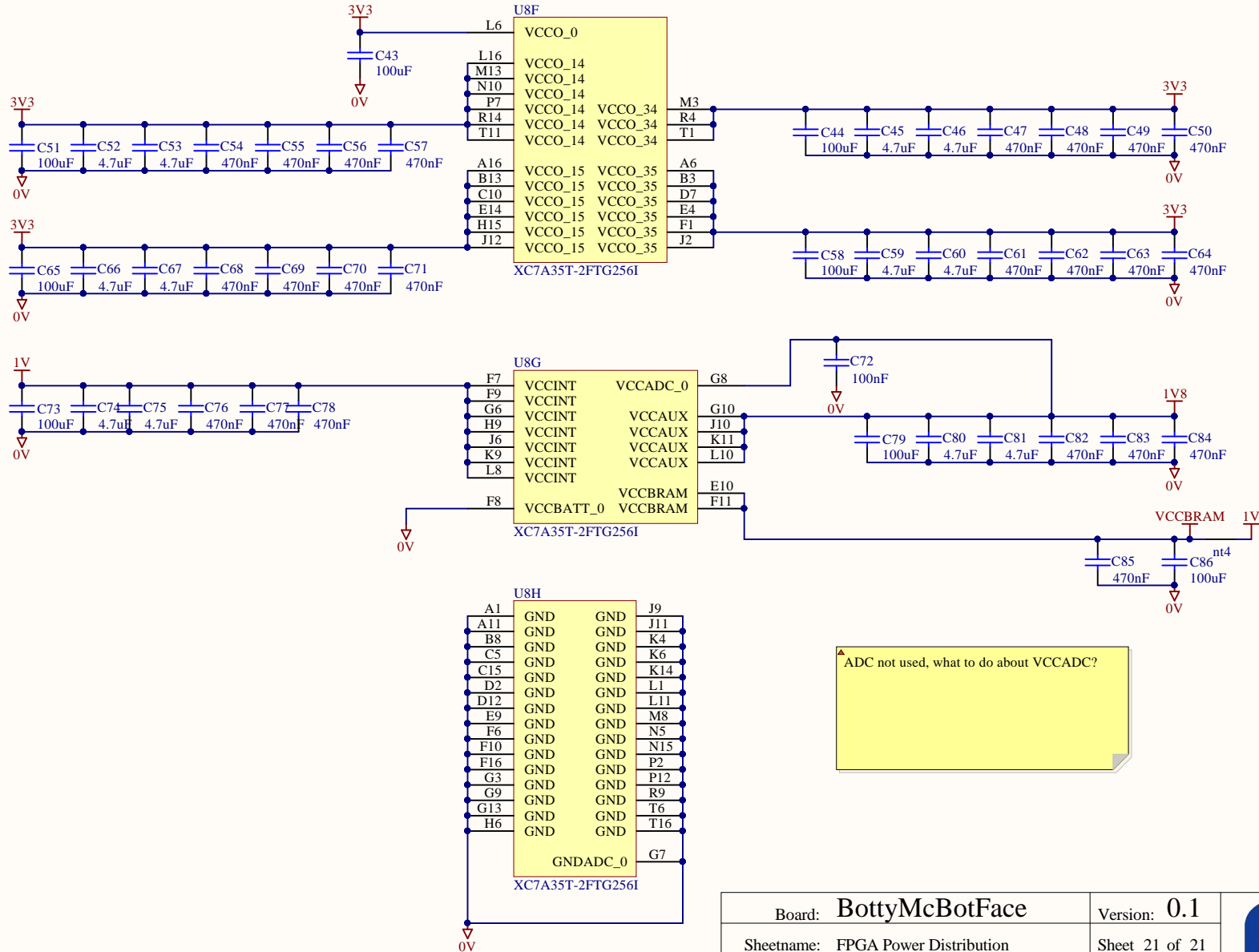
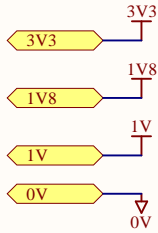
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ADC not used, what to do about VCCADC?

Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Power Distribution	Sheet	21 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_power.SchDoc		

