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Connectors  
Connectors.SchDoc

MCU  
MCUtop.SchDoc

FPGA  
XC7A35TFTG256.SchDoc

LEDs  
LED.SchDoc

UART-USB  
UART\_connect.SchDoc

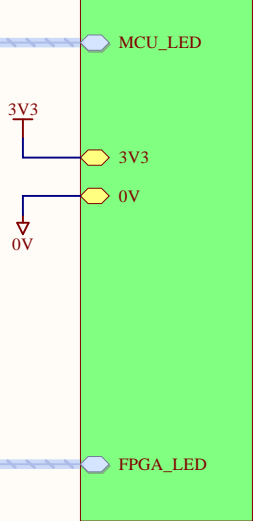
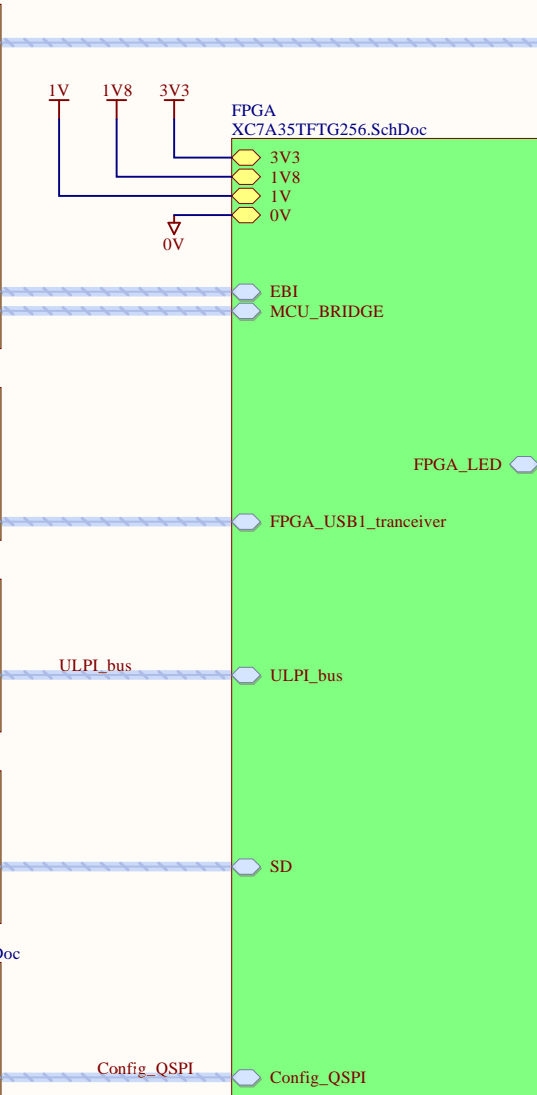
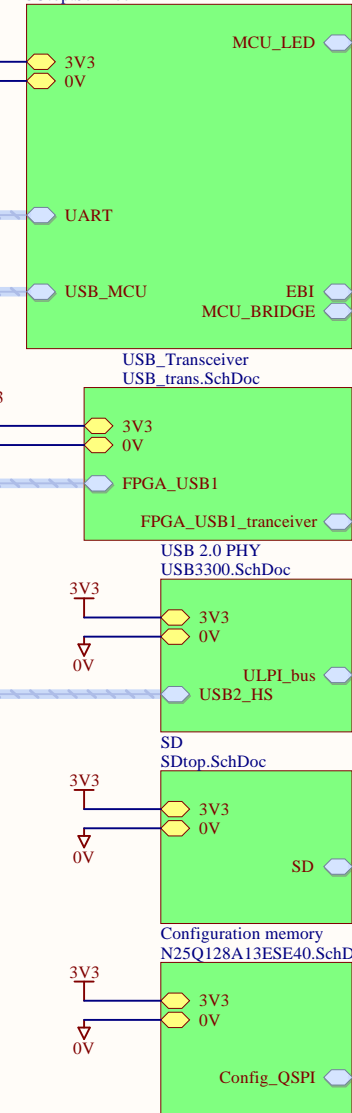
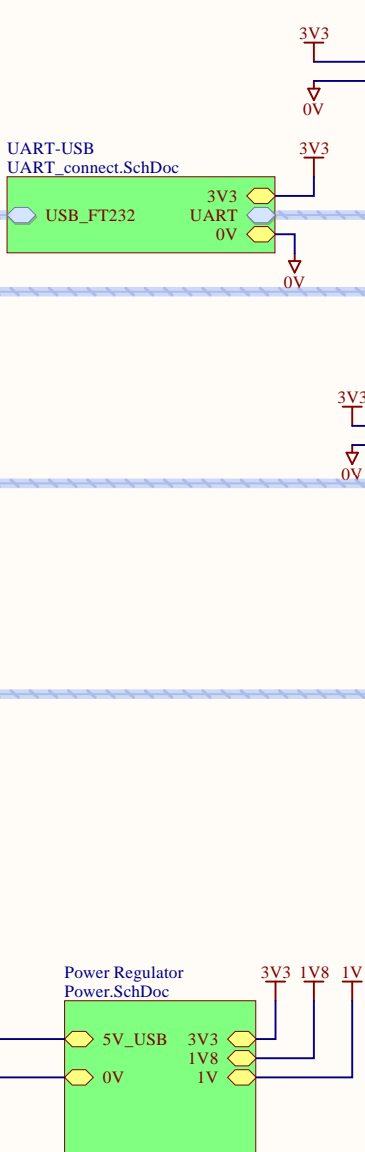
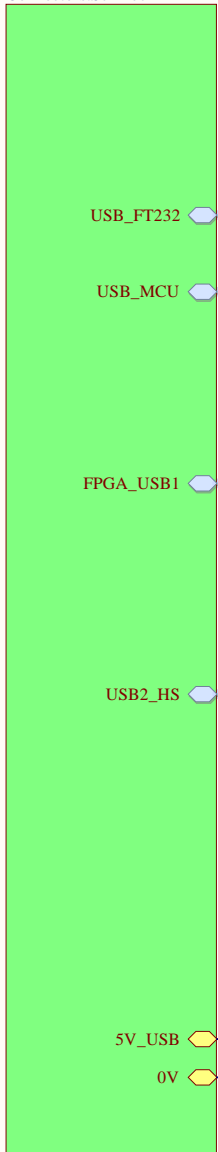
USB Transceiver  
USB\_trans.SchDoc

USB 2.0 PHY  
USB3300.SchDoc

SD  
SDtop.SchDoc

Configuration memory  
N25Q128A13ESE40.SchDoc

Power Regulator  
Power.SchDoc



Board:	PACMAN	Version:	0.3
Sheetname:	Top level	Sheet	1 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	main.SchDoc		



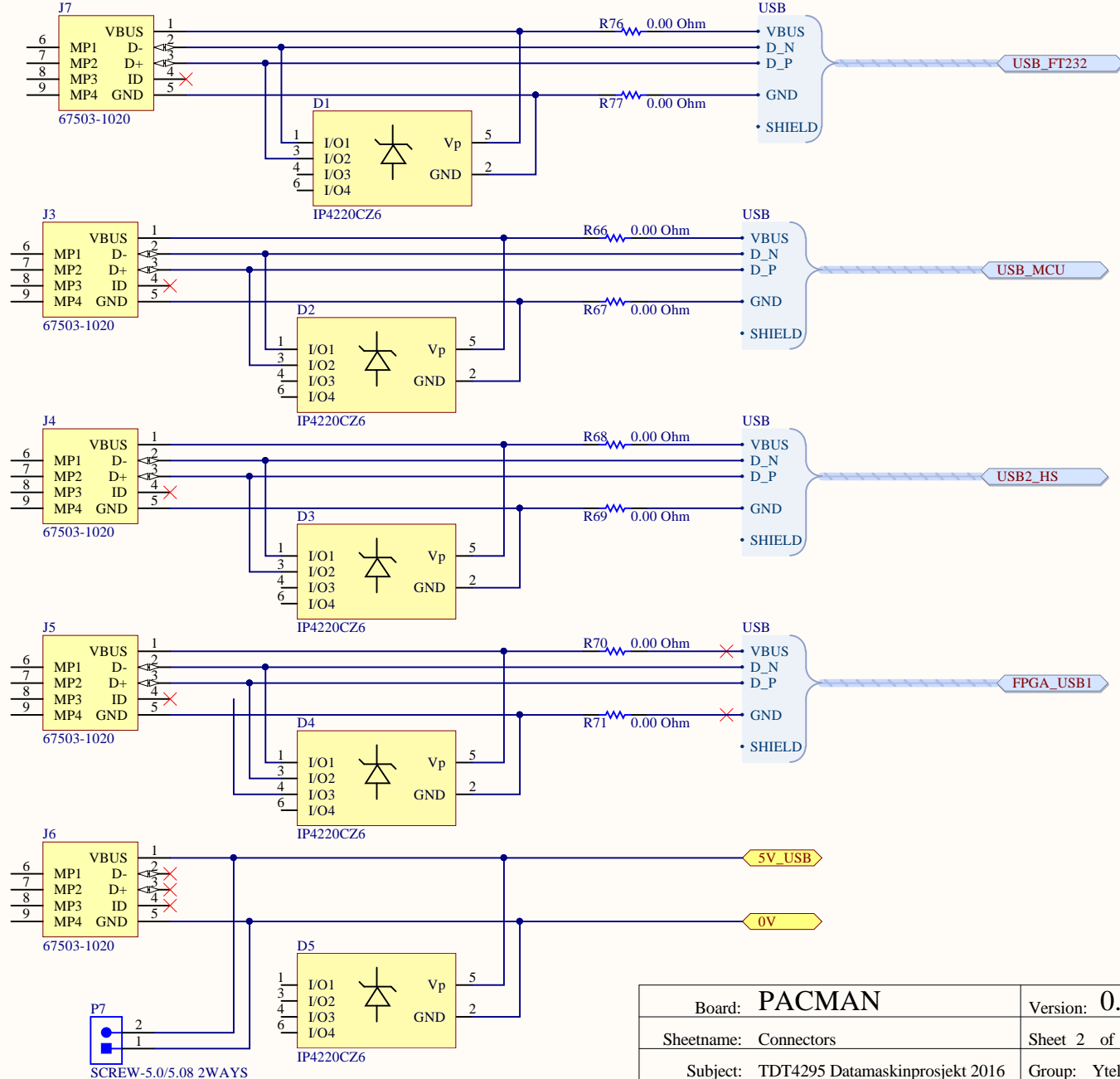
Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side



Board: PACMAN	Version: 0.3
Sheetname: Connectors	Sheet 2 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Schematic file: Connectors.SchDoc	



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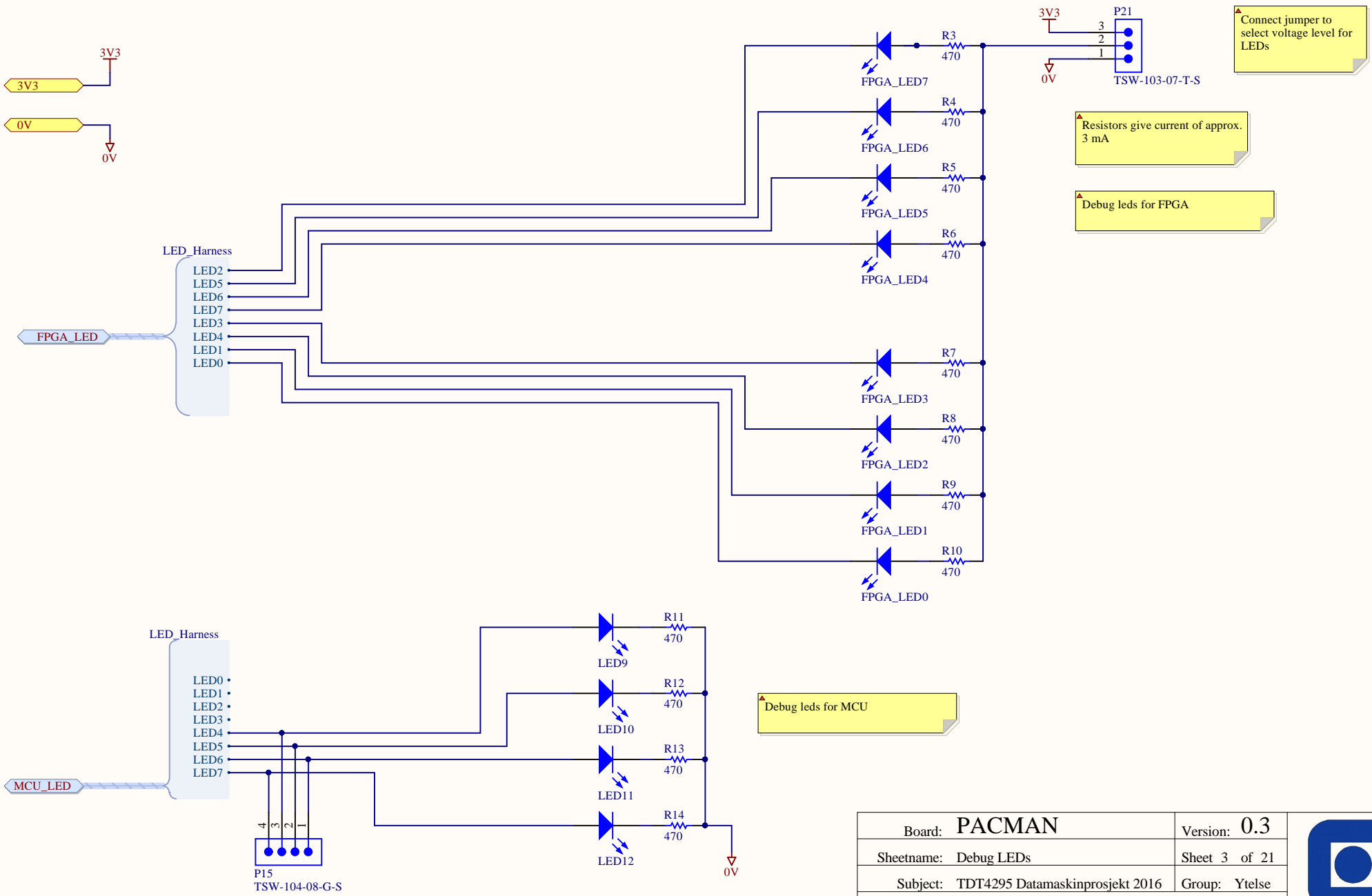
D

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Board: PACMAN	Version: 0.3
Sheetname: Debug LEDs	Sheet 3 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Schematic file: LED.SchDoc	



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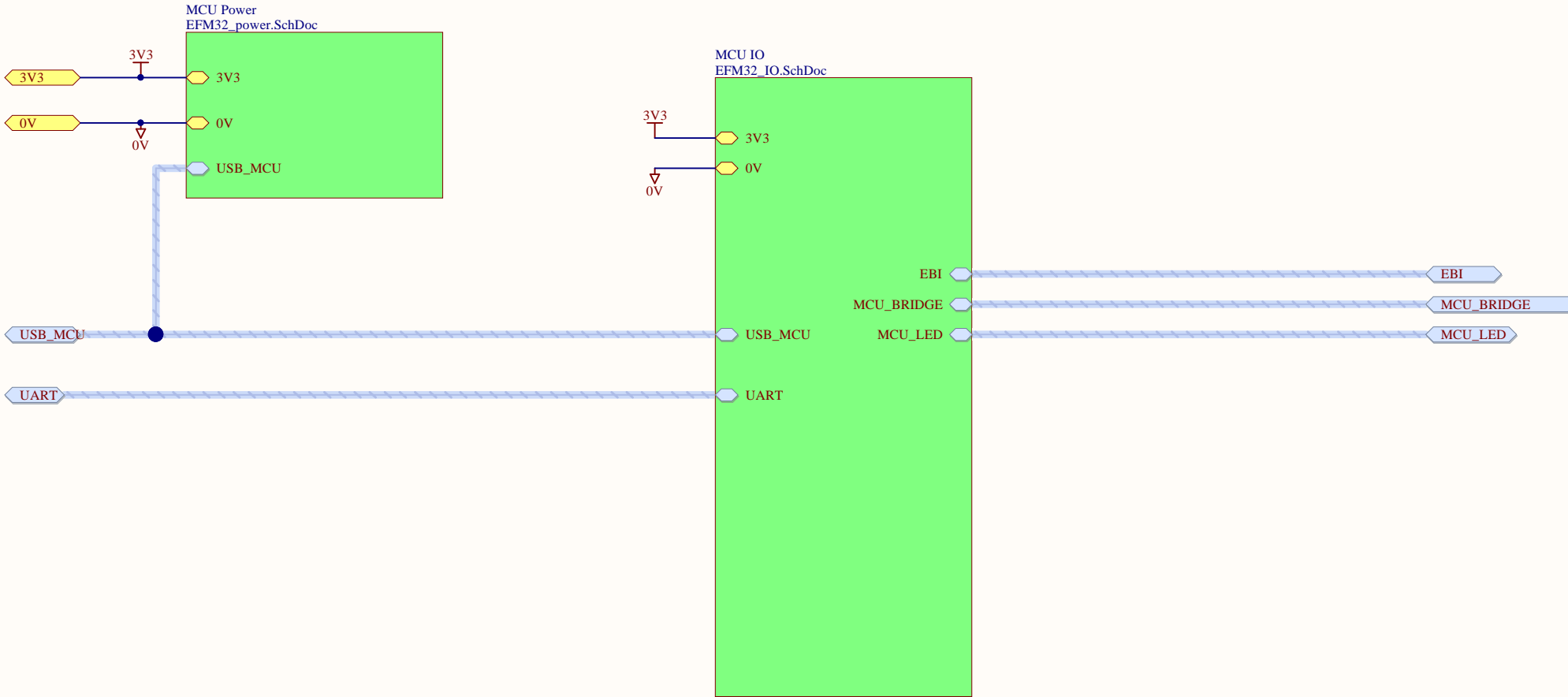
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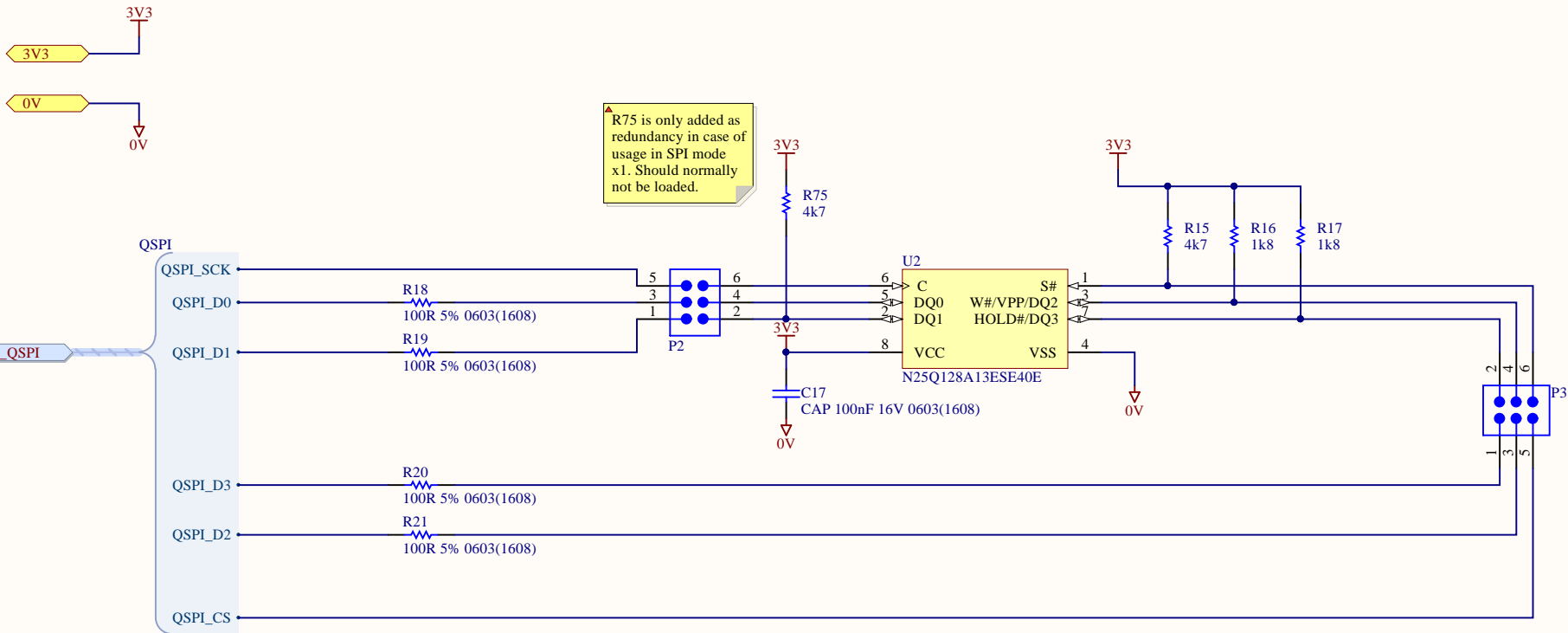
D



Board: PACMAN	Version: 0.3	
Sheetname: Microcontroller Top Level	Sheet 4 of 21	
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse	
Schematic file: MCUtop.SchDoc		







R75 is only added as redundancy in case of usage in SPI mode x1. Should normally not be loaded.

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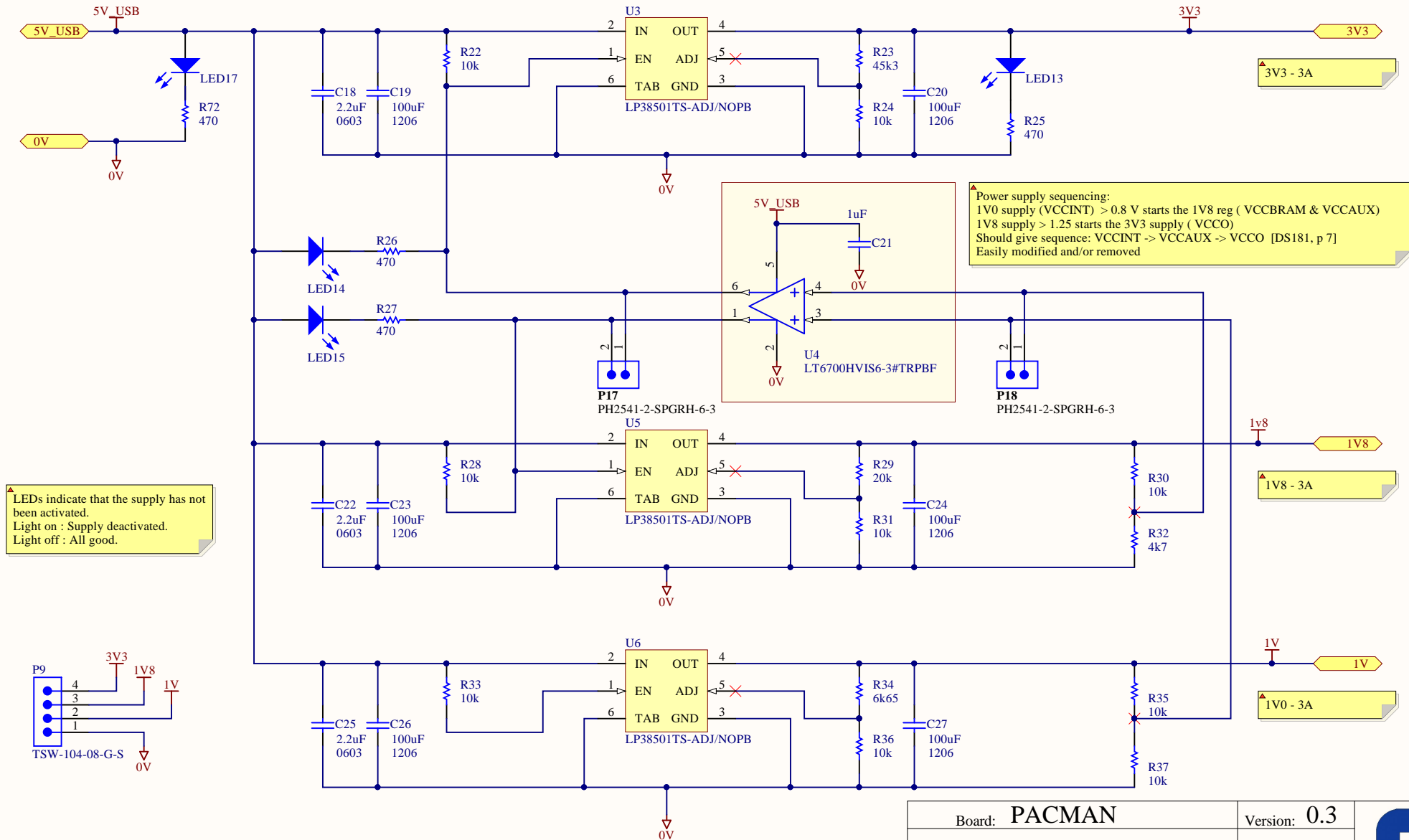
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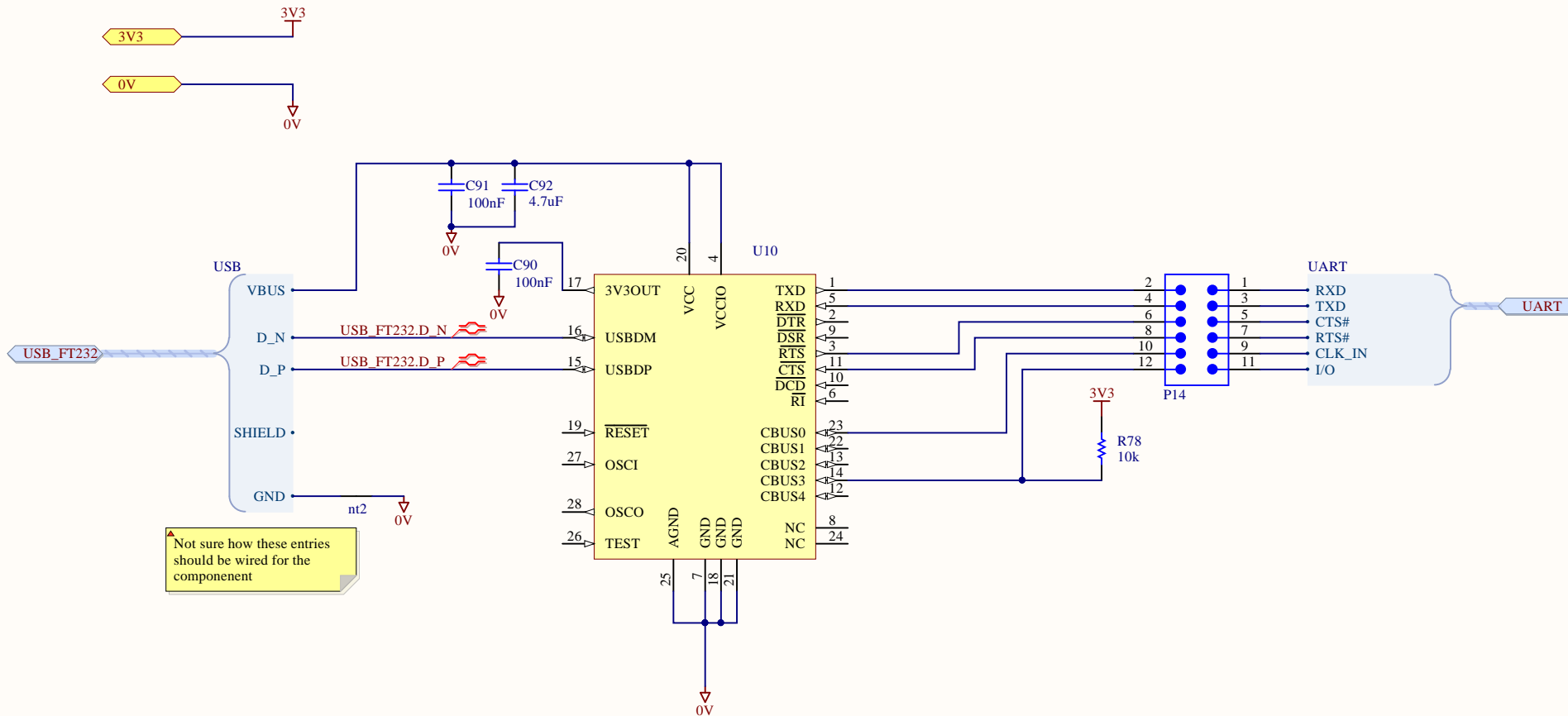



Board:	PACMAN	Version:	0.3
Sheetname:	Power Regulators	Sheet	8 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	Power.SchDoc		









Board: PACMAN	Version: 0.3	
Sheetname: UART to USB Bridge	Sheet 10 of 21	
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse	
Shematic file: UART_connect.SchDoc		

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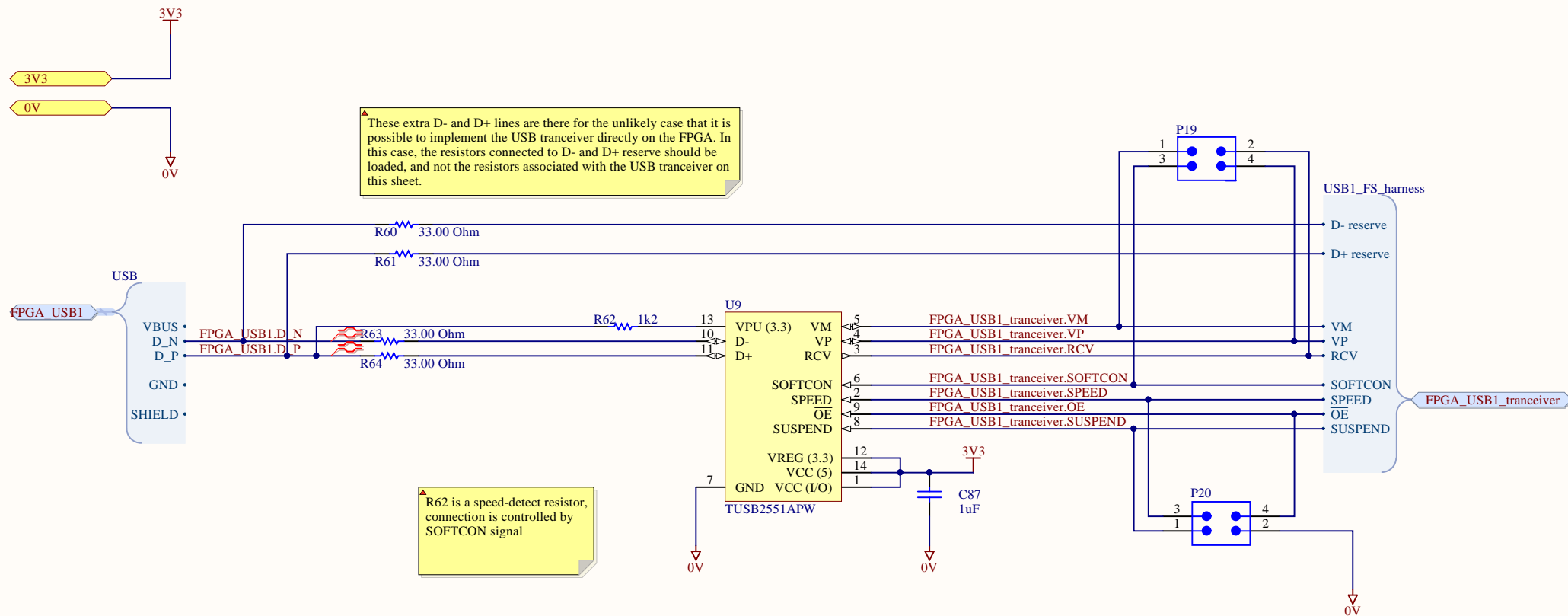
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Board:	PACMAN	Version:	0.3
Sheetname:	USB Full Speed transceiver	Sheet	11 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	USB_trans.SchDoc		





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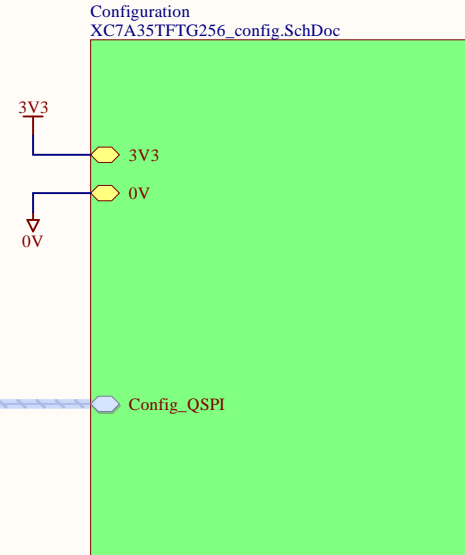
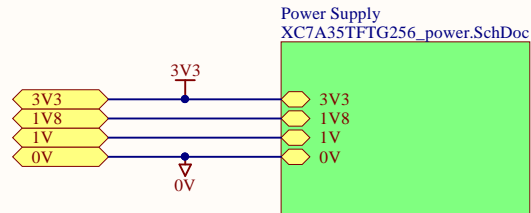
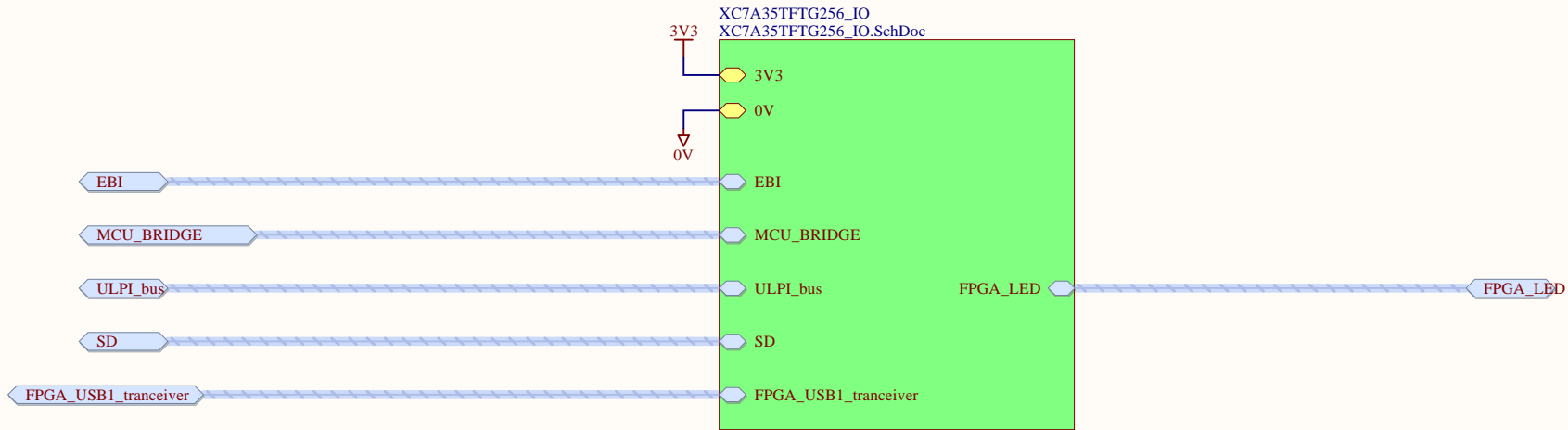
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Board:	PACMAN	Version:	0.3	
Sheetname:	FPGA Top level	Sheet	13 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file:			XC7A35TFTG256,SchDoc	

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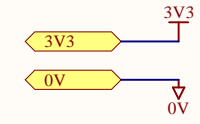
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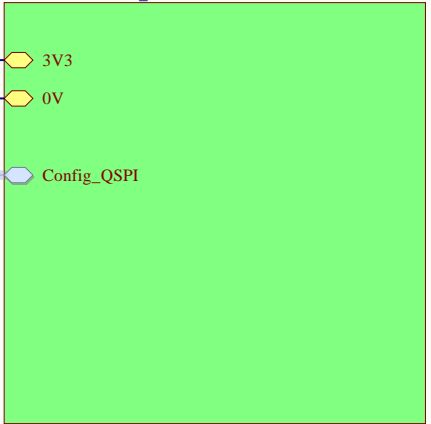
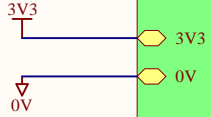
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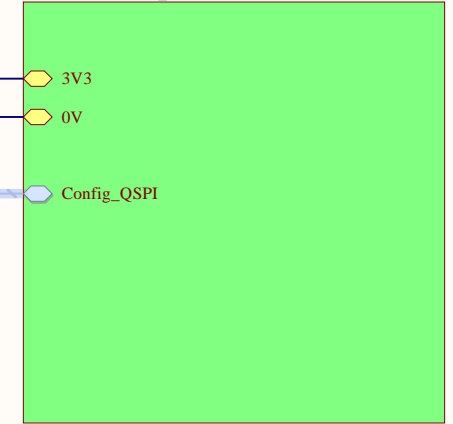
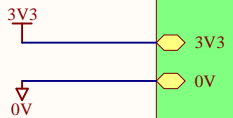
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BANK14  
XC7A35TFTG256\_bank14.SchDoc




BANK0  
XC7A35TFTG256\_bank0.SchDoc

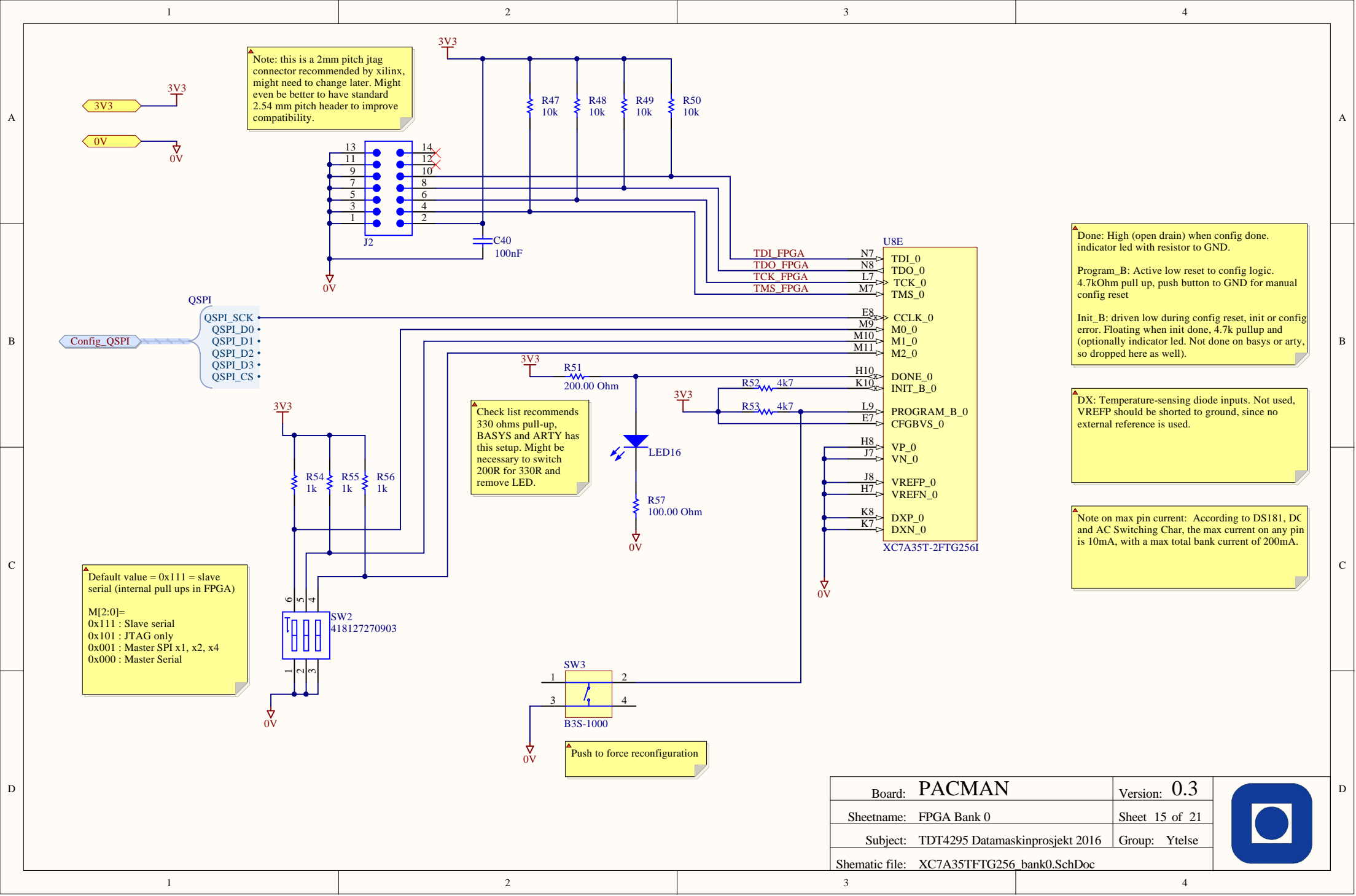


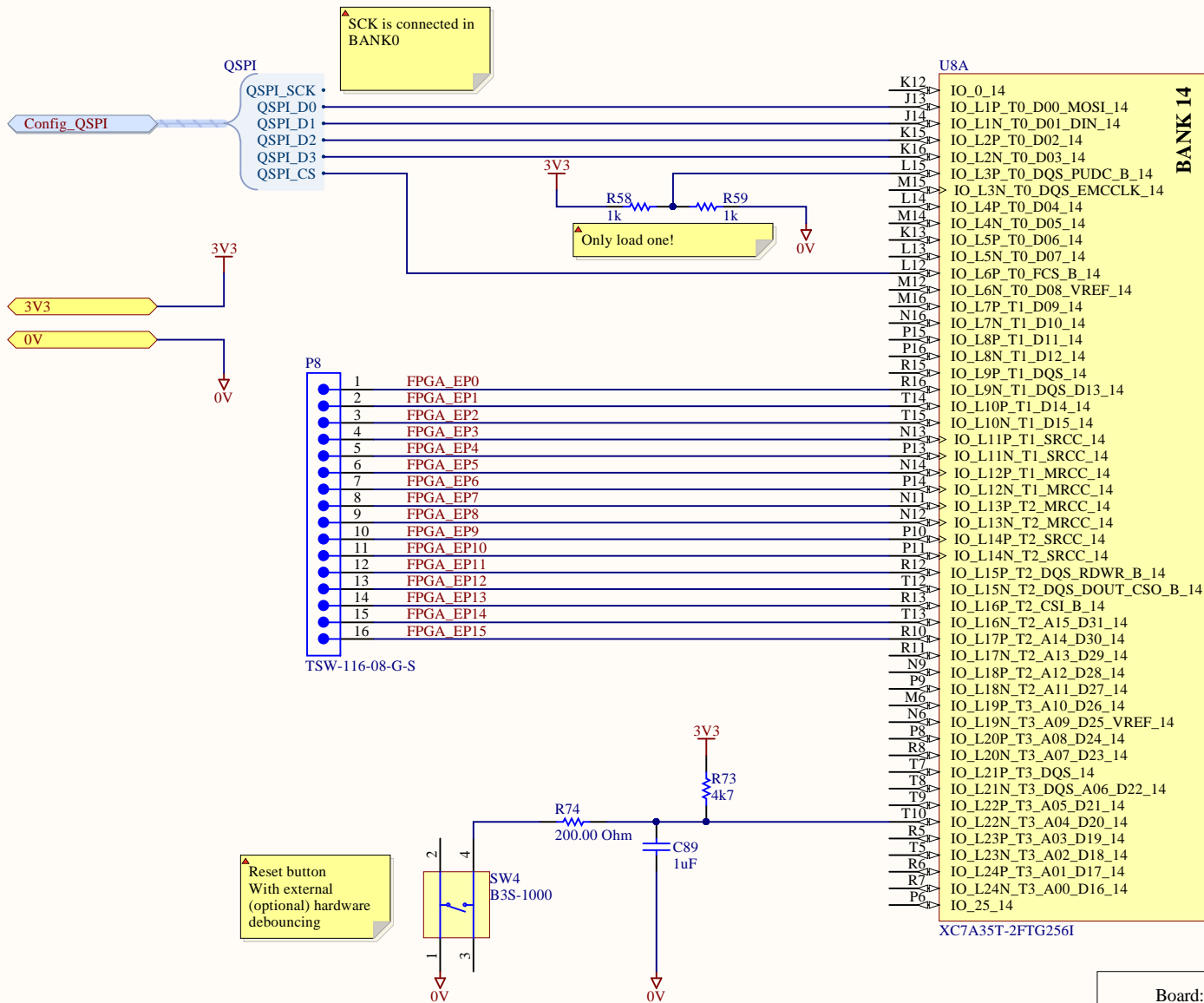
Config\_QSPI

Config\_QSPI

Config\_QSPI

Board:	PACMAN	Version:	0.3	
Sheetname:	FPGA Configuration Top Level	Sheet	14 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_config.SchDoc				





▲ PUDC: PullUp During Config. Low = Pull-up on selectIO, High = no Pull-up on SelectIO. Must not float!

Seems like PUDC=0 means that all IO will have pull-ups during config. Could be nice to have. Most safe option is to insert resistors that will allow selection between them.

EMCCCLK: External Master Config Clock. Optional external clock source for config. Necessary?

▲ FCS\_B = Flash chip select

▲ VREF = Input reference voltage for Single-ended I/O standards with differential input buffer. Se UG471, page 18.

Appears to be a reference for a schmitt-trigger or something, and can be sourced internally, if needed. However, that will mean that the max Vref = 0.9V. Not sure if this is a problem.

Board:	PACMAN	Version:	0.3
Sheetname:	FPGA Bank 14	Sheet	16 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank14.SchDoc		





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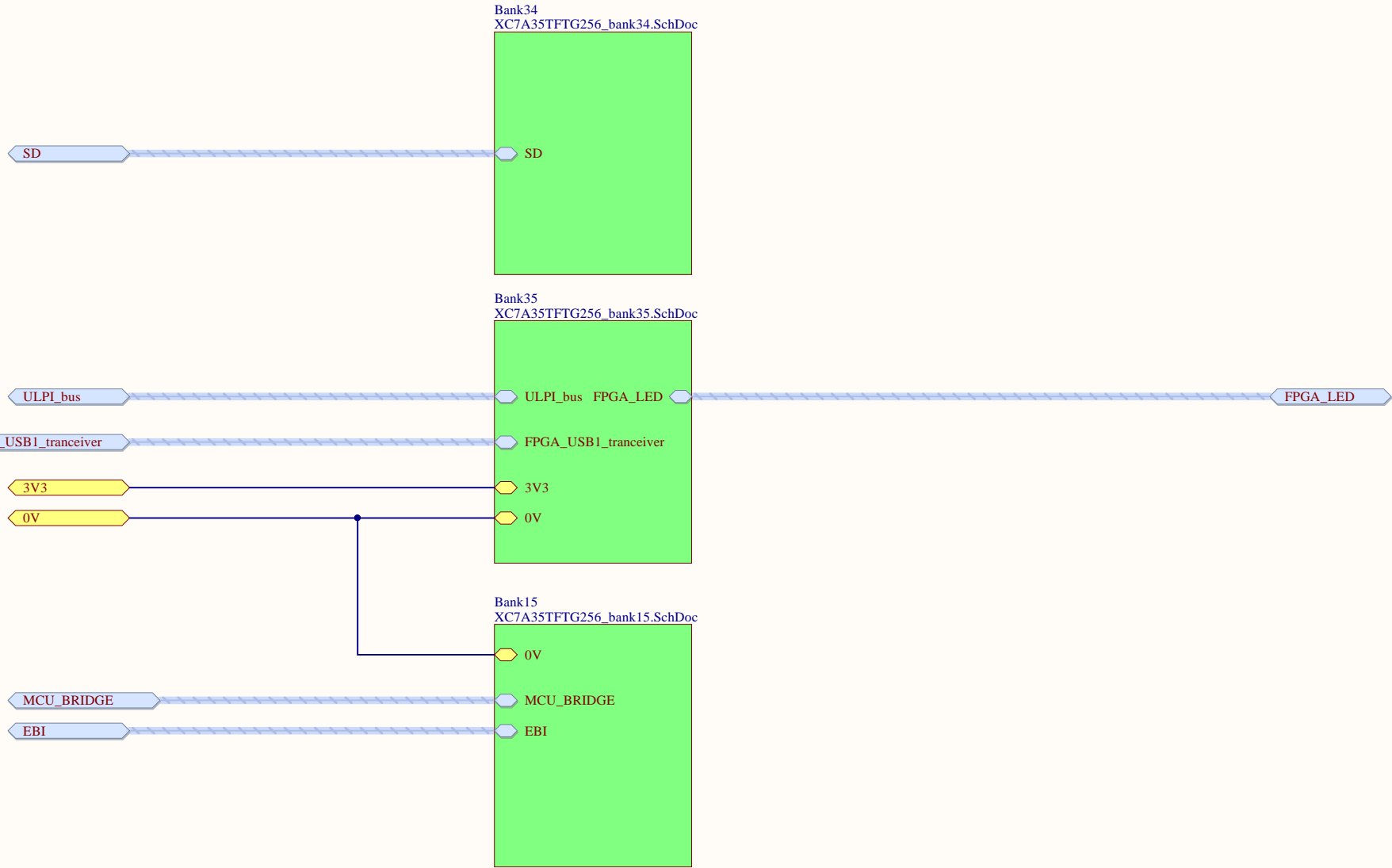
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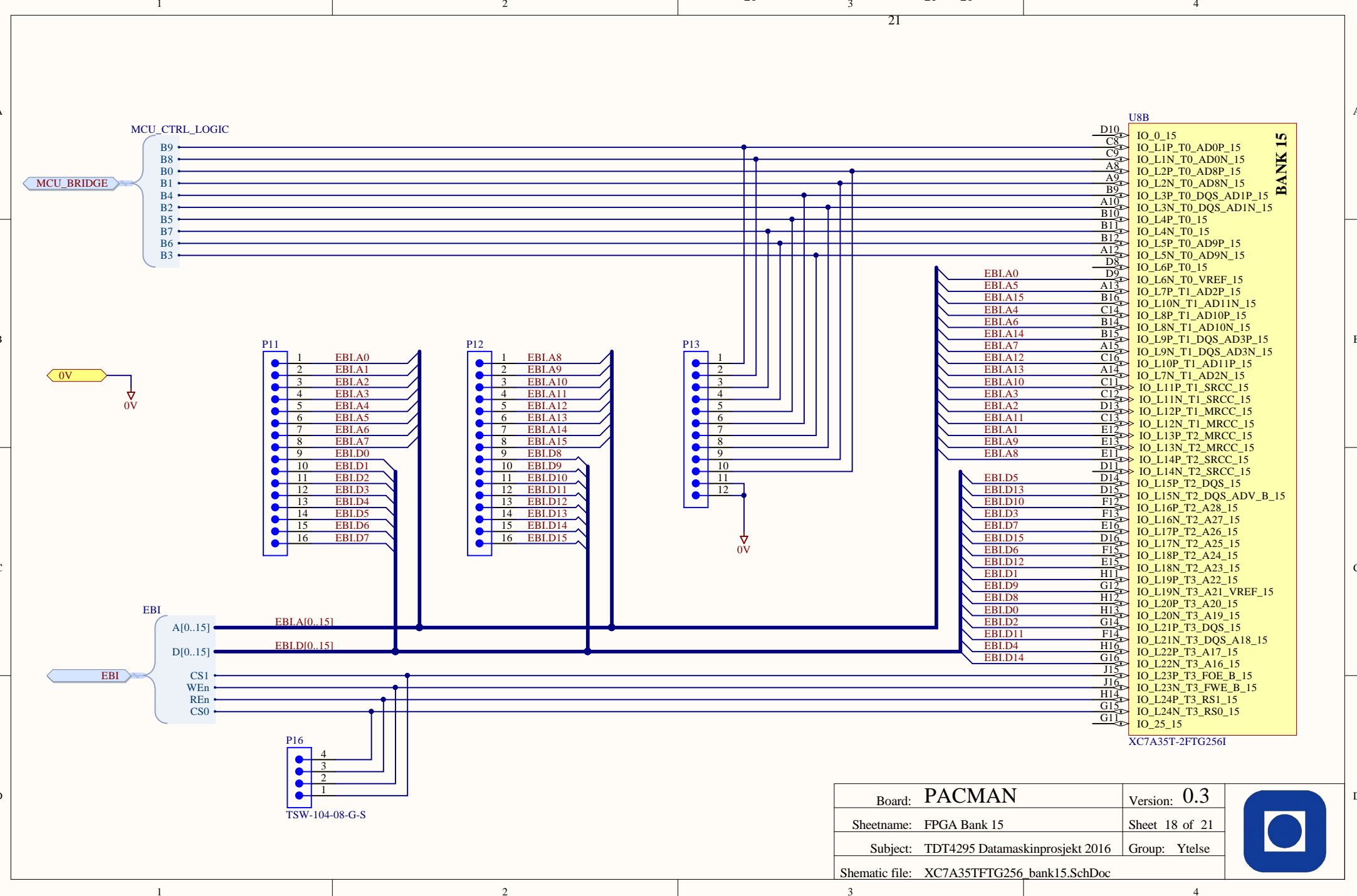
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Board:	PACMAN	Version:	0.3	
Sheetname:	FPGA IO Top level	Sheet	17 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_IO.SchDoc				



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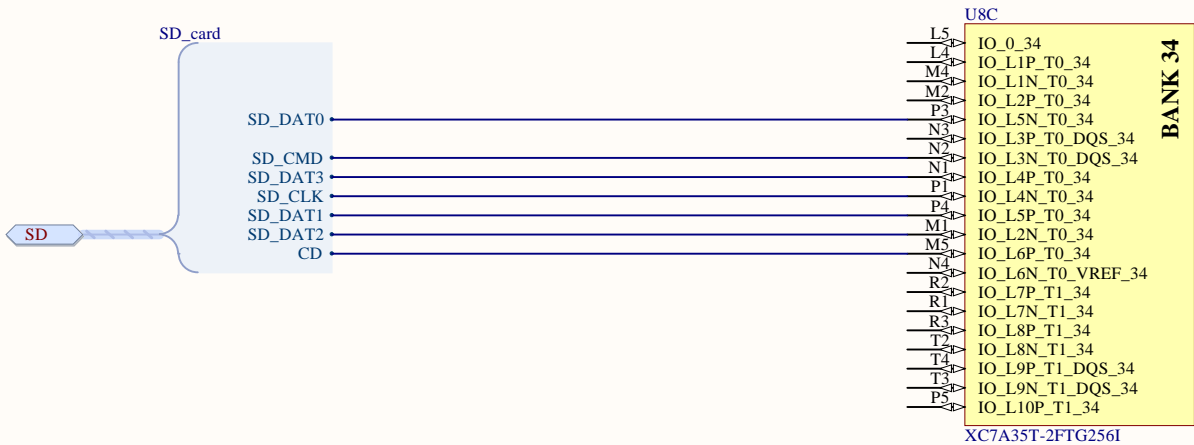
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Board:	PACMAN	Version:	0.3	
Sheetname:	FPGA Bank 34	Sheet	19 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_bank34.SchDoc				

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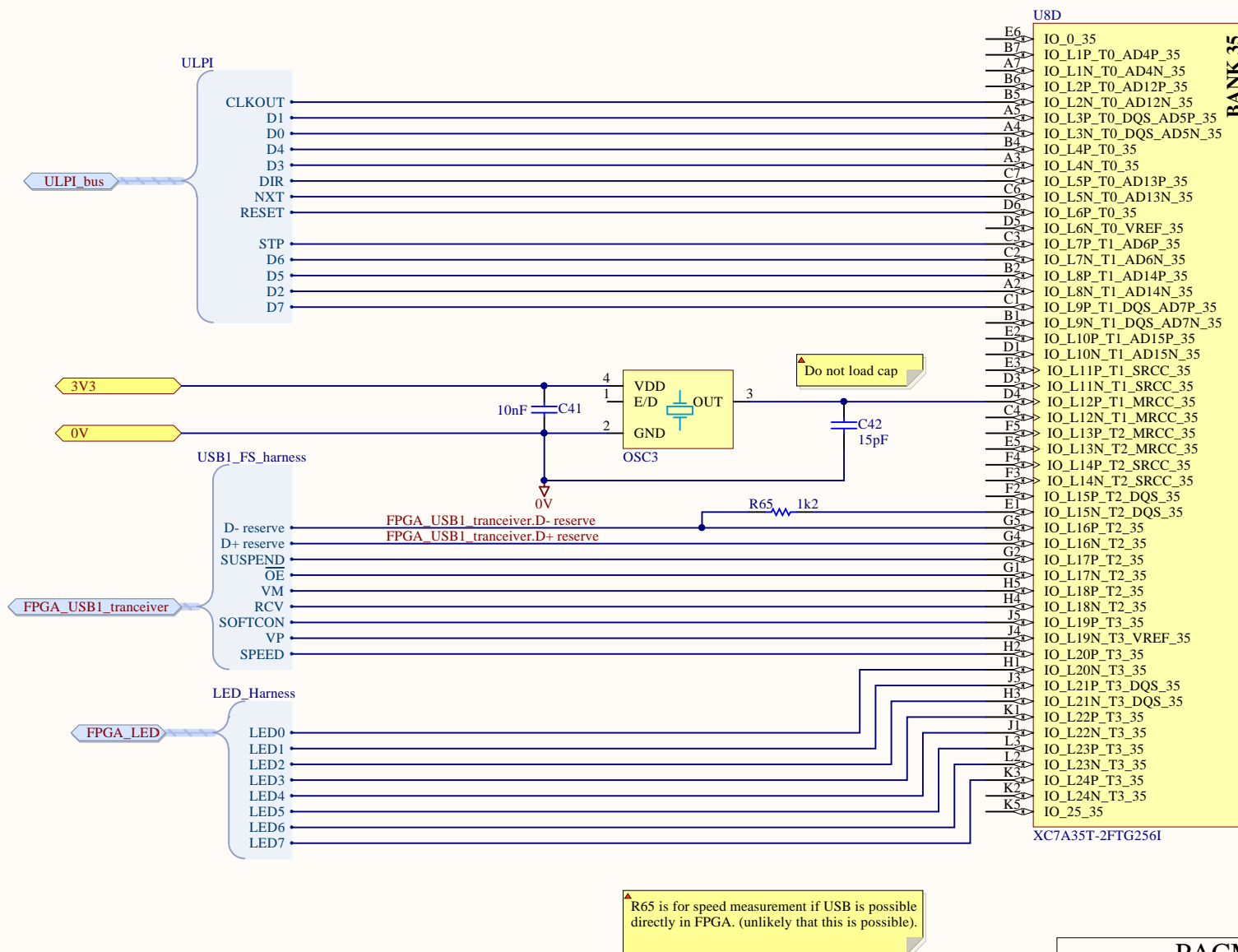
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Board:	PACMAN	Version:	0.3
Sheetname:	FPGA Bank 35	Sheet	20 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank35.SchDoc		



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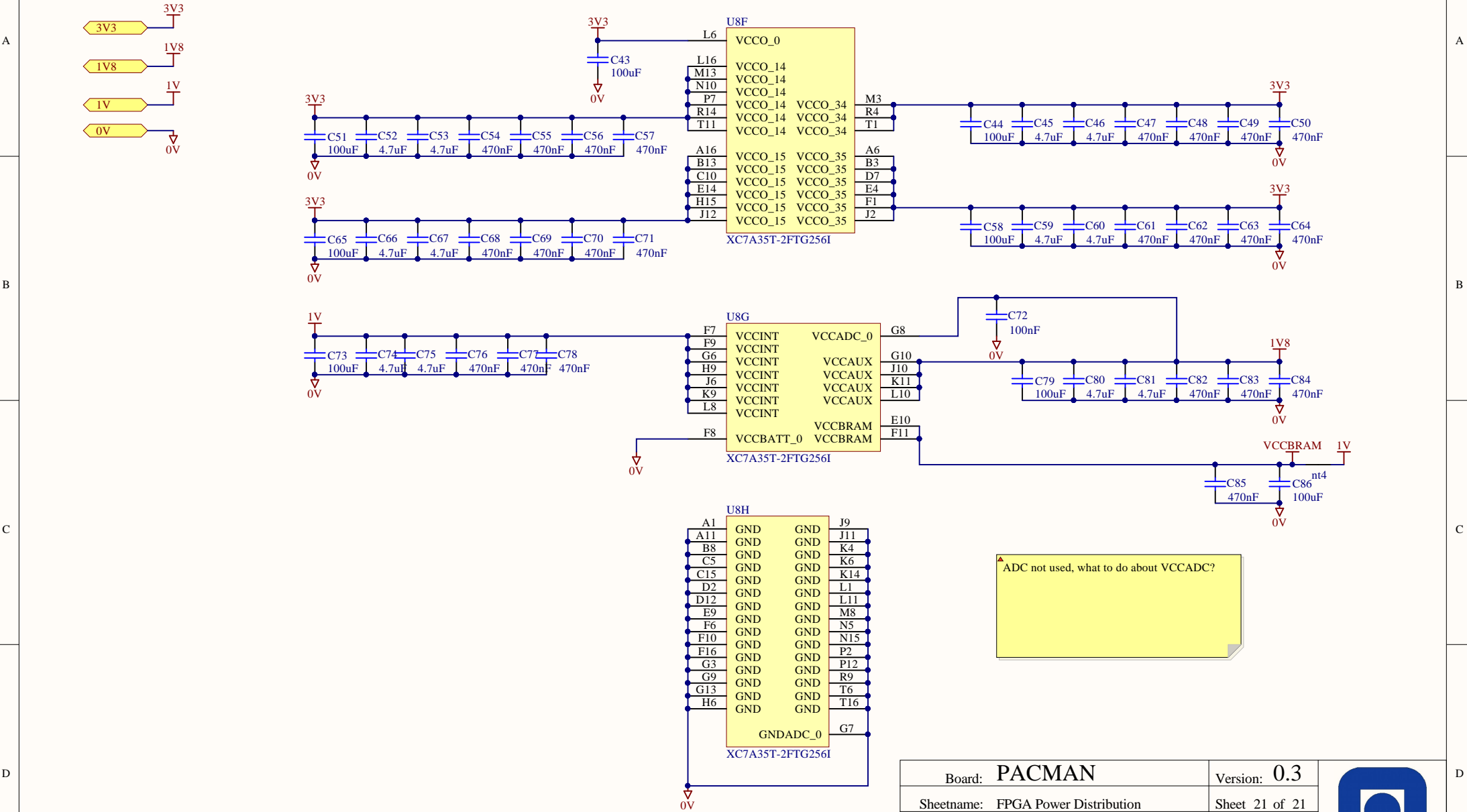
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Board:	PACMAN	Version:	0.3
Sheetname:	FPGA Power Distribution	Sheet	21 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Schematic file: XC7A35TFTG256_power.SchDoc			