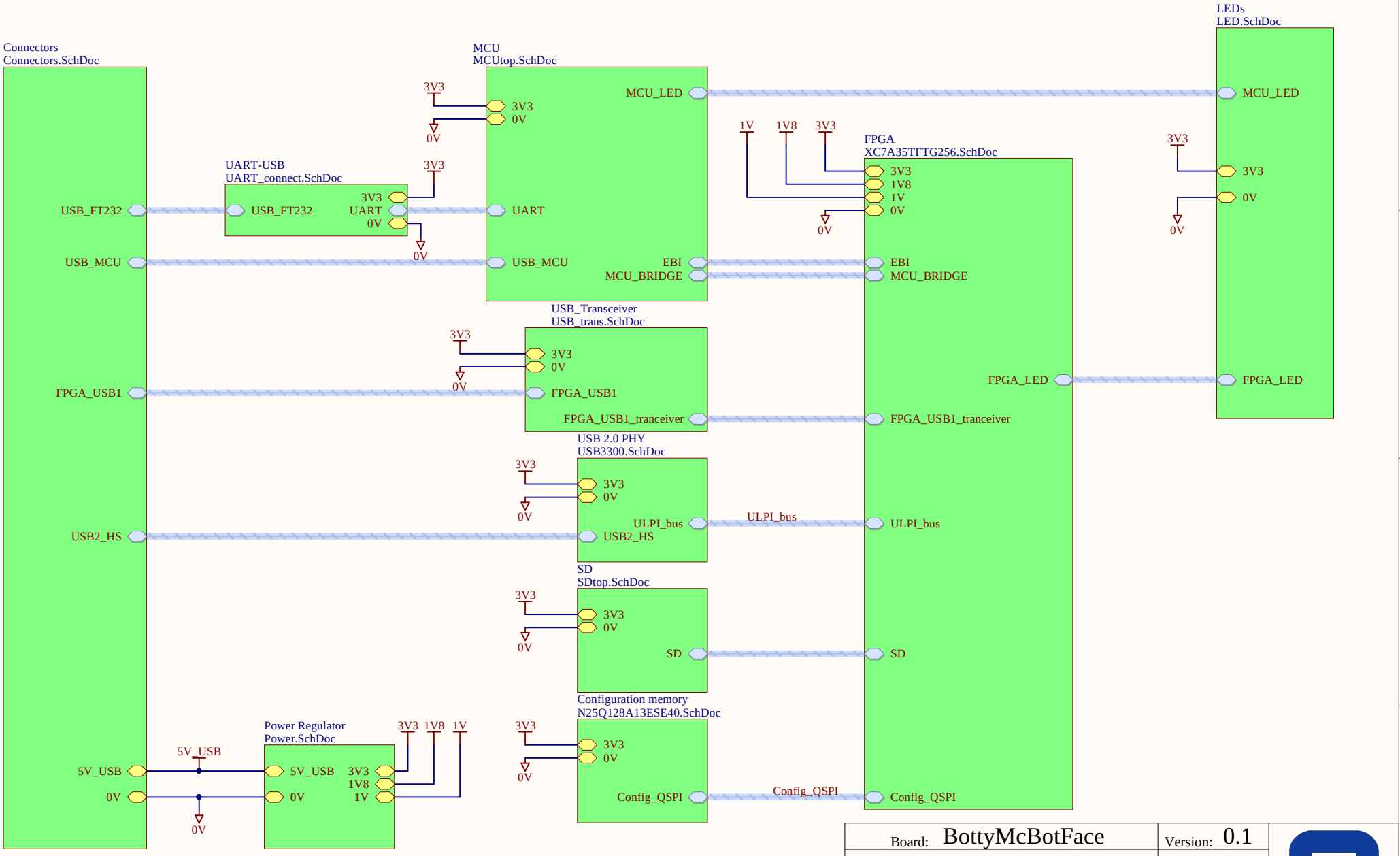
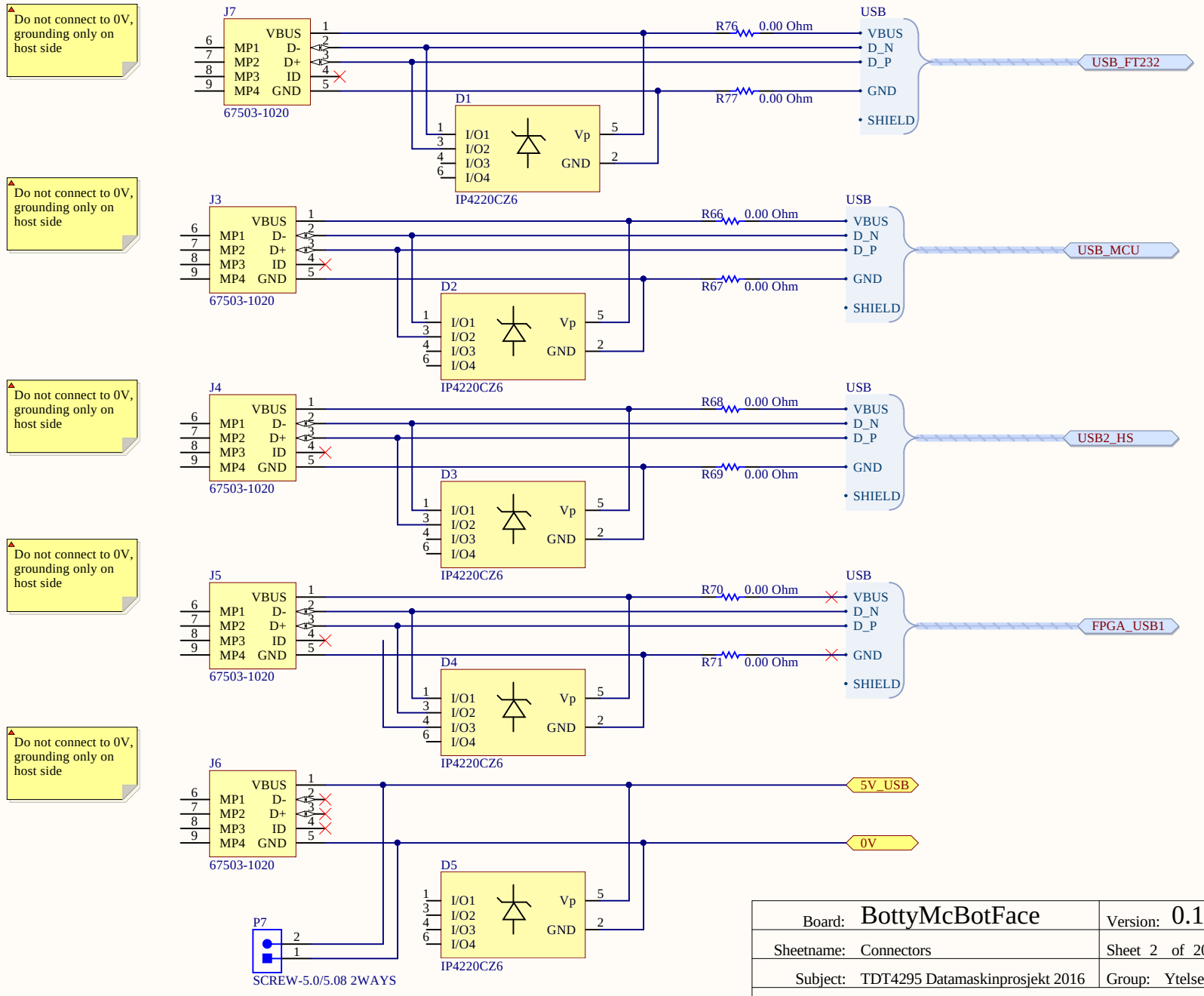
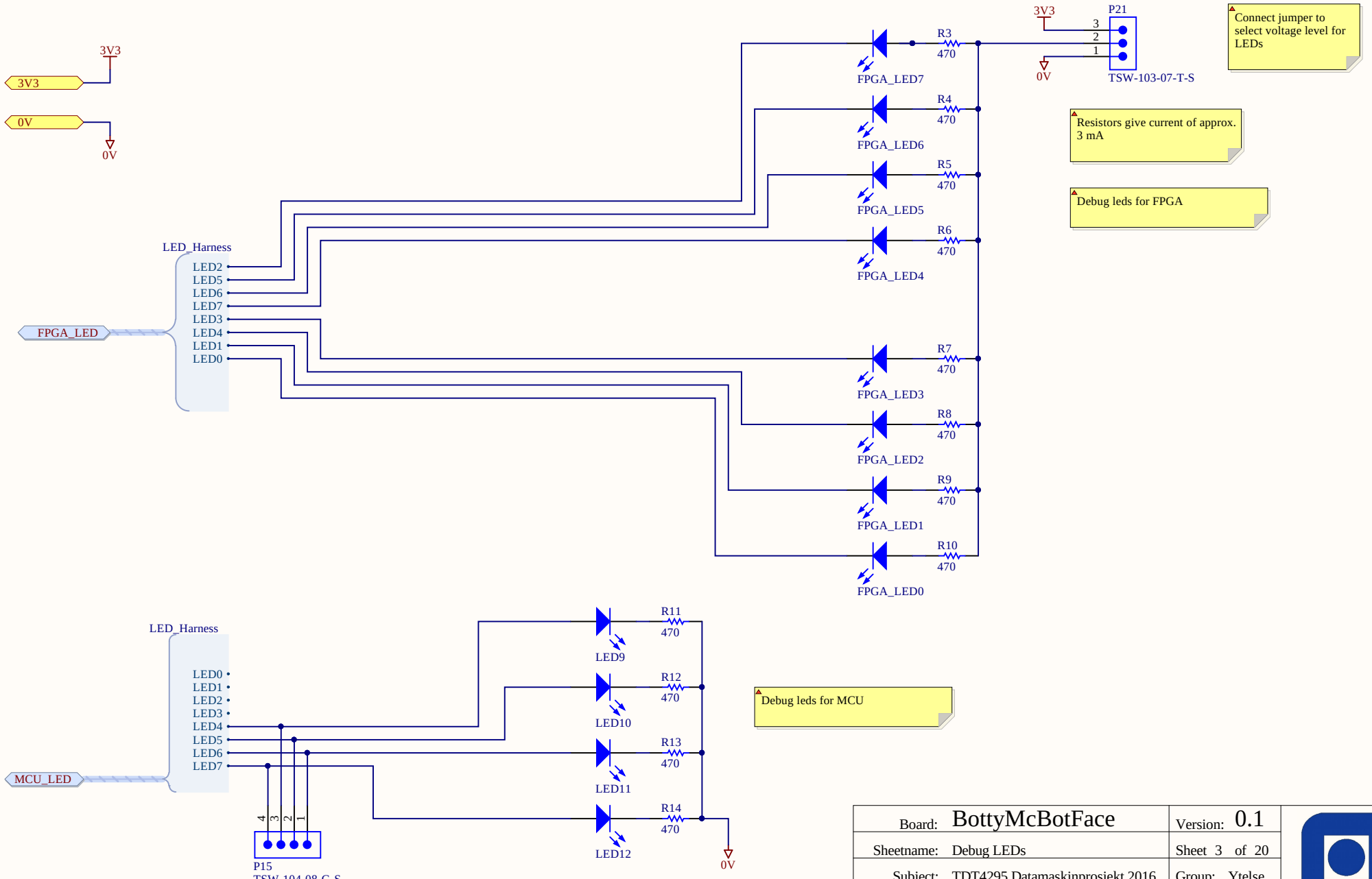
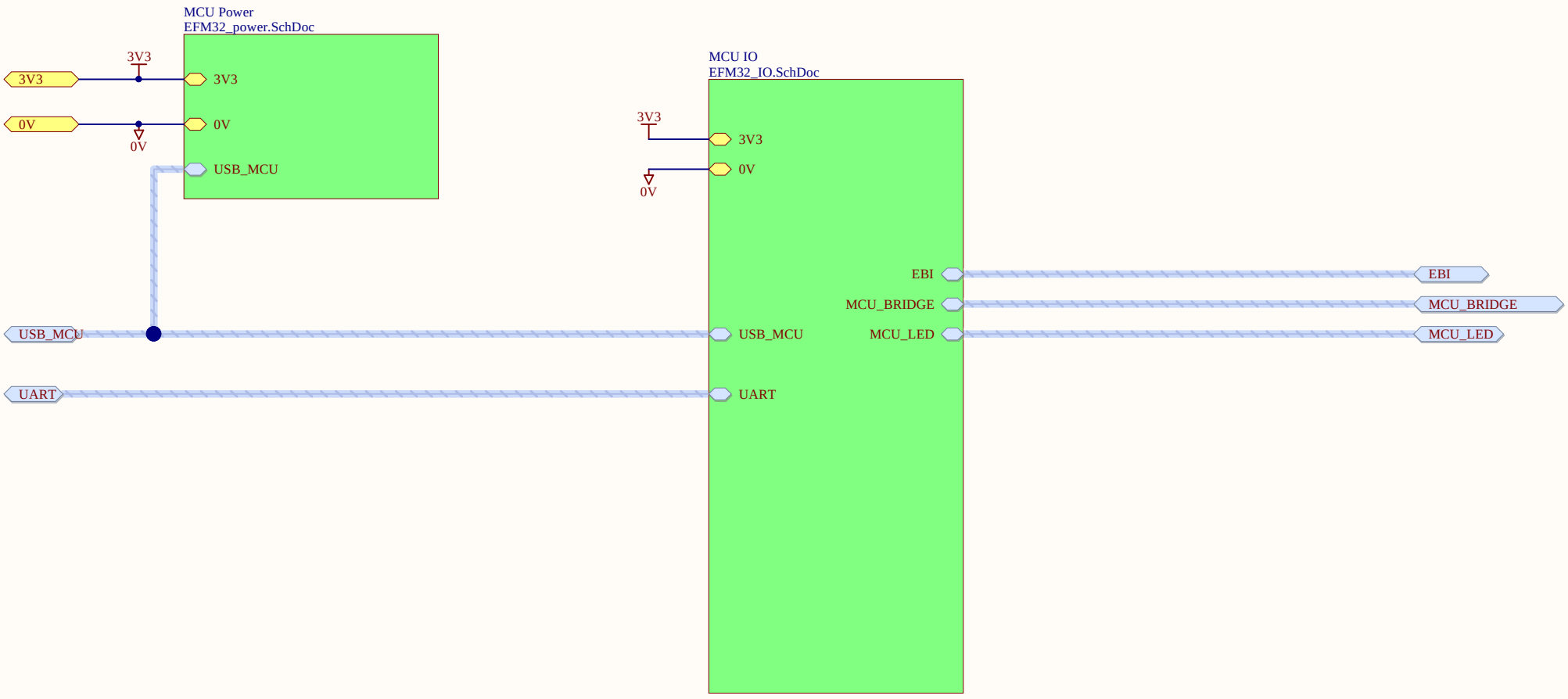


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Top level	Sheet	1 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	main.SchDoc		

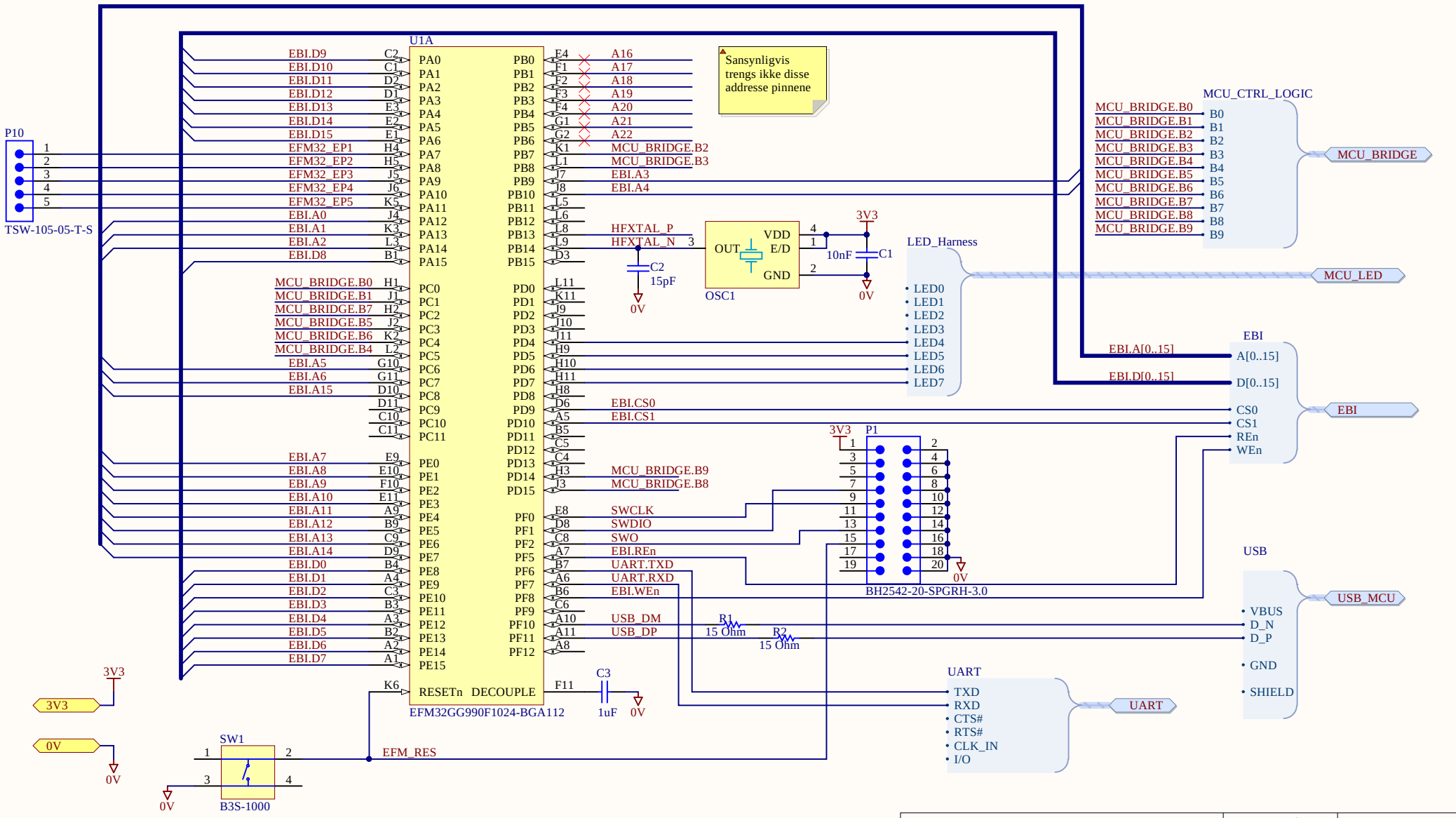

Do not connect to 0V, grounding only on host side
Do not connect to 0V, grounding only on host side
Do not connect to 0V, grounding only on host side
Do not connect to 0V, grounding only on host side
Do not connect to 0V, grounding only on host side
J7
J3
J4
J5
J6
P7
VBUS
D-
D+
ID
GND
MP1
MP2
MP3
MP4
67503-1020
SCREW-5.0/5.08 2WAYS
D1
D2
D3
D4
D5
I/O1
I/O2
I/O3
I/O4
Vp
IP4220CZ6
R76
R77
R66
R67
R68
R69
R70
R71
0.00 Ohm
USB
D_N
D_P
SHIELD
USB_FT232
USB_MCU
USB2_HS
FPGA_USB1
5V_USB
0V
Board: BottyMcBotFace
Version: 0.1
Sheetname: Connectors
Sheet 2 of 20
Subject: TDT4295 Datamaskinprosjekt 2016
Group: Ytelse
Shematic file: Connectors.SchDoc

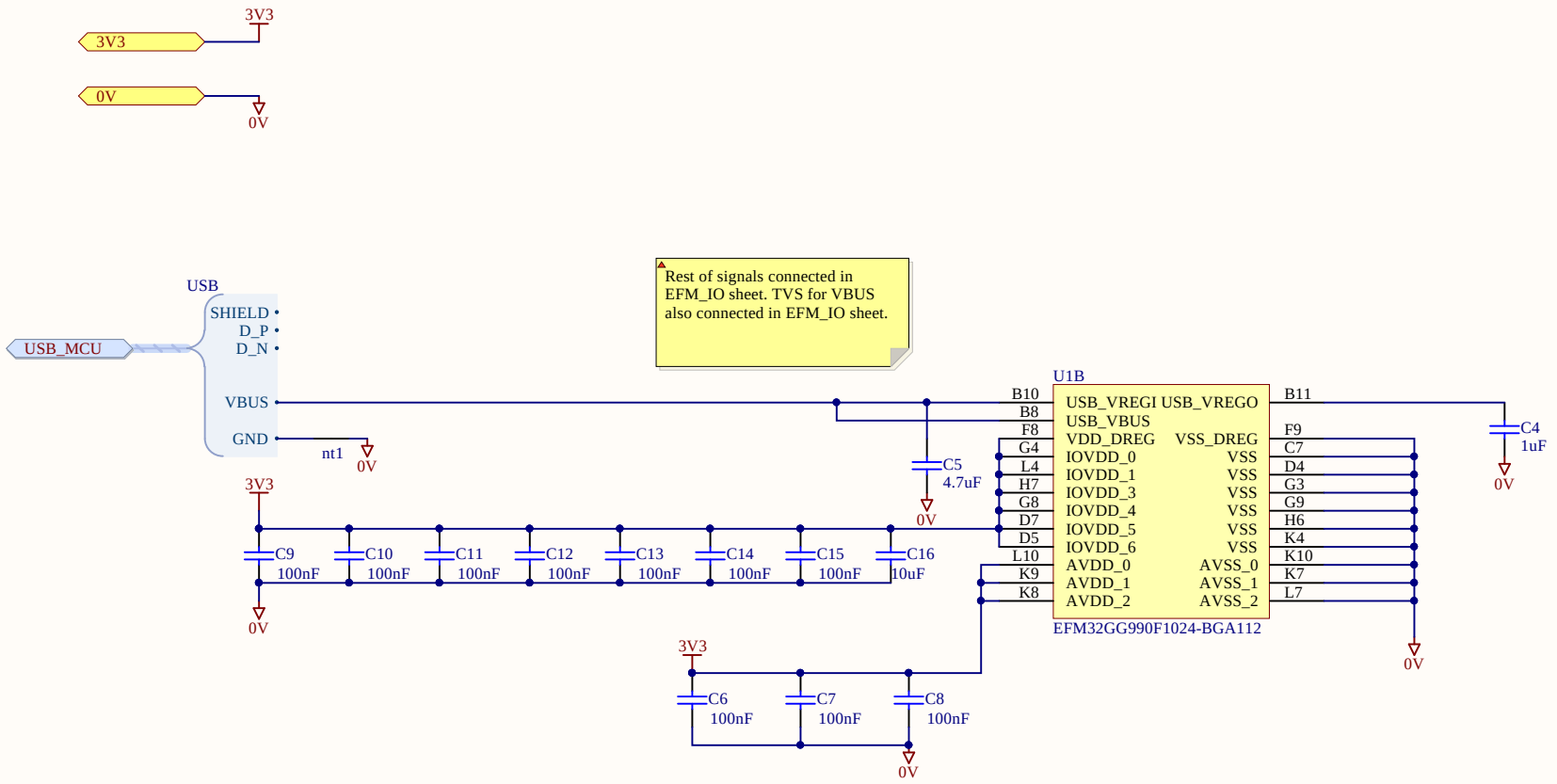


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Debug LEDs	Sheet	3 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	LED.SchDoc		

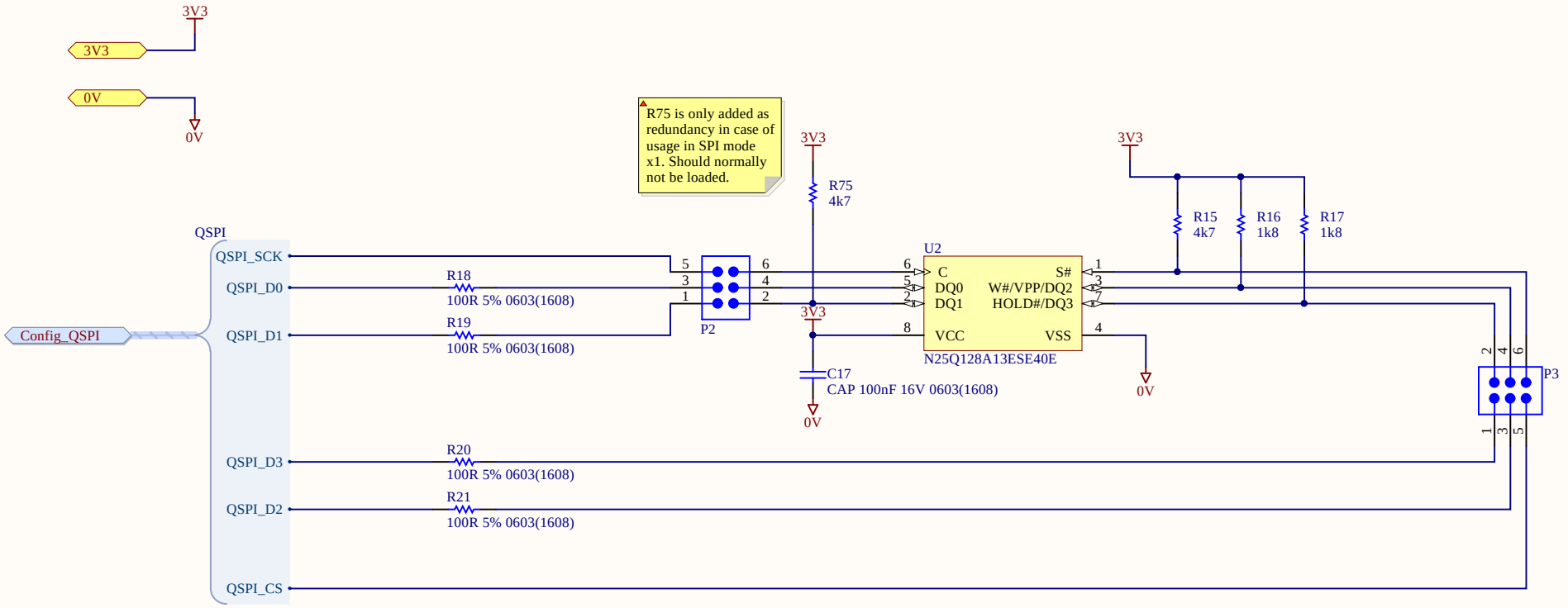


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Microcontroller Top Level	Sheet	4 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	MCUtop.SchDoc		

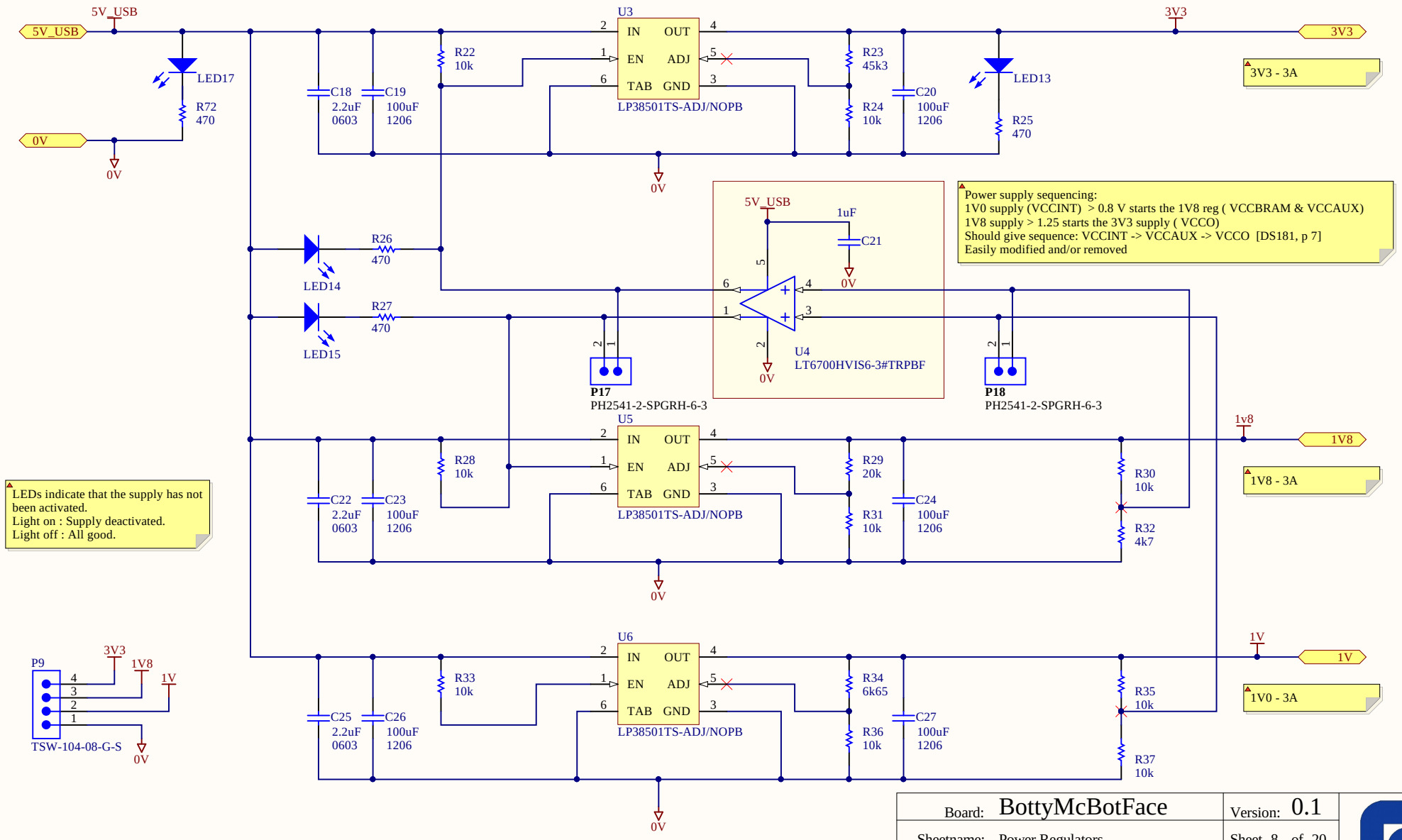

U1A
EFM32GG990F1024-BGA112
P10
TSW-105-05-T-S
Sansynligvis trengs ikke disse addresse pinnene
MCU_CTRL_LOGIC
MCU_BRIDGE
MCU_LED
LED_Harness
EBI
USB
USB_MCU
UART
OSC1
10nF
C1
C2
15pF
C3
1uF
R1
15 Ohm
R2
15 Ohm
P1
BH2542-20-SPGRH-3.0
SW1
B3S-1000
3V3
0V
EFM_RES
Board: BottyMcBotFace
Version: 0.1
Sheetname: Microcontroller IO
Sheet 5 of 20
Subject: TDT4295 Datamaskinprosjekt 2016
Group: Ytelse
Shematic file: EFM32_IO.SchDoc



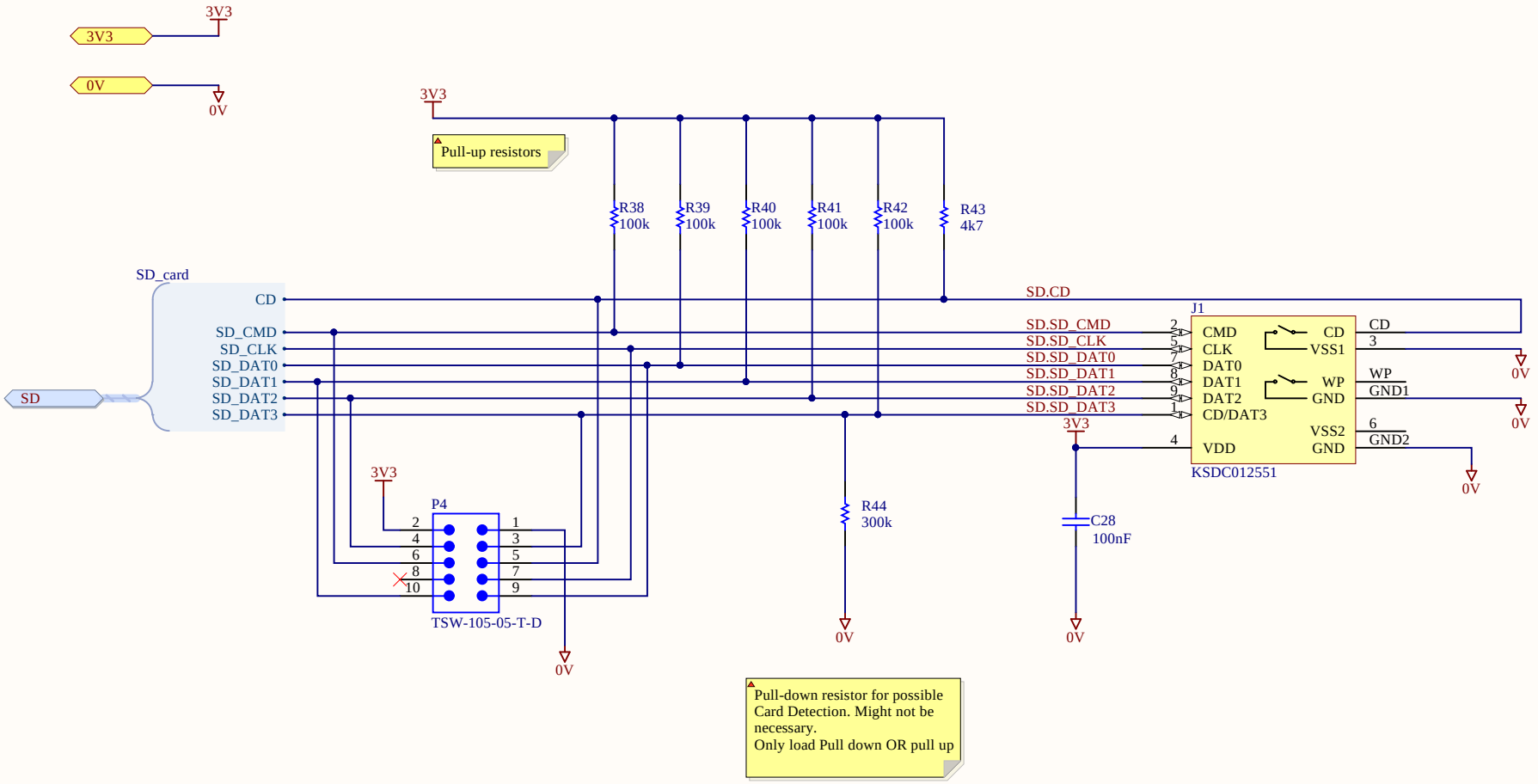
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Microcontroller Power Distribution	Sheet	6 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	EFM32_power.SchDoc		



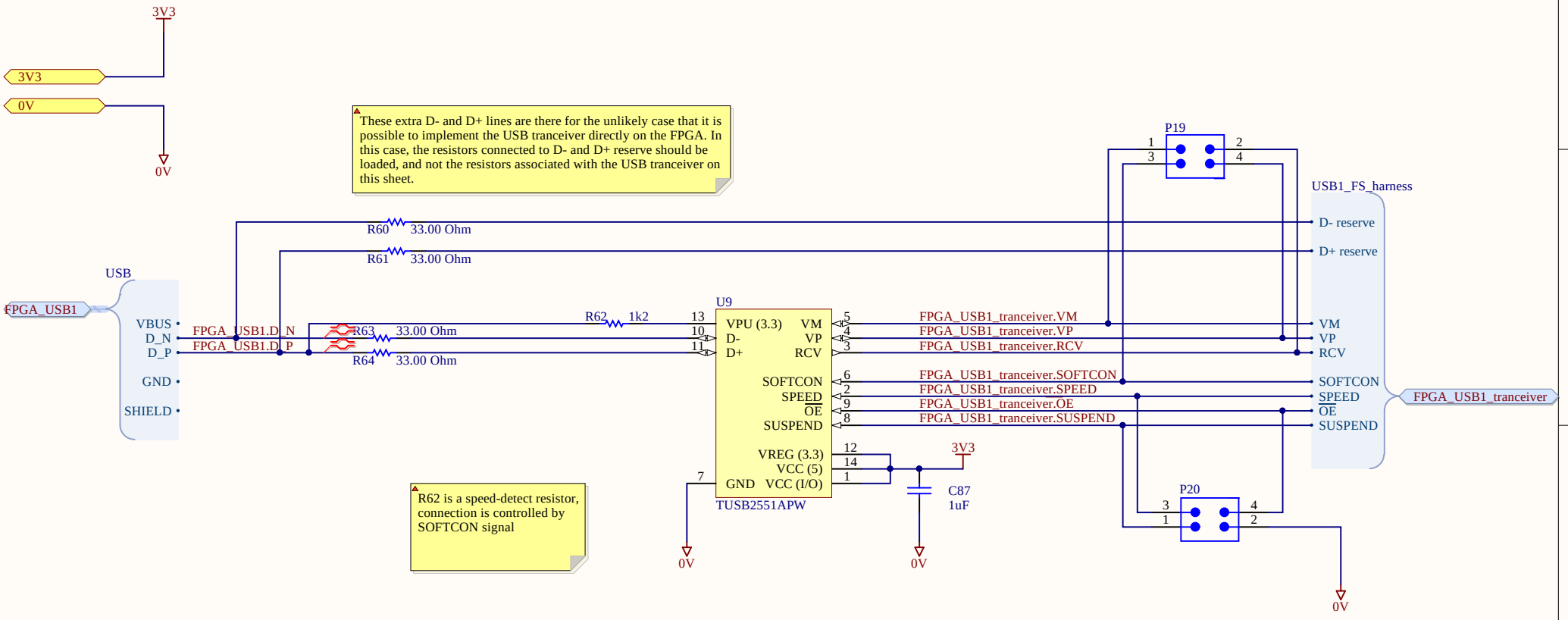
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Configuration Memory	Sheet	7 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	N25Q128A13ESE40.SchDoc		



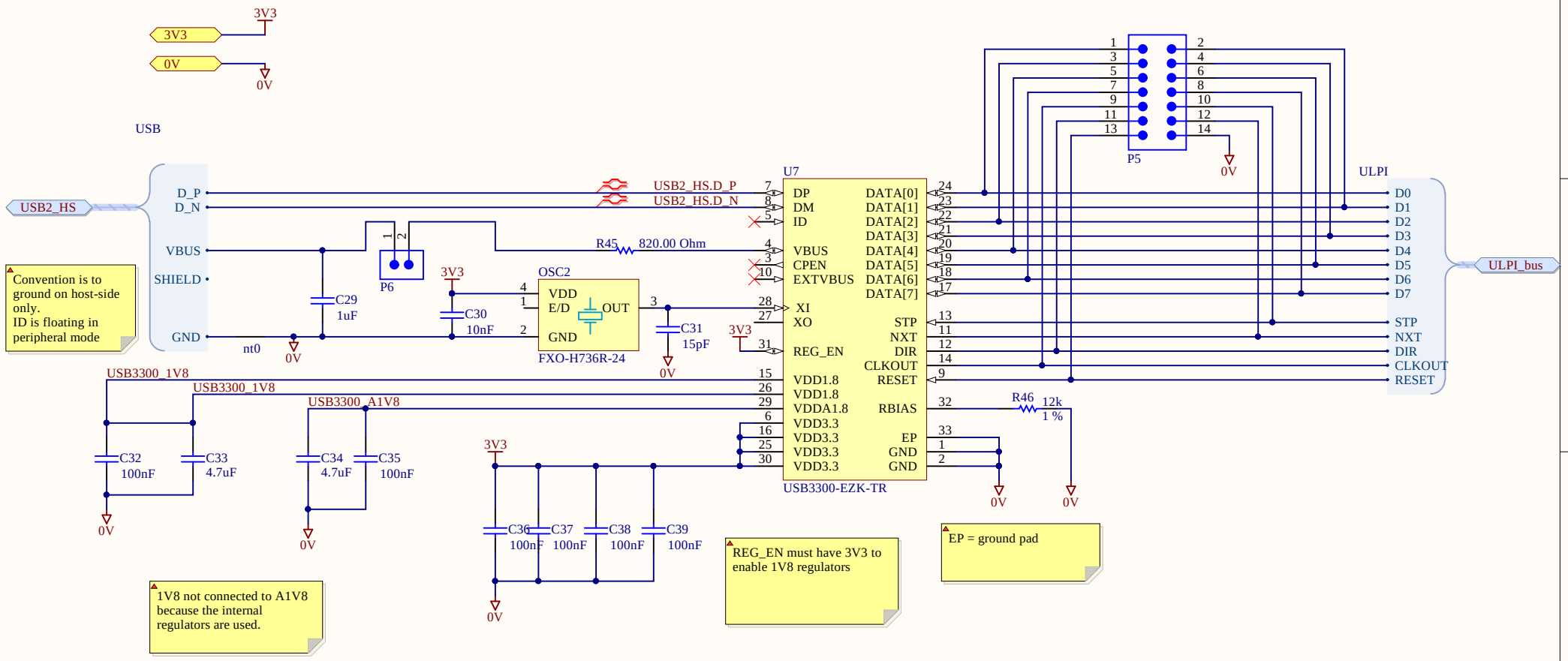
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	Power Regulators	Sheet	8 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	Power.SchDoc		



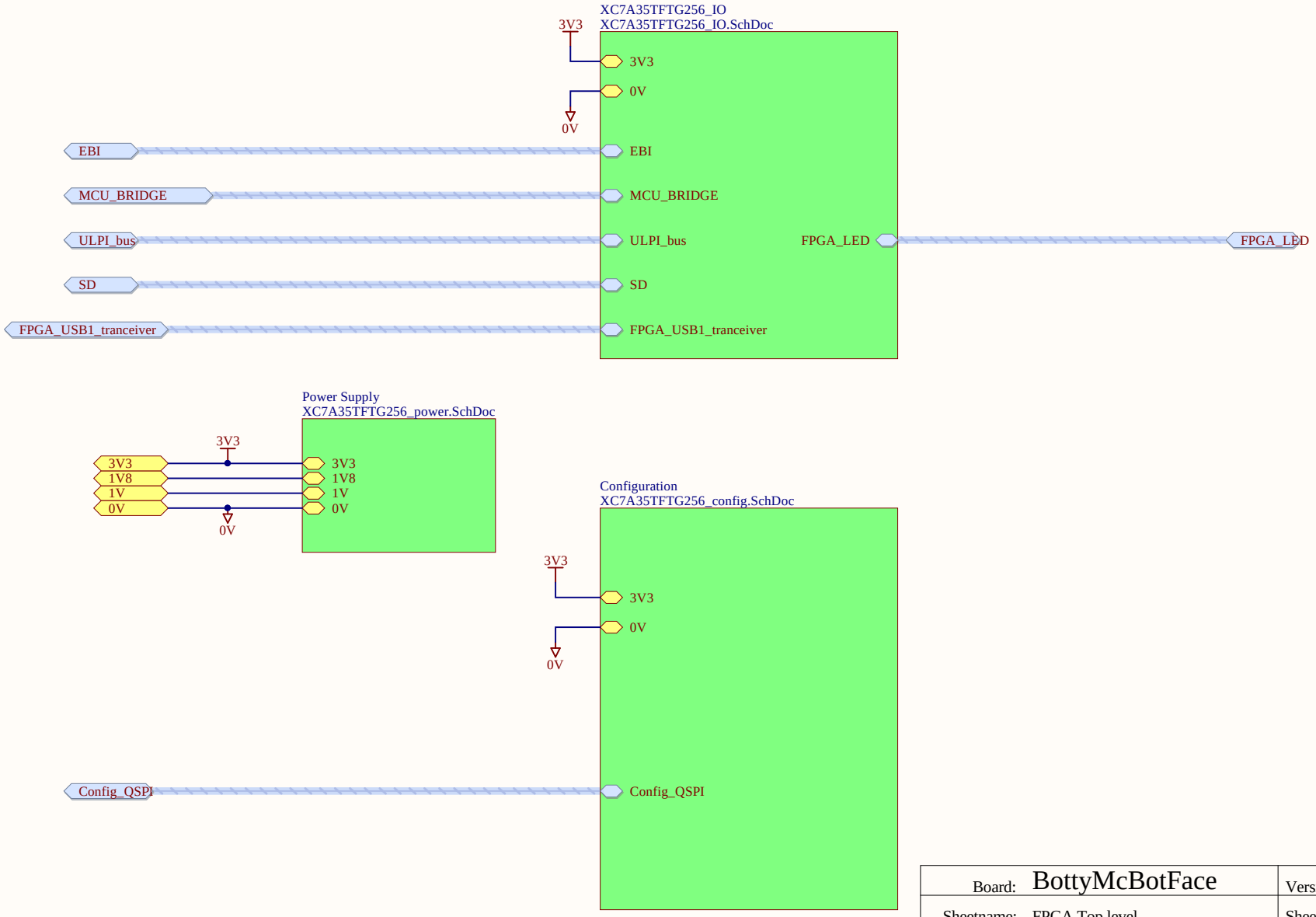
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	SD Card	Sheet	9 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	SDtop.SchDoc		



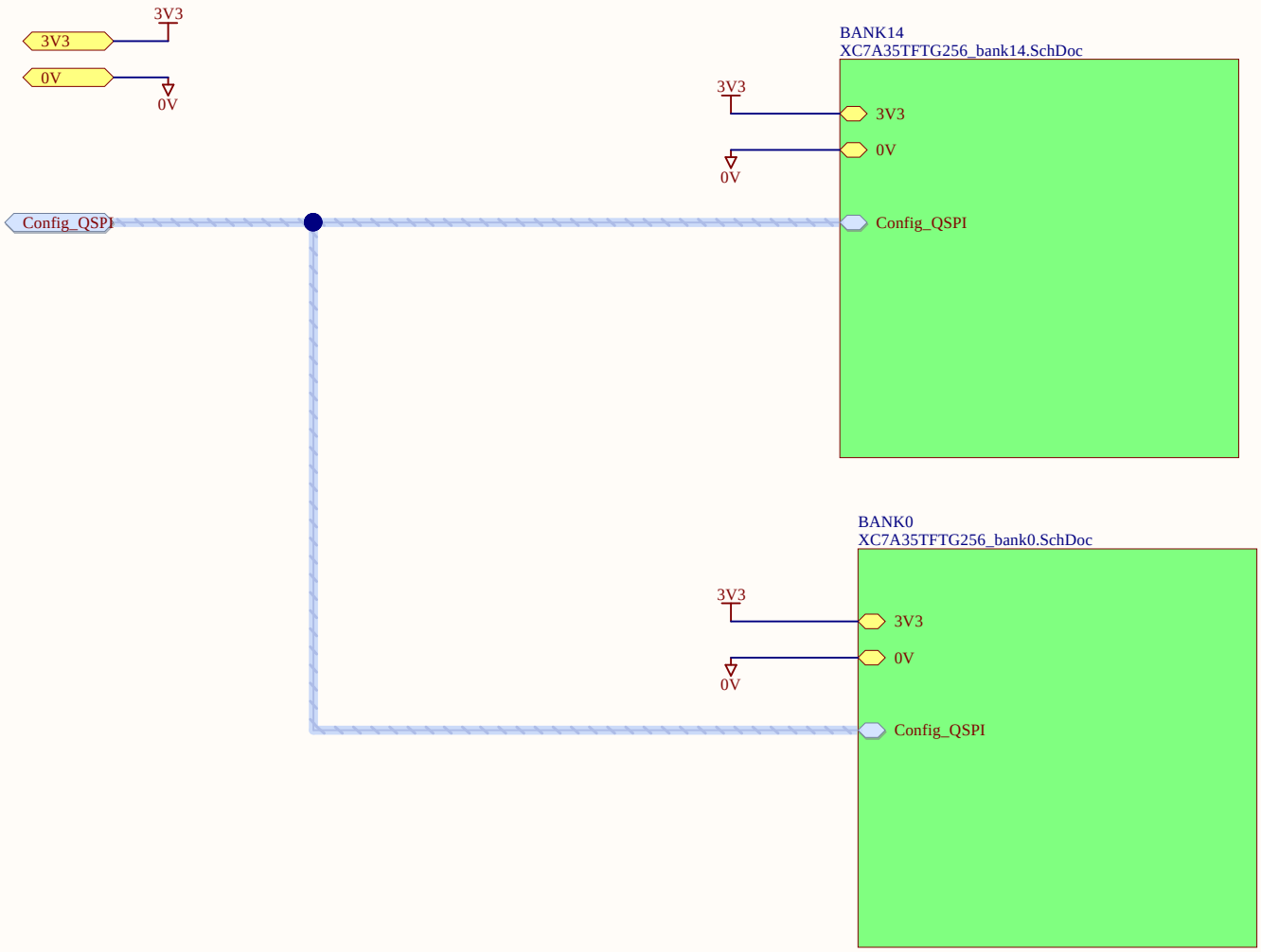
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	USB Full Speed tranceiver	Sheet	10 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	USB_trans.SchDoc		



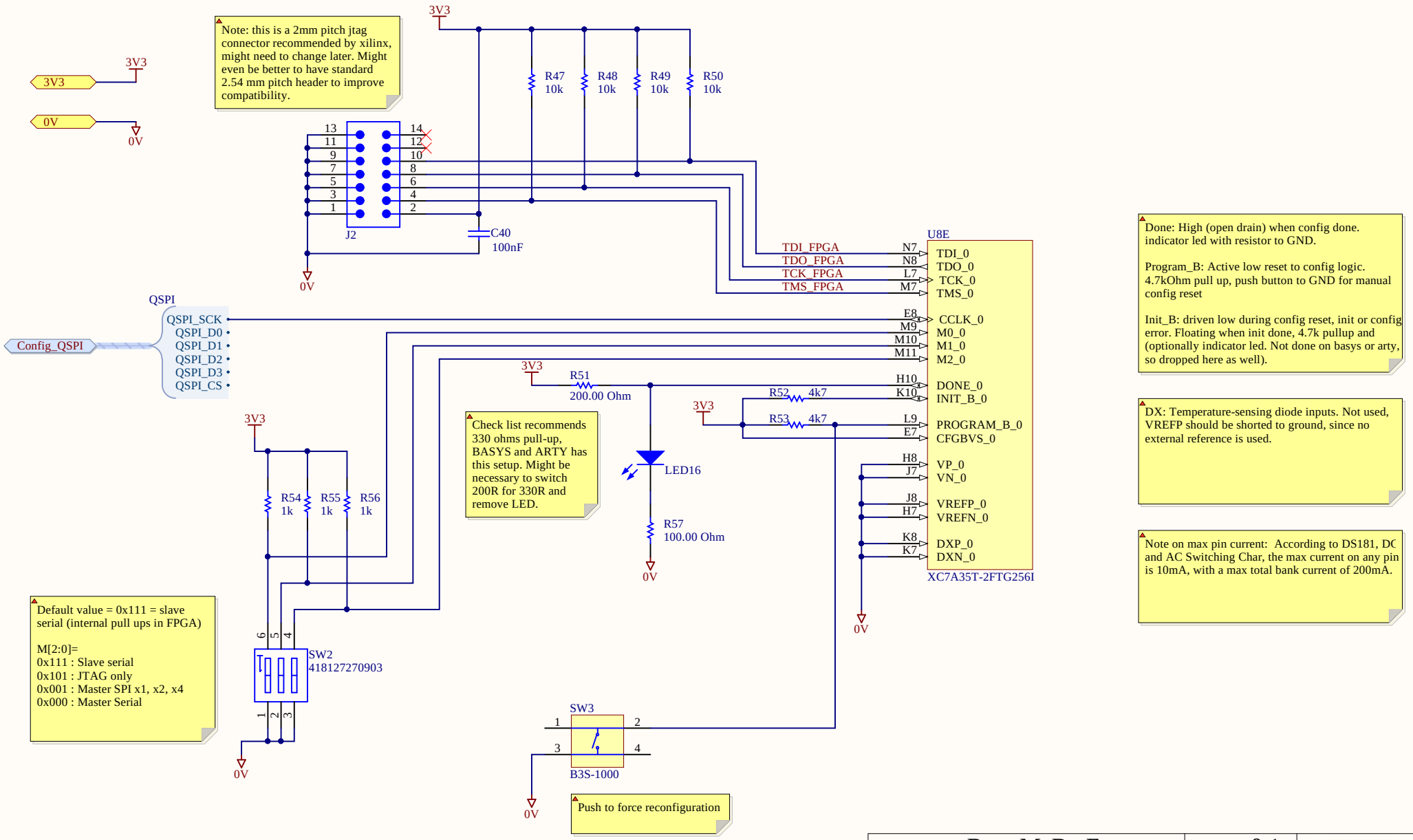
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	USB 2.0 HS PHY	Sheet	11 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	USB3300.SchDoc		

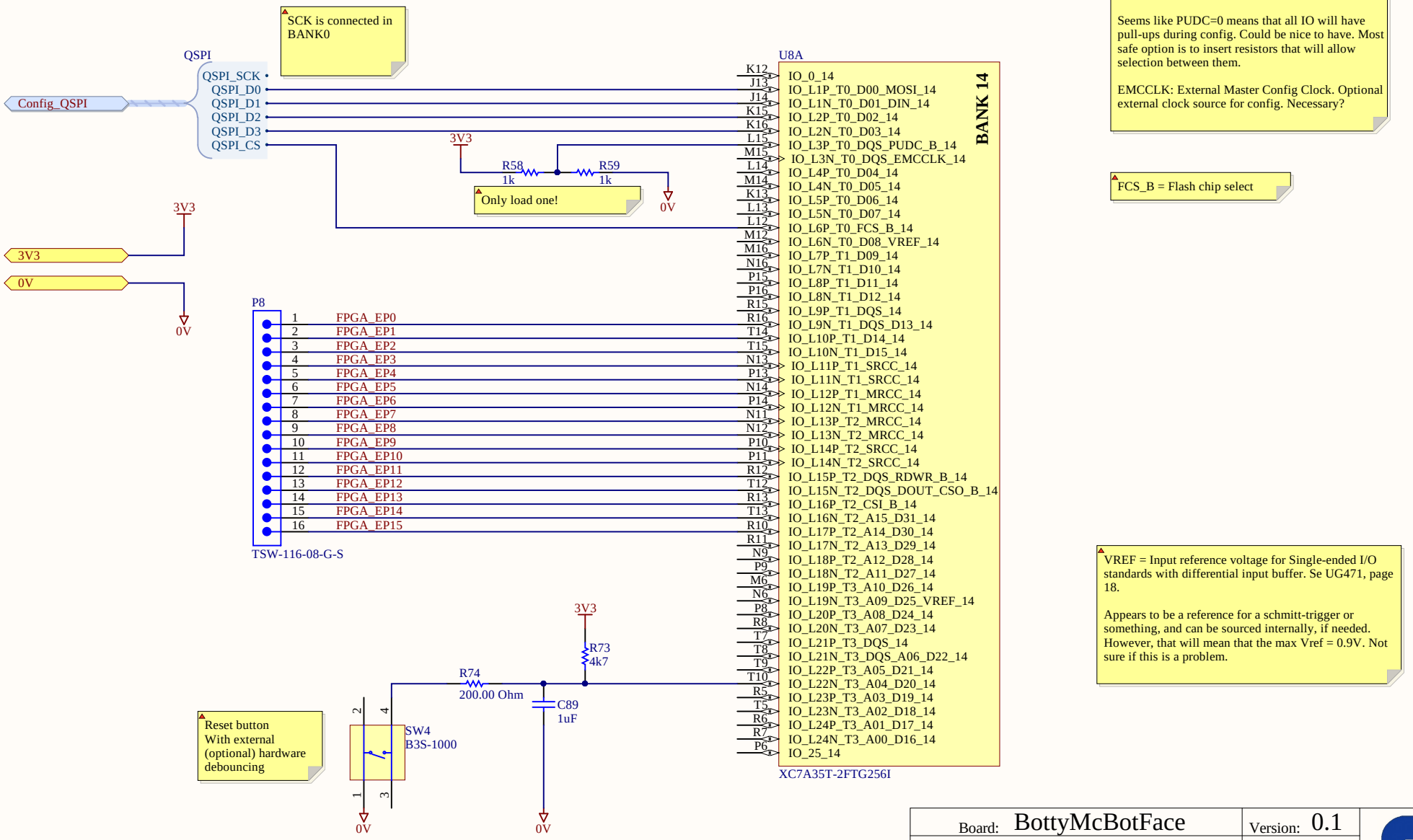


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Top level	Sheet	12 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256.SchDoc		

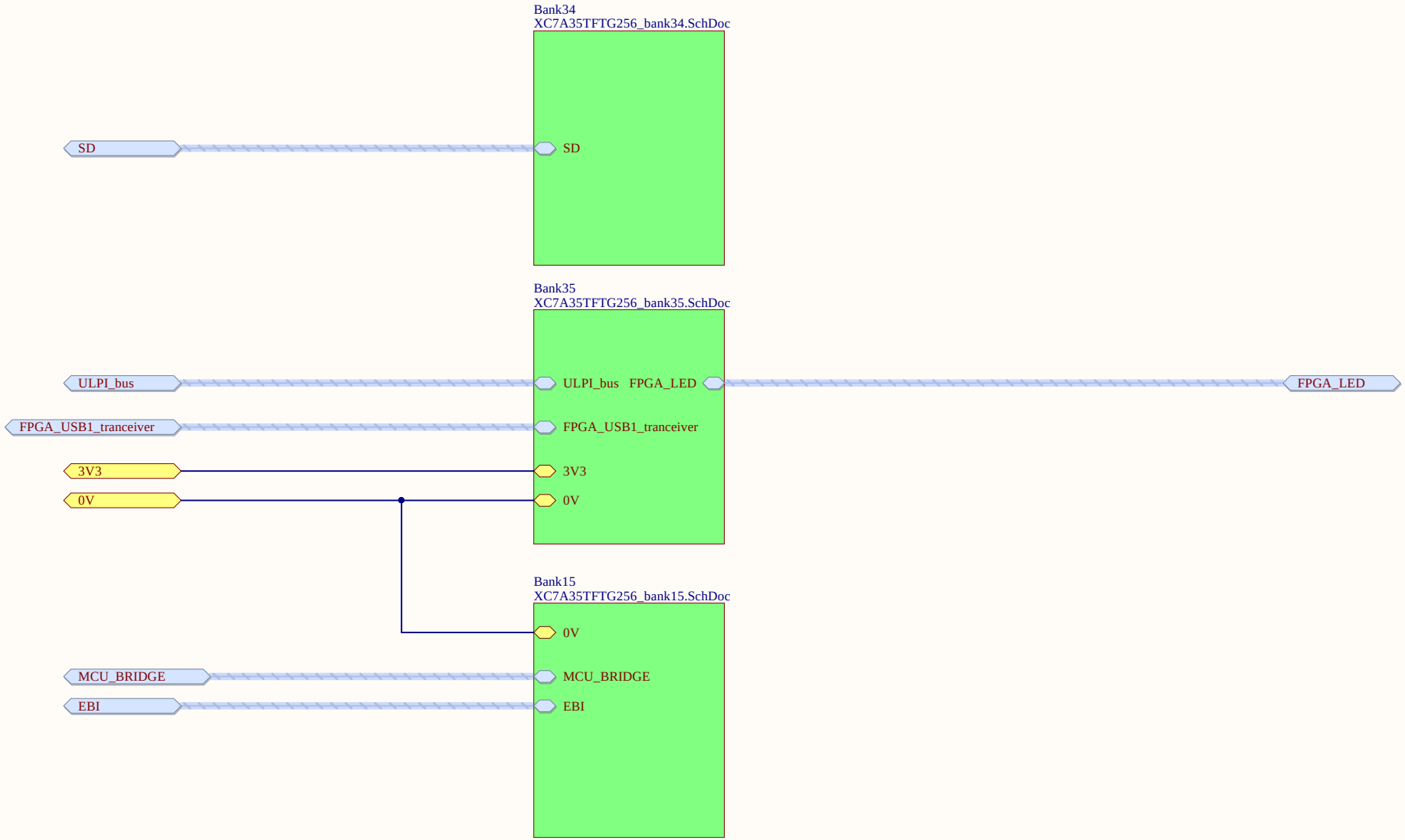


Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Configuration Top Level	Sheet	13 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_config.SchDoc		

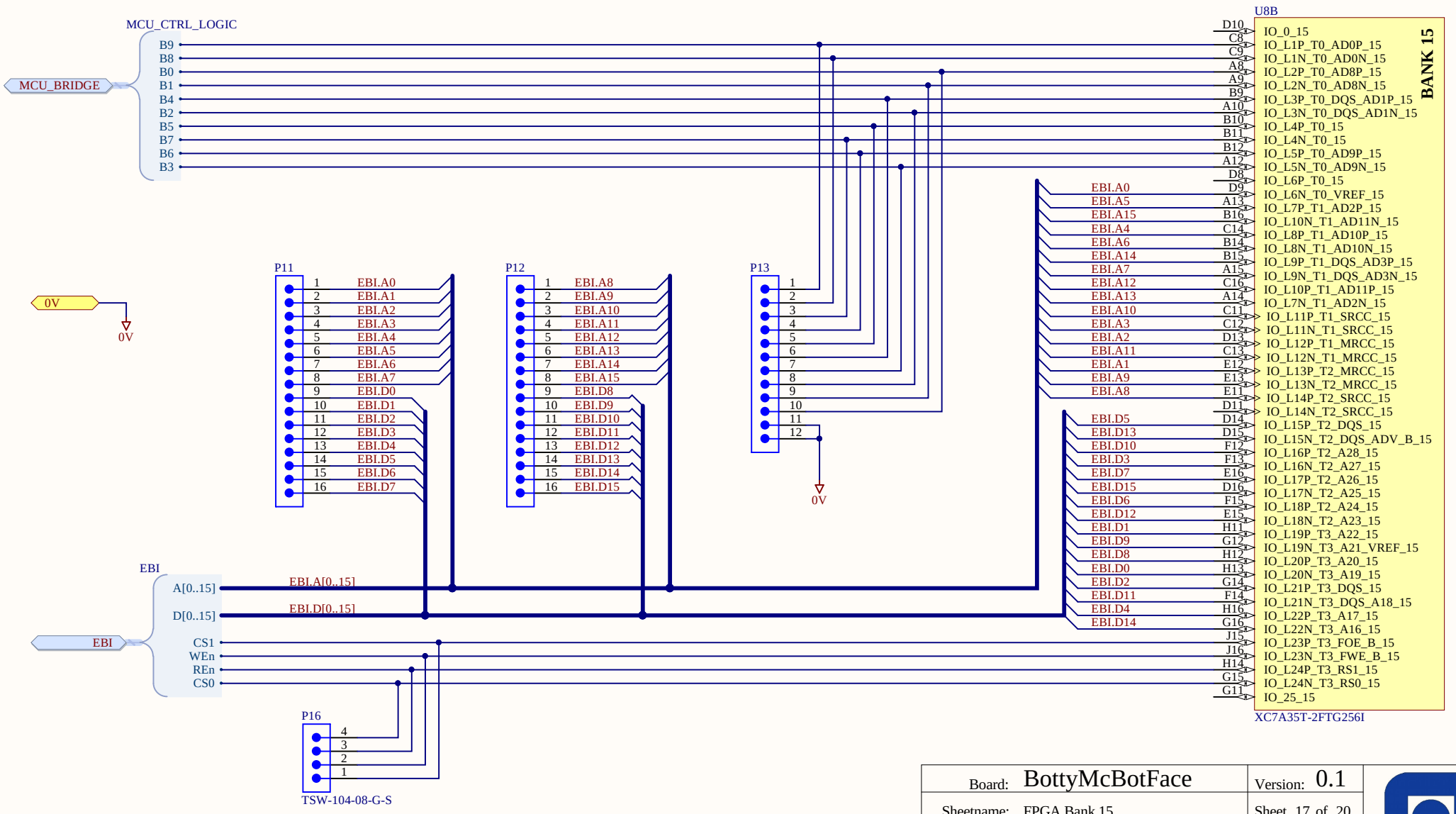

Note: this is a 2mm pitch jtag connector recommended by xilinx, might need to change later. Might even be better to have standard 2.54 mm pitch header to improve compatibility.
3V3
0V
R47 10k
R48 10k
R49 10k
R50 10k
J2
C40 100nF
U8E
TDI_FPGA
TDO_FPGA
TCK_FPGA
TMS_FPGA
TDI_0
TDO_0
TCK_0
TMS_0
QSPI
Config_QSPI
QSPI_SCK
QSPI_D0
QSPI_D1
QSPI_D2
QSPI_D3
QSPI_CS
CCLK_0
M0_0
M1_0
M2_0
R51 200.00 Ohm
R52 4k7
R53 4k7
DONE_0
INIT_B_0
PROGRAM_B_0
CFGBVS_0
VP_0
VN_0
VREFP_0
VREFN_0
DXP_0
DXN_0
XC7A35T-2FTG256I
Check list recommends 330 ohms pull-up, BASYS and ARTY has this setup. Might be necessary to switch 200R for 330R and remove LED.
LED16
R57 100.00 Ohm
R54 1k
R55 1k
R56 1k
SW2 418127270903
Default value = 0x111 = slave serial (internal pull ups in FPGA)
M[2:0]=
0x111 : Slave serial
0x101 : JTAG only
0x001 : Master SPI x1, x2, x4
0x000 : Master Serial
SW3
B3S-1000
Push to force reconfiguration
Done: High (open drain) when config done. indicator led with resistor to GND.
Program_B: Active low reset to config logic. 4.7kOhm pull up, push button to GND for manual config reset
Init_B: driven low during config reset, init or config error. Floating when init done, 4.7k pullup and (optionally indicator led. Not done on basys or arty, so dropped here as well).
DX: Temperature-sensing diode inputs. Not used, VREFP should be shorted to ground, since no external reference is used.
Note on max pin current: According to DS181, DC and AC Switching Char, the max current on any pin is 10mA, with a max total bank current of 200mA.
Board: BottyMcBotFace
Version: 0.1
Sheetname: FPGA Bank 0
Sheet 14 of 20
Subject: TDT4295 Datamaskinprosjekt 2016
Group: Ytelse
Shematic file: XC7A35TFTG256_bank0.SchDoc



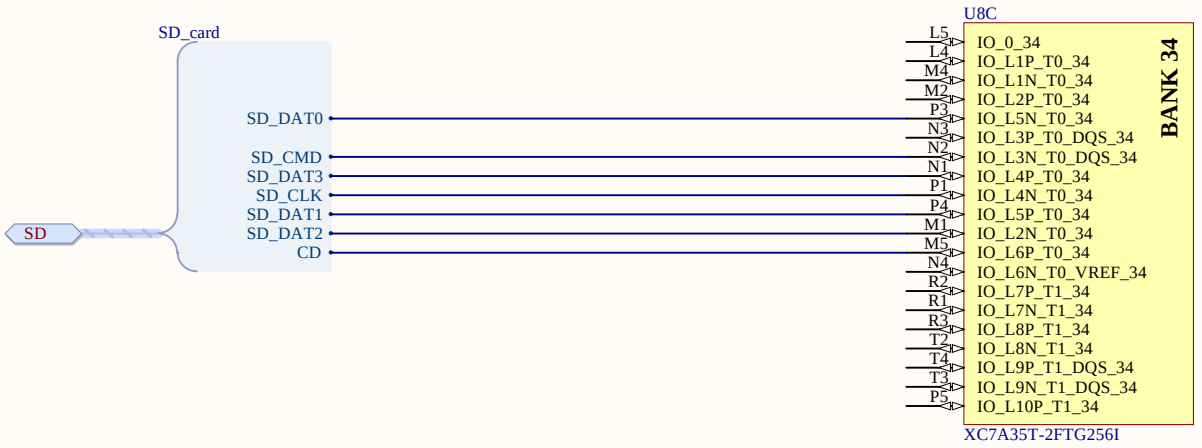
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Bank 14	Sheet	15 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank14.SchDoc		



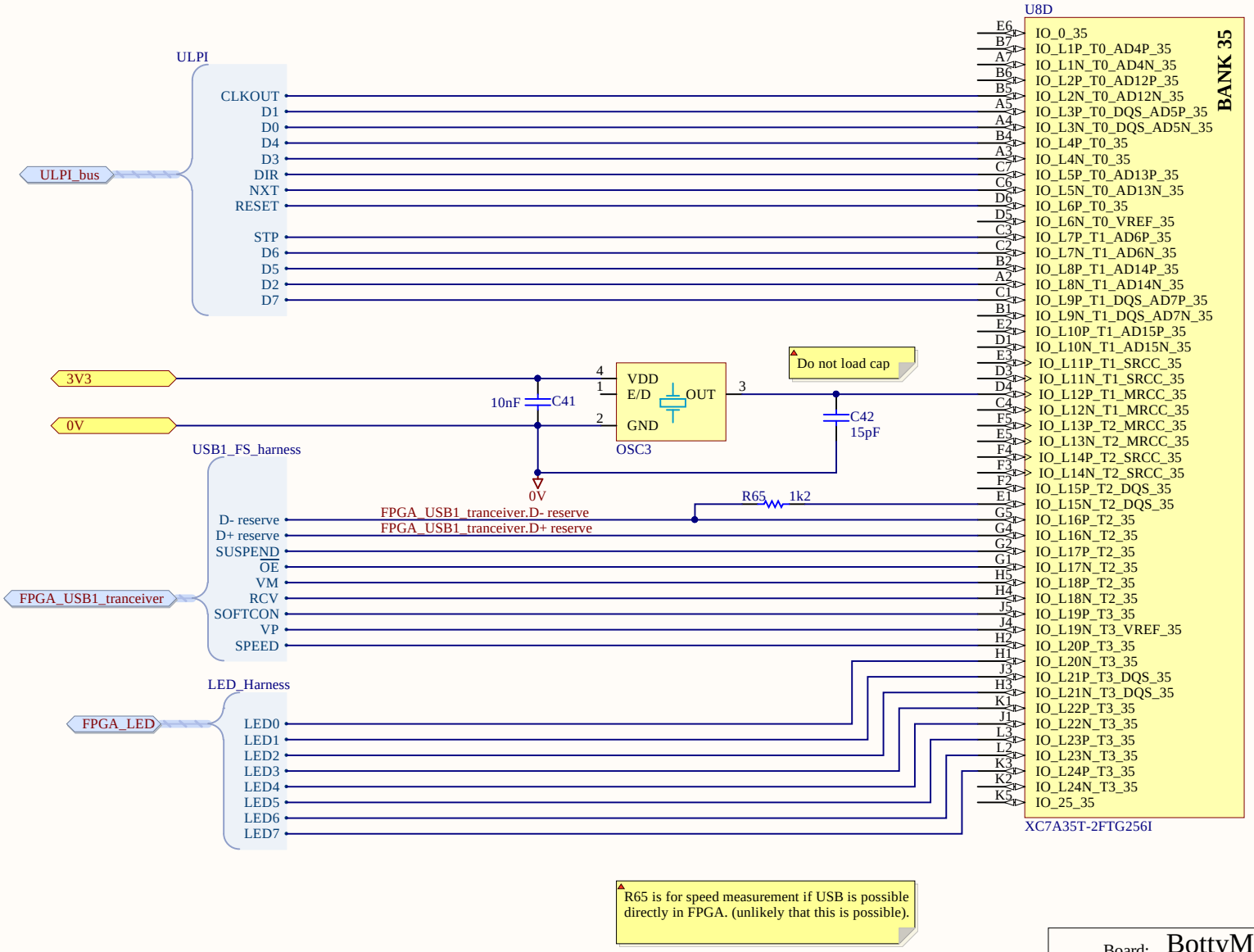
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA IO Top level	Sheet	16 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_IO.SchDoc		



Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Bank 15	Sheet	17 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank15.SchDoc		

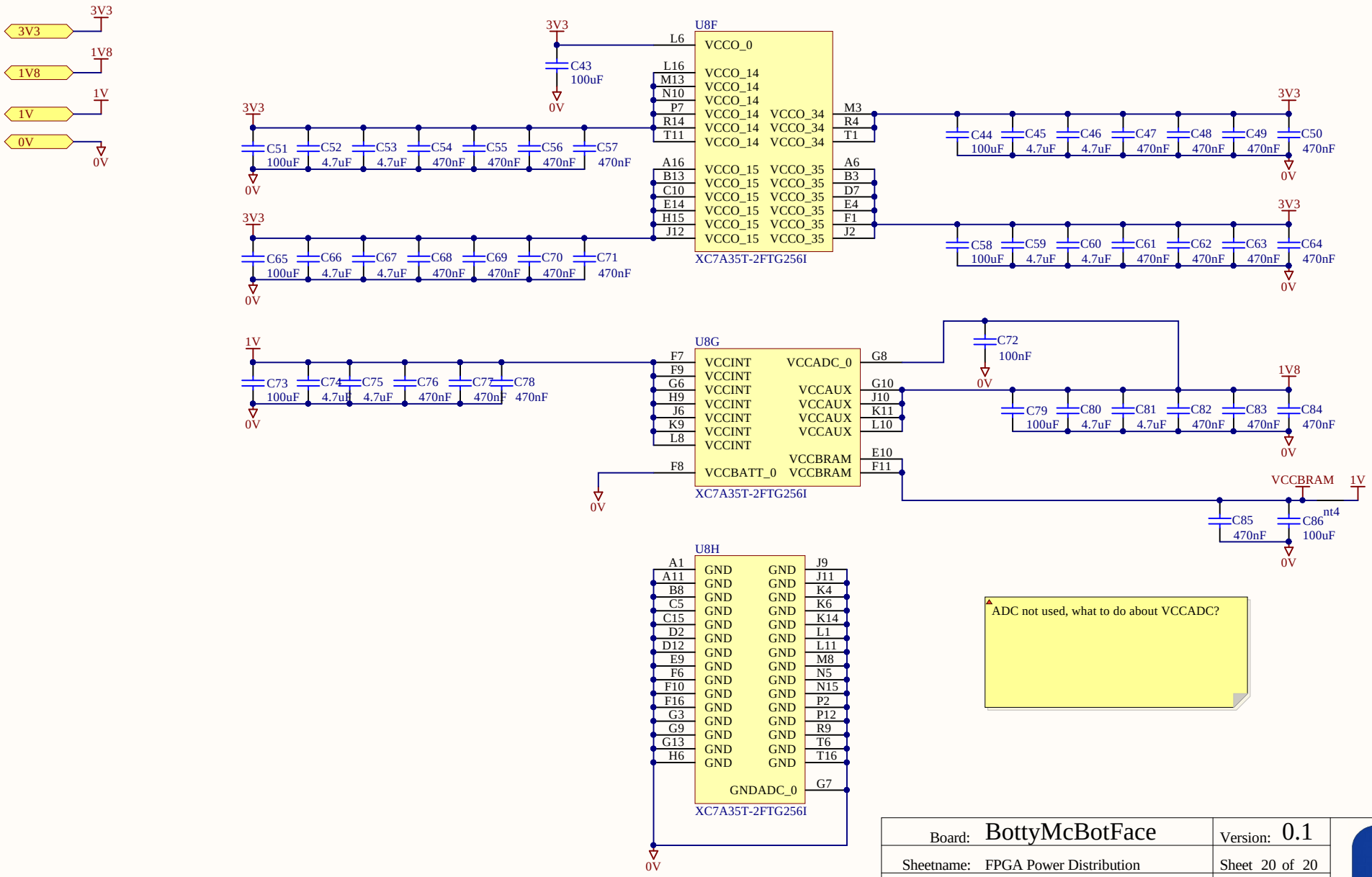


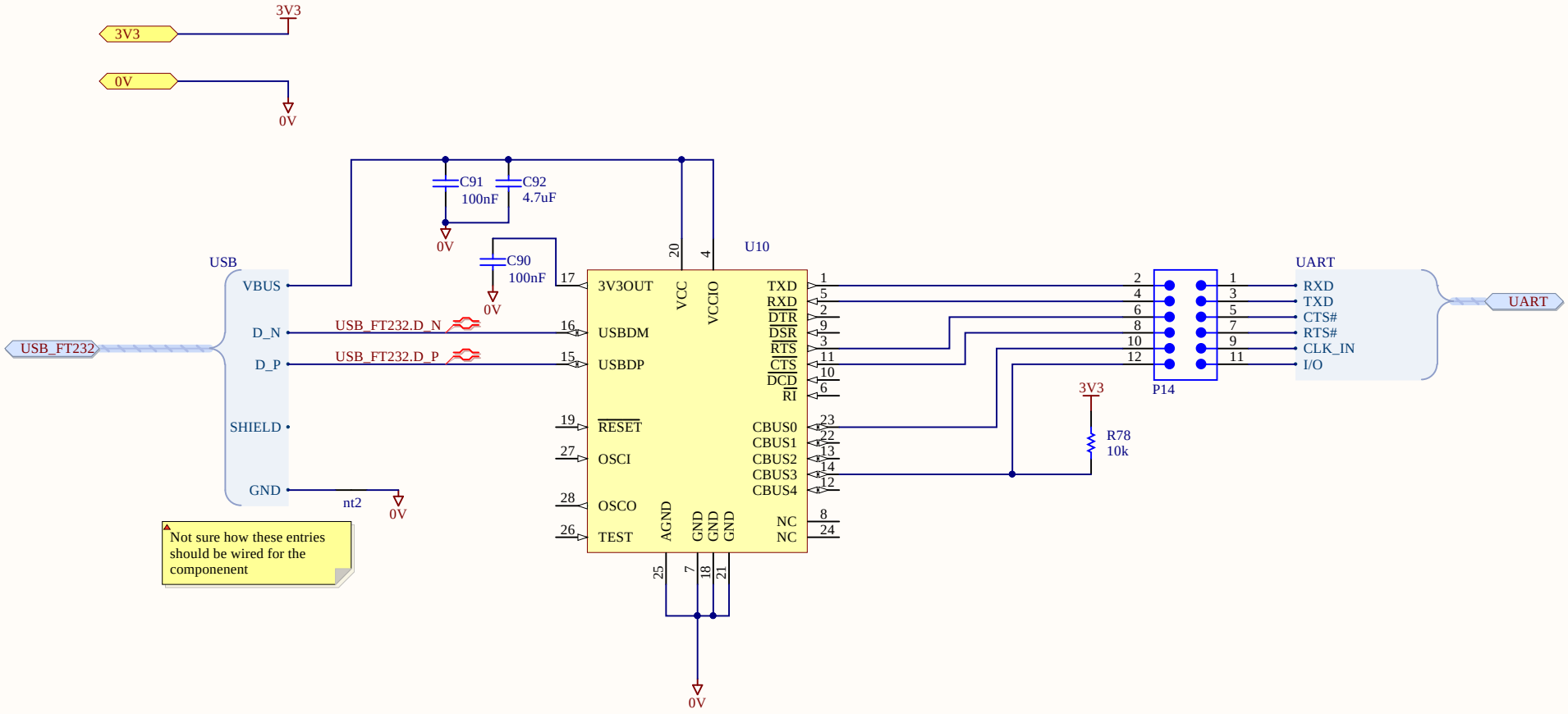
Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Bank 34	Sheet	18 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank34.SchDoc		



R65 is for speed measurement if USB is possible directly in FPGA. (unlikely that this is possible).

Board:	BottyMcBotFace	Version:	0.1
Sheetname:	FPGA Bank 35	Sheet	19 of 20
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank35.SchDoc		


3V3
1V8
1V
0V
U8F
VCCO_0
VCCO_14
VCCO_34
VCCO_15
VCCO_35
XC7A35T-2FTG256I
C43 100uF
C51 100uF
C52 4.7uF
C53 4.7uF
C54 470nF
C55 470nF
C56 470nF
C57 470nF
C44 100uF
C45 4.7uF
C46 4.7uF
C47 470nF
C48 470nF
C49 470nF
C50 470nF
C65 100uF
C66 4.7uF
C67 4.7uF
C68 470nF
C69 470nF
C70 470nF
C71 470nF
C58 100uF
C59 4.7uF
C60 4.7uF
C61 470nF
C62 470nF
C63 470nF
C64 470nF
U8G
VCCINT
VCCADC_0
VCCAUX
VCCBRAM
VCCBATT_0
C72 100nF
C73 100uF
C74 4.7uF
C75 4.7uF
C76 470nF
C77 470nF
C78 470nF
C79 100uF
C80 4.7uF
C81 4.7uF
C82 470nF
C83 470nF
C84 470nF
C85 470nF
C86 100uF
U8H
GND
GNDADC_0
ADC not used, what to do about VCCADC?
Board: BottyMcBotFace
Version: 0.1
Sheetname: FPGA Power Distribution
Sheet 20 of 20
Subject: TDT4295 Datamaskinprosjekt 2016
Group: Ytelse
Shematic file: XC7A35TFTG256_power.SchDoc



Title		
Size A4	Number	Revision
Date: 02.10.2016		Sheet of
File: C:\Users\..\UART_connect.SchDoc		Drawn By: