

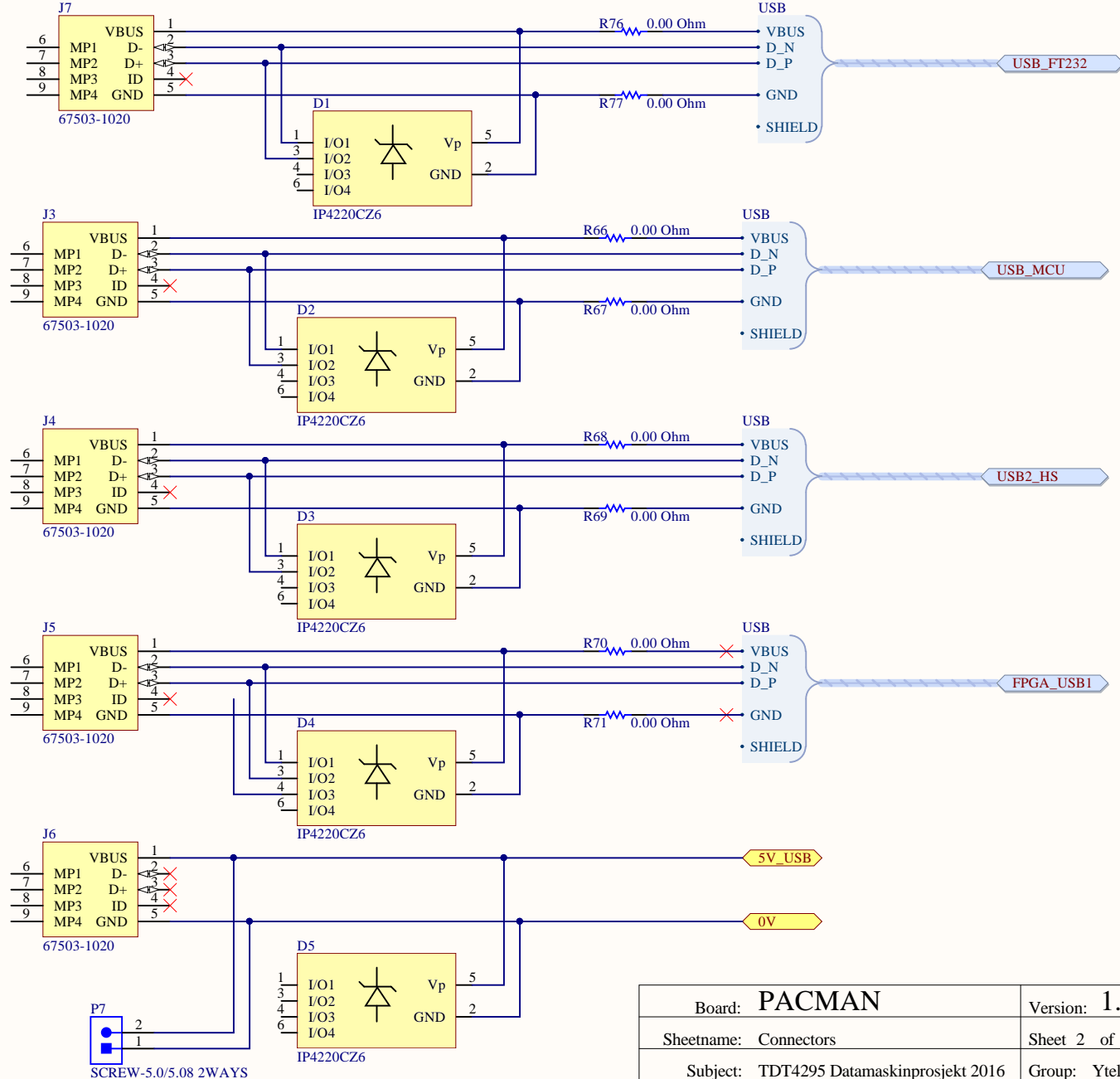
Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side

Do not connect to 0V,  
grounding only on  
host side



Board: PACMAN	Version: 1.0
Sheetname: Connectors	Sheet 2 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Shematic file: Connectors.SchDoc	



A

B

C

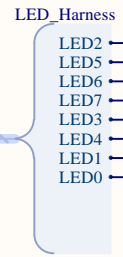
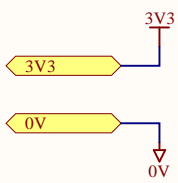
D

A

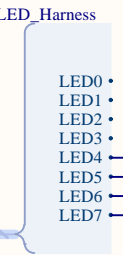
B

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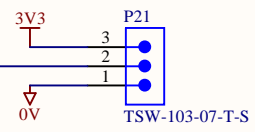
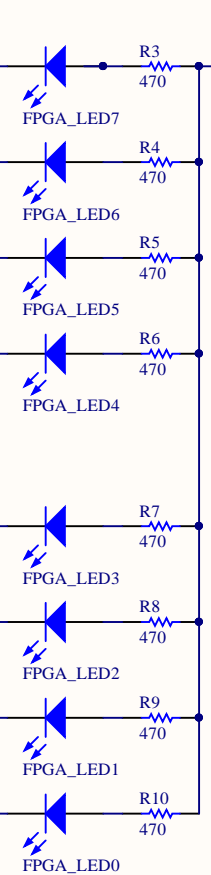
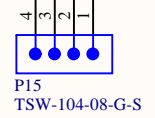
D



FPGA\_LED



MCU\_LED



Connect jumper to select voltage level for LEDs

Resistors give current of approx. 3 mA

Debug leds for FPGA

Debug leds for MCU

Board: PACMAN	Version: 1.0
Sheetname: Debug LEDs	Sheet 3 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Schematic file: LED.SchDoc	



A

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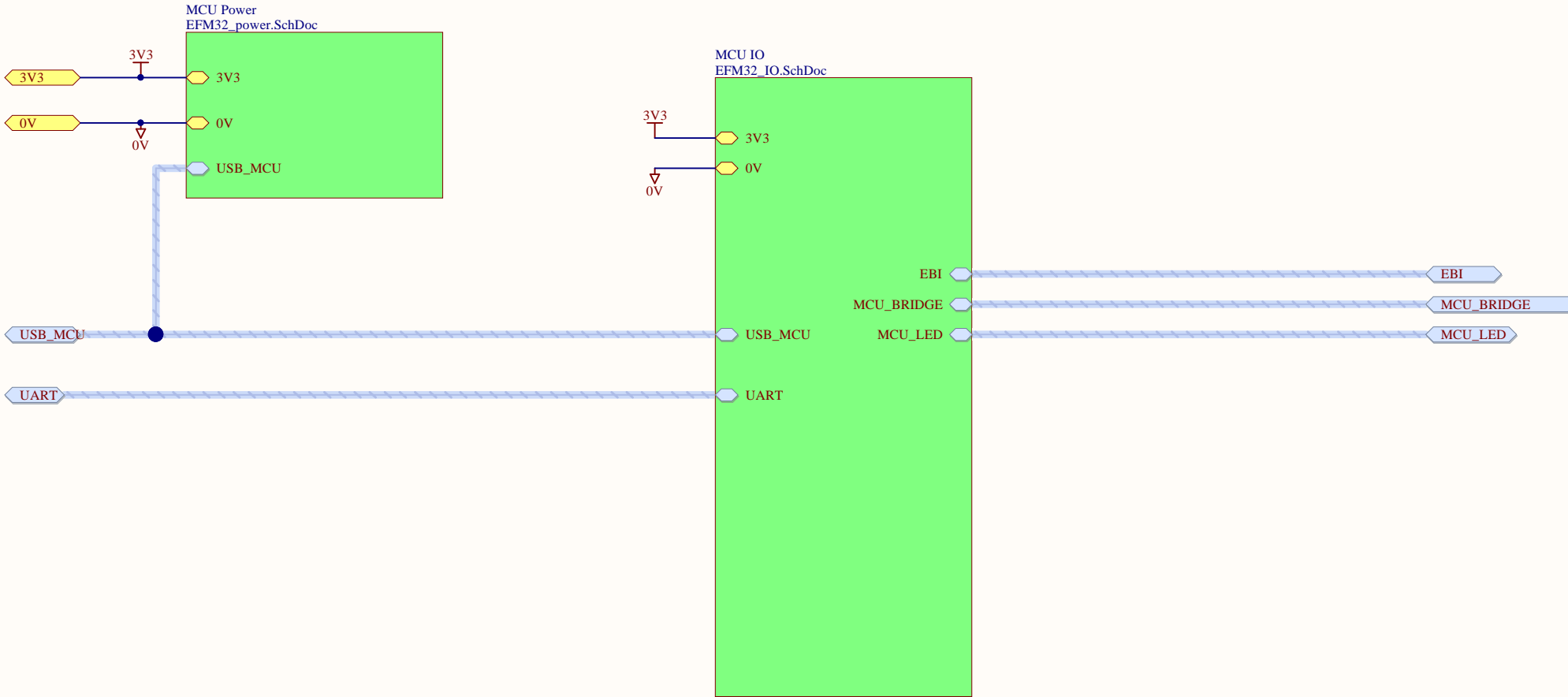
D

A

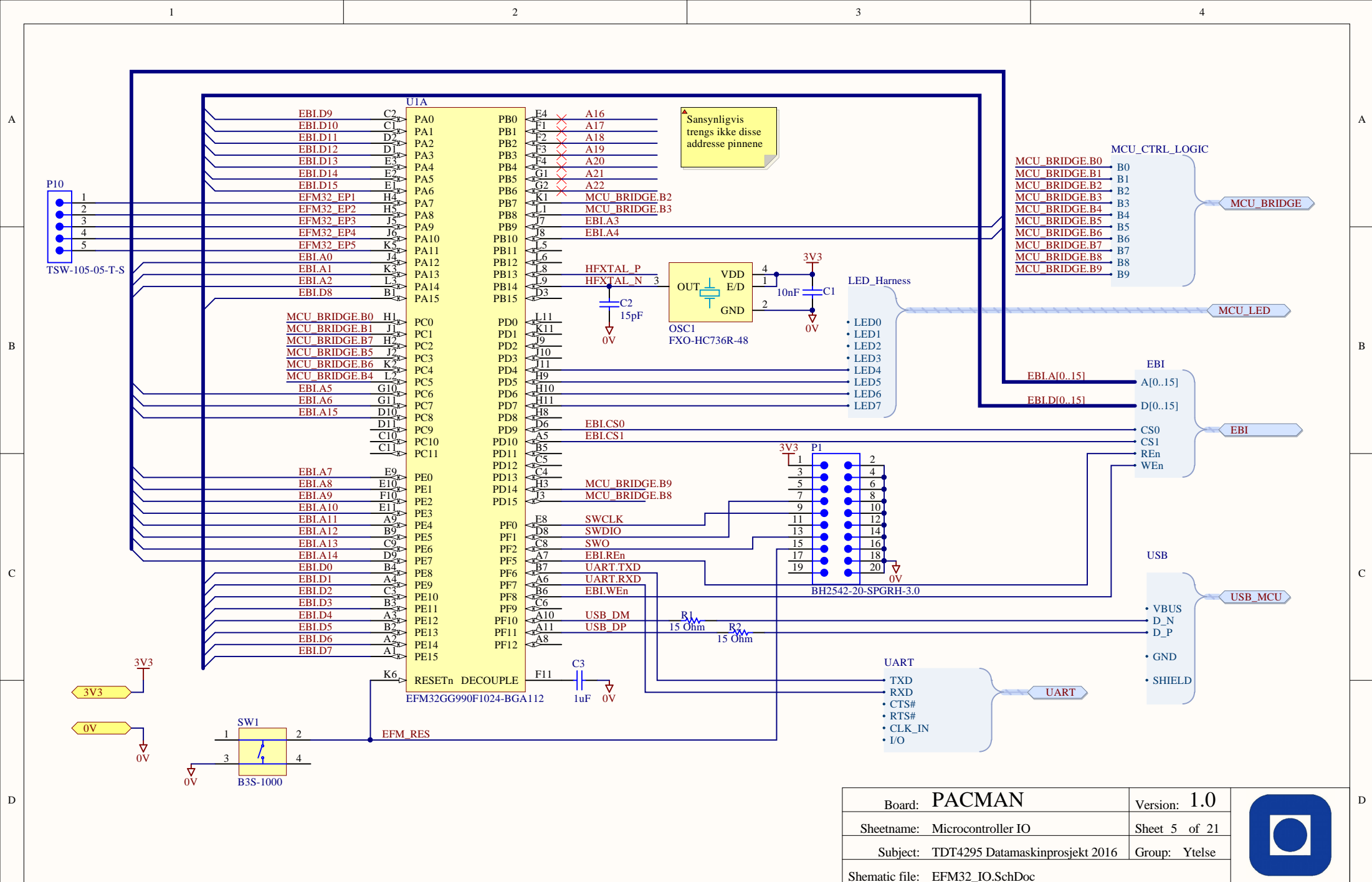
B

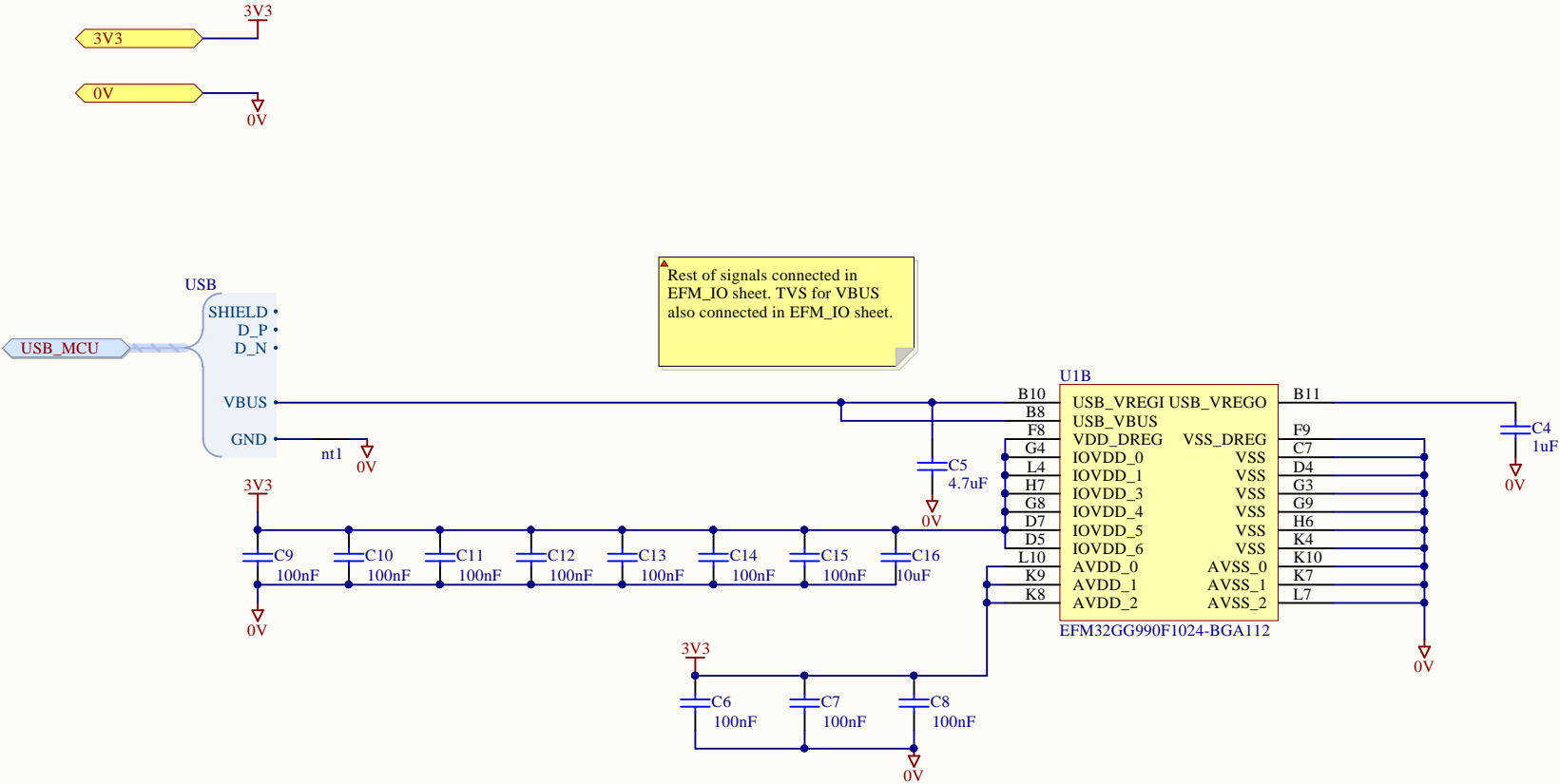
C

D



Board: PACMAN	Version: 1.0	
Sheetname: Microcontroller Top Level	Sheet 4 of 21	
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse	
Schematic file: MCUtop.SchDoc		





Board:	PACMAN	Version:	1.0
Sheetname:	Microcontroller Power Distribution	Sheet	6 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	EFM32_power.SchDoc		





A

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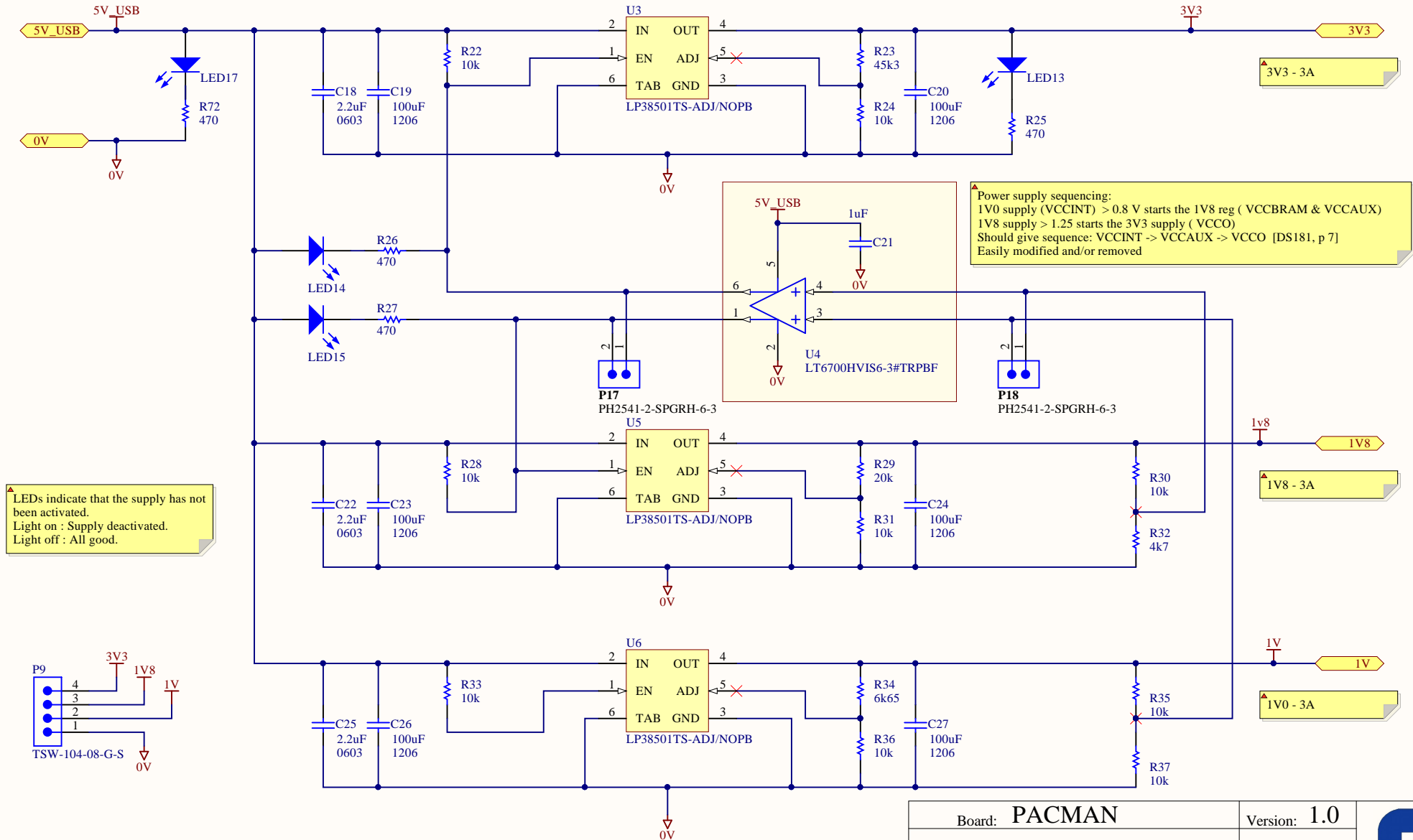
D

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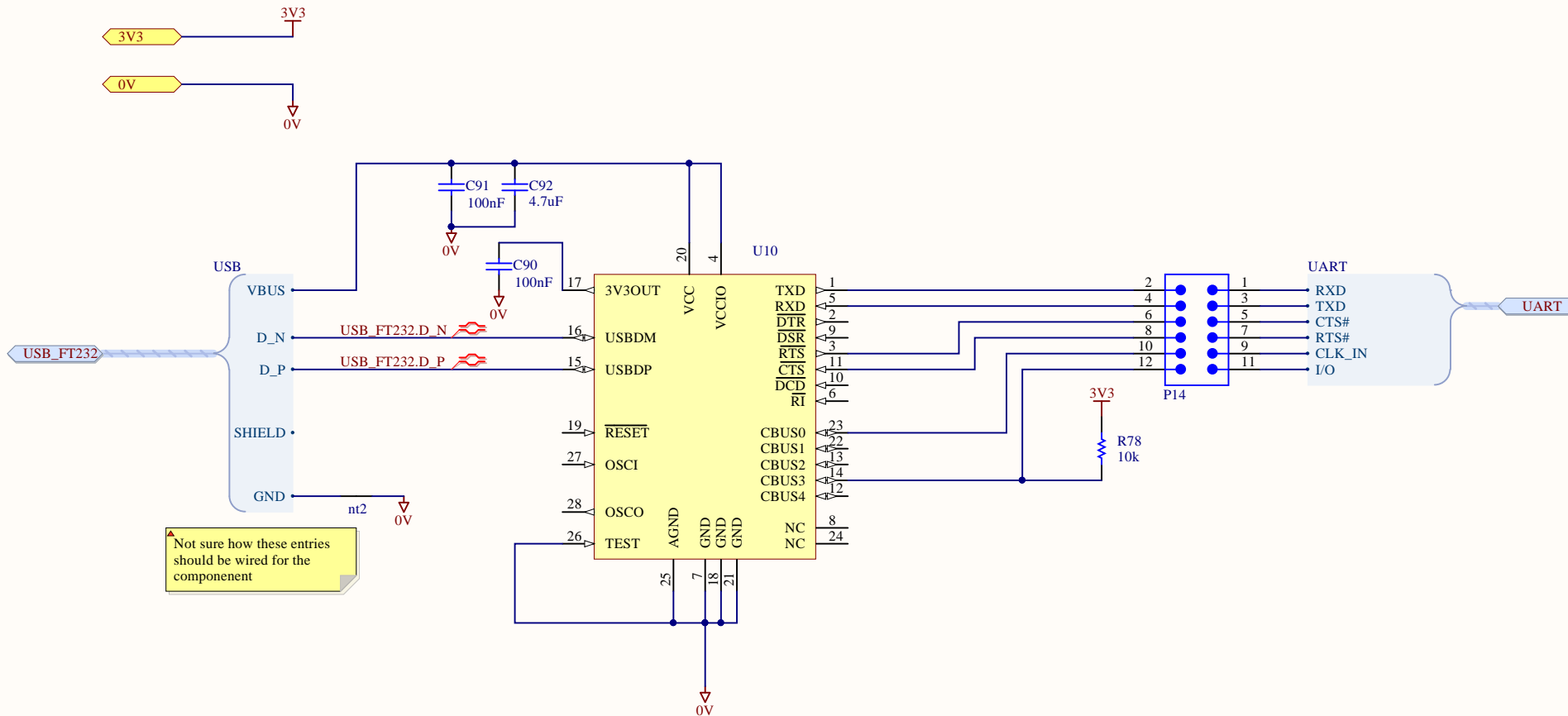


Board:	PACMAN	Version:	1.0
Sheetname:	Power Regulators	Sheet	8 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	Power.SchDoc		









Board: PACMAN	Version: 1.0
Sheetname: UART to USB Bridge	Sheet 10 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Schematic file: UART_connect.SchDoc	



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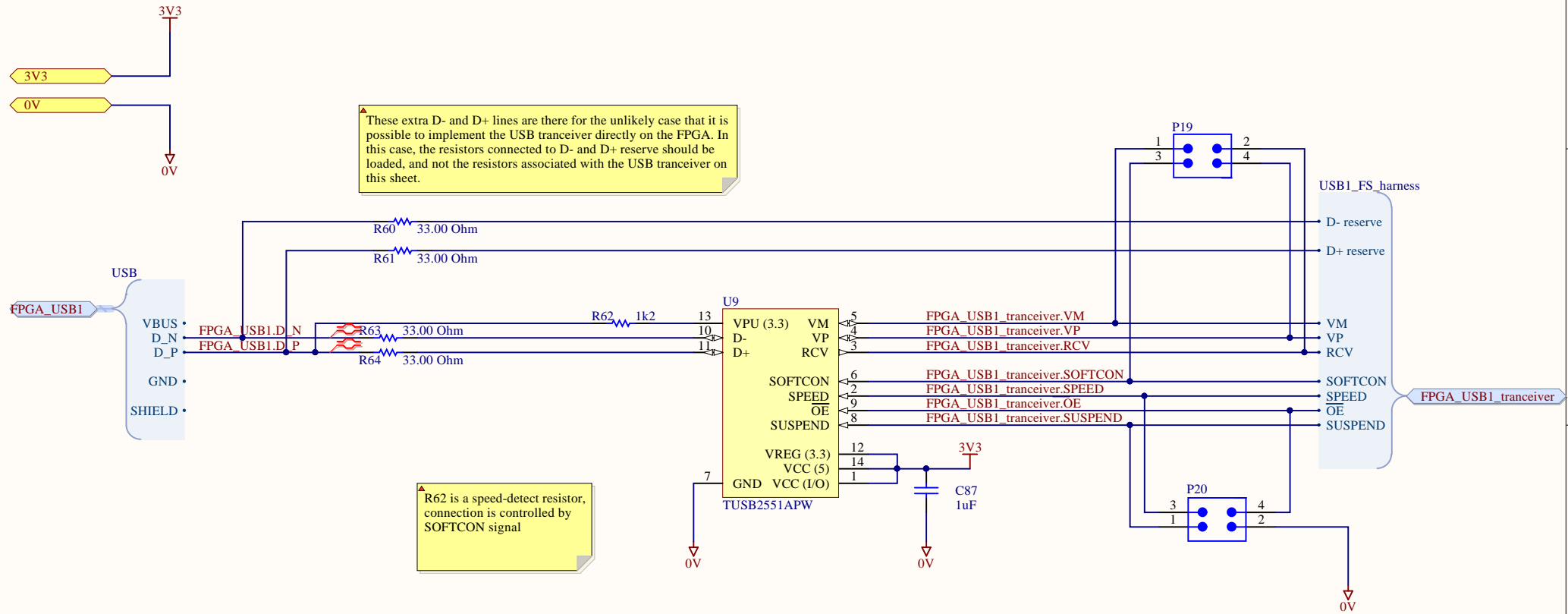
D

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D



Board: PACMAN	Version: 1.0
Sheetname: USB Full Speed transceiver	Sheet 11 of 21
Subject: TDT4295 Datamaskinprosjekt 2016	Group: Ytelse
Shematic file: USB_trans.SchDoc	





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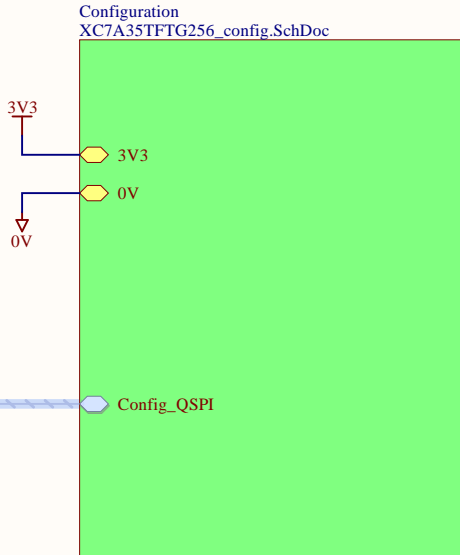
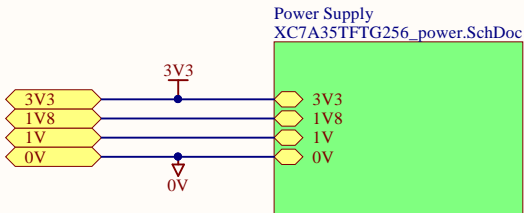
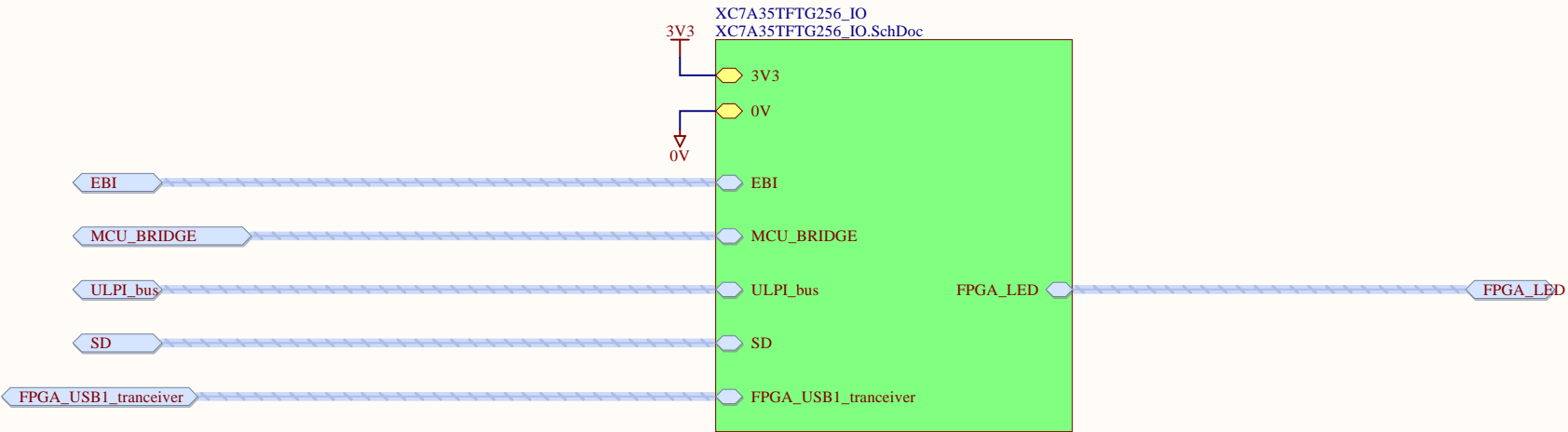
D

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Board:	PACMAN	Version:	1.0
Sheetname:	FPGA Top level	Sheet	13 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256.SchDoc		



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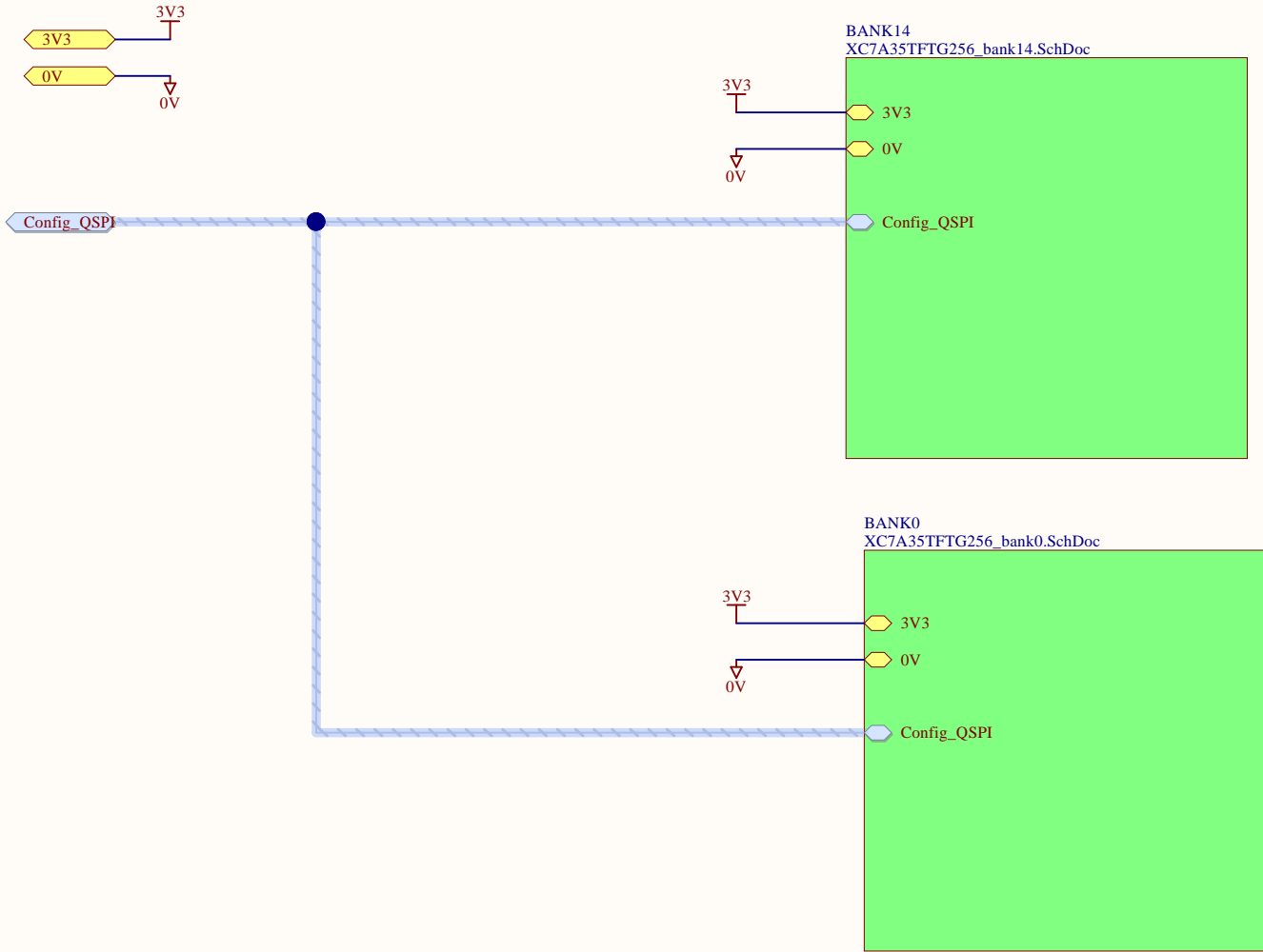
D

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D



Board:	PACMAN	Version:	1.0	
Sheetname:	FPGA Configuration Top Level	Sheet	14 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file: XC7A35TFTG256_config.SchDoc				

Note: this is a 2mm pitch jtag connector recommended by xilinx, might need to change later. Might even be better to have standard 2.54 mm pitch header to improve compatibility.

Check list recommends 330 ohms pull-up, BASYS and ARTY has this setup. Might be necessary to switch 200R for 330R and remove LED.

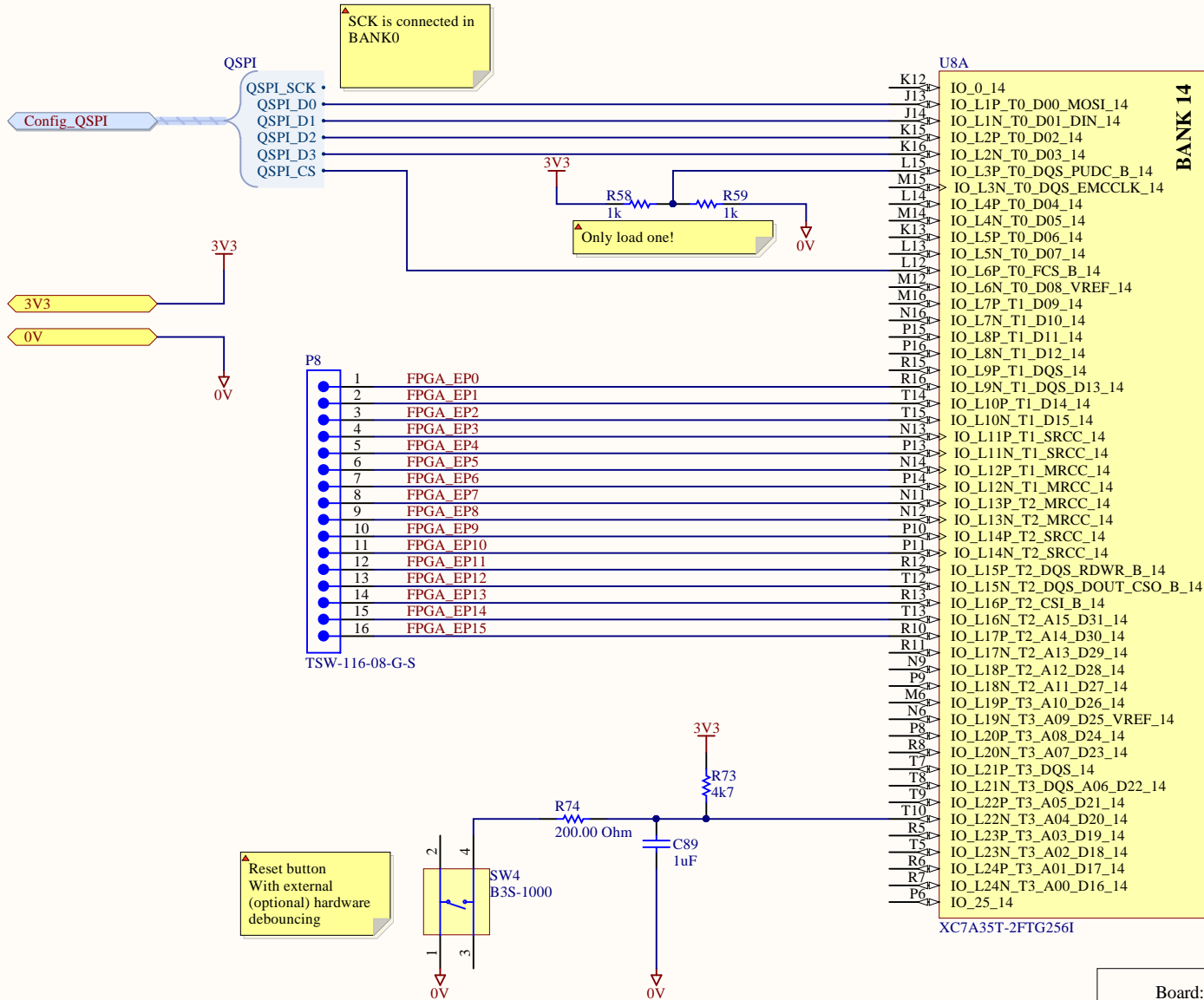
Default value = 0x111 = slave serial (internal pull ups in FPGA)  
  
M[2:0]=  
0x111 : Slave serial  
0x101 : JTAG only  
0x001 : Master SPI x1, x2, x4  
0x000 : Master Serial

Push to force reconfiguration

Done: High (open drain) when config done. indicator led with resistor to GND.  
  
Program\_B: Active low reset to config logic. 4.7kOhm pull up, push button to GND for manual config reset  
  
Init\_B: driven low during config reset, init or config error. Floating when init done, 4.7k pullup and (optionally indicator led. Not done on basys or arty, so dropped here as well).

DX: Temperature-sensing diode inputs. Not used, VREFP should be shorted to ground, since no external reference is used.

Note on max pin current: According to DS181, DC and AC Switching Char, the max current on any pin is 10mA, with a max total bank current of 200mA.



▲ PUDC: PullUp During Config. Low = Pull-up on selectIO, High = no Pull-up on SelectIO. Must not float!

Seems like PUDC=0 means that all IO will have pull-ups during config. Could be nice to have. Most safe option is to insert resistors that will allow selection between them.

EMCCLK: External Master Config Clock. Optional external clock source for config. Necessary?

▲ FCS\_B = Flash chip select

▲ VREF = Input reference voltage for Single-ended I/O standards with differential input buffer. Se UG471, page 18.

Appears to be a reference for a schmitt-trigger or something, and can be sourced internally, if needed. However, that will mean that the max Vref = 0.9V. Not sure if this is a problem.

Board:	PACMAN	Version:	1.0
Sheetname:	FPGA Bank 14	Sheet	16 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank14.SchDoc		





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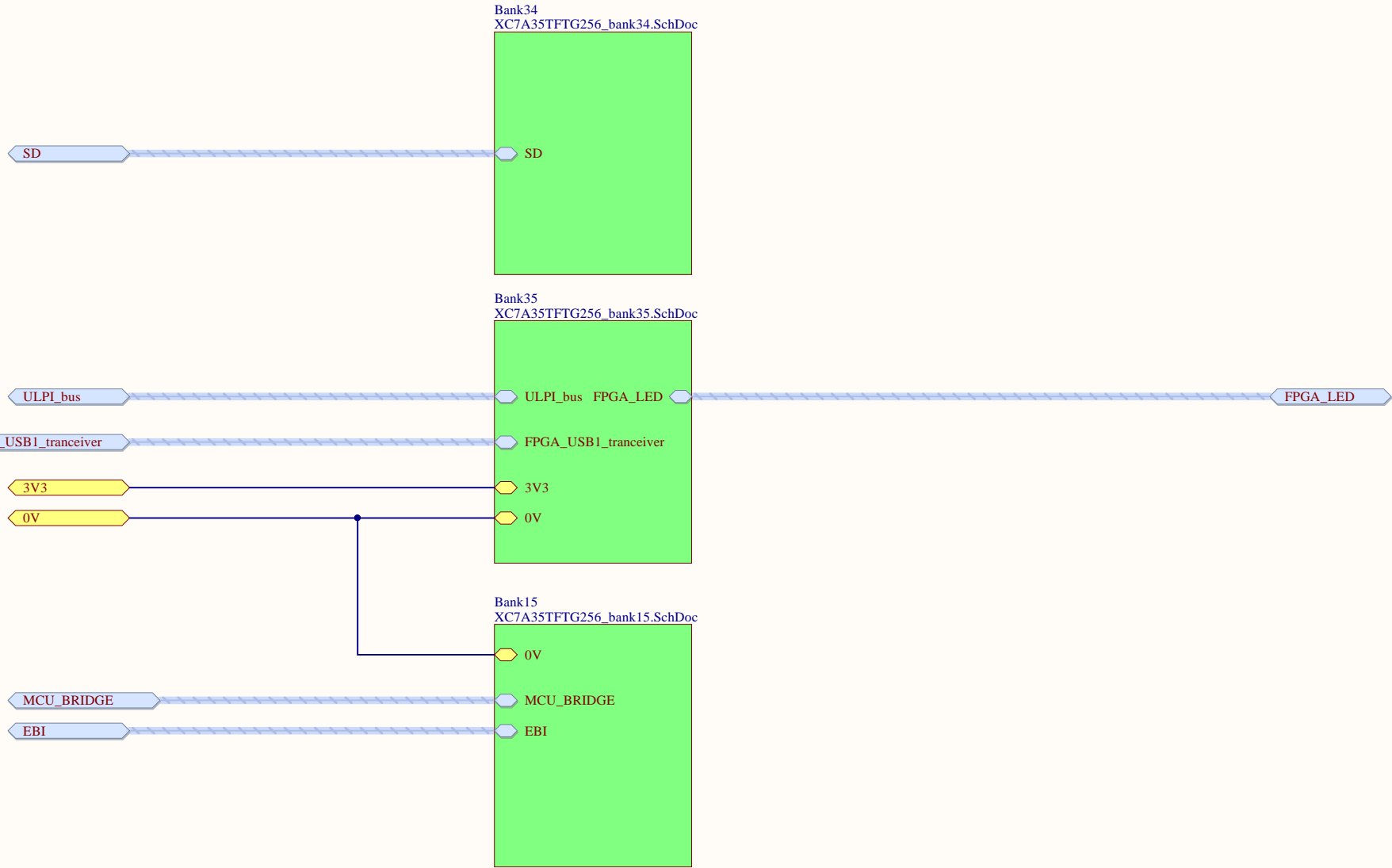
D

A

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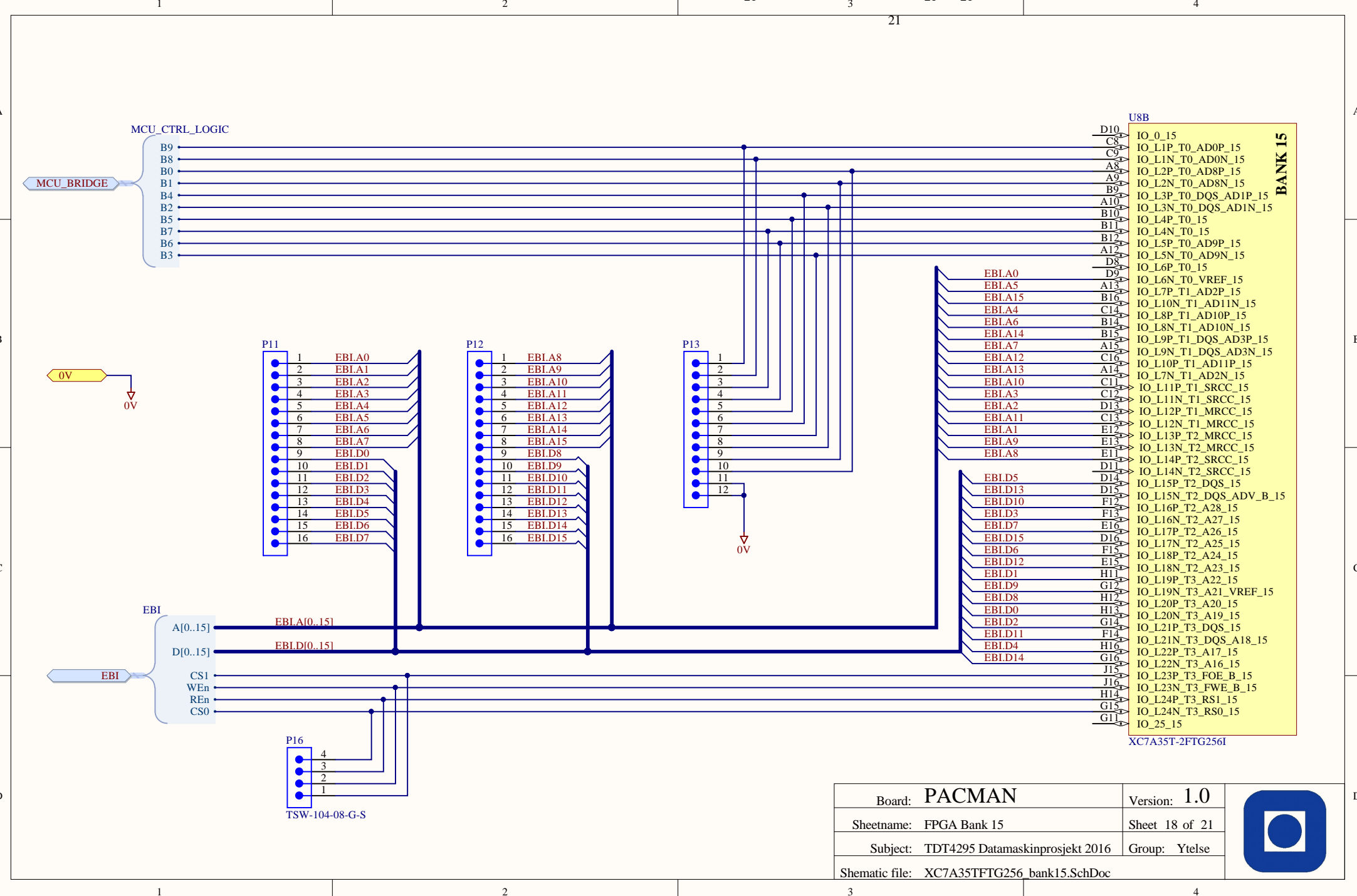
C

D



Board:	PACMAN	Version:	1.0
Sheetname:	FPGA IO Top level	Sheet	17 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Schematic file: XC7A35TFTG256_IO.SchDoc			





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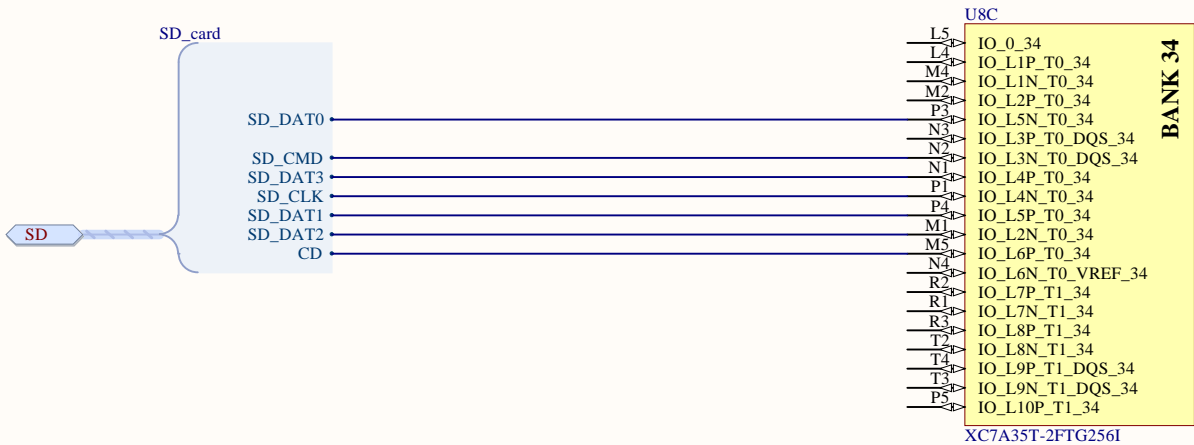
D


A

B

C

D



Board:	PACMAN	Version:	1.0	
Sheetname:	FPGA Bank 34	Sheet	19 of 21	
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse	
Schematic file:	XC7A35TFTG256_bank34.SchDoc			

A

A

B

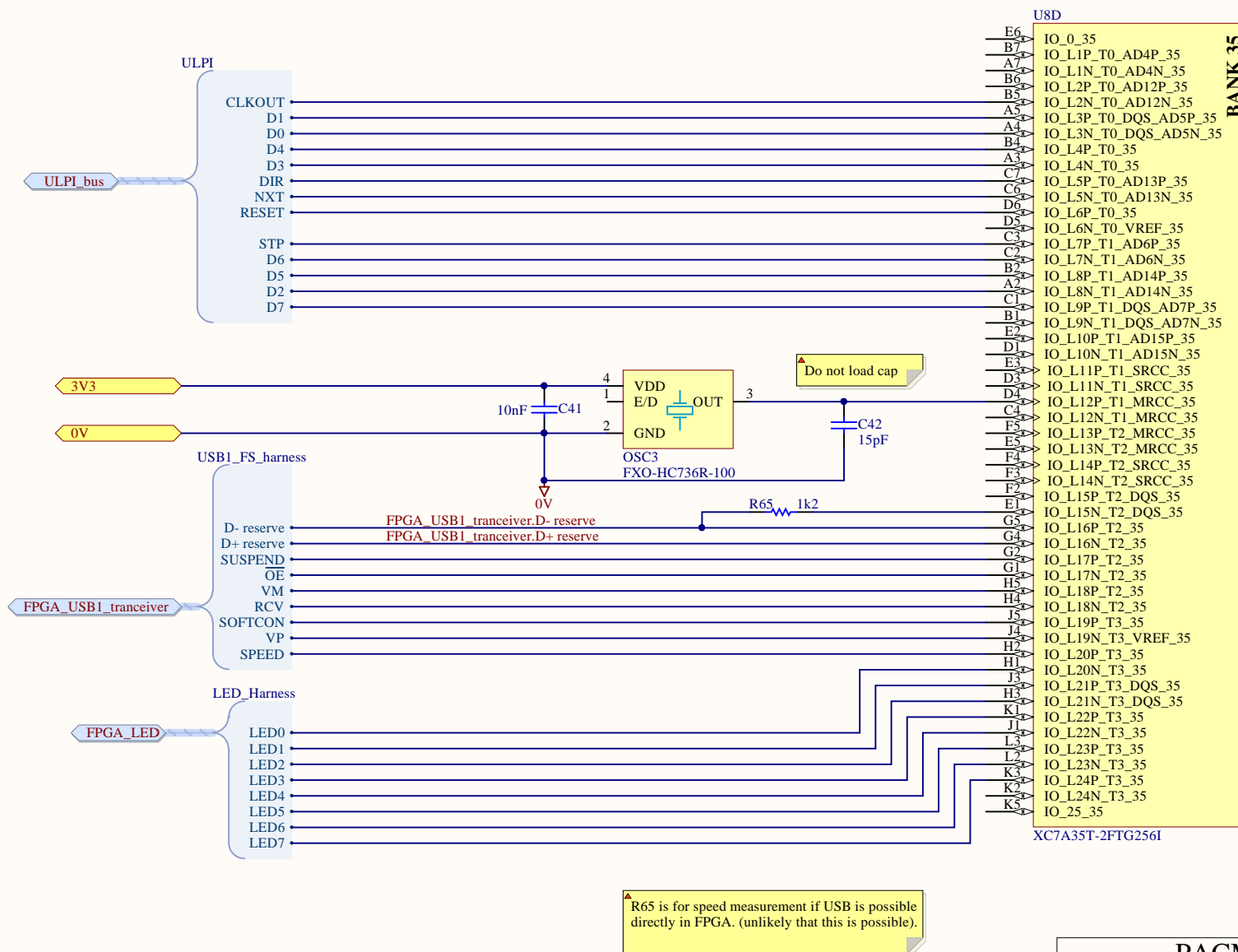
B

C

C

D

D



Board:	PACMAN	Version:	1.0
Sheetname:	FPGA Bank 35	Sheet	20 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Shematic file:	XC7A35TFTG256_bank35.SchDoc		



A

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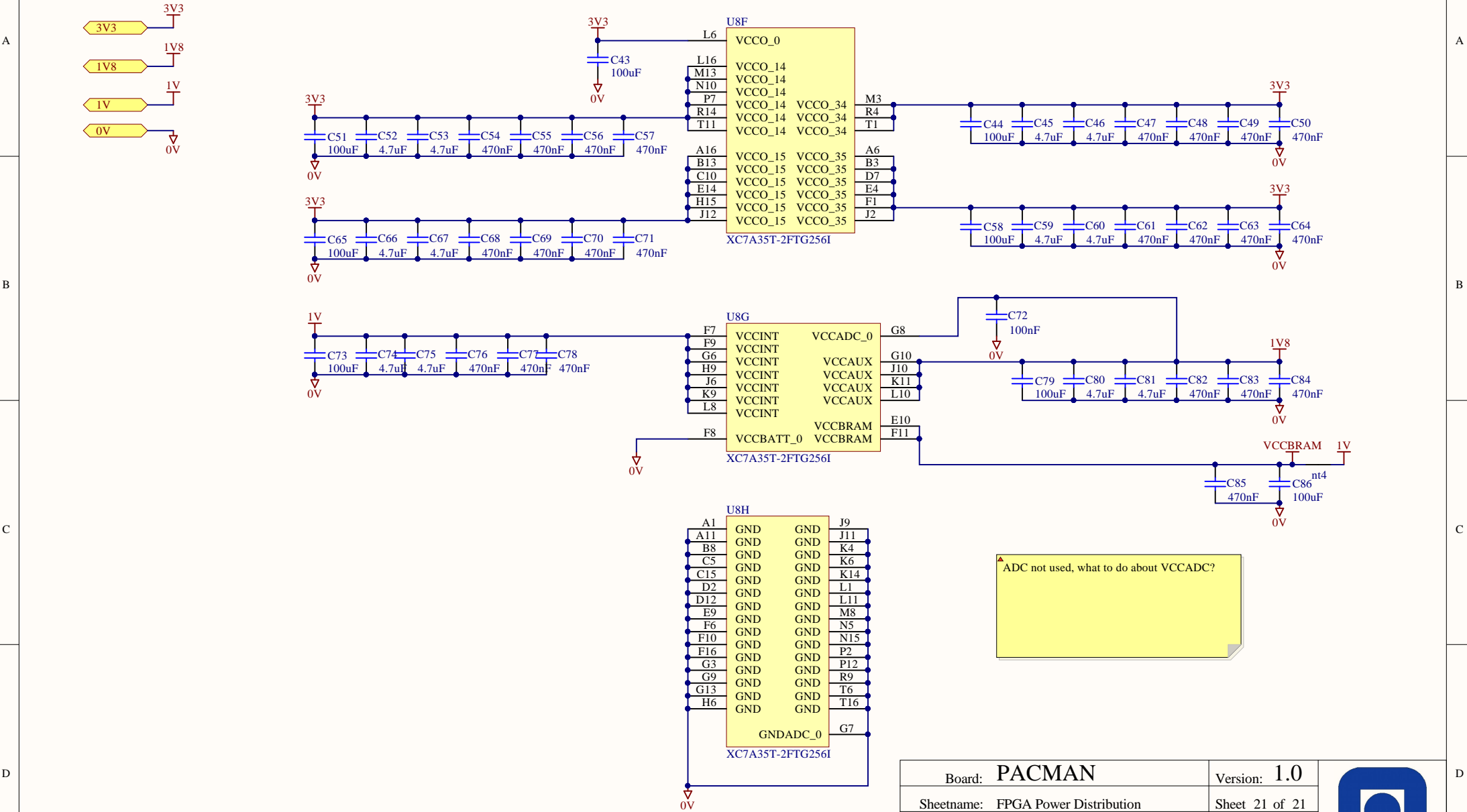
D

A

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D



Board:	PACMAN	Version:	1.0
Sheetname:	FPGA Power Distribution	Sheet	21 of 21
Subject:	TDT4295 Datamaskinprosjekt 2016	Group:	Ytelse
Schematic file: XC7A35TFTG256_power.SchDoc			