SECTION - A

Answer 1 (a)

① DIODE CAPACITANCE :- Depending upon the type of biasing used capacitive effect exist in the P-N Junction diode. It is classified into two types.

(i) Transition Capacitance (C_T) :-
The capacitive effect that took place in Reverse Biased condition of a diode is termed as Transition Capacitance.

(ii) Diffusion Capacitance (C_D) :-
The capacitive effect that took place in forward biased condition of a diode is termed as Diffusion Capacitance.

Answer 1 (b)

Peak Inverse Voltage (PIV) :- The highest voltage a diode can tolerate in the reverse direction without breaking down.

Answer 1 (c)

Clipper Circuit	Clamper Circuit
1) Clipper circuit is used to remove any unwanted part of the given waveform	1) Clamper circuit is used to clamp the complete signal to a different voltage level.
2) It is also called limiters or slicers	2) It is also called d.c. restorer or d.c inserter circuits.

Answer 1 (d)

BJT	FET
1) It is a bipolar device	1) It is a unipolar device.
2) Current conduction is due to electron & holes both	2) Current conduction is either due to e^- or holes
3) Current controlled device	3) Voltage controlled device
4) 3 terminals are Emitter, Base and Collector	4) 3 terminals are Drain, Grate and Source.
5) Large in size	5) Small in size.

Answer 1 (e)

Given :- $I_B = 20\,mA$; $\beta = 50$; $I_E = ?$

We know that

$$\gamma = 1 + \beta = \frac{I_E}{I_B}$$

So $(1+50) = \dfrac{I_E}{20 \times 10^{-3}} \Rightarrow I_E = (51)(20 \times 10^{-3})$

$$\therefore \boxed{I_E = 1020\ mA}$$

Answer 1 (f)

Ideal op-amp Characteristics

1) Infinite voltage gain.
2) Infinite Input impedance.
3) Zero output impedance.
4) Zero offset voltage.
5) Infinite Bandwidth

Signature

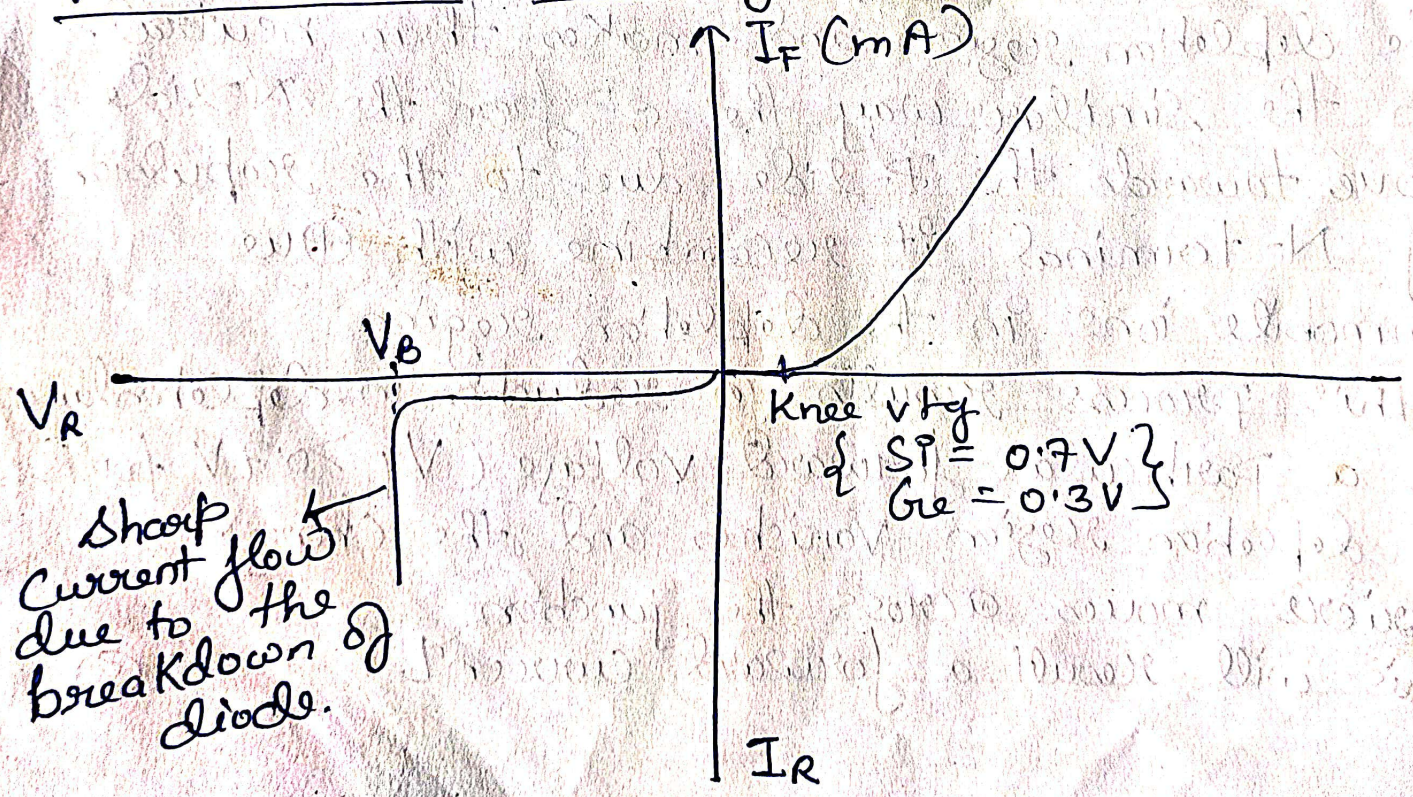
Answer 1(g)

A Lissajous pattern is a pattern that appears on a CRO screen when sinusoidal signals are applied to the CRO's horizontal and vertical deflection plates.
It is used to measure the frequency and phase difference between the signals.

SECTION (B)

Answer (2A)

V-I characteristics of P-N Junction Diode:-



I_o → it is form due to the thermally generated minority charge carrier.

Working :-

→ Very less (+)ve Vtg → Almost No forward Current.

→ $V_F > 0.7$ (in Si) → Significant current is flowing in increasing I_f.

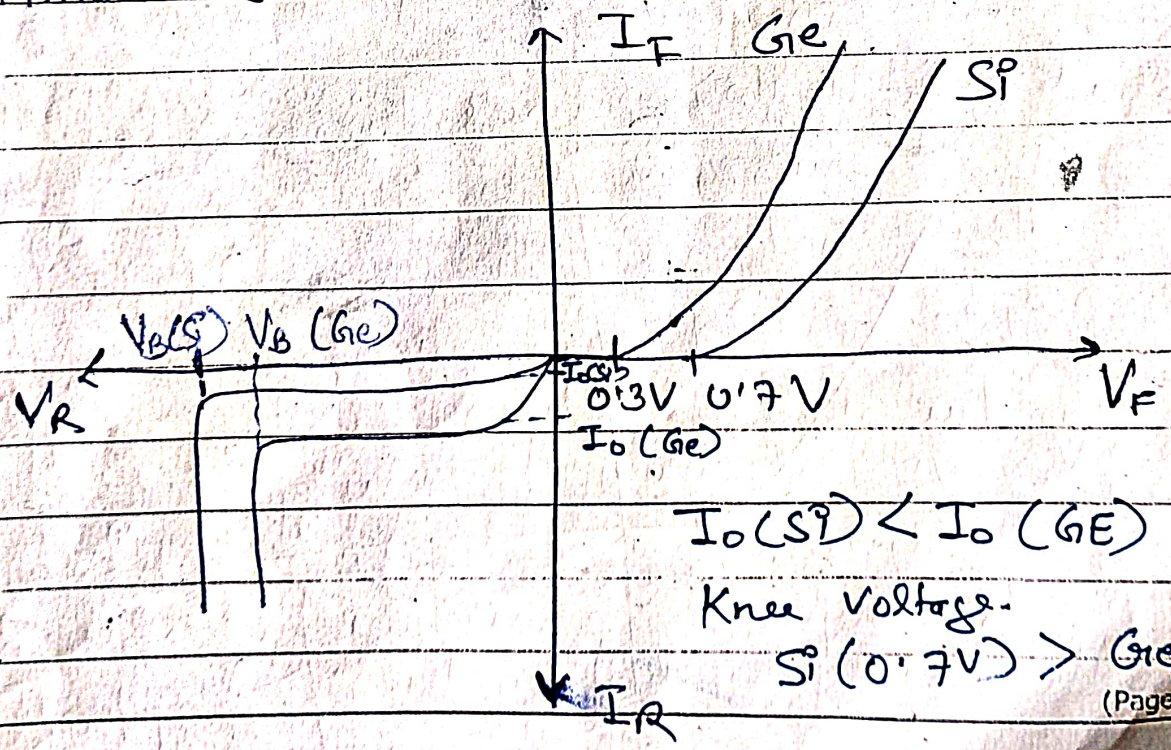
→ In R.B ($V_R = -ve$). $I_R = 0$ ideally.

→ In practical, a very low current flow i.e I_o.
I_o = reverse saturation current.

→ If we keep increasing on V_R, then at a particular vtg diode breaks and that vtg is called Breakdown vtg.

→ Sharp current flows at the breakdown vtg point and it is due to minority charge carriers

COMPARISON IN V-I CHARACTERISTICS OF Si and Ge



I_o(Si) < I_o (GE)

Knee Voltage.

Si (0.7V) > Ge (0.3V)

Effect of Temperature on V-I characteristics of P-N Junction Diode :-

⇒ The temp. has following effects on diode parameters.

1) The cut in vtg decreases as temp. increases.
2) The reverse saturation current ↑s as temp ↑s
⇒ This increase in reverse current is such that it doubles at every 10°C rise in temp

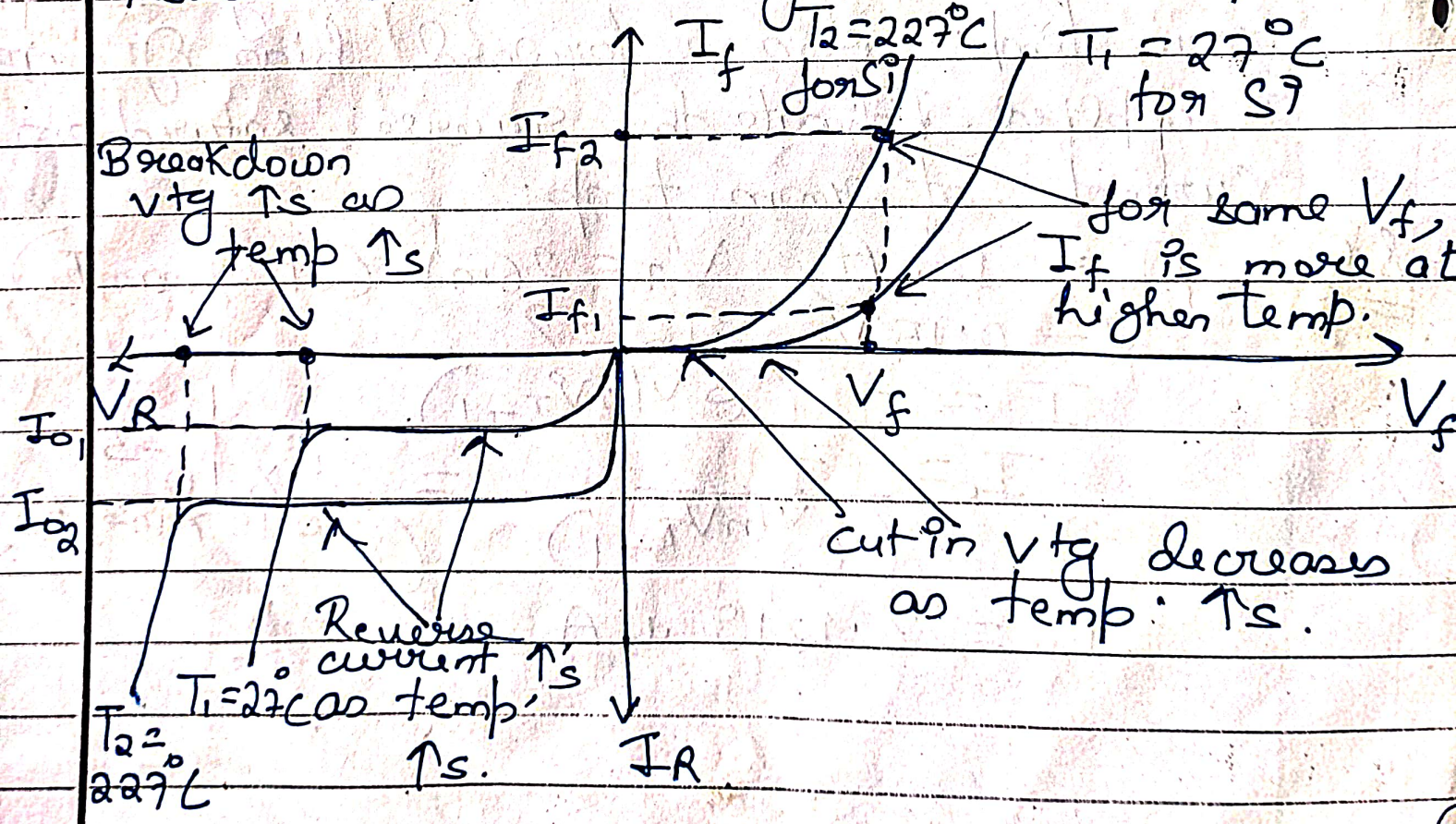
Mathematically

$$I_{02} = 2^{(\Delta T/10)} I_{01}$$

I_{02} = reverse current at T_2 °C, $(\Delta T = T_2 - T_1)$
I_{01} = " " " T_1 °C.

⇒ V_T ↑ as temp. ↑s.

⇒ Reverse breakdown vtg ↑s as temp ↑s



SECTION B

ANSWER (2B)

TUNNEL DIODE :-

→ The diodes in which the concentration of impurity atoms is greatly increased u 1 part in 10^3, to get completely change ch, are called tunnel diodes.

→ Due to the heavy doping, the deple region gets reduced considerably, of the order of about 1/100 the width depletion region in normal p-n jn

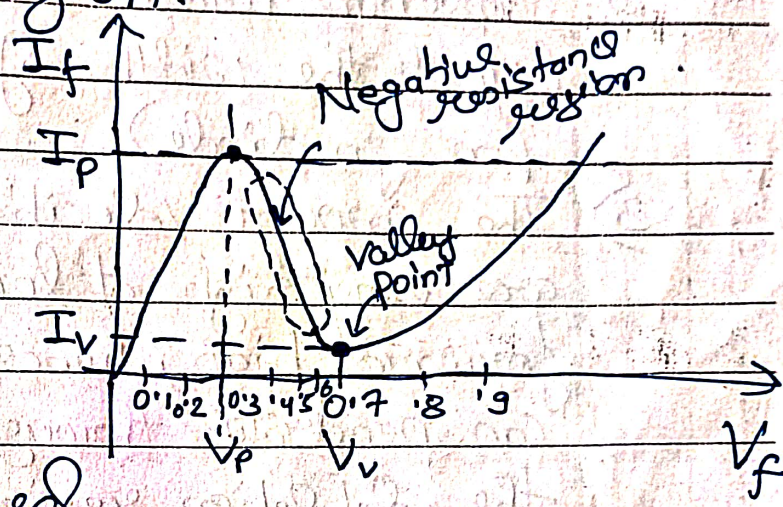
→ Due to the thin depletion region, a e^- penetrates through the barrier. This is called tunneling and hence such high impurity density p-n jn d are called tunnel diodes.

It exhibits negative resitance region which is the most important feature of a tunnel diode.

Working Principle :-

Doping ↑↑ ⇒ Depletion Width ↓↓ negative resistance region.

The depletion region of tunnel diode is thin due to high doping.

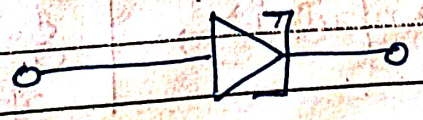


As a result there exists a effect named as tunneling effect.

The e^- charges moves from N-side to P-side and holes moves from P-side to N-side through this very thin depletion region.

Hence a subsiquent or significant current starts to flow at a very low vtg and after its peak value is attained. it decreases due to ⊖ve resistance region presence and after 0.7 V it starts behaving as normal P-N Jn. diode.

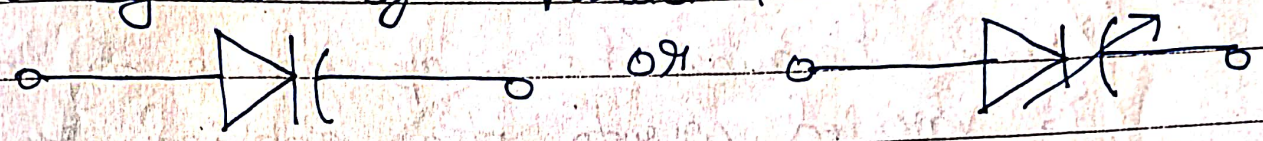
Symbol :-



VARACTOR DIODE :-

Special type of diodes which shows the transition capacitance property more predominantly as compared to the normal diodes are called varactor diodes, vari cap, VVC (voltage Variable Capacitance) or tuning diodes.

The symbol of varactor diode is.



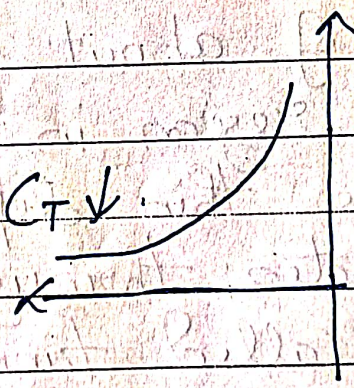
Working :-

* Working of varactor diode is based on capacitive effect of P-N Jn. diode in reverse bias condition. i.e C_T (transition capacitance).

If we increase the reverse voltage across the diode the depletion width also increases and hence C_T decreases.

$$C_T = \frac{\varepsilon A}{W}$$

* $V_R \uparrow$, $W \uparrow$, $C_T \downarrow$



$V_R \downarrow$, $W \downarrow$, $C_T \uparrow$.

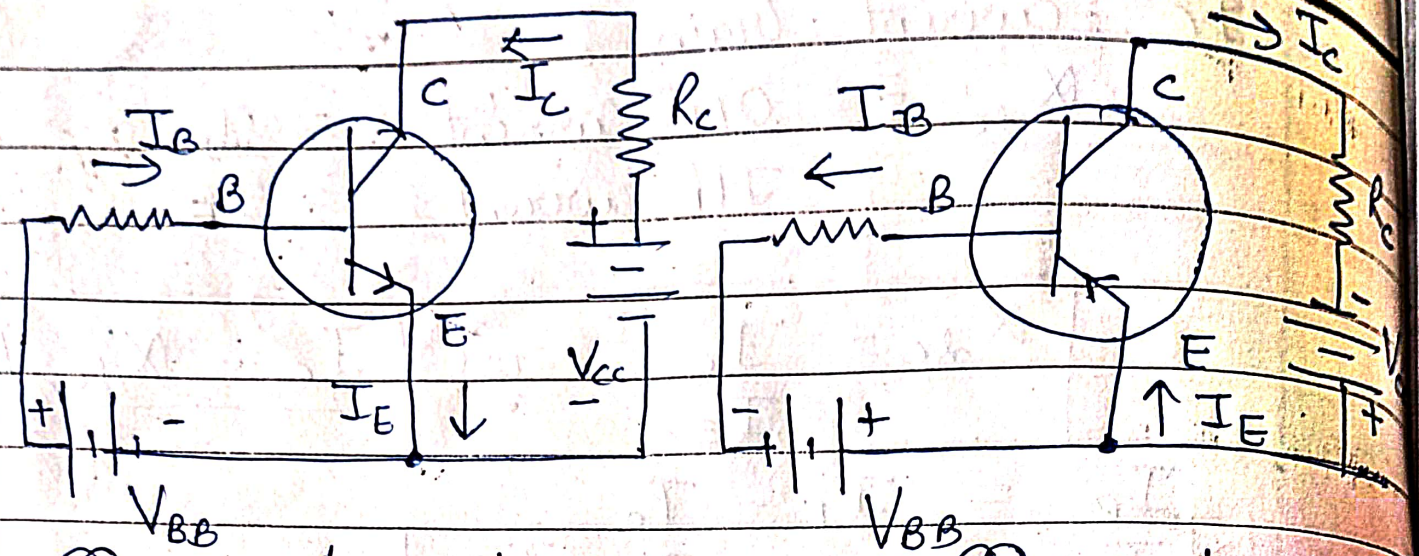
SECTION B

ANSWER (2 C)

COMMON EMITTER CONFIGURATION :-

→ I/P is applied b/w base and emitter and O/P is taken from collector and emitter.

→ Emitter of the transistor is common to both, input and output circuits.



(a) npn transistor (b) pnp transistor

→ I/P voltage in CE configuration is V_{BE} and O/P voltage is V_{CE}, I/P current is I_B and O/P current is I_C.

Current Relations in CE Configuration :-

→ β_{dc} is the ratio of O/P current I_C and I/P current I_B in CE configuration.

$$\beta_{dc} = \frac{I_C}{I_B}$$

We know, $\beta = \frac{I_C}{I_B}$, & we have $I_E = I_B + I_C$

i.e. $I_B = I_E - I_C$.

or $\beta = \frac{I_C}{I_E - I_C}$ ⟹ (1)

Dividing Num & Demo. of eq (1) by I_E,

$$\beta = \frac{I_C/I_E}{I_E/I_E - I_C/I_E} = \frac{\alpha}{1-\alpha}$$

$$\therefore \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

We know that, $\alpha = \frac{I_C}{I_E}$ and $I_E = I_B + I_C$.

$$\therefore \alpha = \frac{I_C}{I_B + I_C} \quad \text{——— (11)}$$

Dividing Num. & deno. of eq (11) by I_B.

$$\alpha = \frac{I_C/I_B}{I_B/I_B + I_C/I_B}$$

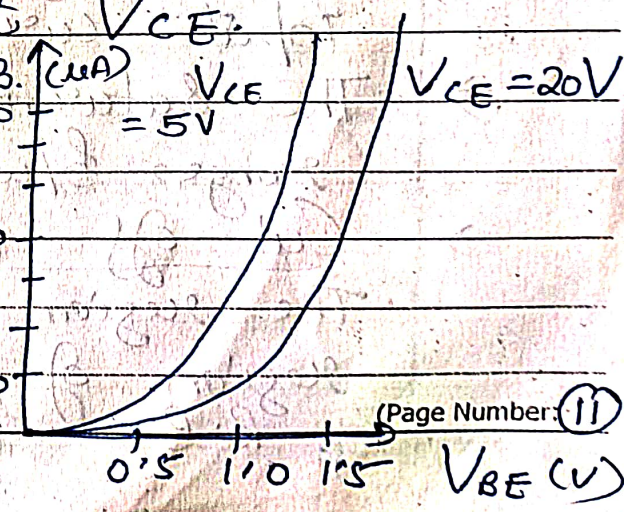
$$\therefore \boxed{\alpha = \frac{\beta}{1+\beta}}$$

Common Emitter (CE) Characteristics :-

1) Input Characteristics :-

→ Curve b/w I/P voltage V_{BE} and I/P current I_B at constant V_{CE}.

→ The input resistance is $r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$



→ CE input Ch. resembles to F.B diode curve.

→ After cut in vtg, I_B increases rapidly w small increase in V_{BE}. Thus I/P resistance is small in CE configuration.

→ For a fixed value of V_{BE}, I_B ↓ as V_{CE} ↑

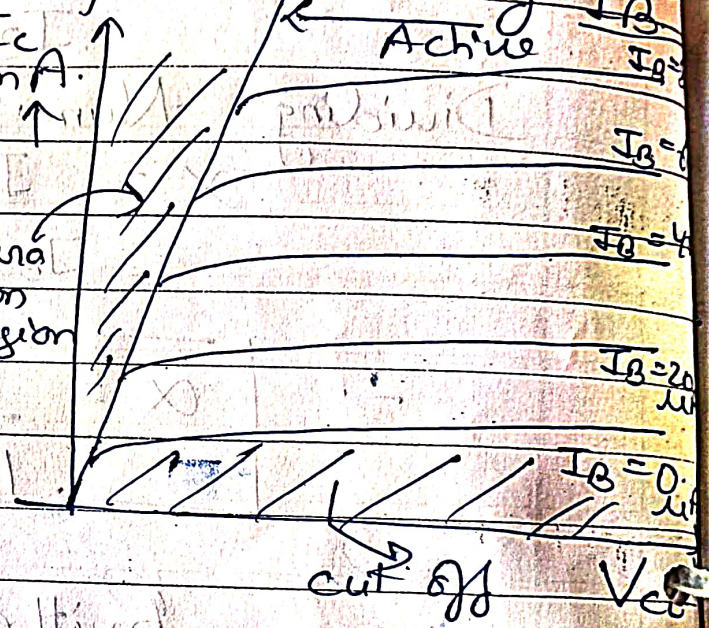
2) Output Characteristics :-

→ It is a curve b/w O/P current I_C and V_{CE}, for various fixed values of I_B.

→ Active Region :-

→ E-B jn is FB & CE jn is RB.

→ I_C rise more sharply with ↑'s V_{CE} in the linear region of O/P ch. of CE transistor.



→ Saturation Region :-

→ EB jn and C-E jn both are F.B. In this region I_C does not depend upon input current I_B.

→ The saturation value of V_{CE} usually ranges b/w 0.1 V to 0.3 V.

→ Cut-off Region :-

The region below $I_B = 0$ is the cut off region of operation. Both the jn are R.B.

SECTION B

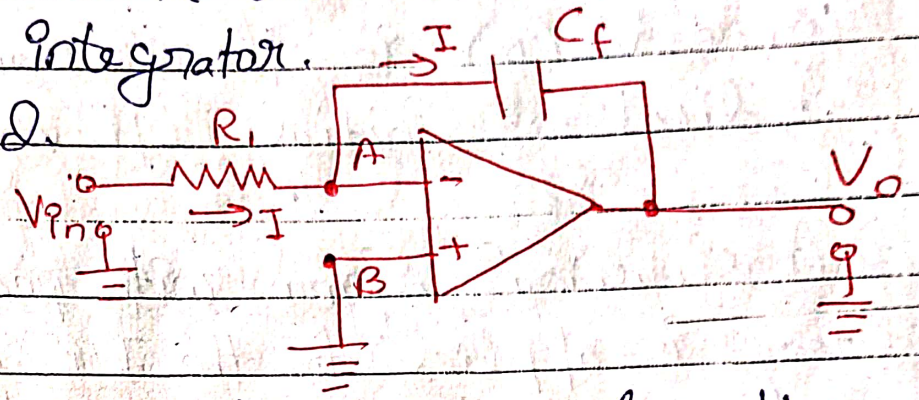
ANSWER (2D)

INTEGRATOR (IDEAL ACTIVE OP-AMP INTEGRATOR)

Integrator using an active devices like op-amp is called active integrator.

Node B is grounded.

So by concept of virtual ground



$$V_A = V_B = 0$$

⇒ I/P current of op-amp is zero., So entire current flows through R_1 & also through C_f

From I/P side we can write

$$I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad \text{— (1)}$$

From O/P side

$$I = C_f \frac{d(V_A - V_o)}{dt} \quad \text{i.e} \quad I = -C_f \frac{dV_o}{dt} \quad \text{— (2)}$$

Equating eq (1) & (2).

$$\frac{V_{in}}{R_1} = -C_f \frac{dV_o}{dt} \quad \text{— (3)}$$

Integrating both sides of eq (3).

$$\int_0^t \frac{V_{in}}{R_1} dt = -C_f \int \frac{dV_o}{dt} dt$$

i.e $\int_0^t \frac{V_{in}}{R_1} dt = -C_f V_o$

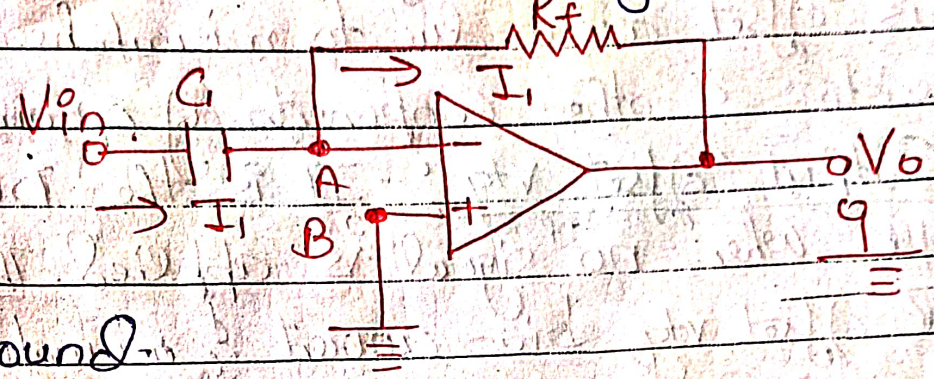
$$\boxed{V_o = \frac{-1}{R_1 C_f} \int_0^t V_{in} dt + V_o(0)}$$

where $V_o(0)$ is the constant of integration, indicating initial O/P vtg.

DIFFERENTIATOR :-

IDEAL ACTIVE OP-AMP DIFFERENTIATOR :-

The differentiator using an active device like op-amp is called an Active differentiator.



The node B is grounded. So by concept of virtual ground.

$$V_A = V_B = 0.$$

From the I/P side we can write

$$I_1 = \frac{(V_A - V_o)}{R_f} \Rightarrow -\frac{V_o}{R_f} \quad \text{—— (1)}$$

From the I/P side we can write.

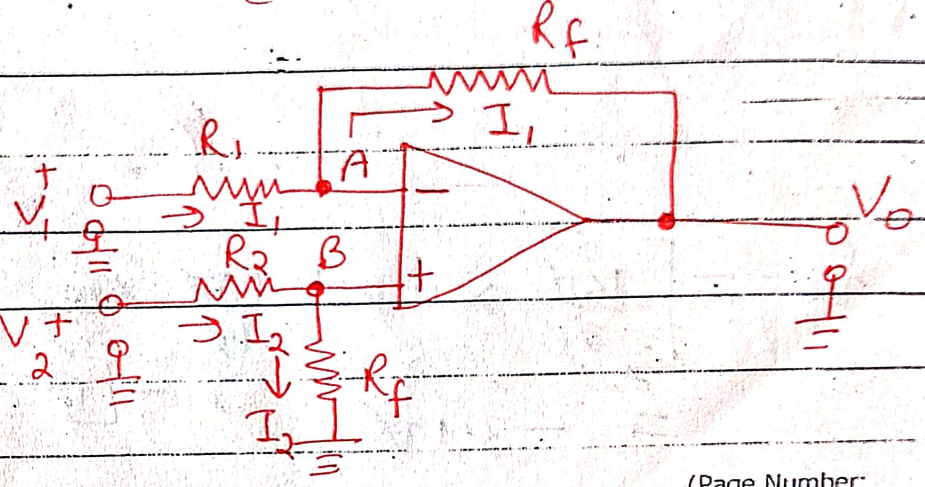
$$I_1 = C_1 \frac{d(V_{in} - V_A)}{dt} = C_1 \frac{dV_{in}}{dt} \quad \text{—— (2)}$$

Equating eq (1) & (2)

$$C_1 \frac{dV_{in}}{dt} = -\frac{V_o}{R_f}$$

$$\boxed{V_o = -C_1 R_f \frac{dV_{in}}{dt}} \quad \text{—— (4)}$$

DIFFERENCE AMPLIFIER (SUBTRACTOR)



find the relation b/w the Inputs and O/P

Let us use Superposition theorem.

Let V_{01} be the O/P, with I/P V_1 acting alone

So $V_2 = 0$ & V_{02} be the O/P with I/P V_2 acting alone and $V_1 = 0$.

when $V_2 = 0$, Ckt acts as Inverting amplifier

$$V_{01} = -\frac{R_f}{R_1} V_1 \quad \text{--- (1)}$$

~~when $V_1 = 0$~~

when $V_1 = 0$, ckt acts as non inverting amplifier

$$V_{02} = \left[1 + \frac{R_f}{R_1}\right] V_B \quad \text{--- (2)}$$

Applying vtg divider rule to the I/P V_2 loop.

$$V_B = \frac{R_f}{R_2 + R_f} V_2 \quad \text{--- (3)}$$

Substituting V_B from eq (3) to eq (2).

$$V_{02} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{R_f}{R_2 + R_f}\right] V_2$$

$$V_0 = V_{02} + V_{01}$$

$$V_0 = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right] \left[\frac{R_f}{R_2 + R_f}\right] V_2$$

If $R_1 = R_2$

$$V_0 = -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right] \left[\frac{R_f}{R_1 + R_f}\right] V_2$$

$$V_0 = -\frac{R_f}{R_1} V_1 + \frac{R_f}{R_1} V_2$$

$$\boxed{V_0 = \frac{R_f}{R_1} [V_2 - V_1]}$$

Thus the O/P vtg is prop. to the differen b/w the two I/P vtgs. Thus it acts as a subtractor or difference amplifier.

⇒ If $R_1 = R_2 = R_f$ is selected.

$$\boxed{V_o = V_2 - V_1}$$

SECTION B

ANSWER (2E)

Types of Digital Voltmeters.

The DVM are classified mainly based on the technique used for A to D conversion.

- DVM
  - Non Integrating type
    - Potentiometric type
      - Servo potentiometric
      - Successive approximation
      - Null balance type
    - Ramp type
      - Linear type
      - Staircase type
  - Integrating
    - Voltage to fr Converter type
    - Dual slope Integrating

RAMP TYPE DVM :-

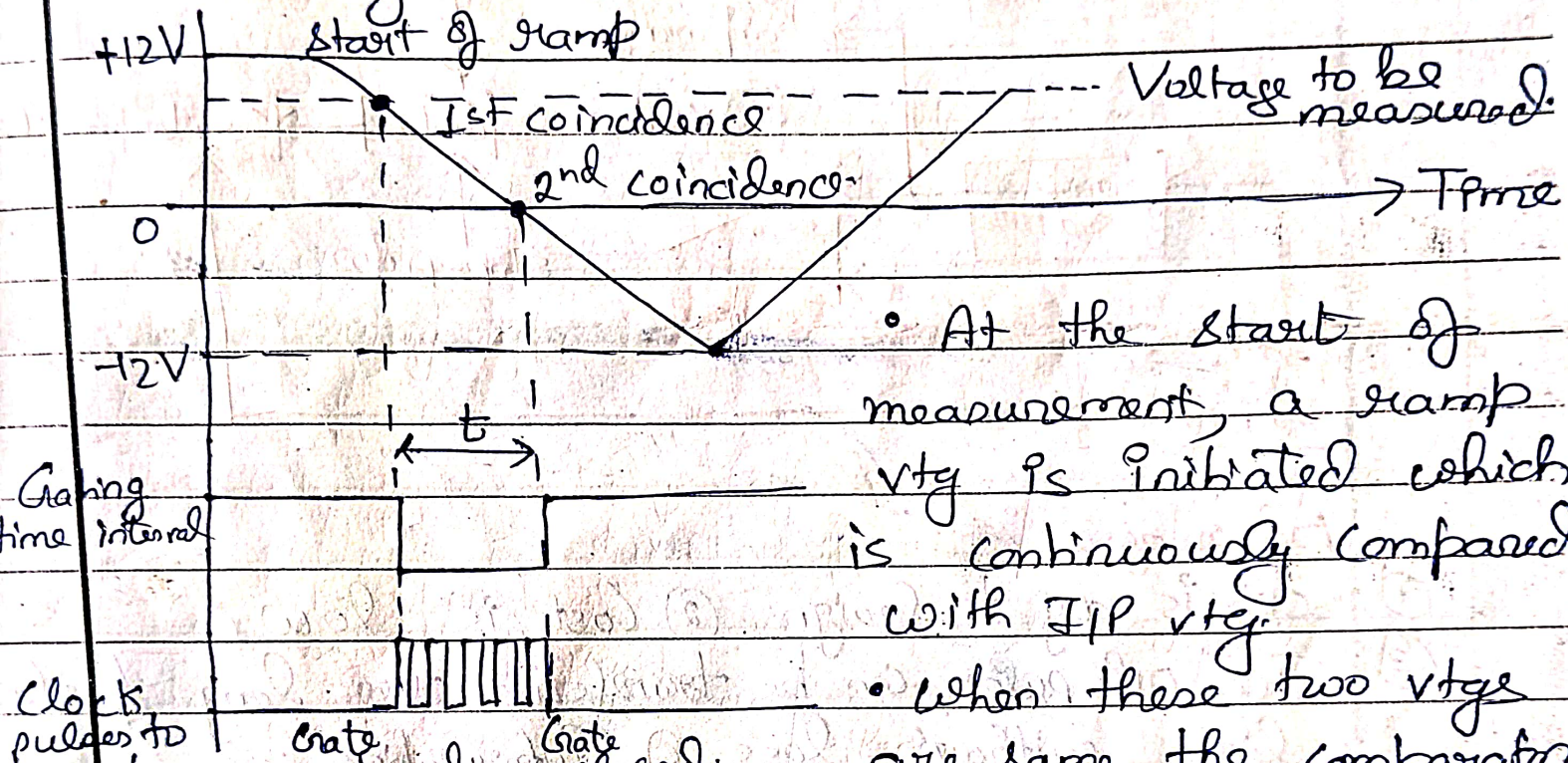
→ It uses a linear ramp technique or staircase ramp technique.

Linear Ramp Technique :-

The basic principle of such measurement is based on the measurement of the time taken by a linear ramp to rise from 0V to the level of the I/P vtg or

to decrease from the level of the I/P vtg to zero. This time is measured with the help of electronic time interval counter and the count is displayed in the numeric form with the help of a digital display.

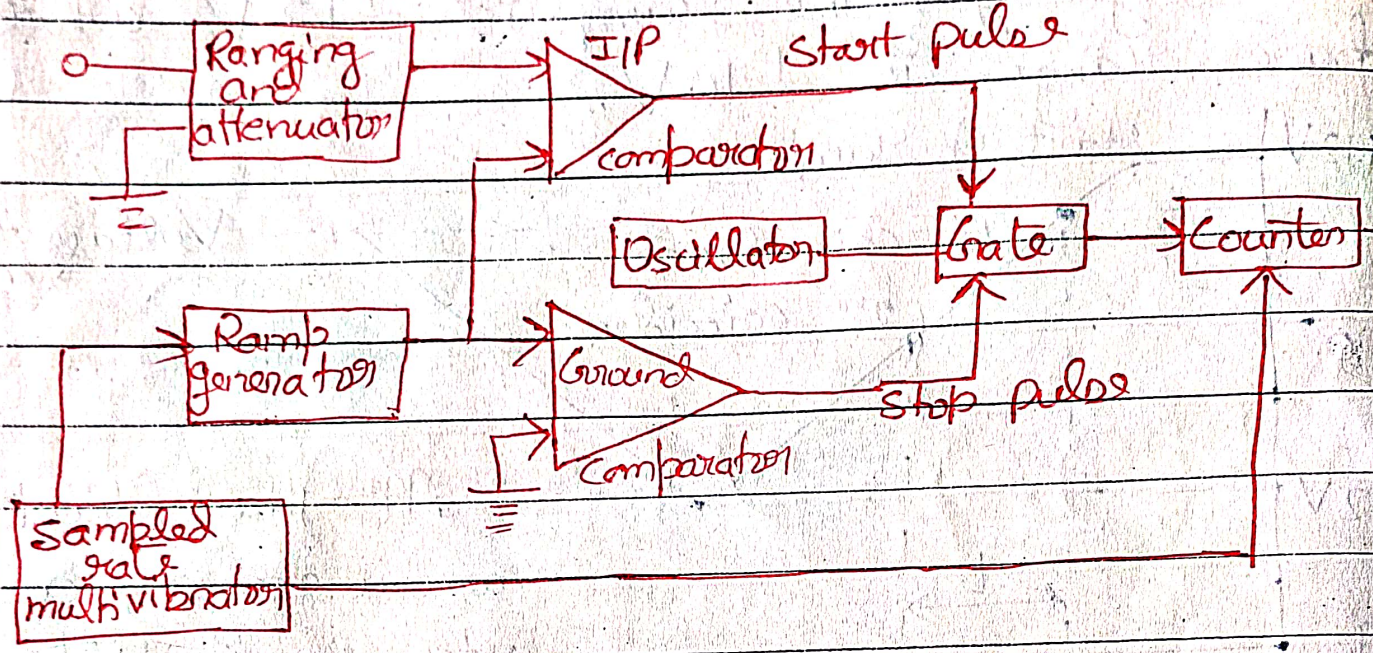
The range of the ramp is ±12V while the base range is ±10V.



- At the start of measurement, a ramp vtg is initiated which is continuously compared with I/P vtg.
- When these two vtgs are same, the comparator generates a pulse which opens a gate i.e I/P comparator generates a start pulse
- The ramp continues to decrease and finally reaches to 0V or ground potential. This is sensed by the second comparator or ground comparator
- At exactly 0V, this comparator produces a stop pulse which closes the gate

f) Vtg to time Conversion.

The no. of clock pulses are measured by co
→ Thus the time duration for which gate
is prop. to I/P vtg.
→ The magnitude of the count indicates the mag
of the I/P vtg, which is displayed by disp



Advantages :-

① ckt is easy to design ② Cost is low.
③ The O/P pulse can be transferred over long freq lines without loss of information.
④ I/P signal is converted to time, which is easy to

Disadvantages :-

→ The accuracy depends on the slope of ramp.
→ Large errors are possible if noise is superimpo on I/P signals
→ Speed of measurement is low.

SECTION C

ANSWER (3A)

BREAKDOWN MECHANISM IN ZENER DIODE:-

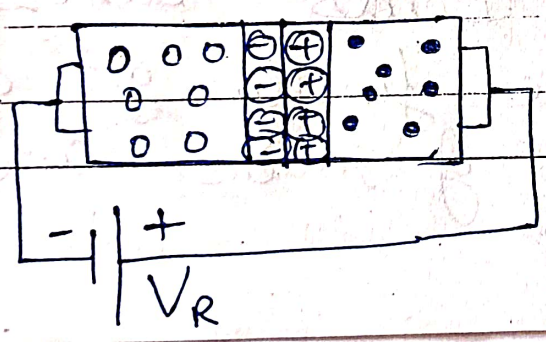
In P-N Junction diode there are two types of breakdown observed while we increase reverse voltage across the diode.

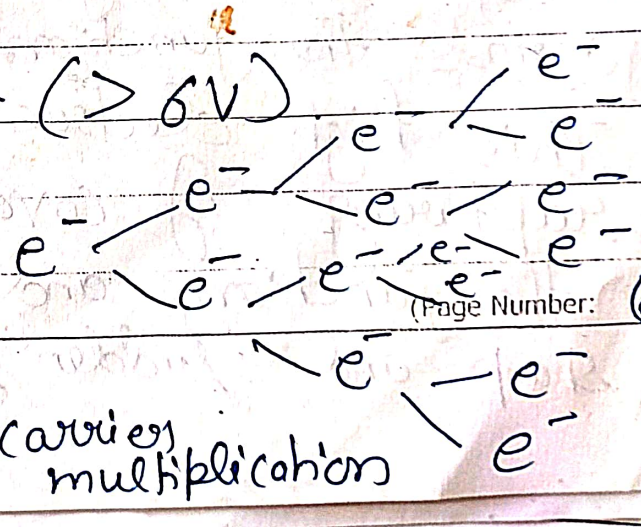
The Breakdown Mechanism are:

(i) Avalanche Breakdown.

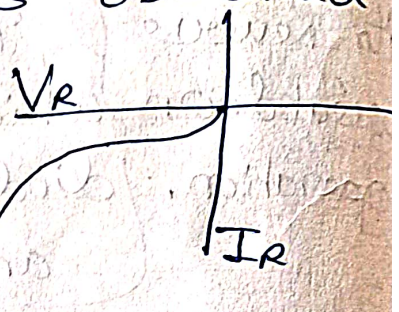
(ii) Zener Breakdown.

1) Avalanche Breakdown- (> 6V)





* It occurs for $V_R > 6V$.
* As we increase V_R, the minority carrie accelerated hence increase KE.
* Now the e^- from P-side collides with nearest atom and break the covalent
* Now the 2 free e^- collide with another atom and produces 4 free e^- in similar
* This way of increasing charge carriers termed as carrier multiplication and sudden increase in current is observed breakdown voltage.



$V_R \uparrow \rightarrow$ charge carriers get accelerated $\rightarrow$ velocity $\uparrow$, Increase gradually

$K.E \uparrow \rightarrow$ minority charge carriers collide with nearest atom $\rightarrow$ Breaks covalent Bond $\rightarrow$ Carrier multipli

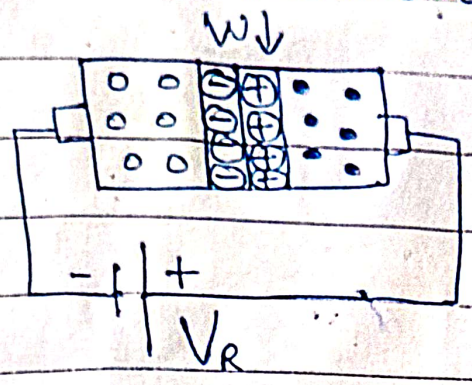
$\downarrow$

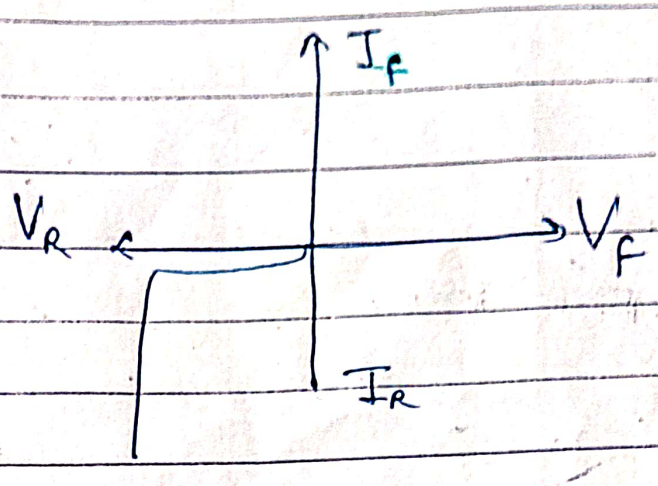
Increase in I at breakdown

2) Zener Breakdown :-

* It is observe for voltage less than 6V.
* The P and N sides are highly doped a compared to Normal P-N jn. diode.
* This result a reduction in depletion laye as compared to normal P-N jn. diode.
* As we know $E = \frac{V}{d}$, as we increase V_R, a high electric field intensity develop across the junction.
* This high electric field intensity results rupturing of covalent Bonds across the junction, and we finally get a sharp and sudden flow of reverse current.

This whole breakdown mechanism is termed as Zener breakdown.





Key points :-

Occurs in $V_R < 6V$

PN Jn diode = Highly doped → Depletion width ↓.

$V_R \uparrow\uparrow \rightarrow \uparrow E = \frac{V}{d}\uparrow \rightarrow$ Rupturing of Covalent Bond ↓ Sharp increase in reverse current.

Comparison b/w Avalanche and Zener Breakdown

Avalanche B.D	Zener B.D.
① It occurs for $V_R > 6V$	① $V_R < 6V$.
② High reverse current flows due to carrier multiplication	② High reverse current flow due to rupturing of Covalent Bond.
③ Reverse current increases gradually	③ Sharp increase in reverse current.
④ +ve temp. coefficient is observed. $V_B \uparrow$ as $T \uparrow$.	④ -ve temp. coefficient is observed. $V_B \downarrow$ as $T \uparrow$

SECTION C

ANSWER (3B)

DIODE RESISTANCE :-

→ The resistance offered by the diode in F.B condition is termed as forward diode resistance.

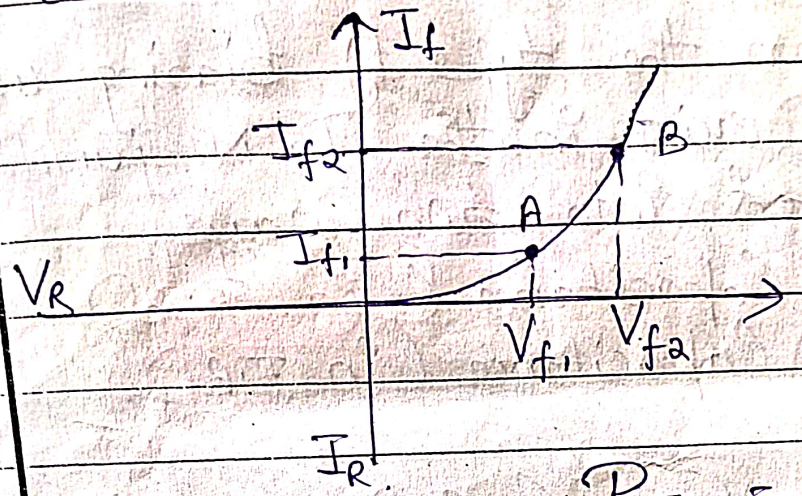
→ The resistance offered by the diode in R.B condition is termed as Reverse diode resistance.

→ This resistive property of a diode is basically due to the formation of Depletion region across the junction of the diode.

→ On the basis of type of supply voltage connected we can also classify diode resistance in two ways :-

Static Resistance (D.C supply)
Dynamic Resistance (A.C supply)
Diode Resistance
1) Forward diode Resistance } Static (D.C)
2) Reverse diode Resistance } Dynamic (A.C)

Forward Diode Resistance.



(i) Static Resistance (D.C).

Static forward Resistance can be given as.

$$R_F (DC) = \frac{V_{F1}}{I_{F1}} \quad \frac{\text{Forward vtg at a pt.}}{\text{forward current at a pt.}}$$

(ii) Dynamic Resistance (A.C)

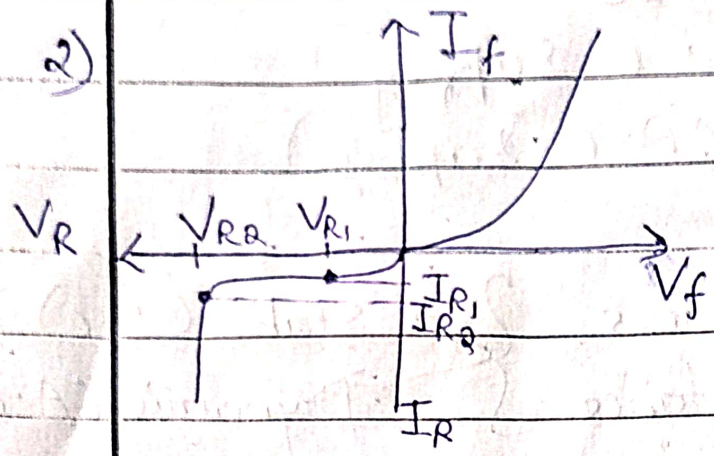
$$r_f (A.C) = \frac{V_{F2} - V_{f1}}{I_{f2} - I_{f1}} = \frac{\Delta V_f}{\Delta I_f}.$$

$$r_f (A.C) = \frac{1}{(\Delta I_f / \Delta V_f)} = \frac{1}{\text{Slope of forward Ch.}}$$

2) Reverse Diode Resistance:-

(i) Static Reverse resistance (DC).

$$R_r = \frac{V_{R1}}{I_{R1}} \quad \frac{\text{Reverse vtg at a point}}{\text{Reverse current at that point.}}$$

2) 

Dynamic Reverse resistance (A

$$r_n = \frac{V_{R2} - V_{R1}}{I_{R2} - I_{R1}}$$

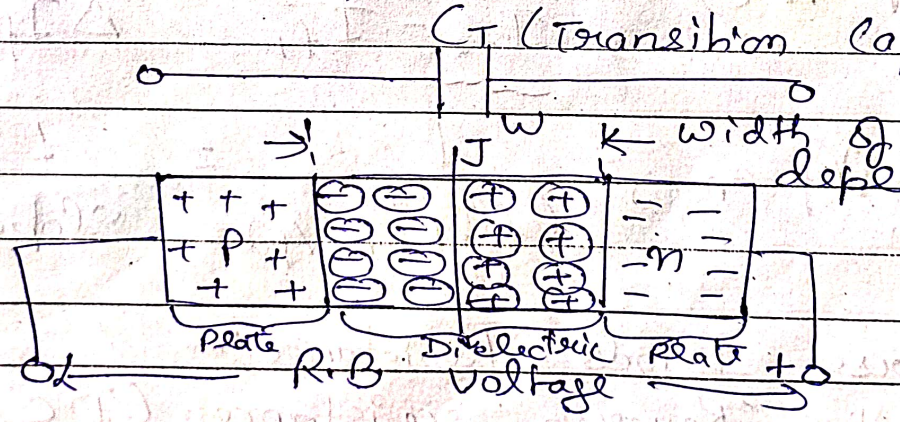
DIODE CAPACITANCE :-

Depending upon the type of biasing we Capacitive effect exist in the P-N junction can be classified into two ways.

(1) Transition Capacitance (in R.B)
(2) Diffusion Capacitance (in F.B.)

1) Transition Capacitance (C_T) :-

→ The capacitive effect that took place in R.B condition of a diode is termed as Transition Capacitance denoted by C_T.



Mathematically it is expressed as

$$\boxed{C_T = \frac{\varepsilon A}{W}}$$

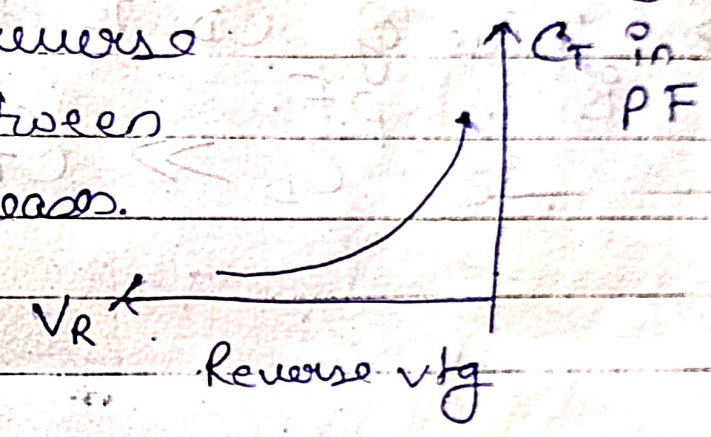
where $\{V_R \uparrow = W \uparrow = C_T \downarrow\}$

ε = permittivity of SC $= \varepsilon_0 \varepsilon_r$

$\varepsilon_0 = \frac{1}{36\pi \times 10^9}$ $= 8.89 \times 10^{-12}$ F/m

ε_r = relative permittivity of SC.
Ge (16) and Si (12).

A = area of crosssection and W = Width of depletion region



As we increase the reverse voltage, the distance between two parallel plates increases. In result the transition capacitance decreases.

→ It is also known as junction capacitance, barrier capacitance or depletion region capacitance

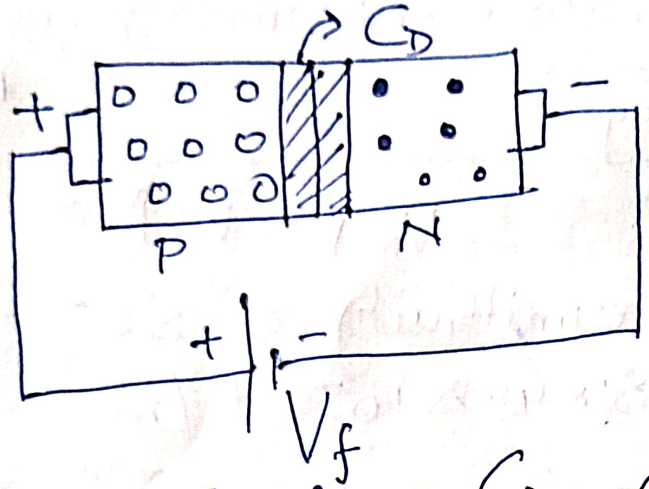
DIFFUSION CAPACITANCE :-

The capacitive effect that takes place when the diode is in F.B condition, is termed as Diffusion Capacitance & is denoted as (C_D)

As we increase the forward voltage, ~~the~~ more charge carriers diffuses across the junction

→ As a result the rate of flow of charge carriers w.r.to the applied forward voltage increases.

→ That in turn increases the C_D.



As we know.

$$C_D = \frac{dQ}{dV}$$

→ Mathematically C_D can also be expressed

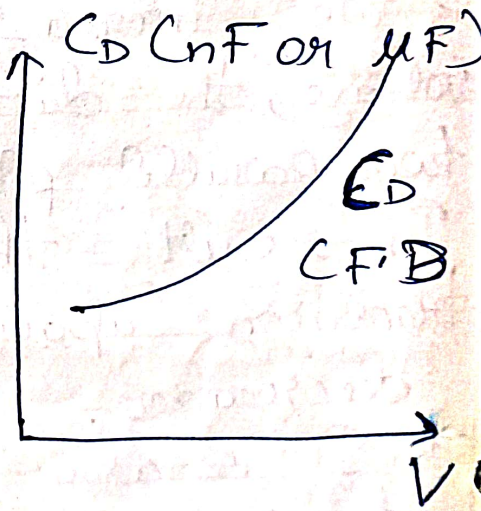
$$C_D = \frac{\tau I}{\eta V_T}$$

where τ = Mean life time for holes

→ So diffusion Capacitance is proportional to I.

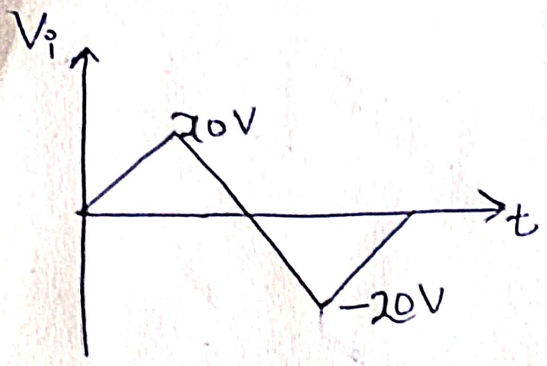
→ Value of C_D is nF to μF. while C_T is in pF.

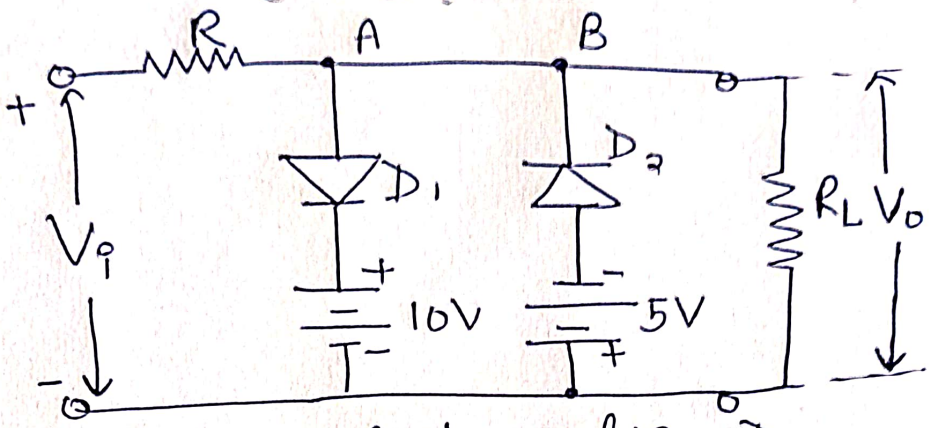
So $C_D \gg C_T$.



SECTION C

ANSWER (4A)





When $V_i > V_A$, Diode D_1 conducts while D_2 remains off. So circuit reduces as shown in fig (a)

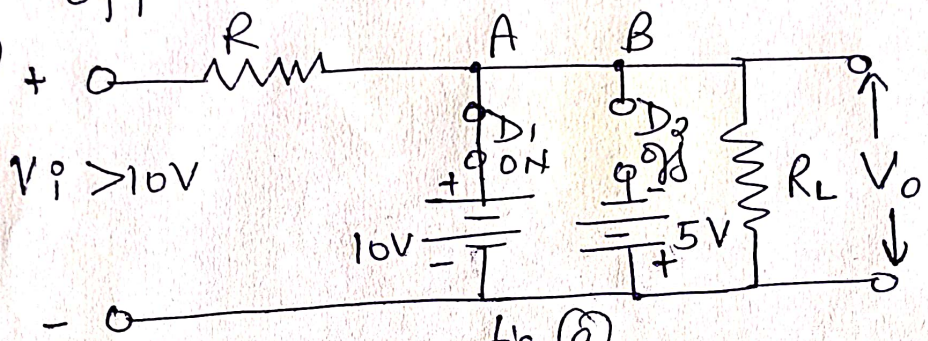
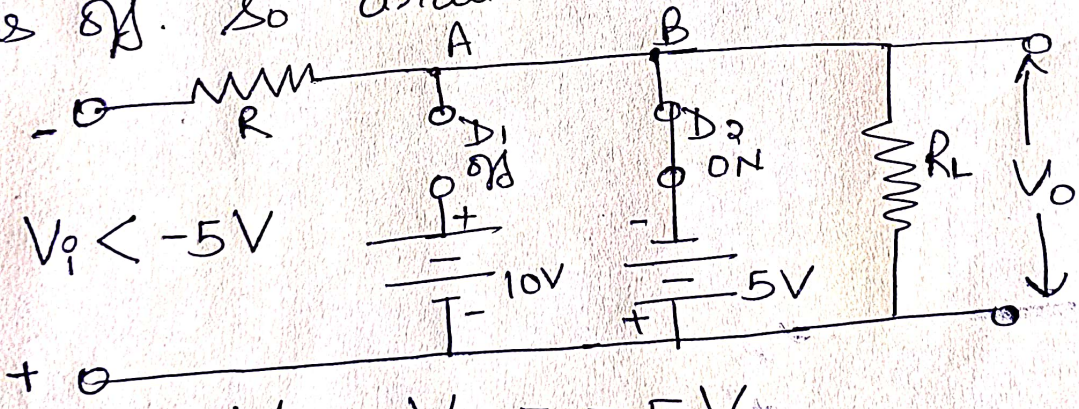


fig (a).

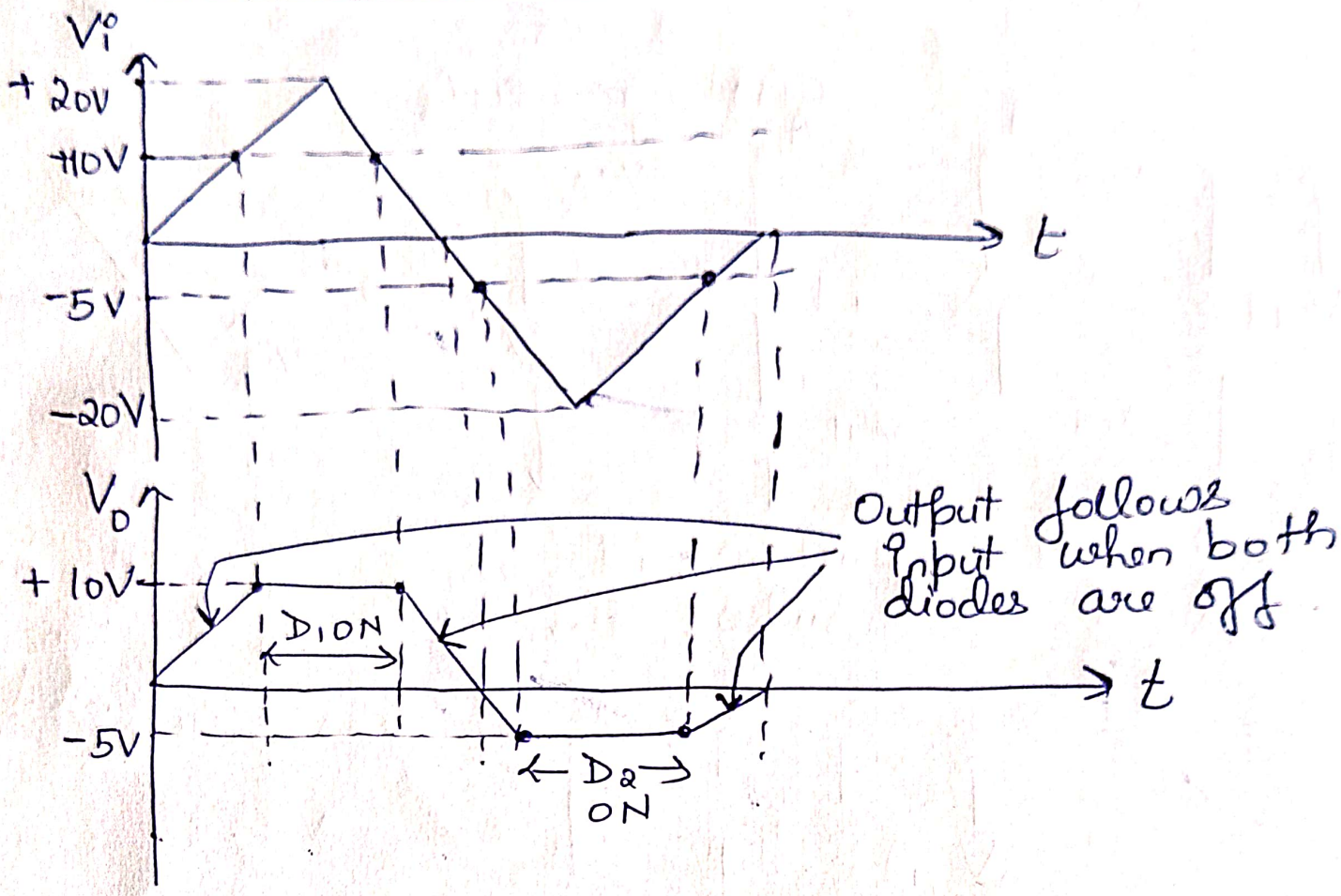
Thus $V_o = V_A = 10V$ —— (1)

When $V_i < V_B$, Diode D_2 conducts while D_1 remains off. So circuit reduces as shown in fig (b)



Thus $V_o = V_B = -5V$.

When $V_i < 10V$ and $V_i > -5V$, the output follows the input as both diodes remain Reverse Biased.


V_i
+20V
+10V
-5V
-20V
t
V_o
+10V
-5V
D_1 ON
D_2 ON
t
Output follows input when both diodes are off

SECTION C

ANSWER (4B)

VOLTAGE MULTIPLIERS :-

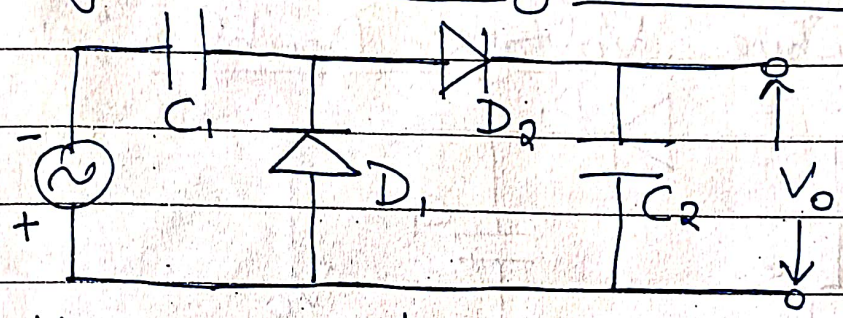
→ The vtg multipliers are used to step up the O/P vtg level to two, three or more times the peak voltage of the input.

→ The various voltage multiplier ckts are,

1) Voltage doubler 2) Voltage tripler 3) Voltage quadrapler

→ Each circuit is further classified as (a) Half wave multiplier (b) Full wave multiplier

1) Half Wave Voltage Doubler :-



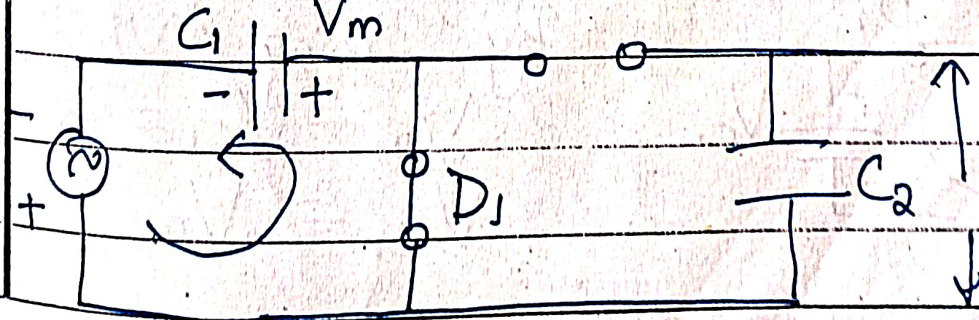
* Here we take that cycle by which the capacitor C_1 get charged because of diode.

→ For ⊖ve Half cycle :-

We take ⊖ve half cycle because in the cycle capacitor C_1 get charged.

$D_1 \rightarrow$ F.B (ON switch)

$D_2 \rightarrow$ R.B (OFF switch)



$V_{C_1} = V_m$

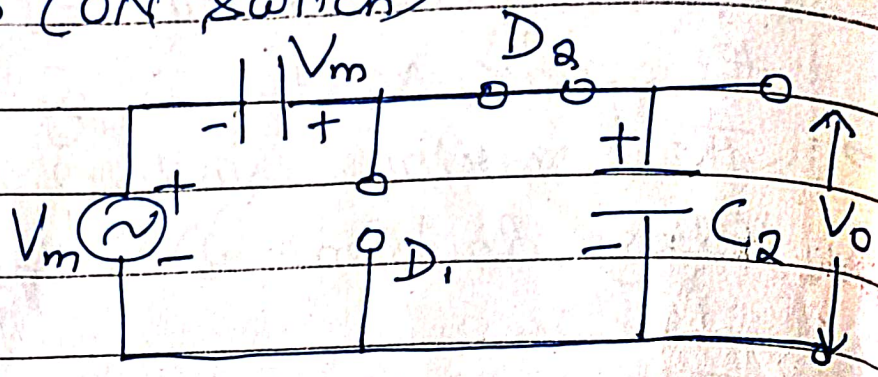
$V_{C_2} = 0$

$V_o = 0$

For One Half cycle :-

Diode $D_1 \rightarrow$ R.B (OFF switch)

Diode $D_2 \rightarrow$ F.B (ON switch)



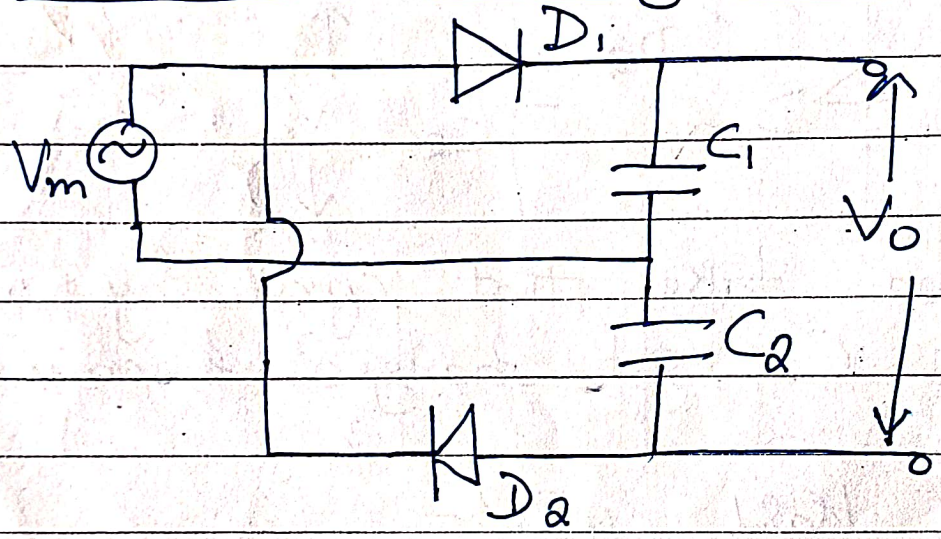
By KVL.

$V_m + V_m - V_{C_2} = 0$

$V_{C_2} = 2V_m$.

$\therefore \boxed{V_o = 2V_m}$

ii) <u>Full Wave Voltage Doubler</u> :-

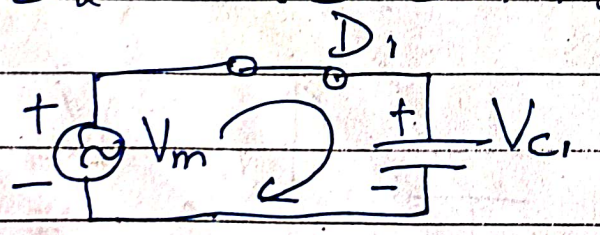


Working :-

For One half cycle

$D_1 \Rightarrow$ F.B (ON) C_1 get charged.

$D_2 \Rightarrow$ R.B (OFF)

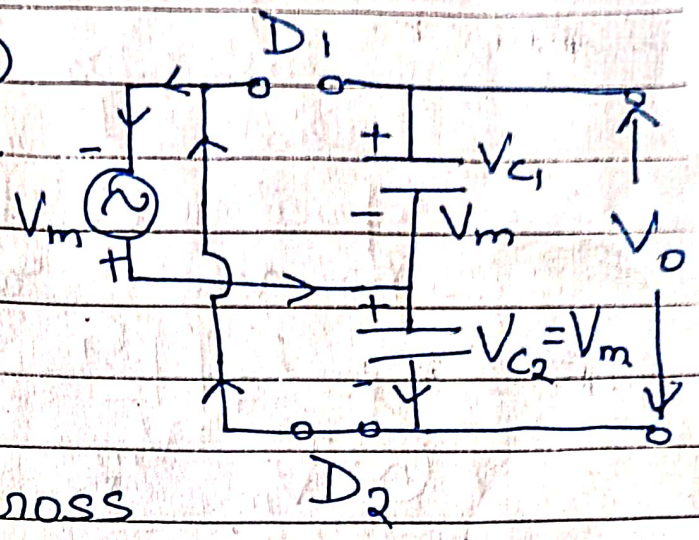


By using KVL

$V_m - V_{C_1} = 0$.

$V_{C_1} = V_m$.

For ⊖ve half cycle.
diode $D_1 \rightarrow$ R.B (OFF)
diode $D_2 \rightarrow$ F.B (ON)



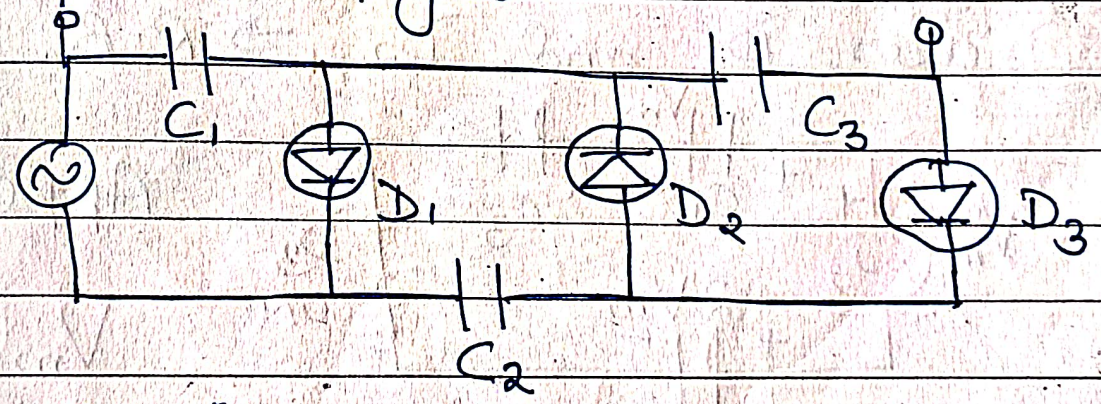
By using KVL
$V_m - V_{C2} = 0$
$V_{C2} = V_m$.

The final output across both capacitor C_1 and C_2.

$$\boxed{V_o = 2V_m.}$$

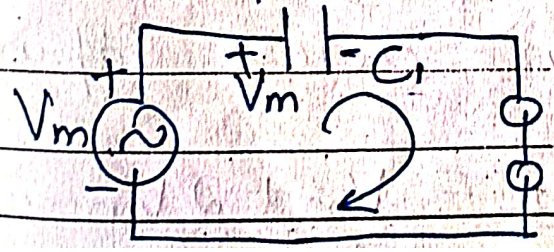
VOLTAGE TRIPLER :-

A voltage tripler is a circuit which gives the DC output to the triple of peak value of input AC signal.



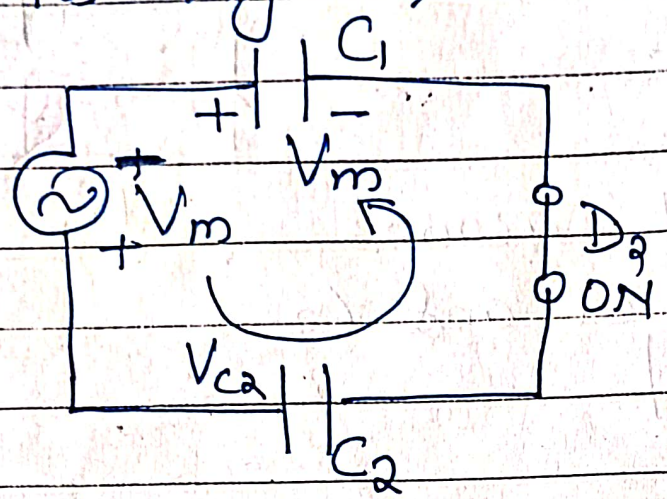
Operation :-

During first ⊕ve half cycle, Diode D_1 is FB and D_2, D_3 are R.B.



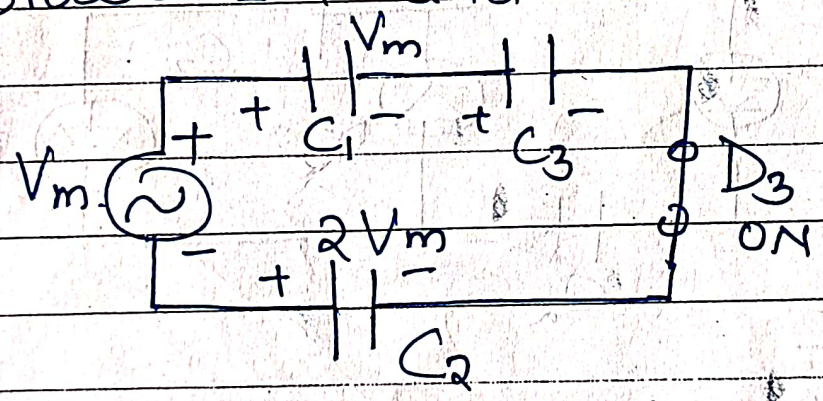
Capacitor C_1 charges to V_m.
$V_{C1} = V_m$.

* During next negative half cycle.
Diode $D_2 \rightarrow$ F.B. (ON)
Diode $D_1, D_3 \rightarrow$ R.B. (OFF)
Capacitor C_1 holds its entire charge and its vtg remains at V_m.



Applying KVL.
$+V_m - V_{C2} + V_{C1}$
i.e. $V_{C2} = V_m + V$
$V_{C2} = 2V_m$.

* In next +ve half cycle, Diode D_3 because C_2 retains its charge & vtg across it to $2V_m$ and at C_1 to
* Diodes D_1 and $D_2 \rightarrow$ R.B.



Applying K
$V_m - V_m -$
$+ V_{C2} =$
$V_m - V_m - V_{C3} + 2V$
$V_{C3} = 2V_m$.

The V_o is taken across capacitor C_1 and C_3.
$V_o = V_{C1} + V_{C3} = V_m + 2V_m$
$= 3V_m$.

SECTION C
ANSWER (5A)

Emitter follower Configuration

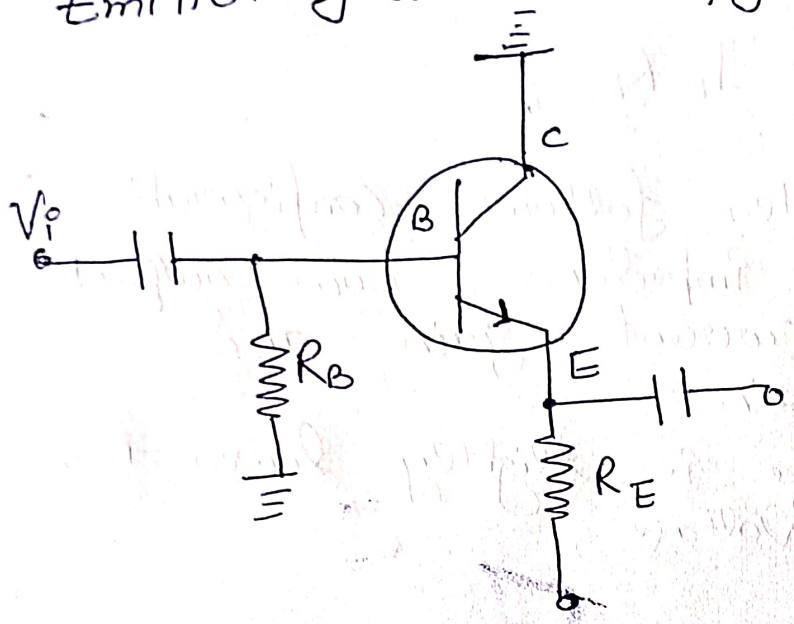


fig (a) Emitter follower Configuration

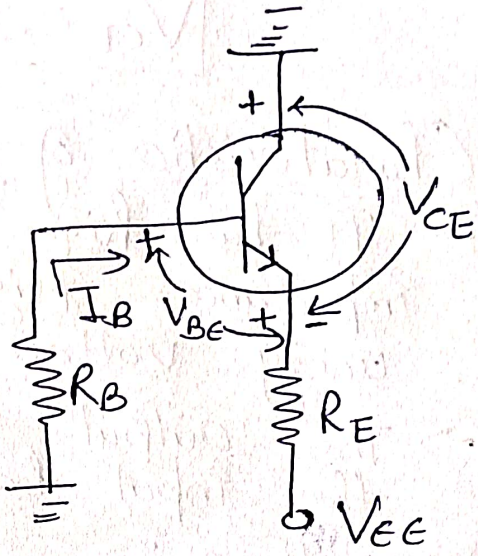


fig (b) DC Equivalent.

1) Base Circuit :- (Input Circuit)

Applying KVL to the base circuit we get :-

$$V_{EE} - I_E R_E - I_B R_B - V_{BE} = 0$$

$$V_{EE} - (1+\beta) I_B R_E - I_B R_B - V_{BE} = 0 \quad \left\{ \because I_E = (1+\beta) I_B \right.$$

$$V_{EE} = I_B[(1+\beta) R_E + R_B] - V_{BE} = 0$$

$$\boxed{I_B = \frac{V_{EE} - V_{BE}}{(1+\beta) R_E + R_B}}$$

② Emitter Circuit (Output Circuit) :-

Applying KVL to output circuit, we get.

$$V_{EE} - I_E R_E - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{EE} - I_E R_E}$$

Charateristics of Emitter follower configuration :-

→ It has high input impedance, Low output impedance, High current gain and unity voltage gain.

→ The output voltage is slightly lower than the input base voltage.

Applications :-

→ Used in power supplies, buffer amplifiers and driving heavy loads.

→ Also used to match high impedance circuitry to low resistance loads.

Advantages :-

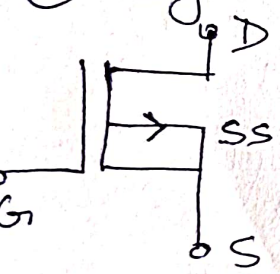
→ It is a simple circuit that requires only a few electronic components.

→ It's also a negative current feedback circuit.

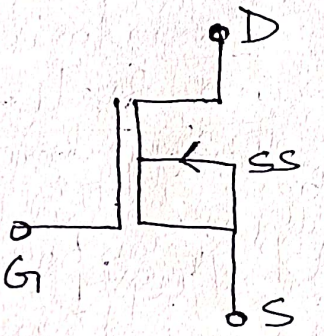
SECTION C

ANSWER (5.B)

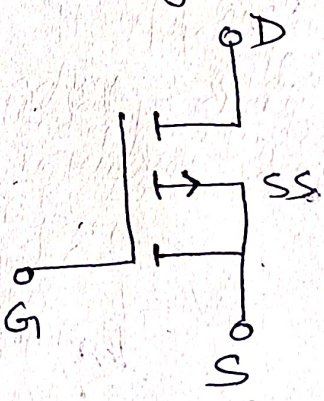
Depletion MOSFET	Enhancement MOSFET
① Channel exist	① No Channel exist
② Types → N Channel D-MOS; → P Channel DMOS	② Types → N Channel EMOSFET; → P Channel EMOSFET.
③ when $V_{GS}=0$, $I_D=$ max.	③ when $V_{GS}=0$, $I_D=0$
④ Channel gets depleted by charge carriers	④ Channel gets enhanced by charge carriers.
⑤ N-Channel $\{V_{DS}=\oplus ve,\ V_{GS}=\ominus ve$; P-Channel $\{V_{DS}=\ominus ve,\ V_{GS}=\oplus ve$	⑤ N Channel $\{V_{DS}=\oplus ve,\ V_{GS}=\oplus ve$; P channel $\{V_{DS}=\ominus ve,\ V_{GS}=\ominus ve$
⑥ Symbol.	⑥ Symbol.



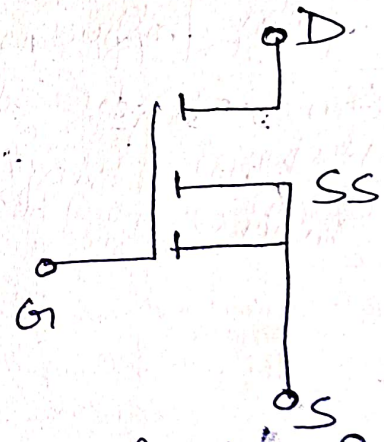
N- channel



P channel



N-channel



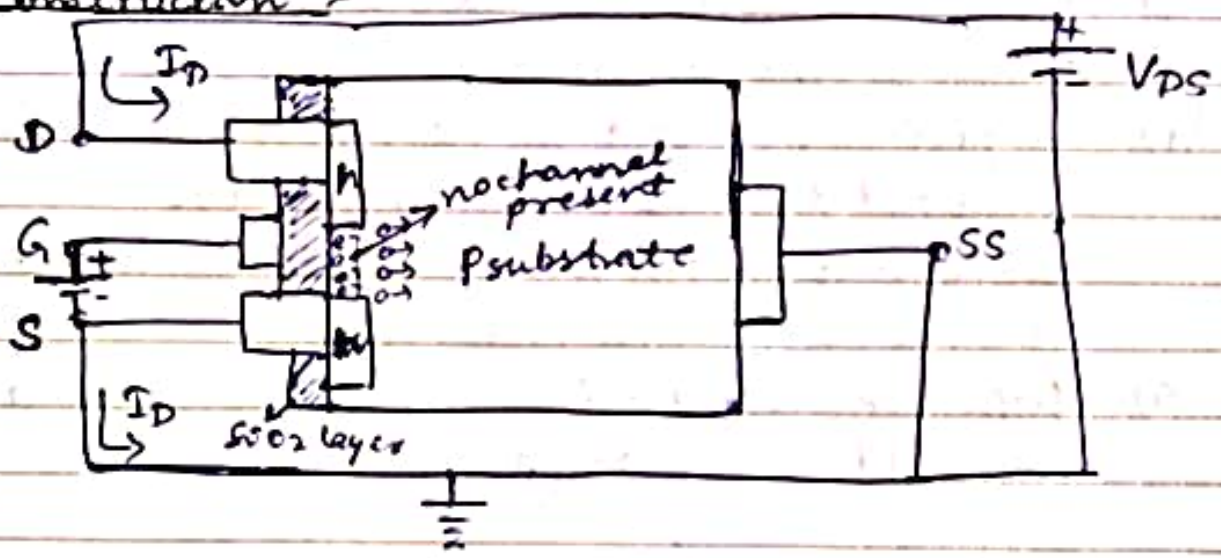
P- channel

Enhancement MOSFET (E-MOS)

There is no physical channel present in between drain and source we enhance the channel by applying suitable voltage at gate terminal.

① N-channel Enhancement MOSFET (EMOS n channel) →

Construction →

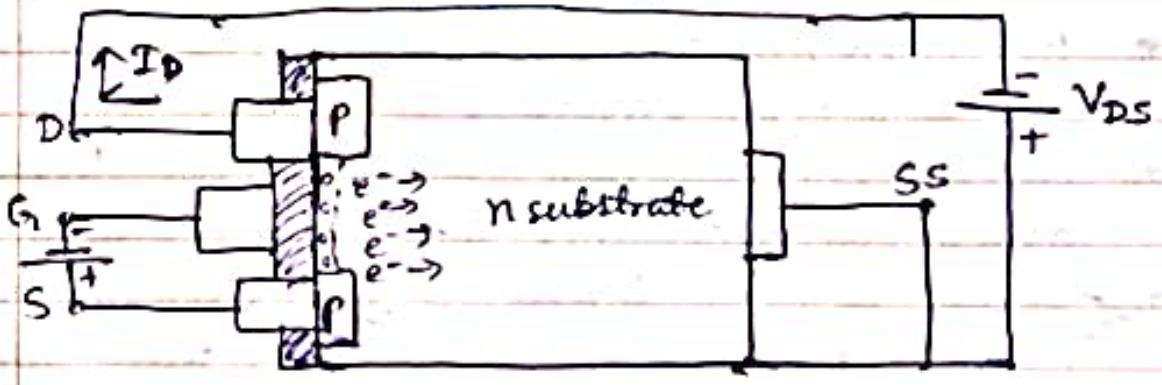


* To highly doped n-regions, are diffused into lightly doped p-type substrate.
* The source and drain are taken out through n-type doped region, channel b/w two n regions is absent
* Silicon dioxide is present to isolate the gate metallic platform from the region b/w drain and source and separated from a section of p-type material.

Working →

1) Apply a +ve voltage in b/w drain and source terminal, there is no channel present in b/w drain and source, so $I_D = 0$.
2) Apply a +ve voltage in b/w gate and source which is termed as V_{GS}.
3) Now, the electrons move towards gate terminal from p-type substrate.
4) At particular voltage V_{GS}, at which channel is induced known as threshold V_{tg}.
Because of this n-channel induced b/w drain and source, I_D starts flowing.
5) With the increase in V_{GS}, I_D increases after threshold V_{tg} is reached.

② P-Channel E-MOSFET →



* Apply a negative voltage in b/w drain and source which is termed as V_{DS} voltage. The holes of p-region which is connected to drain p-region are attracted by negative terminal V_{DS} at the same time, the holes of p-region which is connected to source terminal are repelled by +ve terminal of voltage V_{DS}.

SECTION C

ANSWER (6A)

Given $V_o = -[2V_1 + 4V_2 + 5V_3]$ — (i)

V_1, V_2 and V_3 are input voltages.

We know that :-

For Summing amplifier (Adder circuit) with input applied at inverting terminal

$$V_o = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right] \text{ — (ii)}$$

Let us assume $R_f = 100\,k\Omega$.

Comparing eq (i) and (ii) we get.

$$\Rightarrow \frac{R_f}{R_1} = 2 \quad \text{or} \quad \frac{100 \times 10^3}{R_1} = 2.$$

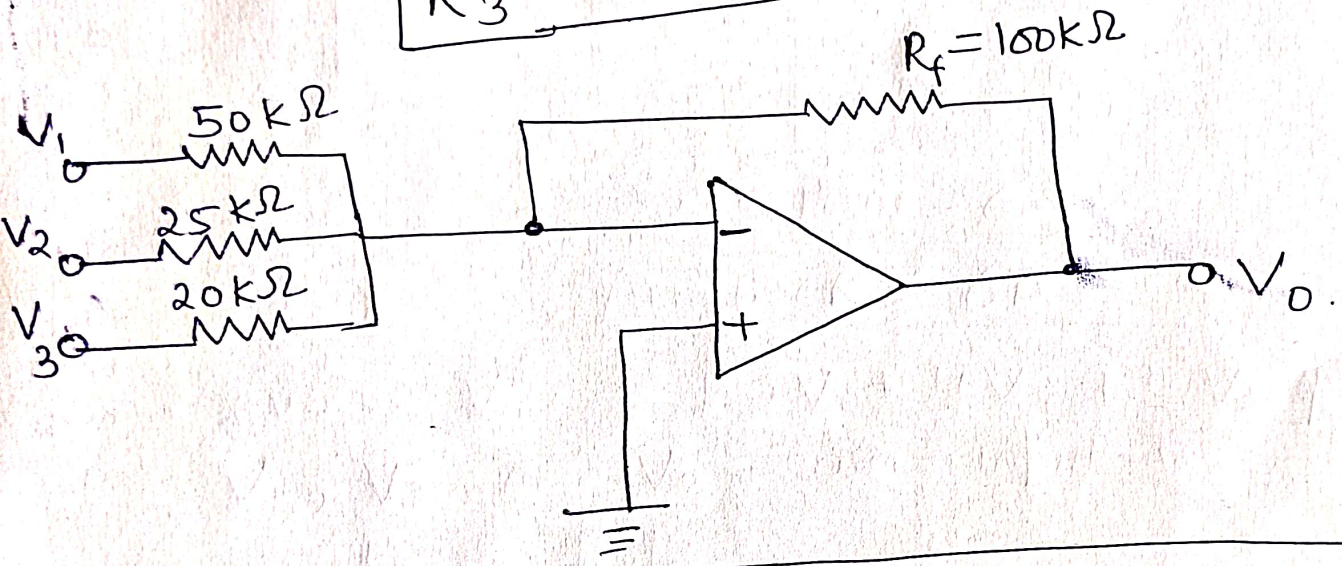
$$\boxed{R_1 = 50\,k\Omega}$$

$$\Rightarrow \frac{R_f}{R_2} = 4 \quad \text{or} \quad \frac{100 \times 10^3}{4} = R_2.$$

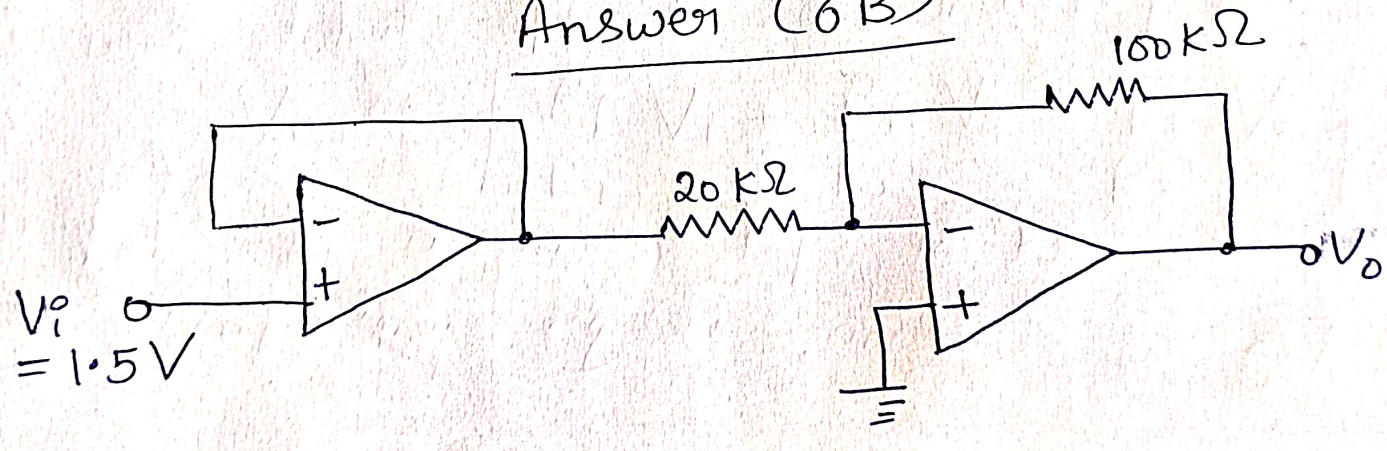
$$\boxed{R_2 = 25\,k\Omega}$$

$$\Rightarrow \frac{R_f}{R_3} = 5 \quad \text{or} \quad \frac{100 \times 10^3}{5} = R_3$$

$$\boxed{R_3 = 20\,k\Omega}$$



SECTION C
Answer (6B)



In the given op-amp circuit,
First part is a unity gain amplifier or Voltage follower.

Since $V_i = 1.5\ V$.

So $V_{o1} = 1.5\ V$ (By Voltage follower)

Now in second op-amp V_{in} will be 1.5V at inverting terminal.

So $V_o = \left(-\frac{R_f}{R_1}\right) V_{in}$.

$$V_o = -\frac{100 \times 10^3}{20 \times 10^3} \times 1.5$$

$$\boxed{V_o = -7.5\ V}$$

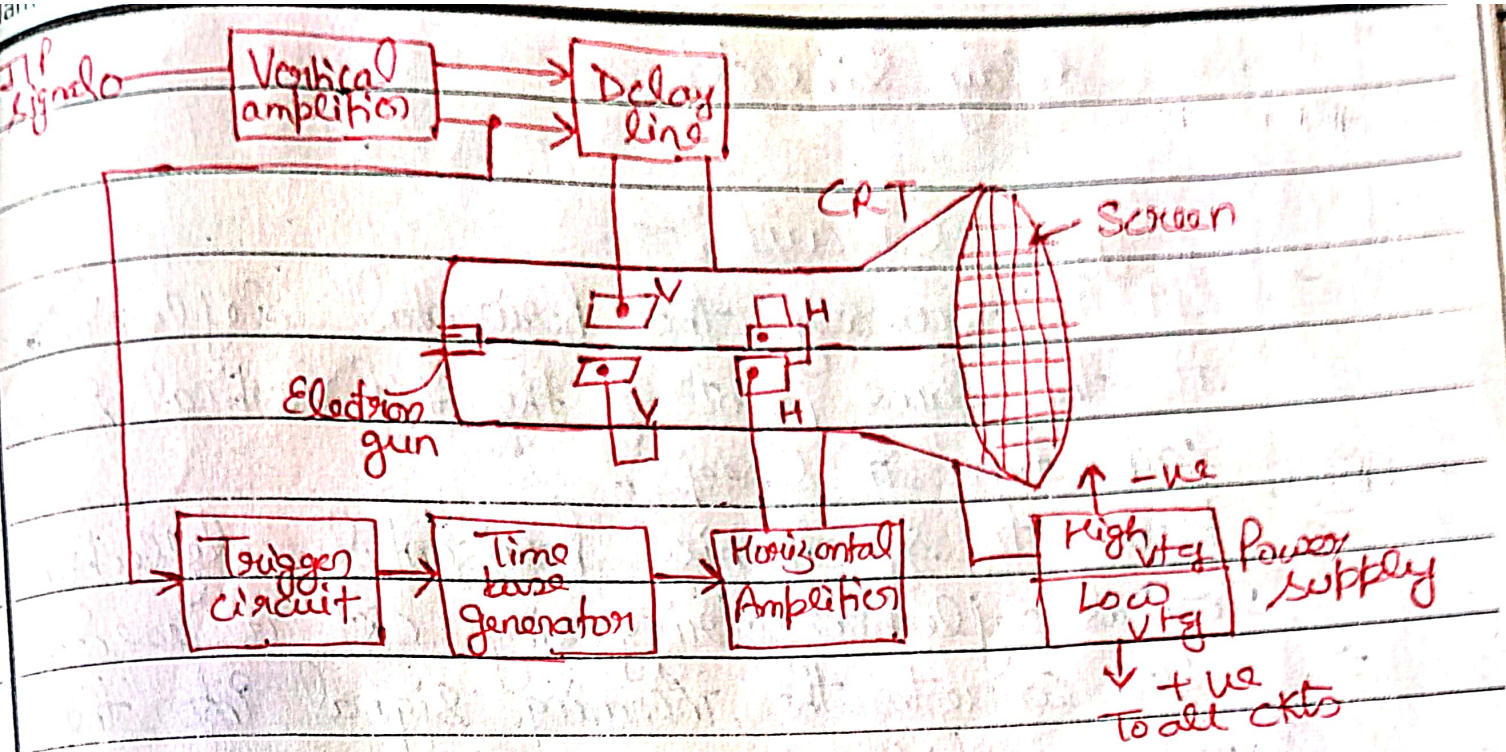
SECTION C

ANSWER (7A)

BLOCK DIAGRAM OF SIMPLE CRO :-

CRT :-

It is used to emit e^-s required to strike the phosphor screen to produce the spot for the visual display of the signals.



Vertical Amplifier :-

→ It is used to amplify the input signals.
→ The amplifier stages used are generally wide band amplifiers so as to pass faithfully the entire band of frequencies to be measured.
→ Similarly it contains the attenuator stages as well. The attenuators are used when very high vtg signals are to be examined, to bring the signals within the proper range of operation.

Delay Line :-

→ It is used to delay the signal for some time in the vertical sections.
→ When the delay line is not used, the part of the signal gets lost. Thus the I/P signal is not applied directly to the vertical plates but is delayed by some time using

a delay line ckt.

(4) Trigger Circuit :-

→ It is necessary that horizontal deflection start at the same point of the I/P vertical signal, each time it sweeps.

→ Hence to synchronize horizontal deflection with vertical deflection triggering ckt is used.

→ It converts the incoming signal into the trigger pulses, which are used for the synchronization.

(5) Time Base Generator :-

→ It is used to generate the sawtooth vtg required to deflect the beam in horizontal sech.

→ This vtg deflects the spot at a constant time dependent rate. Thus the x-axis on the screen can be represented as time, which helps to display & analyse the time varying signals.

(6) Horizontal Amplifier :-

→ The sawtooth vtg produced by the time base generator may not be of sufficient strength. Hence before giving it to the horizontal deflection plates, it is amplified using the horizontal amplifier.

Power Supply :- There are two sections of a power supply block which are HV & LV section. It provides the vtg required by CRT to generate & accelerate an e^- beam and vtgs required by other ckts of the oscilloscope like horizontal amplifier, vertical amplifier etc.

Measurement of Period and Frequency :-

Period $T = \left(\frac{\text{time}}{\text{Division}}\right) \times$ (No. of divisions occupied by 1 cycle).

The freq. is the reciprocal of period :

$$\boxed{f = \frac{1}{T}}$$

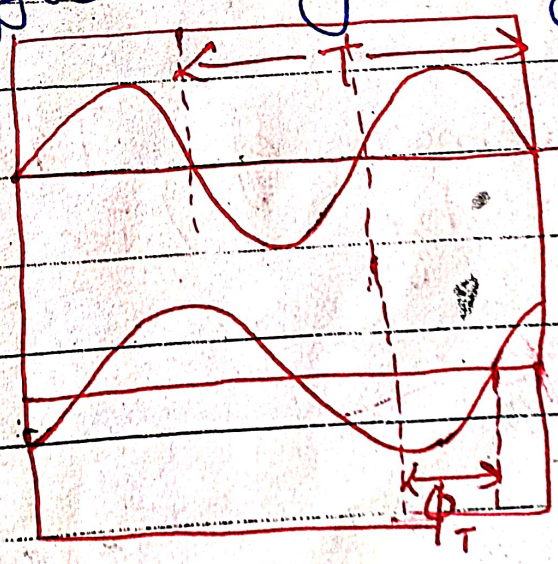
Subject Code:

Phase Measurement :-

Phase b/w two input signals can be obtained by measuring Phase shift as follows:-

1) Display two signal on CRO.
2) Using GND position of switches AC-GND-DC, Allign the time base of both the channels with horizontal lines
3) Using AC position of switches AC-GND-DC, CRO screen will display both the signals.
4) Measure the time phase difference in terms of number of division i.e ϕ_T.
5) Measure the time period of both signals and ensure the signals to be of same time periods.
6) Calculate phase difference by using formula.

$$\phi = \frac{\phi_T \times 360^\circ}{\text{Time period}}$$



SECTION C

ANSWER (7B)

DIGITAL MULTIMETERS (DMM) :-

→ DMM is an instrument which is capable of measuring a.c. vtgs, d.c vtgs, a.c and d.c. currents and resistances over several ranges and display the reading in digital form.

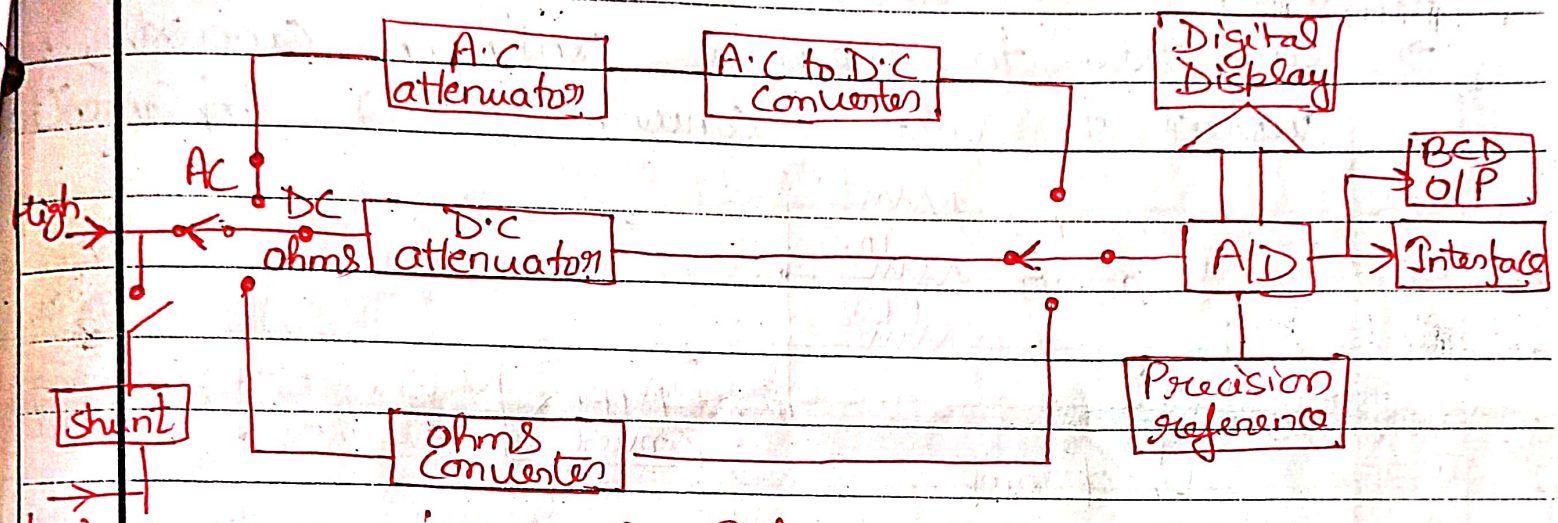


fig) Basic Scheme of Digital Multimeter.

→ The current is converted to vtg by passing it through low shunt resistance.

→ The a.c quantities are converted to d.c by employing various rectifier and filtering ckts.

→ All the quantities are digitized using A/D converter & displayed in the digital form on display

→ Advantages of DMM :-

- Accuracy is very high
- I/P impedance is very high
- Available in very small size.
- Due to improvement in Integrated tech. prices are going low.

→ The basic building blocks of DMM are ser
A/D converters, Counting circuitry & attenuation
→ Generally dual slop integration type ADC is pr
in the multimeters
→ The single attenuator ckt is used for both
and d.c measurements in many commercial M
→ In order to measure unknown currents,
current to voltage converter ckt is implemen

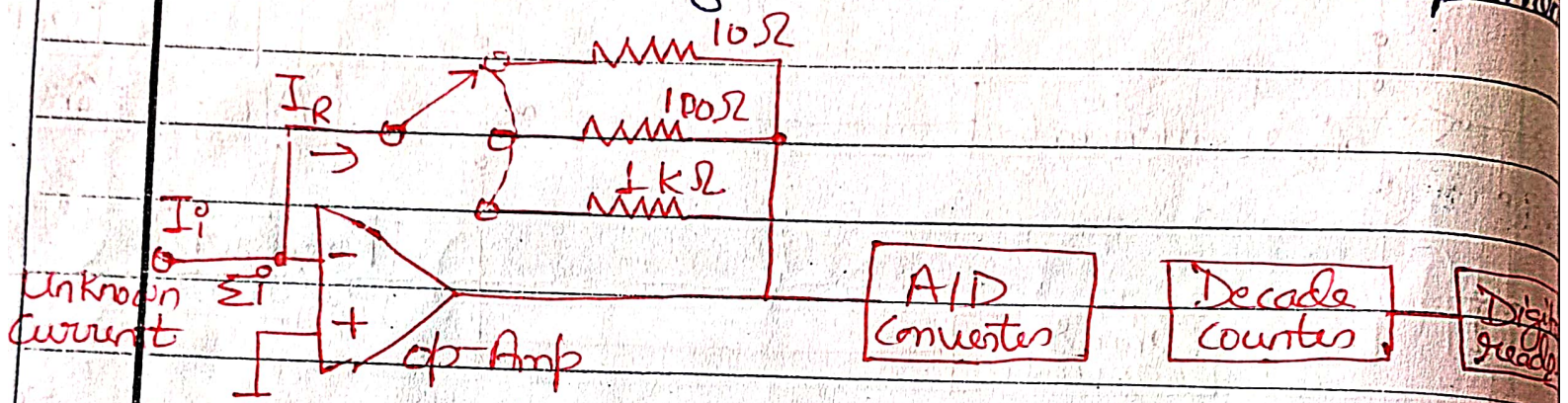


fig) Current to voltage Converter.

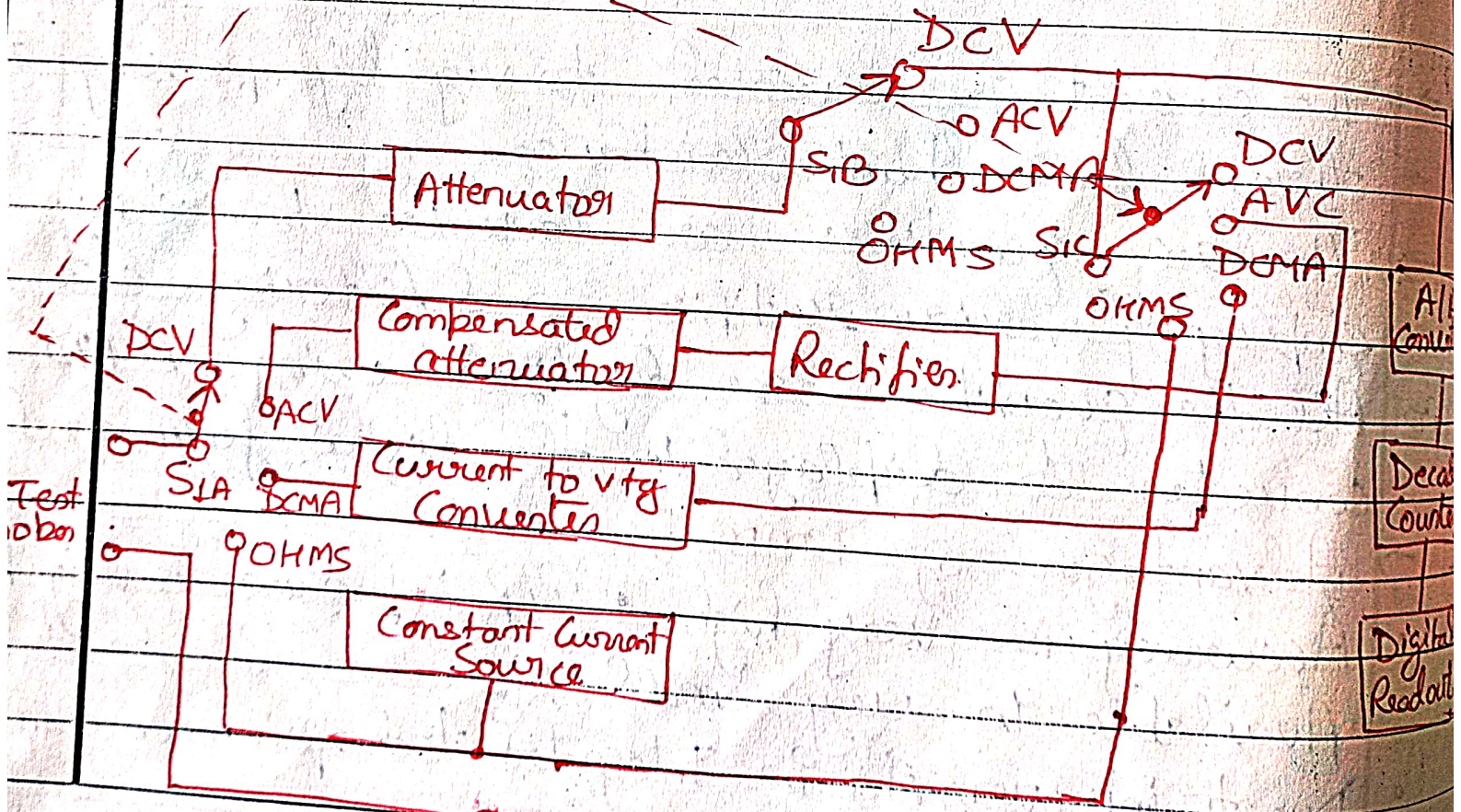


fig) Block diagram of a DMM

Specifications of DMM :-

1) DC Voltage :-

(i) Five voltage ranges are available. Vtg range is from ± 200 mV to ± 10
(ii) Accuracy is about ± 0.03 % (iii) Re
10 μV.

2) AC Voltage :-

(1) Five vtg ranges are available. The vt
is from 200 mV to 750 V.
(2) Accuracy is dependent on freq. Best
is about 0.5 %
(3) Resolution is about 10 μV.

3) Resistance :-

(1) Generally six resistance ranges are ava
200 Ω to 20 MΩ (2) Accuracy is about ±

4) DC Current :-

1) Range is from ± 200 μA to ± 2000 mA.
(2) Accuracy is about ± 0.3 %. (3) Resolution ±

5) AC Current :-

(i) Five current ranges are available.
Range is from ± 200 μA to 2 A.
(ii) Accuracy is dependent on frequency
± 1 %.