25 Spring ECEN 607: Advanced Analog Circuit Tech Design Post-lab Report

Lab3: Op Amp Design - I

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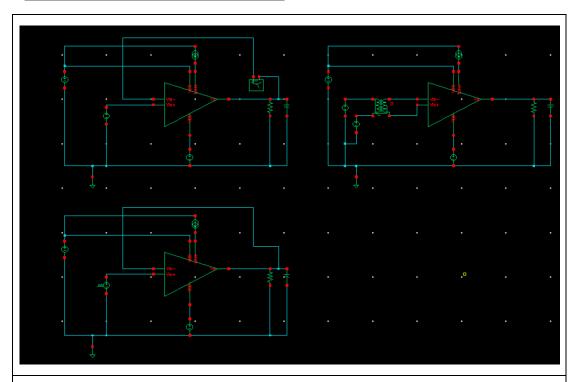
Section:601

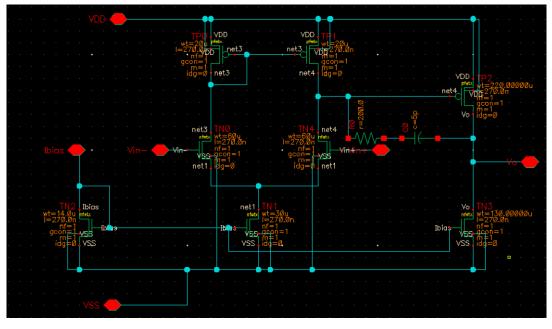
Professor: Jose Silva-Martinez

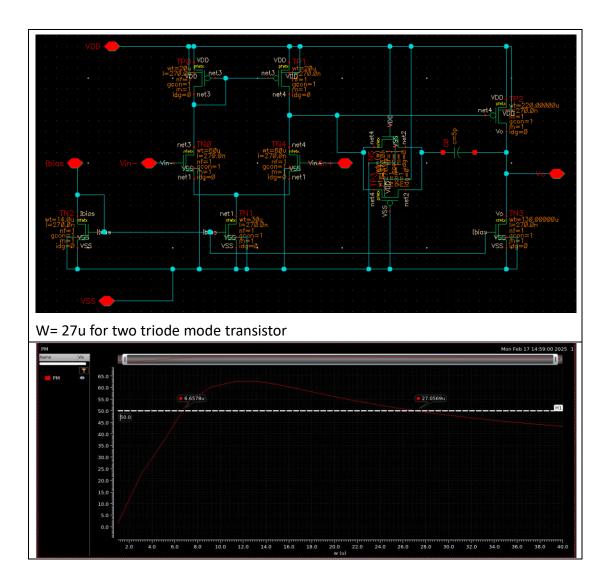
TA: Yoon, Sung J

Table 2-1: Design specifications

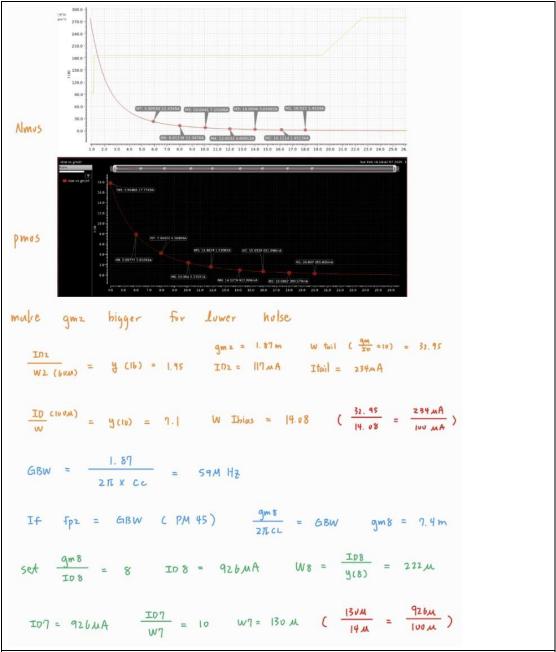
1 abic 2-1. Design specifications				
$V_{ m DD}$ - $V_{ m SS}$	1.8V			
A_{v0}	> 40 dB			
GBW	> 2 MHz			
PM	> 45°			
Output Swing	> 1 V			
C_{L}	20 pF			
$R_{\rm L}$	20kΩ			
Integrated input referred noise	< 30 μVrms			
(10 Hz - 2 MHz)				





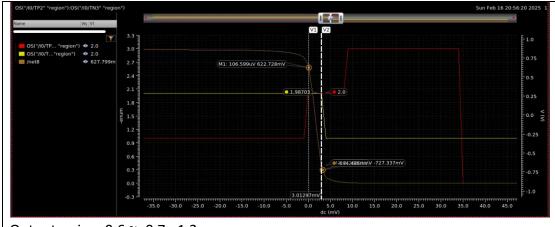


1. Simulate the circuit from the prelab and adjust the transistor sizes accordingly.

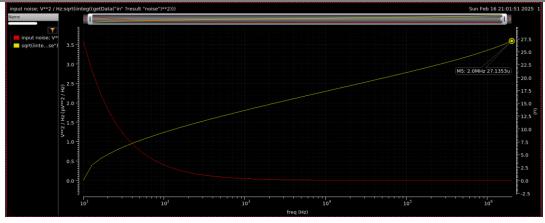




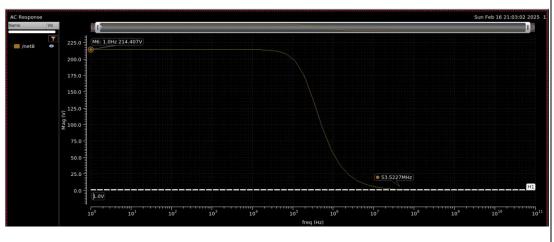
Vcm range



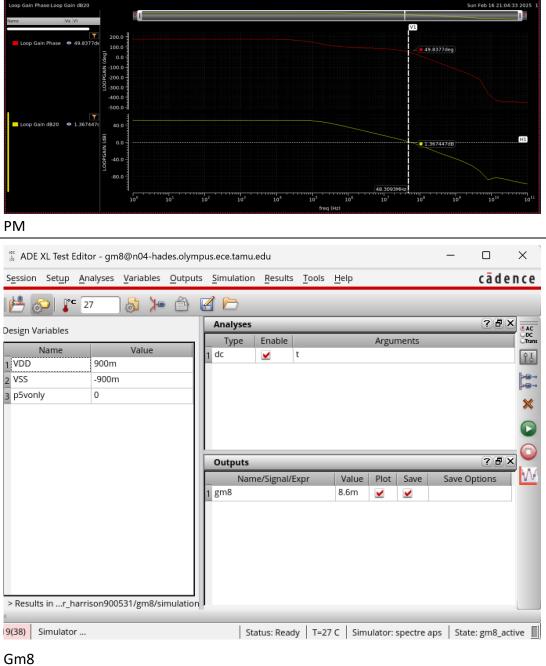
Output swing: $0.6 \sim -0.7 = 1.3v$



Input ref noise

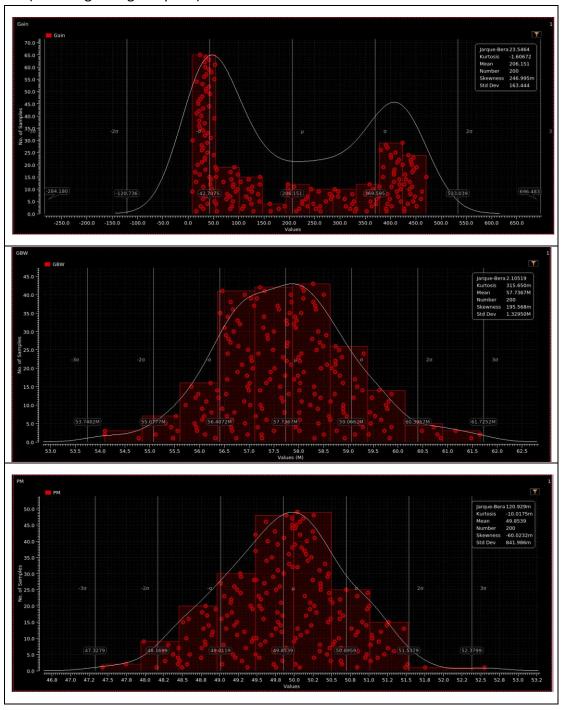


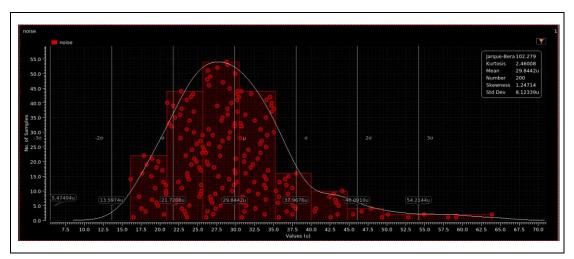
GBW & Av0



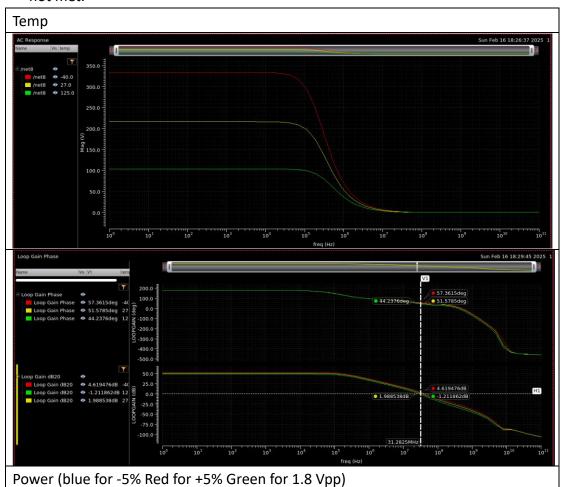
Test	Output	Nominal	Spec	Weight	Pass/Fail
AC	/net8	<u>~</u>			
AC	Gain	214.4			
AC	net8	<u>L</u>			
stability	GBW	61.95M			
stability	PM	45.49			
stability	/I0/TP2	<u>L</u>			
noise	noise	27.14u			
gm8	gm8	8.6m			
gm8	/I0/TP2	<u>L</u>			

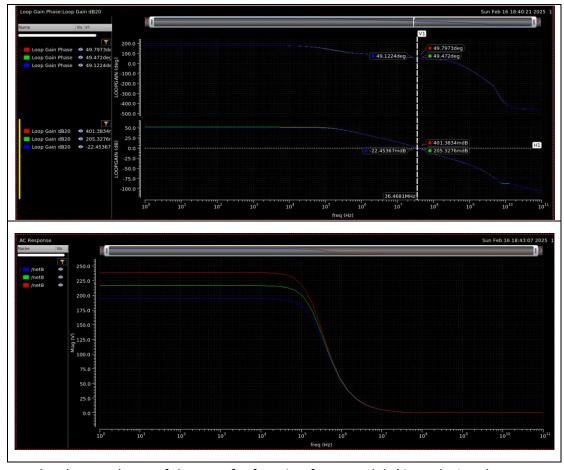
2. Run MC simulation and adjust your design to target a 3-sigma yield for DC Gain, GBW, Phase Margin and input referred noise until all specifications are met. Provide necessary screen shots such that you clearly show the specs are met. (including histogram plots).



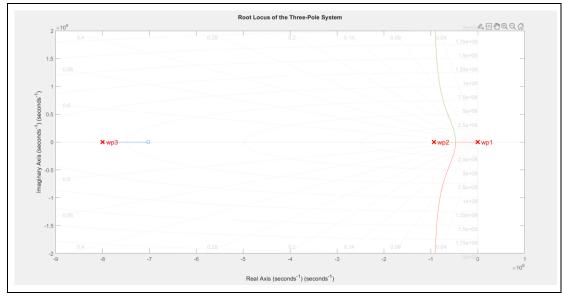


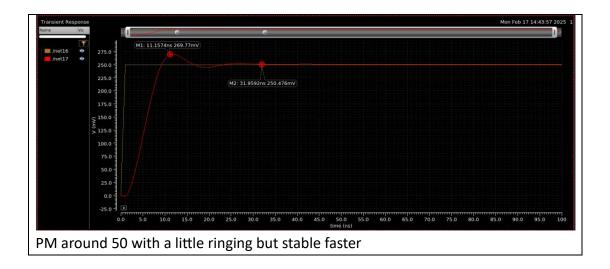
3. Simulate the supply voltage variations (+5, -5%) and temperature (-40, 125C) for DC Gain, GBW, Phase Margin. You do not have to adjust the design if specs are not met.





4. Plot the root-locus of the transfer function from pre-lab (Over design the RHZ, 2*gm8/Cc). Use MATLAB function rlocus. Comment on the result with 250mV step response on unity-gain buffer configuration (beta=1).





Conclusion

Miller compensation is essential for stabilizing OPAs but introduces an undesirable Right-Half Plane (RHP) zero, which degrades phase margin and stability. To counteract this, zero canceling techniques introduce a Left-Half Plane (LHP) zero via a series resistor, effectively mitigating the RHP zero's impact. Proper Miller RC compensation shapes the root locus, optimizing pole placement, loop stability, and transient response. By carefully designing zero placement, designers can enhance bandwidth, phase margin, and gain performance, ensuring a well-behaved amplifier with minimal overshoot and ringing.

Appendix

