25 Spring ECEN 607: Advanced Analog Circuit Tech Design Post-lab Report

Lab1: MOS Device Characterization

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Section:601

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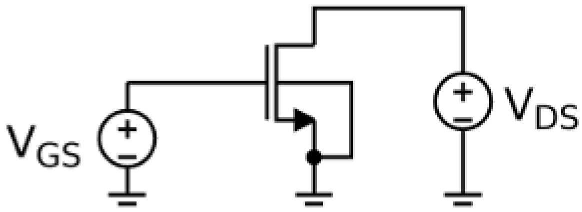
TA: Yoon, Sung J

Description:

In this lab, we learn how to use Cadence Virtuoso to plot and measure some basic characteristics of the different parameters (W/L, finger) of NMOS and PMOS. Generating the waveform plot and examinate the result.

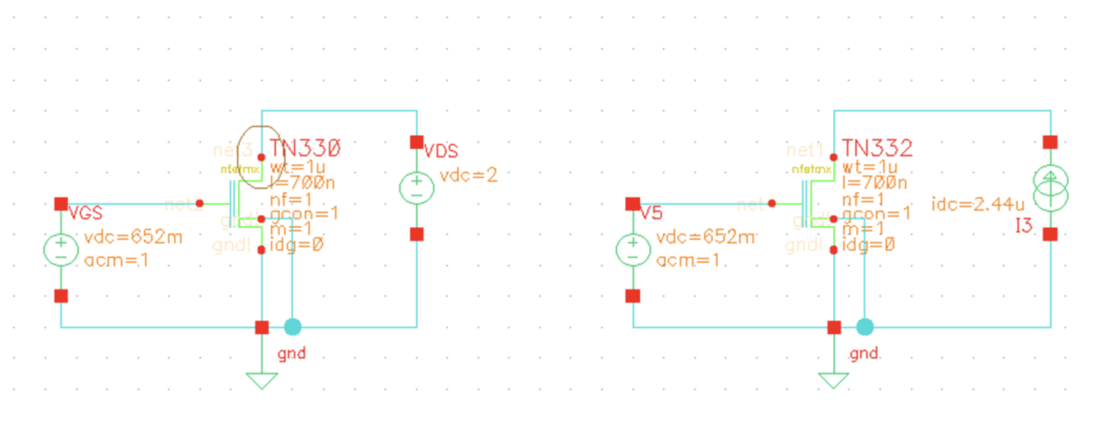
Design & result

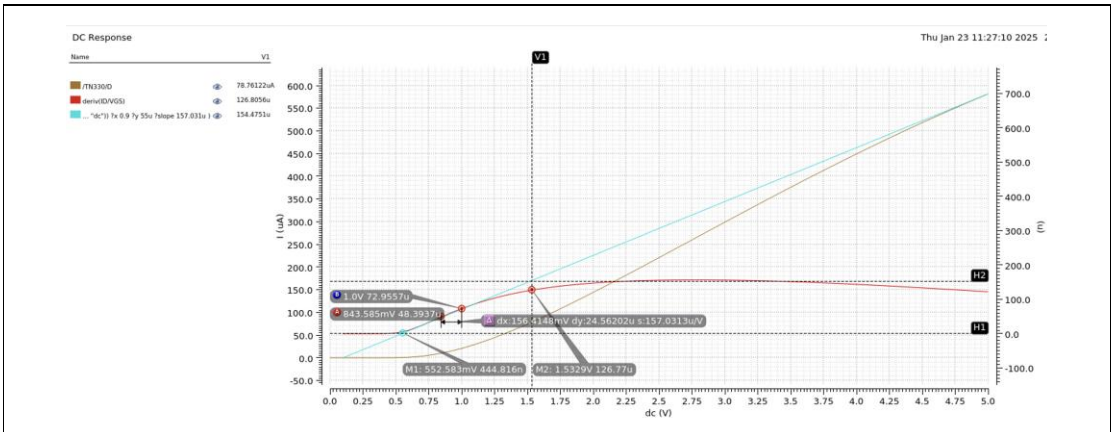


1. nfetmx transistor with W/L=1μ/0.7μ.

a. *Fix VDS=2V. Sweep VGS from 0 to 5V, plot ID and gm (dID/dVGS) vs. VGS, and extract Vtn, μnCox and ϑ.*

schematic

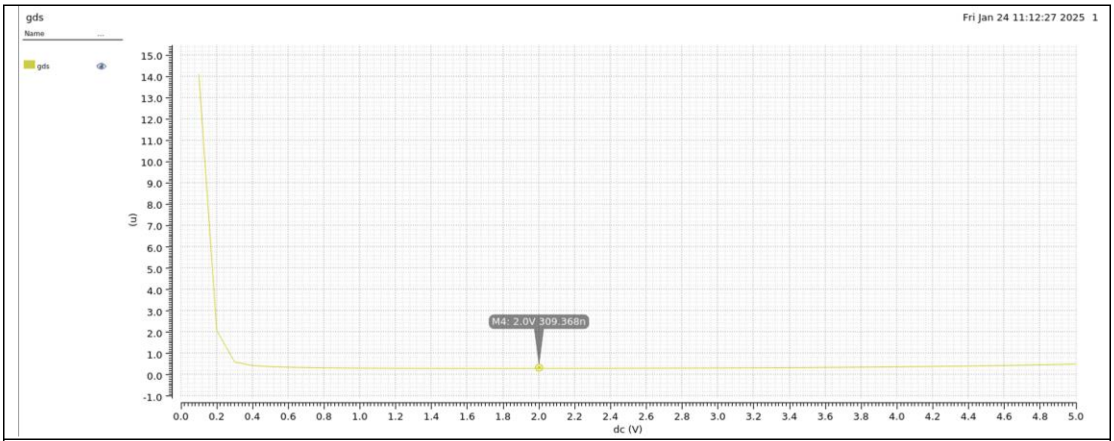




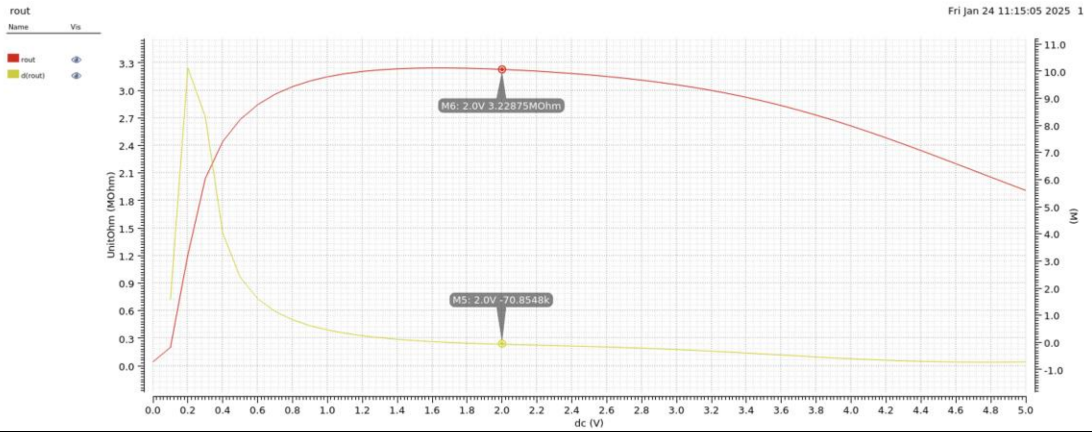
- By finding the intersection point of the red line (dID/dVGS) and the minimum horizon line of the red line v=0, we can find the Vth which is Vth=0.552v
- By finding the slope of the red line, which is blue line, we can get the

μnCox*W/L=157.031u/v, while W/L=1u/0.7u, μnCox=109.96u/V ● By finding the intersection point of the blue line and the maximum horizon line of the red line, we can find the Vth+(1/2θ), and θ will be θ=0.51

b. *Set VGS=Vtn+100mV. Sweep VDS from 0 to 5V, plot and gds (dID/dVDS) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VDS.*

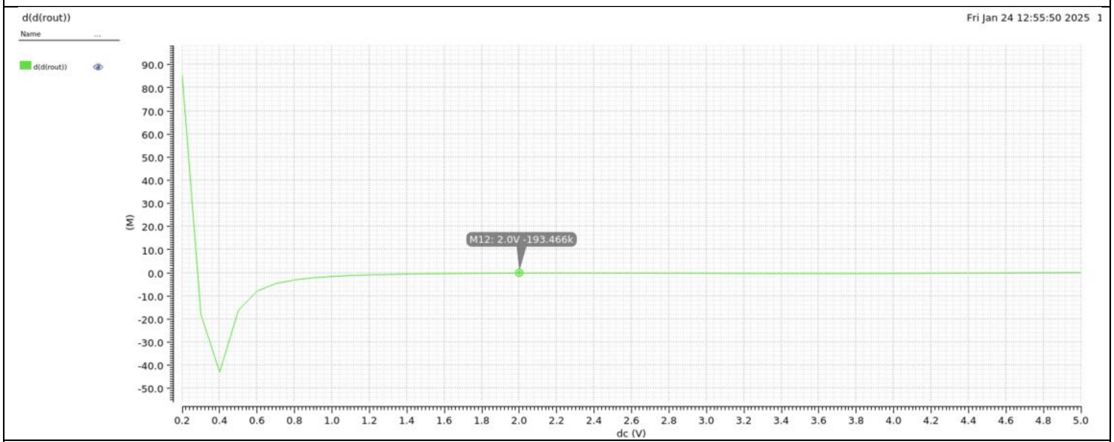


● gds = ∂Ids/∂Vds The output conductance represents the linear relationship between the drain current and the drain-source voltage.



● Red line: output resistance rds.

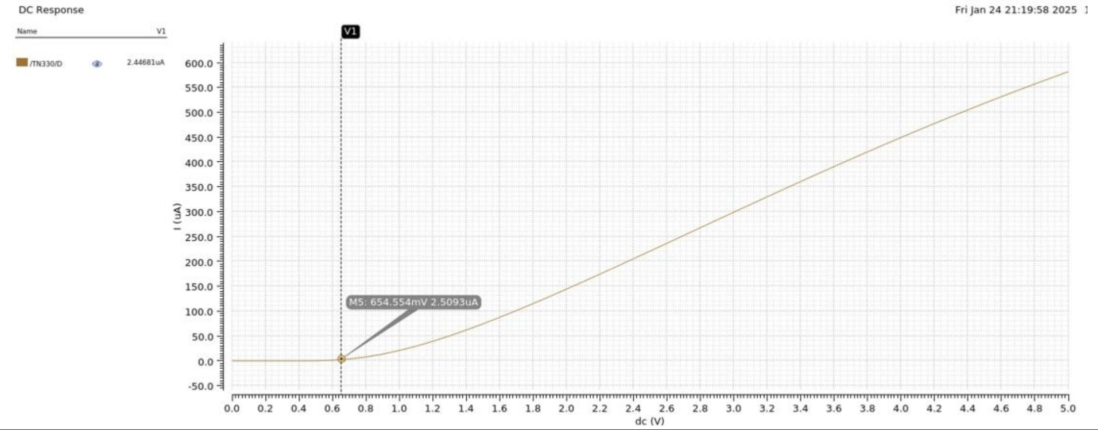
● Yellow line: first derivative function of VDS.



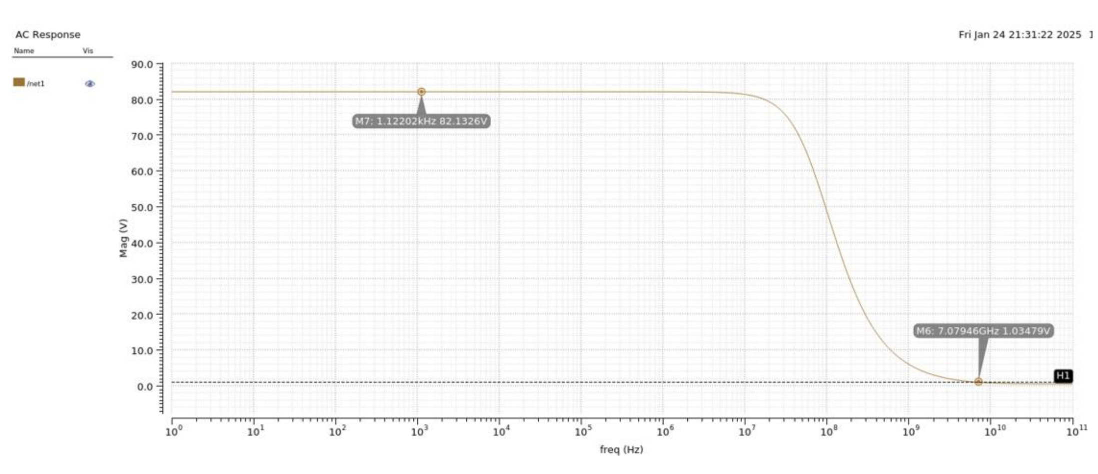
● Green line: second derivative as function of VDS.

c. *Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when*

VDS=2V and VGS=Vtn+100mV.



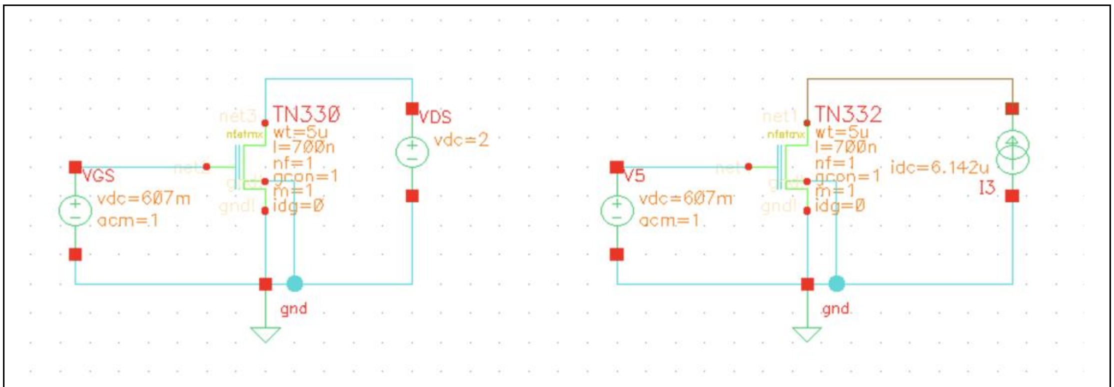
Replace the VDS with the current source IDS when VGS= *Vtn+100mV=0.652, IDS=2.44u*

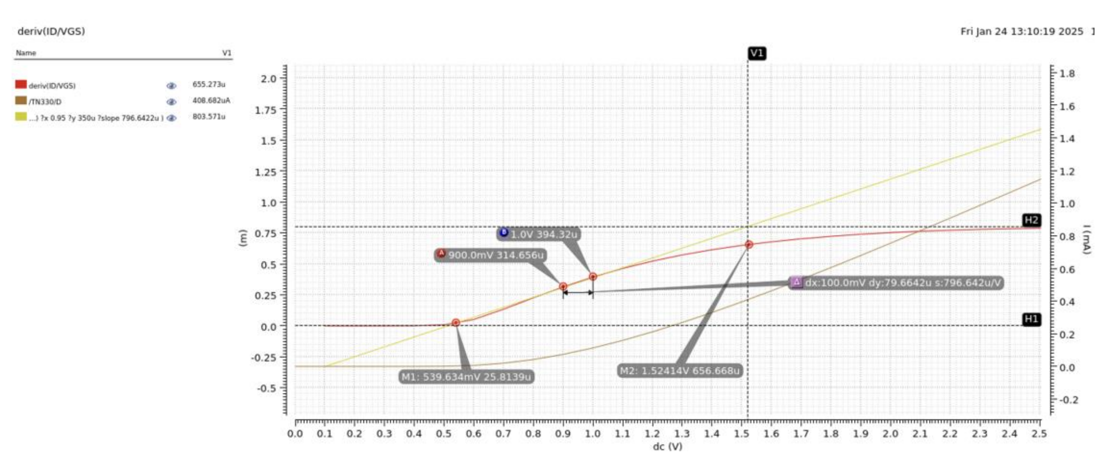


- *intrinsic gain (Ai): when VGS ACM=1, VD= 82.1326*v
- *unity-gain frequency (ft): when gain=1, ft=7.07G*

2. nfetmx transistor with W/L=5μ/0.7μ.

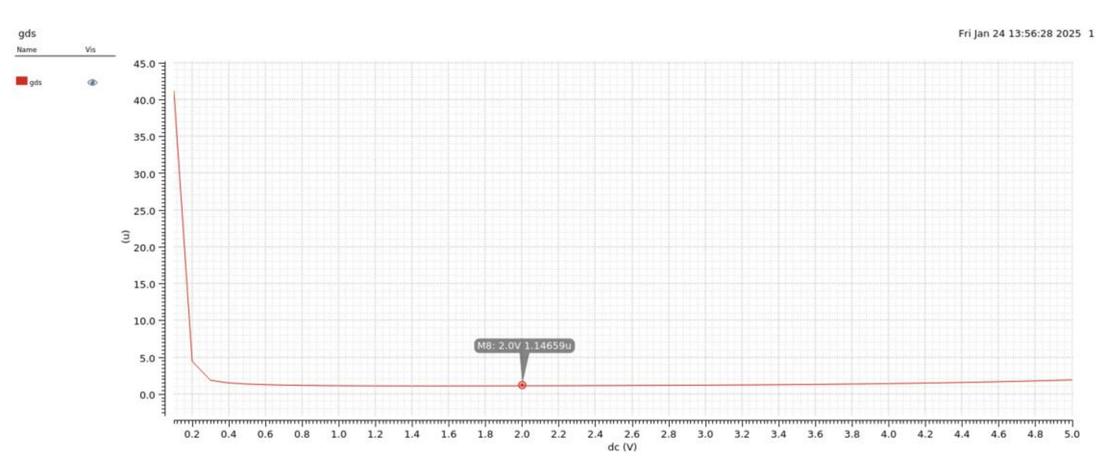
a. Fix VDS=2V. Sweep VGS from 0 to 5V, plot ID and gm (dID/dVGS) vs. VGS, and extract Vtn, μnCox and ϑ.



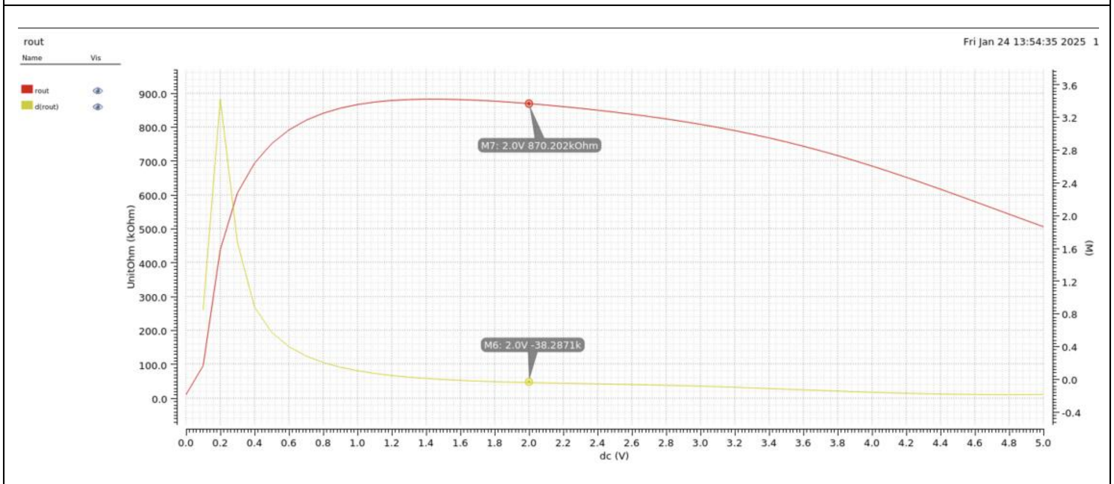


- Vth=0.539v
- µnCox=111.529u/V
- θ=0.507

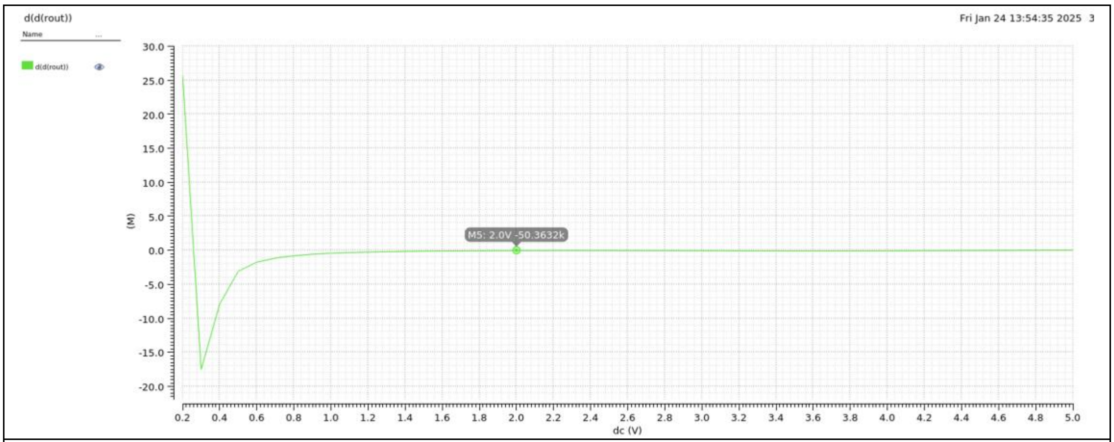
b. Set VGS=Vtn+100mV. Sweep VDS from 0 to 5V, plot and gds (dID/dVDS) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VDS.



- The output conductance gds

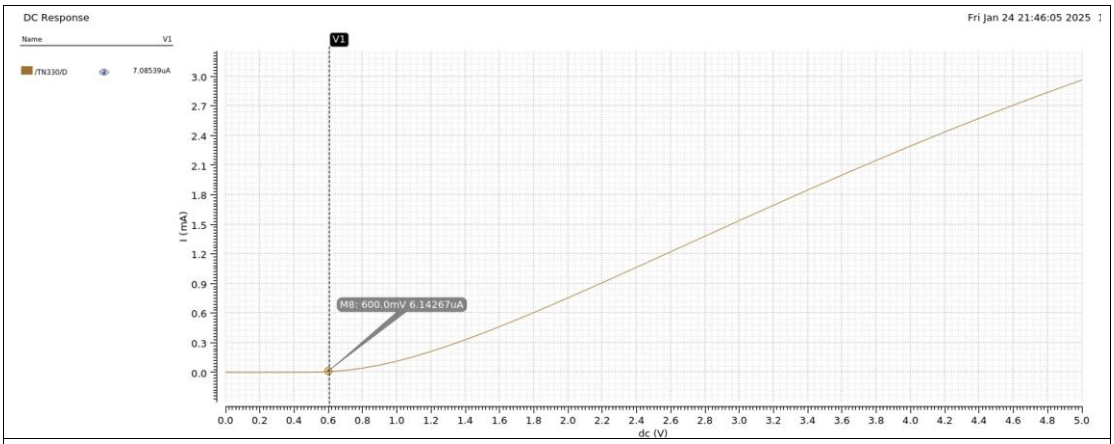


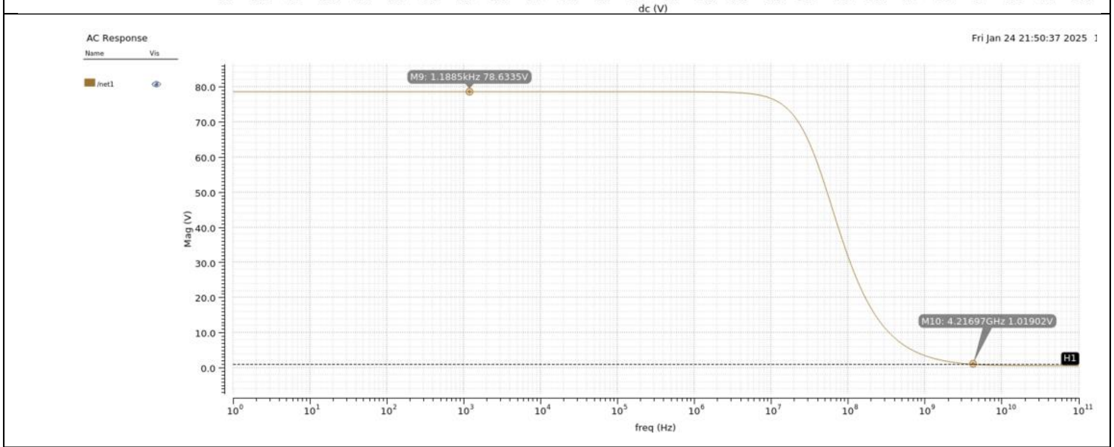
- Red line: output resistance rds.
- Yellow line: first derivative function of VDS.



- Green line: second derivative as function of VDS.

c. Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when VDS=2V and VGS=Vtn+100mV.

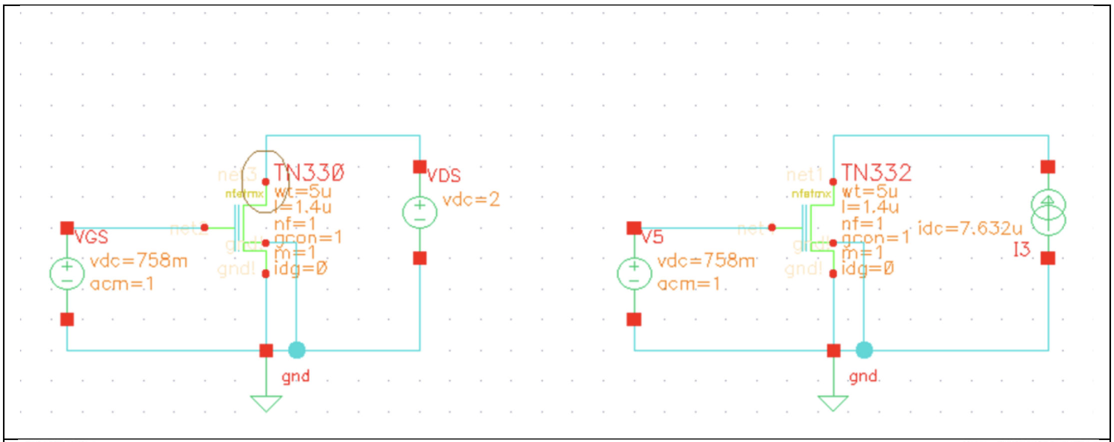


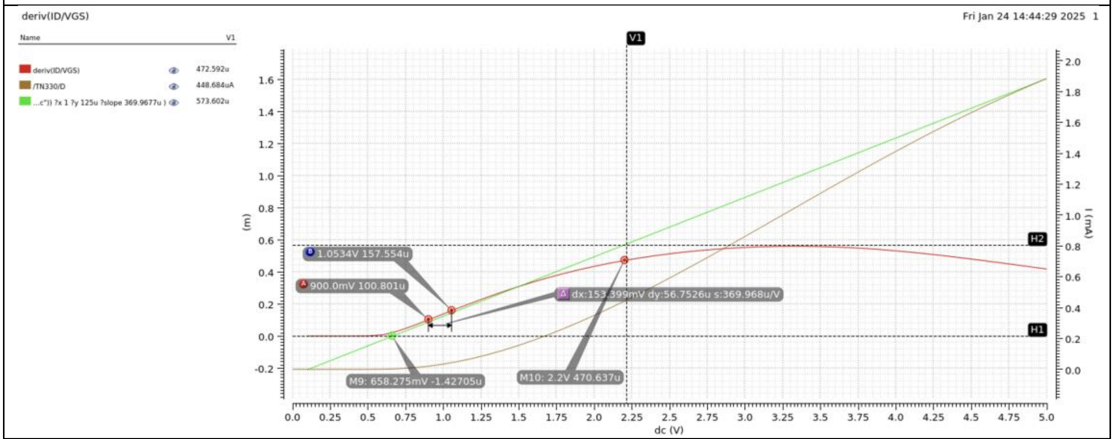


- intrinsic gain (Ai)= 78.633
- ft=4.21GHz

3. nfetmx transistor with W/L=5μ/1.4μ.

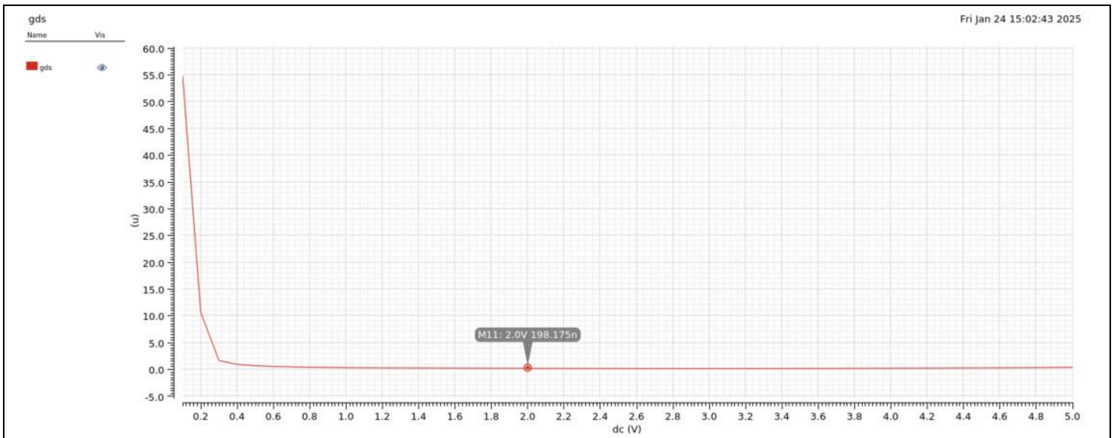
a. Fix VDS=2V. Sweep VGS from 0 to 5V, plot ID and gm (dID/dVGS) vs. VGS, and extract Vtn, μnCox and ϑ.



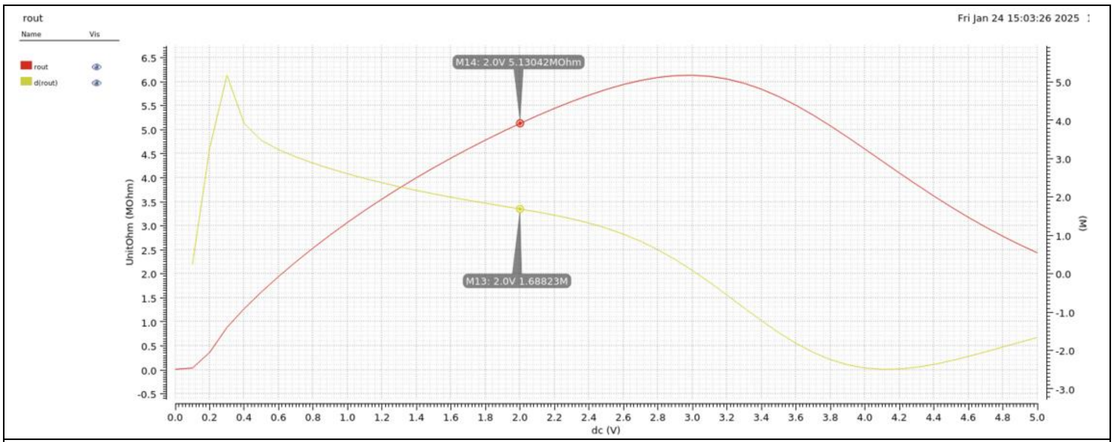


- Vth=0.658v
- µnCox=103.591u/V
- θ=0.324

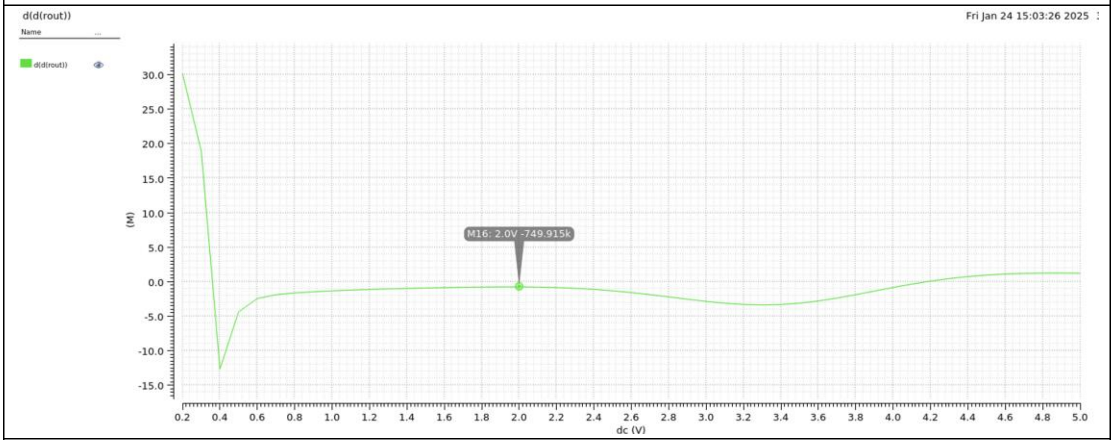
b. Set VGS=Vtn+100mV. Sweep VDS from 0 to 5V, plot and gds (dID/dVDS) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VDS.



- The output conductance gds

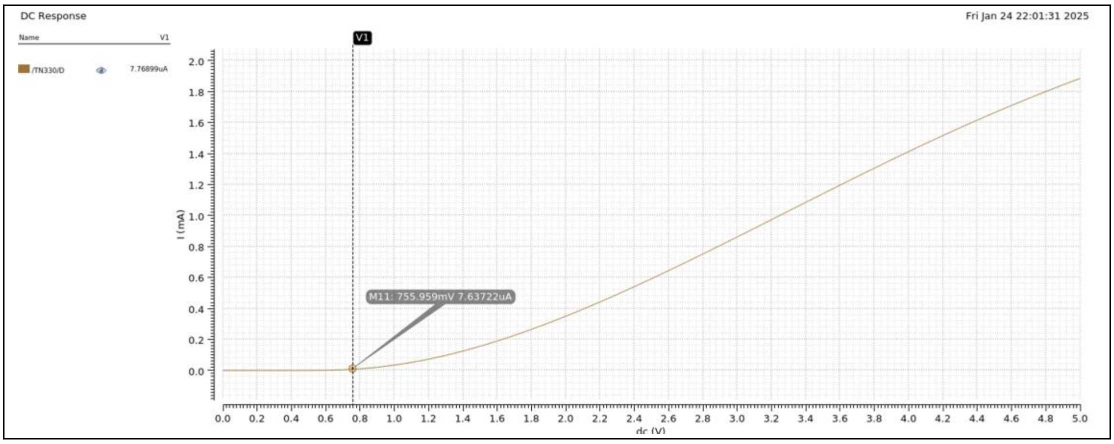


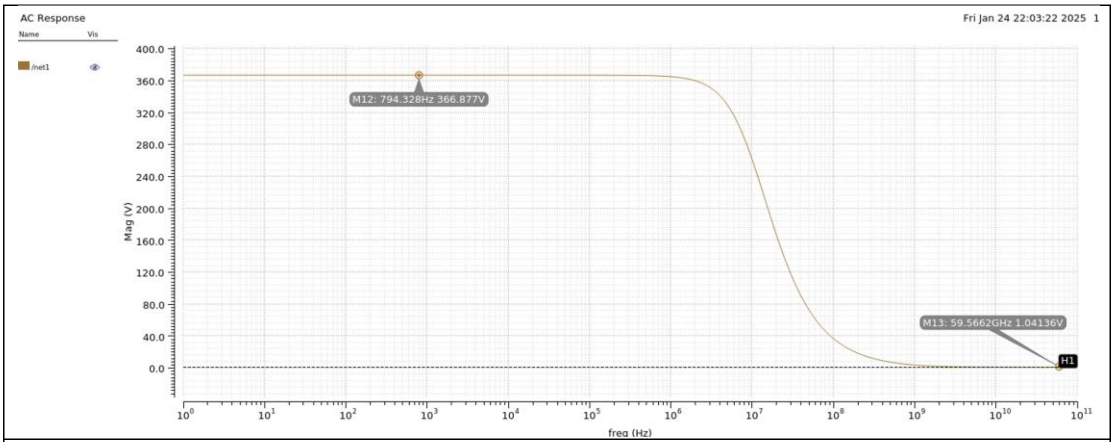
- Red line: output resistance rds.
- Yellow line: first derivative function of VDS.



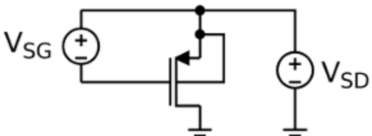
- Green line: second derivative as function of VDS.

c. *Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when VDS=2V and VGS=Vtn+100mV.*





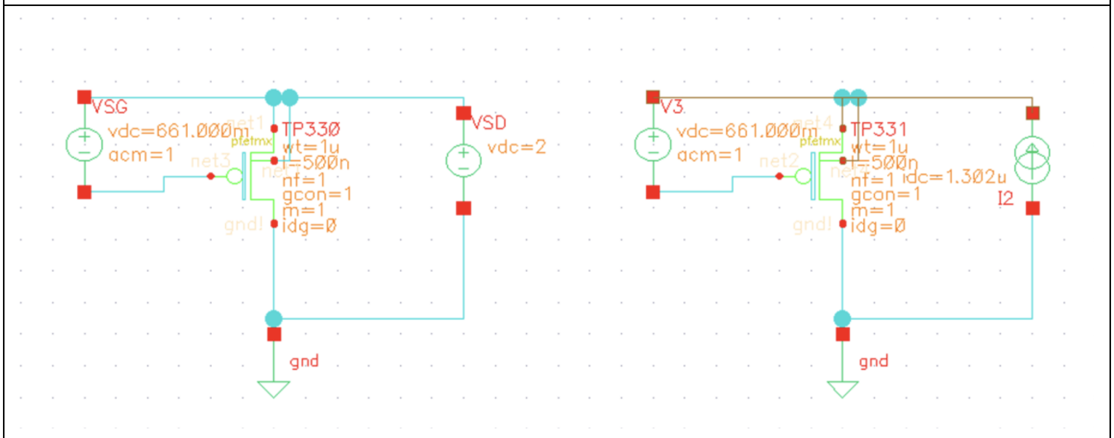
- intrinsic gain (Ai)= 366.877
- ft=59.566GHz

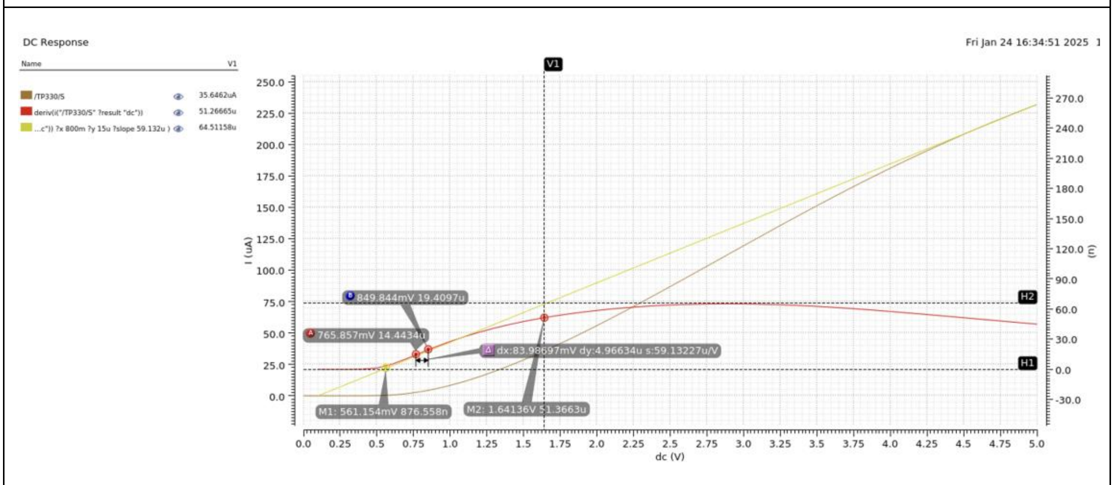


4. pfetmx transistor with W/L=1μ/0.5μ.

a. VSD=2V. Sweep VSG from 0 to 5V, plot ID and gm=dID/dVSG vs. VSG, and extract Vtp, μpCox and ϑ.

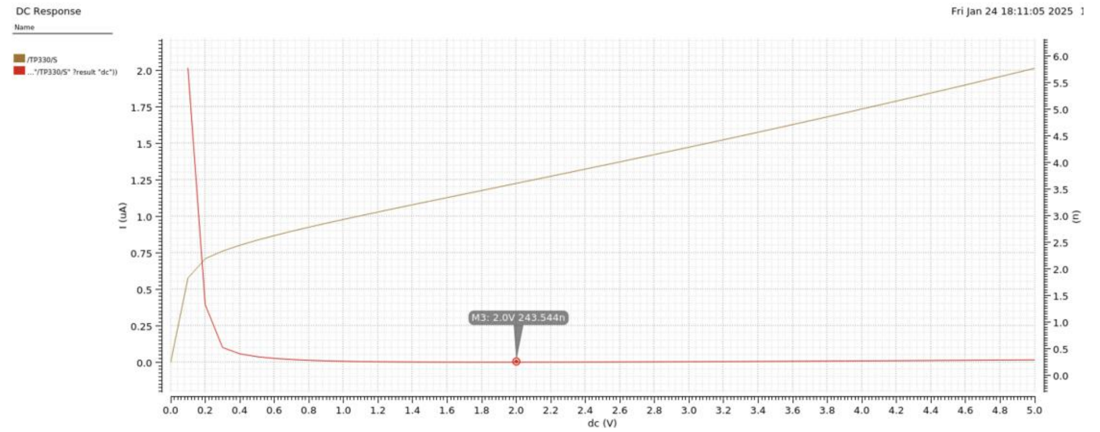
schematic



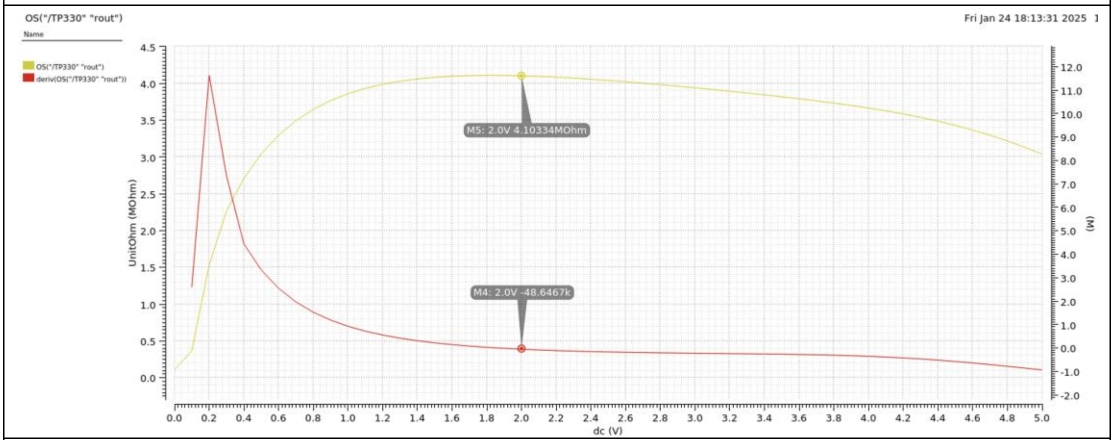


- Vth=0.561v
- μnCox=29.566u/V
- θ=0.462

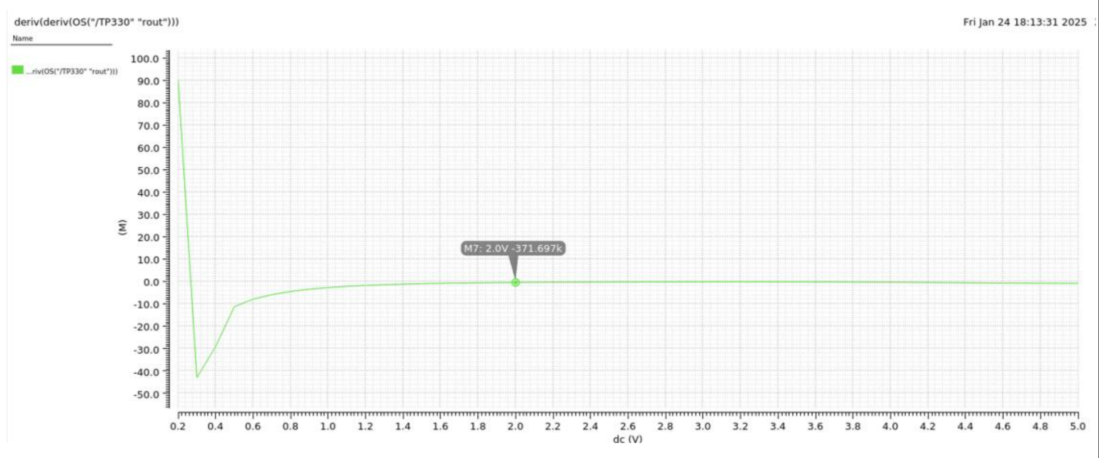
b. VSG=|Vtp|+100mV. Sweep VSD from 0 to 5V, plot and gds (dID/dVSD) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VSD.



- gds = ∂Ids/∂Vds The output conductance.



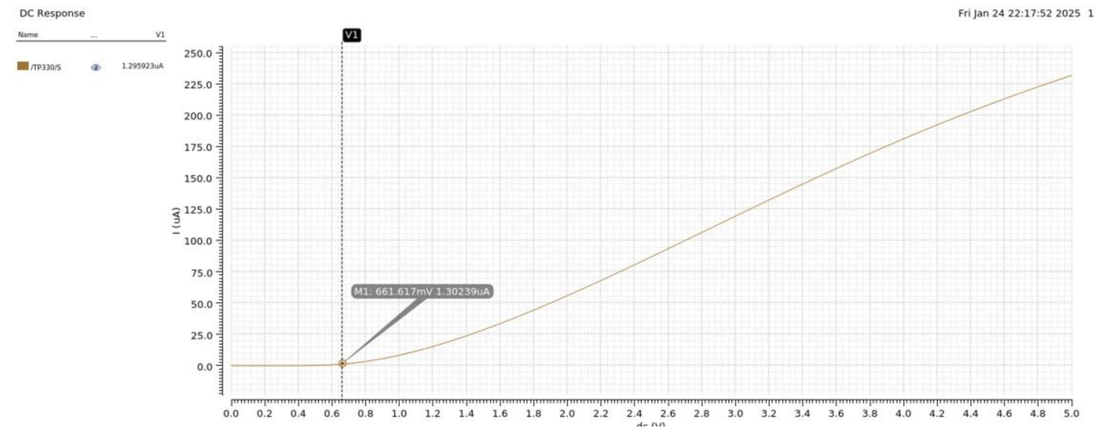
- Yellow line: output resistance rds.
- Red line: first derivative function of VDS.

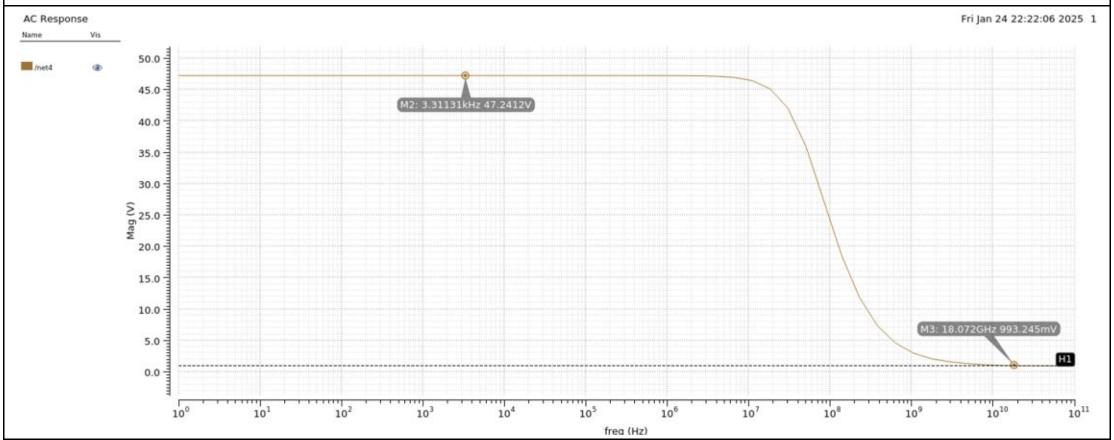


- Green line: second derivative as function of VDS.

c. Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when

VSD=2V and VSG=|Vtp|+100mV.



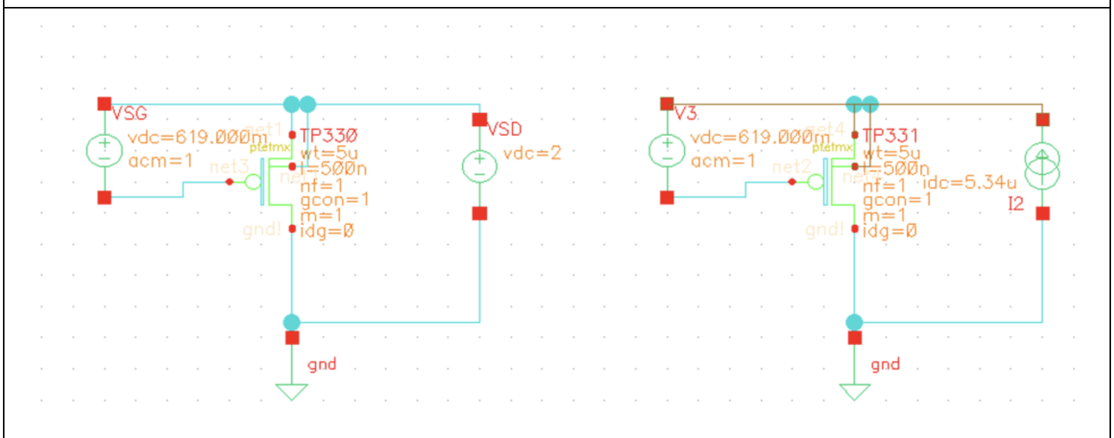


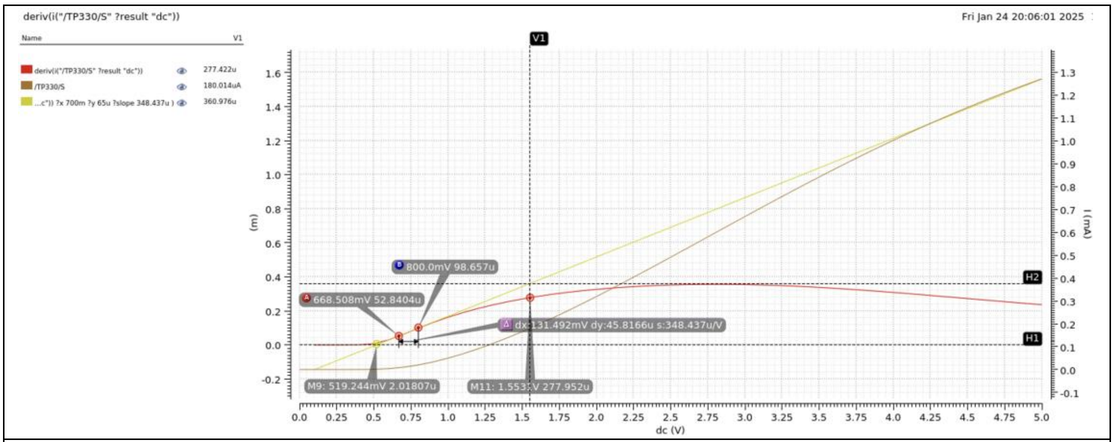
- intrinsic gain (Ai)= 47.24
- ft=18.07GHz

5. pfetmx transistor with W/L=5μ/0.5μ.

a. *VSD=2V. Sweep VSG from 0 to 5V, plot ID and gm=dID/dVSG vs. VSG, and extract Vtp, μpCox and ϑ.*

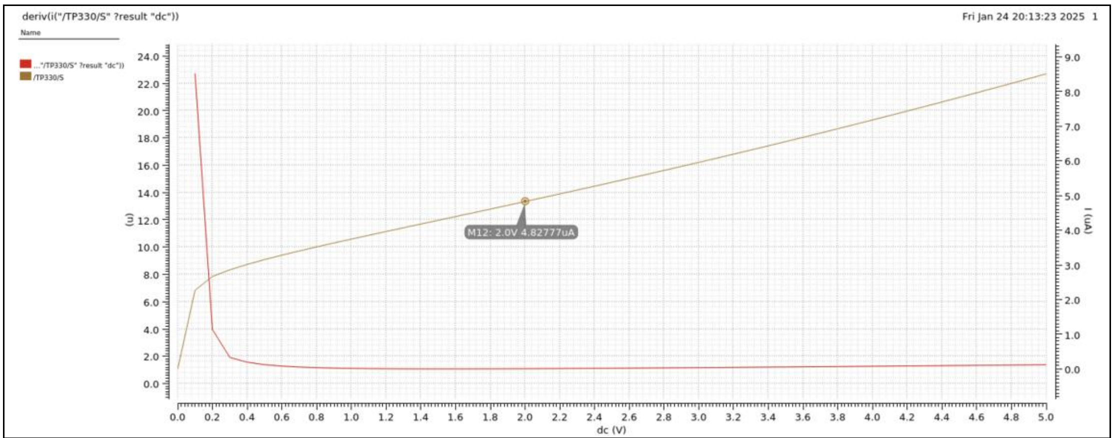
schematic



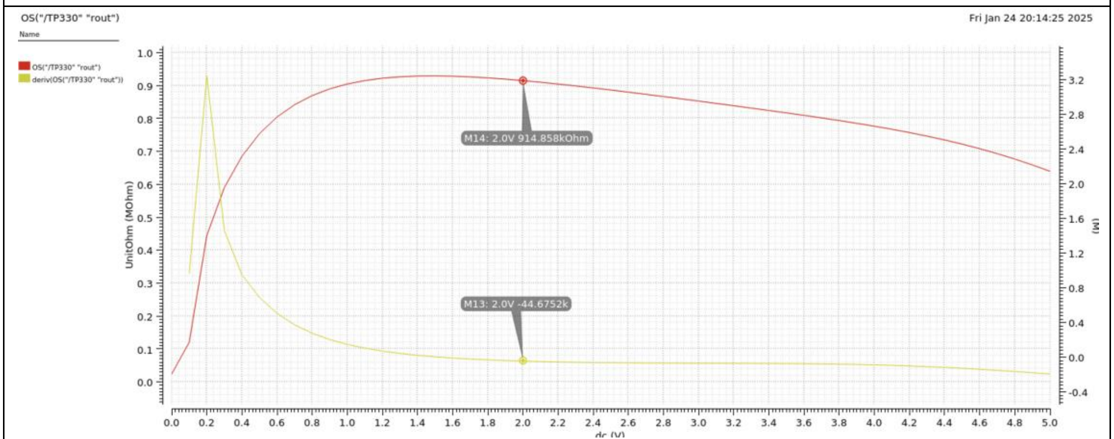


- Vth=0.519v
- µnCox=34.83u/V
- θ=0.483

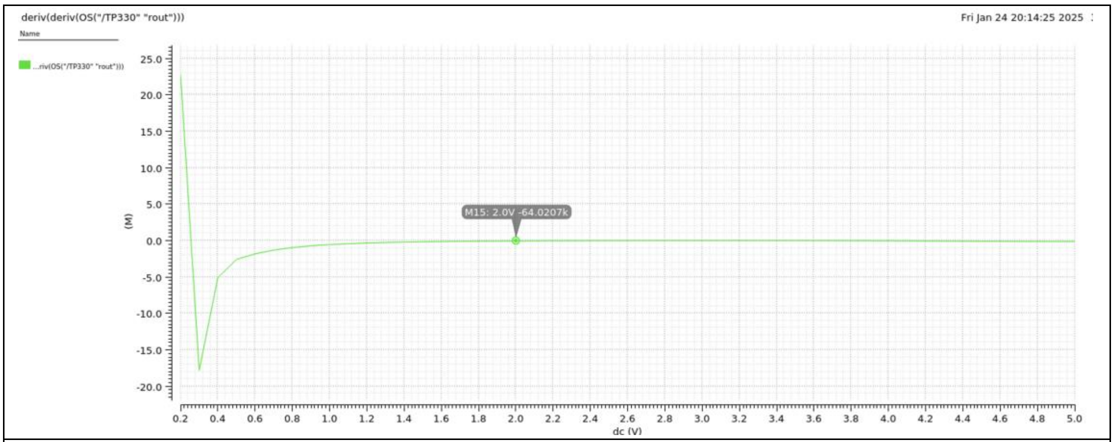
b. VSG=|Vtp|+100mV. Sweep VSD from 0 to 5V, plot and gds (dID/dVSD) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VSD.



- gds = ∂Ids/∂Vds The output conductance.

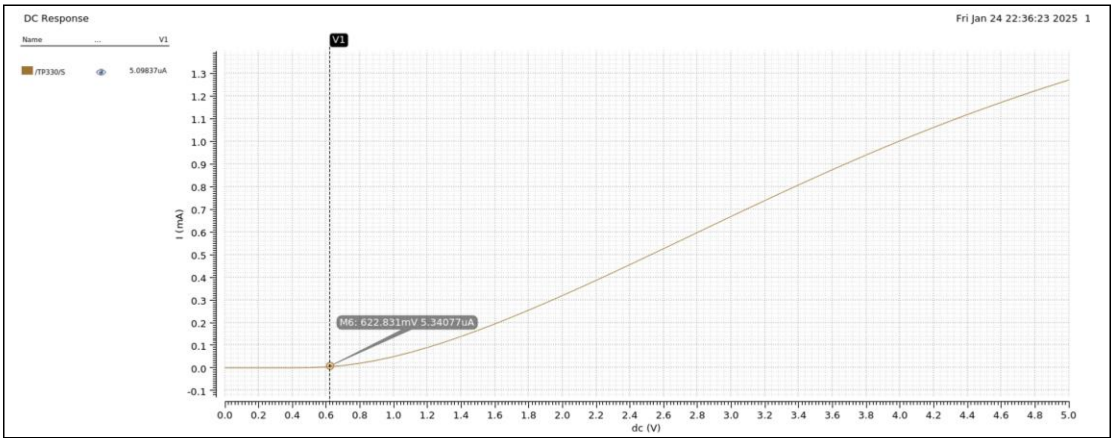


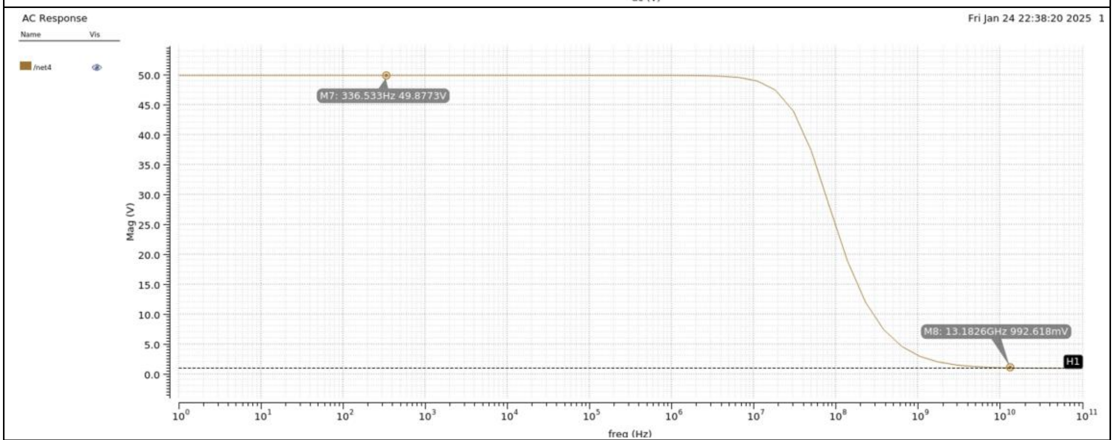
- Red line: output resistance rds.
- Yellow line: first derivative function of VDS.



- Green line: second derivative as function of VDS.

C. Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when VSD=2V and VSG=|Vtp|+100mV.



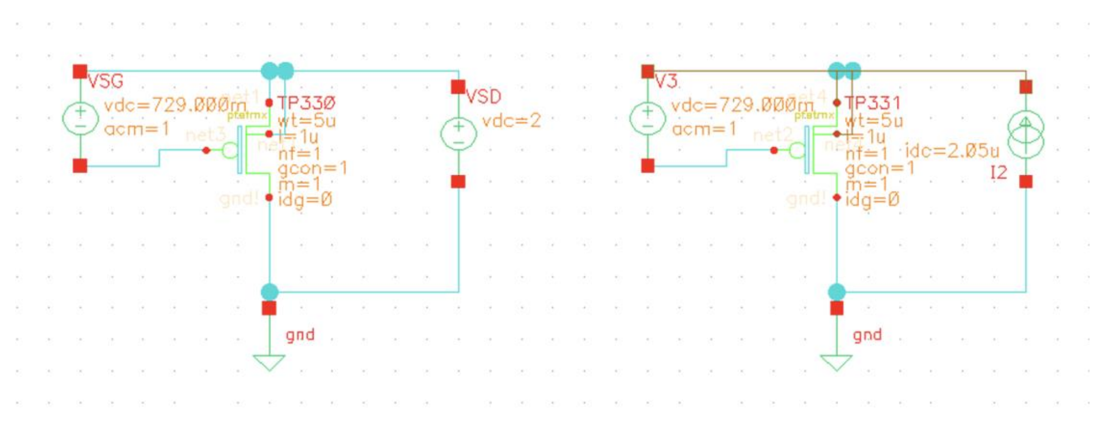


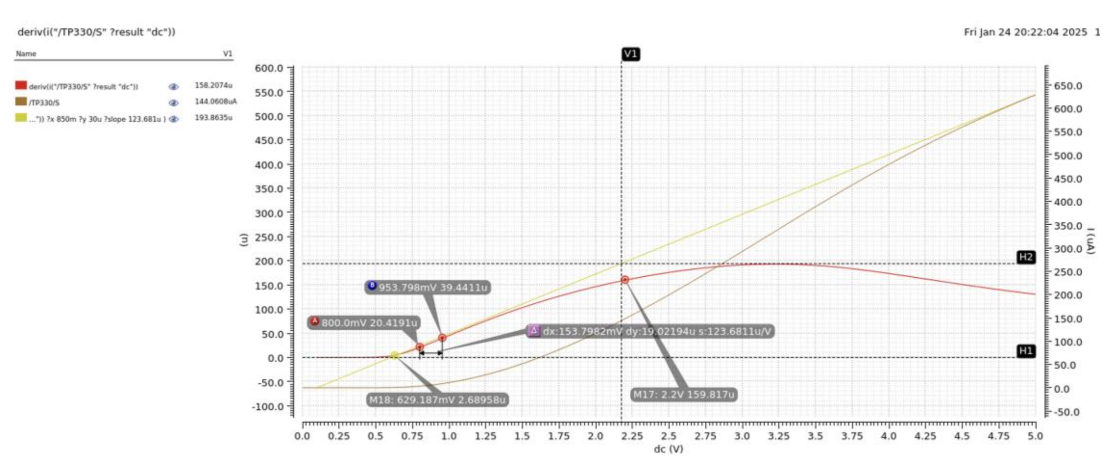
- intrinsic gain (Ai)= 49.877
- ft=13.182GHz

6. pfetmx transistor with W/L=5μ/1μ.

a. VSD=2V. Sweep VSG from 0 to 5V, plot ID and gm=dID/dVSG vs. VSG, and extract Vtp, μpCox and ϑ.

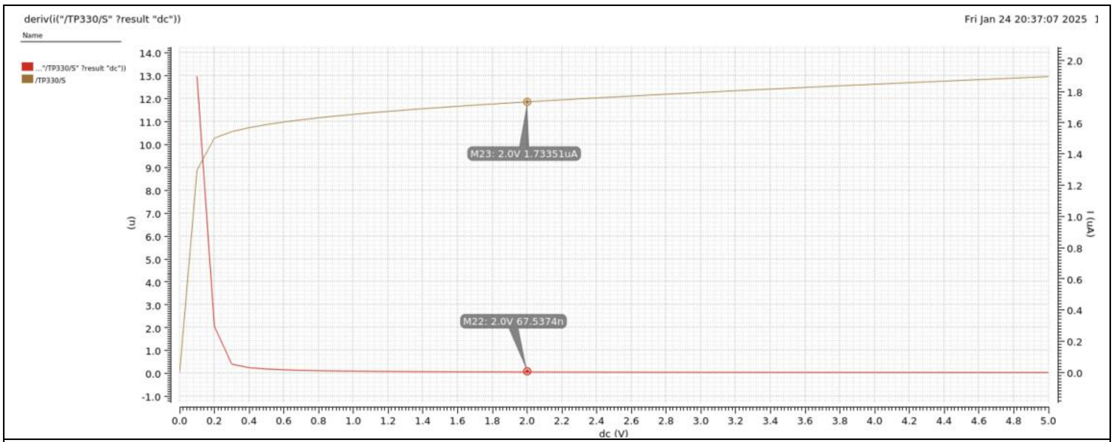
schematic



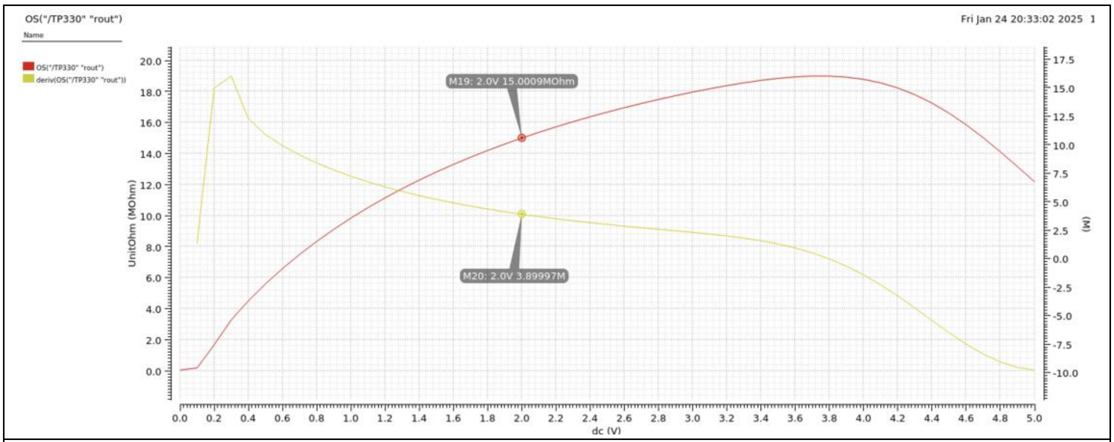


- $Vth=0.629v$
- $\mu nCox=24.736u/V$
- $\theta=0.318$

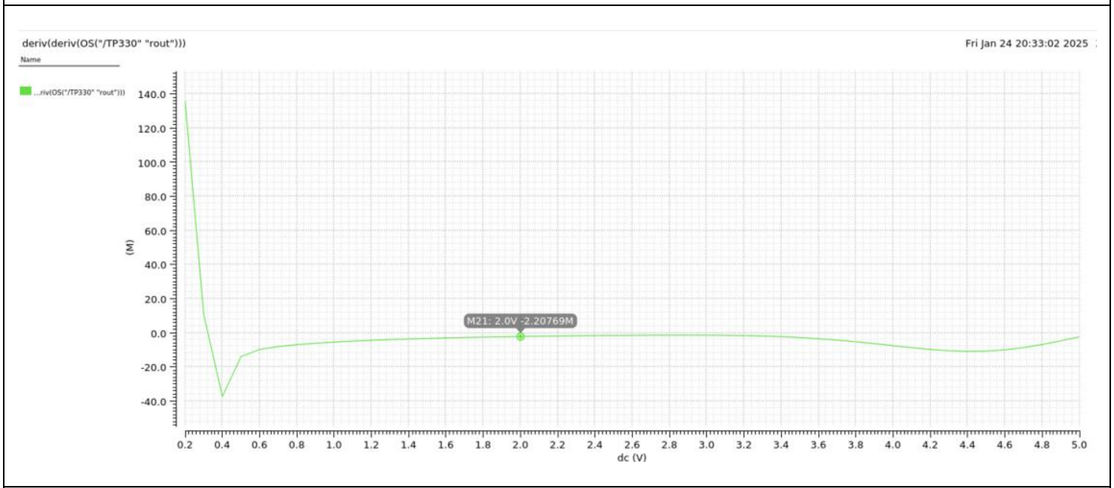
b. VSG=|Vtp|+100mV. Sweep VSD from 0 to 5V, plot and gds (dID/dVSD) vs. VDS. Plot the output resistance rds, and its first and second derivative as function of VSD.



- gds = ∂Ids/∂Vds The output conductance.

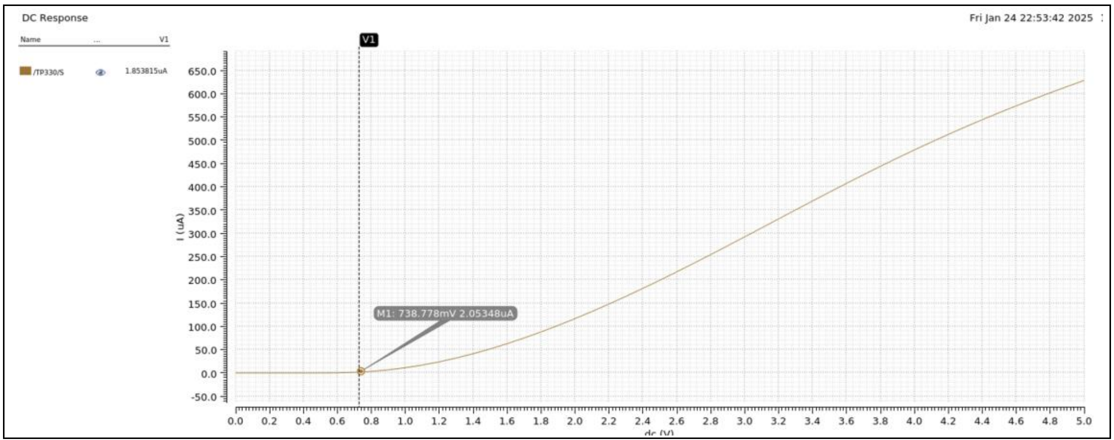


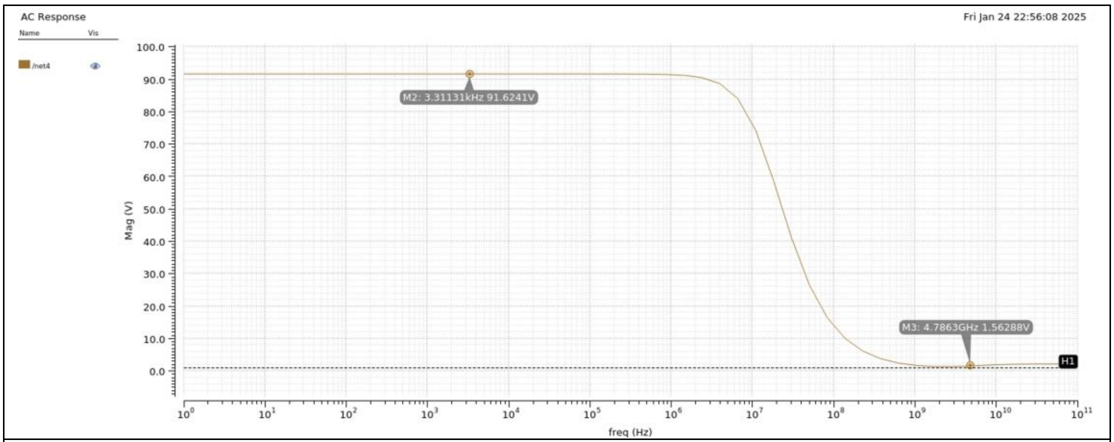
- Red line: output resistance rds.
- Yellow line: first derivative function of VDS.



- Green line: second derivative as function of VDS.

c. *Find the intrinsic gain (Ai) and unity-gain frequency (ft) using AC simulations when VSD=2V and VSG=|Vtp|+100mV.*





- intrinsic gain (Ai)= 91.62
- ft=4.786GHz

Discussion:

When the W/L ratio changes (especially when W increases), the changes in ft (cutoff frequency) and intrinsic gain are primarily due to variations in key electrical parameters.

When W increases: gm=μnCox*W/L*(Vgs−Vt), W directly increases gm, also ft=gm /2πCgs, W increases will increase the ft. W directly increases gm, as it widens the effective channel for carriers to move. Cgs is linearly proportional to W, as Cgs=ϵox*(W*L)/tox, where ϵox is the oxide permittivity gate and tox is the oxide thickness. As W increases, the capacitance grows, partially offsetting the improvement in gm.

Intrinsic gain=gm/gds=gm*rds (when vi=1), when W increases, the gm increases. When W/L= increases, the increase in ID is usually smaller compared to the increase in gm, leading to a reduction in rds.

Conclusion:

In this lab, we learn how to operate Virtuoso under Cadence to find the basic characteristics of the different parameters of NMOS and PMOS. Just like what the professor mentioned in class, understanding how to identify the basic characteristics of MOS transistors is essential for an engineer.

The difference between the fetmx and fetx, which we use in ECEN 704 VLSI, is the design specifications, electrical characteristics, manufacturing processes, and application scenarios. The "M" might stand for **Metal Gate** or **Model Extension**, indicating that the component is a special specification of an NMOS transistor. It is often used for circuits requiring higher performance, possibly having larger dimensions, higher drive capabilities, or specific metal-gate structures.