ECEN 607: Advanced Analog Circuit Tech

Lab 2: Two-Stage Amplifier Design with 3σ Driven Statistical Corner Extraction

Pre-lab or Lab Report

Name: FirstName LastName
UIN: ******Last Three Digits

Objectives:

1. Design and simulate a two-stage Miller-compensated amplifier.
2. Observe the effect of voltage and temperature variations.
3. Verify the design with Monte-Carlo simulation.

Prelab:

1. A PMOS input, two-stage Miller compensated op-amp is shown below. Obtain the expressions for
   - From your background in ECEN-704/474, obtain the DC Gain (A_{v0}), frequency of the dominant pole (p1), Second pole (p2), Zero (z), Gain bandwidth product (GBW). Find the expression for Phase Margin (PM).

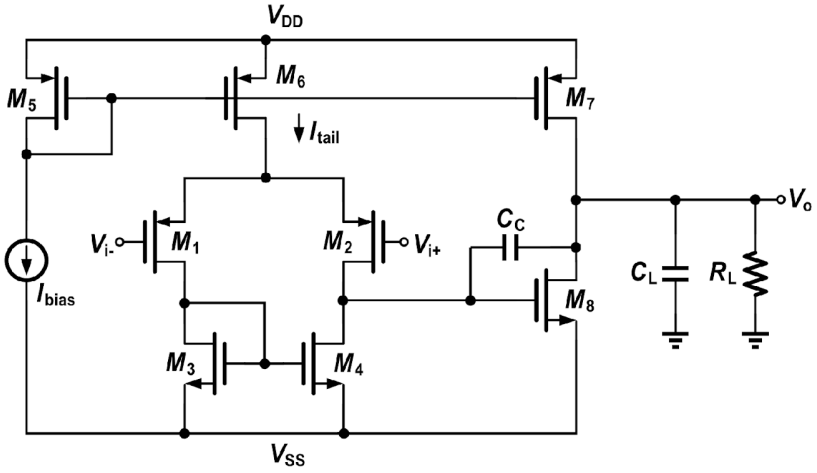


Figure 1: PMOS Two-Stage Miller Opamp

2. Select the current in different branches as well as dimensions of the transistors to satisfy the following specifications:

Table 1: Design specifications. Notice that VDD, VSS, CL and RL are given

V_{DD}	0.9V
V_{SS}	-0.9V
A_{v0}	> 40 dB
GBW	> 2 MHz
PM	> 45°
Output Swing	> 1 V
C_L	30 pF
R_L	10kΩ

The following tables are provided by the vendor of this technology. Take advantage of this information. Notice that relevant parameters are dimension dependent; e.g. threshold voltage is not constant, its value increases with L.

Table 2: Reference parameters of 1.8 V NMOS transistors..

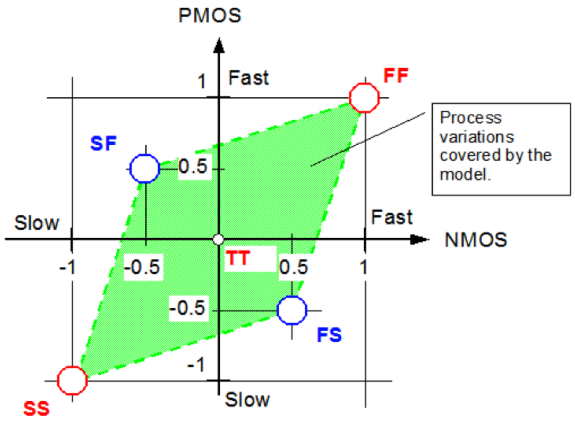
Sl. No	W/L (µm/ µm)	V_{th} (mV)	µn*Cox (mF/Vs)	θ	λ (mV^{-1})	Ai		f_t (GHz)
						(V)	(dB)	
1	0.5/0.18	0.46	0.167	0.92	263	21.17	26.51	51.23
2	5/0.18	0.458	0.215	1.28	329.406	21.65	26.71	49.12
3	5/0.27	0.447	0.214	0.994	131.158	45.212	33.11	26.82

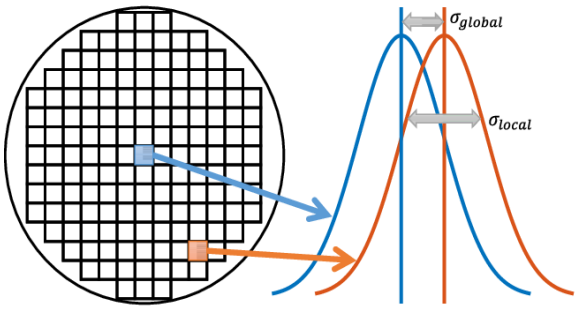
Table 3: Reference parameters of 1.8 V PMOS transistors

Sl. No	W/L (µm/ µm)	V_{tp} (mV)	µn*Cox (µF/Vs)	θ	λ (mV^{-1})	Ai		f_t (GHz)
						(V)	(dB)	
1	0.5/0.18	0.43	47.2	0.744	289.27	17.39	24.81	17.41
2	5/0.18	0.413	56.22	0.77	292.15	17.63	24.93	19.64
3	5/0.27	0.42	47.37	0.653	158.16	28.085	28.97	8.851

Lab:

Corner models have been a mainstay of integrated circuit design for decades. However, there are significant inaccuracies that arise when digital CMOS corner models are used for analog circuits, or any types of circuits or measures of circuit performance they were not targeted for. The standard FF, SS SF, FS corners represent statistical bounds of global process variation for the device-level performances of speed and power. These models are appropriate when the device-level performances of speed and power directly relate to all circuit-level performances, such as digital standard cell performances of speed and power. When these conditions are not met (i.e. when device speed/power don't directly relate to circuit output measures of interest such as DC gain, GBW etc.), then a statistical simulation is appropriate.





This part of the lab is concerned with designing circuits when global or local process variations need to be verified with statistical simulation, Monte-Carlo.

Lab Report: Provide necessary plots, explanations etc. in the report for the following questions.

1. Simulate the design from the prelab and adjust the transistor sizes accordingly until all specifications are met. Notice that most relevant transistors are M1=M2 and M8. Check the slides discussed lecture 01/30/2024.
2. Plot and report (from simulations) the input referred noise density (what this does mean?) and find RMS voltage noise integrated in the band (10 Hz – 2 MHz).
3. In addition, provide comparison tables of hand-calculated vs. final transistor sizes, and required specs (Table 1-1) vs. simulated specs. Comment on your results.
4. Plot the magnitude and phase response of your amplifier. Measure the phase margin and unity gain frequency from simulations.
5. Simulate statistical simulation, Monte-Carlo, for GBW, Phase Margin and DC gain at least 200 points. Plot the histograms.
6. Close the loop to implement a unity gain buffer (b factor =1) and measure the step response for an input step of 20mV. Report the results.
7. Close the loop with two resistors of 100kΩ and/or larger to implement a 6dB gain inverting amplifier. Report the 250mV step response. Any ringing? Explain your results.

References:

1. https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6658428
2. Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide, Springer 2012
3. https://community.cadence.com/cadence_blogs_8/b/cic/posts/fast-yield-analysis-and-statistical-corners