

25 Spring ECEN 607: Advanced Analog Circuit Tech  
Design Post-lab Report

Lab2: Two-Stage Amplifier Design with  $3\sigma$  Driven  
Statistical Corner Extraction

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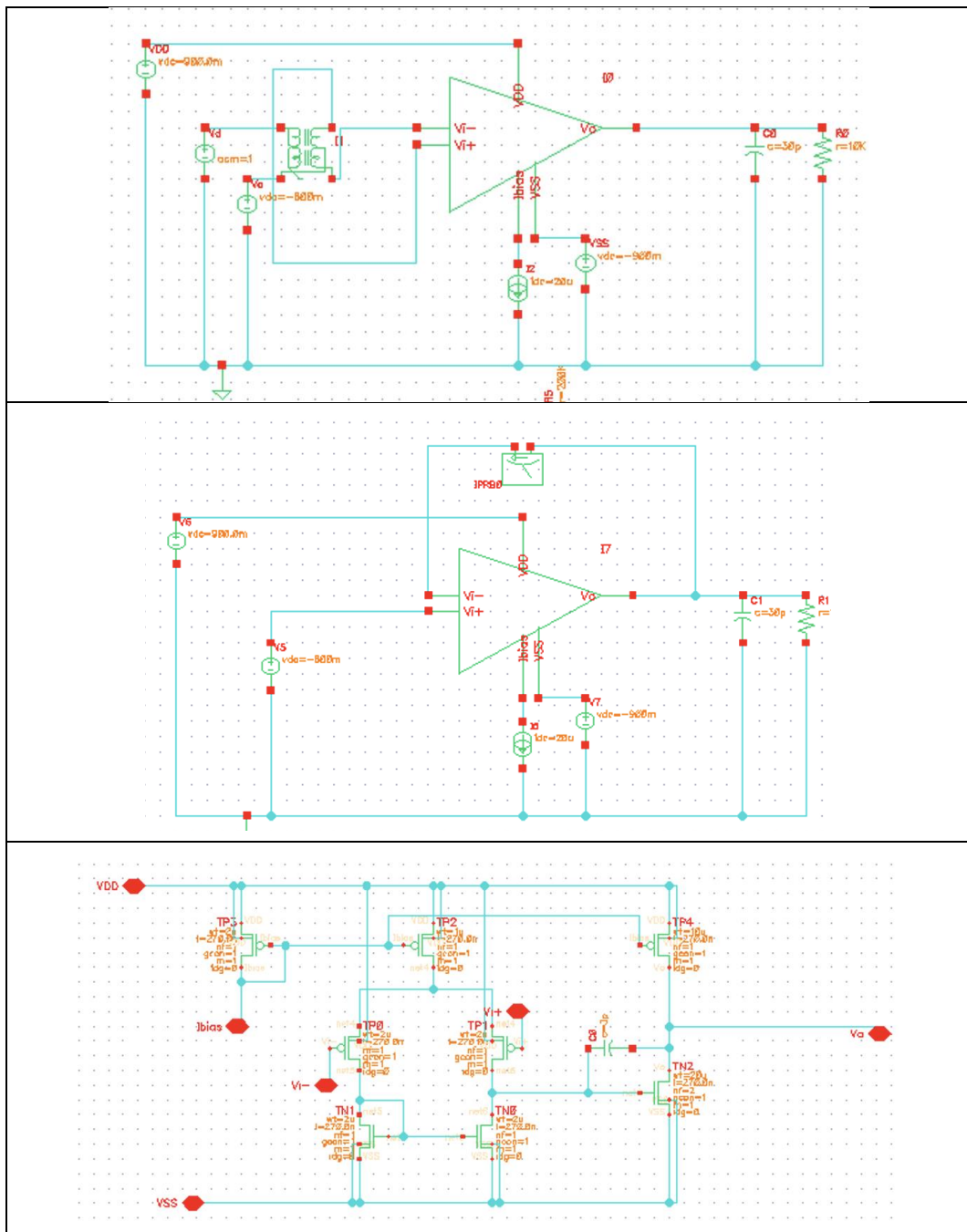
TA: Yoon, Sung J

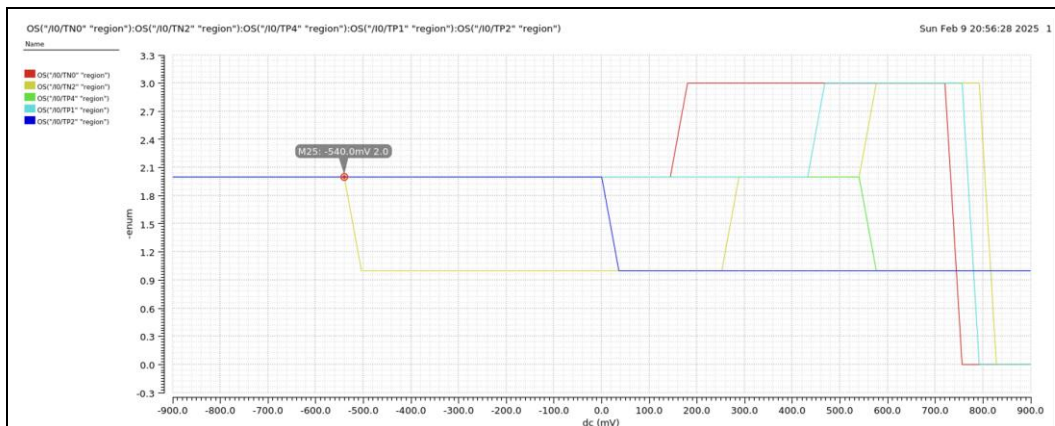
## Objectives:

1. Design and simulate a two-stage Miller-compensated amplifier.
2. Observe the effect of voltage and temperature variations.
3. Verify the design with Monte-Carlo simulation.

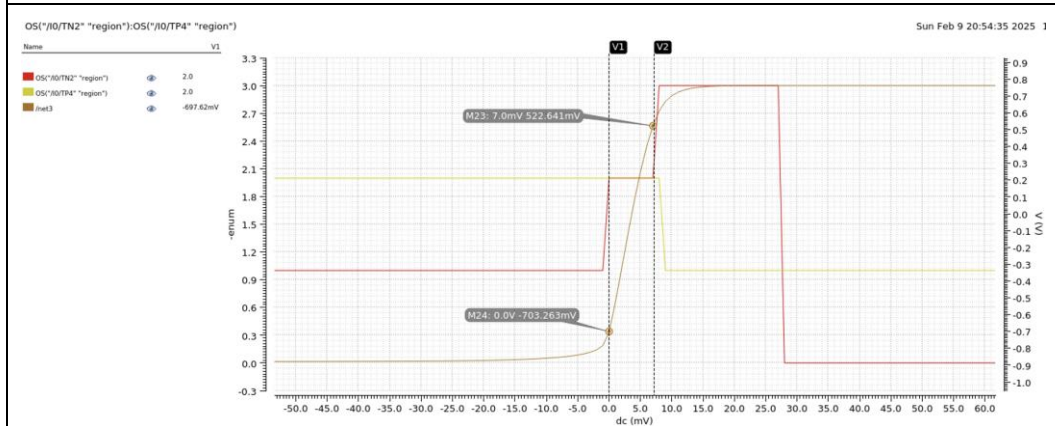
## Design & results:

1. Simulate the design from the prelab and adjust the transistor sizes accordingly until all specifications are met. Notice that most relevant transistors are M1=M2 and M8. Check the slides discussed lecture 01/30/2024.

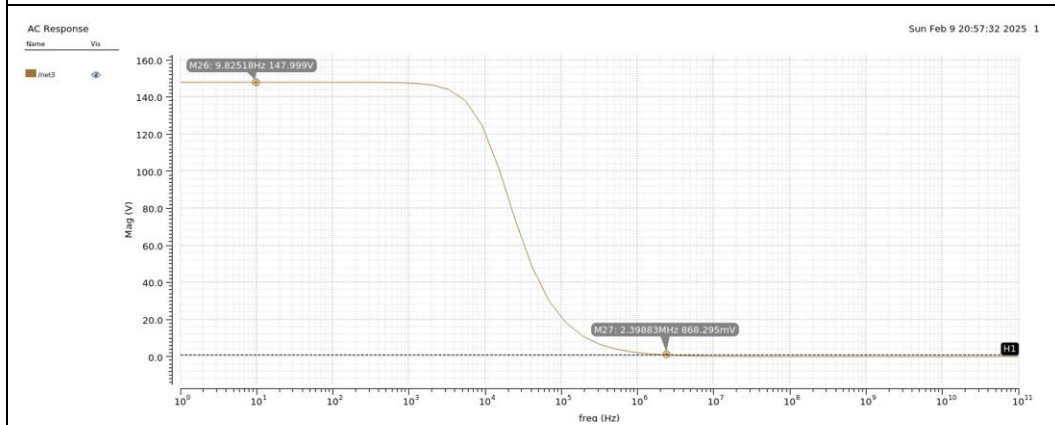




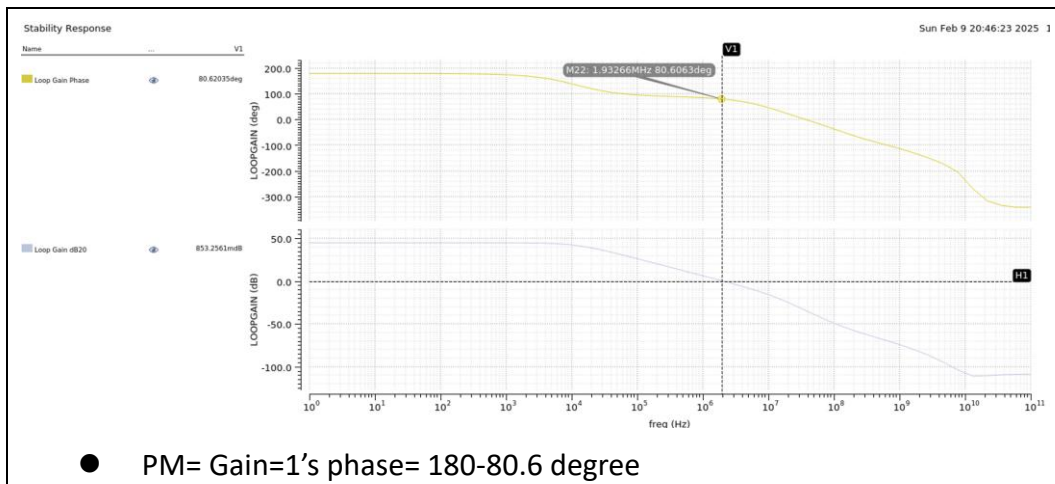
- Vcm range the dc operation point (-0.9~-0.54)



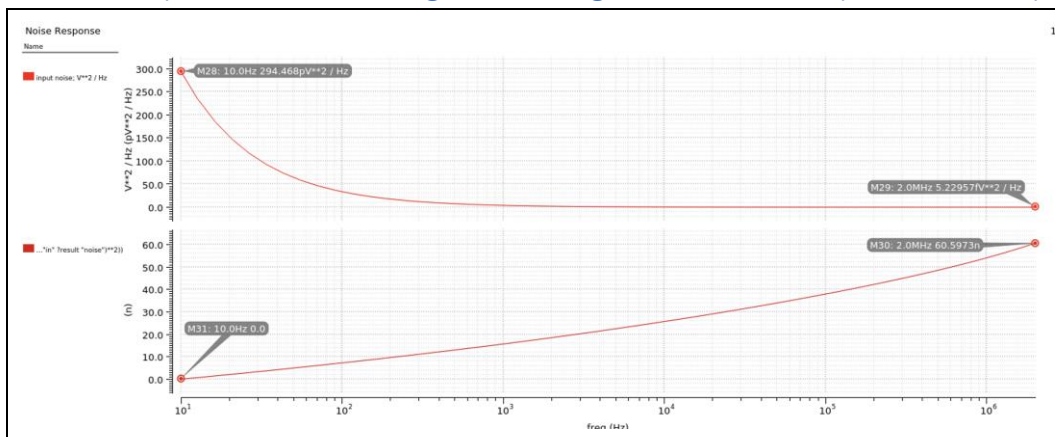
- Output swing (under Vcm=-600m)  $0.52 - (-0.7) = 1.2$
- Show the small range for Vd-linear because of the high gain and open loop



- Gain= 43dB, GBW=2.3M

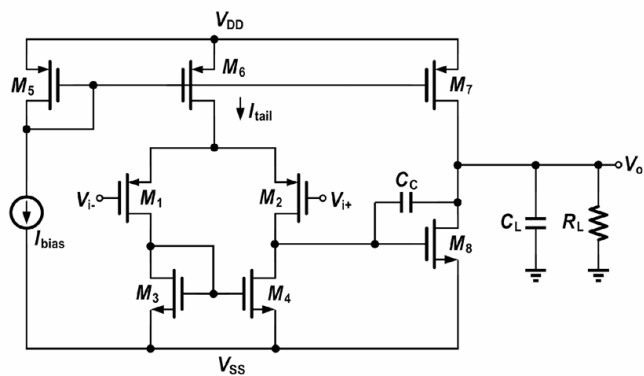


- Plot and report (from simulations) the input referred noise density (what this does mean?) and find RMS voltage noise integrated in the band (10 Hz – 2 MHz).



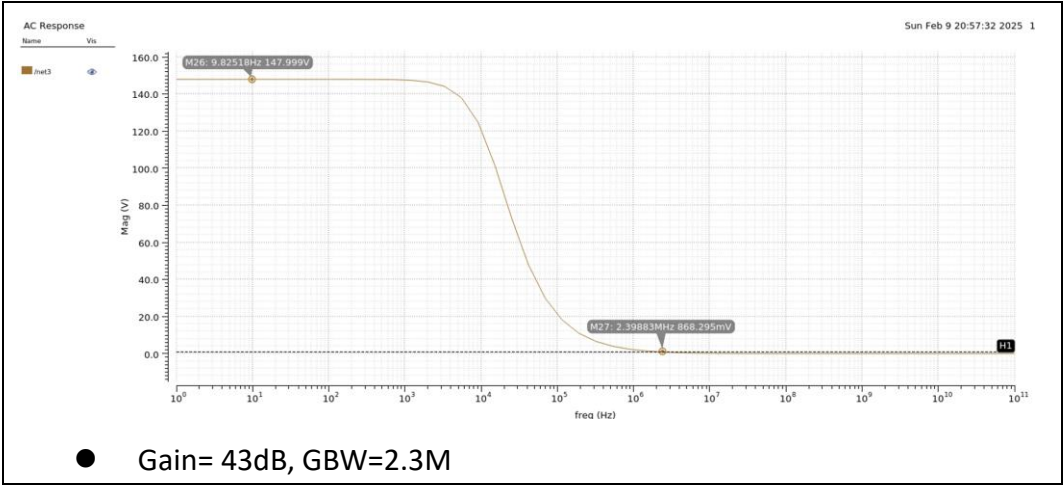
- In analog circuit design (such as op-amps and ADCs), the **input-referred noise density** represents all noise sources **referred back to the input**, making it easier to evaluate their impact on the signal.
  - Input-Referred Noise Density = Total Output Noise Density / Gain<sup>2</sup>
  - Top Curve (pV<sup>2</sup>/Hz) → Input-Referred Noise Density**  
 At **low frequencies (~10 Hz)**, noise is higher, which is mainly due to **1/f (Flicker) noise**.  
 At **high frequencies (~2 MHz)**, the noise density stabilizes, dominated by **thermal noise**.
  - Bottom Curve (nV) → Integrated RMS Noise**  
 This curve represents the **cumulative noise across the 10 Hz to 2 MHz band**.  
 As frequency increases, **total integrated noise accumulates**, leading to a higher noise voltage.
- In addition, provide comparison tables of hand-calculated vs. final transistor sizes, and required specs (Table 1-1) vs. simulated specs. Comment on your results.

Due to the miscalculation of PM and didn't consider about the Vcm range, I redesign the circuit into following size

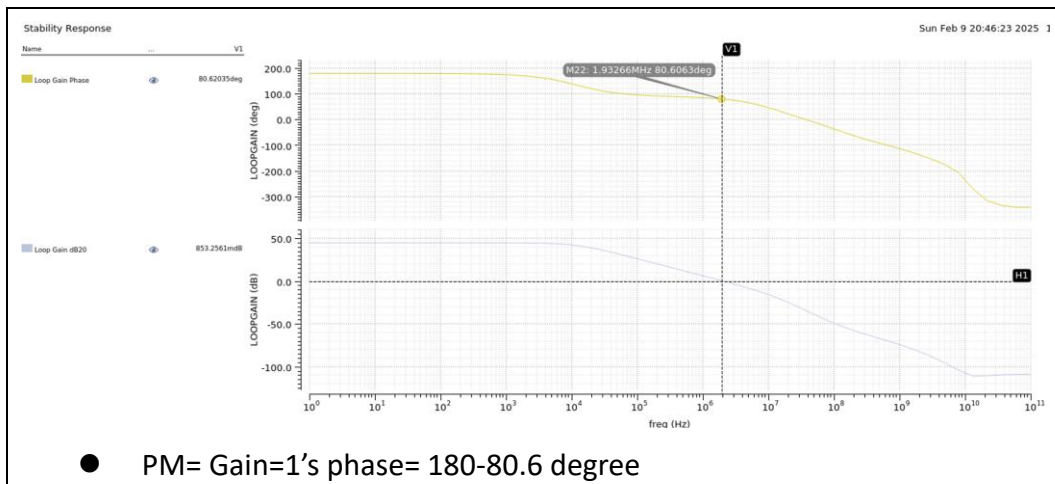


|                   | Pre       | Post      |                | Pre        | Post |
|-------------------|-----------|-----------|----------------|------------|------|
| I <sub>bais</sub> | 20u       | 20u       | A <sub>v</sub> | 196        | 146  |
| C <sub>c</sub>    | 16p       | 3p        | GBW            | 2.48M      | 2.3M |
| M1                | 10u/0.18u | 2u/0.27u  | PM             | 60.18(mis) | 80   |
| M2                | 10u/0.18u | 2u/0.27u  | Swing          | 1.56       | 1.2  |
| M3                | 5u/0.18u  | 2u/0.27u  |                |            |      |
| M4                | 5u/0.18u  | 2u/0.27u  |                |            |      |
| M5                | 5u/0.18u  | 2u/0.27u  |                |            |      |
| M6                | 5u/0.18u  | 1u/0.27u  |                |            |      |
| M7                | 10u/0.18u | 10u/0.27u |                |            |      |
| M8                | 10u/0.18u | 20u/0.27u |                |            |      |

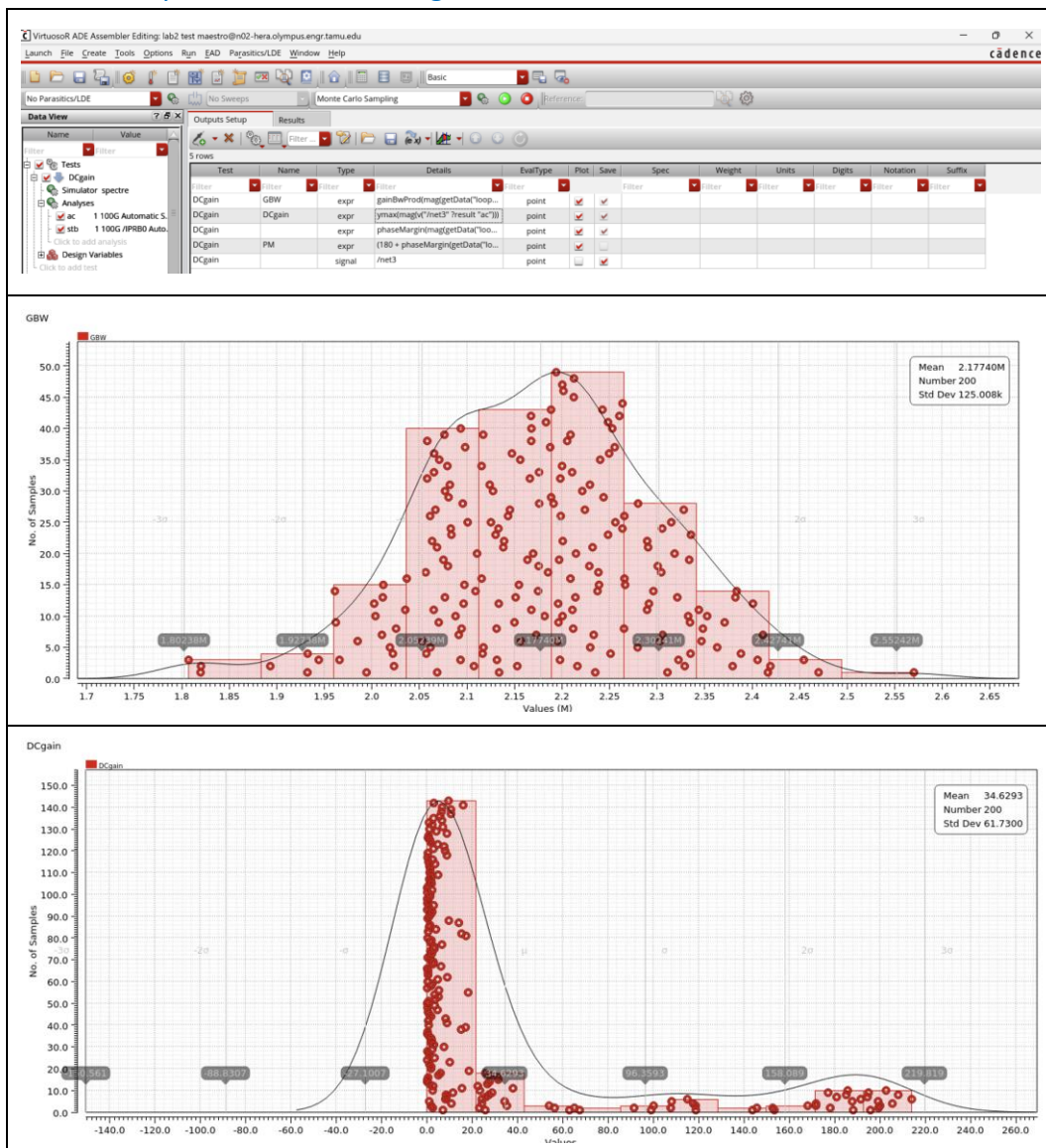
4. Plot the magnitude and phase response of your amplifier. Measure the phase margin and unity gain frequency from simulations.

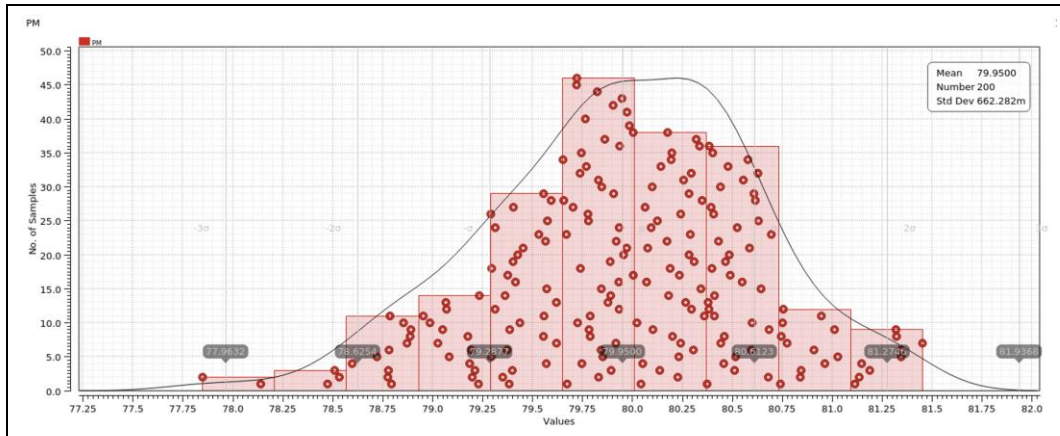




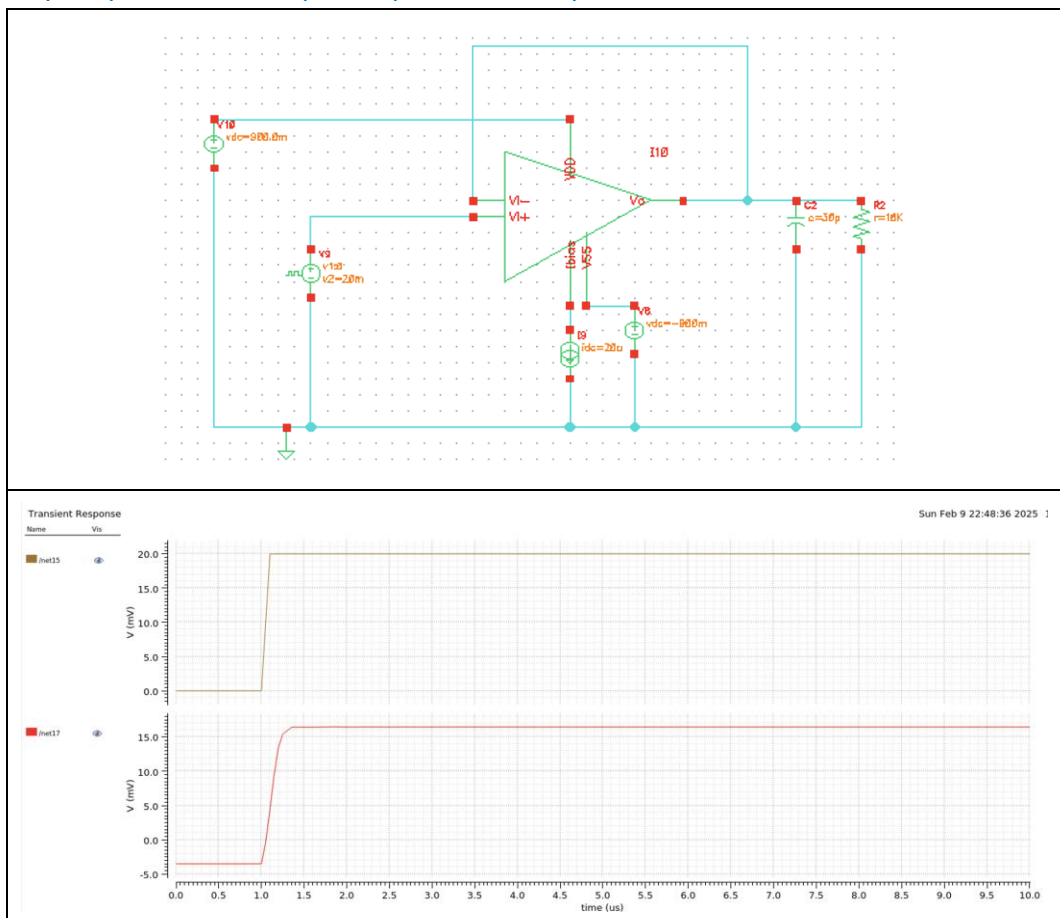


5. Simulate statistical simulation, Monte-Carlo, for GBW, Phase Margin and DC gain at least 200 points. Plot the histograms.





6. Close the loop to implement a unity gain buffer (b factor =1) and measure the step response for an input step of 20mV. Report the results.



7. Close the loop with two resistors of 100kΩ and/or larger to implement a 6dB gain inverting amplifier. Report the 250mV step response. Any ringing? Explain your results.

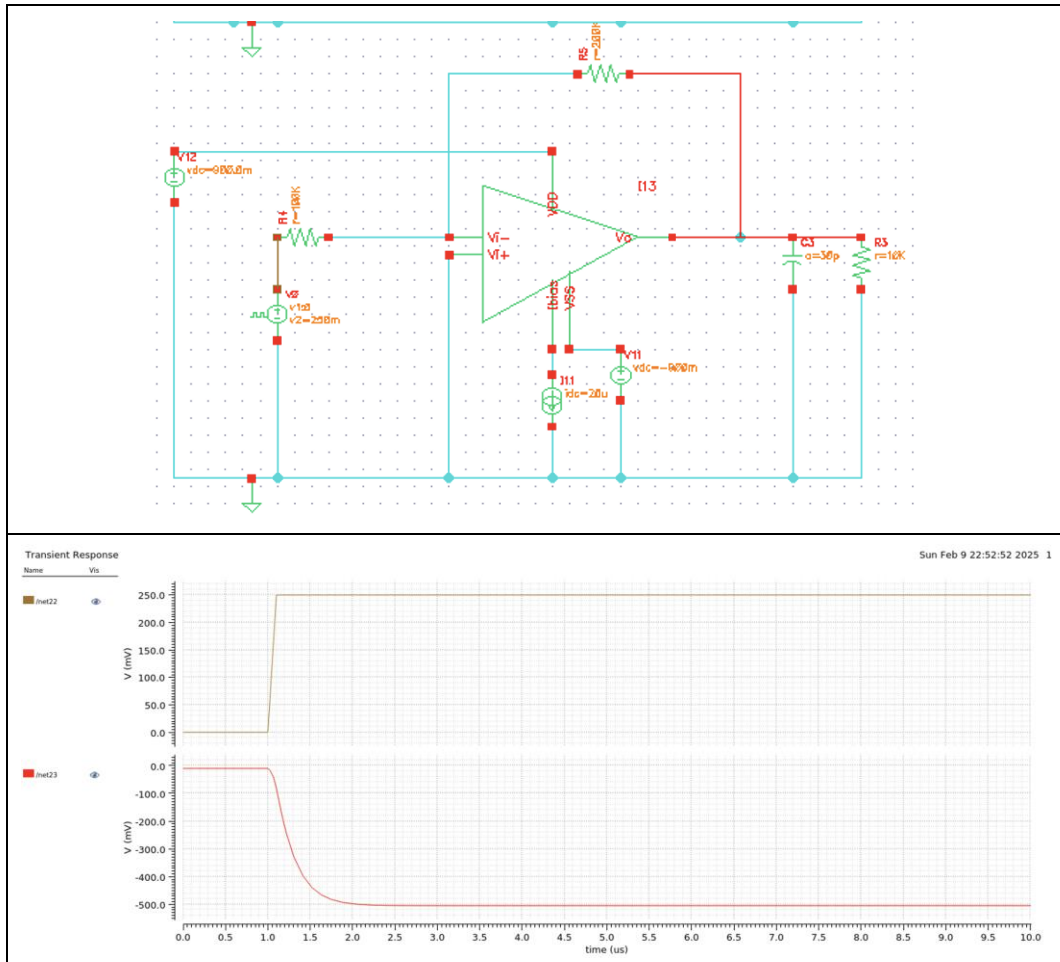
$$H(s) = \underbrace{\left( \frac{R_{in} + R_F}{R_{in}} \right)}_{\text{linear}} \underbrace{\left( \frac{1}{1 + \frac{1}{A_V \left( \frac{R_{in}}{R_{in} + R_F} \right)}} \right)}_{\text{non-linear}} \cong \left( \frac{R_{in} + R_F}{R_{in}} \right) \left( 1 - \frac{1}{A_V \left( \frac{R_{in}}{R_{in} + R_F} \right)} \right)$$

$\frac{1}{1 + \frac{1}{\infty}} \approx 1$

In case of **large loop gain**  $A_V \left( \frac{R_{in}}{R_{in} + R_F} \right) \gg 1$ , the system can safely be approximated by the first factor, then we called this term as the ideal system transfer function

$$H_{ideal}(s) = \left( \frac{1}{\beta} \right) = \left( \frac{R_{in} + R_F}{R_{in}} \right) = 1 + \frac{R_F}{R_{in}} \quad L = A\beta \quad (\text{VLSI Ch5})$$

when  $A \rightarrow \infty$   $L = \frac{1}{\beta}$



- $PM > 60^\circ \rightarrow$  Smooth response, minimal overshoot or ringing.
- $PM 30^\circ \sim 60^\circ \rightarrow$  Some overshoot and slight ringing.
- $PM < 30^\circ \rightarrow$  Significant overshoot, potential sustained oscillation