

24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab2: Layout Design, Simulation and Verification in Cadence

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Section:601

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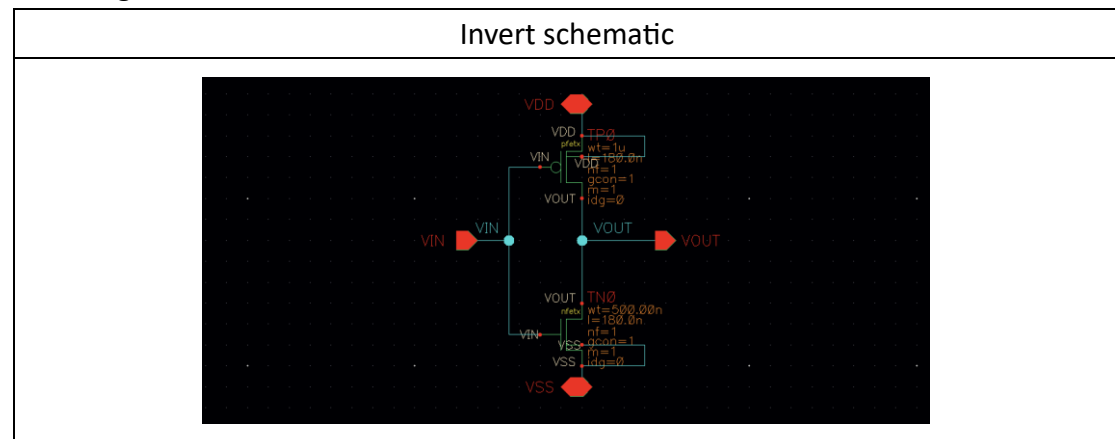
TA: Troy Buhr

Description:

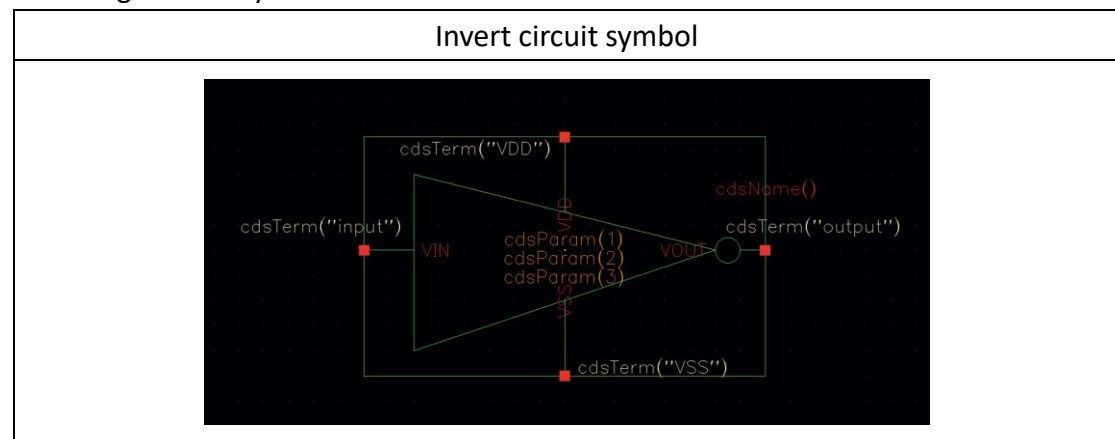
In this lab, we began by creating an inverter circuit and its symbol. Later, we learned how to conduct a post-layout simulation to evaluate the Design Rule Check (DRC) and the Layout versus Schematic (LVS).

Design & result

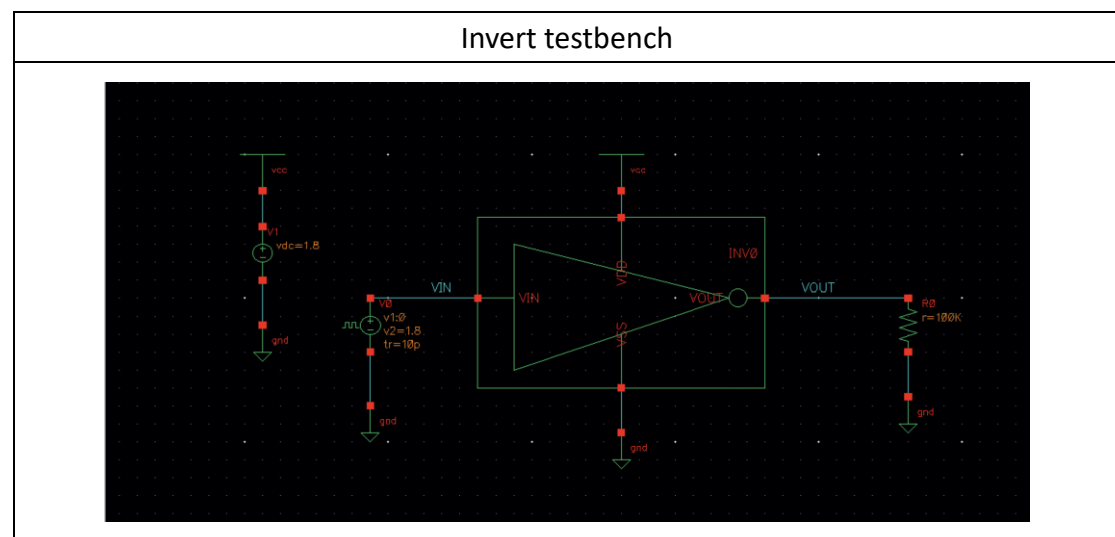
1. Design of the schematic



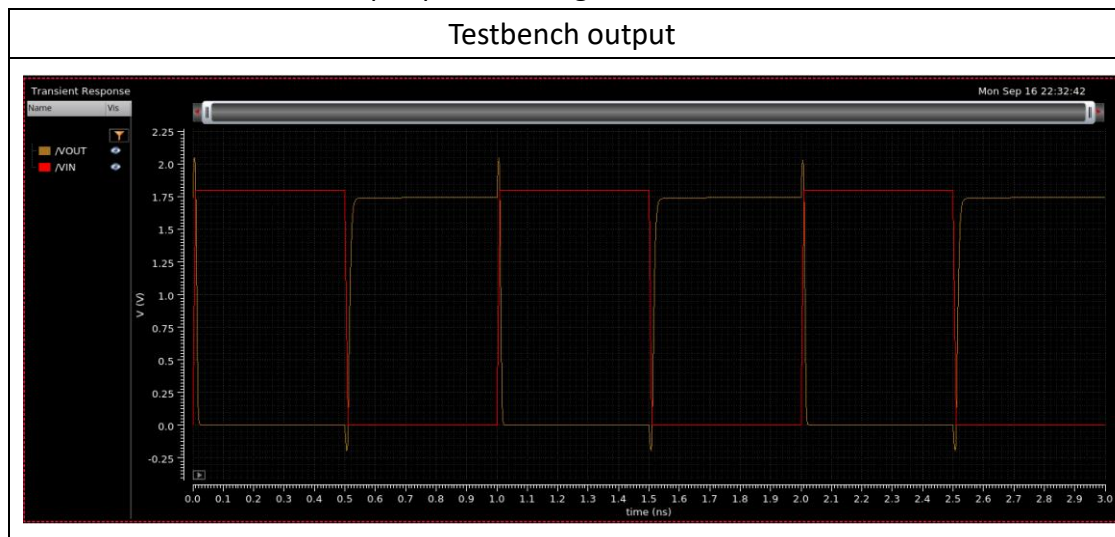
2. Design of the symbol



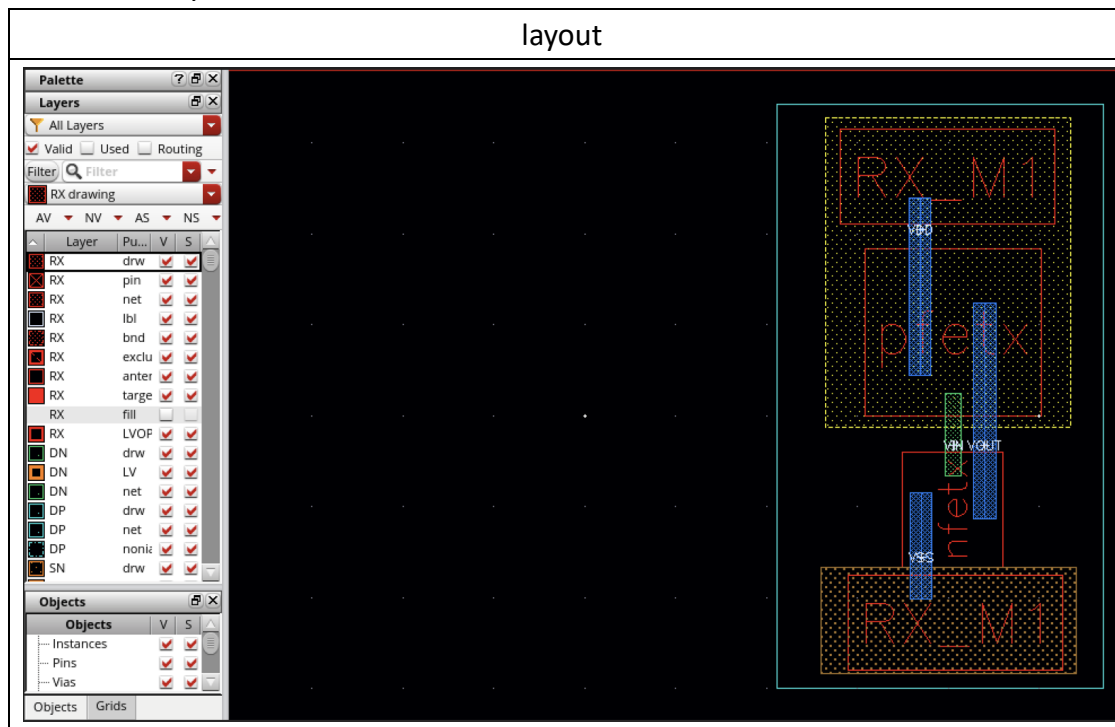
3. Schematic simulation on a test bench

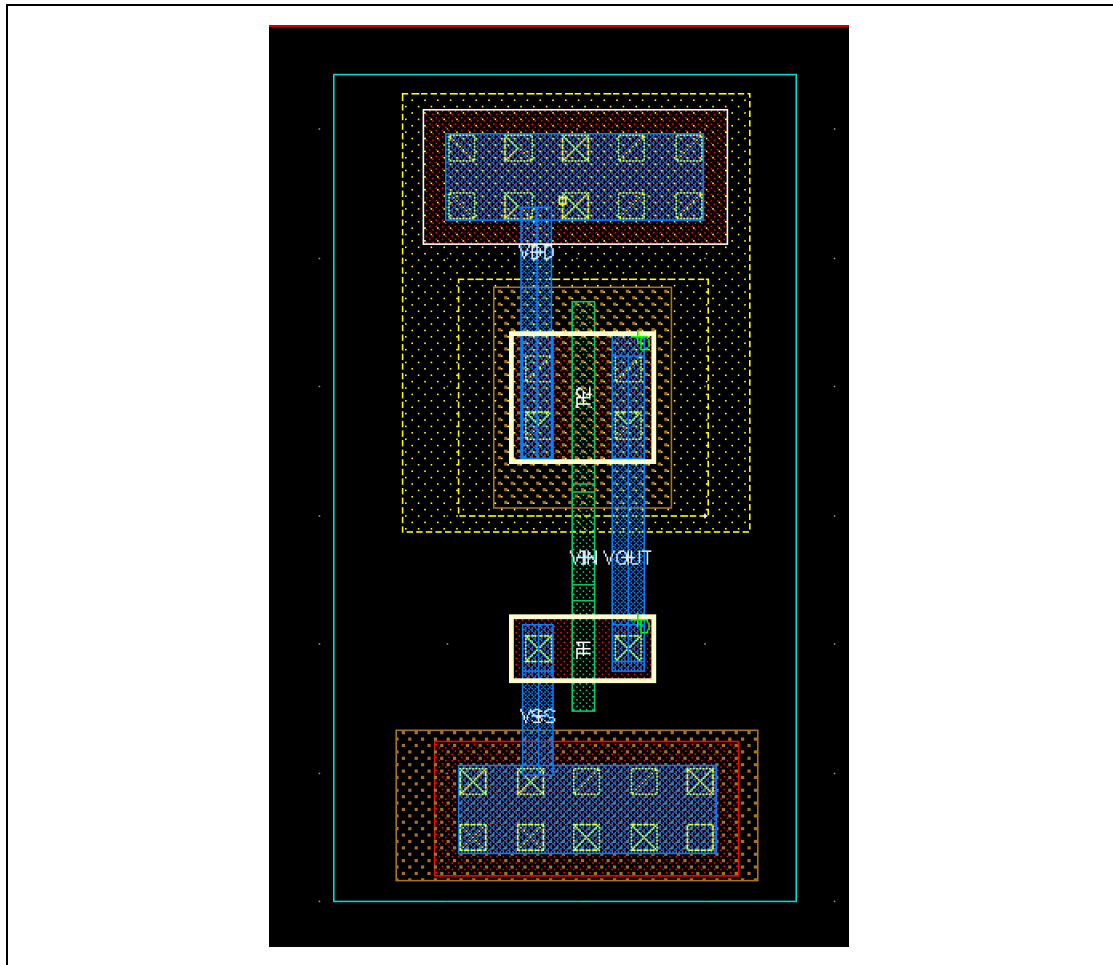


4. Transient simulation output plot showing VOUT and VIN

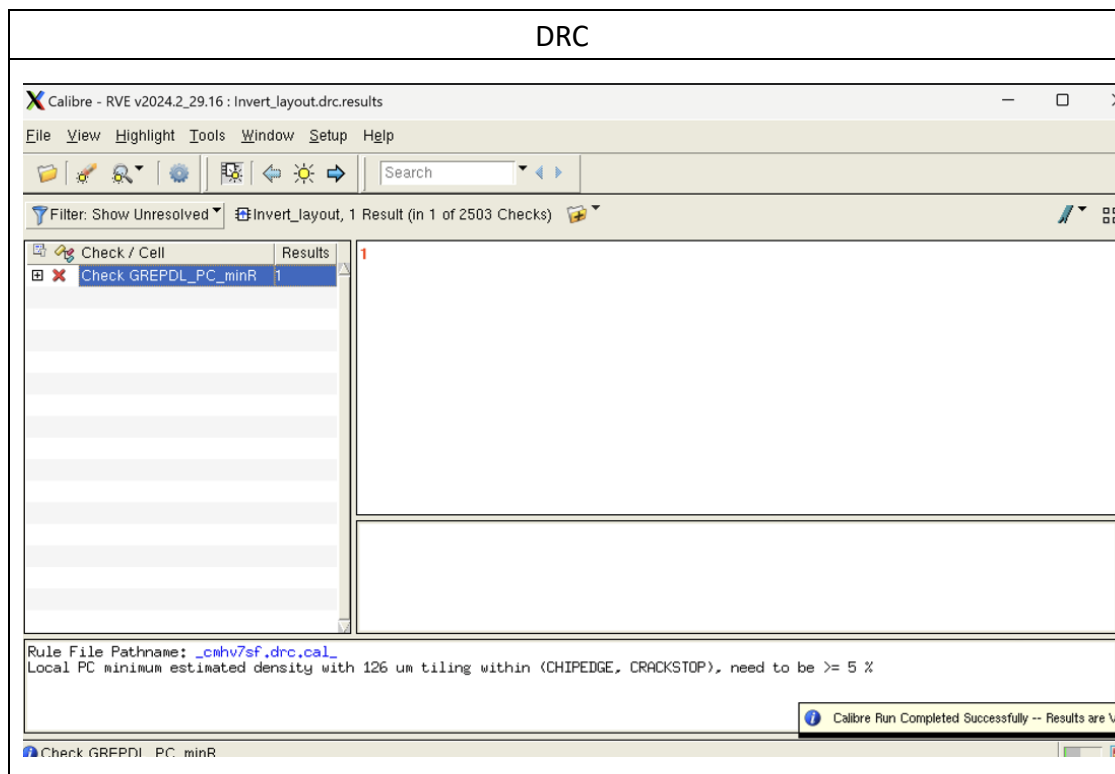


5. Inverter layout



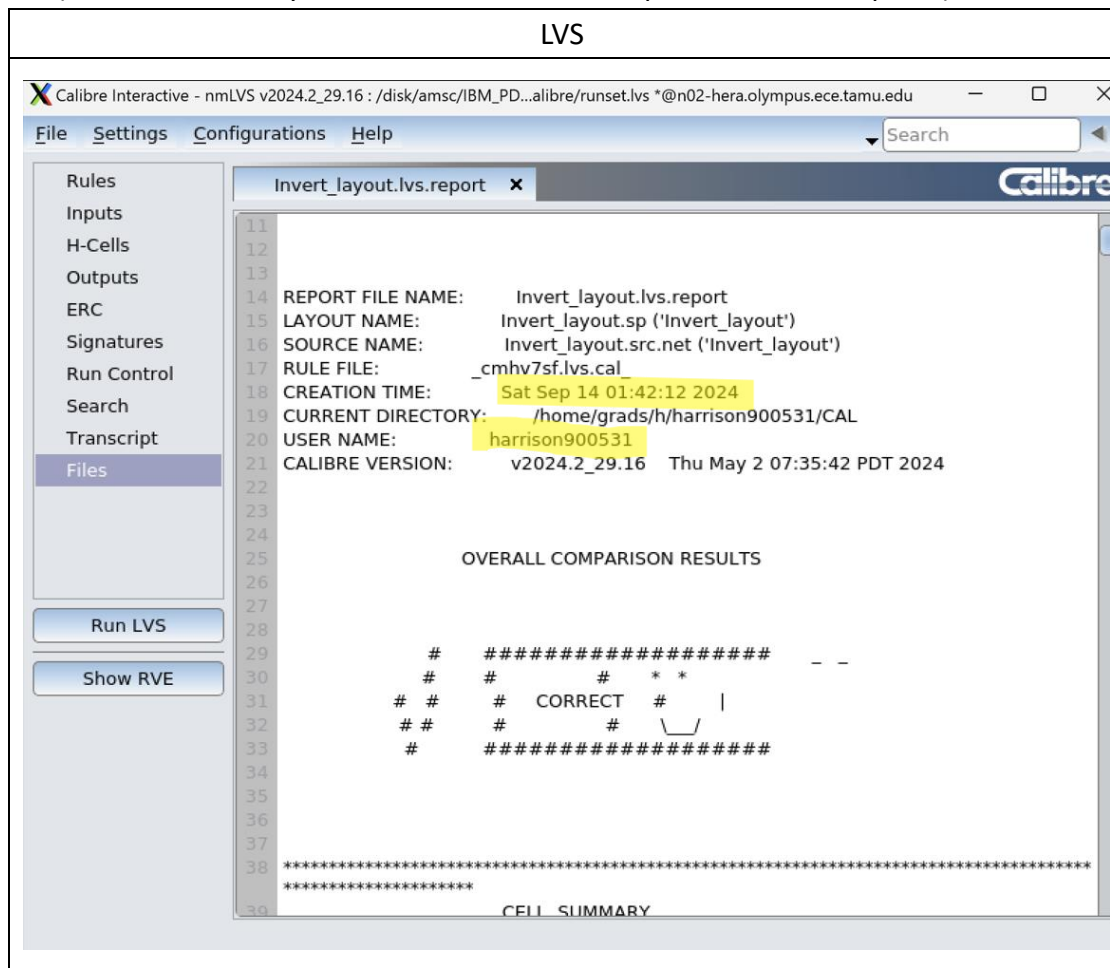


6. Screenshot of the DRC RVE window with results filtered to “show unresolved”

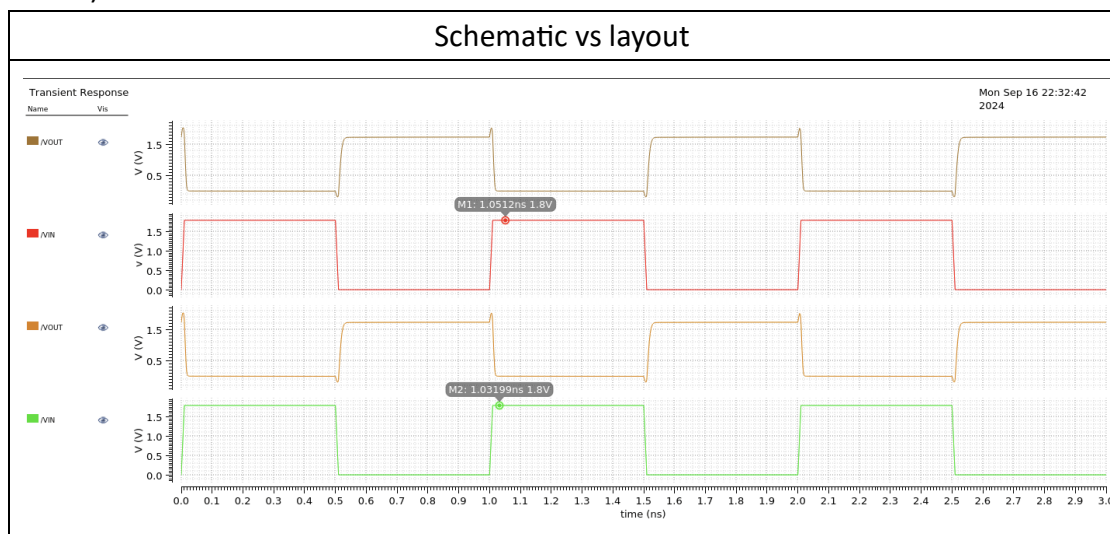


7. Copy of the LVS output file showing that the netlists match

(needs to include your NetID and a time stamp in the screen capture)



8. Plot of the post-layout simulation (display post-layout simulation results in a single window with the pre-layout simulation results as well to make differences between the two more visible).



- The red and the green line represent the schematic and layout vin
- The brown and orange line represent the schematic and layout vout

Discussion:

In this lab, we began by creating an invert schematic and converting it into a symbol for testing. Finally, we drew a layout for this inverter.

When I first ran the Design Rule Check (DRC), I get an error regarding the width of the wires that connect two gates, drains, and sources to VCC and GND. After adjusting the wire thickness to match the original connection points on the layout, the DRC error was resolved. I think the underlying reason for this issue is related to the DRC protocol and the λ rule that the professor discussed in the lecture on MOS layout.

When I encountered the final error about the density in the DRC, I was still confused about the reason behind it. However, a week later, the professor explained that the reason is because building the metal layer on top of each previous layer requires filling the empty spaces with metal, even though it is not utilized. This process ensures that the subsequent metal layer remains as flat as possible.

Conclusion:

After completing Lab 2, we have gained a fundamental understanding of the integrated circuit (IC) design flow. We also learned how to create a "symbol" in Virtuoso, and most importantly, we acquired knowledge of the basic layout process.