24 Fall ECEN 704: VLSI Circuit Design

Design Pre-lab Report

Lab3: Layout Design Techniques

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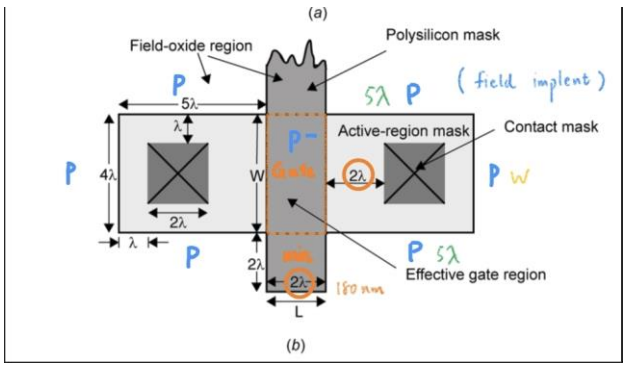
1. What are the absolute minimum dimensions of a transistor? Explain your reasoning. Remember to consider minimum contact size. Do we actually use this minimum size or do we use a slightly larger size for convenience?

The dimensions of a transistor refer to the physical sizes of its key structural elements. According to this definition, I think the minimum dimension of a transistor is determined by the λ rule mentioned by the professor in the lecture. Typically, the minimum dimension is 2λ. For example, in the 180nm process, the length (L) of the gate will be 2λ = 180nm.

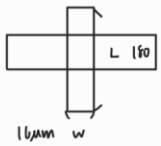


We don't actually use the minimum size; in fact, we usually use slightly lager size. It is because some of the reasons below.

- During fabrication, variations can occur due to reasons like equipment limitations, temperature fluctuations, and material. Using slightly larger size can mitigate these affects and make the performance more predictable.
- Using the absolute minimum channel length increases short-channel effects, leading to issues like leakage currents and lower threshold voltages.
- Also in smaller devices, hot carrier effects will also cause the shift of Vt.

2. Draw a common-centroid layout of a simple current mirror with equal size transistors of L = 180nm and W = 16 µm. Use a finger width of 500 nm for each transistor segment. Remember to draw the drain, source, gate and bulk connections. Use dummy transistors and all other good layout techniques learned in the lab. Include a floor plan.

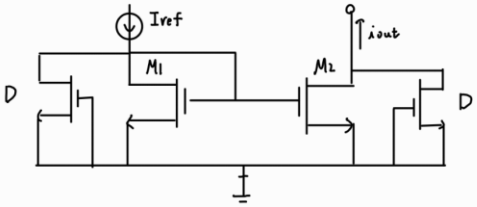
2.

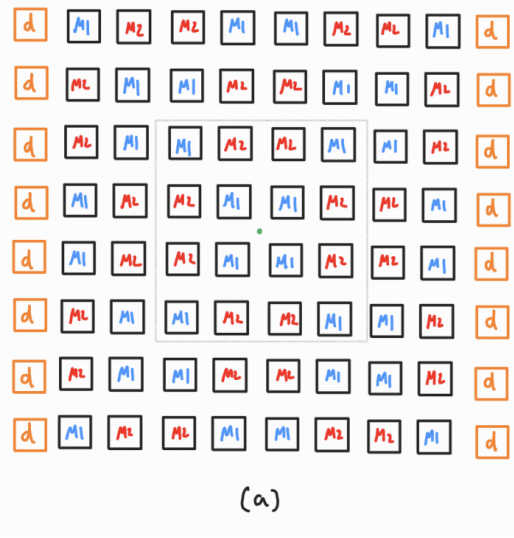


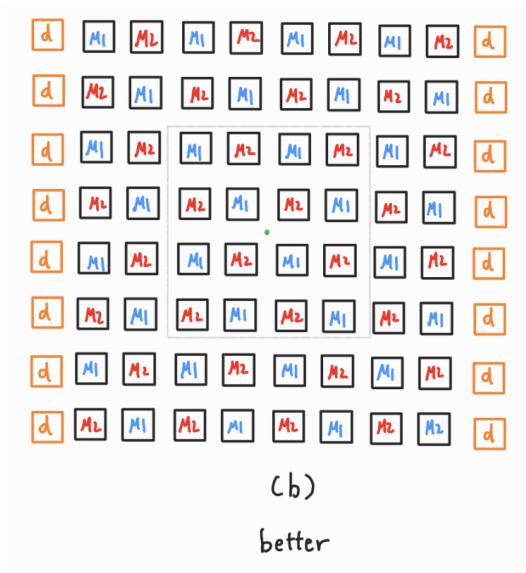
finger W = 0.5 μm

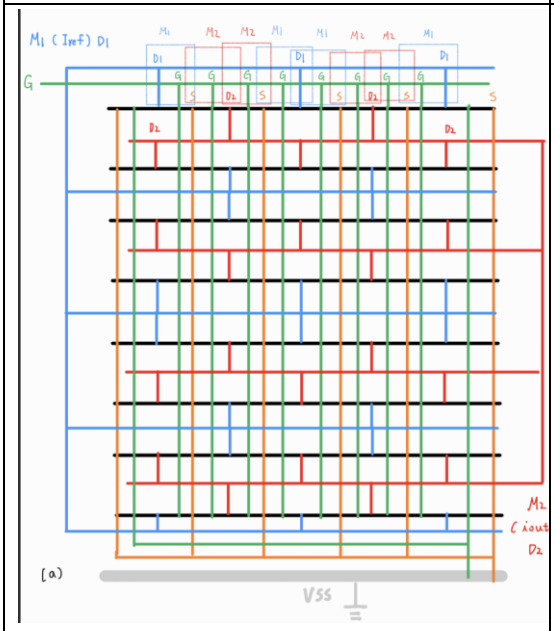
$\frac{\text{Total } 16\mu m}{0.5\mu m} = 32$ 32 X 2 current mirror = 64

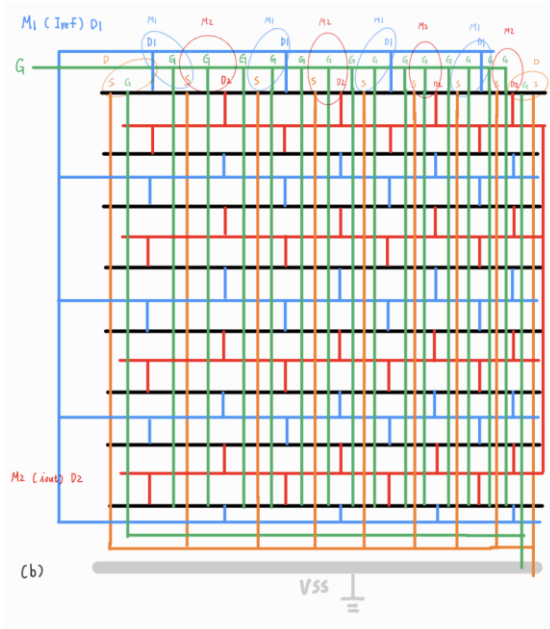
getting best common-centroid layer → 8x8











3. Design a common-centroid layout for a MOM capacitor array. The capacitors have a ratio of 1.3:1. The capacitor array should consist of eight unit capacitors (i.e. I1 = I 2 = 4) and one non-unit capacitor. Determine the form of the common-centroid layout and interconnect the capacitors. Each unit capacitance should have a separate top and bottom plate. Do not use a common bottom plate. Use the techniques described in the lab manual to give good matching. Also, give the size of the non-unit capacitor. The unit capacitor is 10.56 µm x 10.56 µm (W x L).

3. $\frac{C1}{C2} = \frac{1}{1.3} = \frac{I_1 C_u}{I_2 C_u + N C_u} \Rightarrow \frac{4 C_u}{4 C_u + N C_u}$

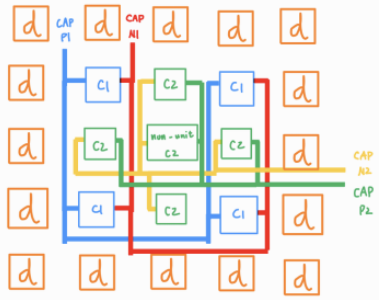
$4 C_u + N C_u = 5.2 C_u \qquad N = 1.2$

non-unit C:

$L_{nu} = L_o (N + \sqrt{N(N-1)}) = 10.56 (1.2 + \sqrt{1.2 \times 0.1})$

$= 17.845\ \mu m$

$W_{nu} = N \frac{L_o^2}{L_{nu}} = 1.2 \frac{(10.56\mu)^2}{17.845} = 7.498\ \mu m$



4. Design two matched polysilicon (oprppresx) resistors to realize a total resistance of 12 kΩ each. Remember to account for contact resistance. Determine the approximate length and width of the diffusion. Use an interdigitized layout with four resistance segments for each resistor. Use good layout techniques.

4. total = 12kΩ / 4 each = 3kΩ

$R_{num} = R_S \times \frac{L}{W} + 2 \frac{R_{con}}{W} \Rightarrow 3 = 0.165 \times \frac{L}{W} + 2 \times \frac{0.015}{W}$

$3W = 0.165 \times L + 0.03$ When $W = 1.8\ (\mu m)$ $L = 32.54\ (\mu m)$

(10 times 180 nm)