

24 Fall ECEN 704: VLSI Circuit Design

Design Pre-lab Report

Lab6: Differential Pairs

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1. Compare the two single-ended differential amplifiers discussed in this lab. Rate the differential gain, common-mode gain, output voltage swing range, CMRR and common-mode input voltage range. Include expressions for each design specification.
2. Design the simple differential amplifier in Figure 6-6 to obtain the following specifications:

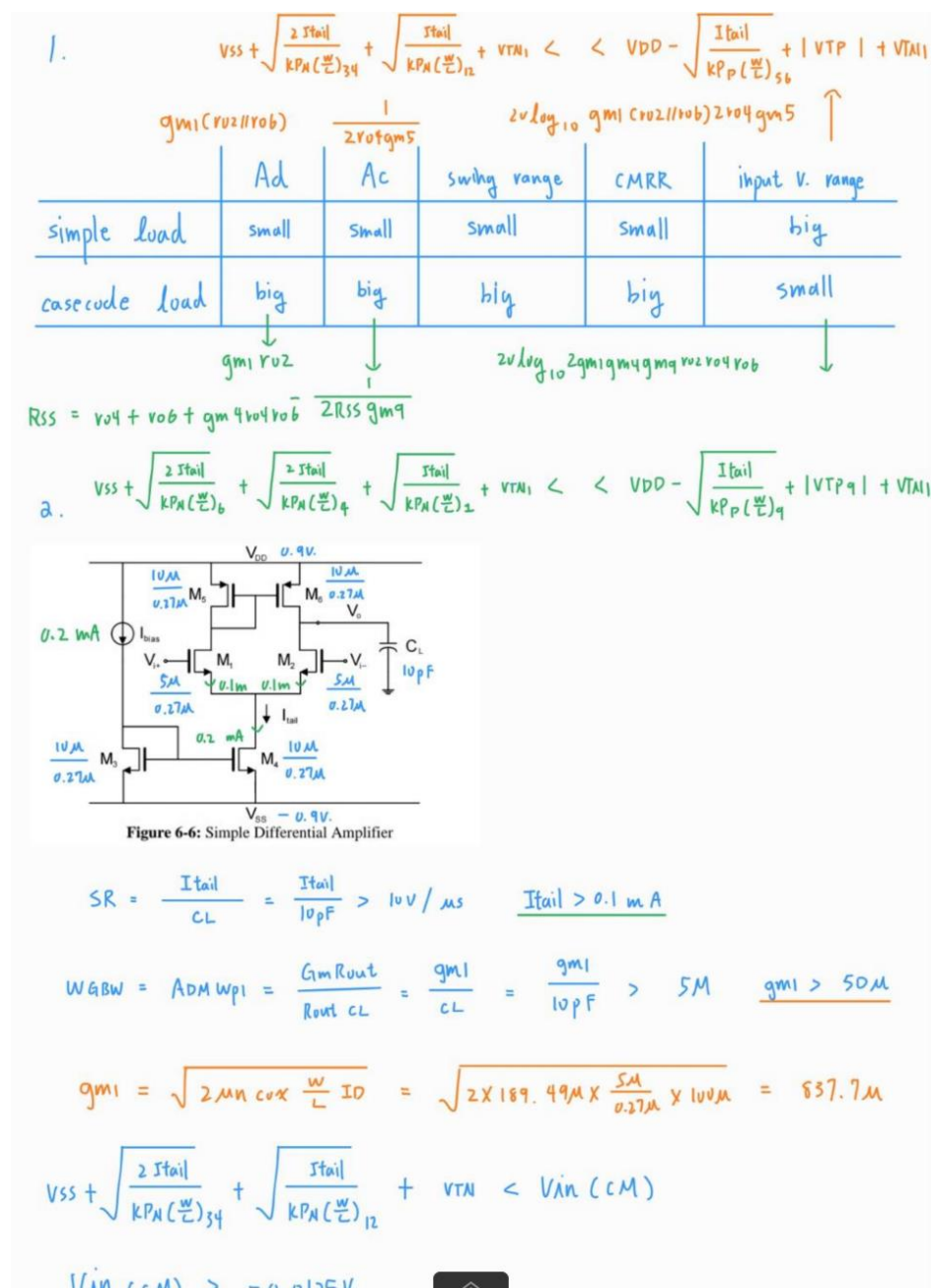
Slew Rate > 10 V/μs

Gain-Bandwidth Product > 5 MHz

Common-mode Input Voltage Range > 0.5 V

Power Supply $V_{DD} = -V_{SS} = 0.9$ V

Load Capacitance 10 pF



3. Design the differential amplifier with cascode current mirrors in Figure 6-8 to obtain the following

specifications:

Slew Rate $> 10 \text{ V}/\mu\text{s}$

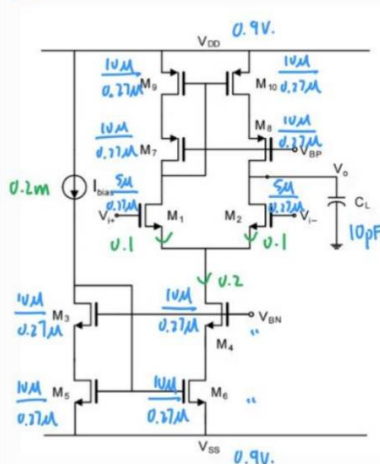
Gain-Bandwidth Product $> 5 \text{ MHz}$

CMRR $> 60 \text{ dB}$

Power Supply $V_{DD} = -V_{SS} = 0.9 \text{ V}$

Load Capacitance

3.



$$SR = \frac{I_{tail}}{C_L} = \frac{I_{tail}}{10pF} > 10V/\mu s \quad \underline{I_{tail} > 0.1mA}$$

$$WGBW = ADM \omega_{p1} = \frac{G_m R_{out}}{R_{out} C_L} = \frac{g_m}{C_L} = \frac{g_m}{10pF} > 5M \quad \underline{g_m > 50\mu}$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \sqrt{2 \times 189.49\mu \times \frac{5\mu}{0.27\mu} \times 100\mu} = 837.7\mu$$

$$CMRR = 20 \log \frac{ADM}{ACM} \approx 20 \log_{10} (2 g_m g_{m4} g_{m9} r_{o2} r_{o4} r_{o6})$$

$$g_{m1} = 837.7\mu \quad g_{m4} = 1675.48\mu \quad g_{m9} = 837.7\mu$$

$$r_{o4} = 68.49K \quad r_{o4} = r_{o6} = 34.246K$$

$$CMRR = 105.5dB$$