ECEN 474/704 Lab 2: Layout Design, Simulation and Verification in Cadence

In this lab, the following design steps will be performed for a simple inverter circuit:

1. Design of the schematic
2. Design of the symbol
3. Schematic simulation on a test bench
4. Design of the layout
5. Design rule check (DRC)
6. Layout versus schematic (LVS)
7. Parasitic extraction (PEX)
8. Post-layout simulation

Inverter Schematic

Schematic cells should be designed with input and output pins to allow generation of their symbol views. After placing and wiring the transistors for the inverter circuit (named Inv1), pins can be added using the menu item *Add* → *Pin* or "P" hotkey to pull up the pin editor. Pin names and directions need to be consistent within the schematic and symbol views, where the "inputOutput" direction is recommended for power supplies. It is recommended to use uppercase letters when naming pins to distinguish them from nets within the sub-circuit. Spaces are not allowed in pin names. Additionally, underscores ("_") are the only special character allowed in pin names. The use of other special characters like "+" or "–" as part of pin names can lead to errors during the LVS phase. When complete, the schematic should resemble Figure 2-1.

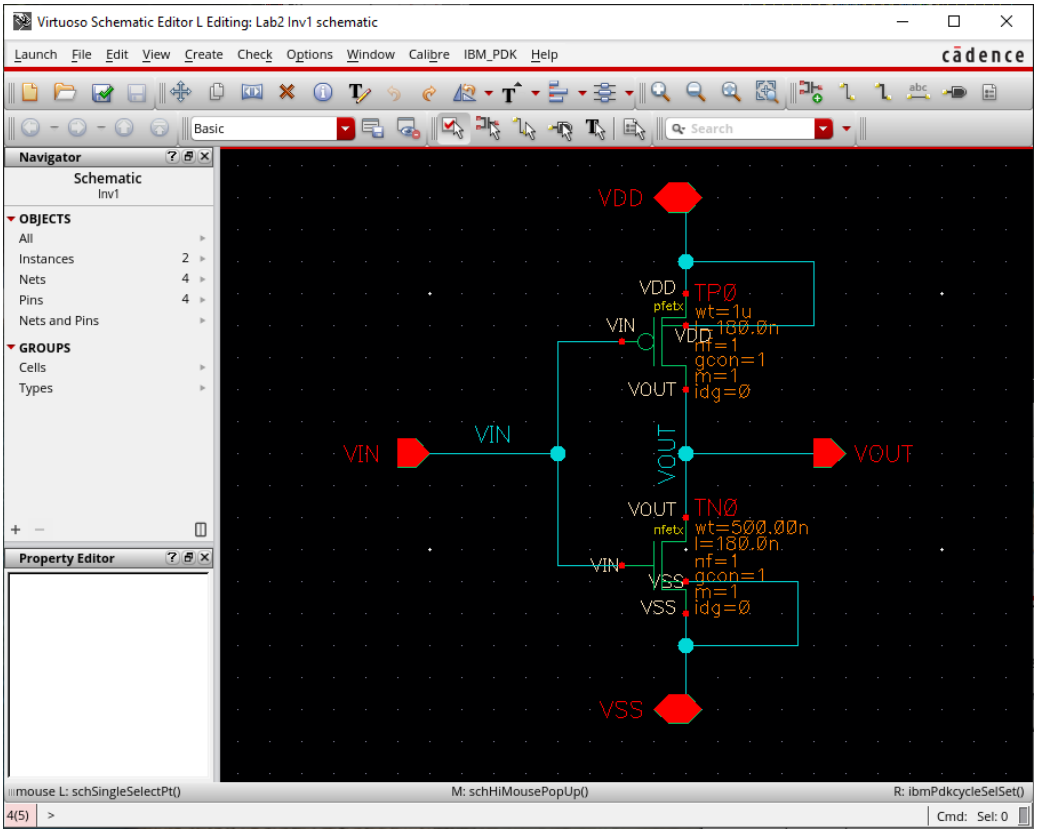

Figure 2-1: Complete Inverter Schematic with Input and Output pins

Inverter Symbol

In the schematic window, select *Create* → *Cellview* → *From Cellview* and click OK (Figure 2-2). In the next window arrange the pin specifications and click OK. Note that when listing pins from right to left they will appear from right to left on the top and bottom and when listed from right to left on the "Left Pins" and "Right Pins" fields they will appear from top to bottom in that order. Next, the symbol editor will appear with the default symbol, which is a box with inputs and outputs. Edit the symbol using the drawing tools such that it resembles the one in Figure 2-3. The origin of the symbol can be adjusted by selecting *Edit* → *Origin*, and then clicking the position on the symbol where you want the origin to be (the origin of the symbol is the point that will be directly under your mouse when placing the symbol in a schematic). The instance name prefix can be changed by selecting *Edit* → *Properties* → *Cellview…*, or using the Shift-Q hotkey. In the window that appears, show the system properties by checking the "system" box at the top of the window. The "instNamePrefix" field is a letter-only abbreviation that will begin every name of the symbol when placed in another schematic. The default abbreviation is typically "I," but this could be changed to "INV" to more clearly indicate that the instance name refers to an inverter. Modifying this prefix for a cell can provide clarity in simulations when saving internal signals of a subcircuit by better indicating where the signals are coming from. When finished creating the symbol, save and exit this window.

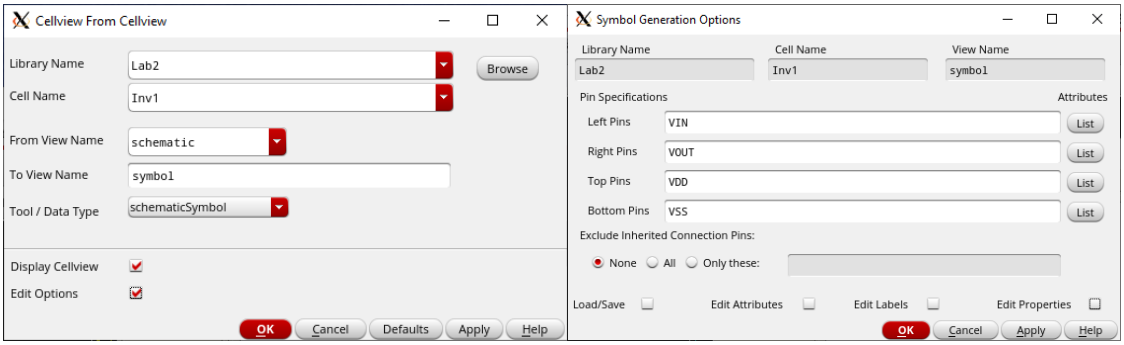

Figure 2-2: Creating a Symbol from a Schematic

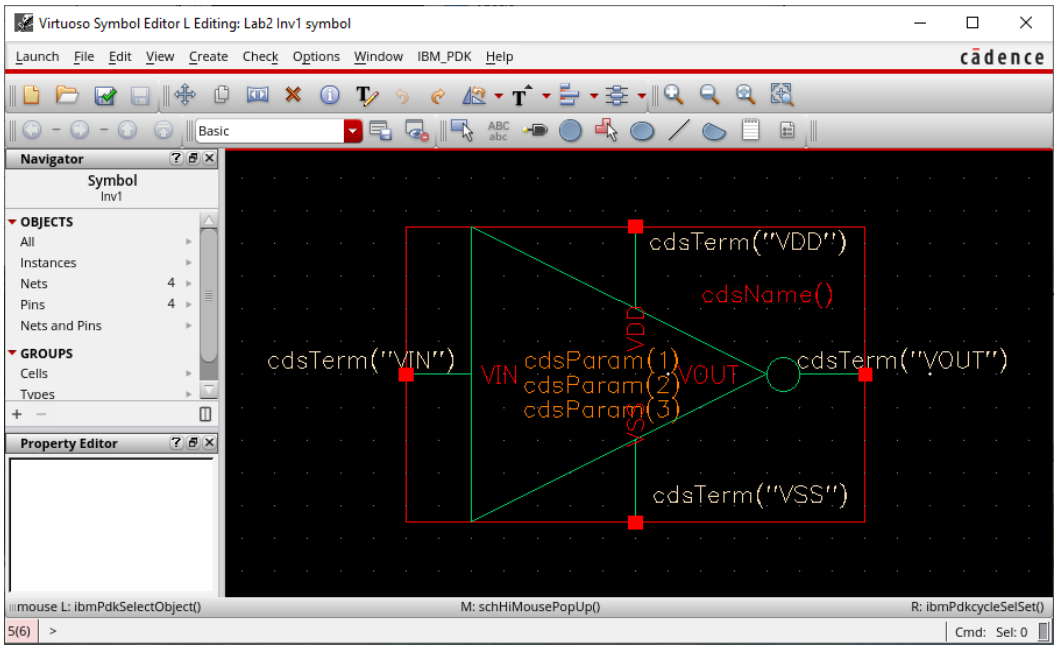

Figure 2-3: Final Inverter Symbol

Schematic Simulation on a Test Bench

To run simulations using the newly created symbol, we need to create a "test bench" or another schematic plane under the "Cell" field in the "Library Manager". To do this, go to the "Library Manager" window and select the design library, then select *File* → *New* → *Cell View* and title the new cell as "InvTest", then click OK. A new schematic plane should pop up and when an instance is added (remember, press "I") the symbol will appear under the "Inv1" cell when it is highlighted. Next, create the test bench configuration shown in Figure 2-4. The parameters of the voltage source at "VIN" are displayed in the "Property Editor" sub-window near the bottom-left of Figure 2-4. Finally, start the simulator by selecting *Launch* → *ADE L,* and plot VOUT and VIN after running a transient simulation for 3ns. **Note that post-layout simulations cannot be performed directly on the transistor-level schematic of a cell/subcircuit. A test bench must be created for proper post-layout simulations.**

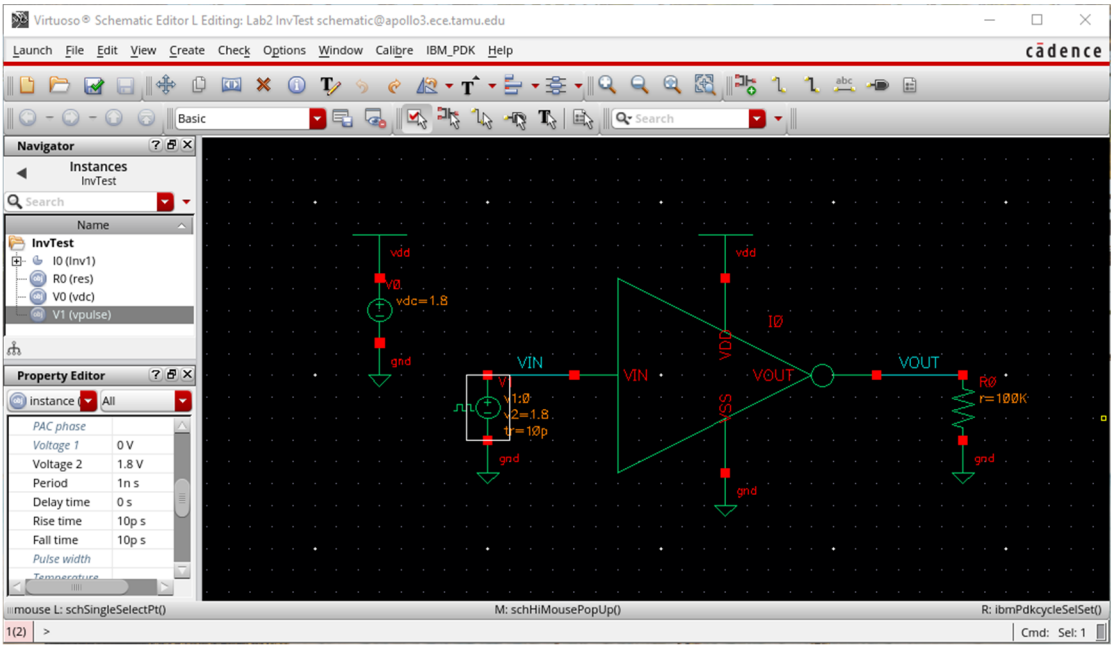

Figure 2-4: Inverter Test Bench Schematic

Inverter Layout

From the library manager select *File* → *New* → *Cell View*. Select Layout as the Type (Figure 2-5). After clicking OK (and OK again for the following two popup windows), Virtuoso Layout Suite should open as shown in Figure 2-6.

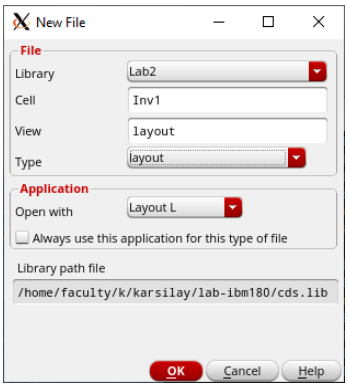

Figure 2-5: Creating a Layout Cell View

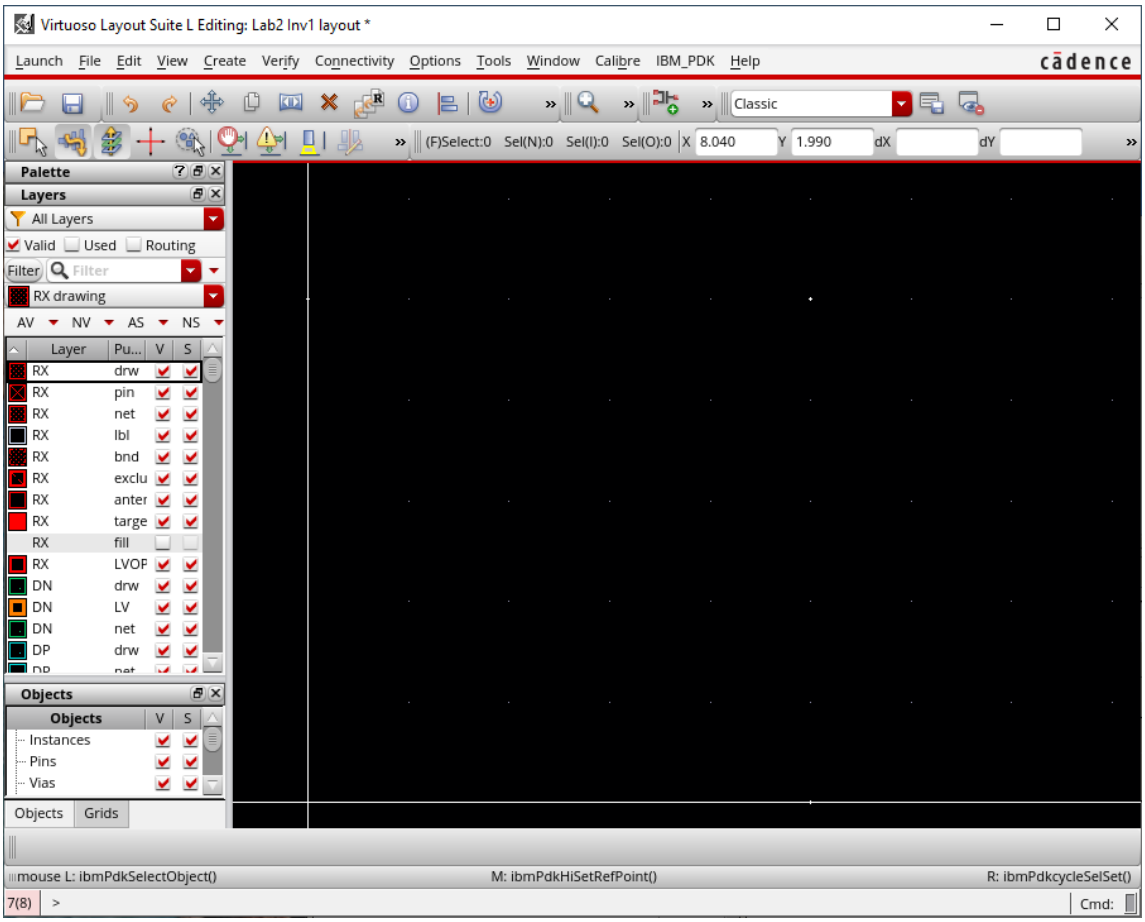

Figure 2-6: The Virtuoso Layout Suite

Gravity enables the cursor to only move to critical points on the layout design. For our purposes it is suggested that the student work with Gravity both on and off, and figure out which style is more practical. To toggle gravity on or off, go to *Options* → *Editor*, then disable (or enable) "Gravity On" (Figure 2-7).

As the first step, place the NFET on the layout. Hit "I" and then "Browse", then make sure under "Library" that **cmhv7sf** is highlighted. Under the "Cell" field scroll down to **nfetx** and then make sure that under "View" the word "layout" is highlighted. After placement, the transistor will first appear as a red box with the cell name on it, so Shift-F needs to be pressed to change the view to show the layers (Figure 2-8).

Next, the PFET needs to be placed above the NFET. Repeat the process except selecting **pfetx** instead of **nfetx**, and when the parameter window pops up be sure to change the width from 500 nm to 1 µm. PFET and NFET should be repositioned such that the centers of the two are vertically aligned. To do this, select a device and press "Q", then change the "Origin" X and Y such that both devices are aligned. Be sure to **deselect a device once you are done editing it by using Ctrl-d**.

Next, we need to add substrate contacts (i.e. vias between RX and M1 layers) using the hotkey "O" (or *Create* → *Via)*. The "Via Definition" field will be "RX_M1" for substrate contacts. Set Rows as 2 and Columns as 5, then place the vias above and below the transistors. The RX layer defines the active areas, which are heavily doped regions. When placed over the substrate material (the background of the layout viewer) or in an N-Well, RX defines n+ regions, whereas a combination (or overlap) of the RX and BP layers defines p+ regions on the common p- substrate. Therefore, a single N-Well should cover the entire

RX_M1 contacts and PMOS transistors to create the substrate connection for the PMOS devices. For NMOS devices, BP layer covering the RX_M1 contacts provides the substrate connection. These regions of higher doping for the substrate contacts are necessary to create good ohmic contact with the respective bulk material of the different types of transistors. Without these heavily doped regions, the difference in charge carrier density between the transistor bulk material and the metal used for routing would create a small depletion region, preventing a strong connection between the bulk material and the supply nets.

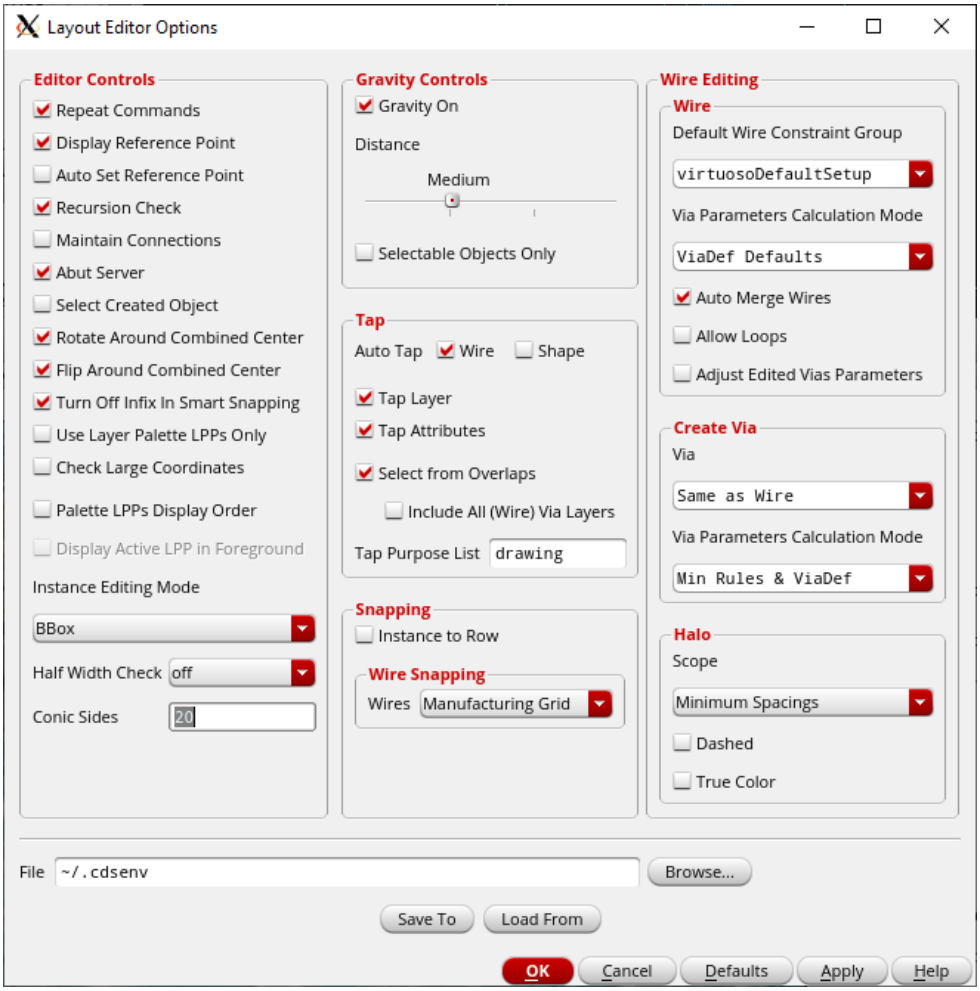

Figure 2-7: Window to Toggle Gravity Option

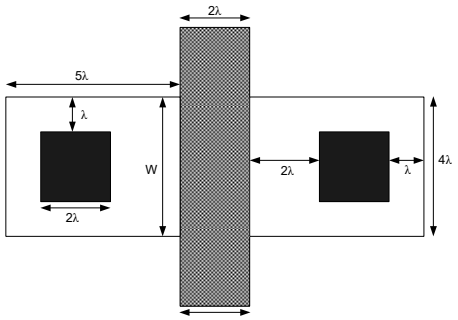

Figure 2-8: A View of the Transistor

To draw such layers, look to the left of the screen; it should have a list of layers and purposes. The layers can be grouped together by purpose and sorted alphabetically within a given purpose by clicking “Layer” at the top of the layer list followed by clicking “Purpose” at the top of the list. In these labs, we will primarily use layers with the “drw” (drawing) purpose field when adding structures to the layouts. Find the “NW” layer in the list and select it, or in the search bar above type "NW" to query the list for the N-well material. Now, we are ready to draw a rectangle by pressing the "R" hotkey and click and drag the N-well to encompass the RX_M1 vias and the PMOS transistor. Next, a BP layer will be needed to encompass RX_M1 vias of the NMOS (not including the NMOS though). Draw such a rectangle on the BP drawing layer using the same procedure.

Next, we will need to wire the transistors and power sources together. Under that same search bar, find "M1 drw" and wire the transistor sources and drains either using the "P" or "R" hotkeys. If you draw a trace that is too thin or too thick, you may stretch it by using the "S" hotkey. Then, find "PC drw" for the gate layers and wire the two gates together. Finally, a layer of GRLOGIC ("GR") will encompass the entire layout. To check the widths of the traces you can use the hotkey "K" for the ruler tool (Shift-K to delete). If a trace is too thin it will not pass the DRC. Some simple DRC rules relating to minimum dimensions and spacing for shapes in various layers can be displayed while creating a layout by toggling the “DRD Notify” () or “DRD Enforce” () settings near the top of the layout window. Only one of these options should be enabled at a time. Both options display similar information but affect the layout process in different ways. Try both options and determine which of these settings you prefer. However, running DRC is still necessary to identify and correct many other errors beyond these due to the increased complexity of the design rules.

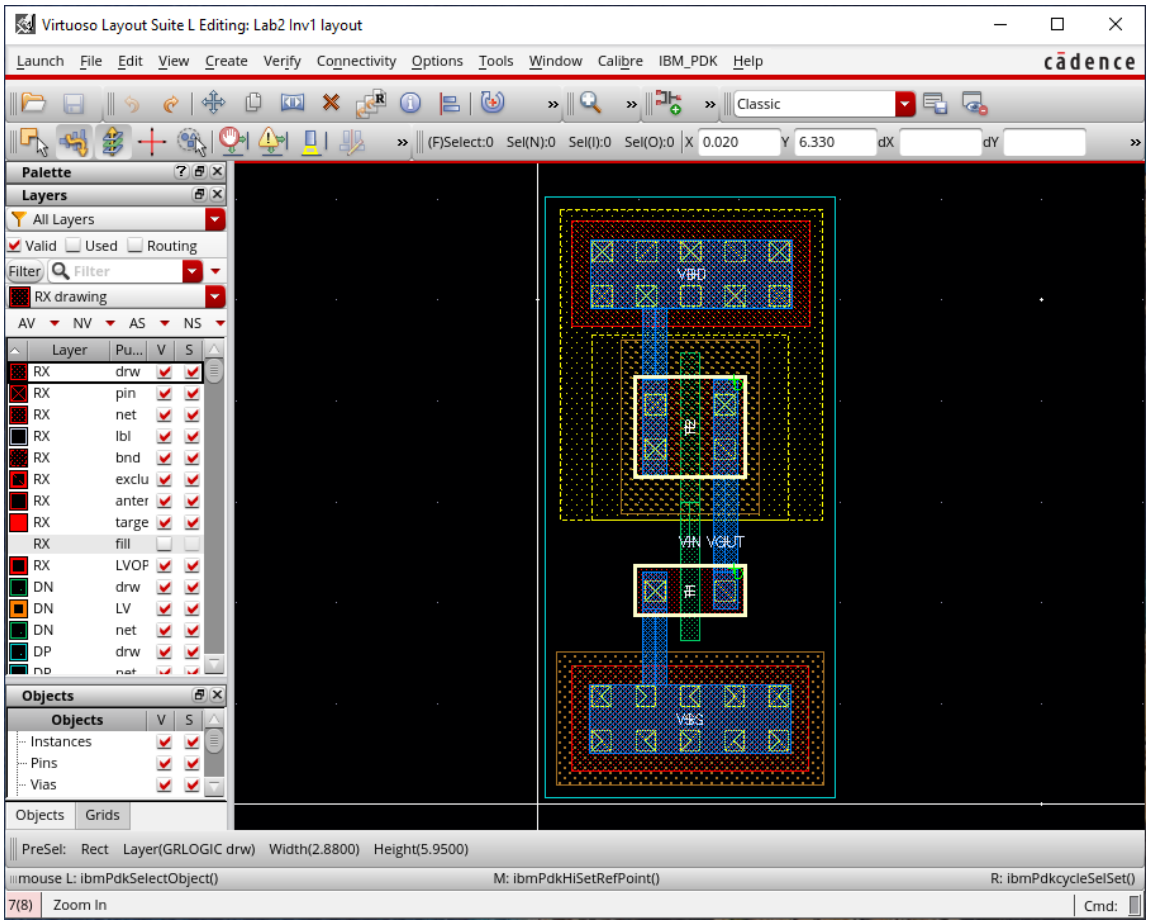

Figure 2-9: Inverter Layout

The last step to completing our layout is to add labels for the pins. Go to *Create* → *Label* → *<give the pin the same name as the one in the schematic>* → *<select the "Select Layer" option under the label layer/purpose field and adjust it accordingly>*. Alternatively, use the Shift-L hotkey to open the label editor. For VDD, VSS and VOUT the field "label layer/purpose" needs to be "M1 label", and for VIN it needs to be "PC label". When the process is complete the layout should resemble Figure 2-9. Be sure that the GRLOGIC layer surrounds everything including the letters on the labels.

A summary of common hotkeys for the layout editor is provided in Table 1-1. The options menu for a tool can be quite useful and provides additional options for various tools, and this menu can be brought up, if applicable, using the F3 key as mentioned in Table 1-1. As examples, some of these options include more precise movements to align objects (for the move and stretch tools) as well as allowing the creation of multiple copies of instances (for the copy tool).

Table 1-1: Common Layout Editor Commands

I	Add instance
Q	Open Property Editor for an instance
delete	Delete anything that is selected or clicked
esc	Return the cursor to its normal state
R	Draw a rectangle in the currently selected layer
M	Move objects
S	Stretch objects (moves edges of rectangles or segments of paths; also acts like the move tool if an entire object is selected)
C	Copy objects
U	Undo
Shift-U	Redo
P	Create a path in the currently selected layer (double-click to end)
O	Create vias to join different layers together
F	Zoom fit
Shift-F	Display layout layers contained within layout instances
Ctrl-F	Hide layout layers within layout instances, only shows instance outlines
E	Open layout window display options
Shift-E	Open layout editor options
Shift-L	Create label(s)
K	Add a ruler
Shift-K	Delete all rulers
T	“Tap” tool that selects a layer from an object in the layout as the current layer when creating shapes
Ctrl-D	Deselect everything
Right-click and drag	Will zoom in on drawn region
Shift-R	Flip element across y-axis (while moving)
Ctrl-R	Flip element across x-axis (while moving)
F3	Open the options menu for the current tool being used

Design Rule Check (DRC)

DRCs should be run not just at the end of the layout construction, but during it as well. From the layout window select *Calibre* → *Run nmDRC*, then click on "Run DRC" in the next window (Figure 2-10) and wait for the RVE window (Figure 2-11) to pop up. Once the RVE window pops up you will see all the

checks given. There are too many to scroll through, so if you click the word "Filter" on the left side of the RVE window you may filter the checks and errors (change the filter to “show unresolved” to display only the violations). To have Cadence tell you where the error was detected, double click on the red number shown to the right after highlighting the error. Run DRC until no errors appear (with the exception of density violations, which do not need to be corrected unless you plan on physically manufacturing your layout on a chip).

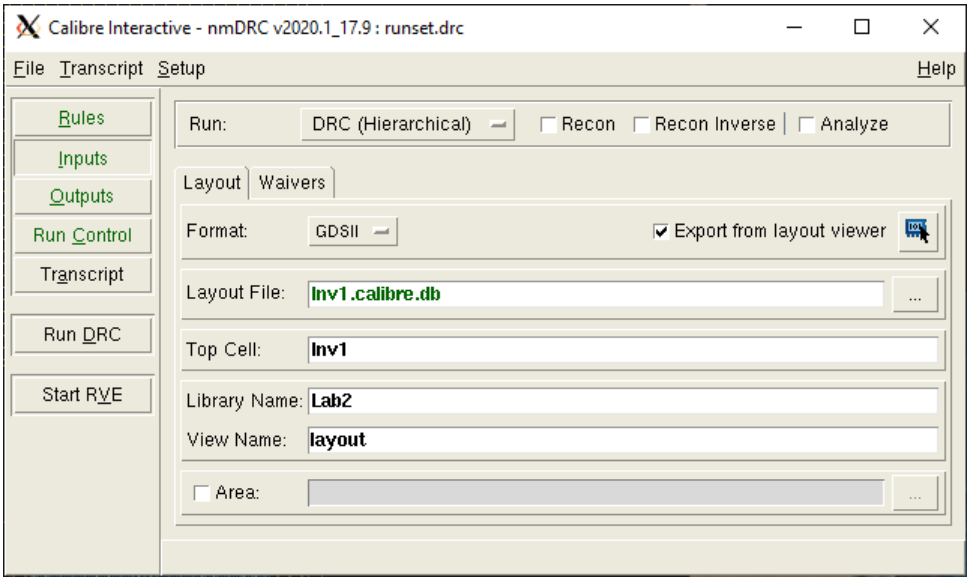

Figure 2-10: Calibre Interactive DRC Window

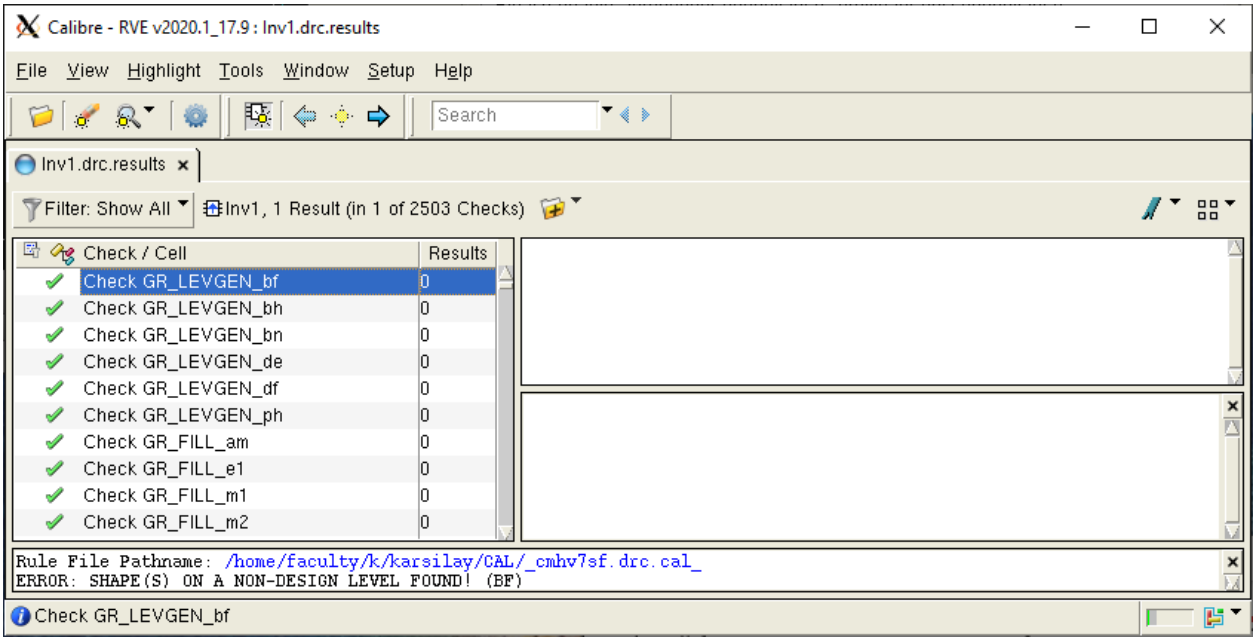

Figure 2-11: Calibre RVE Window Showing the DRC Results

Layout versus Schematic (LVS)

From the layout window, select Calibre → Run *nmLVS*. In the next window (Figure 2-12), click on "Run LVS". A new window or tab should appear which says "Calibre System LVS Report" at the top (it should appear similar to what is shown in Figure 2-13). You will need to take a screen capture of this window with your NetID and the time stamp included in the image. **No credit will be given if the LVS report is missing either the NetID or the time stamp.** Another window will also appear after running LVS which is the LVS RVE window, and this window will be used primarily for debugging any LVS errors which occur. If there are errors, open the "Comparison Results" tab in the RVE window after running LVS to get more information regarding the number and types of discrepancies. The discrepancies are grouped into various types, but different types of discrepancies can sometimes be related to the same errors in the layout. Therefore, it can be helpful to rerun LVS after any significant corrections to remove any discrepancies that are correlated to the same layout issue. Using the LVS RVE window as a guide, adjust the layout to match, and rerun DRC and LVS until the netlists match.

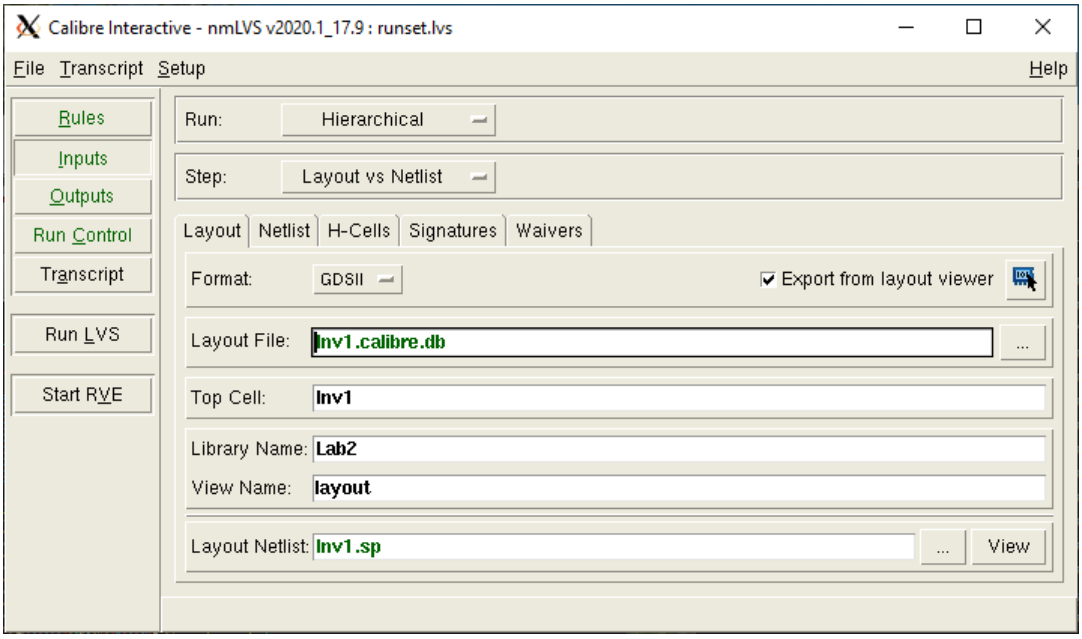

Figure 2-12: Calibre Interactive LVS Window

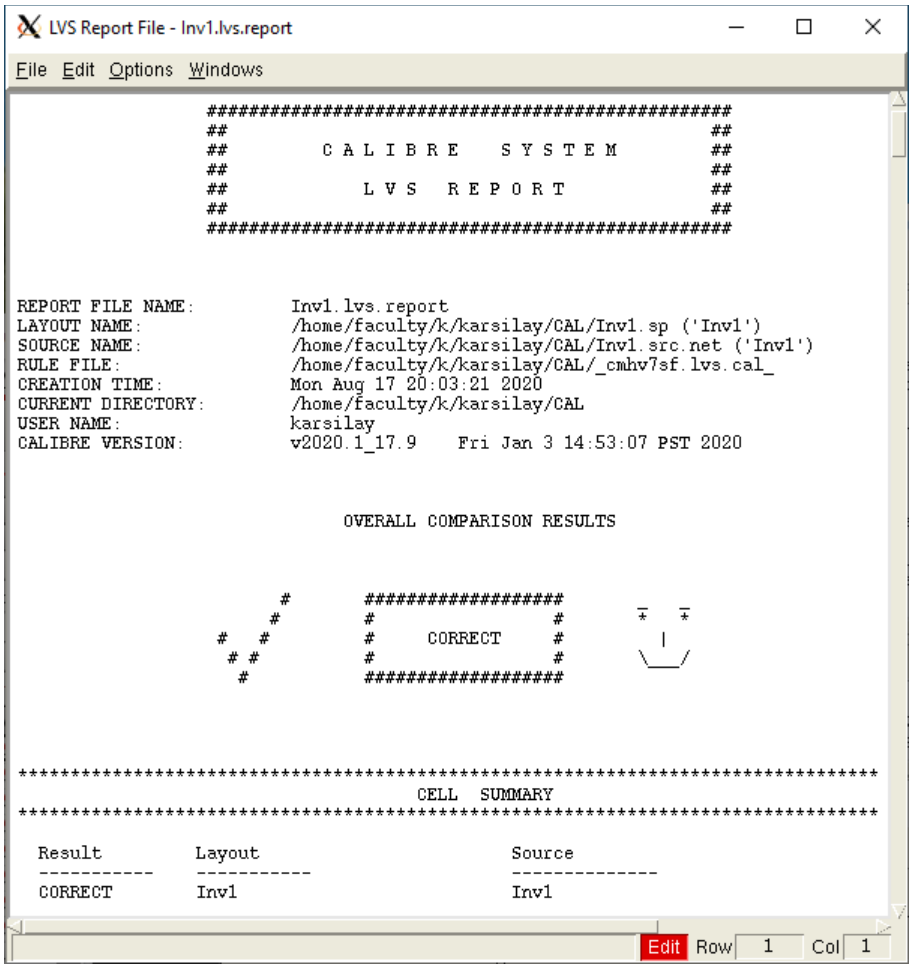

Figure 2-13: Calibre LVS Report Showing NetID and Time Stamp

Layout Versus Schematic (LVS) – Alternative Method

The alternative method described below will be needed for future labs utilizing capacitors or resistors from the process library. Note that this is specific to this process and may not be necessary when working with other PDKs.

From the schematic window, select *IBM_PDK* → *Netlist* → *Create CDL Netlist*. In the next window, type "~/LVS" for the "Run Directory", then click OK (see Figure 2-11). To confirm, you will receive "Analysis Job Succeeded" message. Next, select *IBM_PDK* → *Netlist* → *CDL pre_Process for LVS*. Change the "Run Directory" to "~/LVS" and click on "Refresh File List", then click to highlight the "Inv1.netlist" file and click the "<<" button to move it from the right column to the left column (Figure 2-14). Finally, click OK and the file "Inv1.netlist.lvs" will be generated.

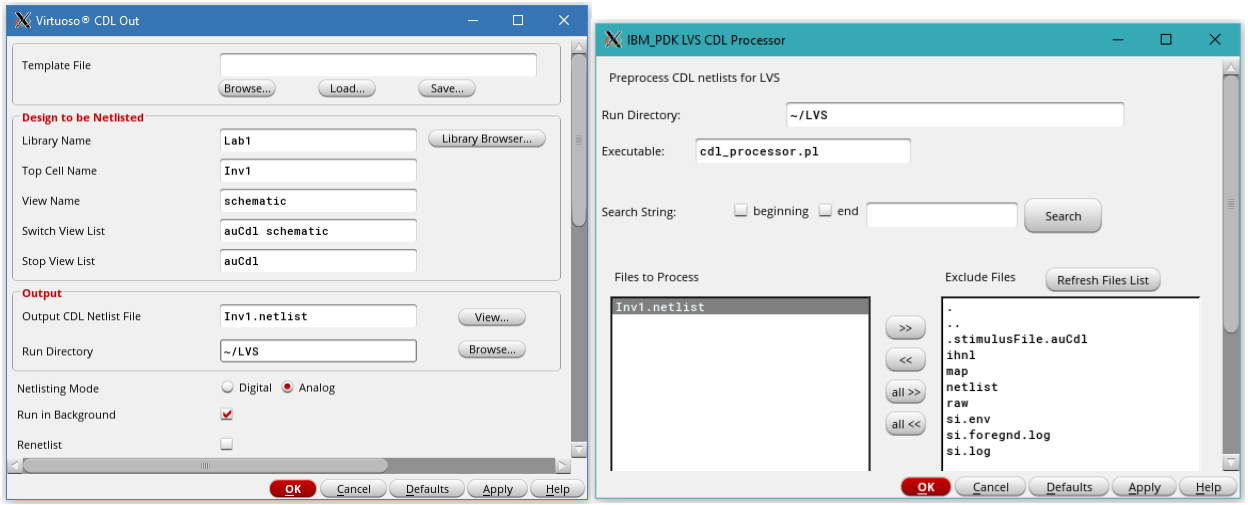

Figure 2-14: Netlist Generation from Schematic for LVS

Go back to the layout window and select *Calibre* → *Run LVS*. In the Calibre LVS window (Figure 2-15) click on the "Inputs" tab on the left side, then click on the "Netlist" tab. **Make sure the "Export from schematic viewer" box has been unchecked**. Next, find the "Inv1.netlist.lvs" file in "~/LVS" directory after clicking on the "..." button, then click on "Run LVS".

As described previously for the standard LVS method, you should see a Calibre LVS report (like in Figure 2-16) and you need to take a screenshot of this report. **No credit will be given if the LVS report is missing either the NetID or the time stamp.** If there are errors, open the "Comparison Results" tab in the LVS RVE window after running LVS to get more information regarding the number and types of discrepancies. As stated in the previous section on LVS, the errors will be grouped into various types, and multiple errors may be caused by the same issue in the layout. Therefore, it is recommended to rerun LVS after any significant corrections to remove any discrepancies that are correlated to the same layout issue. Using the LVS RVE window as a guide, adjust the layout to match, and rerun DRC and LVS until the netlists match.

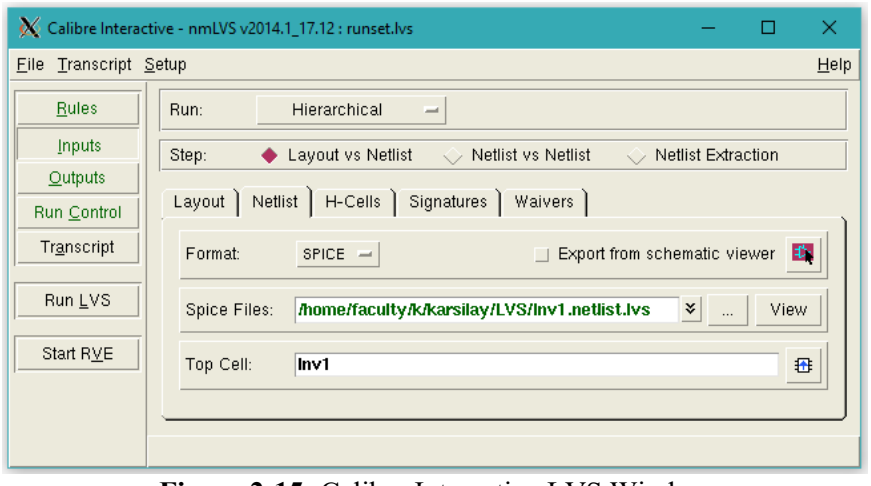

Figure 2-15: Calibre Interactive LVS Window

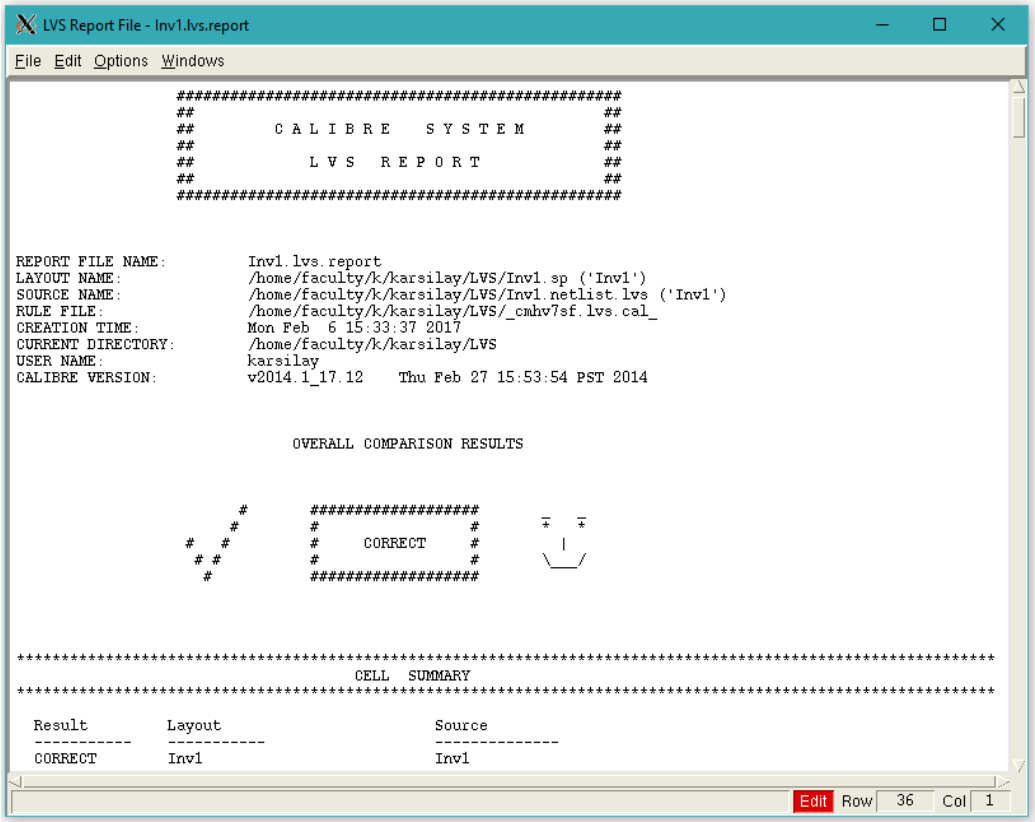

Figure 2-16: Calibre LVS Report Showing NetID and Time Stamp

Parasitic Extraction (PEX)

Once DRC and LVS are successful, you can now extract the layout for post-layout simulation using PEX. From the layout window select *Calibre* → *Run PEX*. In the Calibre interactive PEX window (Figure 2-17), click on "Run PEX".

In the middle of the extraction process, the Calibre View Setup window will pop up (Figure 2-18), just click OK to continue. PEX should run to completion, click "close" when the final window pops up with the number of errors and warnings.

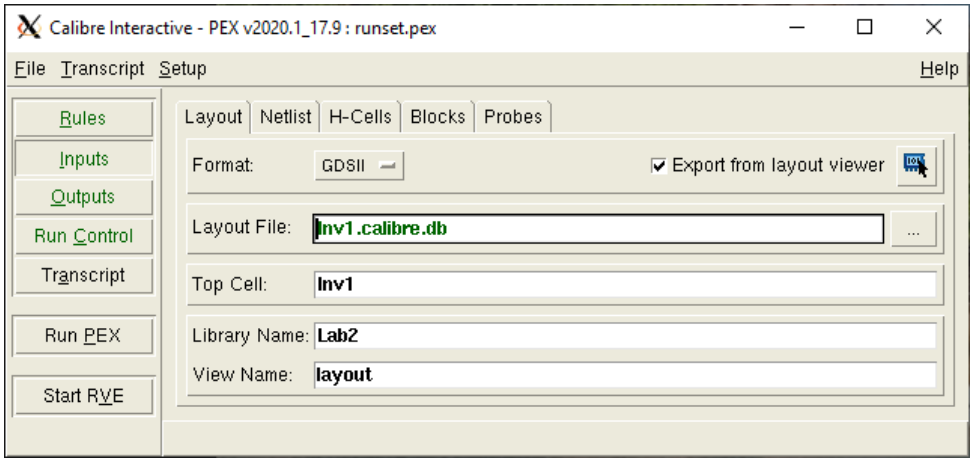

Figure 2-17: Calibre Interactive PEX Window

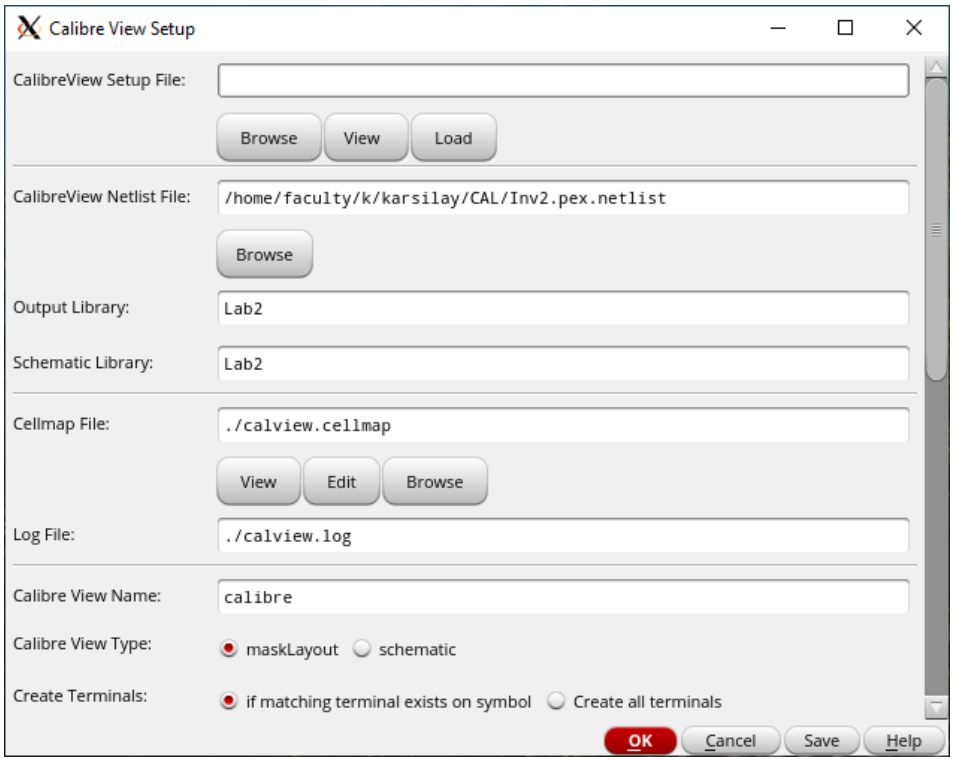

Figure 2-18: Calibre View Setup Window

Post-Layout Simulation

Using the same test bench (Figure 2-4), start the simulator by *Launch* → *ADE L*. With the default setup, simulation will use the schematic (ideal components) instead of the layout (components with routing parasitics). To simulate the layout, go to *Setup* → *Environment* in the ADE L window and in the field labeled "Switch View List", add "calibre" between "cmos.sch" and "schematic" (see Figure 2-19), then click OK. Now, if you run the simulation, the extracted netlist from the layout will be used. If the "calibre" view of the cell is deleted or the Switch View List is modified back to its original, "schematic" view can still be used for simulation.

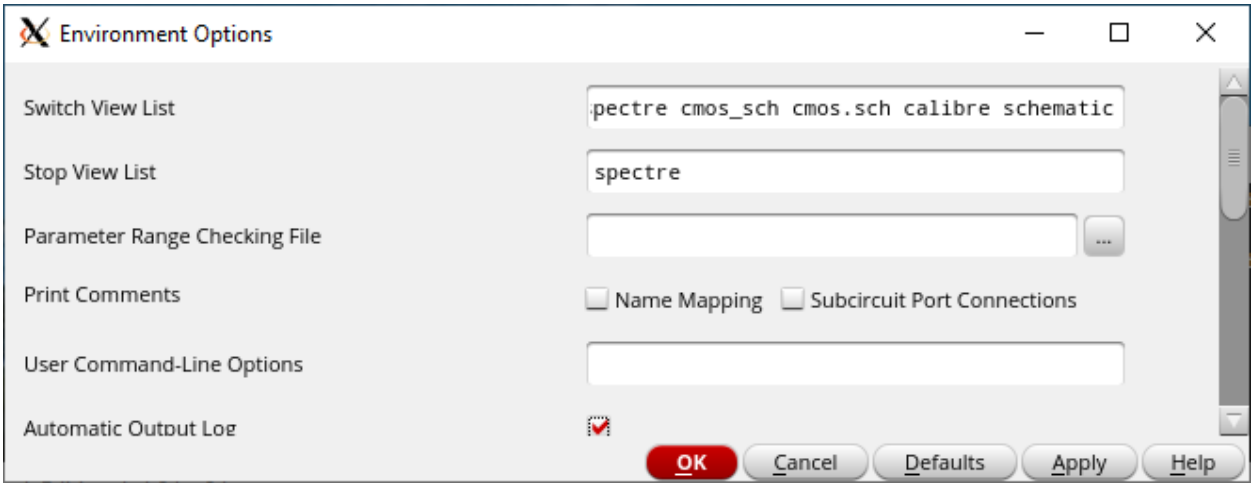

Figure 2-19: Switch View List in Environment Options

In order to make the differences easier to see between the pre- and post-layout simulations, the results from both simulations can be plotted in the same window. Here is one method of doing this: first, plot the results from the pre-layout simulation. Then, before running the post-layout simulations, change the "Plotting Mode" near the bottom-right corner of the ADE L window to "Append." This will add the plots from the new simulation to the existing window with the previous results. As an alternative method, the plotting mode option can be changed to "New Window" to plot results from a new simulation in a separate tab of the waveform viewer window. Then the results from either simulation can be copied from one tab to another by right-clicking on the desired traces and selecting "copy" and then pasting the results into the desired window. Make sure that the pre- and post-layout simulation traces use different colors. The trace color can be changed from the right-click menu associated with a trace in order to make the differences between the simulations more visible.

Lab Report

Turn in printouts of the following as a lab report:

1. Inverter schematic
2. Inverter symbol
3. Schematic test bench
4. Transient simulation output plot showing VOUT and VIN
5. Inverter layout
6. Screenshot of the DRC RVE window with results filtered to "show unresolved"
7. Copy of the LVS output file showing that the netlists match
   (needs to include your NetID and a time stamp in the screen capture)
8. Plot of the post-layout simulation (display post-layout simulation results in a single window with the pre-layout simulation results as well to make differences between the two more visible).
9. Discussion