ECEN 704 VLSI Circuit Design Project

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■ 1. Introduction

Design a Fully Differential Folded Cascode Amplifier (FDFC) with common mode feedback (CMFB) and a wide-swing current mirror bias circuit, adhering to the following design specifications.

DESIGN SPECIFICATIONS

Technology	**IBM180nmCMOS**		
	Specification	***Value***	***loop***
VDD	Supply voltage	1.8v	
VCM	Common-modelevel	0.9v	
Power	Power dissipation	≤3mW	Open
Gain	DCgain	≥60dB	Open
GBW	Gain Band Width	≥120MHz	Open
SR	Slew rate	≥75V/μs	Open
Noise	Input-referred noise (1Hz-100MHz)	≤ 50μVrms	Open
PM	Differential phase margin	≥60◦	Close
CMFB PM	CMFB phase margin	≥60◦	Close
IM3	IM3(1Vpp@1MHz)	≤−60dB	Close
Area	Chip area (including pads)	1mm×1mm	

■ 2. Design Procedure

2-1 Circuit Topology

A fully differential folded cascode amplifier offers better phase margin and output swing, while a Miller OPA is preferable if need a very high gain. Also, fully differential folded cascode amplifier can omit extra capacitors and also reduces design area.

2-2 Design Calculations

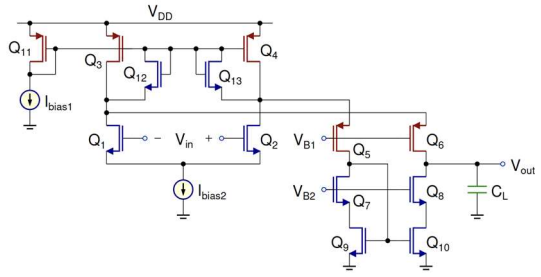


Figure 1

- To achieve the Power dissipation ≤3mW we can know that 1.8v*I ≤3mW, I-all ≤1.66mA
- For the SR we can first decide the current over the Q4 and Q5, I/CL (2.5p) ≥75V/μs, I ≥187.5mA. Choosing 250uA for Q4, 150uA for Q2, 100uA for Q5 Q7 Q9, 300uA for Ibais2
- Next, we can determine the W/L of the transistors by using the gm/Id method, transconductance efficiency, provides a measure of how efficiently a transistor converts a given current (Id) into transconductance (gm). (reference 1)

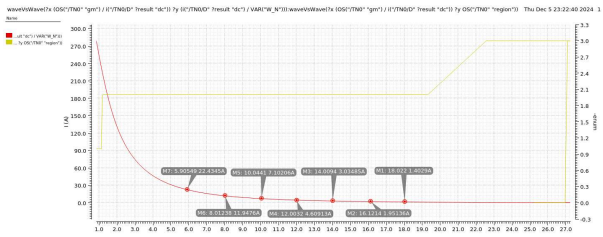


Figure (2-1) NMOS Id/W | gm/id

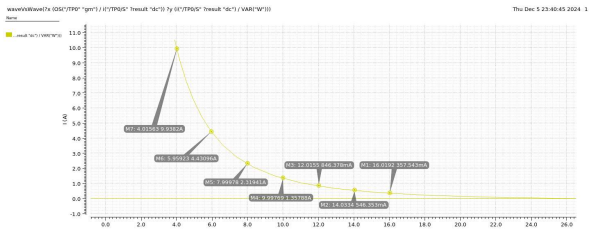


Figure (2-2) PMOS Id/W | gm/id

- To achieve the DC gain we choose L=500n to lower λ, higher rds.
- We require a higher transconductance (gm) for the first amplifier, Q2 NMOS, for

reduced noise and a gain-bandwidth product (GBW) of at least 120 MHz, which is defined by the condition gm/2 π CL $\geq$ 120 MHz and gm $\geq$ 1.884 m. This implies that gm/id (150 µA) must be at least 13. For our design, we select gm = 2.7 m under a bias current of I = 150 µA, resulting in an x-axis gm/id of 18, a y-axis Id/W of 1.4, and a width (W) of 80.

For the other transistors, after determining the current for each transistor, we selected an NMOS with a gm/id ratio of 8 and a PMOS with a gm/id ratio of 4 to achieve lower power consumption.

3. SCHEMATICS AND SIMULATION RESULTS

3-1 Design Schematics and Descriptions

The complete schematic consists of three components: the bias circuit, the fully differential pair, and the common mode feedback. (Figure 3)

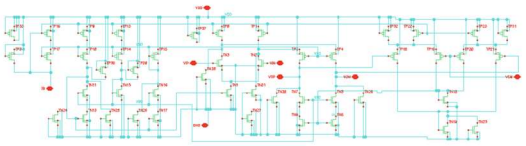


Fig 3. Full schematic

Using a PMOS wide-swing cascode current mirror in series with an NMOS wide-swing cascode current mirror, along with several dummy transistors for the bias circuit (see Figure 3-1).

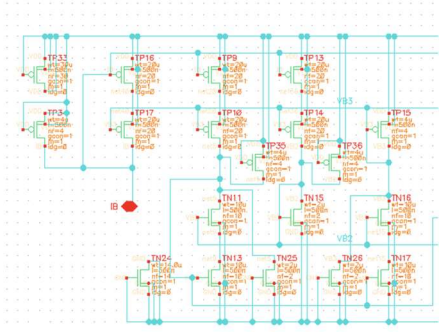


Figure 3-1

The Fully Differential Folded Cascode Amplifier (FDFC), as shown in Figure 3-2, is biased using the bias circuit.

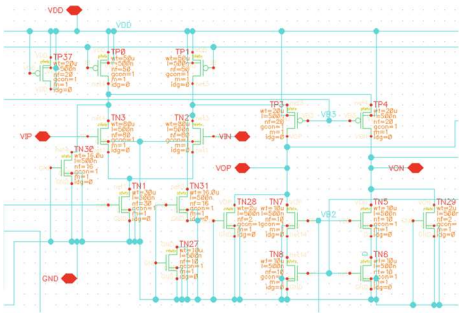


Figure 3-2

For the CMFB, decide 50uA on each side for the lower power dissipation. (Figure 3-3)

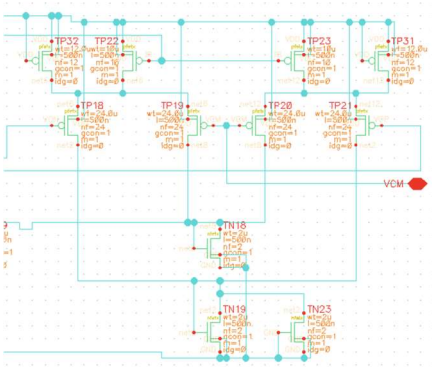


Figure 3-3

3-2 Simulation Results

Using ideal balun and some Vdc, Vsin to create open and close loop testbench

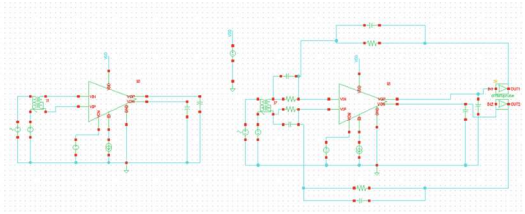


Figure 4 testbench

Checking dc voltage = 0.9V is in the common-mode range **(0.792~1.8)** that keep all transistors in active

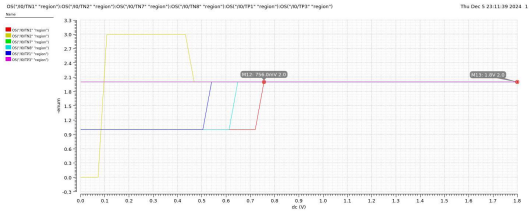
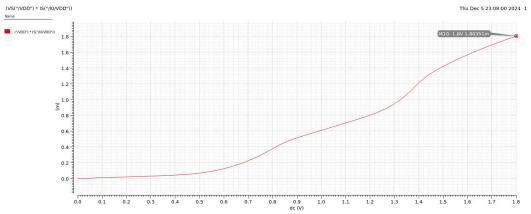


Figure 5 Common-mode range

The Power dissipation is **1.8035mW**



DC gain (**59.3208dB**) & GBW (**128.893MHz**) on the 0dB point (figure 5-2)

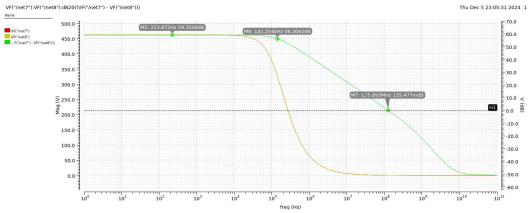


Figure 5-2 DC gain & GBW

Input-referred noise (1Hz-100MHz) =**52.7258u** (Figure 5-3)

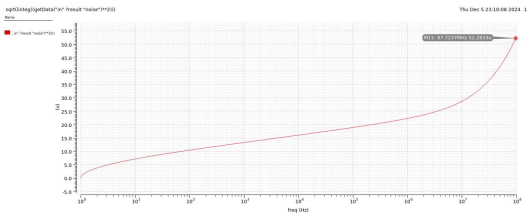


Figure 5-3 Input-referred noise

Slew rate = **82.89 V/μs** (figure 5-4)

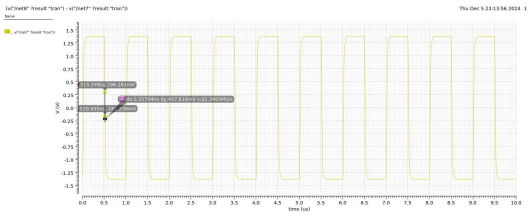


Figure 5-4 SR

Phase margin = 180 ◦ - the 0dB point PM (85.91 ◦) = **94.09** ◦ (Figure 5-5)

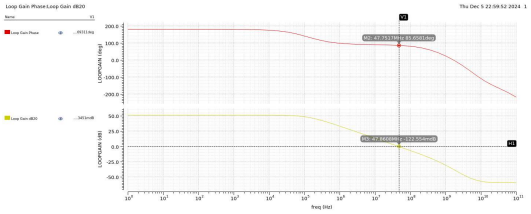


Figure 5-5 PM

Phase margin for the CMFB = 180 ◦ - the 0dB point PM (72.23 ◦) = **107.77** ◦ (Figure 5-6)

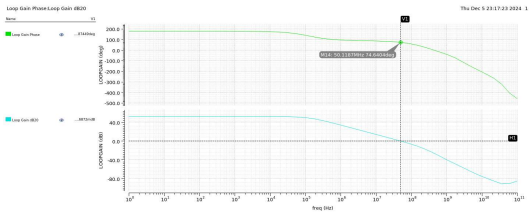


Figure 5-6 CMFB PM

0.9M(-44dB)-1M(-12dB) =**-32dB** (figure 5-7)

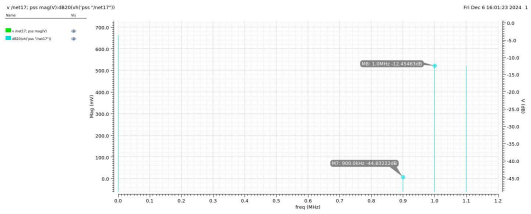
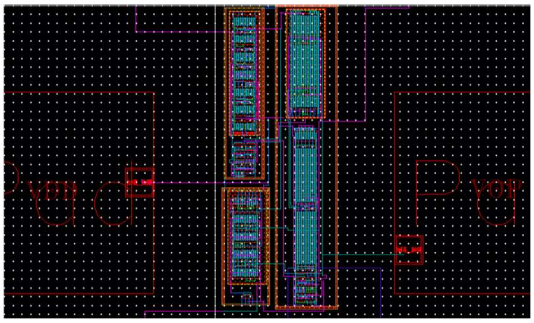


Figure 5-7 IM3

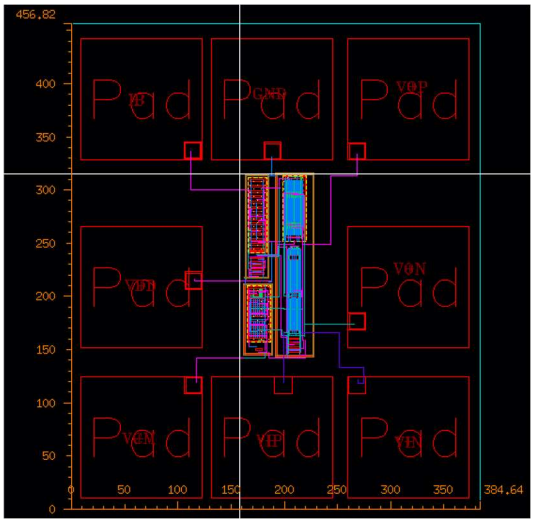
■ 4. CHIP LAYOUT

4-1 Layout Blocks

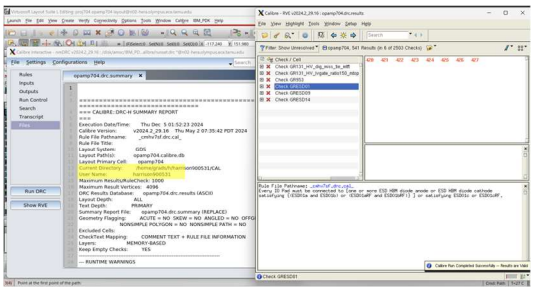


4-2 Complete Chip

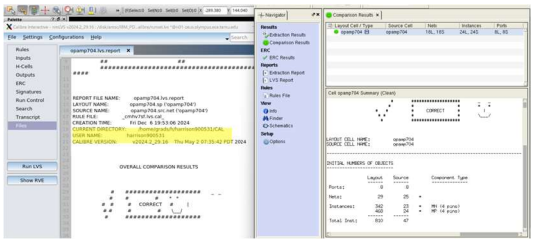
Chip area: **0.45u*0.38u**



4-3 DRC (with some antenna and ESD errors)

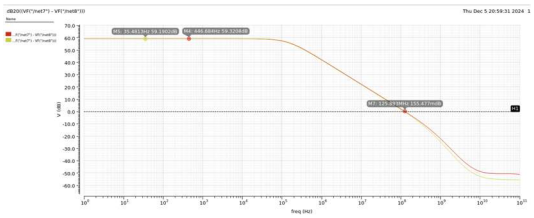


4-4 LVS

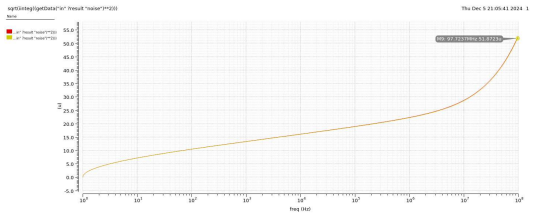


■ 5. Post layout simulation

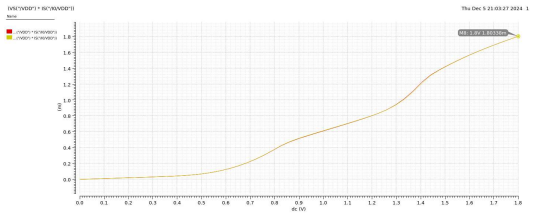
Post layout DC gain **(59.19dB)** & GBW **(121.108MHz)**



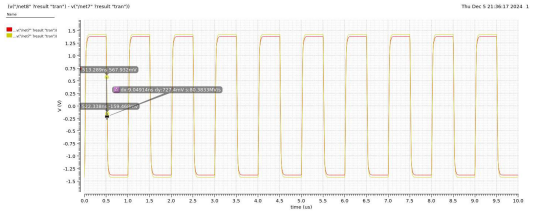
Post layout noise = **51.8u**



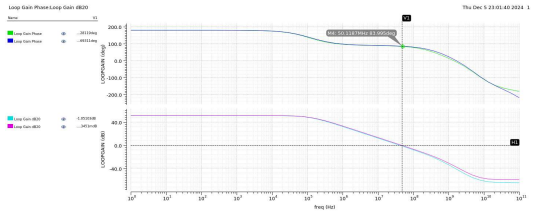
Power post layout =**1.8mW**



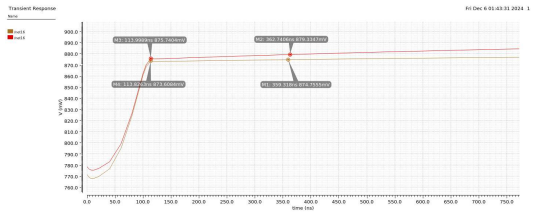
SR post layout = **79.7V/us**



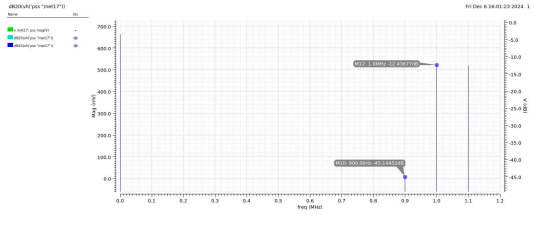
PM post layout= 180-84.6= **95.4**



Comparing CMFB phase margin by ringing in the step response which related to the phase margin.



IM3 (-45) -(-12) = **-33dB**



■ 6. Conclusion

	specifications	Post layout
DC gain	≥60dB	59.19dB
GBW	≥120MHz	121.108MHz
Noise	≤ 50μVrms	51.8u
Power	≤3mW	1.8mW
SR	≥75V/μs	79.7 V/μs
PM	≥60◦	95.4
IM3	≤−60dB	-33dB

The advantage of FDFC lies in its stability; however, having a large proportional gain (PM) can result in a slow system response, which may pose issues in certain situations.

■ 7. Reference

[1] N. Bako1, Ž. Butkovi 2 and A. Bari 2 1Systemcom Ltd., Zagreb, Croatia- Design of Fully Differential Folded Cascode Operational Amplifier by the gm/ID Methodology https://www.edaboard.com/attachments/05533393-pdf.50616/