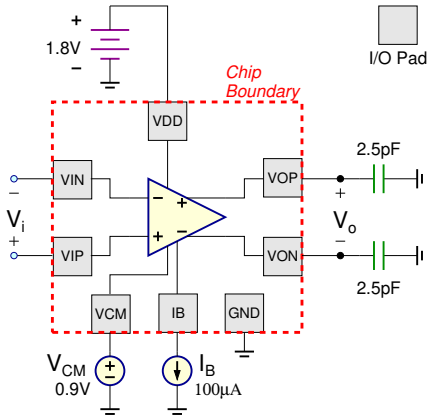
ECEN 704 PROJECT

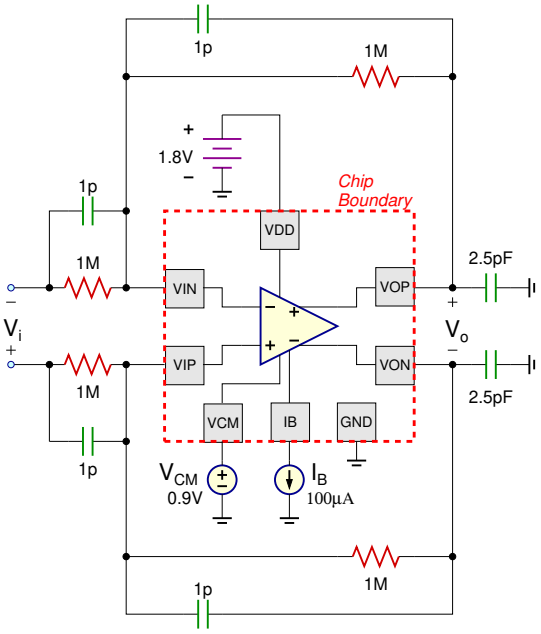
Due date: Friday, December 6, 2024

Design a chip for a fully-differential amplifier (including the common-mode feedback circuit) with the following post-layout specifications:

Technology	IBM 180nm CMOS	
Chip area (including pads)	1mm×1mm	
Supply voltage	1.8V	
Common-mode level (V_{CM})	0.9V	
Power dissipation	$\leq$ 3mW	Open-loop
DC gain	$\geq$ 60 dB	Open-loop
GBW	$\geq$ 120 MHz	Open-loop
Slew rate	$\geq 75V/\mu s$	Open-loop
Input-referred noise (1Hz-100MHz)	$\leq 50\mu V_{rms}$	Open-loop
IM3 (1V$_{pp}$@1MHz)	≤ -60 dB	Closed-loop
Differential phase margin	$\geq 60°$	Closed-loop
CMFB phase margin	$\geq 60°$	Closed-loop



Open–loop



Closed–loop

Using the circuit configurations provided above, measurements can be performed following the guidelines below:

- For DC gain and GBW measurements, connect *vsin* (ac magnitude = 1), *vdc* (dc voltage = 0.9V) and *ideal_balun* from *analogLib* to the input V_i as in Lab 9, and run AC simulation.
- To measure slew rate, replace *vsin* with *vpulse* (-0.5 to 0.5V) at the input, and run transient analysis.
- Refer to Lab 9 for noise and IM3 measurements.

All components in the chip should be from *cmhv7sf* (only transistors, capacitors, and pads) or *proj704* libraries, use the following naming conventions:

Design library name	proj704
Top-level cellname	opamp704
I/O pins	VDD, GND, VIP, VIN, VOP, VON, VCM, IB

Project report should be typed based on the provided Word template, and should not exceed 4 pages. It should include the design procedure, calculations, schematics, simulation results, layout, verification results (DRC and LVS reports), post-layout simulations, and concluding remarks. Upload the report (searchable pdf format) and the compressed tar file of the design library (tar.gz format) on Canvas before the deadline. **Late submissions will not be accepted.** Turnitin score must be less than 20% for all reports, submissions with no Turnitin score will not be accepted.

You can use the following commands to create the compressed tar file of your design library:

```
> tar cvf UIN.tar proj704
> gzip UIN.tar
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