24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab9: Two stage OPA

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Section:601

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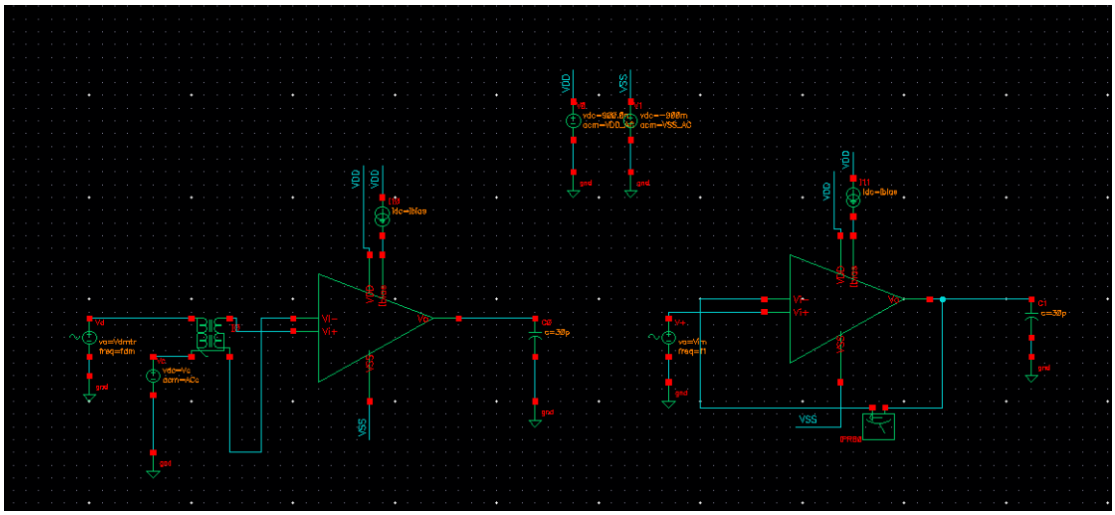
TA: Troy Buhr

Description:

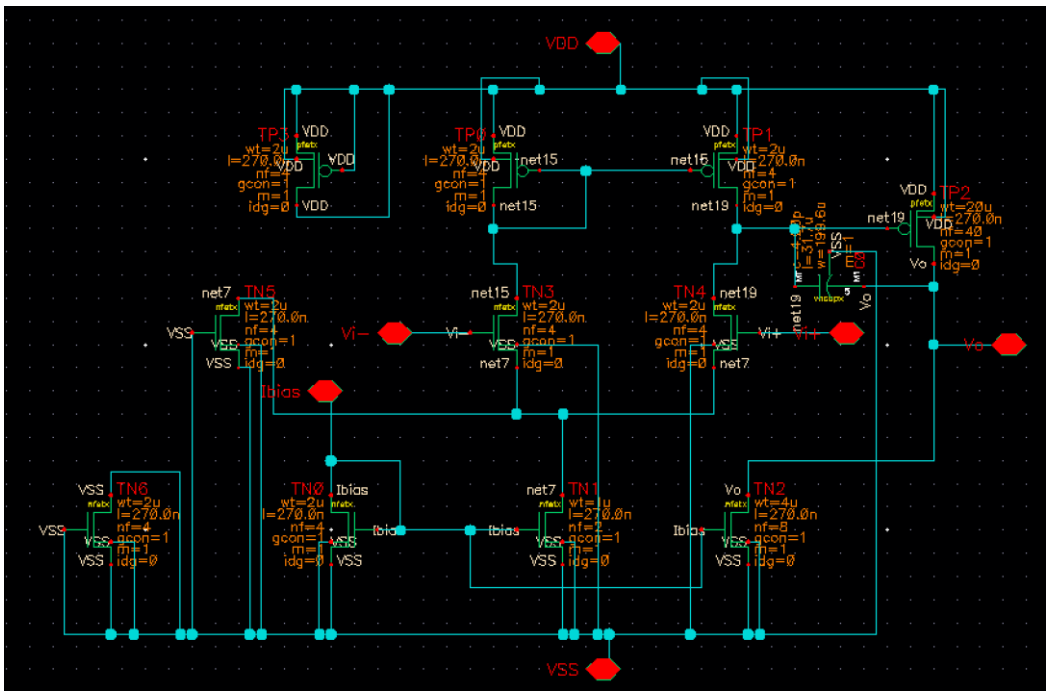
Operational amplifiers (op-amps) are fundamental to analog system design, widely used in both integrated circuit and board-level applications. With their high gain, op-amps play critical roles in systems like filters, regulators, and function generators. They also enable the creation of buffers, logarithmic amplifiers, instrumentation amplifiers, and can even serve as comparators. Understanding op-amp functionality and design is crucial for creating versatile and efficient analog circuits, making them an indispensable tool for engineers in the field.

Design & result

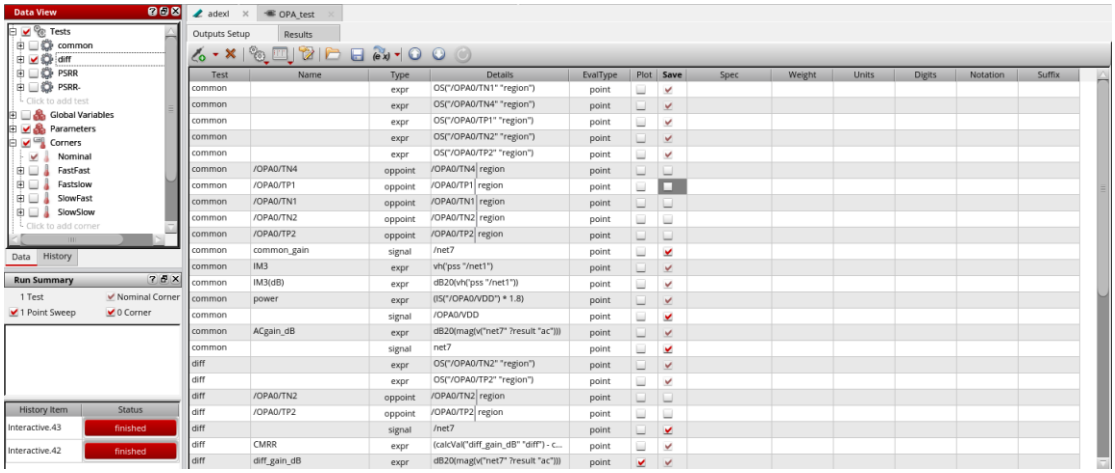
testbench



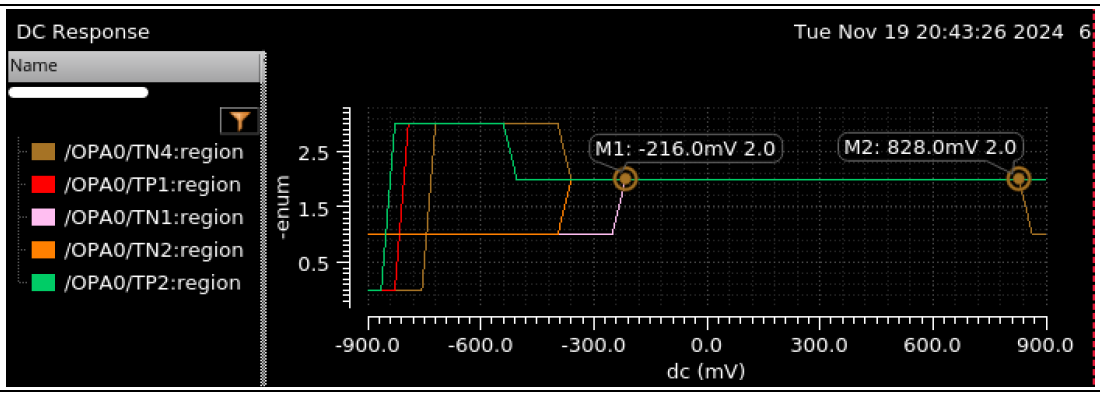
schematic



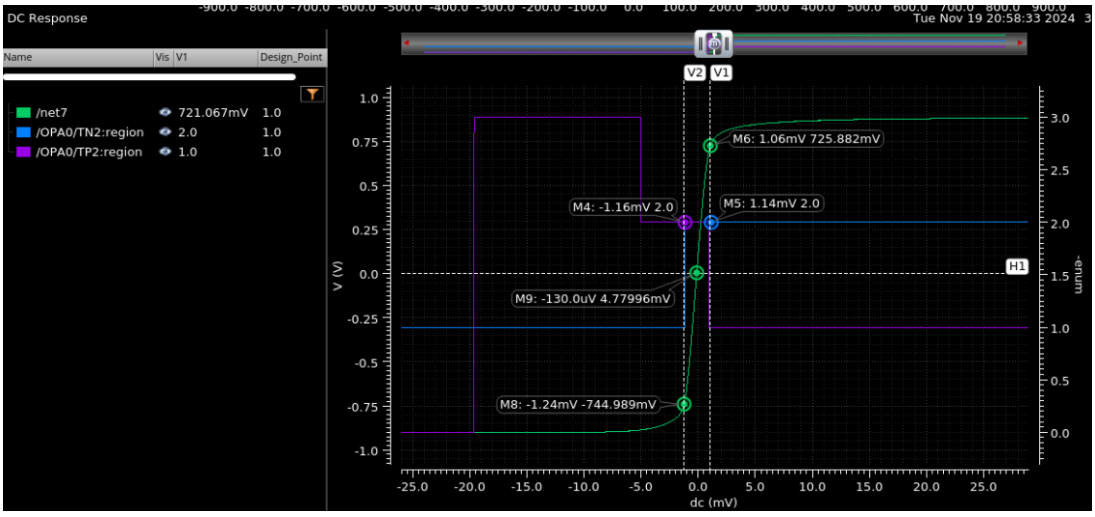
ADE XL



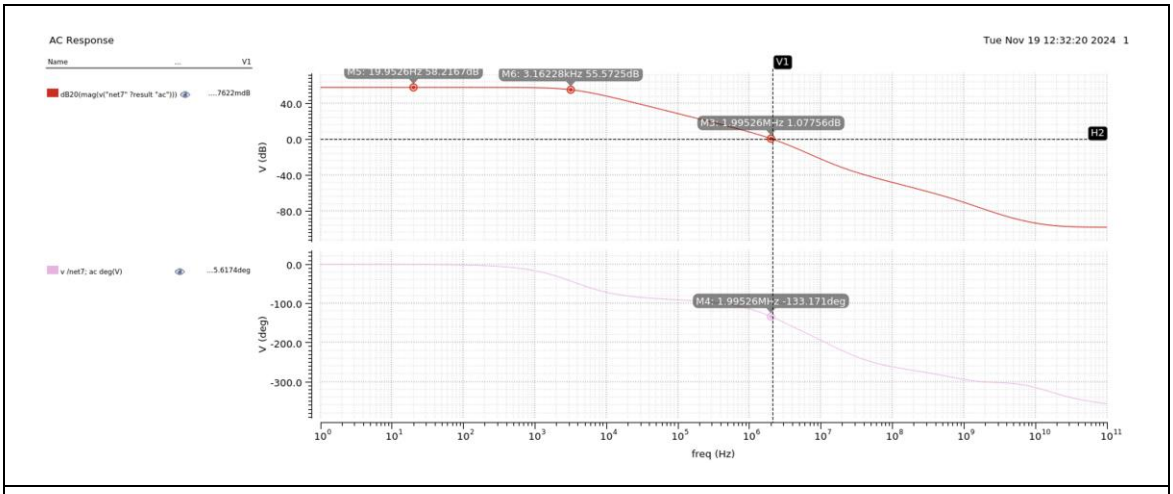
Common-mode DC operation offset point range



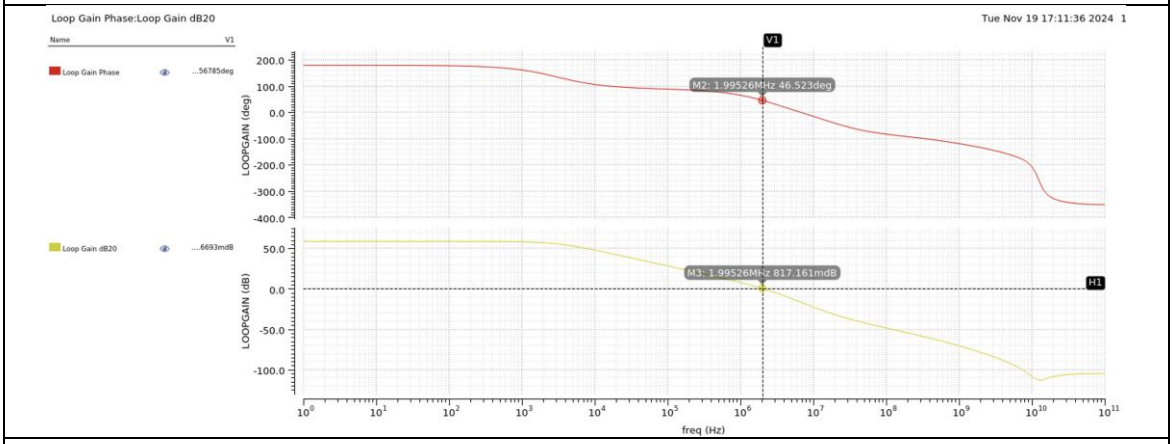
Different-mode range



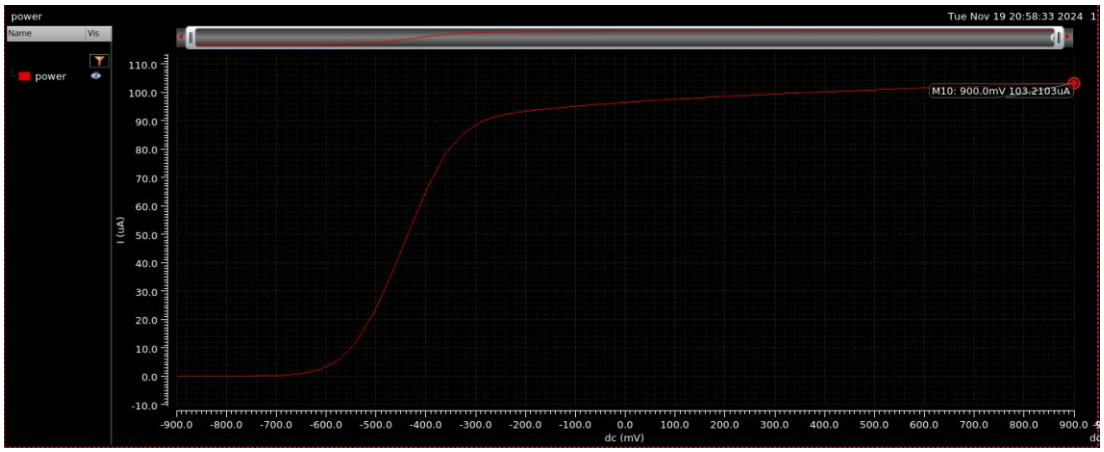
Open-loop Gain fp1 GBW PM



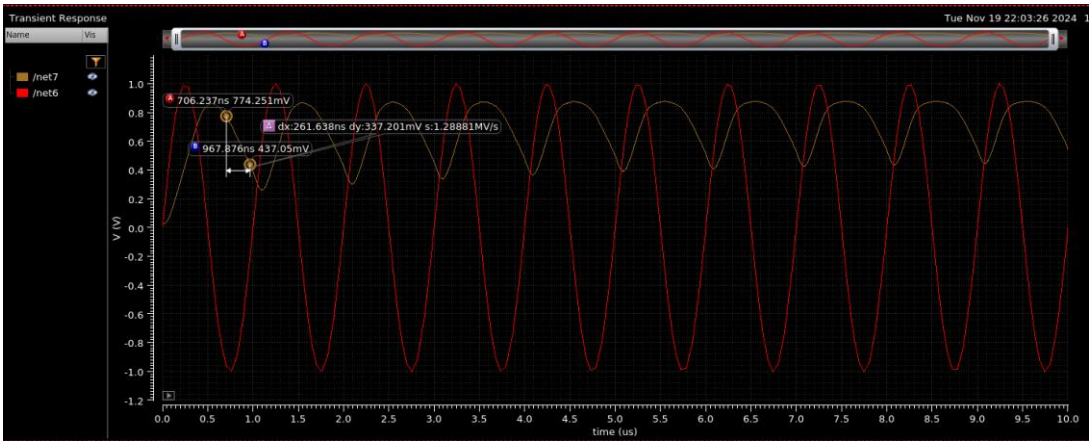
Loop-gain GBW PM

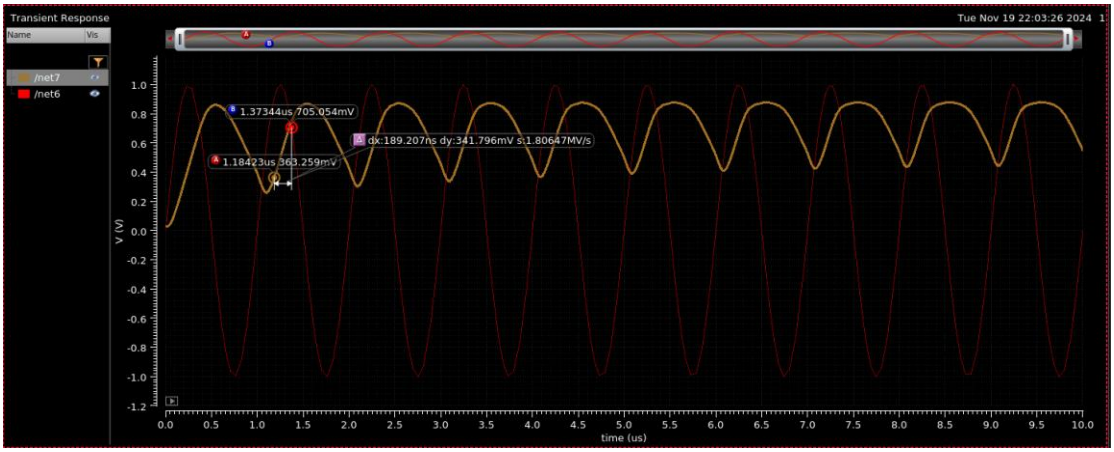


power

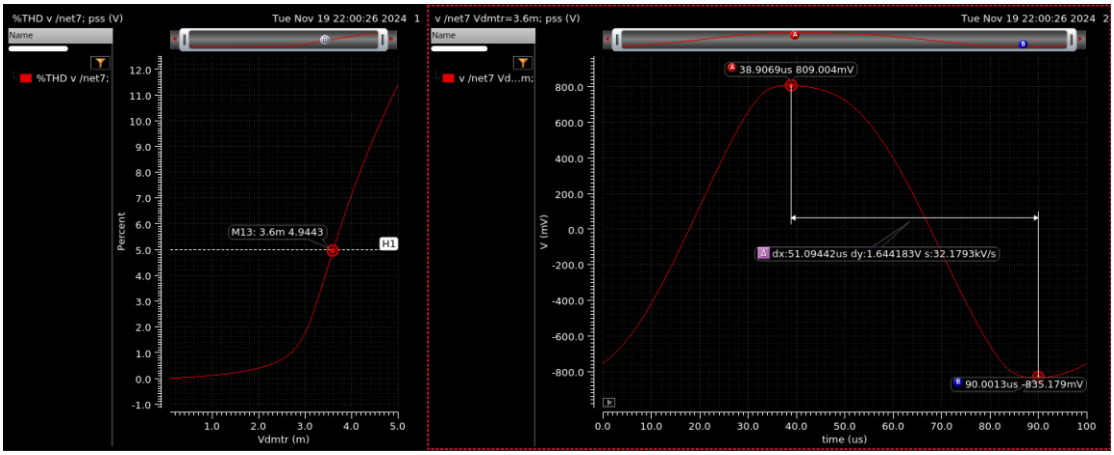


SR

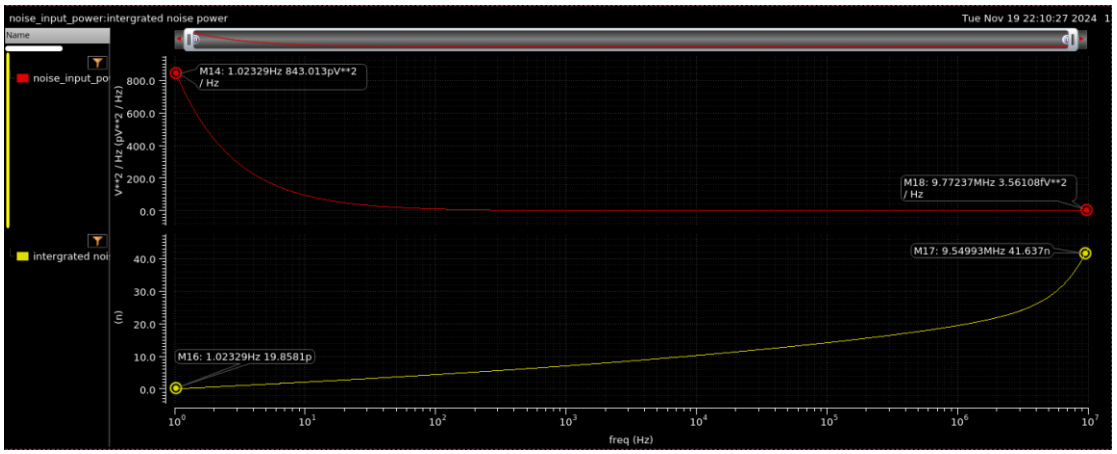




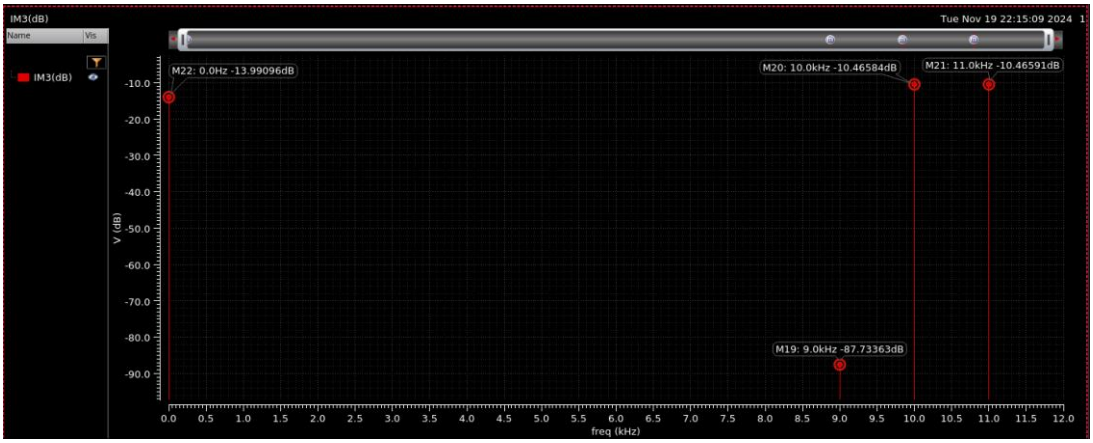
PSS output swing



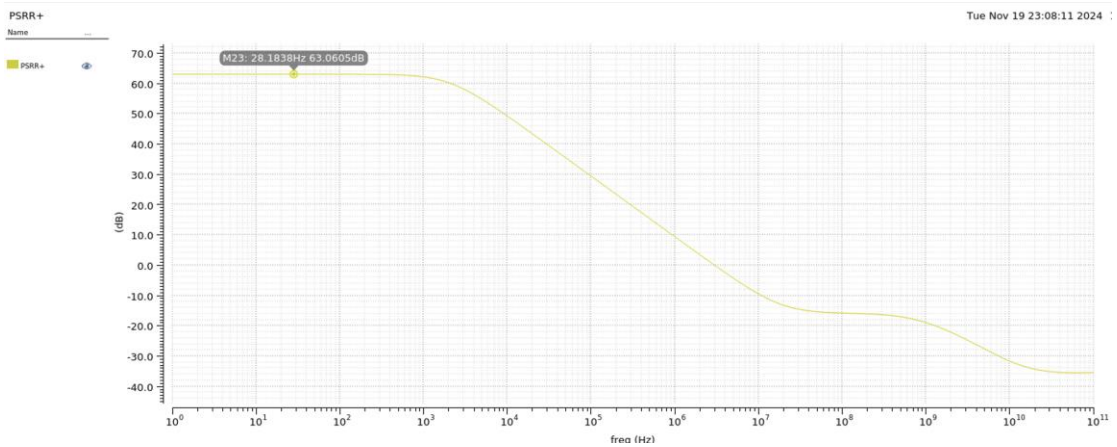
Noise



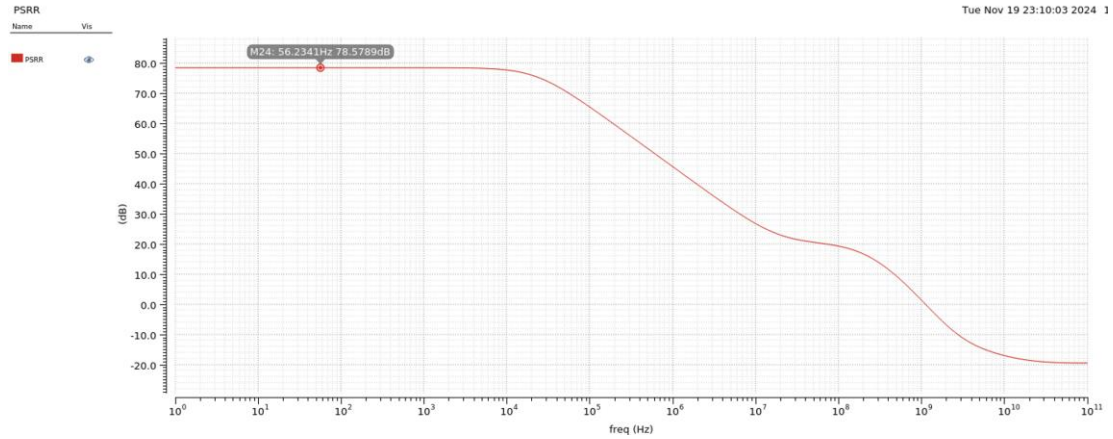
Third-order Intermodulation product (IM3)



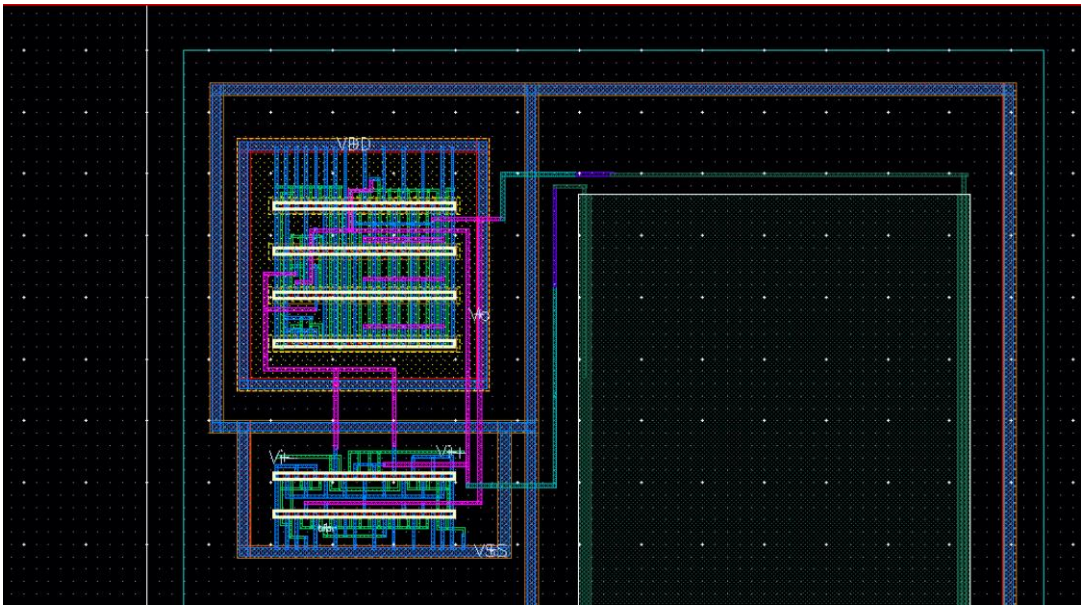
PSRR+



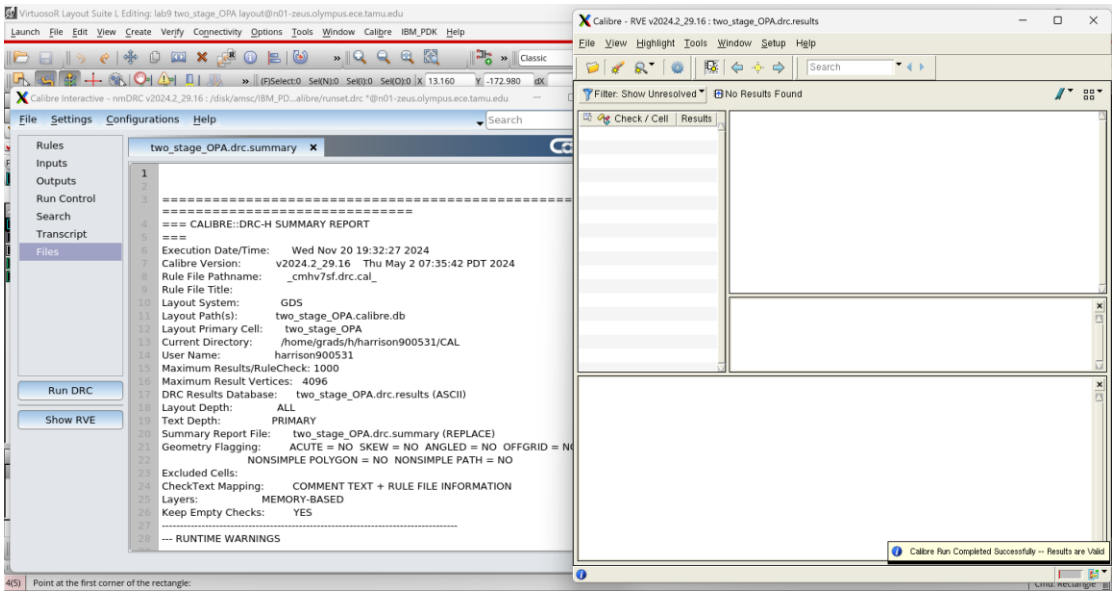
PSRR-


PSRR
Name
Vis
PSRR
Tue Nov 19 23:10:03 2024
M24: 56.2341Hz 78.5789dB
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
-10.0
-20.0
(dB)
freq (Hz)

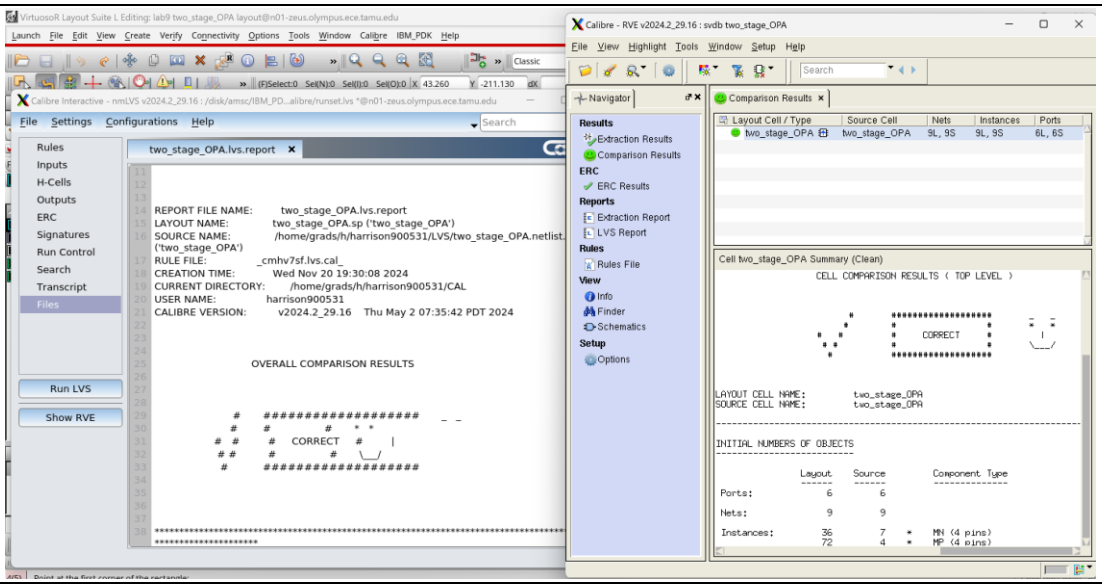
layout

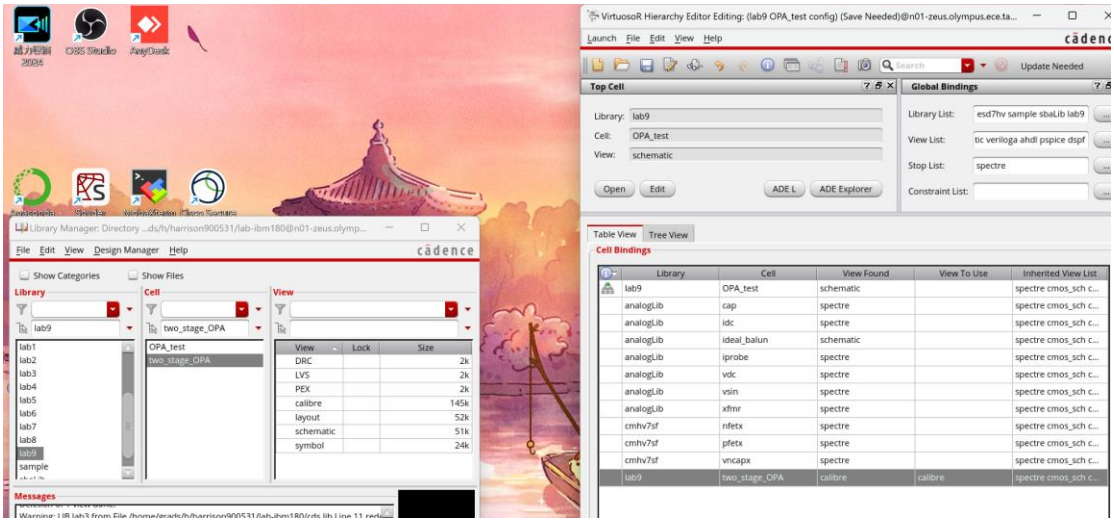

VDD
VSS

DRC

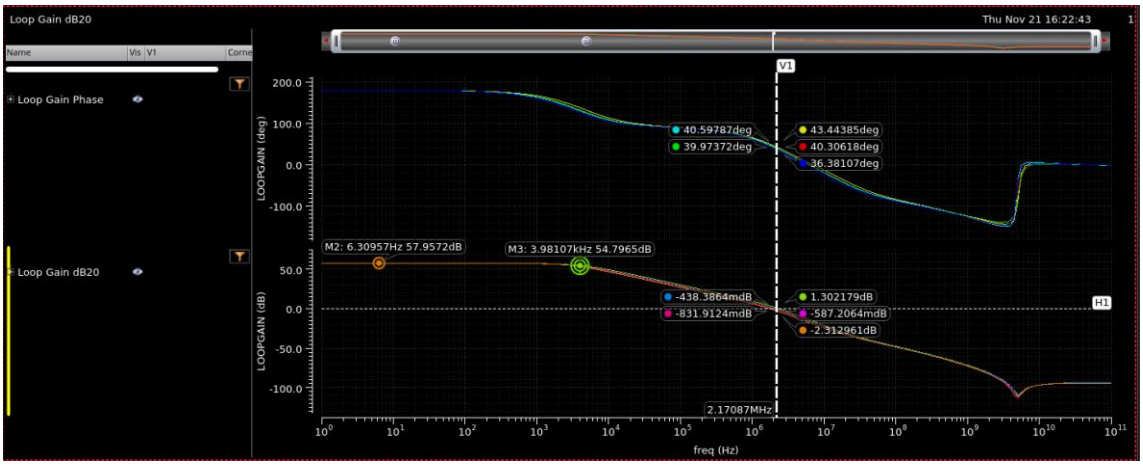

two_stage_OPA.drc.summary
=== CALIBRE::DRC-H SUMMARY REPORT
Execution Date/Time: Wed Nov 20 19:32:27 2024
Calibre Version: v2024.2_29.16 Thu May 2 07:35:42 PDT 2024
Rule File Pathname: _cmhv7sf.drc.cal_
Rule File Title:
Layout System: GDS
Layout Path(s): two_stage_OPA.calibre.db
Layout Primary Cell: two_stage_OPA
Current Directory: /home/grads/h/harrison900531/CAL
User Name: harrison900531
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: two_stage_OPA.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: two_stage_OPA.drc.summary (REPLACE)
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
Run DRC
Show RVE
Calibre Run Completed Successfully -- Results are Valid

LVS

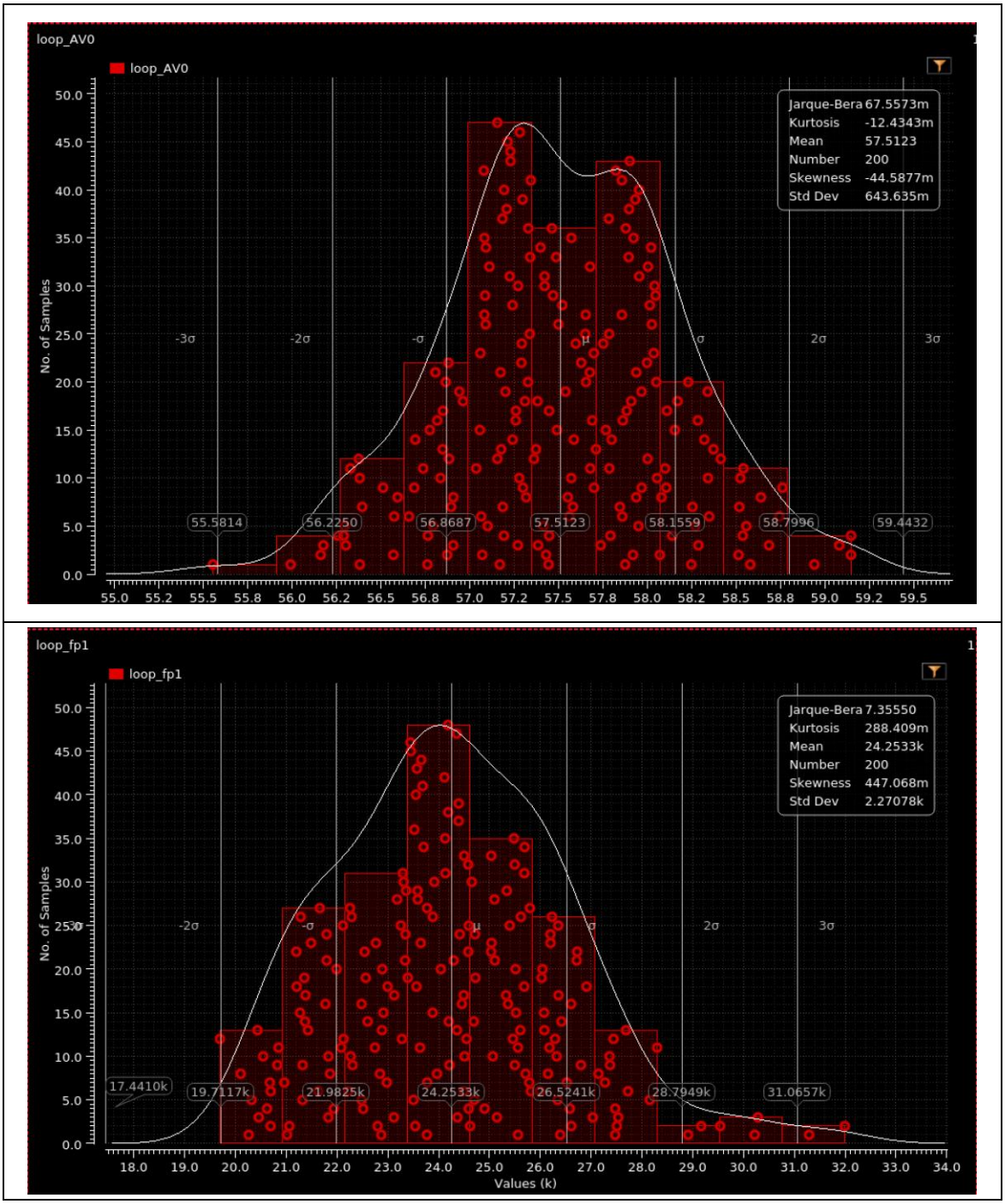


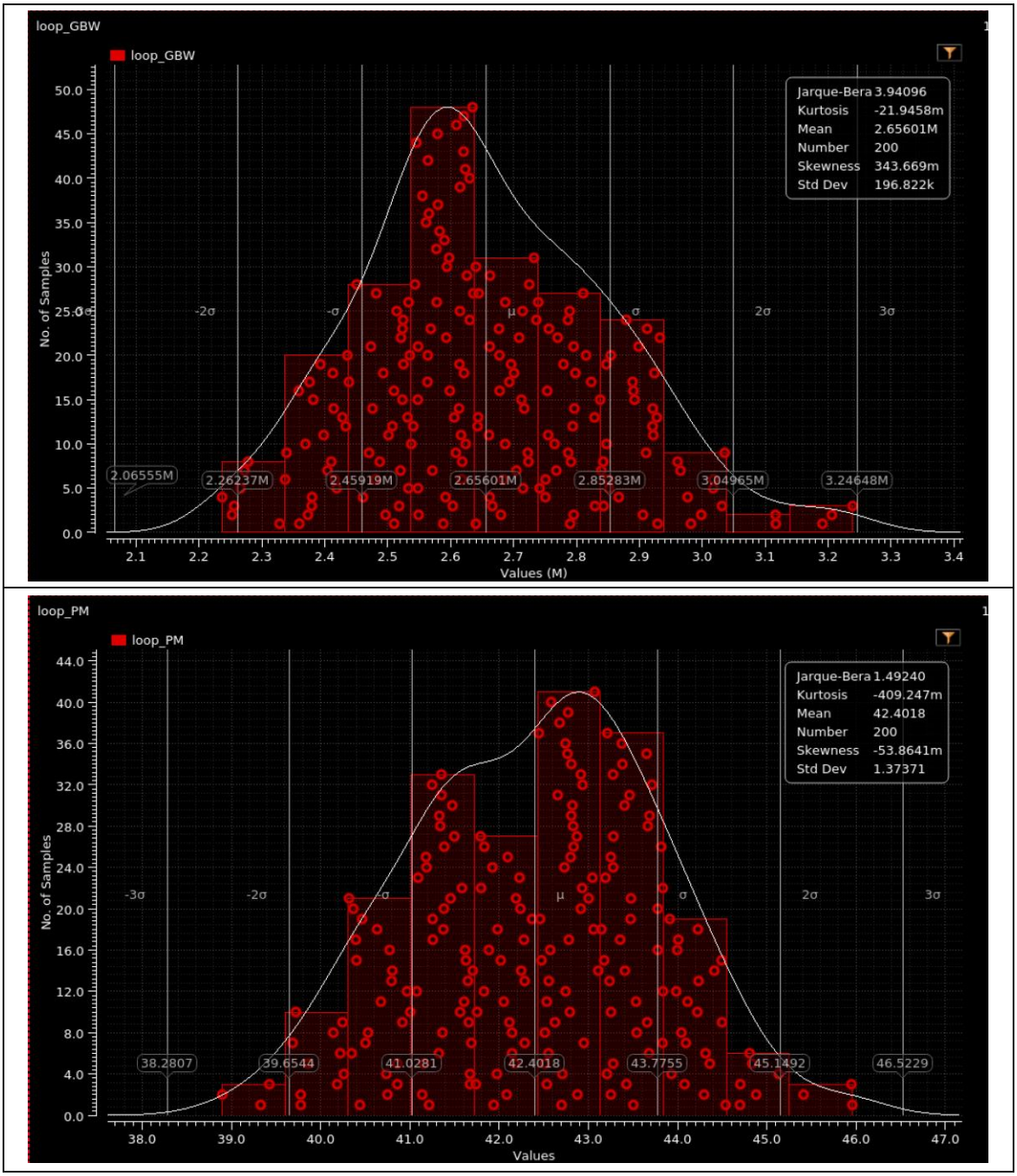


Corner (postlayout)



Monte


loop_AV0
loop_AV0
Jarque-Bera 67.5573m
Kurtosis -12.4343m
Mean 57.5123
Number 200
Skewness -44.5877m
Std Dev 643.635m
No. of Samples
-3σ
-2σ
-σ
μ
σ
2σ
3σ
55.5814
56.2250
56.8687
57.5123
58.1559
58.7996
59.4432
loop_fp1
loop_fp1
Jarque-Bera 7.35550
Kurtosis 288.409m
Mean 24.2533k
Number 200
Skewness 447.068m
Std Dev 2.27078k
No. of Samples
-2σ
-σ
μ
σ
2σ
3σ
17.4410k
19.7117k
21.9825k
24.2533k
26.5241k
28.7949k
31.0657k
Values (k)



Discussion:

I modified the M8 by increasing the W of it to get higher Av on the second stage also I think increasing the W will make the output swing larger because of the veff8=$\sqrt{\frac{I_{tail}}{KP_p\left(\frac{W}{L}\right)_{5,6}}}$ and increasing W means smaller veff for VDD-veff. Also increasing M1 and M2 will have the same effect for VCM.

When I plotted the Vd region for the output swing, I discovered that 0 is still within the region. Initially, I thought that 0 indicated VCM, which involves adding 0+ and 0- on the differential side, suggesting that only a DC voltage is applied. This would imply that the

output might resemble a DC offset point. However, according to the plot, there are still some signals (Vd) being amplified and added to the output side. I later consulted with TA, who explained that although Vd is 0, there are still some offset voltages present in the circuit. This means that it does not behave as if Vd = 0, which is why the output is not purely DC.

When I attempted to use the calcVal function to plot the Common-Mode Rejection Ratio (CMRR), I initially encountered difficulties because I was using the signal instead of the expression within the calcVal function. The correct approach is to utilize the expression within the calcVal to ensure the function operates correctly. To conduct the Monte Carlo simulation, I must first run the ADE XL to obtain at least one result for the random simulation.

In this lab, we got a large C on the output. I think when the Miller capacitor being split into two sides, the output node experiences a minor effect from the Miller capacitor while still having a large load capacitance (CL). This situation could cause the two poles to become close. One potential solution is to use a current mirror operational amplifier (OPA) to separate the two poles more effectively, or to add a resistor (R) with (Cc) and introduce a zero (Wz) to make phase margin better.

Conclusion:

After completing Lab 9, we have gained a deeper understanding of the functionality and versatility of operational amplifiers in analog system design. By exploring their applications in systems such as filters, regulators, and amplifiers, as well as their role as comparators, we have reinforced the importance of op-amps as essential components in both integrated circuits and board-level designs. We have learned many new methods for measurement, such as output swing, noise analysis, and various simulation techniques. All of these factors will be important when analyzing a circuit or working on the final project.