ECEN 474/704 Lab 8: Operational Transconductance Amplifiers

Introduction

The operational transconductance amplifier (OTA) is a basic building block of electronic systems. The function of a transconductor is to convert an input voltage to an output current. The transconductance amplifier can be configured to amplify or integrate either voltages or currents. The versatility of an OTA allows its use in many electronic systems such as filters, analog to digital converters, and oscillators. An OTA is also used as the core amplifier for an operational amplifier. The OTA is an essential element of many analog systems.

The symbol for a single-ended OTA is shown in Figure 8-1. The amplifier has two voltage inputs and a single current output. Fully differential versions have two current outputs, and are commonly used in integrated circuits.

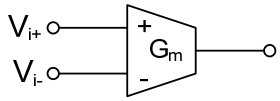

Figure 8-1: The OTA Symbol

The output current of an OTA is proportional to the difference between the input voltages. The relationship between the input voltages and output current is given by:

$$I_o = G_m(V_i^+ - V_i^-)$$

Typical input-output characteristic for an OTA is shown in Figure 8-2. Notice that this characteristic is similar to the input-output characteristic for the differential amplifier. For a given maximum output current, the width of the OTA's linear region is inversely related to the magnitude of the transconductance. The larger the linear region, the smaller the transconductance and vice versa.

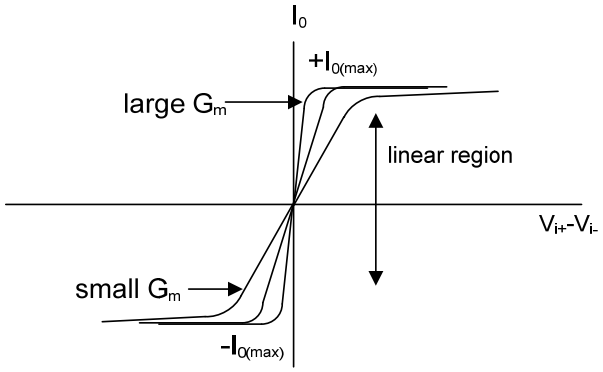

Figure 8-2: Typical Input-Output Characteristics for an OTA

The input and output resistances must be large in an OTA. Infinite input impedance allows maximum transfer of the source voltage to the input of the OTA. Maximum transfer of output current to the load occurs when the output resistance is infinite. The schematic of a basic OTA is shown in Figure 8-3.

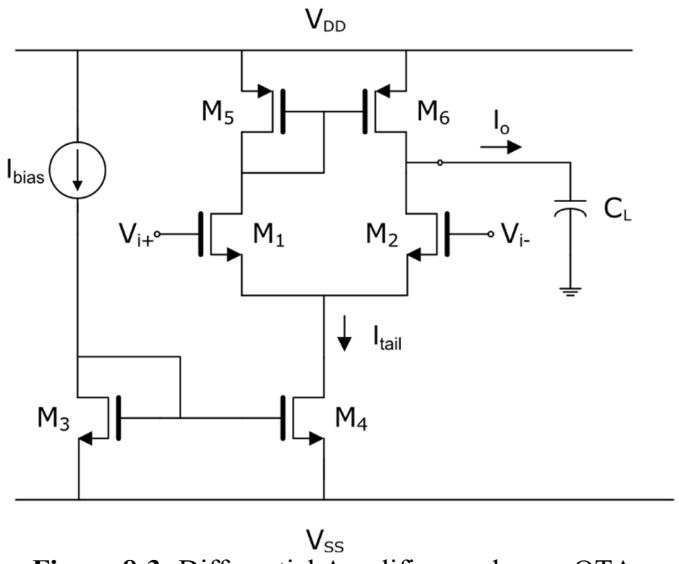

Figure 8-3: Differential Amplifier used as an OTA

A quick analysis of this amplifier shows that the transconductance is given by:

$$G_m = g_{m1,2}$$

The input resistance is large due to the inputs being at the gate terminals of the MOSFET differential pair. Notice that the output resistance is also large.

$$R_{out} = r_{02}||r_{06}$$

The gain-bandwidth product (GBW) is given approximately by:

$$\omega_{GBW} = \frac{g_{m1,2}}{C_L}$$

An improvement of the differential amplifier in Figure 8-3 is to use self-biased loads. The circuit in Figure 8-4 is called a symmetric OTA or the three current-mirror OTA. This circuit is constructed from all the basic elements discussed in the previous labs. The input stage is a differential pair, the sub-circuits composed of $M_{1,3}$ and $M_{2,4}$ are self-biased inverters, and the transistors $M_{3,5}$, $M_{4,6}$, $M_{7,8}$ and $M_{9,10}$ are simple current mirrors.

When designing the symmetrical OTA, transistors M_1=M_2, M_3=M_4, M_5=M_6 and M_7=M_8. This reduces the number of designable parameters to four transistor sizes and the tail current. An analysis of this amplifier shows the transconductance is given by:

$$G_m = N g_{m1,2} \qquad N = \frac{\left(\frac{W}{L}\right)_{5,6}}{\left(\frac{W}{L}\right)_{3,4}}$$

The input resistance is large due to the MOSFET input stage. The output resistance is given by:

$$R_{out} = r_{06}||r_{08}$$

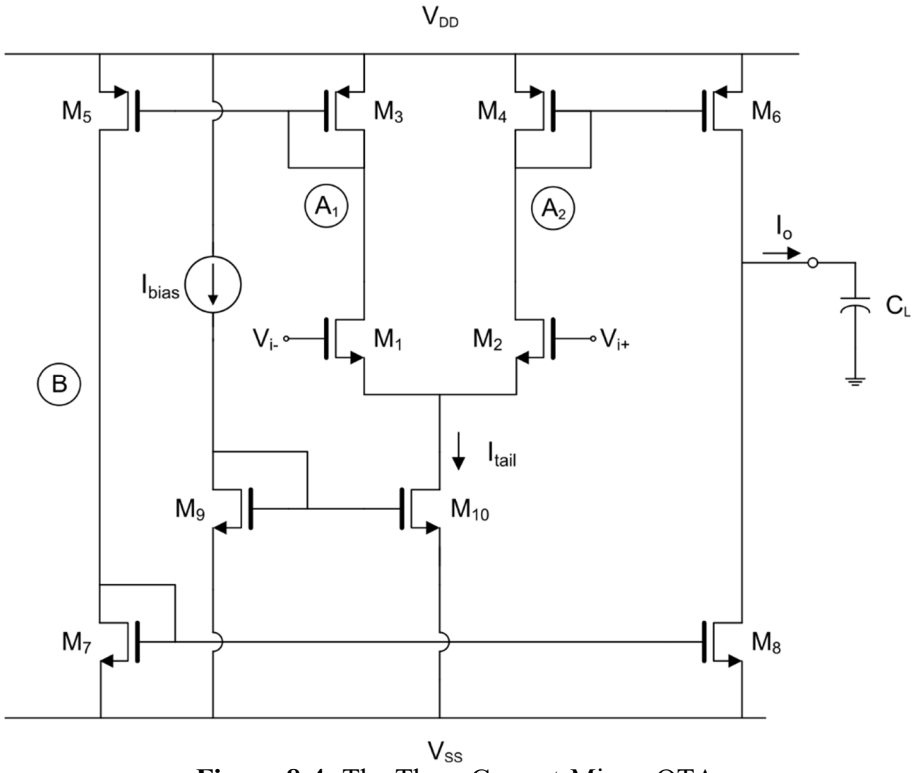

Figure 8-4: The Three Current-Mirror OTA

The gain-bandwidth product is given approximately by:

$$\omega_{GBW} = N\frac{g_{m1,2}}{C_L}$$

Analysis shows that the symmetric OTA has a larger transconductance, slew rate and GBW than the OTA of Figure 8-3. These specifications are made larger by increasing *N*.

Design Description

The design of an OTA begins with a consideration of the design specifications. The typical design specifications for an OTA include transconductance, slew rate, output resistance, GBW, noise, phase margin, power dissipation and output loading. The transconductance of the symmetric OTA was listed previously and is repeated here for convenience:

$$G_m = Ng_{m1,2} = N\sqrt{KP_N\left(\frac{W}{L}\right)_{1,2} I_{tail}} \quad , \qquad N = \frac{\left(\frac{W}{L}\right)_{5,6}}{\left(\frac{W}{L}\right)_{3,4}}$$

In the above equation, notice that the DC current in transistors $M_{5,6}$ is *N* times larger than the currents in transistors $M_{3,4}$. The transconductance can be set by the tail current source, current mirror ratio, or size of the input transistors. The transconductance is usually the most important parameter, and it is fortunate that it can be determined by several parameters. Automatic tuning circuits sometimes vary the bias current to adjust the transconductance to the desired value.

The slew rate of the OTA is given by:

$$SR = N\frac{I_{tail}}{C_L}$$

Notice the slew rate is larger than the slew rate of the differential amplifier. The increased slew rate comes with the disadvantage of an increase in current which leads to an increase in power consumption. The current drawn from the power supply (not including the bias current source) is given by:

$$I_{DD} = \frac{1}{2}I_{tail} + \frac{1}{2}I_{tail} + \frac{1}{2}NI_{tail} + \frac{1}{2}NI_{tail} = (N+1)I_{tail}$$

The output resistance was provided earlier and is repeated below as:

$$R_{out} = r_{06}||r_{08}$$

The gain-bandwidth product is given by:

$$\omega_{GBW} = A_{v0}\omega_{p1} = (G_m R_{out})\left(\frac{1}{R_{out}C_L}\right) = \frac{G_m}{C_L}$$

Another design consideration is noise. The noise performance is improved when the voltage gain of the first stage is large. The voltage gain of the first stage is given by:

$$A_{v1} = \frac{g_{m1,2}}{g_{m3,4}} = \sqrt{\frac{2KP_N\left(\frac{W}{L}\right)_{1,2}\frac{I_{tail}}{2}}{2KP_P\left(\frac{W}{L}\right)_{3,4}\frac{I_{tail}}{2}}} = \sqrt{\frac{KP_N\left(\frac{W}{L}\right)_{1,2}}{KP_P\left(\frac{W}{L}\right)_{3,4}}}$$

The phase margin is a measure of stability for the amplifier. In most cases, the load capacitance is much larger than the capacitance at the other nodes. When this is the case, the OTA has a dominant pole at the output node and two non-dominant poles at the other two nodes. Due to the symmetric behavior at the input stage, the amplifier also has a right half plane zero. For most symmetric OTA designs, the non-dominant poles and zero are much larger than the gain-bandwidth product and degrade the phase margin by less than 10º each. This gives a typical phase margin of greater than 60º. The transfer function of the OTA is given by:

$$H(s) = \frac{A_{v0}\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)\left(1 + \frac{s}{\omega_{p3}}\right)}$$

where ω_{p1} is the dominant pole located at the output node:

$$\omega_{p1} = \frac{1}{R_{out}C_L}$$

ω_{p2} is the non-dominant pole located at nodes A_1 and A_2:

$$\omega_{p2} = \frac{1}{R_A C_A} \approx \frac{g_{m3,4}}{C_A}$$

ω_{p3} is the non-dominant pole located at node B:

$$\omega_{p3} = \frac{1}{R_B C_B} \approx \frac{g_{m7}}{C_B}$$

ω_z is the zero due to the pole-zero double formed by the symmetric input stage:

$$\omega_z = 2\omega_{p2}$$

In the above expressions, C_A is the parasitic capacitance connected at either node A_1 or A_2, and C_B is the capacitance connected to node B. For a system that can be approximated as having a single pole, the phase margin can be approximated as:

$$PM = 180° - \tan^{-1}(A_{v0}) - \tan^{-1}\left(\frac{\omega_{UGF}}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_{UGF}}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_{UGF}}{\omega_{p3}}\right)$$

$$PM \approx 90° - \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_{GBW}}{2\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_{GBW}}{\omega_{p3}}\right)$$

In the above phase margin expression, ω_{UGF} is the unity-gain frequency of the amplifier. The above design description shows that many performance figures are inversely related. For example, increasing slew rate results in an increase in power dissipation.

Determining Output Swing

One method of determining the output swing from simulations is to use a DC sweep on the open-loop OTA. The *region* operating point parameter of the output transistors can be used to determine when the devices transition from the saturation region to the triode region. The output voltages at which one of the devices is no longer in saturation can define the output swing of the OTA. An example of what these simulation results may look like is shown in Figure 8-5. The vertical markers (placed with the "V" hotkey) are placed where either of the output devices transition between the saturation and triode regions. The output swing would be the difference between the output voltage values indicated at these two points, which is about 1.45V in this case. When using this method for evaluating the output swing range, the simulation will need to be updated for post-layout simulations. To plot the region parameter of the output transistors, the devices must be re-selected from the calibre view of the cell after the post-layout extraction. Refer to the Lab 5 manual for more information on using the region parameter in schematic simulations and how to plot the region parameter of a transistor in post-layout simulations.

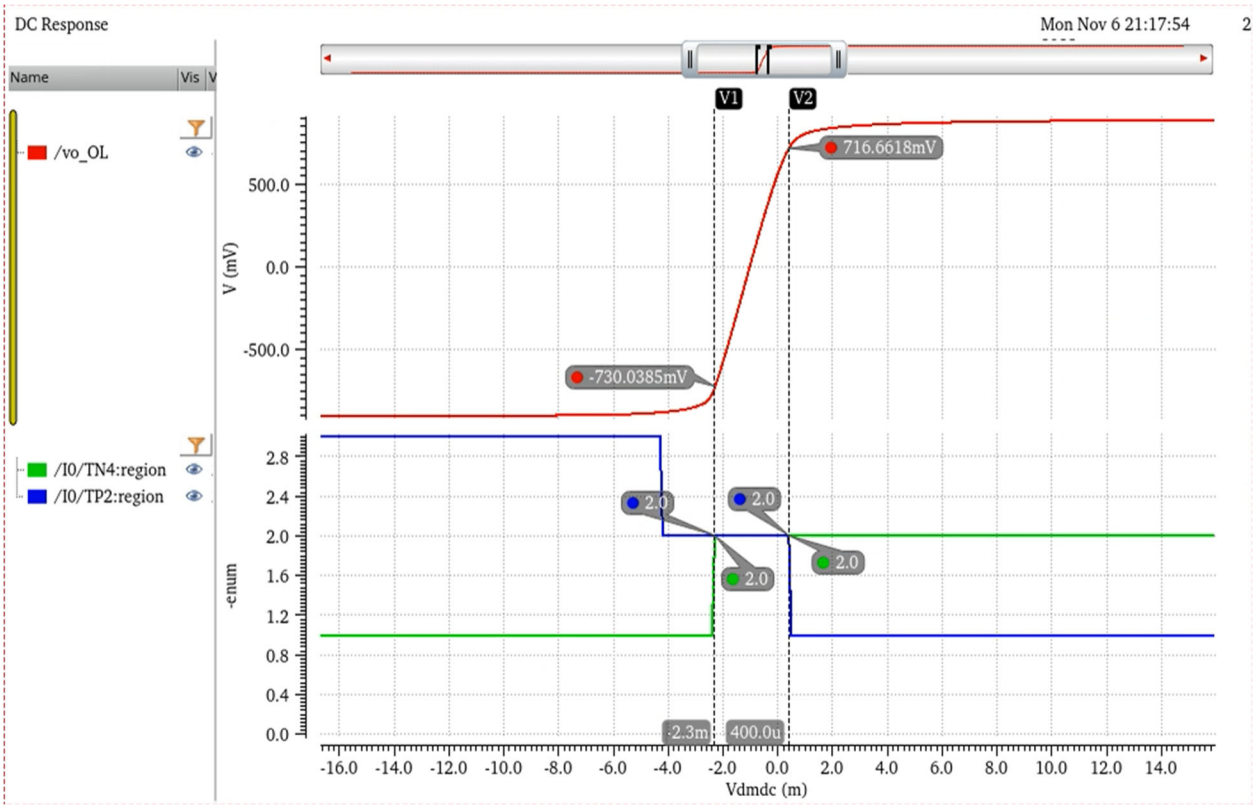

Figure 8-5: Output swing measurement based on transistor region parameter

Stability Analysis

Because phase margin is a stability criterion for a system that is connected in feedback, a stability analysis must be performed in Cadence in order to accurately characterize it. The stability analysis is very similar to an AC analysis in that it utilizes a linearized model of the circuit based around the circuit's DC operating point. However, it differs in that the stability analysis will break the feedback loop of a system in such a way that the DC operating point is preserved, it will inject an AC signal into the feedback loop, and then the magnitude and phase of the signal will be evaluated at a point just before where the signal was injected. This kind of analysis allows us to measure the loop gain and phase responses of a system in feedback so that we can properly evaluate the system's stability.

While there are multiple ways to break the feedback loop of an analog circuit and inject an AC signal while preserving the system's DC operating point, one of the simplest ways to do so in Cadence is with a component called **iprobe** from the **analogLib** library, shown in Figure 8-6.

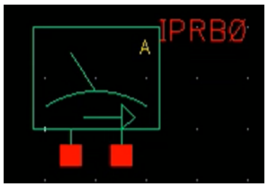

Figure 8-6: iprobe component from **analogLib** library

In order to use the **iprobe** for stability analysis, the amplifier must be connected in a feedback configuration, and the **iprobe** will be placed in the feedback loop at a position that breaks the signal's return path to an

input of the amplifier. The arrow on the **iprobe** should point in the same direction that the signal will propagate through the loop. An example of a negative feedback setup is shown in Figure 8-7. The negative feedback comes from connecting the OTA's output to its inverting input ("VN"), and the result is that this configuration creates a unity-gain buffer. Additionally, it should be noted that if a stability analysis of a fully-differential amplifier circuit is needed, the **diffstbprobe** component from the **analogLib** library should be used instead of the **iprobe** component.

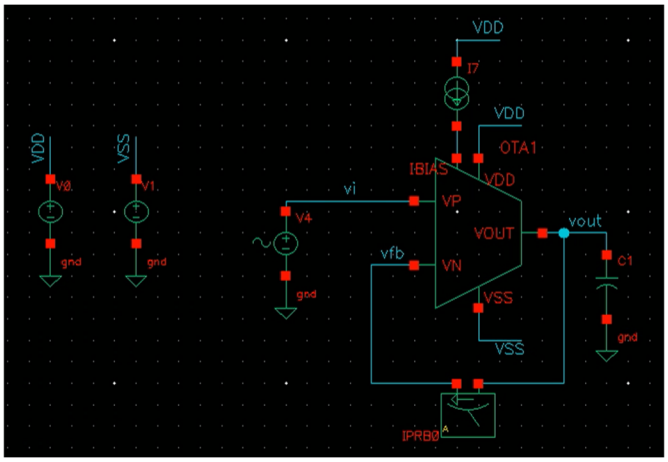

Figure 8-7: Unity-gain buffer configuration for stability analysis

From the ADE L window, create a new analysis type, and select the "stb" analysis in the analysis setup window. Configure the stability analysis similarly to an AC sweep. The main difference in the setup is the additional "Probe Instance/Terminal" field. Click the "Select" button next to this field, go to the test bench schematic window, select the **iprobe** component in the schematic, and return to the analysis setup window. The "Probe Instance/Terminal" field should now be filled with the instance name associated with the iprobe component. The "Local Ground Name" field can be left empty. Click "OK" to save the analysis settings and add the stability analysis to the list of simulations in the ADE L state, and then run a simulation. Note that the AC magnitude parameters of sources in the schematic are ignored in the stb analysis.

To see the loop gain magnitude and phase responses from the stability analysis, from the ADE L window go to *Results* → *Direct Plot* → *Main Form…*, and in the window that appears (shown in Figure 8-8), select the "stb" analysis results, choose the "Loop Gain" option, make sure that "Magnitude and Phase" are selected in the "Modifier" field, and click the "plot" button at the bottom of the window. The loop gain and phase response can also be added to the list of ADE L outputs with the "Add To Outputs" button.

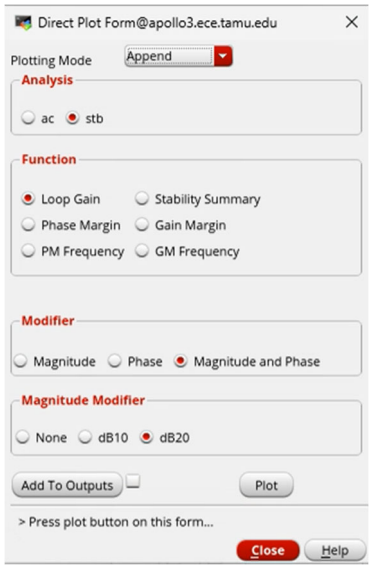

Figure 8-8: Direct Plot settings for plotting stability analysis results

The plot of the loop gain and phase responses should look similar to what is shown in Figure 8-9. Note that for this feedback configuration, the phase plot begins at a phase of 180° because the system is connected in a negative feedback configuration. From this plot, the phase margin of the circuit can be determined.

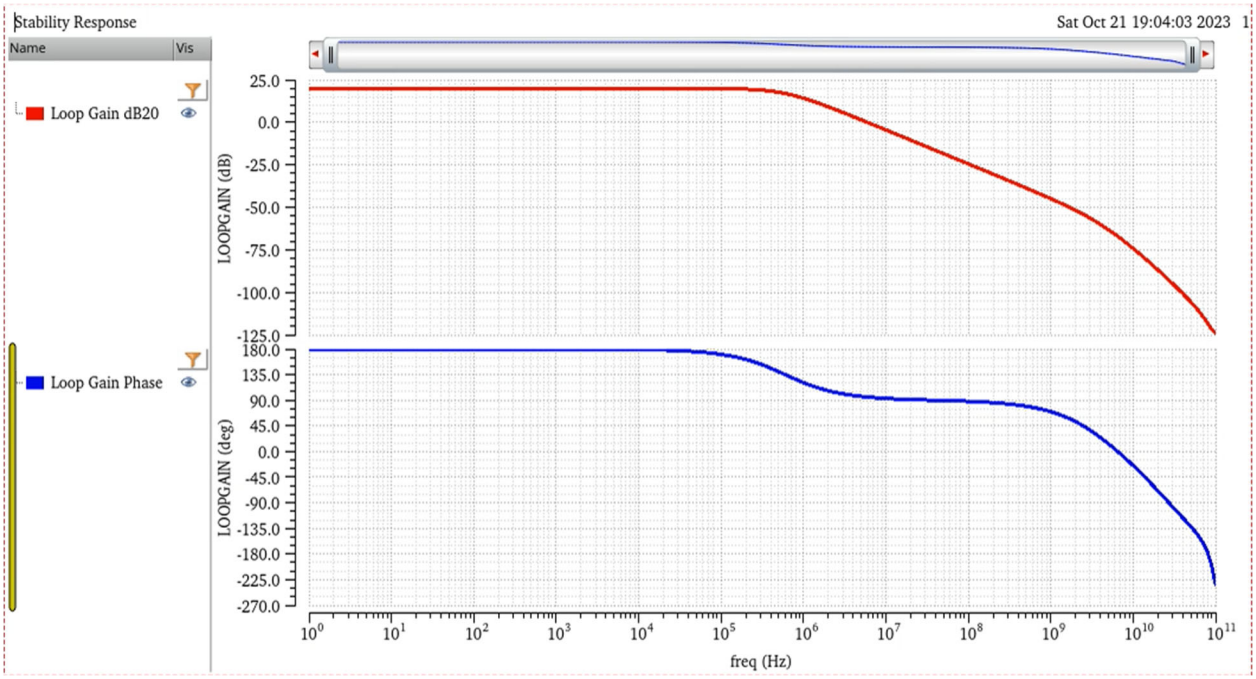

Figure 8-9: Loop Gain and Phase responses from stability analysis results

Prelab

Design the three current mirror OTA of Figure 8-4 to obtain the following specifications:

G_m	> 500 µA/V
Slew Rate	> 10 V/µs
Peak-to-Peak Output Swing	> 1 V
Load Capacitance	20 pF
Power	< 1 mW (not including bias current source)
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V

Lab Report

1. Simulate the designs from the prelab. Measure (include formulas used) and plot (use markers):

   a) Power consumption (max power consumption over the common-mode input voltage range)
   b) Open-loop Transconductance versus frequency
   c) Open-loop Voltage gain versus frequency
   d) Dominant pole frequency
   e) Gain-bandwidth product
   f) Slew rate
   g) Phase margin in unity-gain buffer configuration

   Normally the transconductance of a circuit is characterized as the ratio between the short-circuit output current and the input voltage. In this case, measure the output current of the OTA into the capacitor in order to not significantly disturb the natural DC operating point of the OTA. This will cause the plot of transconductance versus frequency to have a band-pass response. The maximum value of the transconductance within the pass-band region should be compared against the specification.

   Additionally, for this OTA circuit, the common-mode input voltage range is defined by the common-mode voltage over which the transistors in the first stage are in the saturation region, similarly to the simple differential input pair designed in Lab 6.

   Use any analysis necessary to obtain the most accurate measurements. Modify your design as necessary to meet the given specifications. Include these results in the lab report.

2. Create three cell views for your OTA. The symbol, schematic and layout. Layout your final design and use good layout techniques and include the LVS report (again NetID and time stamp required for credit). Indicate which transistors should be matched in your lab report. Extract the layout and repeat the measurements from part 1. Be sure to include parasitic capacitances in the extraction.