24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab6: Differential Pairs

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Section:601

Professor: Aydin Karsilayan

TA: Troy Buhr

Description:

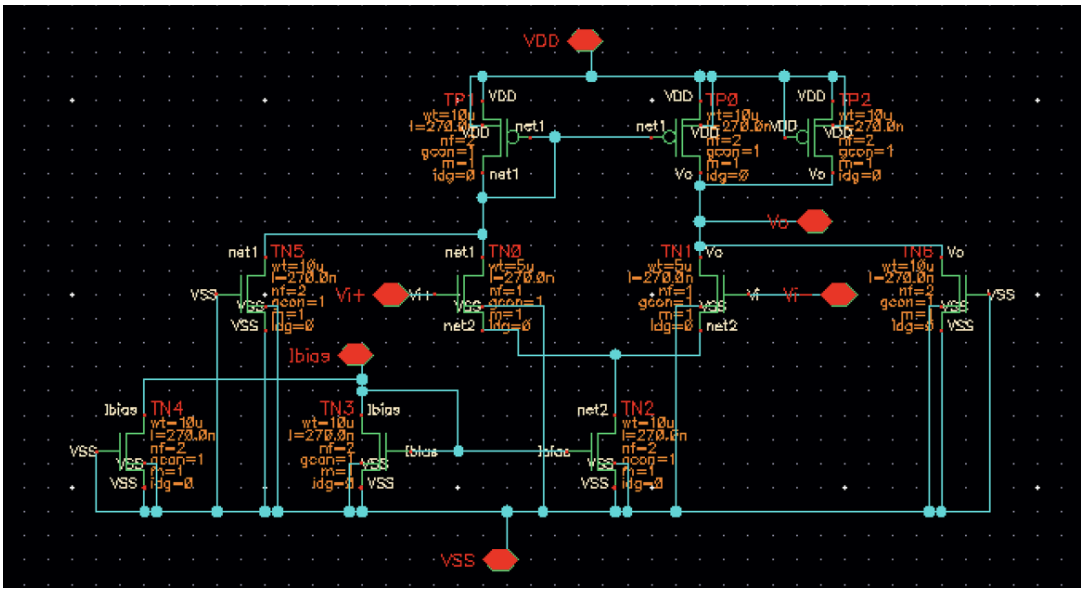
In this lab, we learn to make differential pairs. A **differential pair** is a key building block in analog circuits, commonly used in amplifiers, comparators, and operational amplifiers. It consists of two transistors with shared current and complementary inputs, allowing the circuit to amplify the difference between two input signals while rejecting common-mode noise. This makes differential pairs ideal for noise-immune applications in both analog and mixed-signal designs.

Design & result

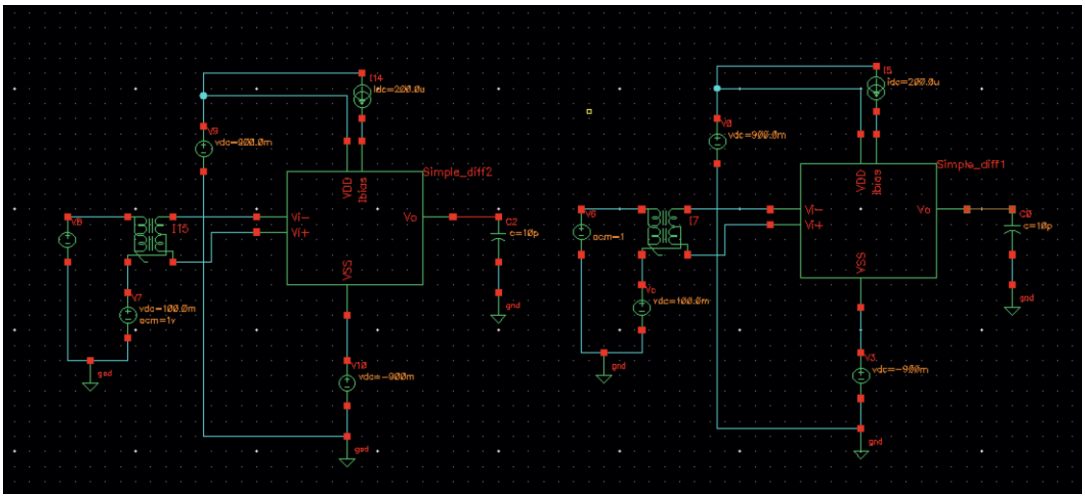
1. Design the simple differential amplifier to obtain the following specifications:

Slew Rate	> 10 V/μs
Gain-Bandwidth Product	> 5 MHz
Common-mode Input Voltage Range	> 0.5 V
Power Supply	V_{DD} = -V_{SS} = 0.9 V
Load Capacitance	10 pF

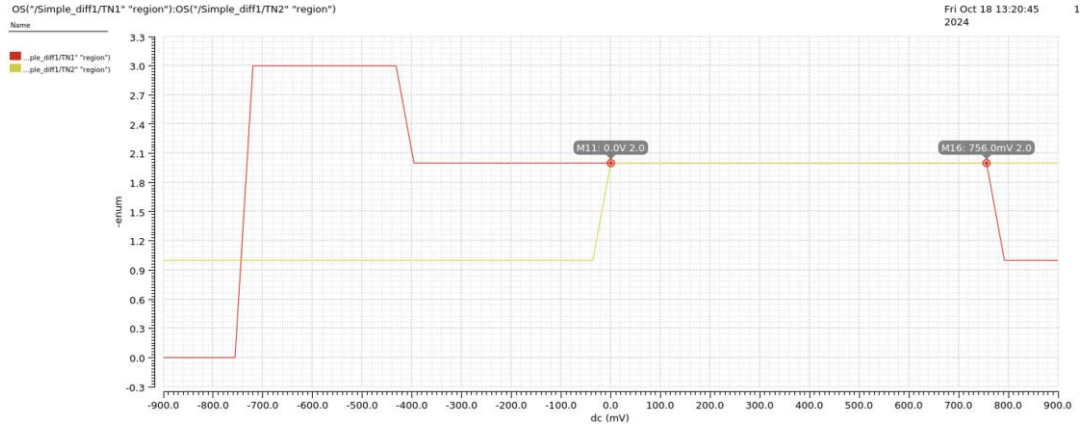
schematic



testbench

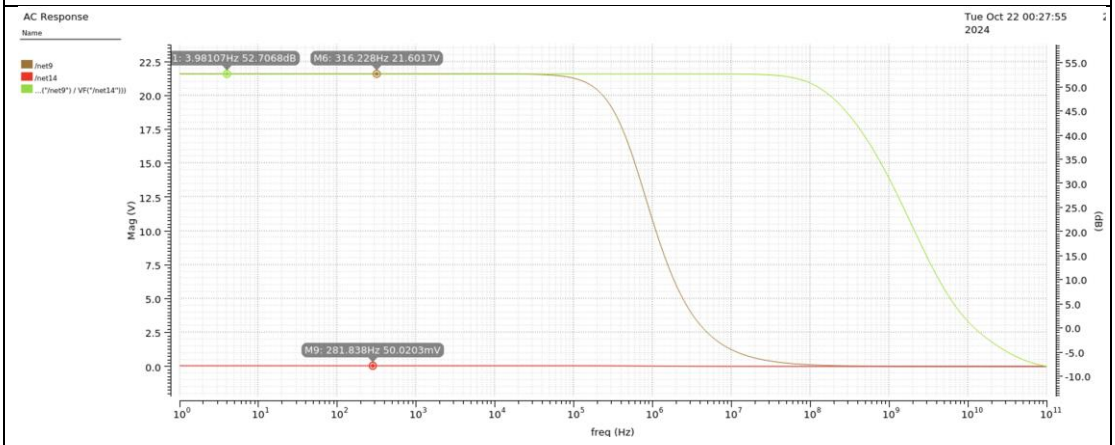


Common-mode range $Vin(CM)$



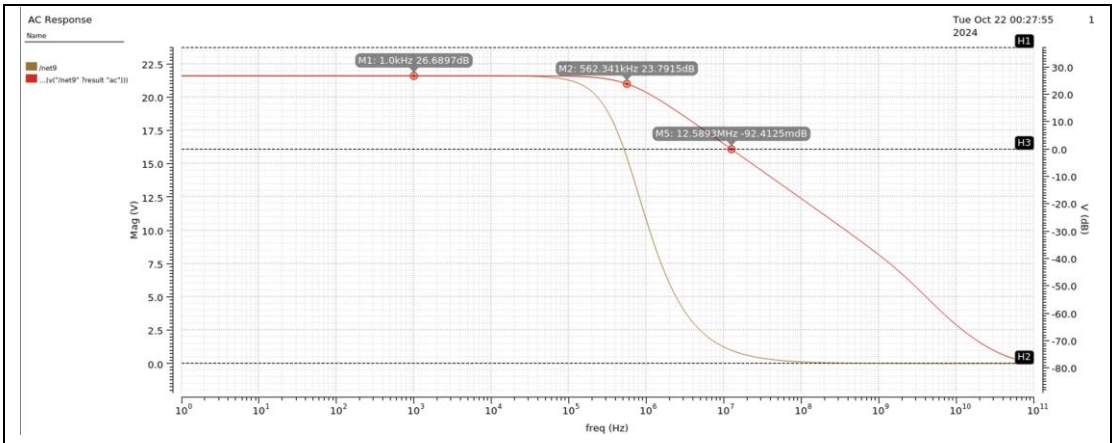
- Red line: TN1 (Vo)
- Yellow line: TN2 (bottom right MOS)

Differential-mode gain & Common-mode gain & CMRR



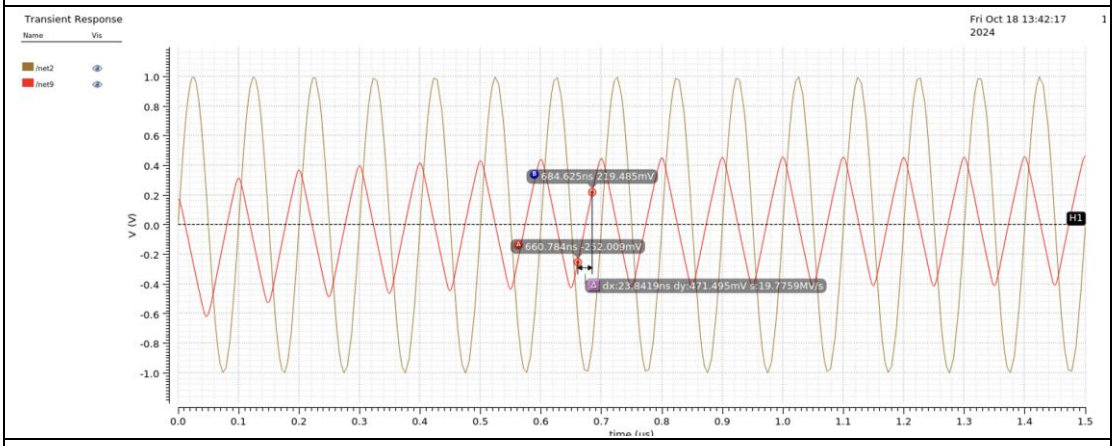
- Red line: Common-mode gain Ac
- Brown line: Common-mode gain Ad
- Green line: CMRR (dB)

GBW & Dominant pole fp1

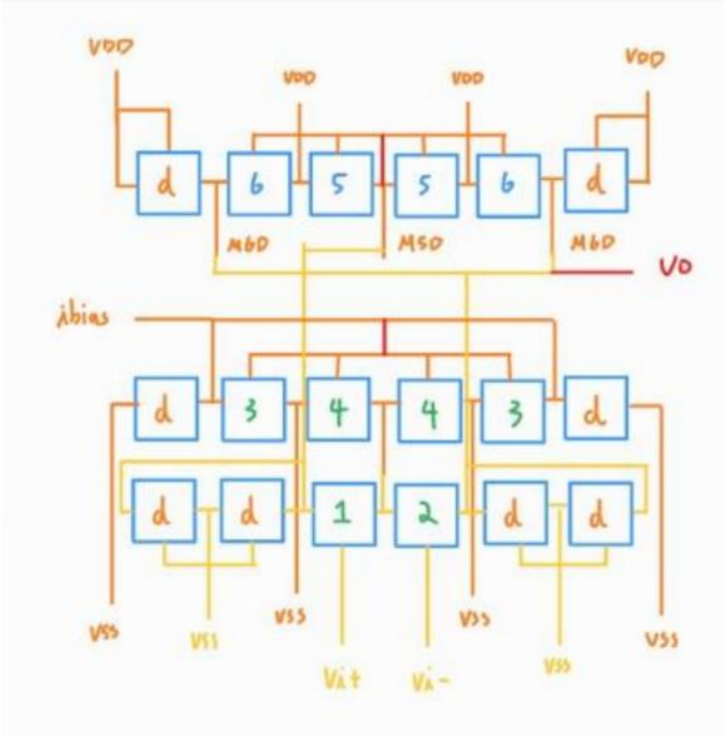


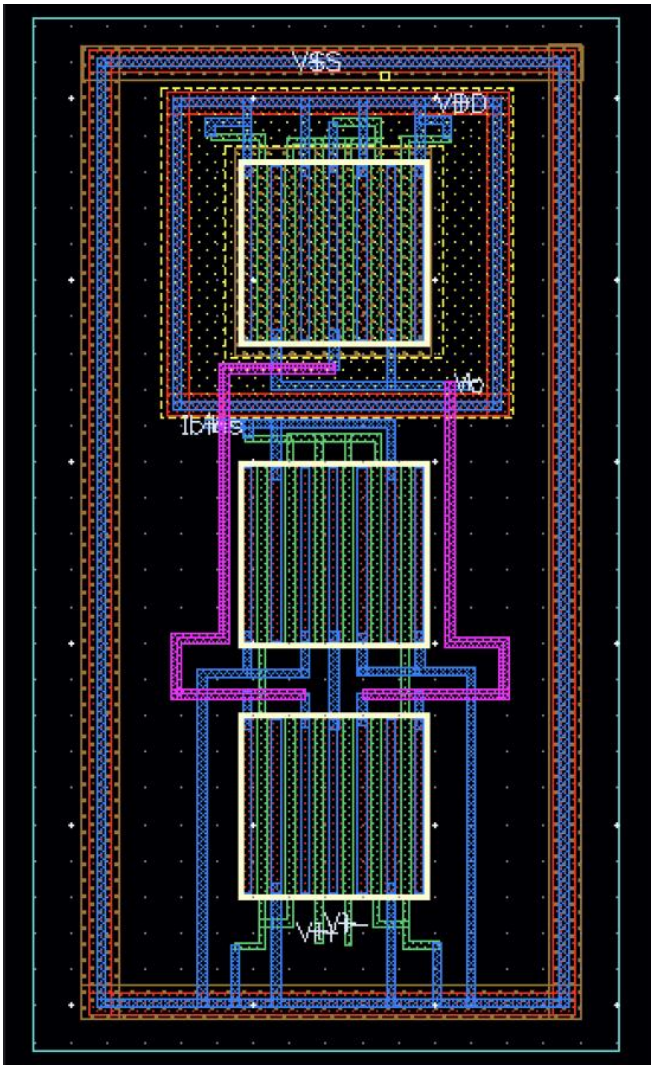
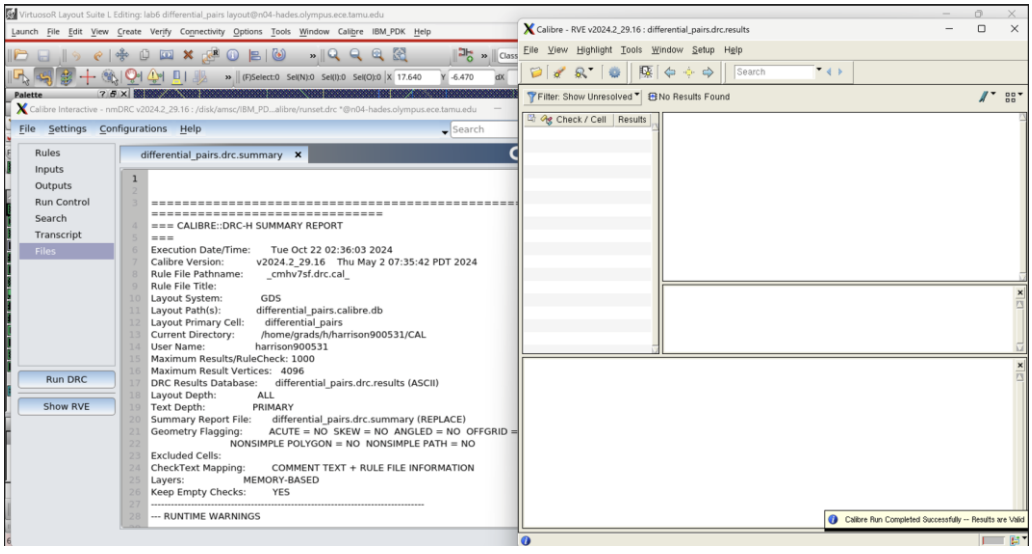
- M2: Dominant pole fp1 (-3dB)
- M3: GBW (0dB / Gain=1)

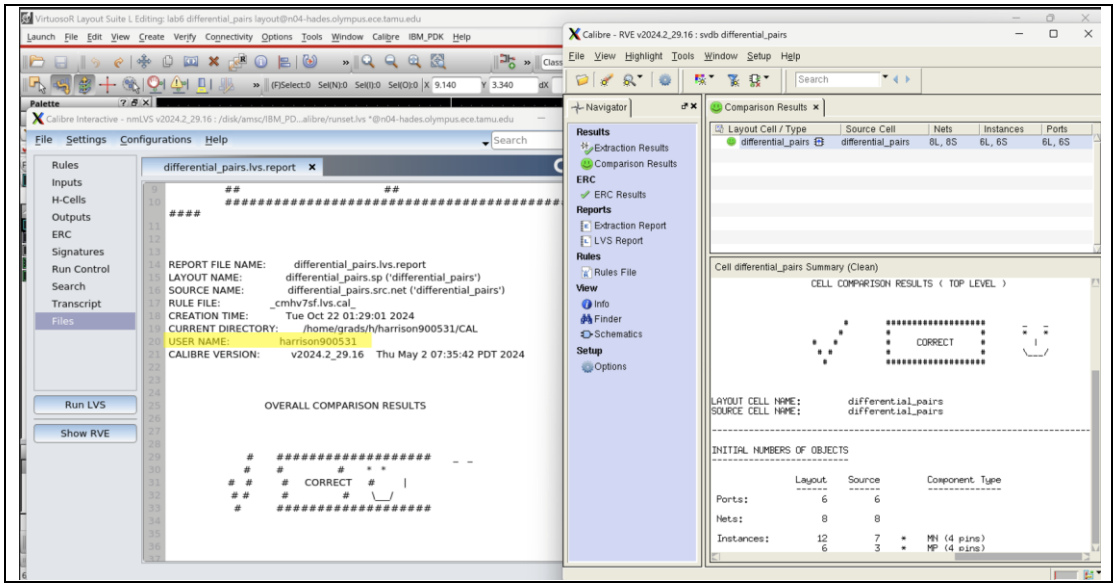
Slew rate



Floor Plan



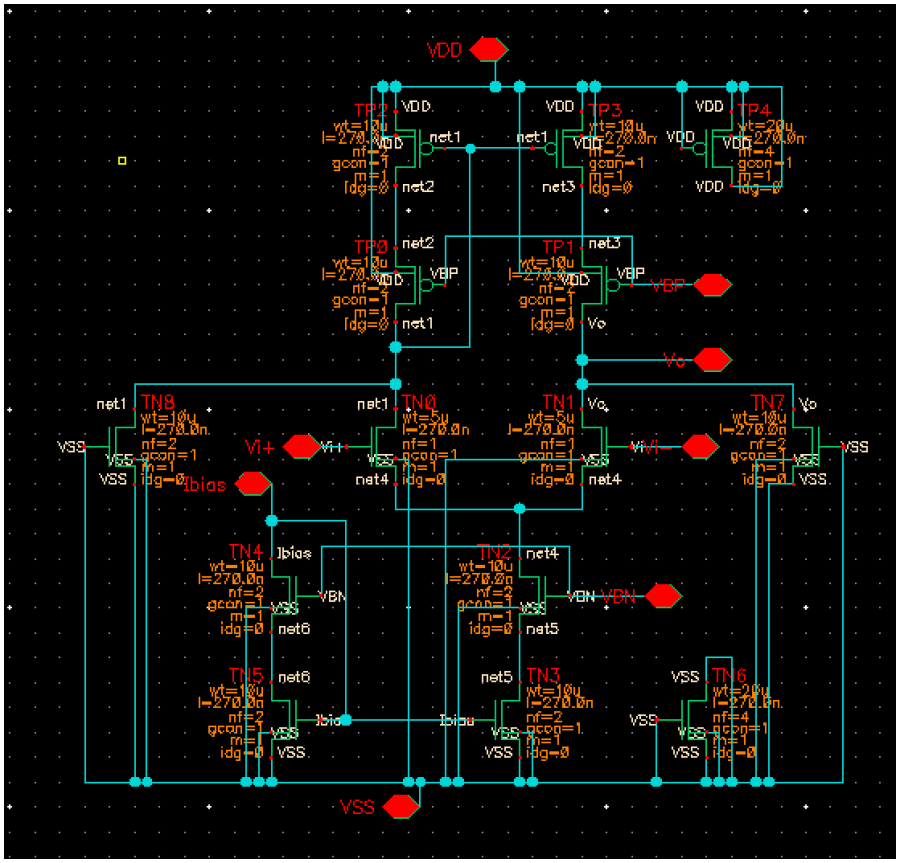
layout

DRC

LVS



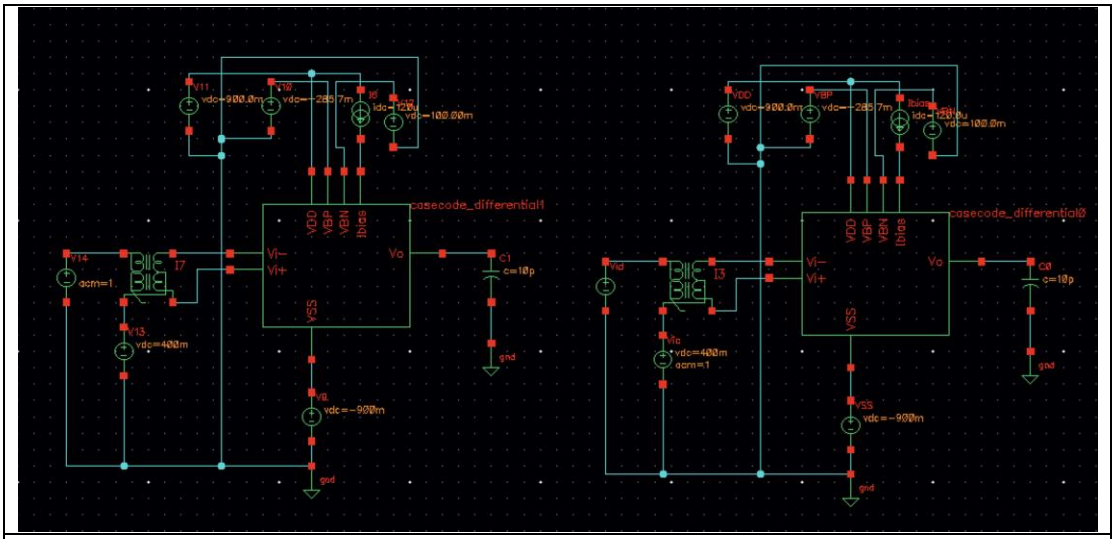
2. Design the differential amplifier with cascode current mirrors

Slew Rate	> 10 V/μs
Gain-Bandwidth Product	> 5 MHz
CMRR	> 60 dB
Power Supply	V_{DD} = -V_{SS} = 0.9 V
Load Capacitance	10 pF

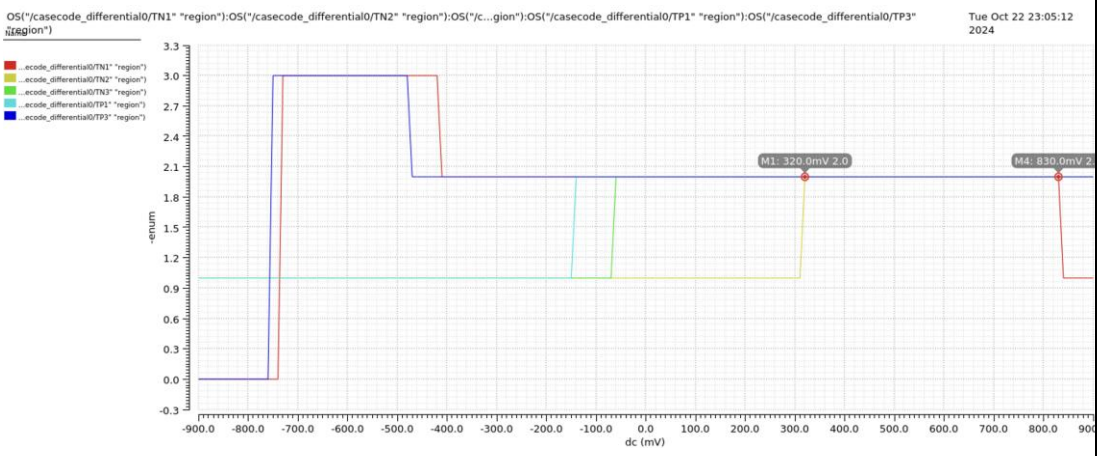
schematic



testbench

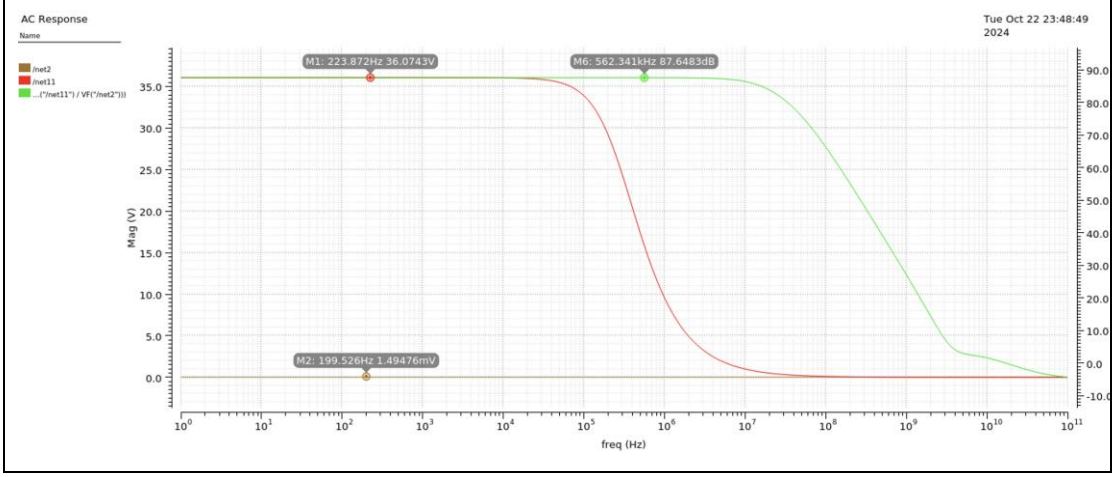


Common-mode range $Vin(CM)$



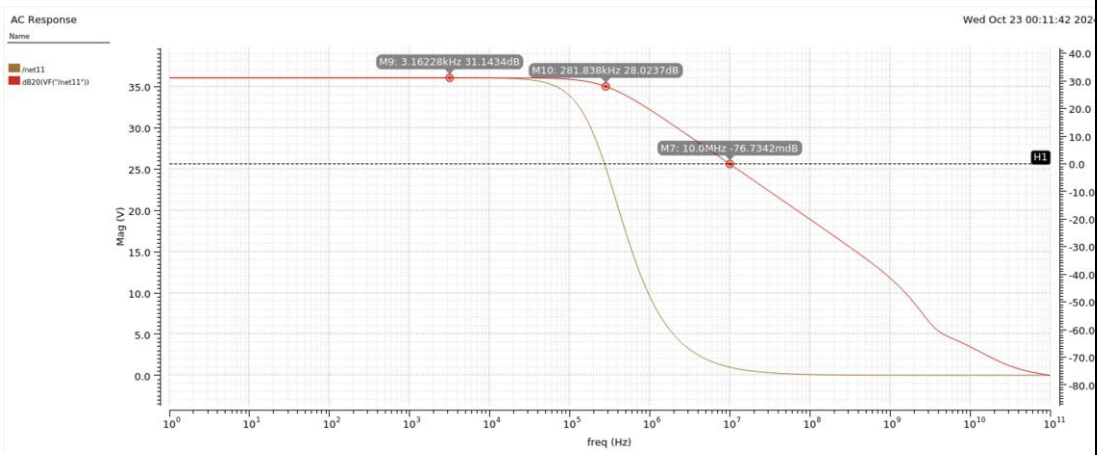
- Red line: TN1 (Vo)
- Yellow line: TN2 (bellow Vo)
- Green line: TN3 (bellow TN2)
- Bright Blue line: TP1 (above Vo)
- Blue line: TP3 (above TP1)

Differential-mode gain & Common-mode gain & CMRR



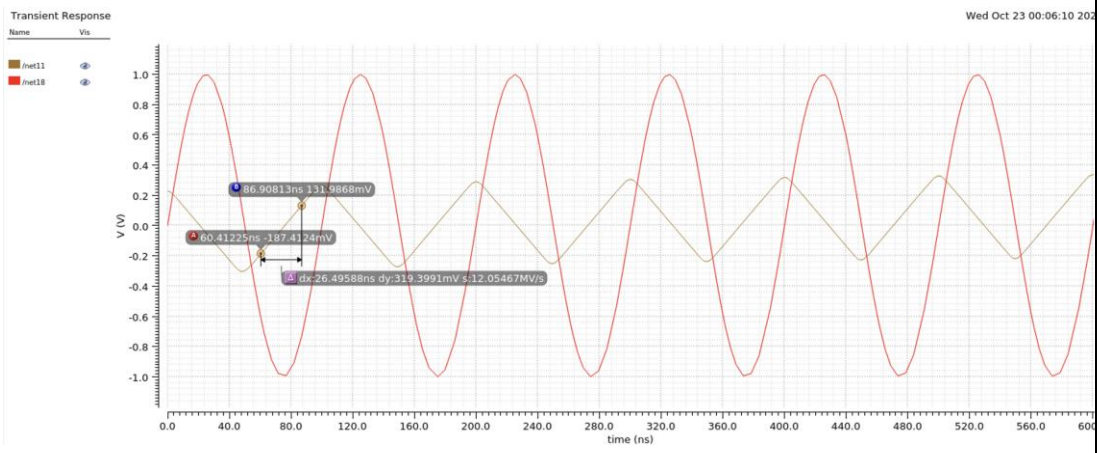
- Brown line: Common-mode gain Ac
- Red line: Common-mode gain Ad
- Green line: CMRR (dB)

GBW & Dominant pole fp1

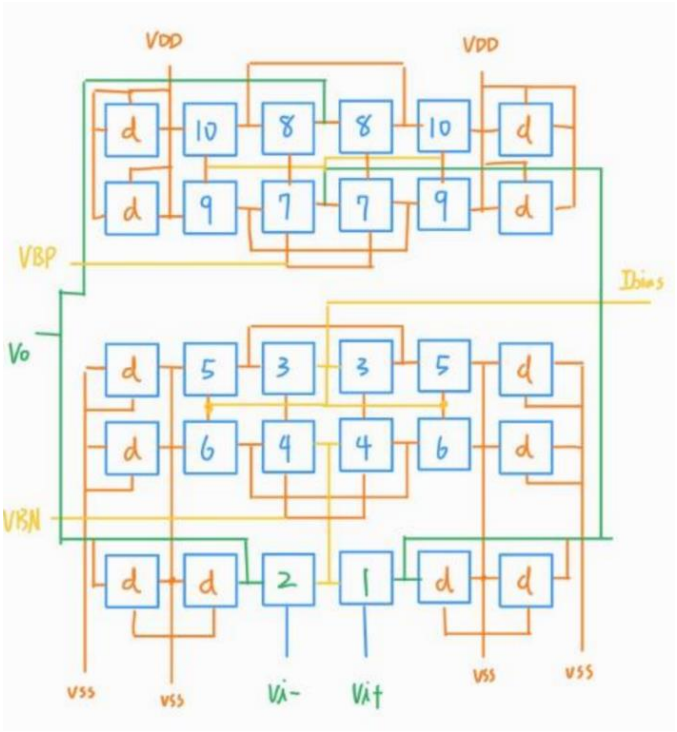


- M10: Dominant pole fp1
- M7: GBW

Slew rate



Floor Plan


VDD
VDD
d
10
8
8
10
d
d
9
7
7
9
d
VBP
Ibias
Vo
d
5
3
3
5
d
d
6
4
4
6
d
VBN
d
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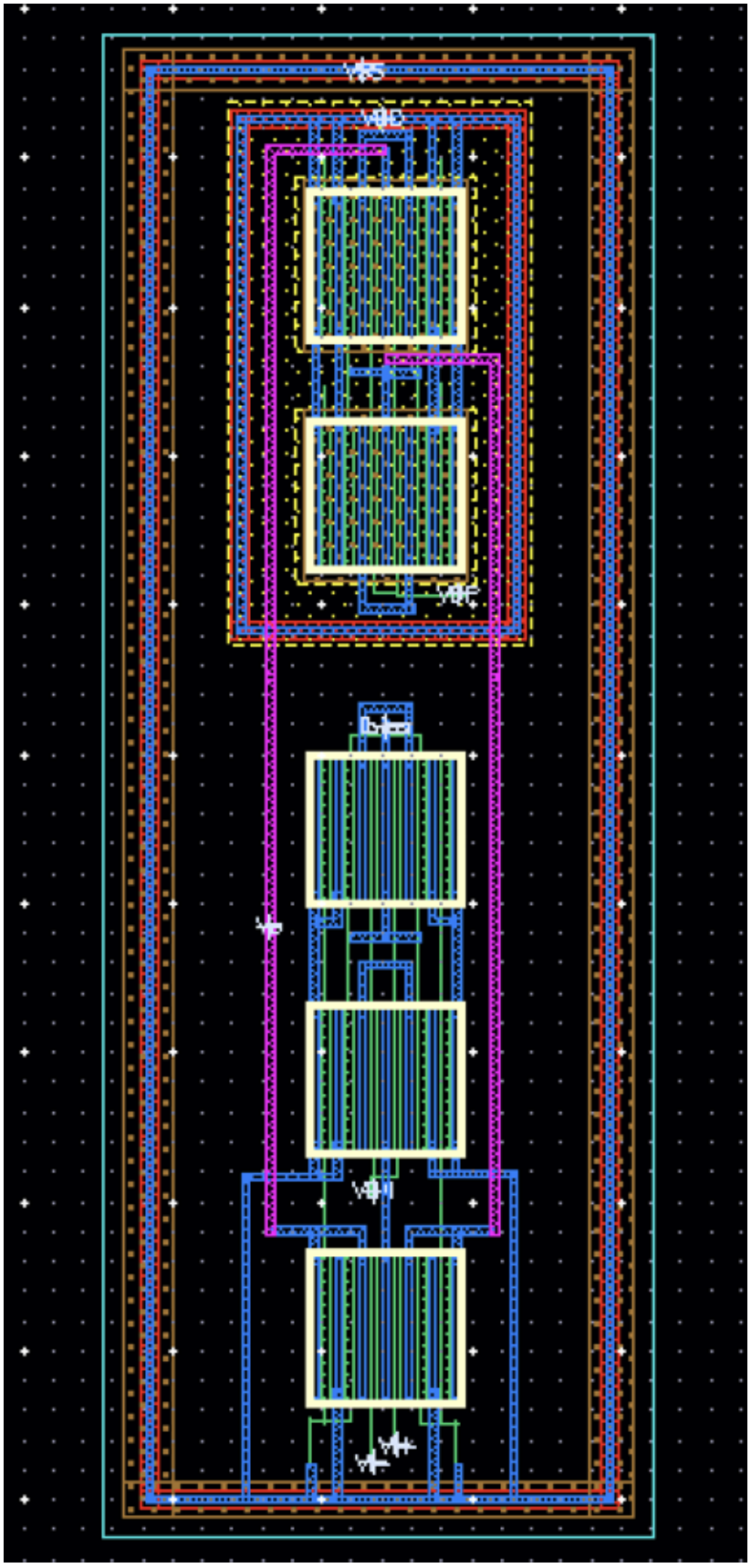
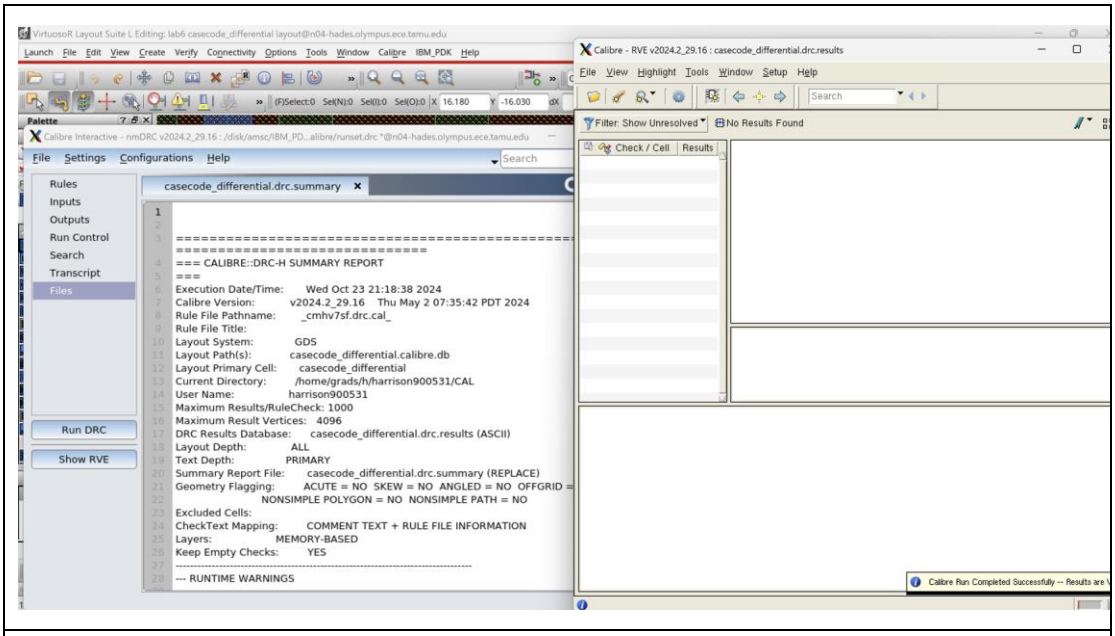
2
1
d
d
VSS
VSS
VA-
VA+
VSS
VSS

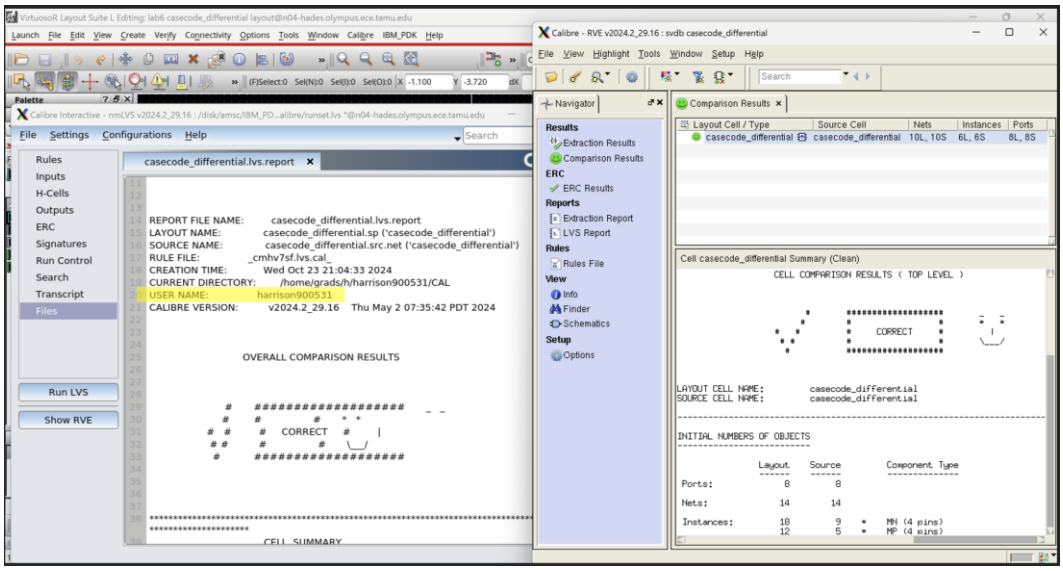
layout



DRC



LVS



Discussion:

The common-mode input voltage determines the output DC voltage, which in turn affects the swing of the AC differential voltage. Therefore, it is crucial to select the common-mode input voltage carefully to ensure it does not impact the AC differential gain. However, achieving the optimal swing, where Vo equals min number of Veff, makes it challenging to determine the values of W/L, Ibias, VBP, and VBN through hand calculations alone. This difficulty arises because the voltage at each point will change based on variations in a single factor.

To eliminate the noise from the input, which will equally affect both inputs and lead to common-mode gain, we ideally want the common-mode gain (Ac) to be zero. Although

Ac is not exactly zero, it is still a small value compared to the differential gain (Ad), allowing us to ignore or nearly neglect the impact of Ac, which is the noise effect.

Conclusion:

After completing Lab 6, we learned how to design a simple differential amplifier and a differential amplifier with cascode current mirrors. Although there are many factors to consider, we can still obtain an estimated value and fix one factor, using simulation to determine the other factors, ensuring that they all meet the requirements. It is important for us to know how to use and design differential pairs because of their ability to eliminate noise at the input.