24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab4: Advanced Layout Design Techniques

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Section:601

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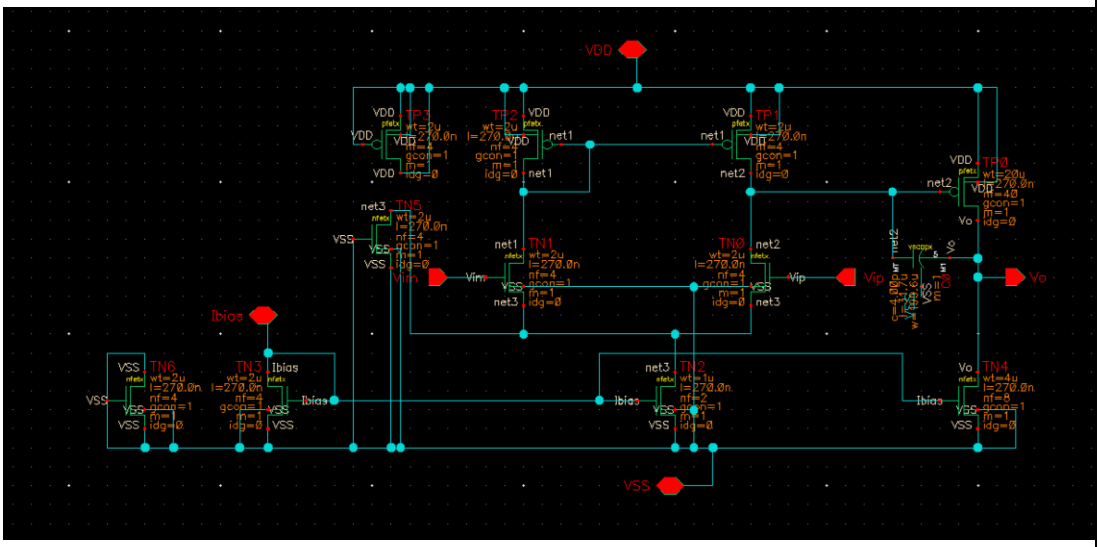
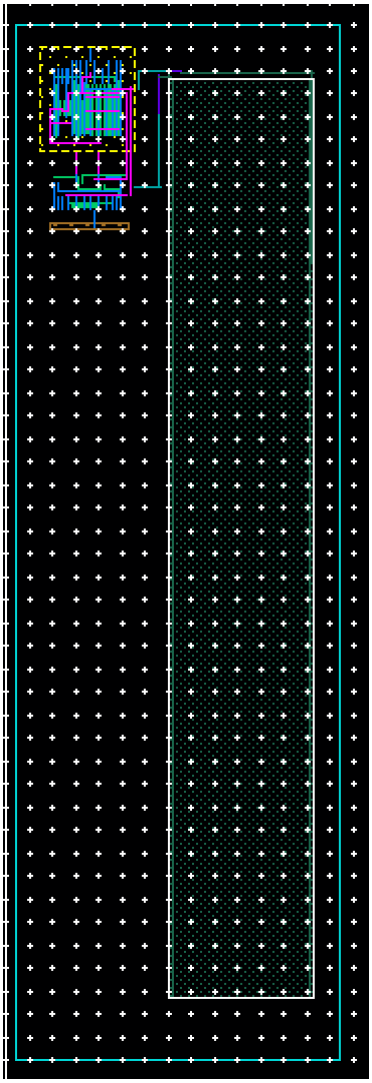
TA: Troy Buhr

Description:

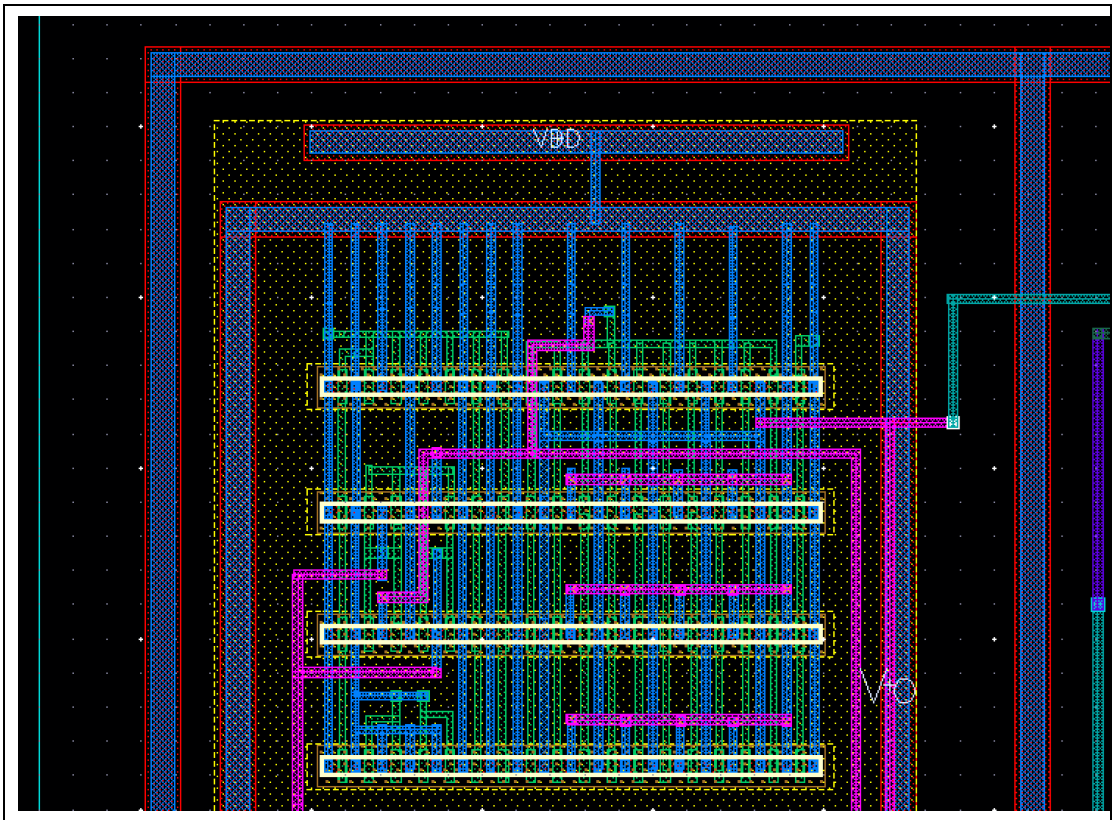
In this lab, we learned to utilize various layout techniques, including guard rings, I/O pads, and ESD protection. By employing these techniques, we can enhance circuit performance by improving matching, reducing interference from external factors, and providing protection against permanent damage

Design & result

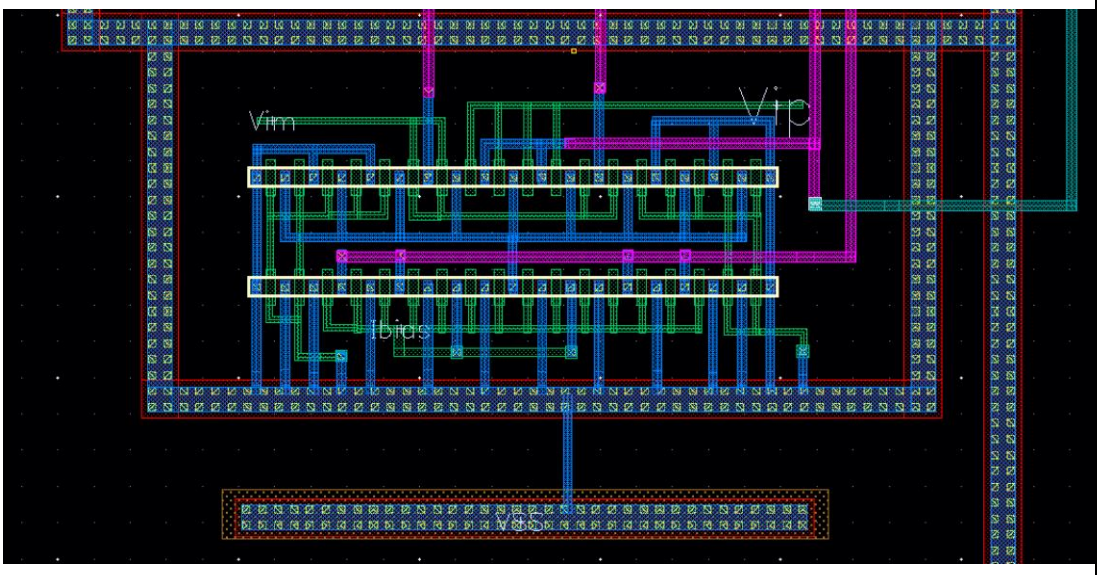
Schematic (without I/O pad)

layout



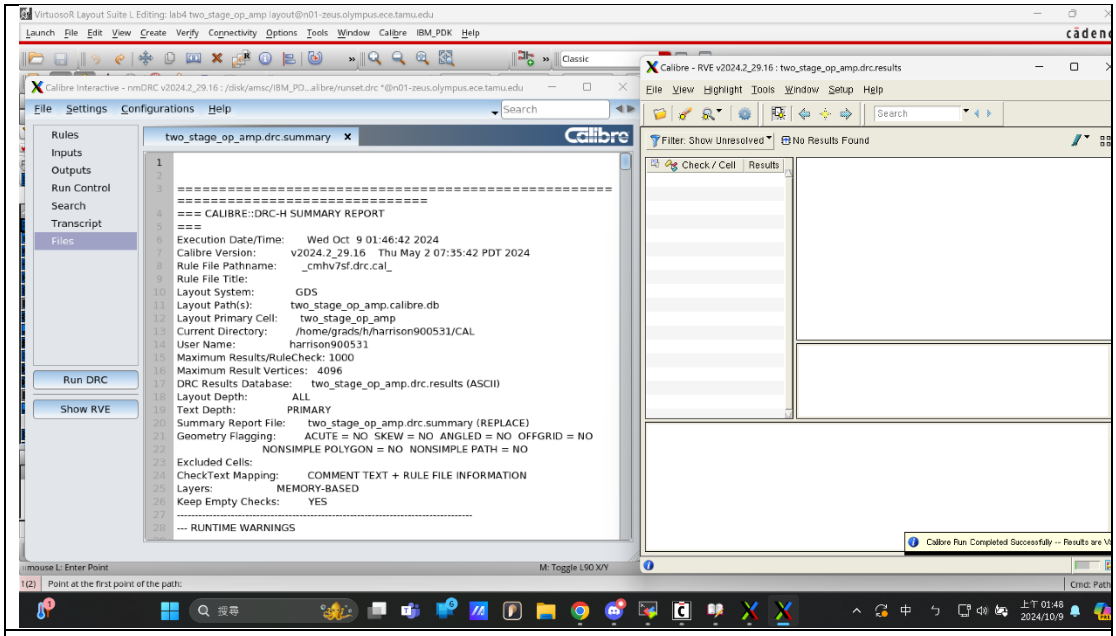
Layout(PMOS)



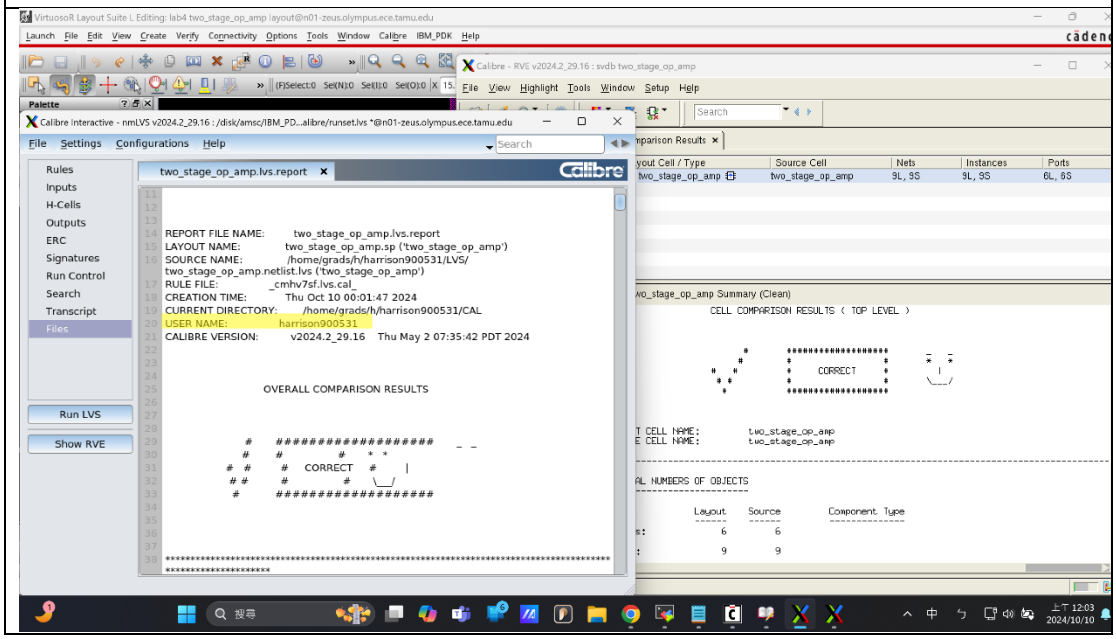
Layout(NMOS)



DRC

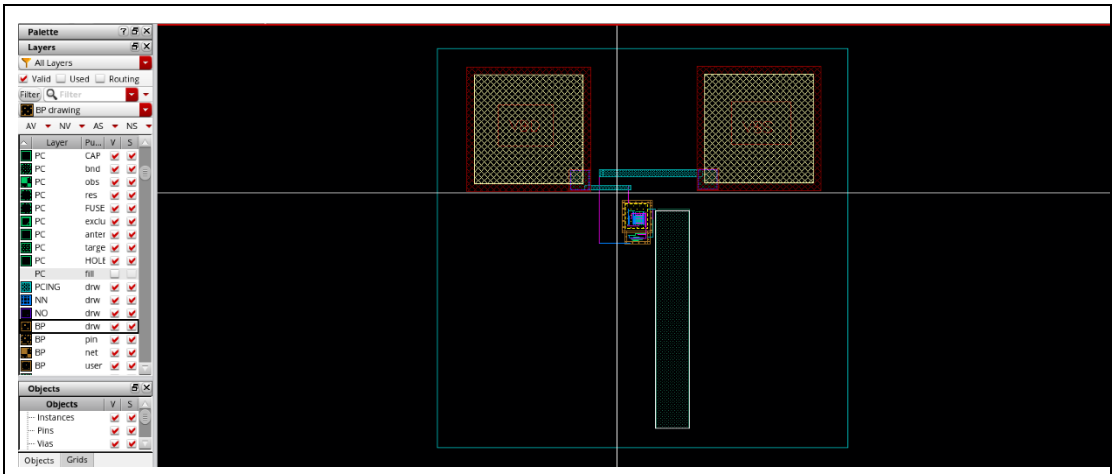


LVS

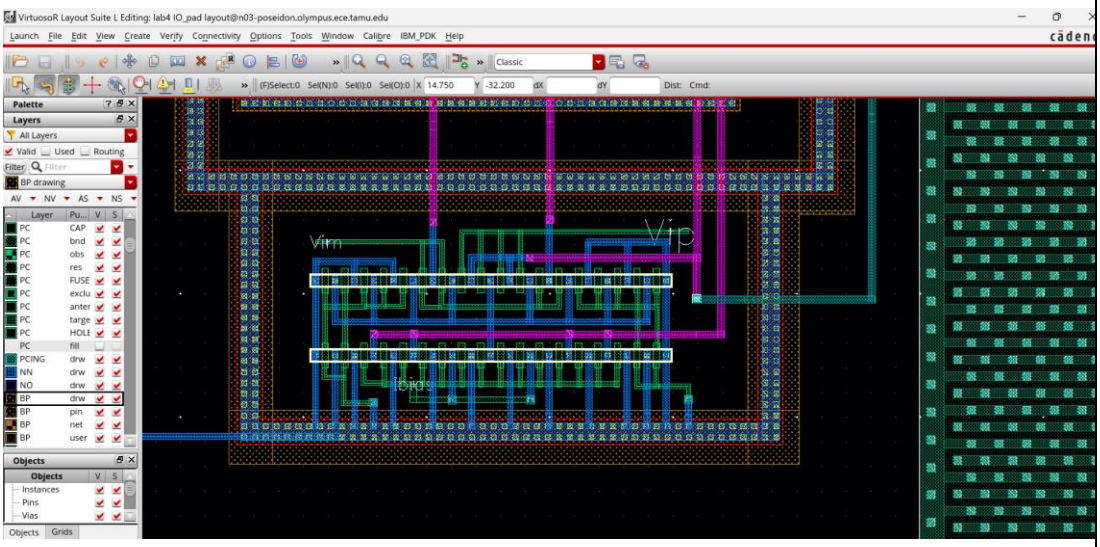


I/O pad

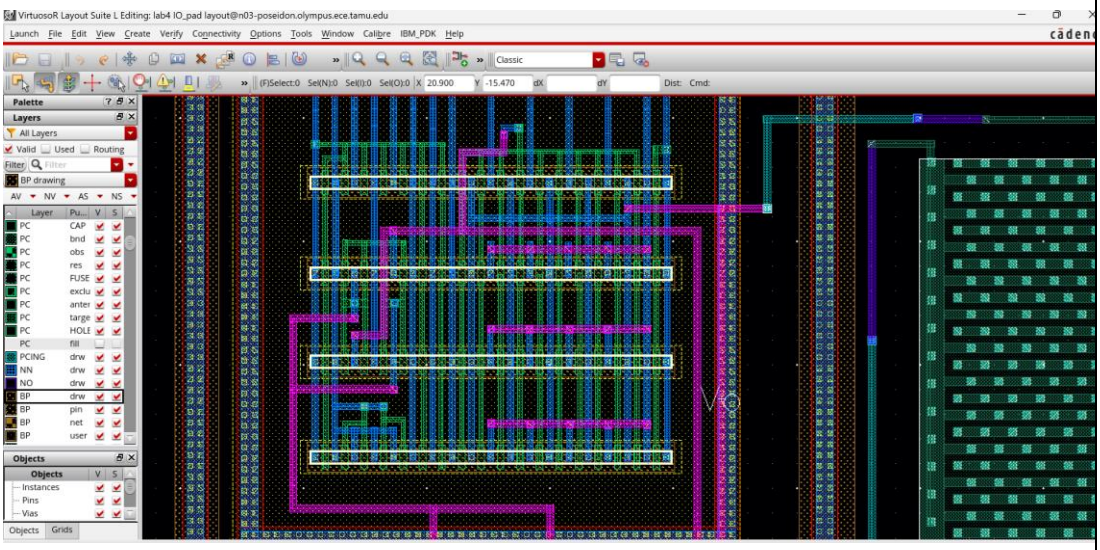
I/O pad



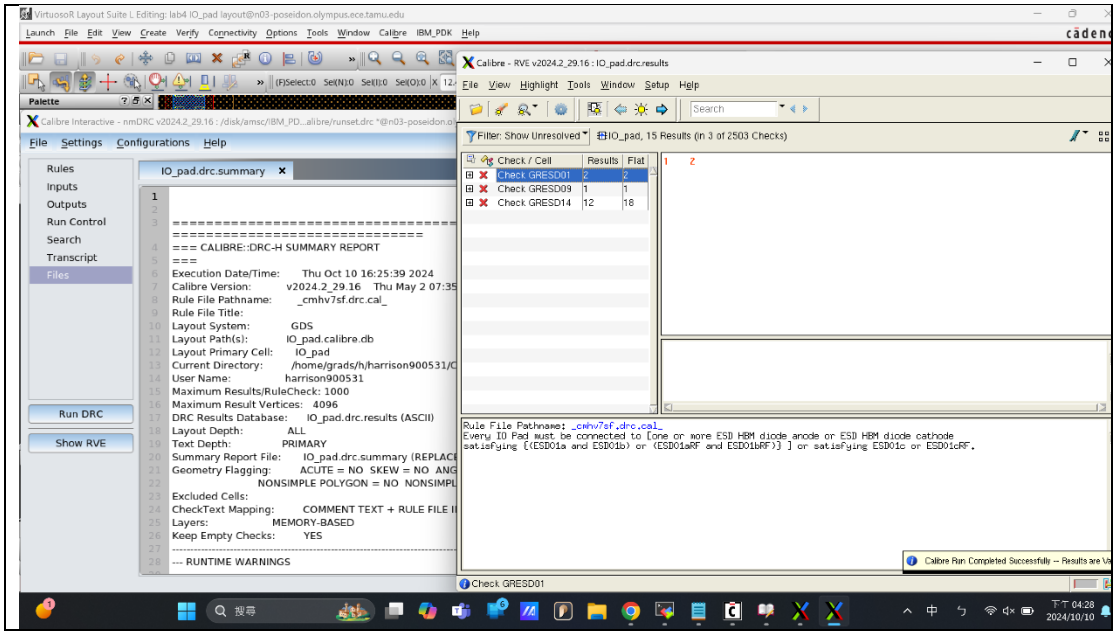
I/O pad (n)



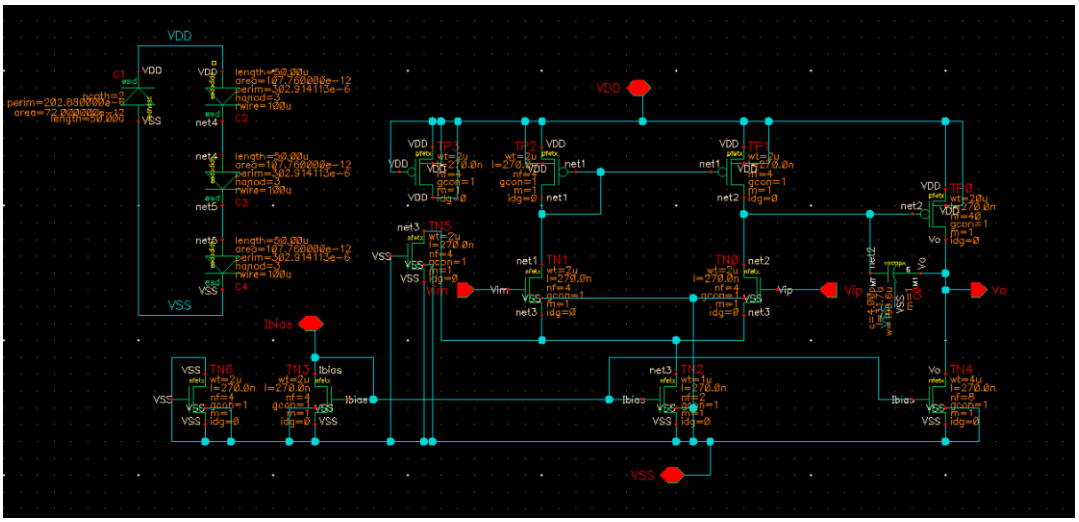
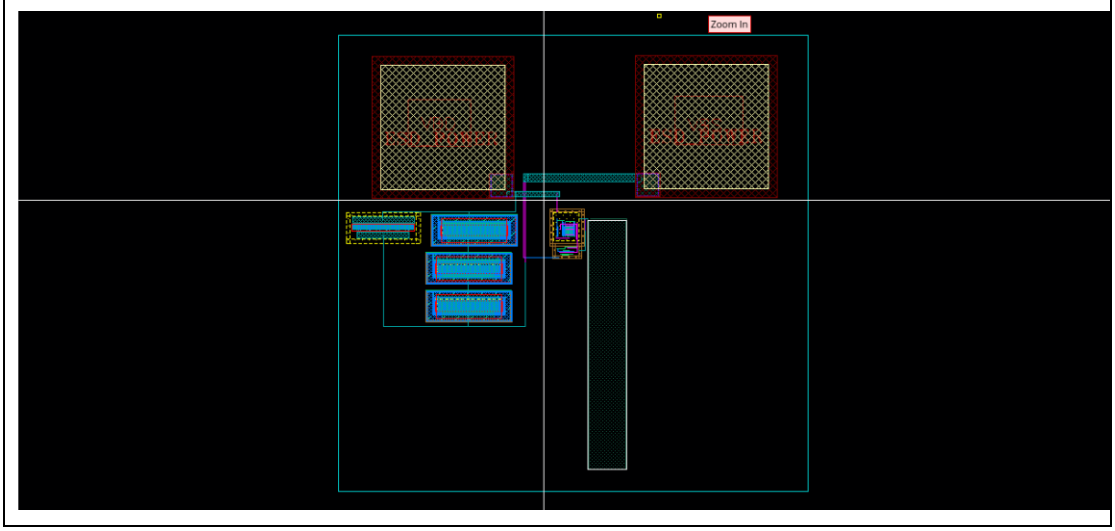
I/O pad (p)

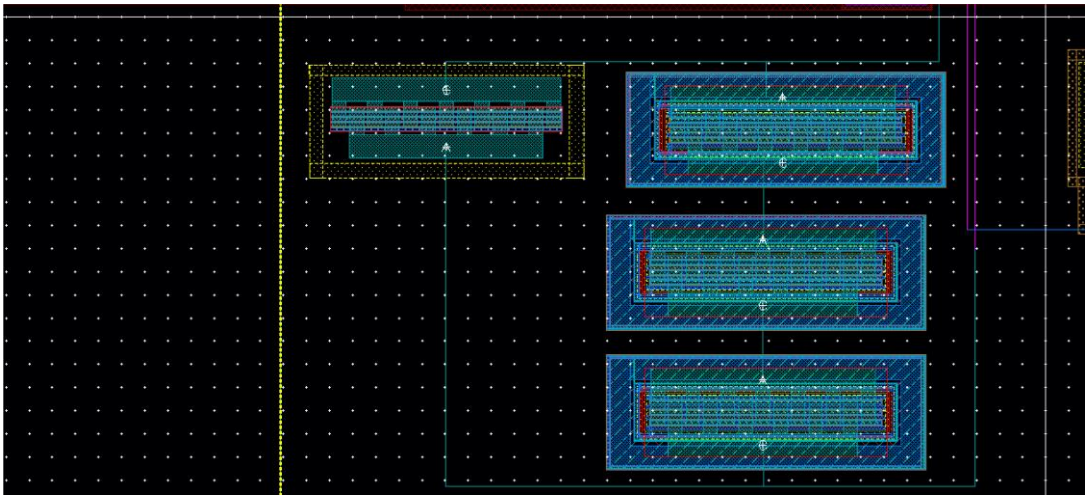


DRC

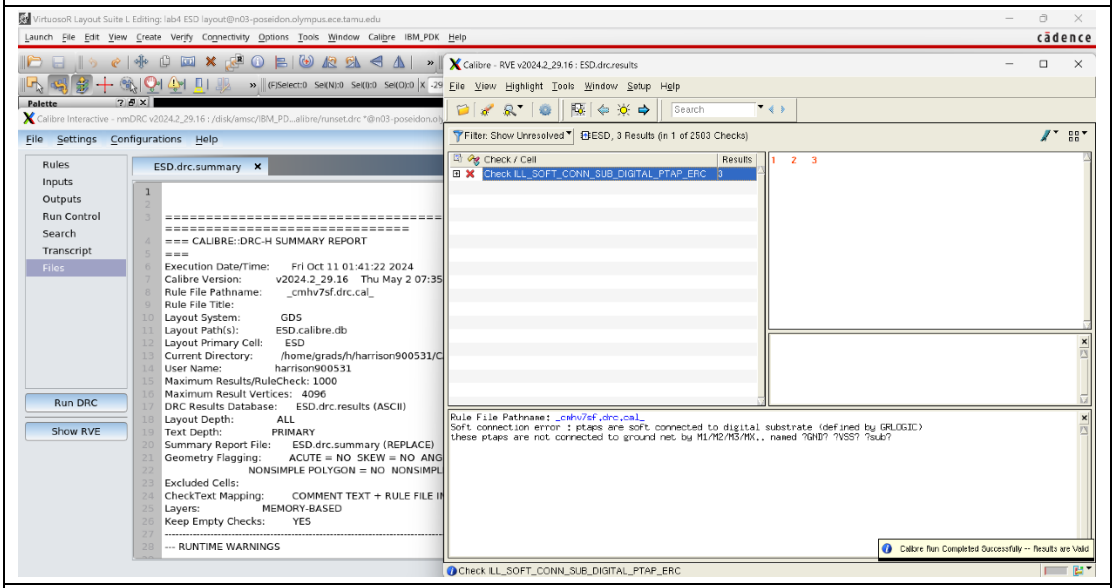


ESD

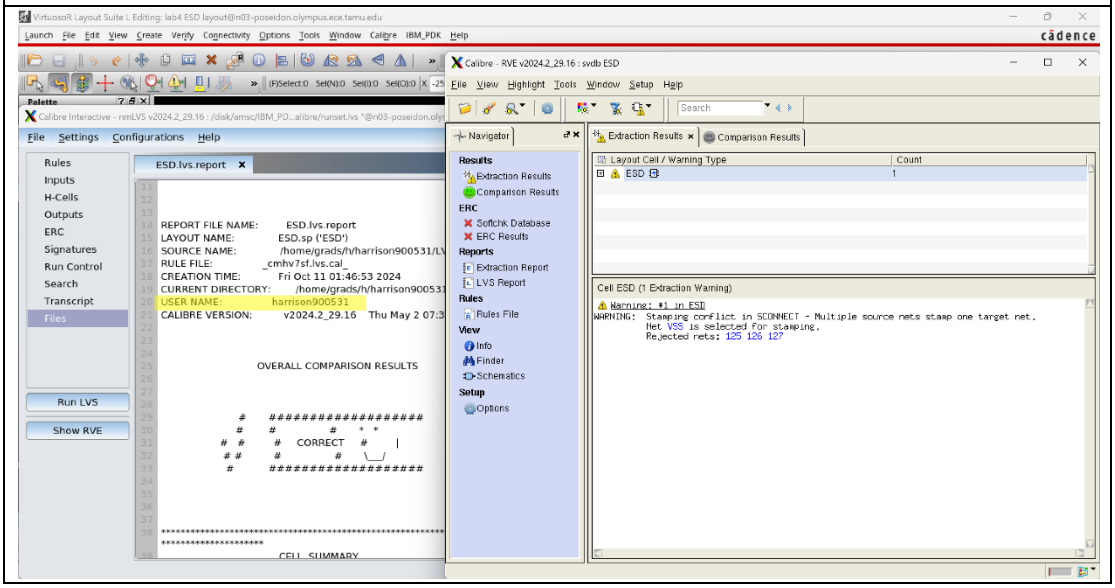
Adding ESD

layout


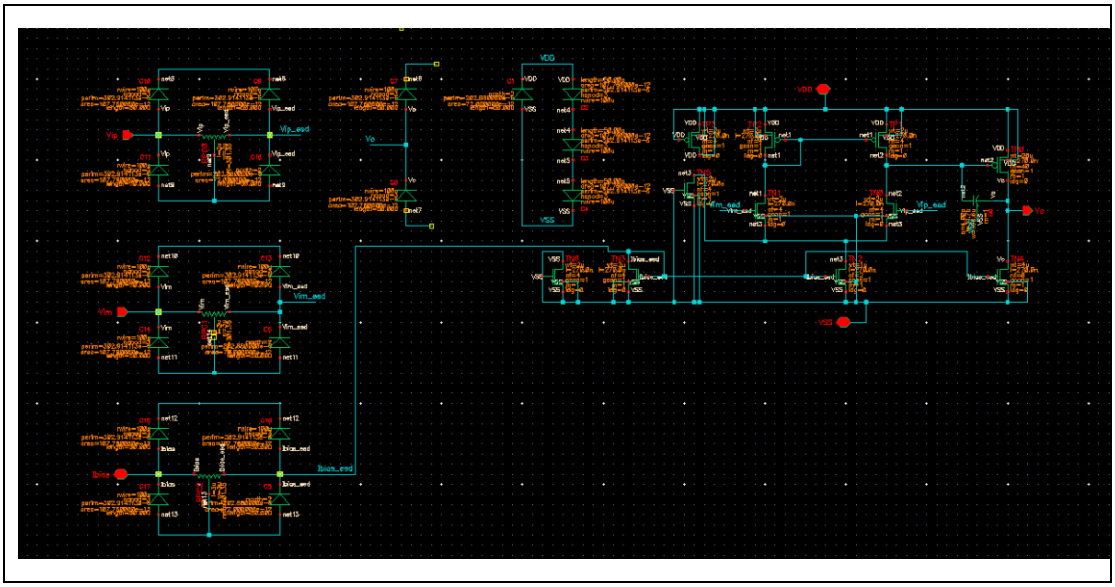


DRC


ESD.drc.summary
=== CALIBRE::DRC-H SUMMARY REPORT ===
Execution Date/Time: Fri Oct 11 01:41:22 2024
Calibre Version: v2024.2_29.16 Thu May 2 07:35
Rule File Pathname: _cmhv7sf.drc.cal_
Layout System: GDS
Layout Path(s): ESD.calibre.db
Layout Primary Cell: ESD
Current Directory: /home/grads/h/harrison900531/C
User Name: harrison900531
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: ESD.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: ESD.drc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANG
NONSIMPLE POLYGON = NO NONSIMPL
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE I
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS
Run DRC
Show RVE
Rule File Pathname: _cmhv7sf.drc.cal_
Soft connection error : ptaps are soft connected to digital substrate (defined by GRLOGIC)
these ptaps are not connected to ground net by M1/M2/M3/MX.. named ?GND? ?VSS? ?sub?
Calibre Run Completed Successfully -- Results are Valid
Check ILL_SOFT_CONN_SUB_DIGITAL_PTAP_ERC

LVS


ESD.lvs.report
REPORT FILE NAME: ESD.lvs.report
LAYOUT NAME: ESD.sp ('ESD')
SOURCE NAME: /home/grads/h/harrison900531/LV
RULE FILE: _cmhv7sf.lvs.cal_
CREATION TIME: Fri Oct 11 01:46:53 2024
CURRENT DIRECTORY: /home/grads/h/harrison900531
USER NAME: harrison900531
CALIBRE VERSION: v2024.2_29.16 Thu May 2 07:3
OVERALL COMPARISON RESULTS
CORRECT
CELL SUMMARY
Run LVS
Show RVE
Extraction Results
Comparison Results
Layout Cell / Warning Type
Count
ESD
Cell ESD (1 Extraction Warning)
Warning: #1 in ESD
WARNING: Stamping conflict in SCONNECT - Multiple source nets stamp one target net.
Net VSS is selected for stamping.
Rejected nets: 125 126 127



Discussion:

After consulting with the teaching assistant about the dummy transistors in the floor plan, I finally resolved my question regarding the absence of two additional rows of dummy transistors at the top and bottom of the floorplan. While it is generally advantageous to include these two rows, it is not essential in this instance (or in typical scenarios); their necessity arises primarily in high-speed circuit applications.

In this lab, I believe we learned more about how to manage a complex circuit. By separating the circuit into multiple steps, we can check the Design Rule Check (DRC) and Layout Versus Schematic (LVS) for each step before proceeding to the next. This approach ensures that we do not confront the entire, massive problem all at once, making it easier to debug and fix the circuit.

Conclusion:

After completing Lab 4, we learned important layout techniques like ESD protection and guard rings, which enhance circuit performance and reliability. ESD protection helps safeguard components from voltage spikes, preventing damage, while guard rings improve matching and reduce interference from external noise. These techniques make the circuit more robust and less affected by environmental factors, ensuring higher accuracy and long-term durability in various applications.