24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab3: Layout Design Techniques

Name: Yu-Hao Chen

UIN:435009528

Section:601

Professor: Aydin Karsilayan

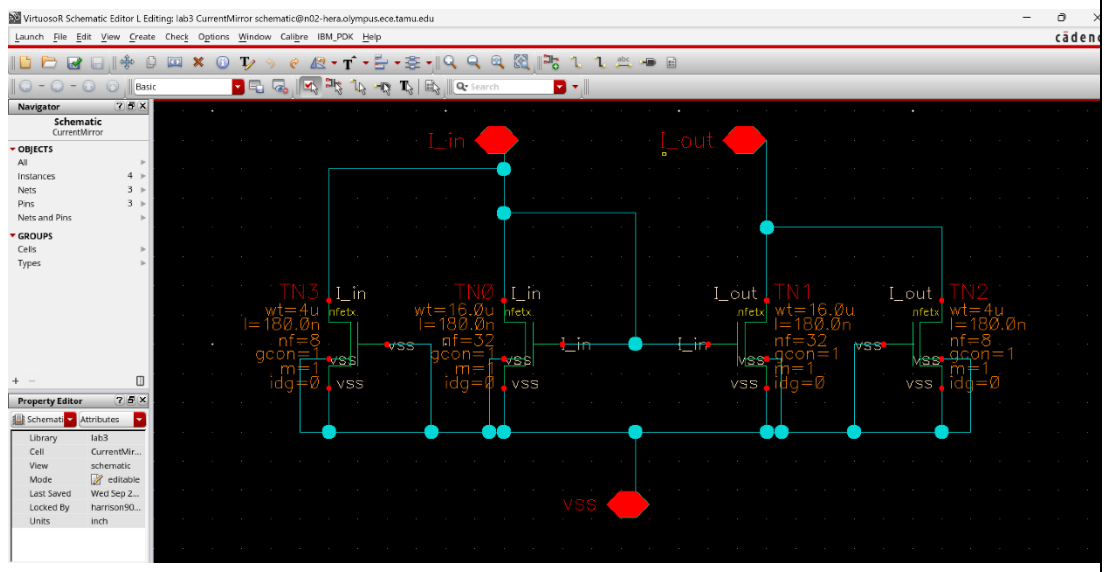
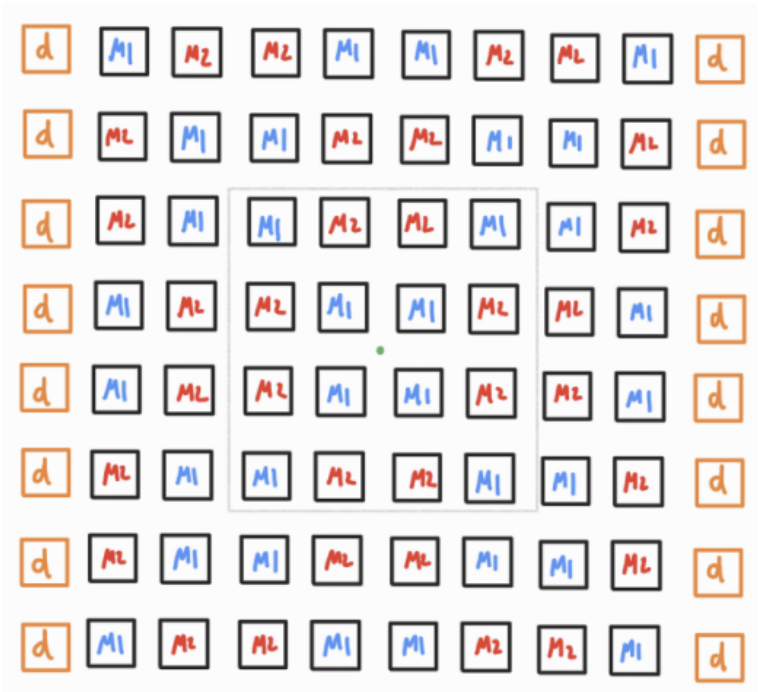
TA: Troy Buhr

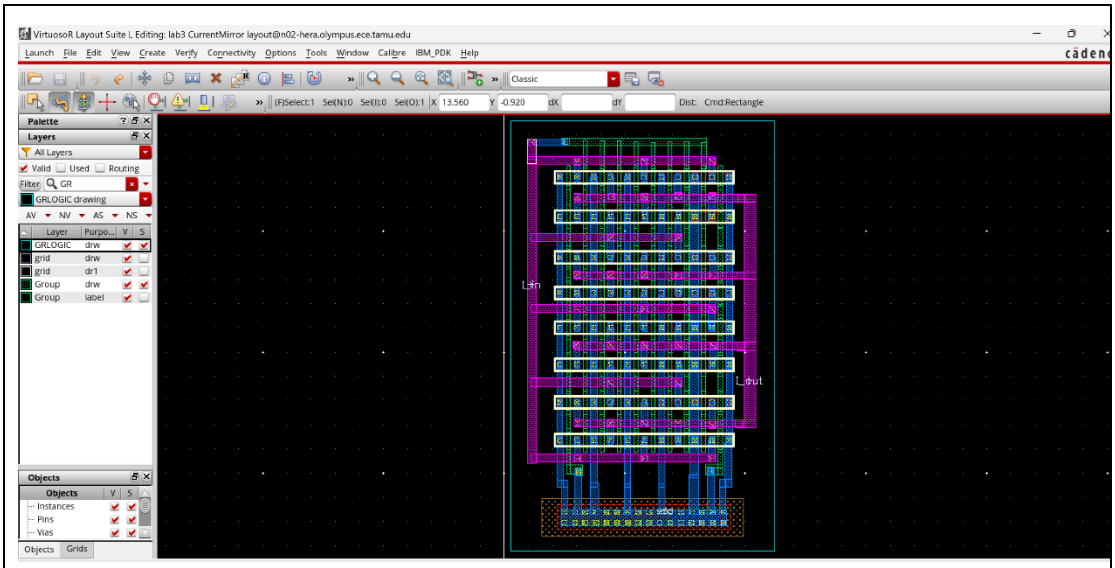
Description:

In this lab, we learn to make a current mirror using layout techniques of matched transistors, also using the layout techniques to make resistors and capacitors. By the floor plan design in pre-lab 3, we can draw the layout of the schematic with common centroid.

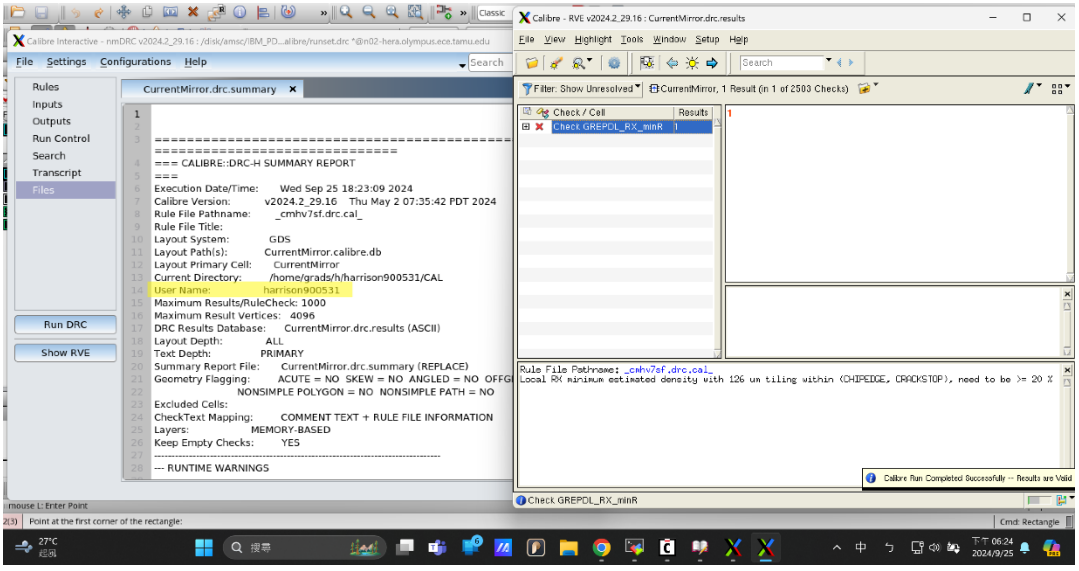
Design & result

1. Simple current mirror

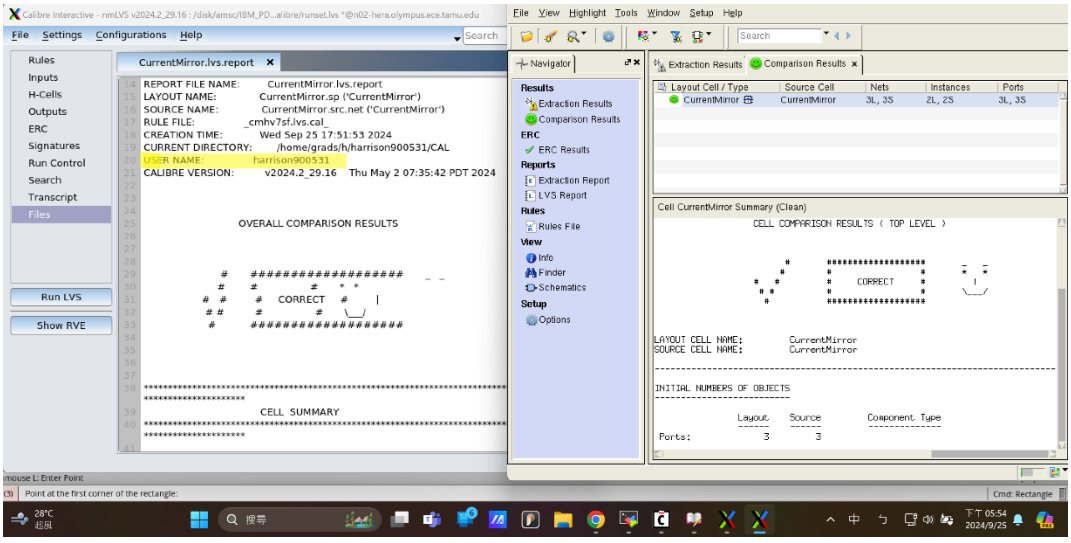
schematic

Floorplan (common centroid)

Layout (common centroid)



DRC

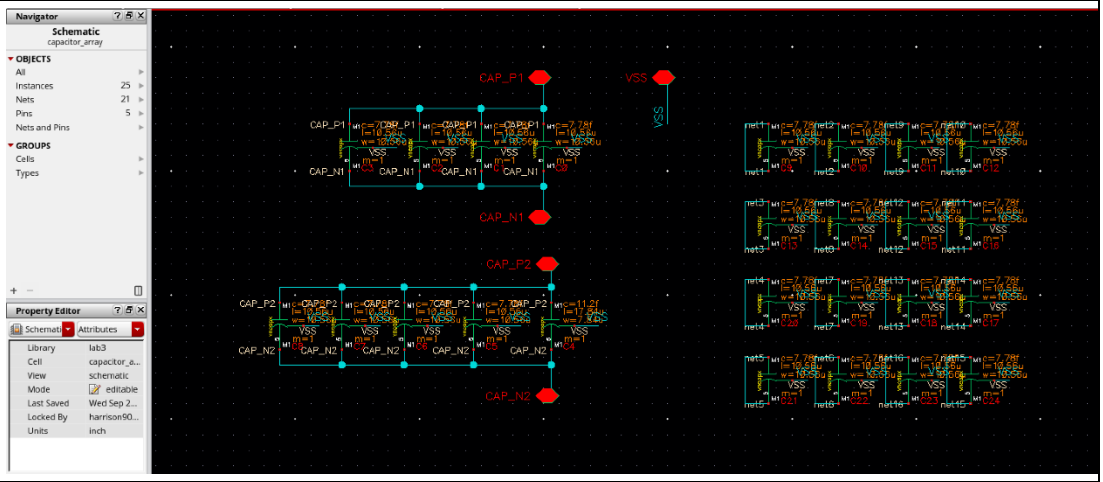


LVS

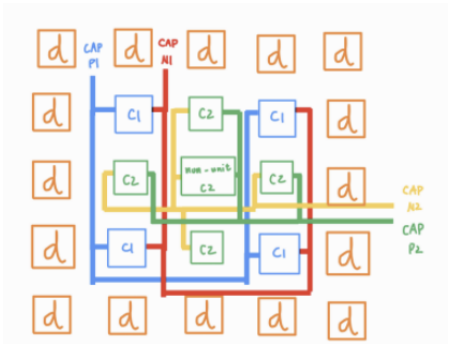


2. MOM capacitor array

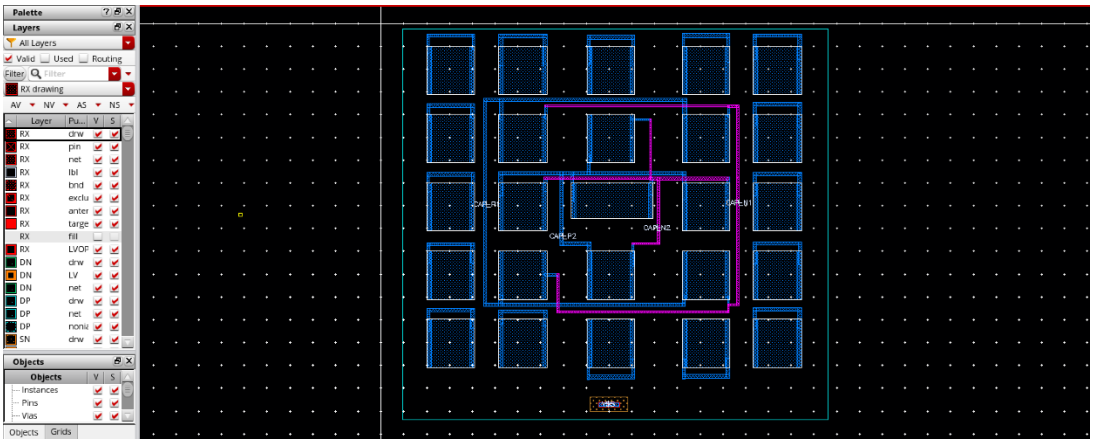
schematic



Floor plan (common centroid)



Layout (common centroid)



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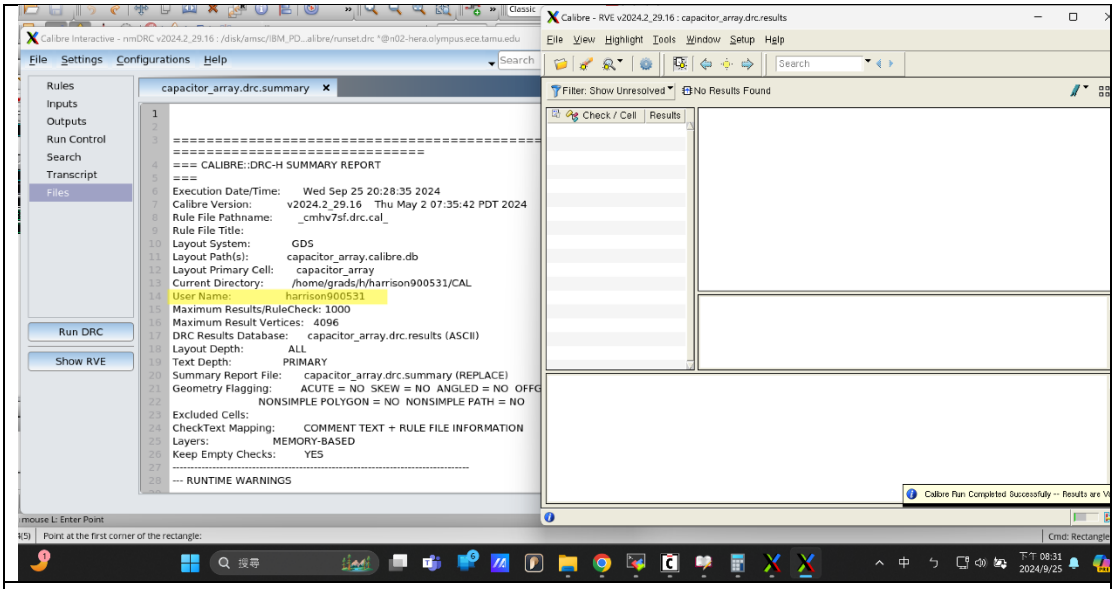

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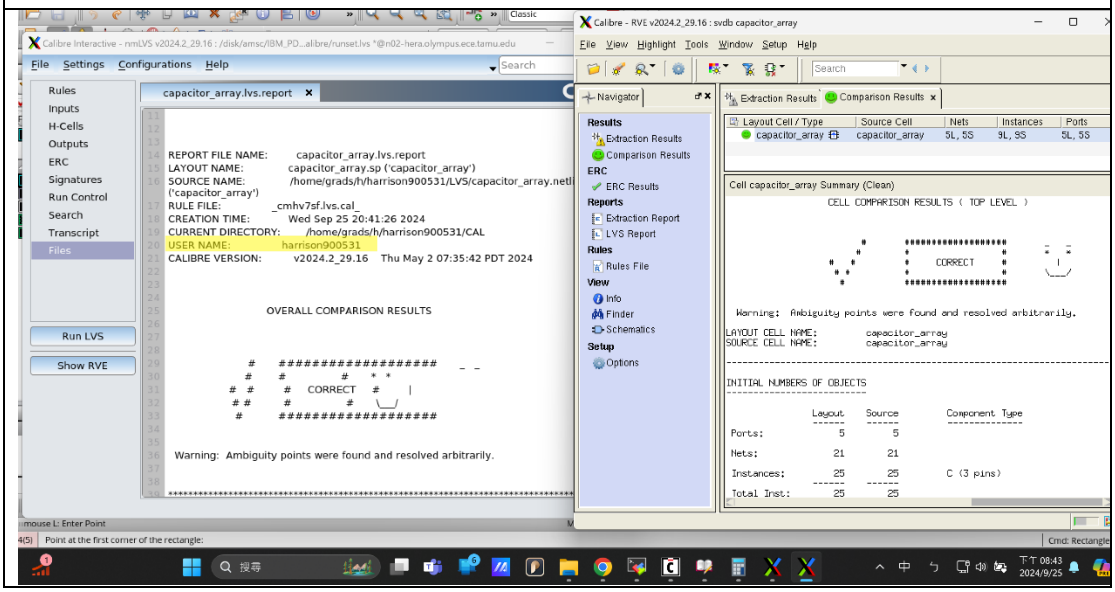
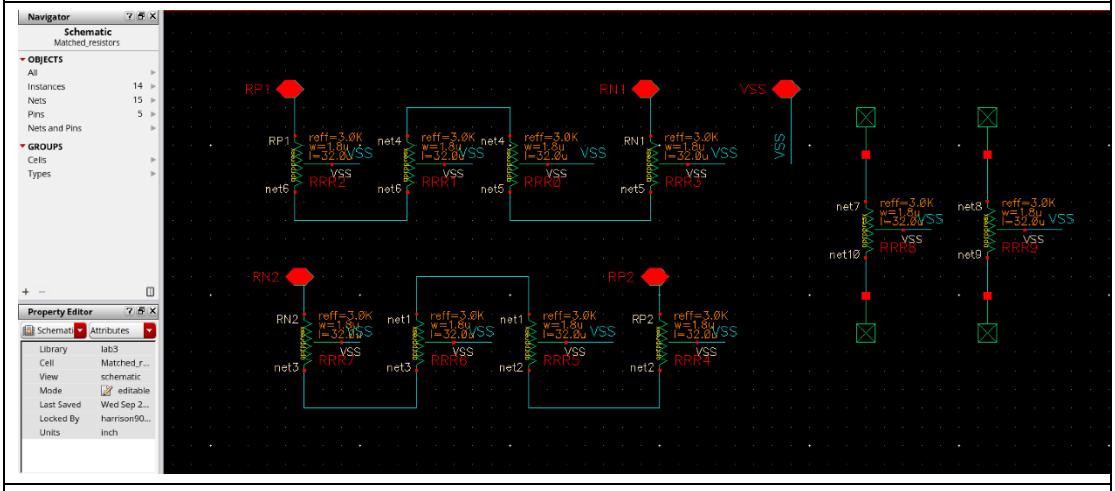
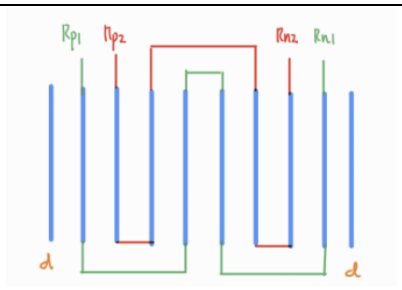


3. Matched polysilicon (oprppresx) resistors

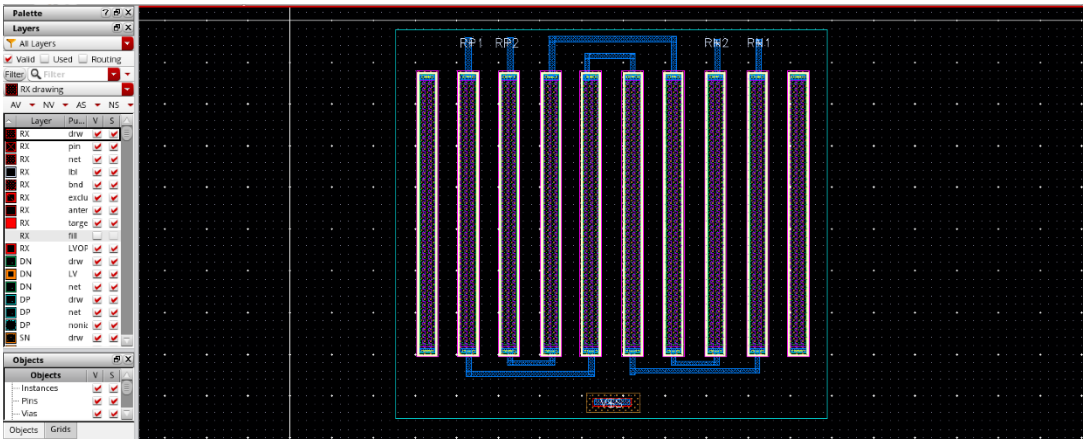
Schematic



Floor plan



Layout



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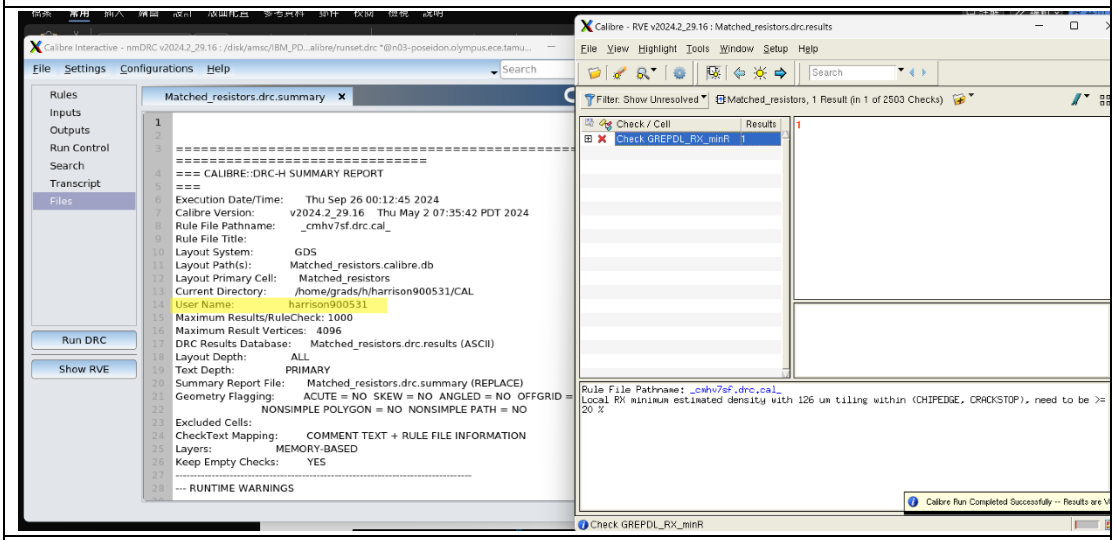
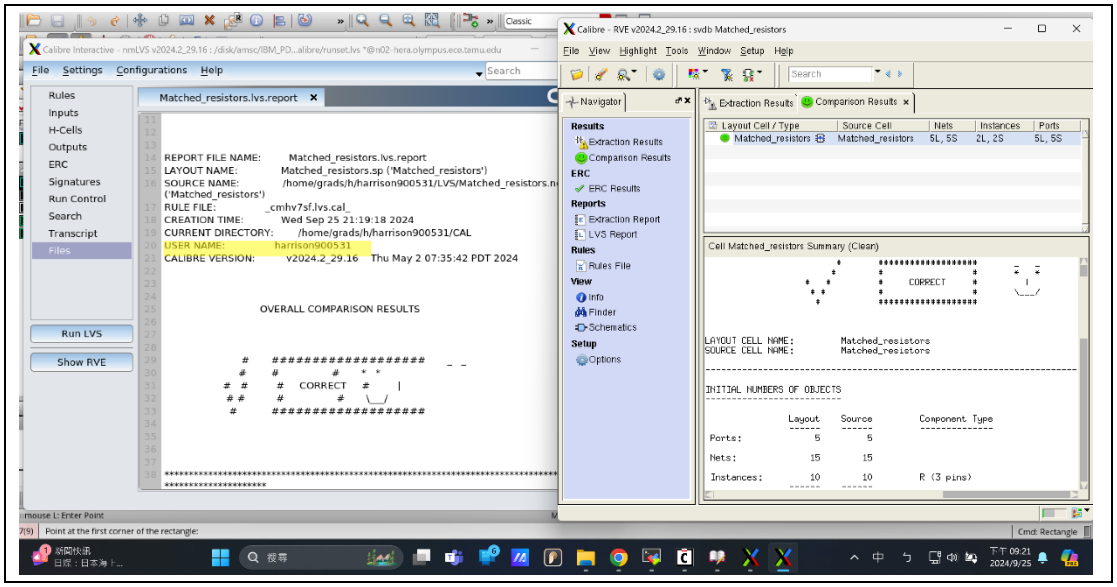


LVS



Discussion:

In the first lab (current mirror), I remember the professor answering my question about whether adding another row of dummy transistors on the top and bottom sides would make the circuit more reliable. However, in this case, the dummy transistors on the first and the last column still ensuring that the second and second-to-last columns of the circuit maintain the same boundary conditions.

In the second lab (capacitor array), the capacitor array illustrates the scenario I mentioned earlier, where dummy components are placed around the 3x3 capacitor array to enhance the circuit's reliability.

In the last lab (resistors), I adjusted the width (W) and length (L) of the resistor from the values specified in the prelab. I discovered that using the hand-calculated values (W = 1.8 µm, which is ten times 180 nm, and L = 32.54 µm) resulted in an actual resistance of 3.05 kΩ, slightly larger than the target of 3 kΩ. Consequently, I modified my length to 32 µm, which make the resistor's value 3 kΩ.

Conclusion:

After completing Lab 3, we learned how to use layout techniques to create matched polysilicon (oprppresx) resistors, MOM capacitor array, and simple current mirror. We learned how to create a common centroid floor plan for the layout design, which enhances the circuit's robustness against variations. Additionally, we utilized dummy structures to ensure that all elements in the circuit have the same boundary conditions. In conclusion, these techniques makes the circuit more reliable and the matching between each component better.