24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab7: Frequency Response of Inverting Amplifiers

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Section:601

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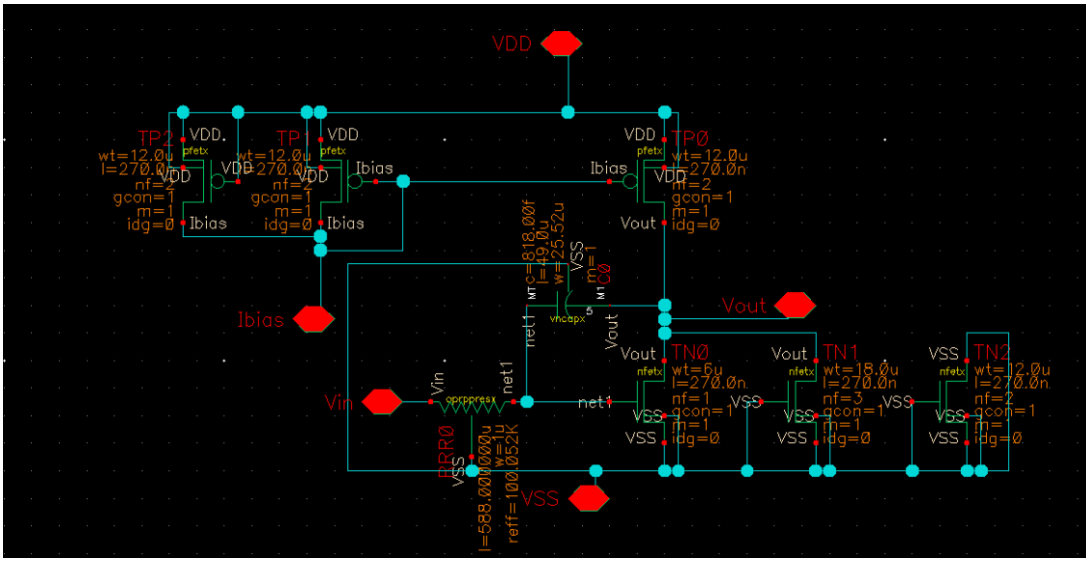
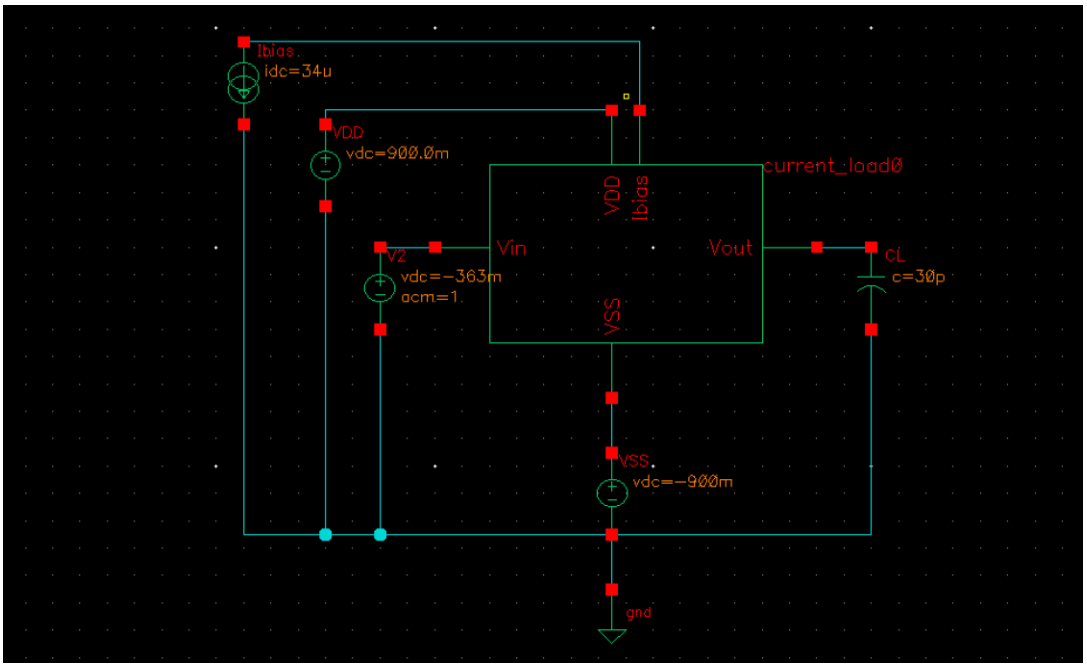
TA: Troy Buhr

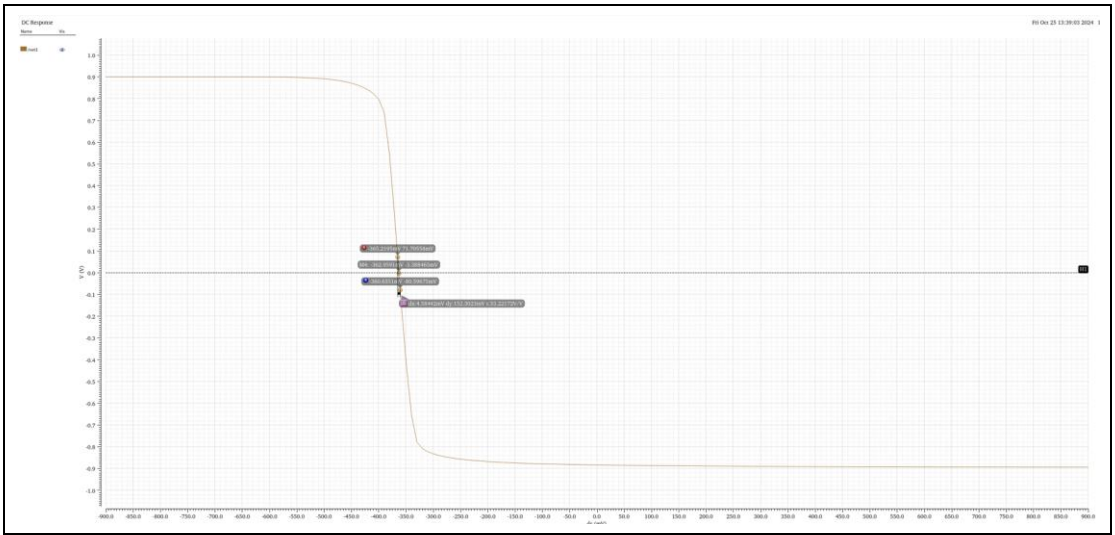
Description:

Lab 7 emphasizes the importance of analyzing and designing inverting amplifiers, Inverting amplifiers are essential components in electronic circuit design, serving key roles in applications such as gain stages in operational amplifiers and NOT gates in digital circuits. Understanding their frequency response is crucial for designing circuits that function reliably across different frequencies.

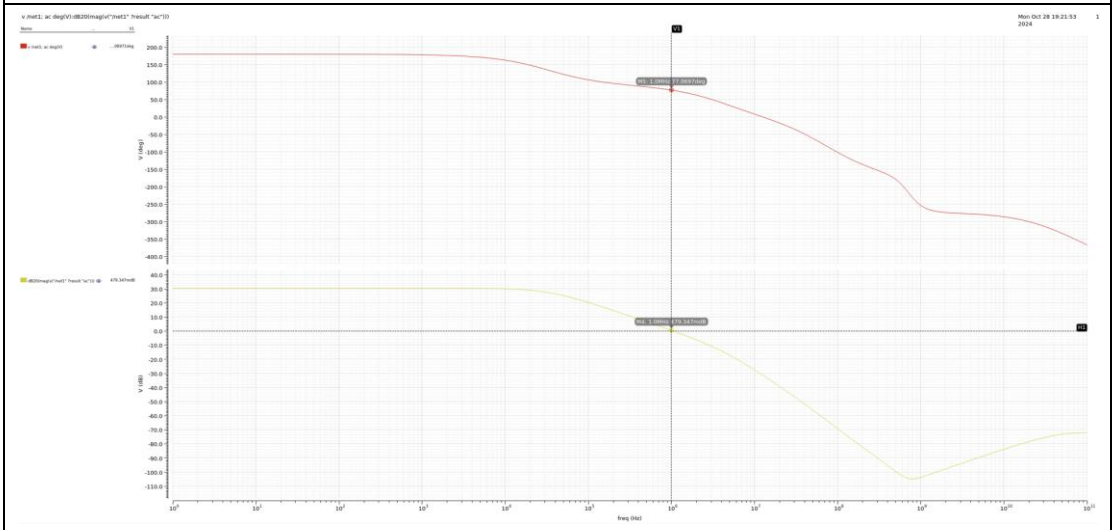
Design & result

a) Current mirror load inverter

schematic

testbench

DC sweep

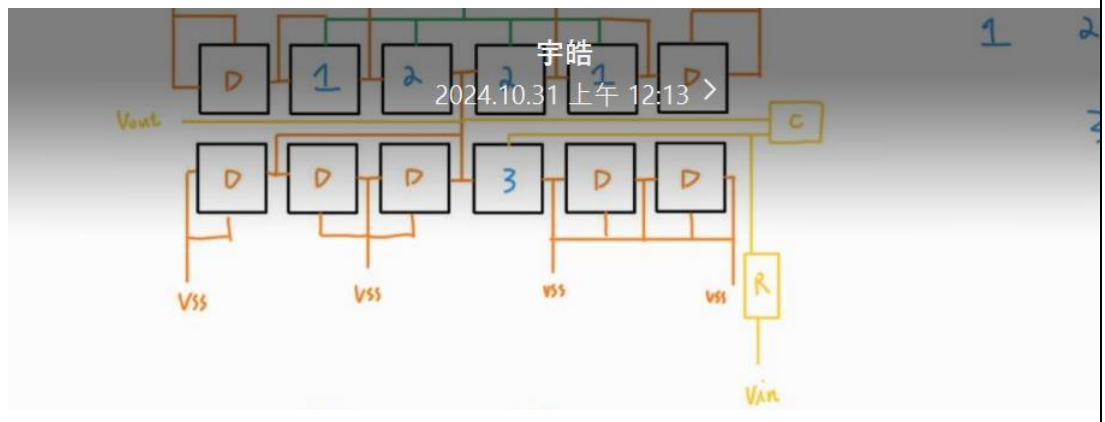


AC Freq

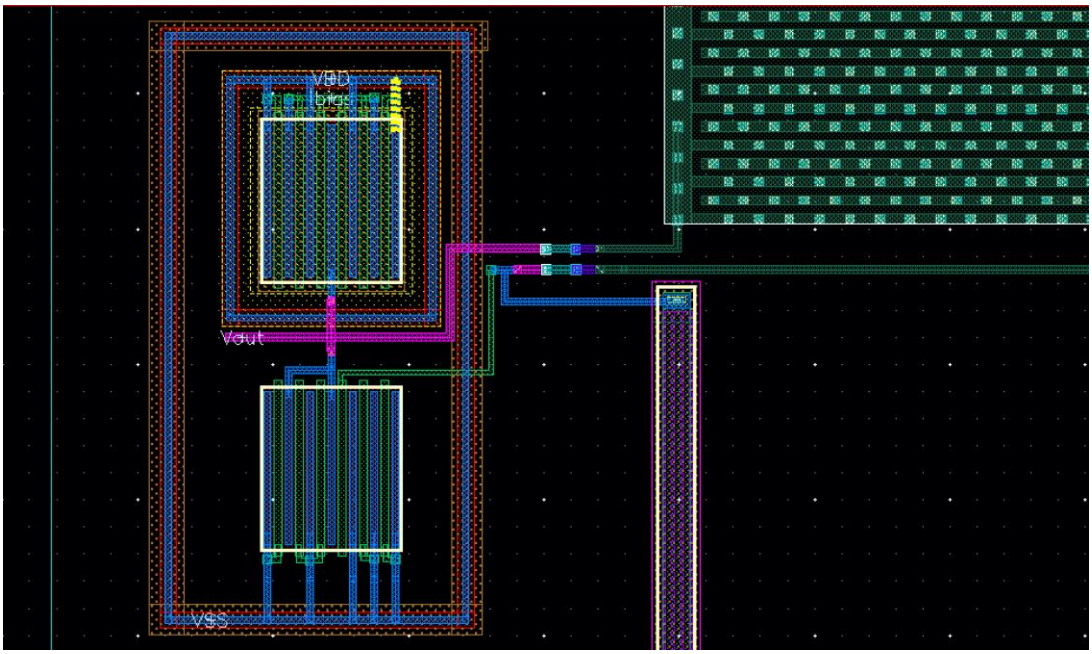


- Phase margin = 180 – phase shift -> phase margin = 77 phase shift = 103

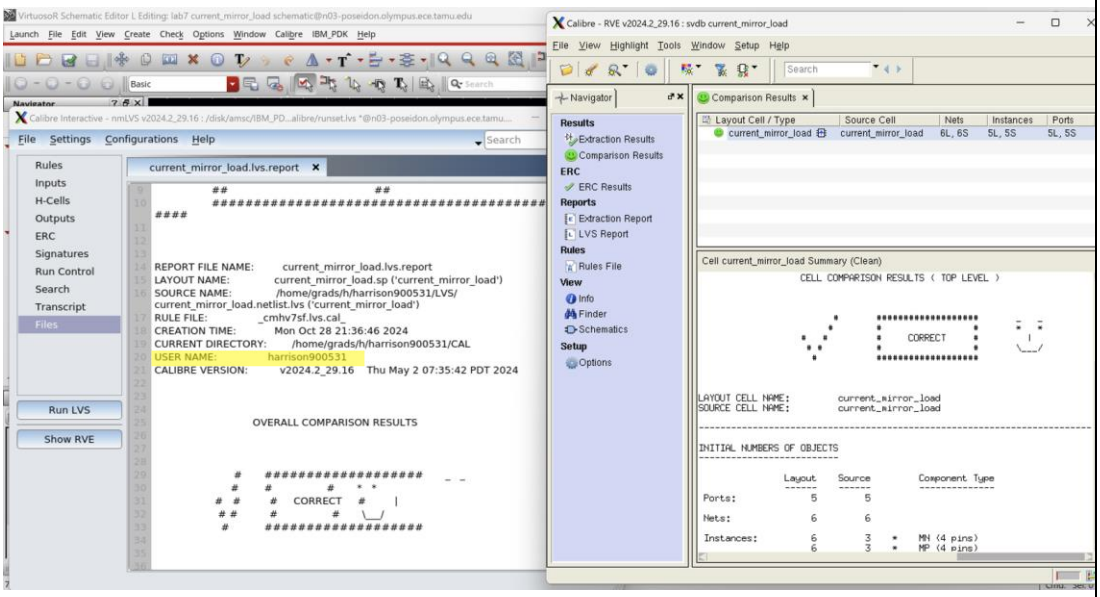
Floor Plan



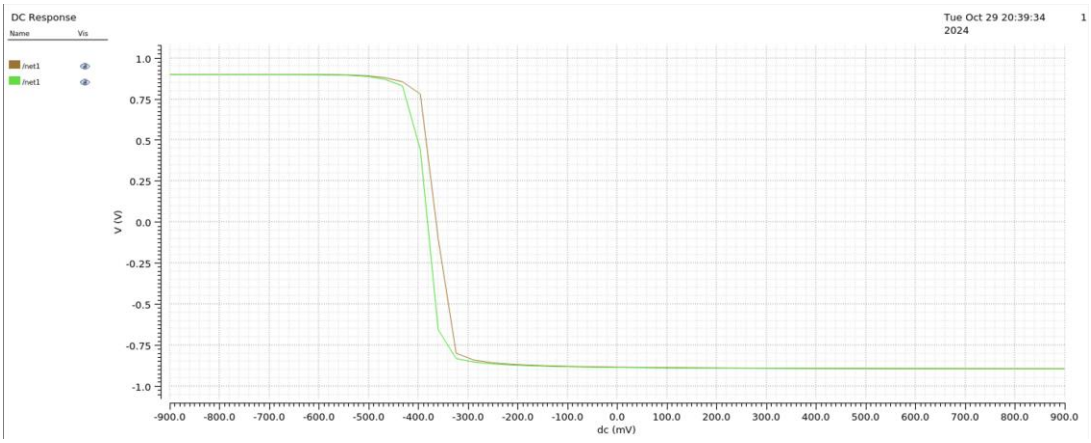
Layout



LVS



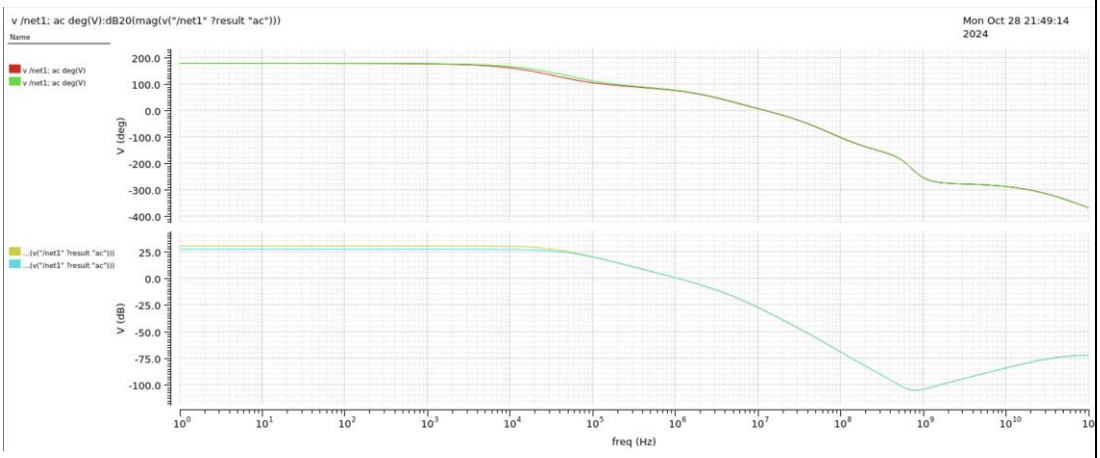
Post layout



Red line: schematic

Green line: layout

Post layout



Red line: schematic phase

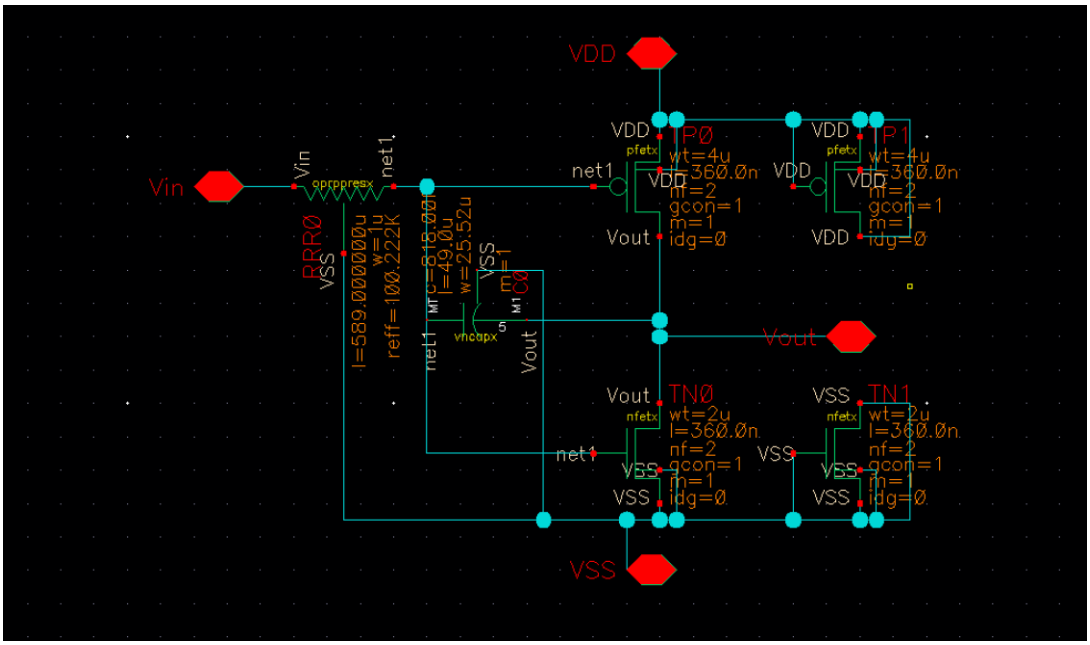
Green line: layout phase dB

Yellow line: schematic AC gain dB

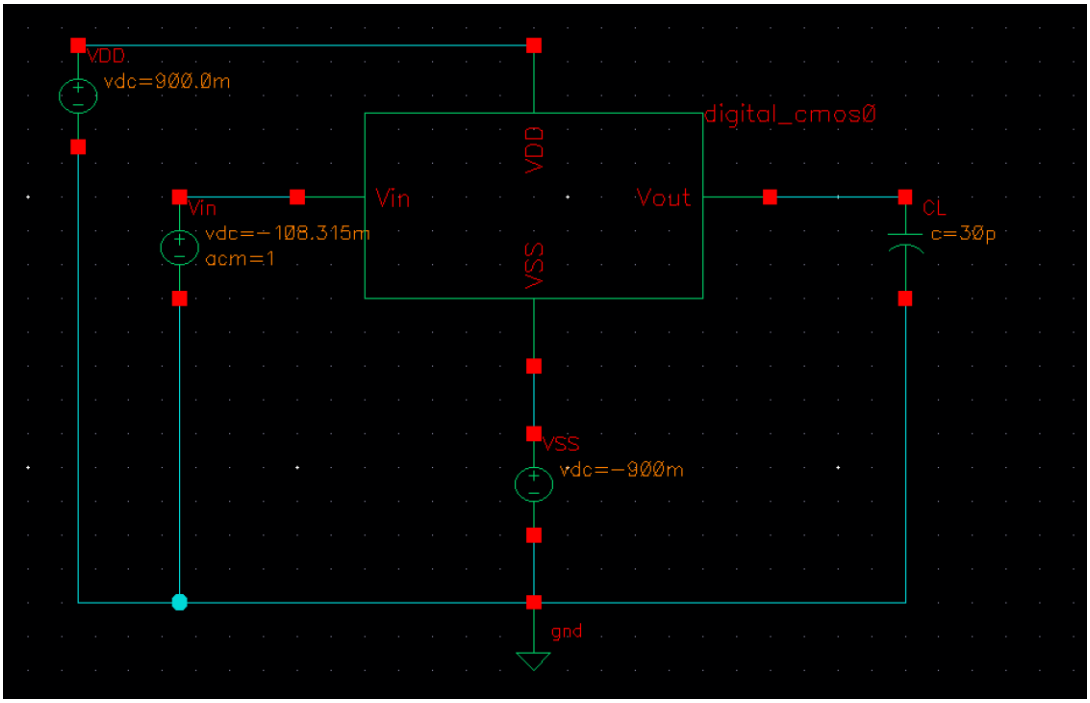
Blue line: layout AC gain dB

b) Digital CMOS inverter

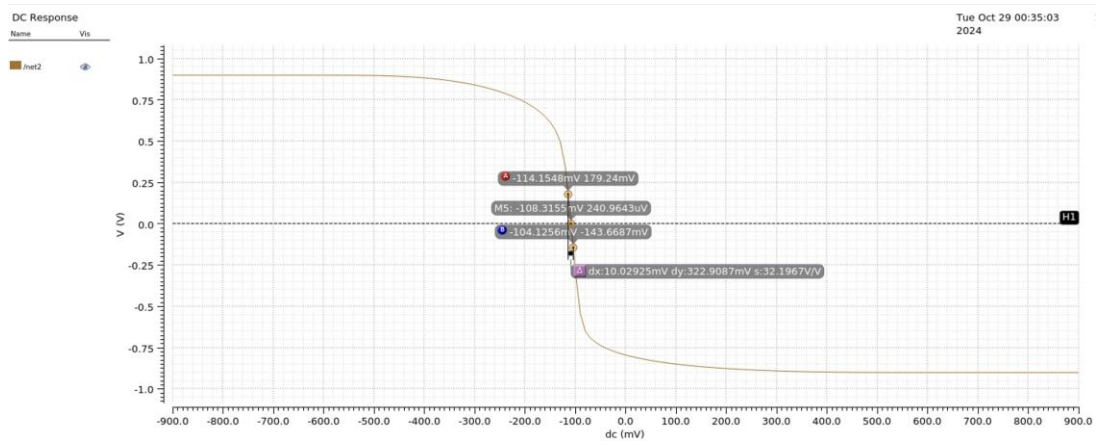
schematic



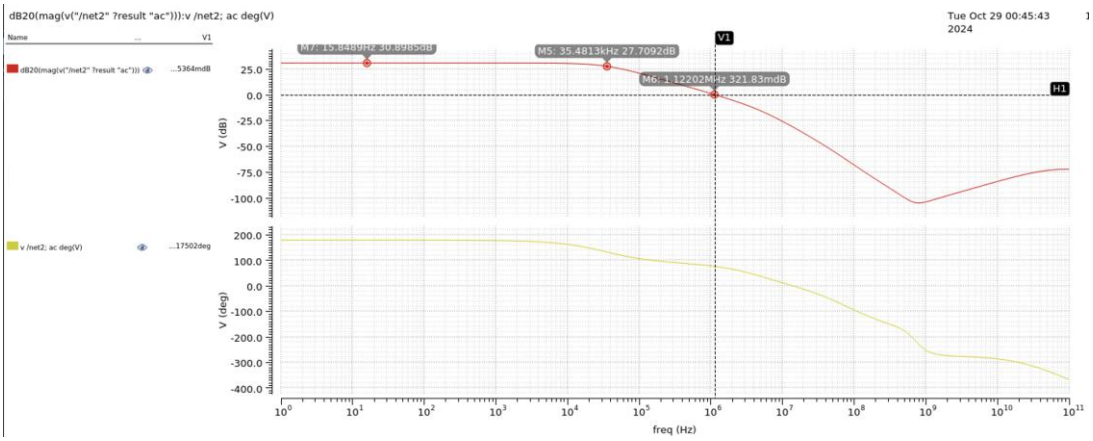
testbench



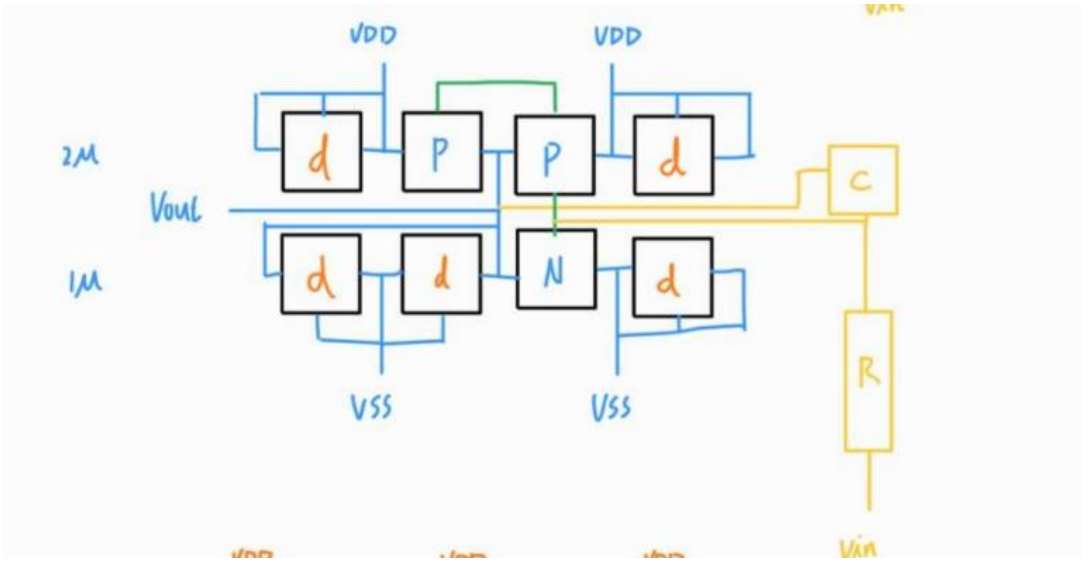
DC sweep



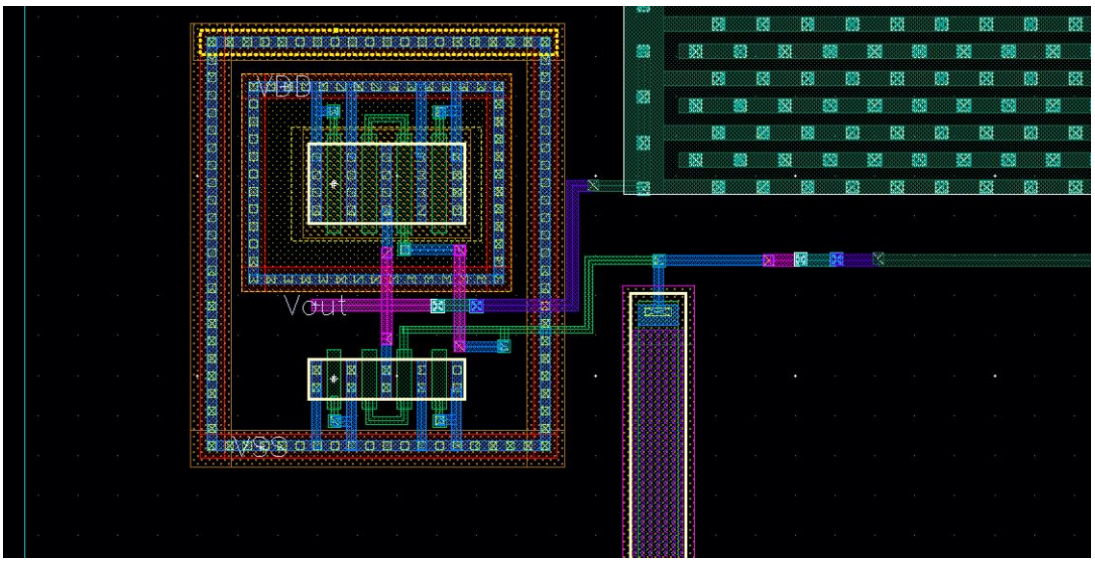
AC Freq



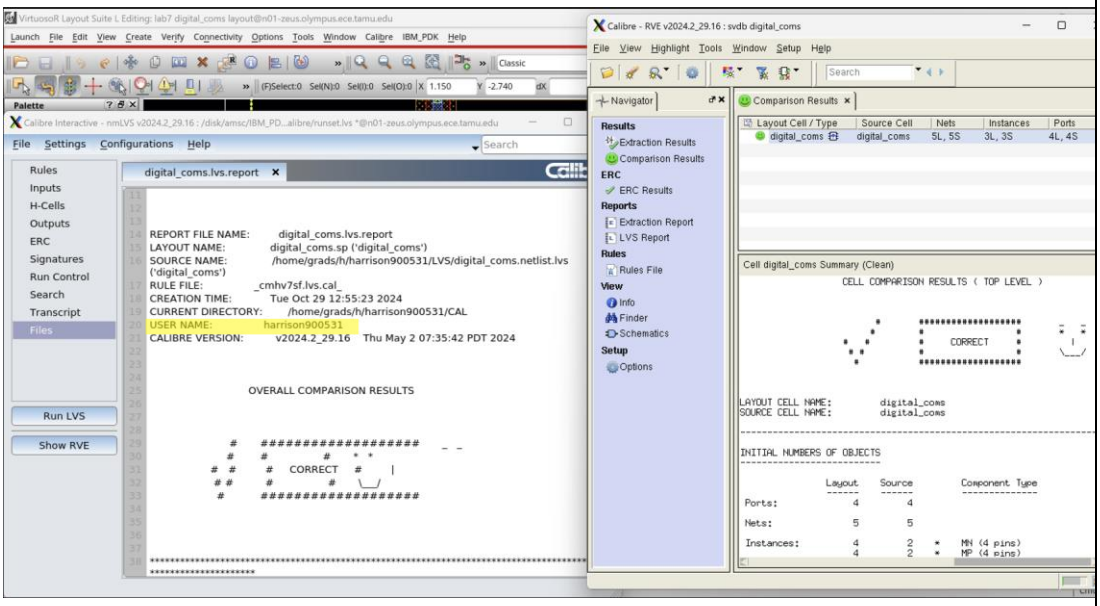
Floor Plan



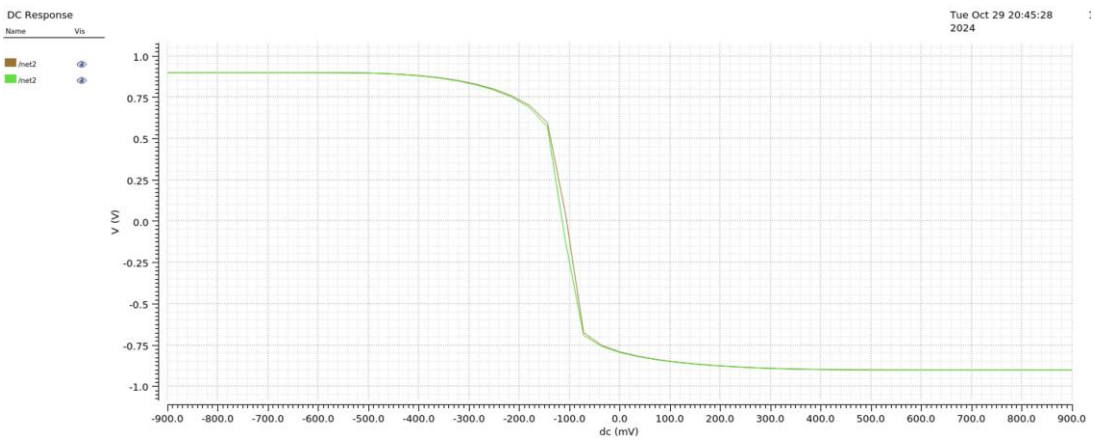
Layout



LVS



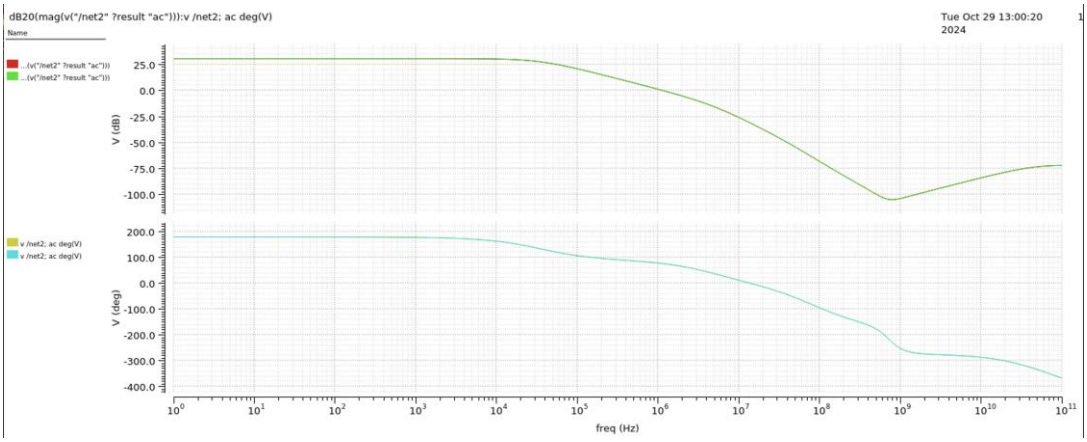
Post layout



Red line: schematic

Green line: layout

Post layout



Red line: schematic AC gain dB

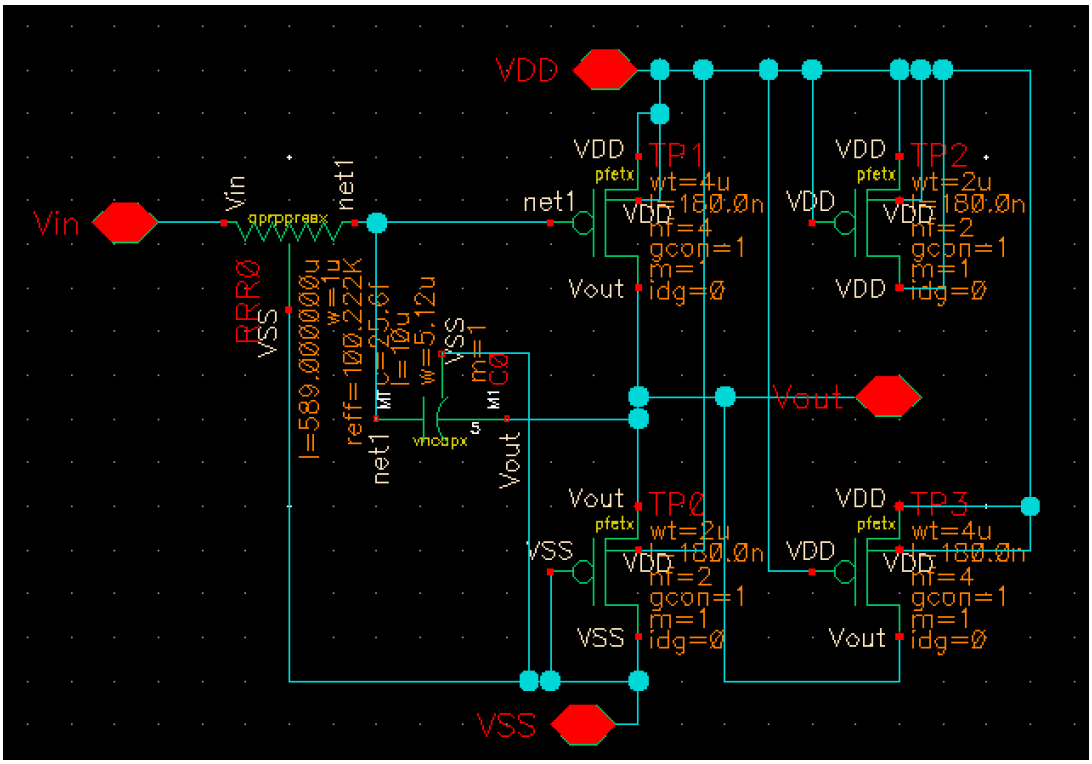
Green line: layout AC gain dB

Yellow line: schematic phase

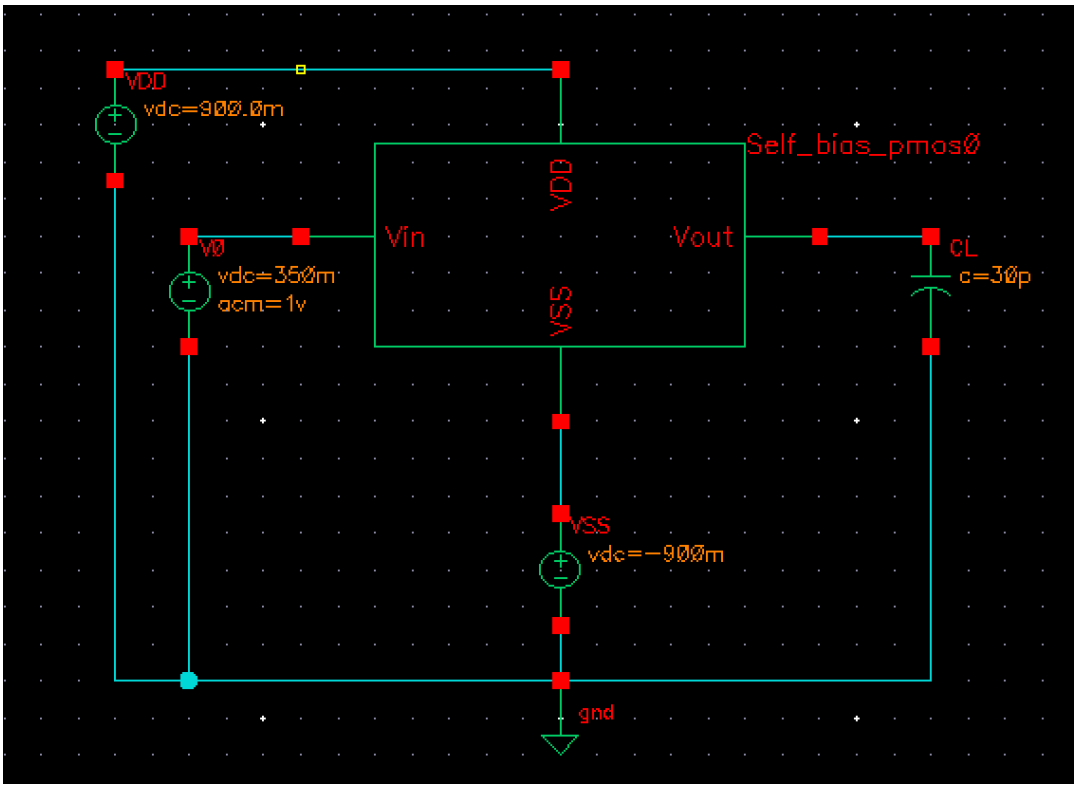
Blue line: layout phase

c)

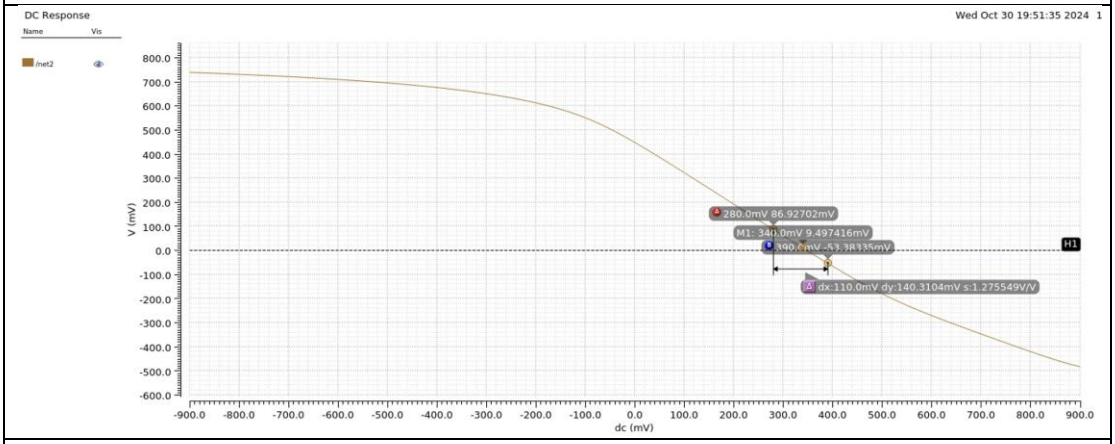
schematic



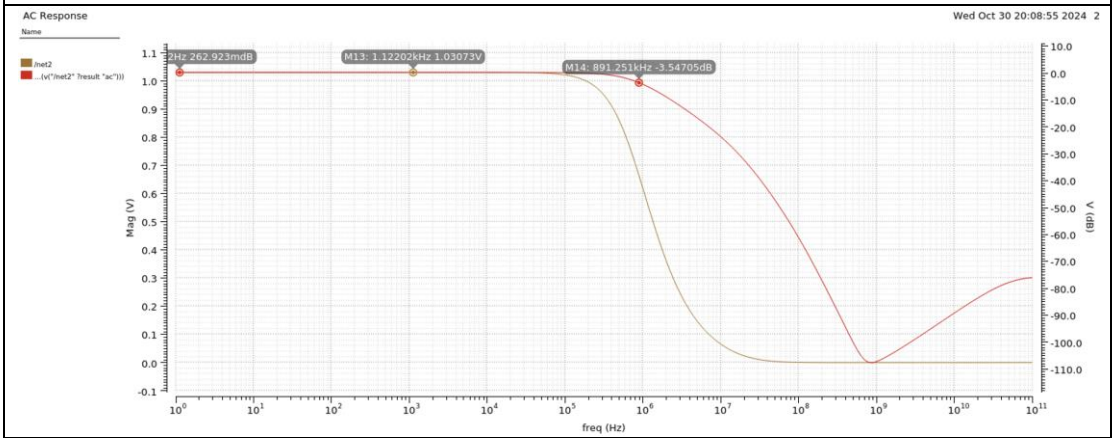
testbench



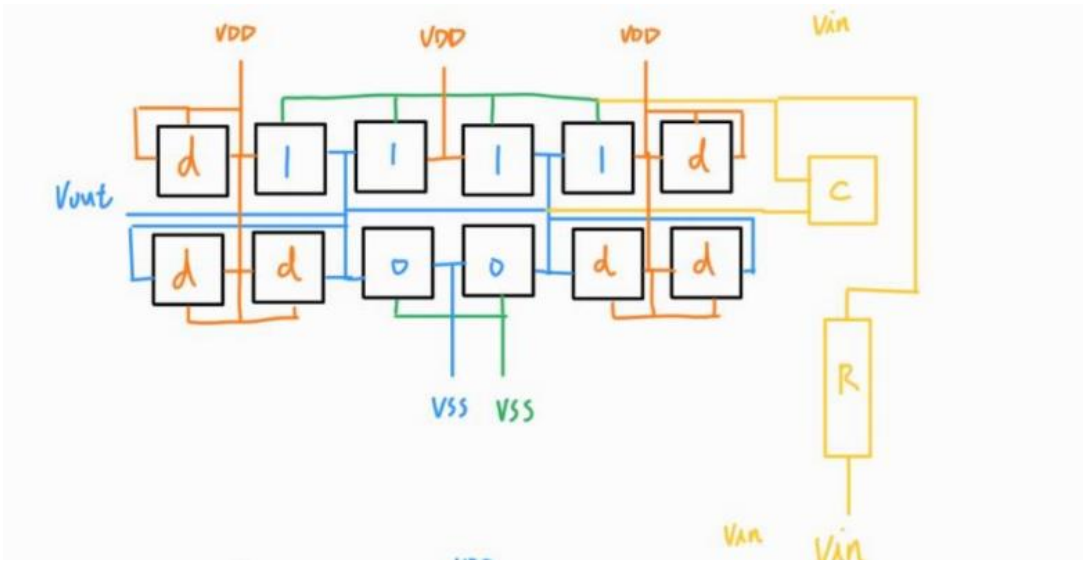
DC sweep



AC Freq



Floor Plan


VDD
VDD
VDD
Vin
Vout
d
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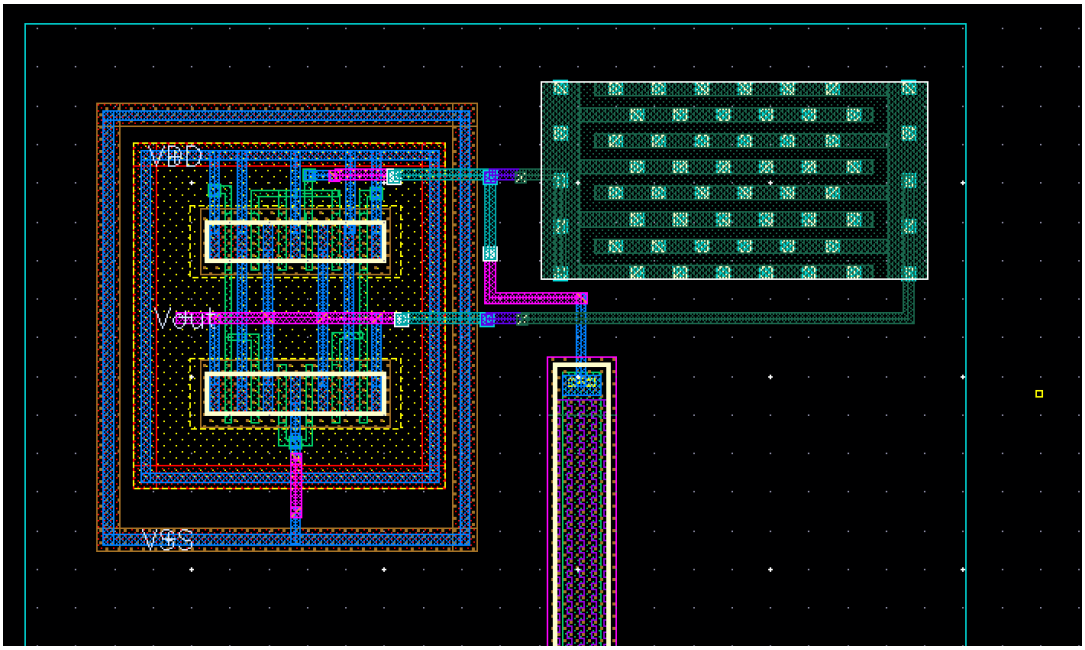
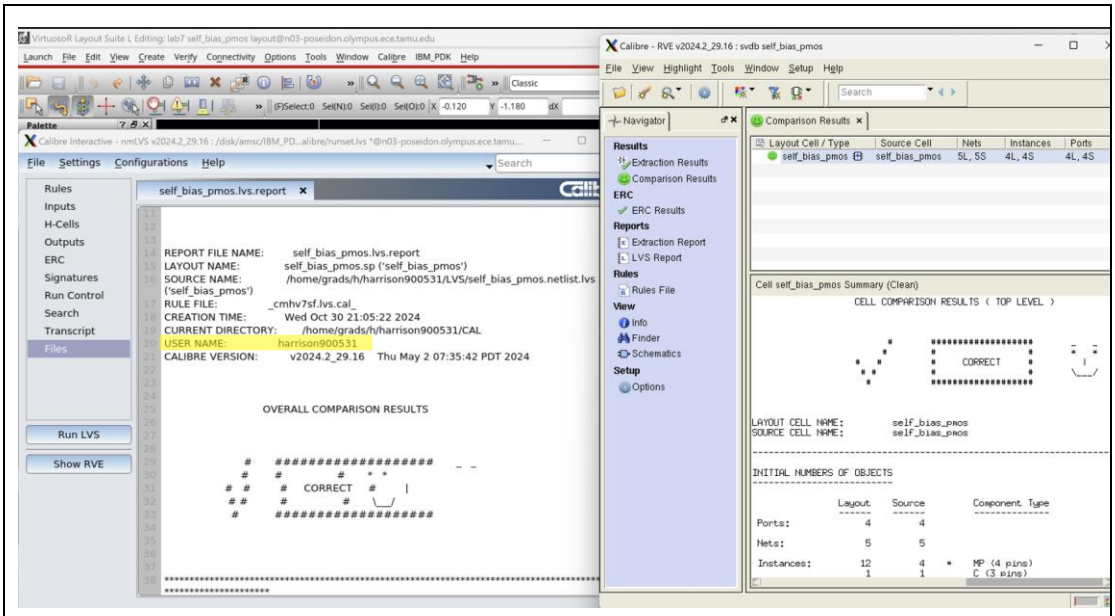
l
l
d
C
d
d
o
o
d
d
R
VSS
VSS
Vin
Vin

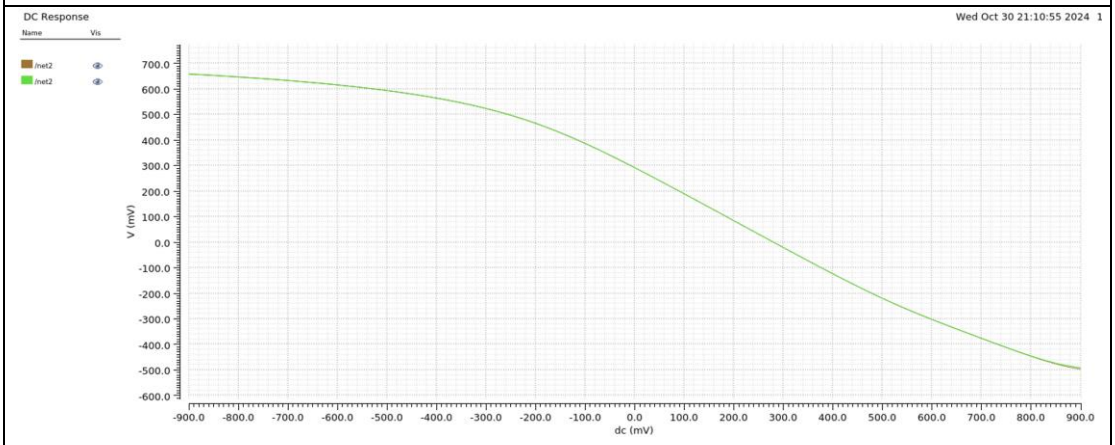
Layout


VDD
Vout
VSS

LVS



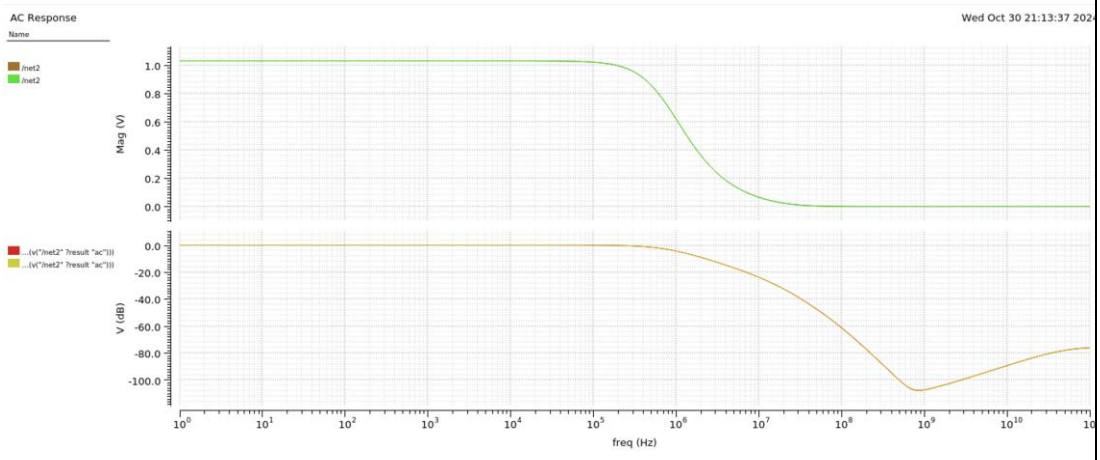
Post layout



Brown line: schematic

Green line: layout

Post layout



Brown line: schematic AC gain

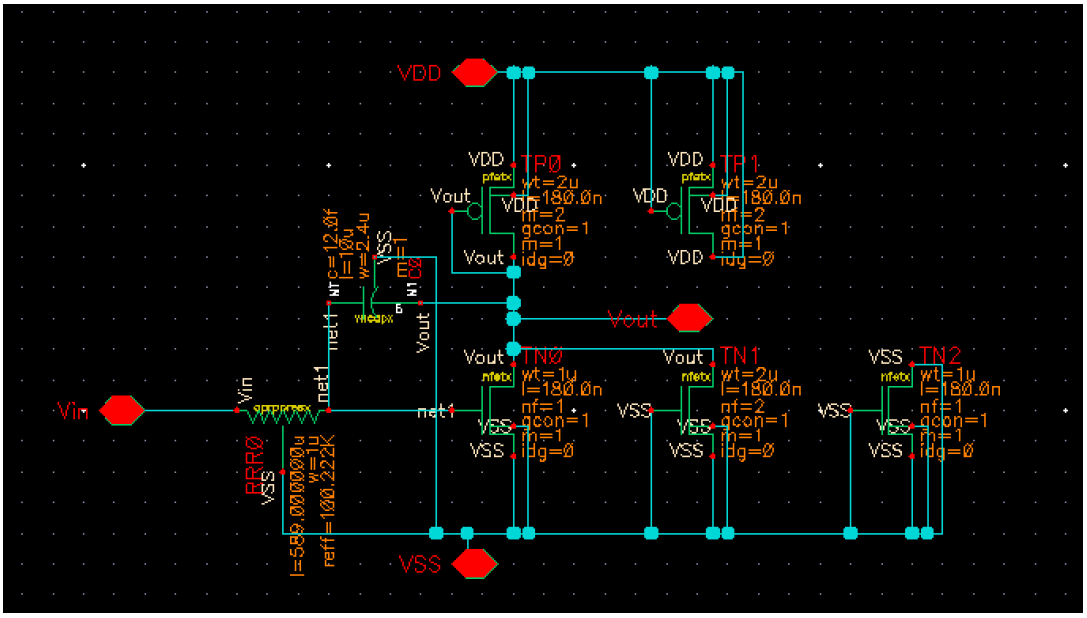
Green line: layout AC gain

Red line: schematic AC gain dB

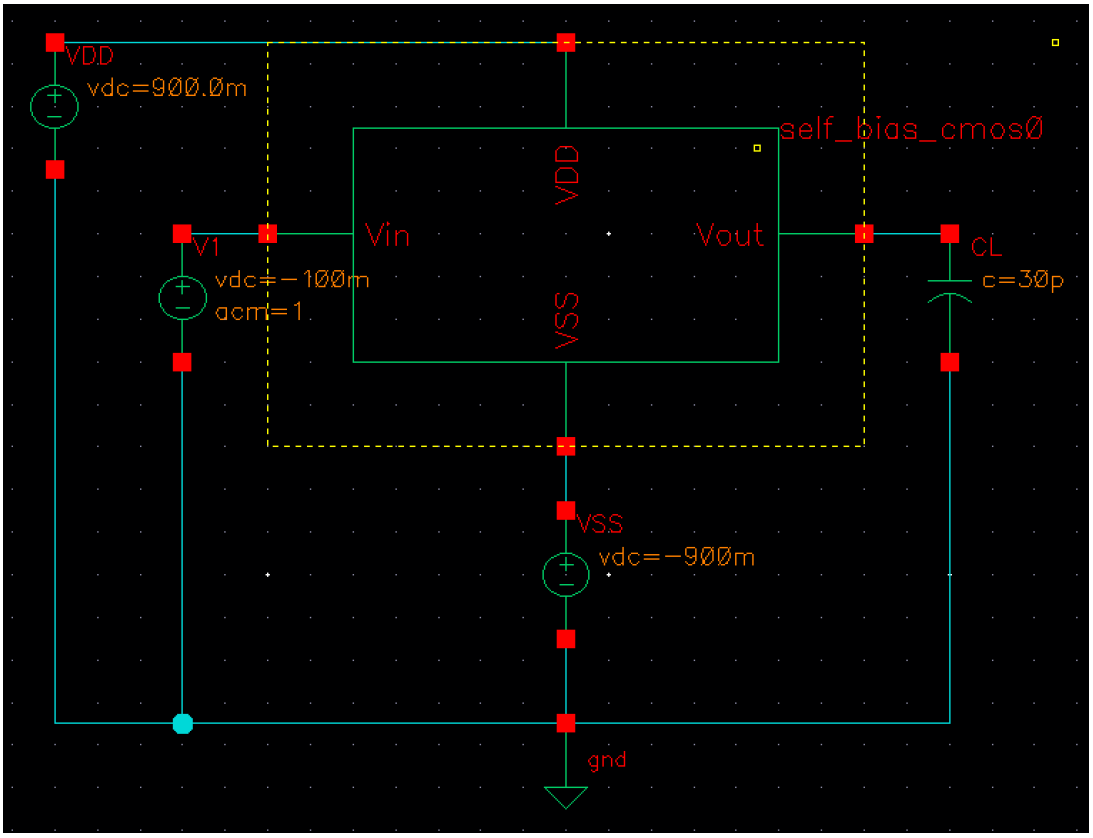
Yellow line: layout AC gain dB

d) Self-biased CMOS inverter

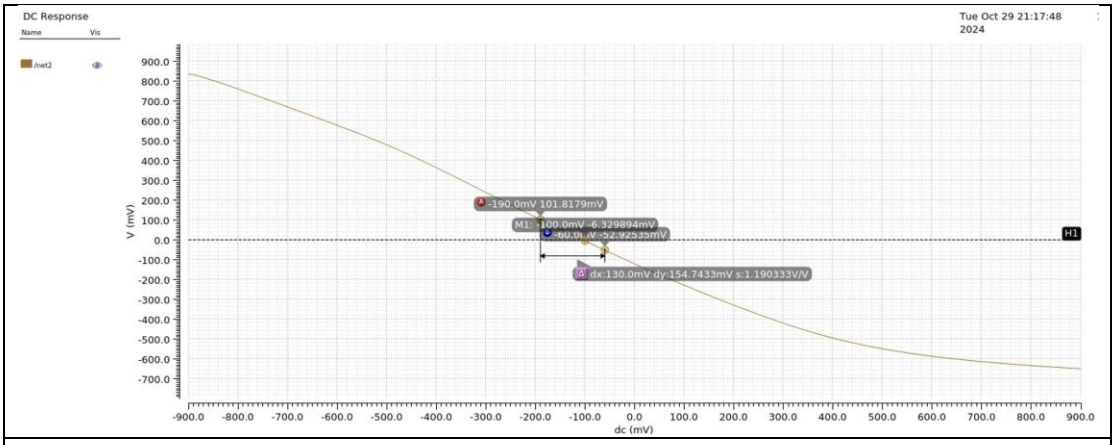
schematic



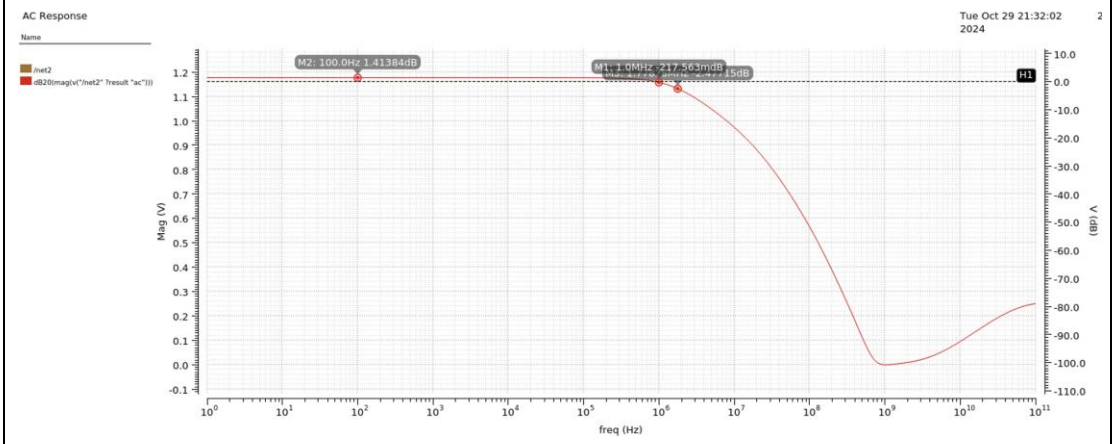
testbench



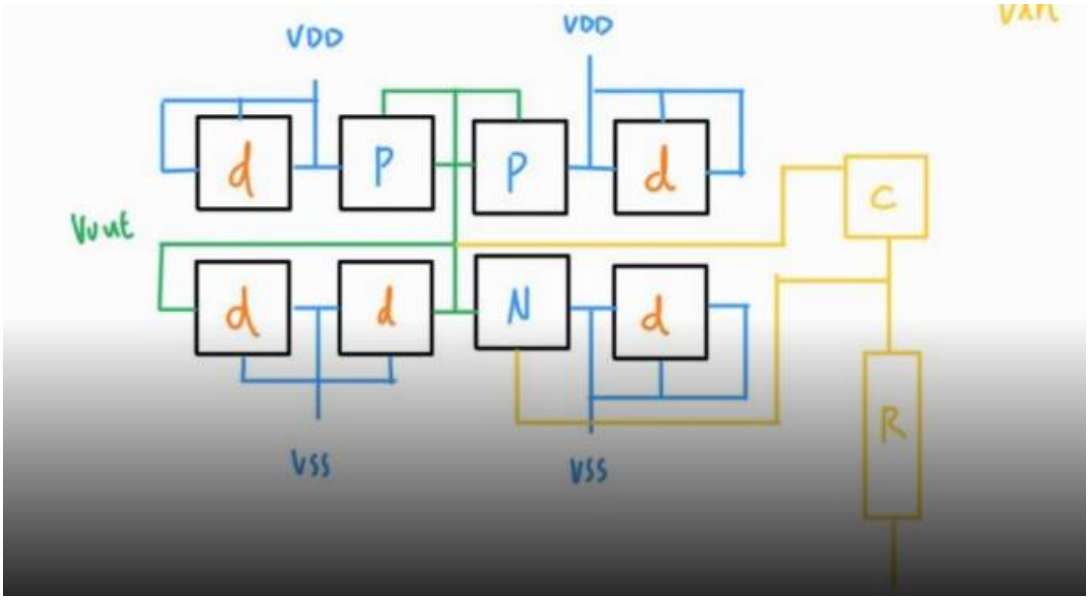
DC sweep



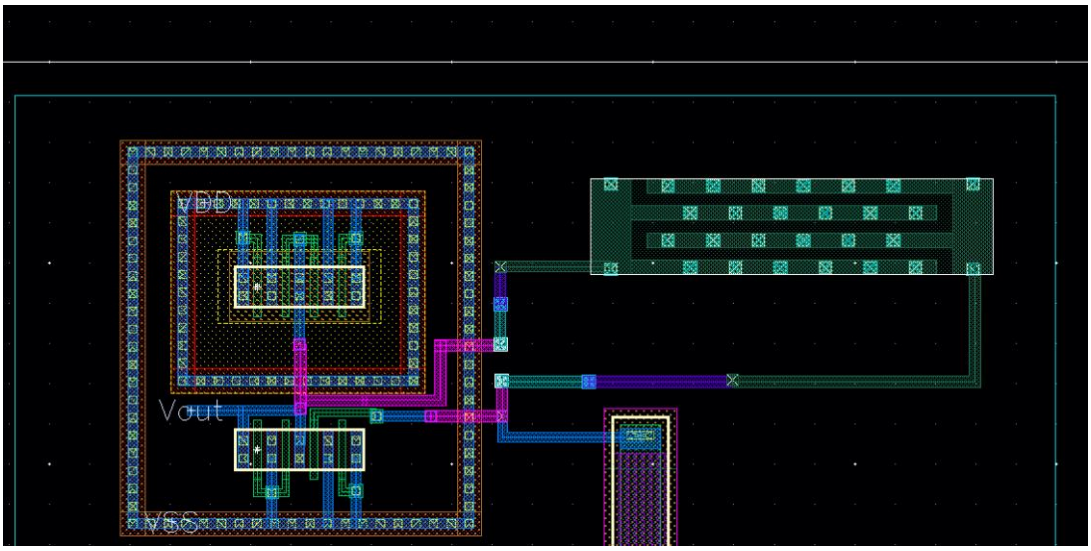
AC Freq



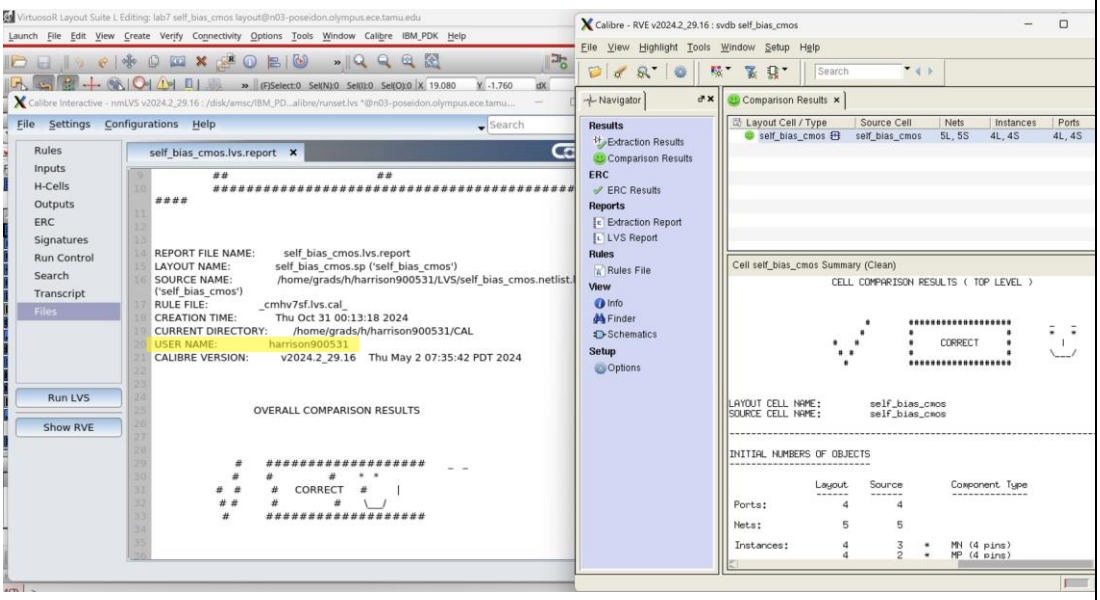
Floor Plan



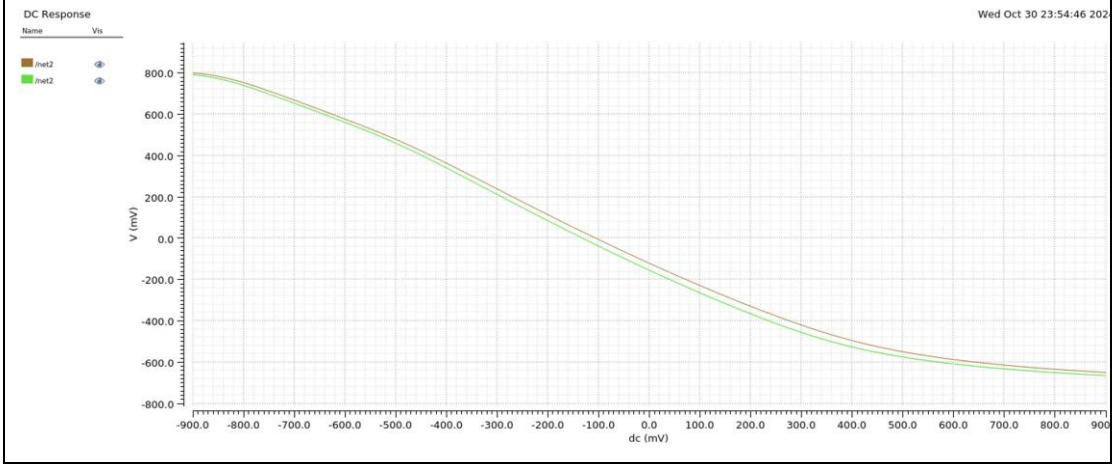
Layout

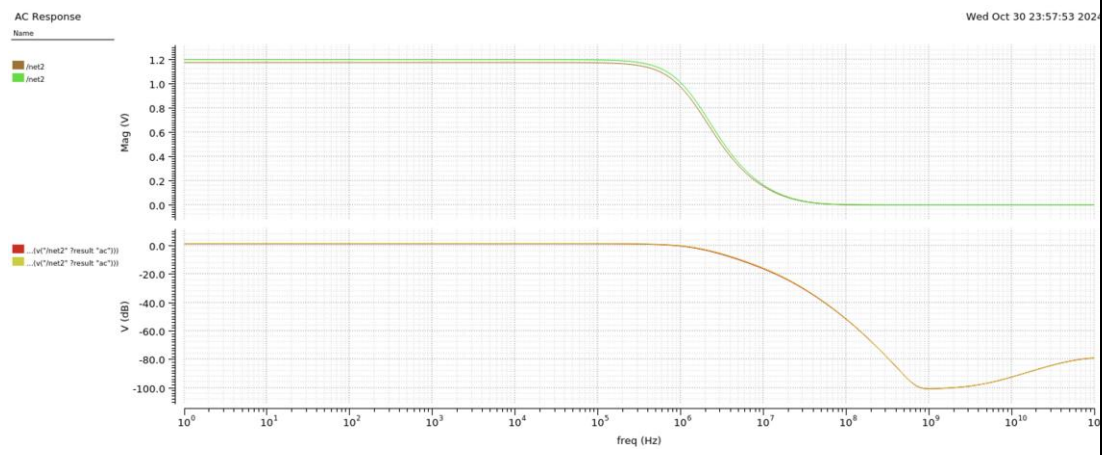


LVS



Post layout



Brown line: schematic Green line: layout
Post layout
   Brown line: schematic AC gain Green line: layout phase AC gain Red line: schematic AC gain dB Yellow line: layout AC gain dB

Discussion:

When I was drawing the layout, I discovered that placing a PC layer over the RX_M1 would create a instance “PCDCAP”. To resolve this issue, I attempted to change the PC layer to a different metal layer, which successfully solved the problem. Although I couldn't find information about “PCDCAP”, I suspect it is related to the differences in materials between the PC layer and the metal layer.

I remember the professor discussing in class that the second pole (fp2) will always affect the dominant pole (fp1). If fp2 is much greater than fp1 (fp2 >> fp1), then fp1 will be approximately equal to the -3 dB point. Conversely, if fp1 is not equal to -3 dB, the relationship changes. Plotting the first two questions is easier because we can determine fp1 by locating the -3 dB point of the AV0 dB point. However, the last two questions are more challenging since AV0 is already approximately equal to 0 dB (the Gain-Bandwidth Product point). If we use the -3 dB point method to find fp1, then fp1 multiplied by AV0 will not equal the Gain-Bandwidth Product (GBW). In this case, fp1 will be greater than GBW, which I find peculiar.

Another consideration is that since the wp1=2pi*fp1=1/AV0*R*C, fp1=1/2pi*AV0*R*C, and C \) is the only variable that affects fp1. However, when I use this equation to calculate the approximate value of fp1 it significantly differs from the value I

mentioned earlier the fp1= AV0 -3dB point.

Conclusion:

After completing Lab 7, we will have a solid understanding of designing inverting amplifiers, especially in high-frequency applications. This lab highlights the effects of capacitance and other factors that influence the amplifier's poles, impacting high-frequency response. By studying these elements, we can estimate high-frequency characteristics like the dominant pole, even when multiple factors interact. Through hand calculations and analysis, we gain practical insights into predicting and controlling amplifier behavior at higher frequencies, which is essential for accurate and reliable circuit design.