24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab5: Current Mirrors

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Section:601

Professor: Aydin Karsilayan

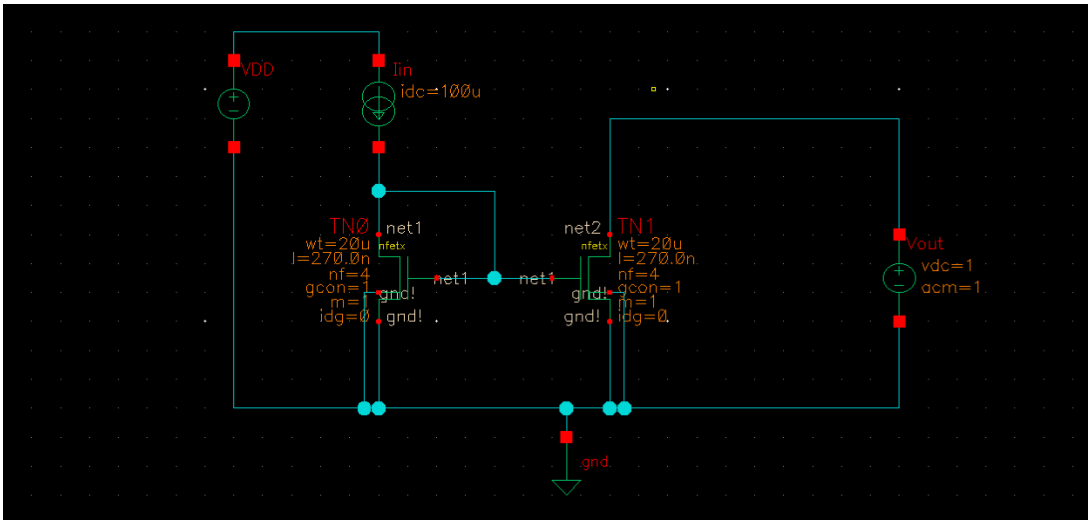
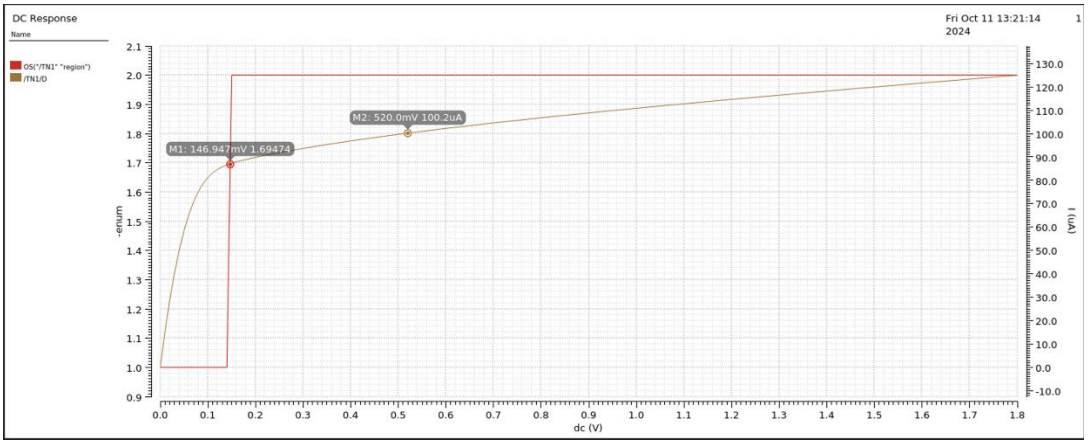
TA: Troy Buhr

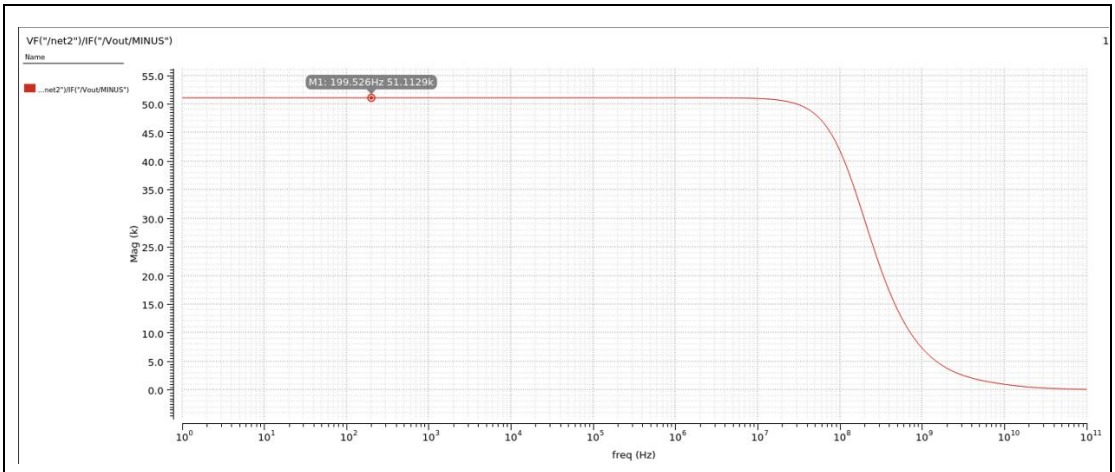
Description:

In this lab, we learn to make different kinds of current mirror such as simple current mirror and low-voltage current mirror (using the good layout techniques.) Current mirrors are essential components in analog circuits, they are the foundation of current-mode and switch-current techniques, making their design and layout critical for effective analog circuit performance.

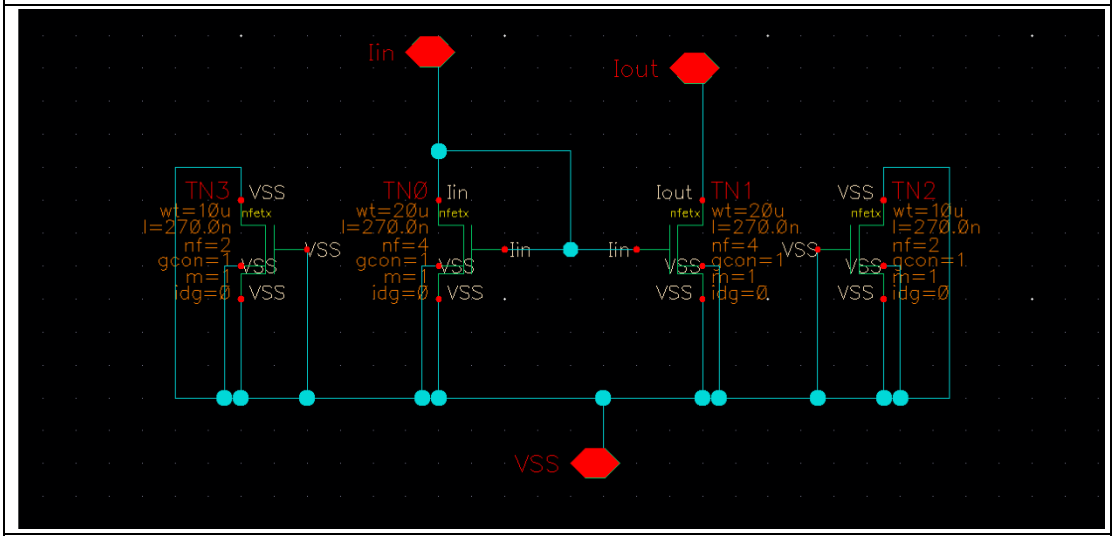
Design & result

1. Simple current mirror

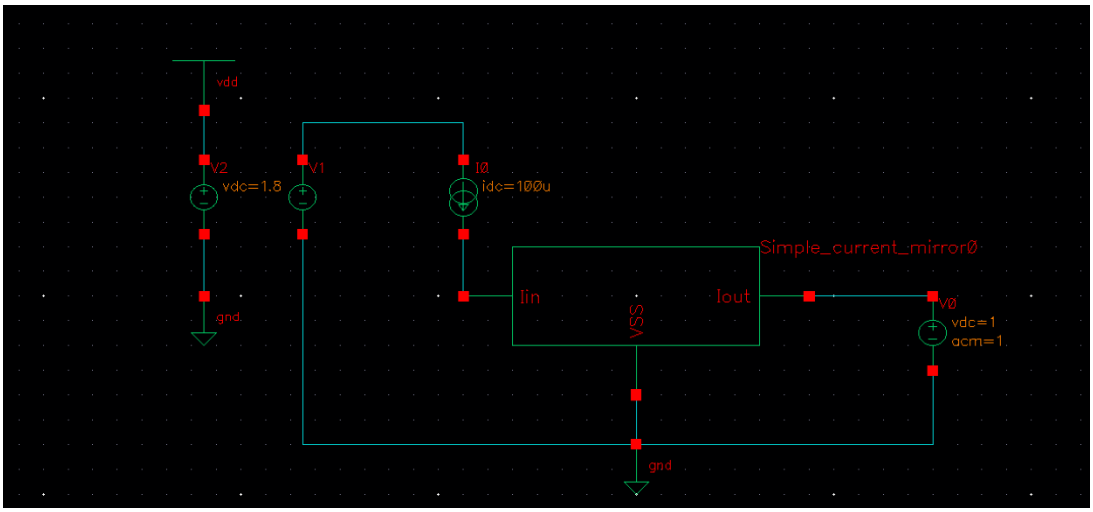
schematic

Compliance Voltage

low frequency output impedance



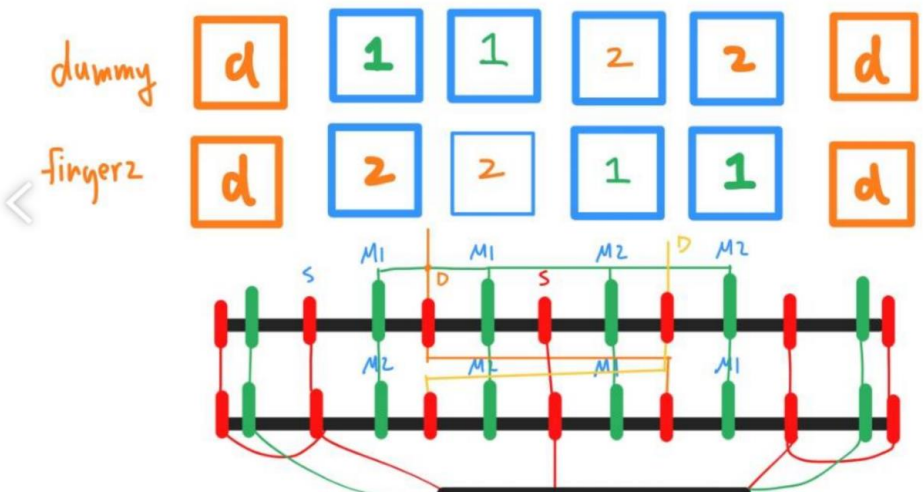
Adding dummy and Pins



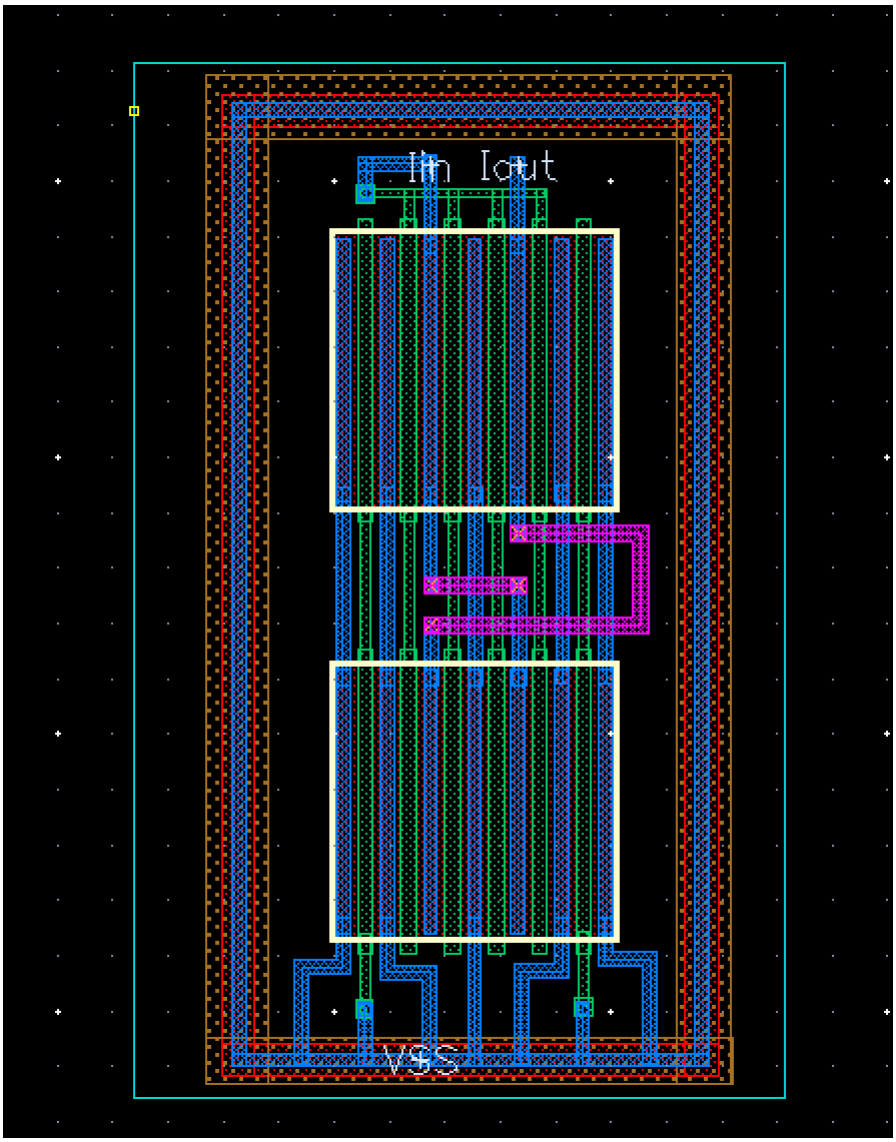
Making into symbol and testbench



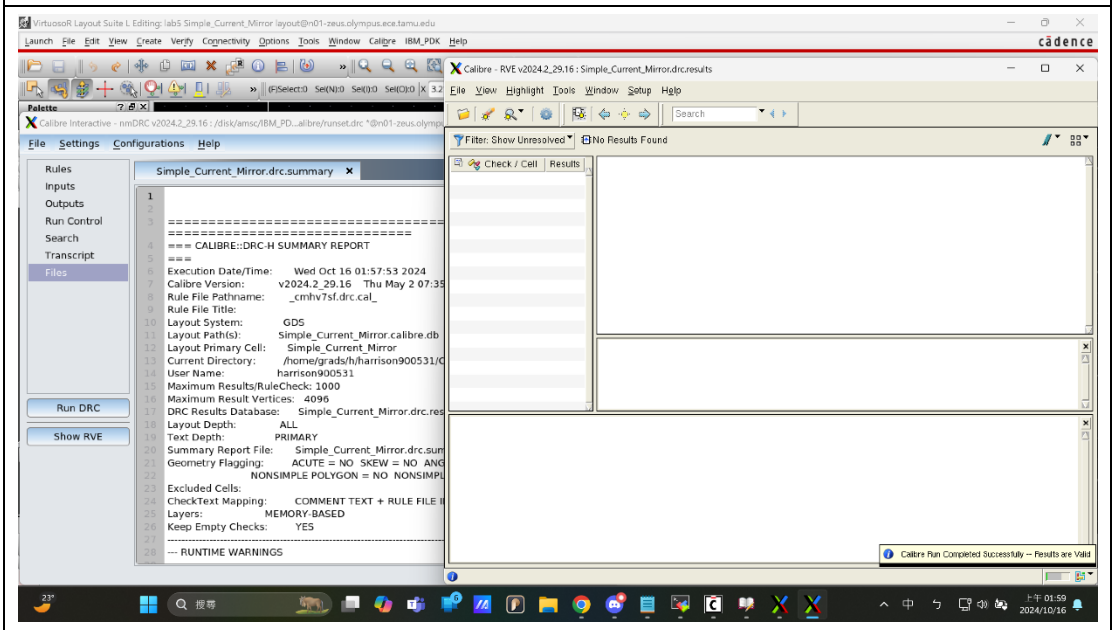
Floor plan


dummy
d
1
1
2
2
d
finger2
d
2
2
1
1
d
M1
M1
M2
D
M2
S
D
S
M2
M2
M1
M1

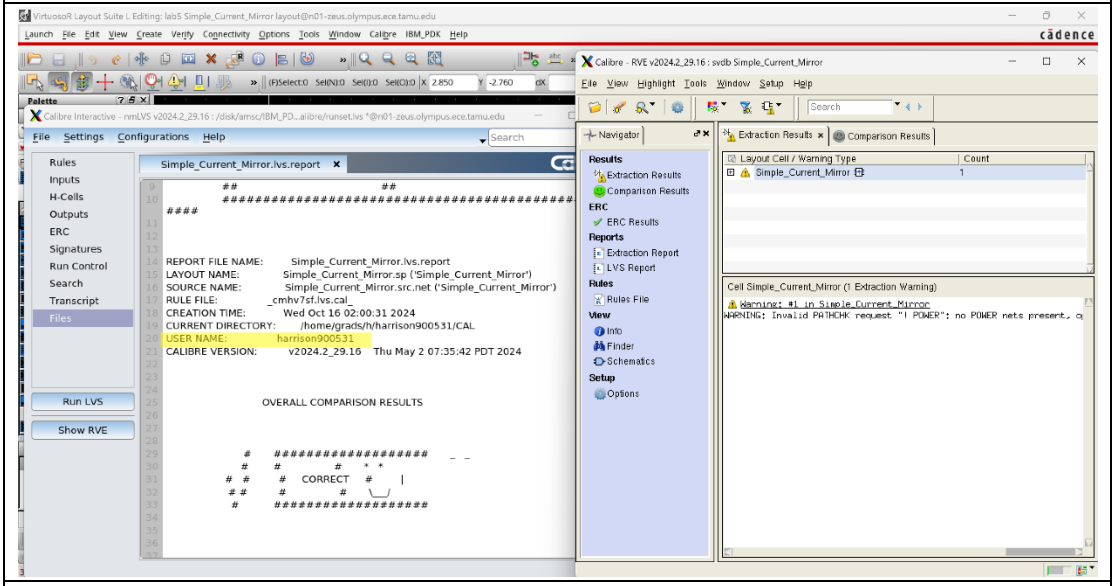
Layout


Iin
Iout

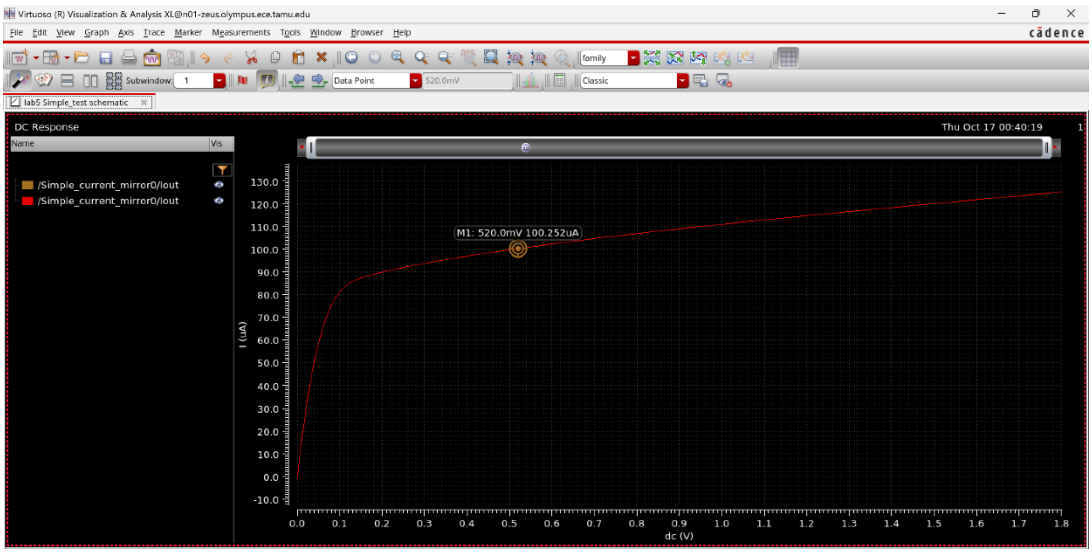
DRC



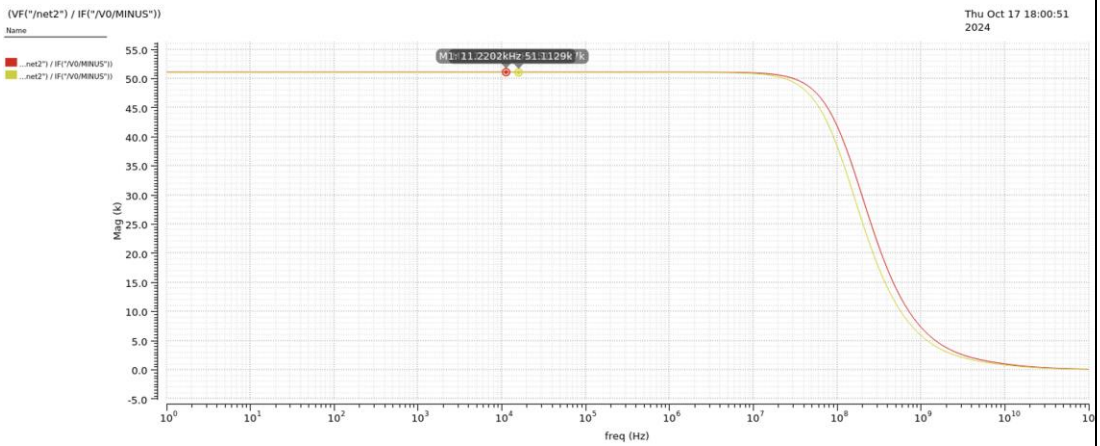
LVS



Comparing plot testbench schematic vs layout

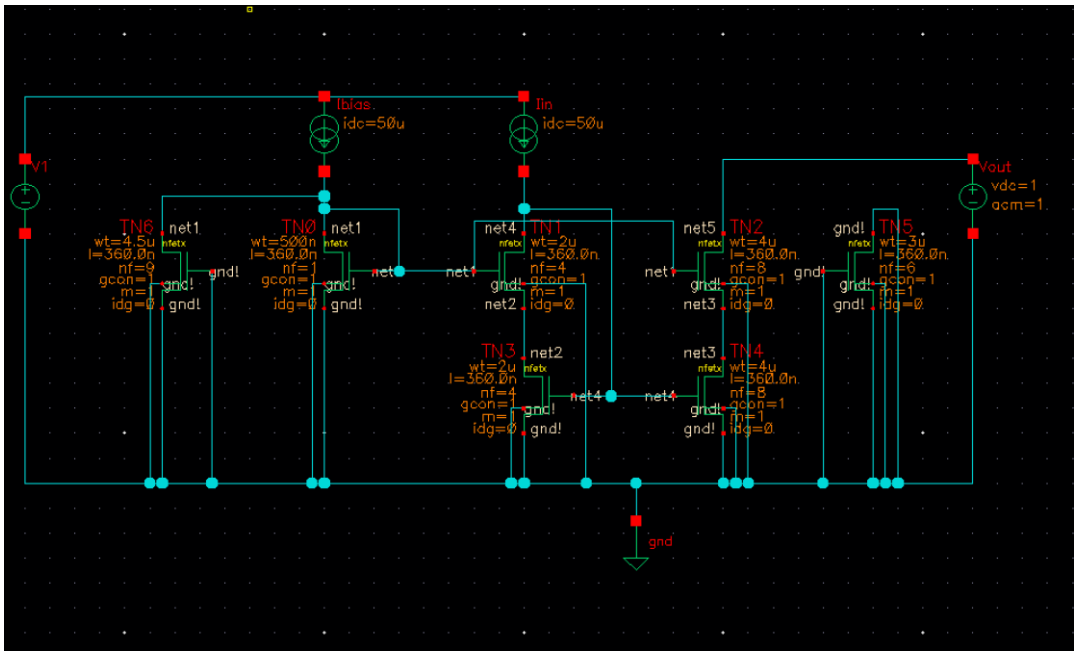


Rout schematice vs layout

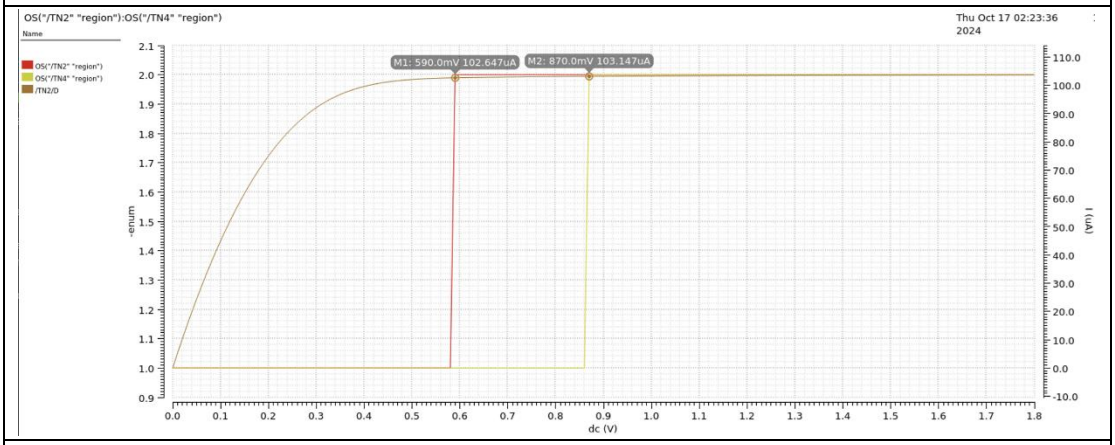


2. Low-voltage current mirror

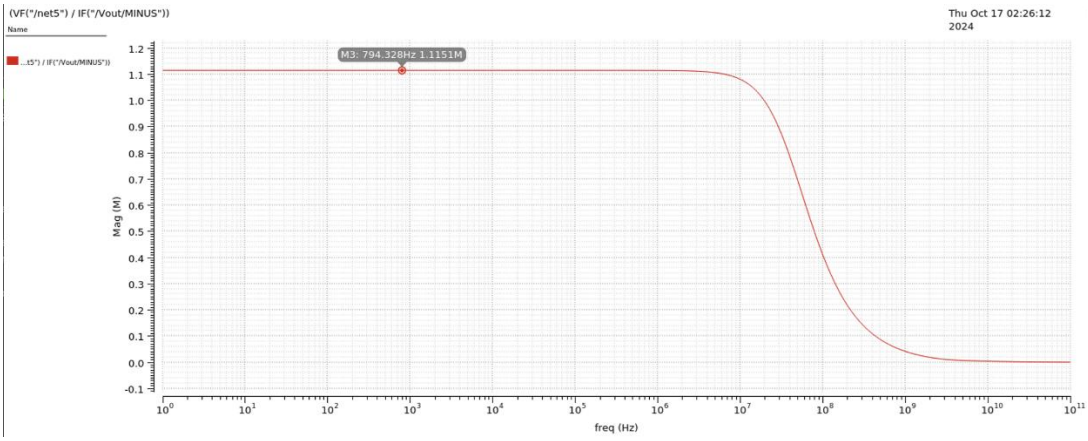
schematic



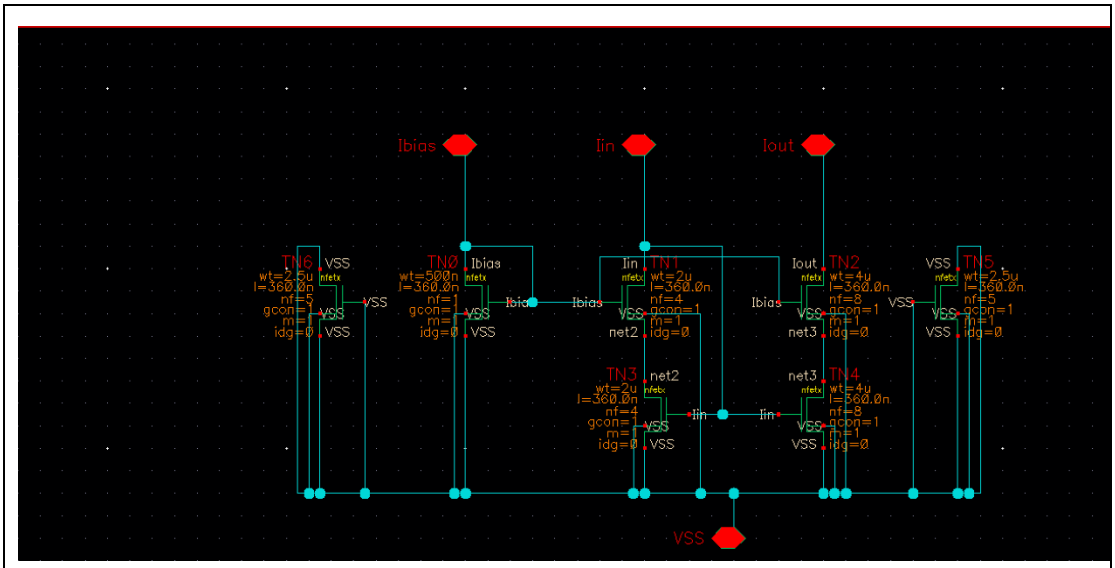
Compliance voltage



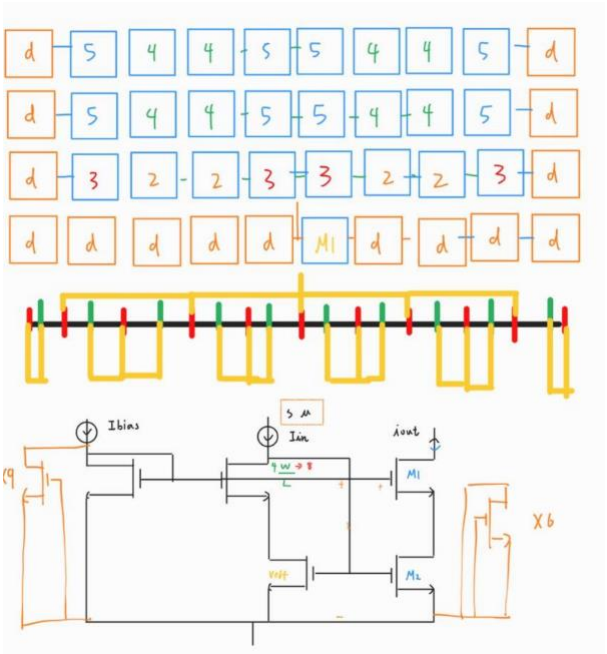
Rout



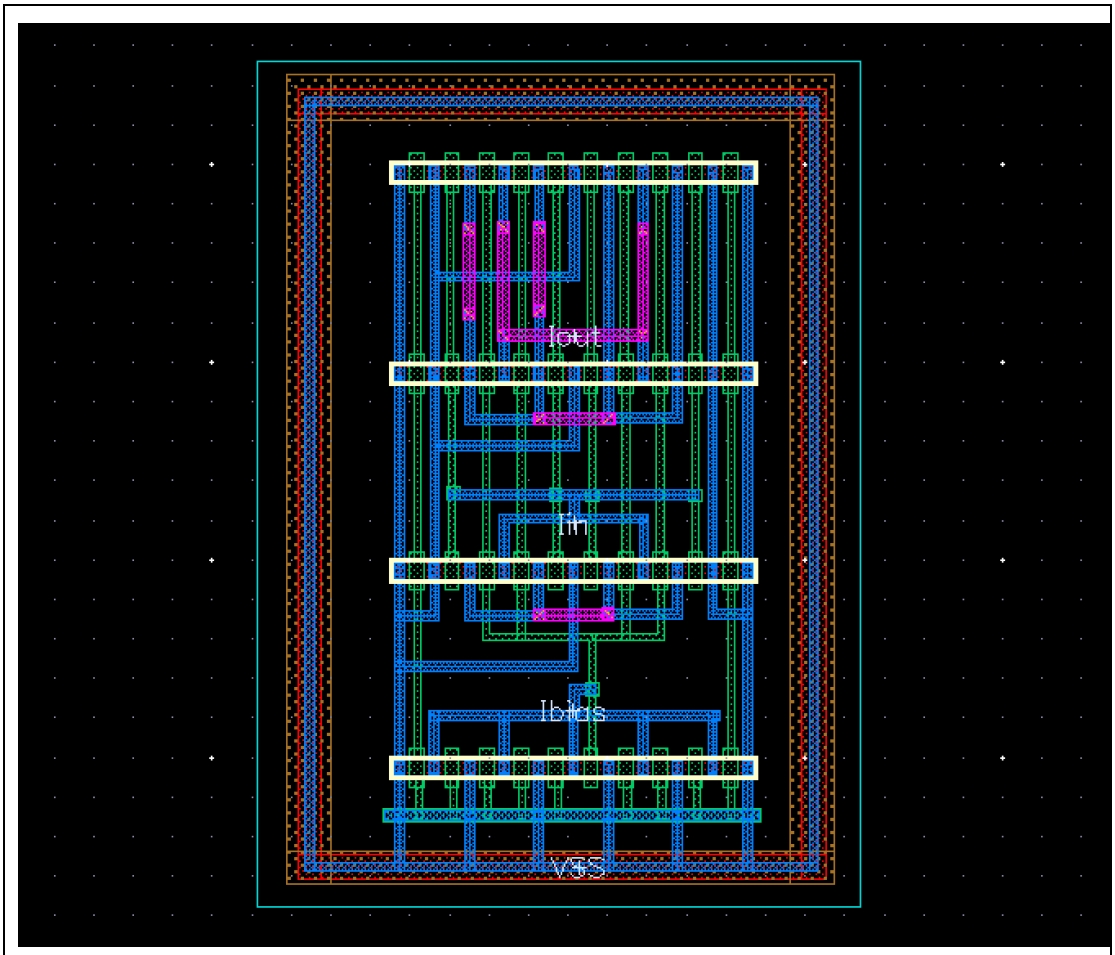
Adding pin and dummy



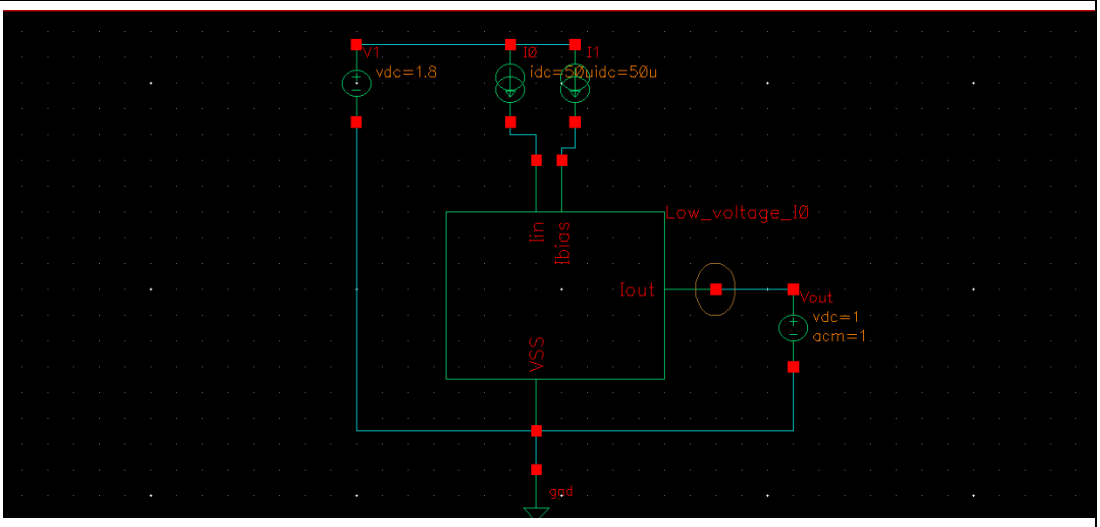
Floor plan



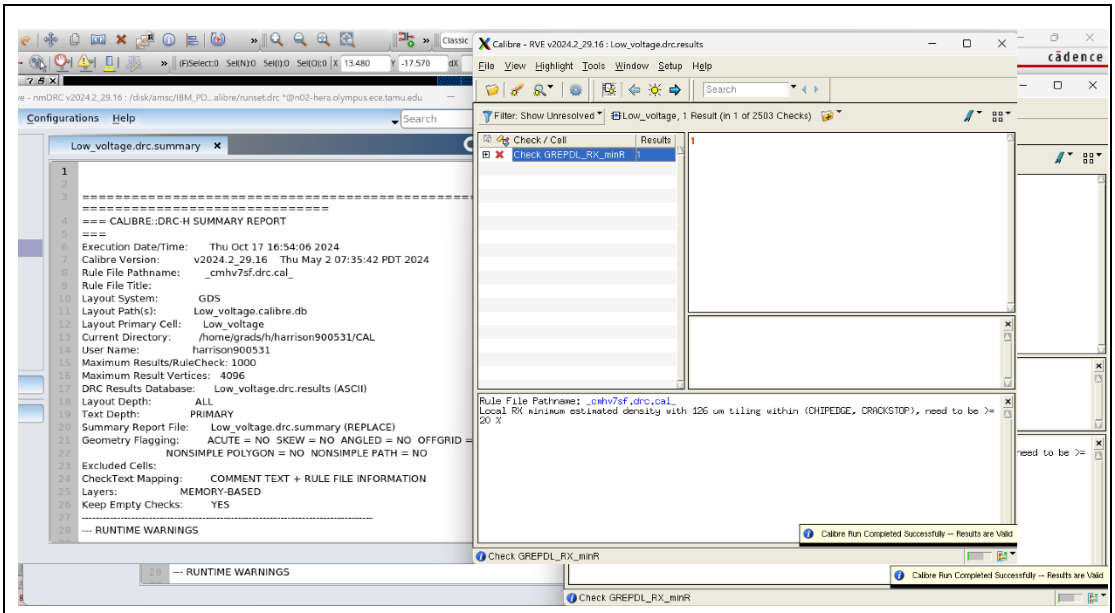
layout



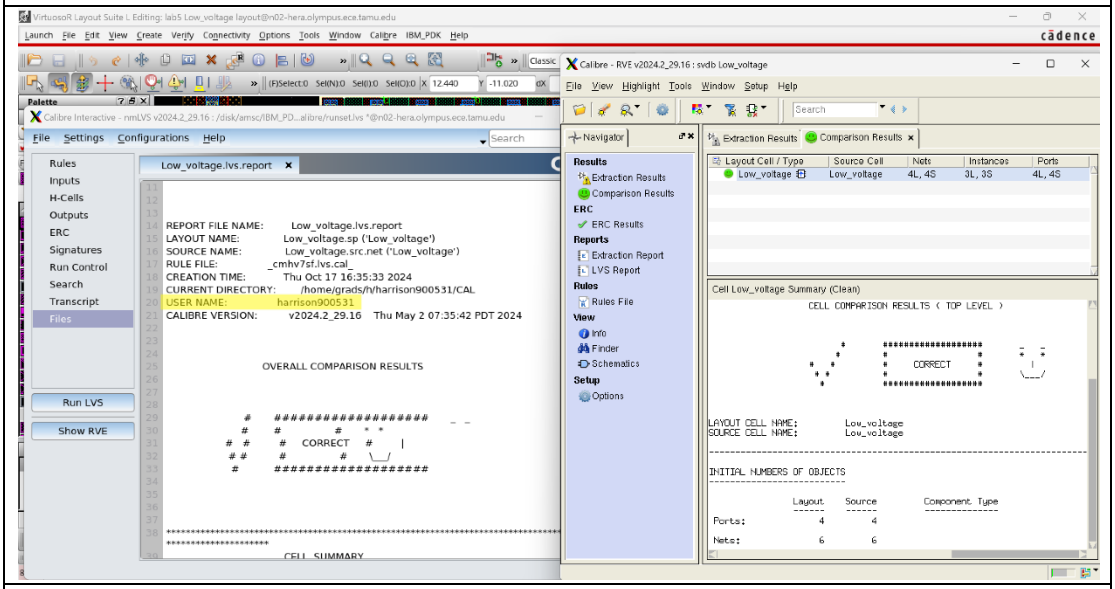
testbench



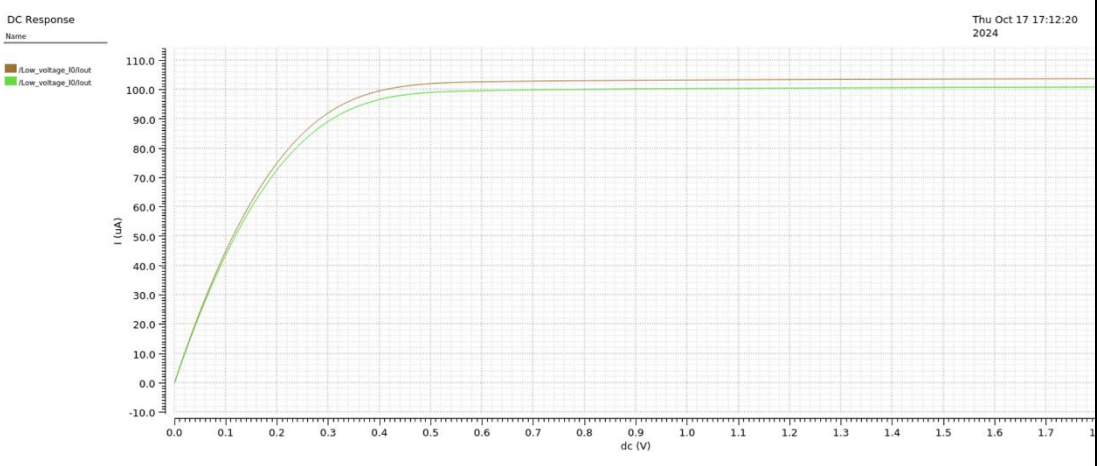
DRC



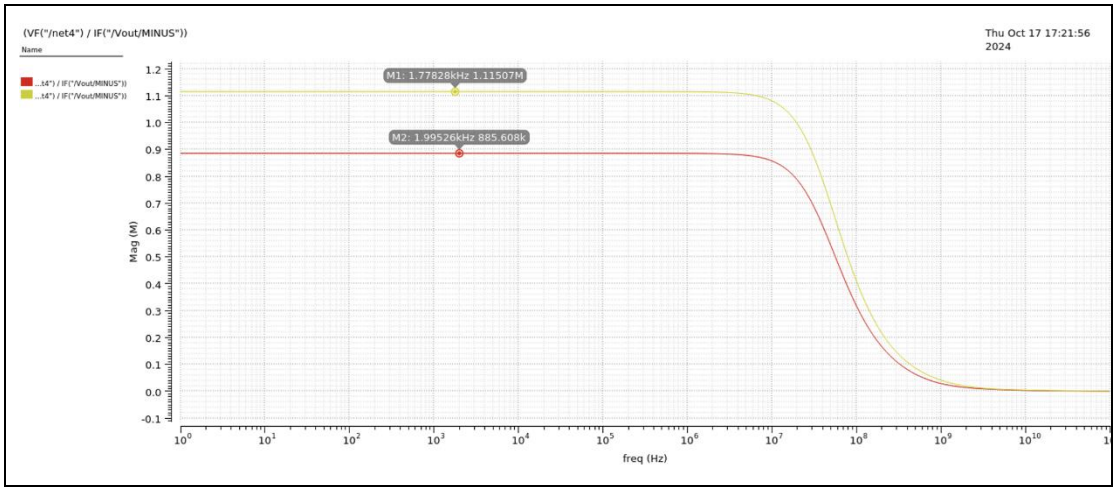
LVS



Compliance voltage schematic vs layout



Rout schematic vs layout



Discussion:

After obtaining the initial compliance voltage and low-frequency output impedance, we discussed the primary reasons for the discrepancies between our hand calculations and the actual simulation results. We assumed that the parameters (Vt, unCox, W/L, λ) were the same as those from Lab 1; therefore, the values obtained from our hand calculations should not differ significantly from the simulation results. However, after discussing this with TA, we realized that we overlooked certain factors. While extracting the parameters from Lab 1, the values of VDS, VGS, or other factors may have differed from those in Lab 1. Consequently, the parameters we used in our hand calculations (Lab 1 values) might actually have different values, leading to the discrepancies observed in the simulation results.

While adjusting the width-to-length (W/L) ratio for the final low-voltage current mirror, the challenging aspect is to achieve sufficient activation of the transistors, reduce the W/L ratio to increase the effective voltage (veff), as described by the equation Id = (1/2) * uncox * (W/L) * (veff^2). Additionally, ensure that the output resistance (Rout) is sufficiently large by optimizing the transconductance (gm), which is defined as gm = (2 * Id) / veff.

Conclusion:

After completing Lab 5, we learned how to design a simple current mirror and a low-voltage current mirror, particularly how to determine the W/L ratio of the current mirror to match the minimum compliance voltage at Vo while operating in the appropriate region. By combining the different types of current mirrors discussed in the lecture, we will gain more experience in determining the optimal matching values for the circuit.