ECEN 474/704 Lab 3: Layout Design Techniques

Introduction

In this lab you will learn in detail how to generate a simple transistor layout. Next, techniques will be developed for generating optimal layouts of wide transistors and matched transistors. Layout techniques for resistors and capacitors will also be illustrated. Finally, you will use all of these techniques to produce a two-stage operational amplifier layout (Lab 4).

Layout Techniques for Transistors

In Lab 1, you learned how to layout small size transistors. Most analog designs will not be limited to these small width transistors, thus special layout techniques need to be learned to layout large width MOSFETS. Luckily, wide transistors can be broken into parallel combinations of small width transistors as seen in Figure 3-1. By doing this horizontal expansion technique for the wide transistor, the drain and source area can be reduced, which decreases parasitic capacitance and resistance.

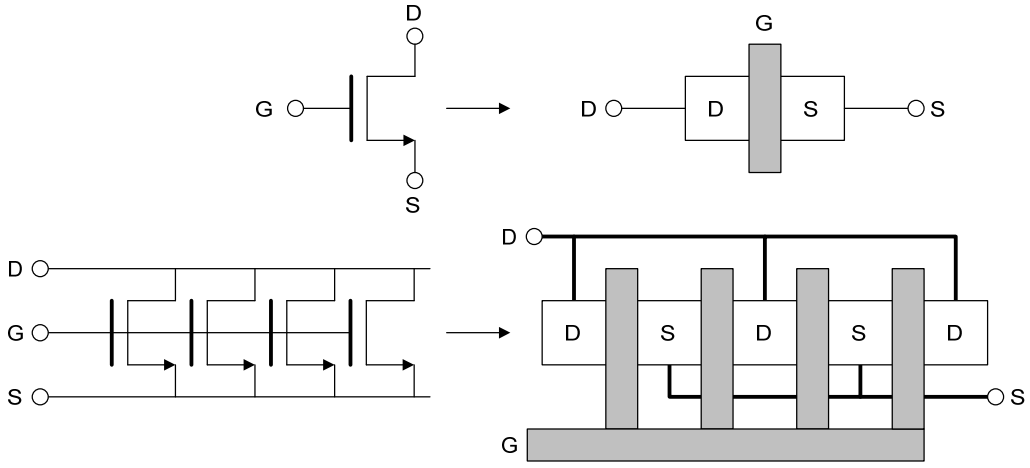

Figure 3-1: Wide MOS Transistor Layout

Another good layout technique is to use "dummy" transistors on both ends of a transistor layout. These dummy transistors ensure that the etching and diffusion processes occur equally over all segments of the transistor layout (Figure 3-2).

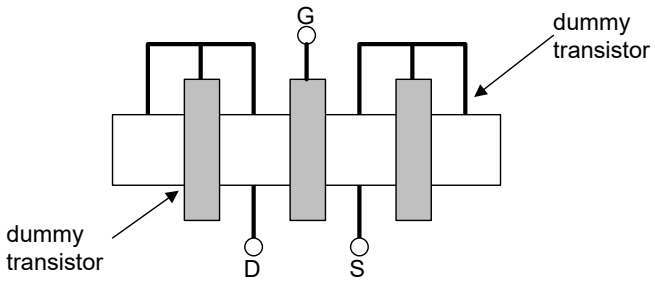

Figure 3-2: Dummy Transistor Layout

Notice the gate, drain and source are connected together which keeps it from conducting any current. This shorted transistor is connected to the drain or source of the functional transistor. Another alternative for dummy transistors is to have the gate and source tied together.

When laying out any device, the key is symmetry, especially when laying out fully-differential components. For matched devices, use interdigitized or common-centroid layout techniques, where two transistors need to have exactly the same geometries. Examples include current mirrors and differential pairs.

An interdigitized layout is shown in Figure 3-3. Notice that the two transistors have been split into smaller size devices and are interleaved. This layout minimizes the effects of process variations on the parameters of the transistors.

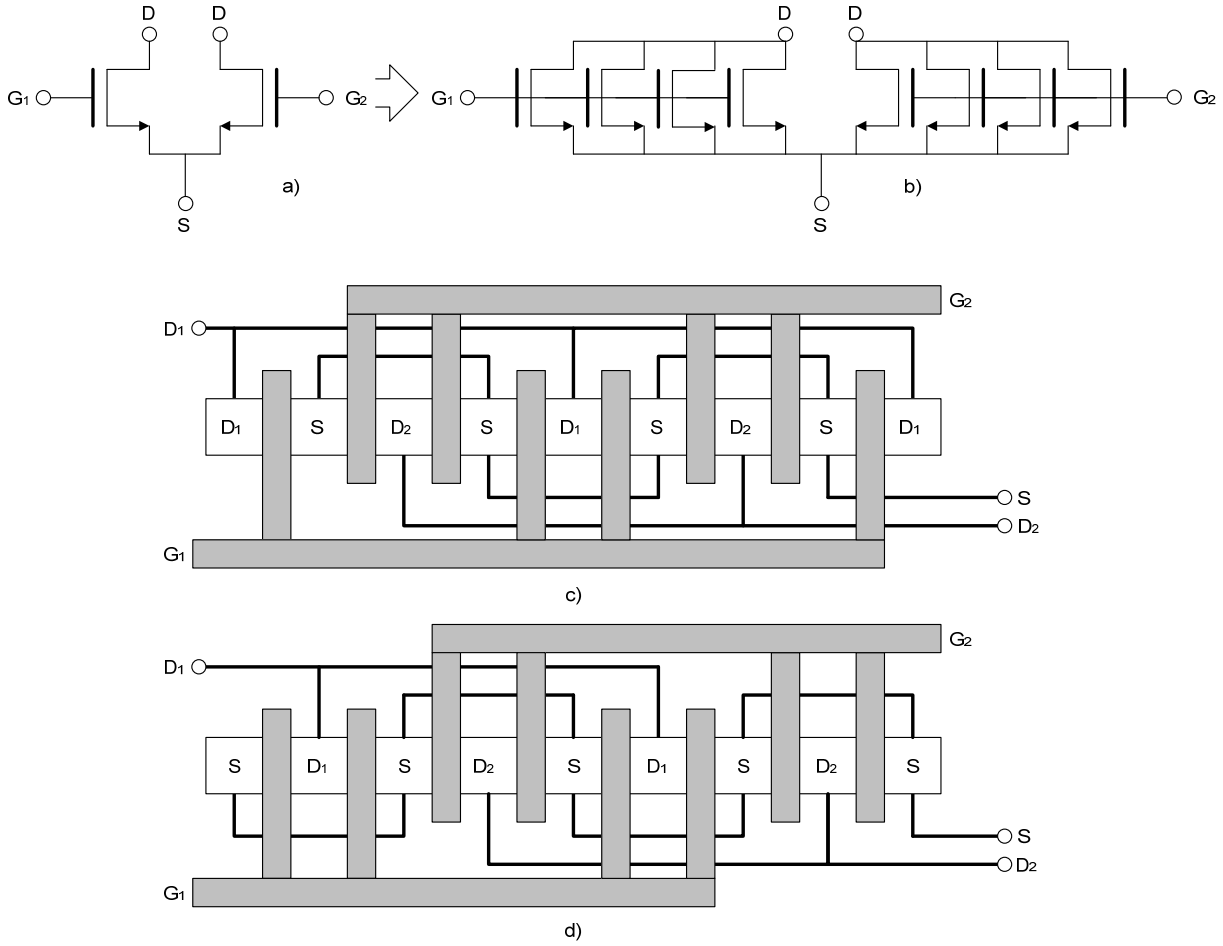

Figure 3-3: Interdigitized Layout of a Differential Pair **(a)** Differential pair **(b)** Horizontal pair
(c) Interdigitized layout (Drain areas are different. Common centroid)
(d) Interdigitized layout (Drain areas are equal. Not common centroid)

The idea behind splitting a transistor up is to average the process parameter gradient over the area of the matched devices. For example, the process variation of KP and the transconductance parameter on the wafer is characterized by a global variation and a local variation. Global variations appear as gradients on the wafer as in Figure 3-4. However, local variations describe the random change in the parameter from one point on the chip to another nearby point. By using layout techniques such as interdigitized and common-centroid, the process variation can hopefully be averaged out among the matched devices.

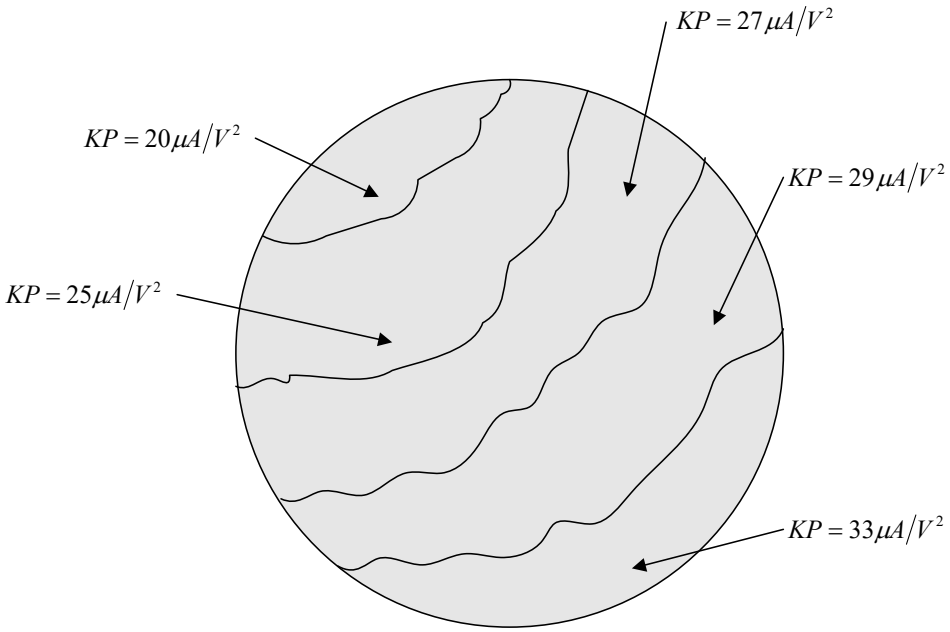

Figure 3-4: Gradient of KP on Wafer

When laying out wider matched transistors the common-centroid layout may be a better choice. This layout technique is illustrated in Figure 3-5 for the case of 8 matched M1 and M2 transistors of a differential pair.

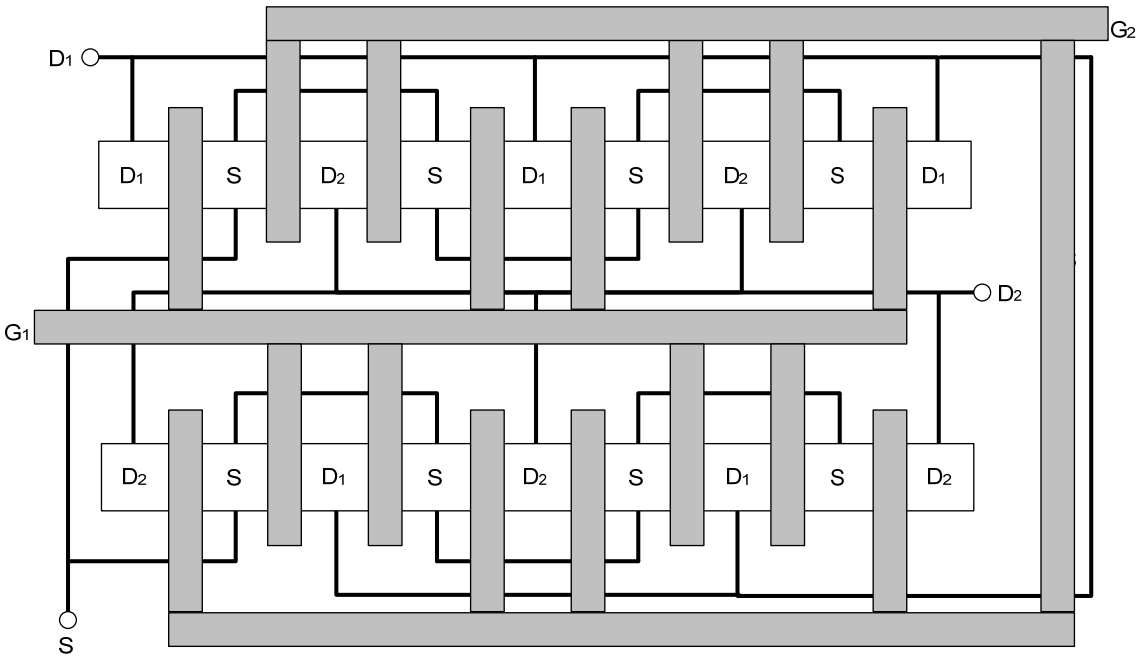

Figure 3-5: Common-Centroid Layout of a Differential Pair

The idea behind the common-centroid layout is to average linear processing gradients that affect the transistors' electrical properties. Common-centroid layouts should have the centroid (center of mass) of each transistor positioned at the same location. The following examples (Figure 3-6) illustrate what is common-centroid and what is not common-centroid.

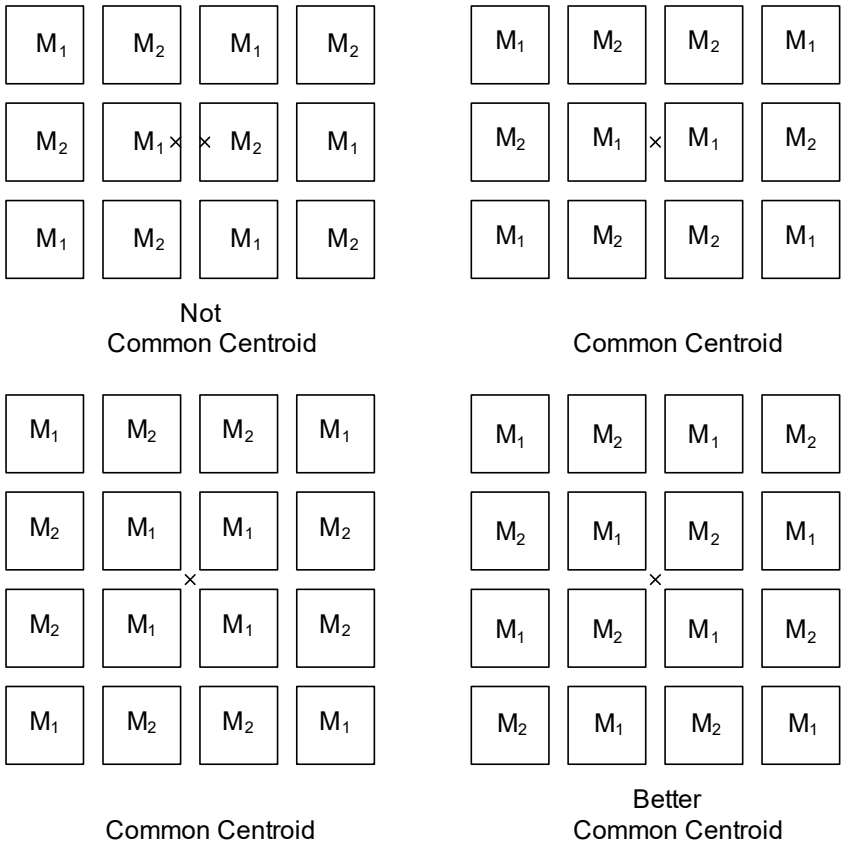

Figure 3-6: Common-Centroid Examples

Additional Notes on Current Mirrors

In this lab you will be asked to create a 64-transistor current mirror, which will require two branches each with 32 transistors. You should first create your schematic with the physical structure of the current mirror in mind. The first step is to draw a typical current mirror and add dummies to the edges, one possible configuration is shown below in Figure 3-7.

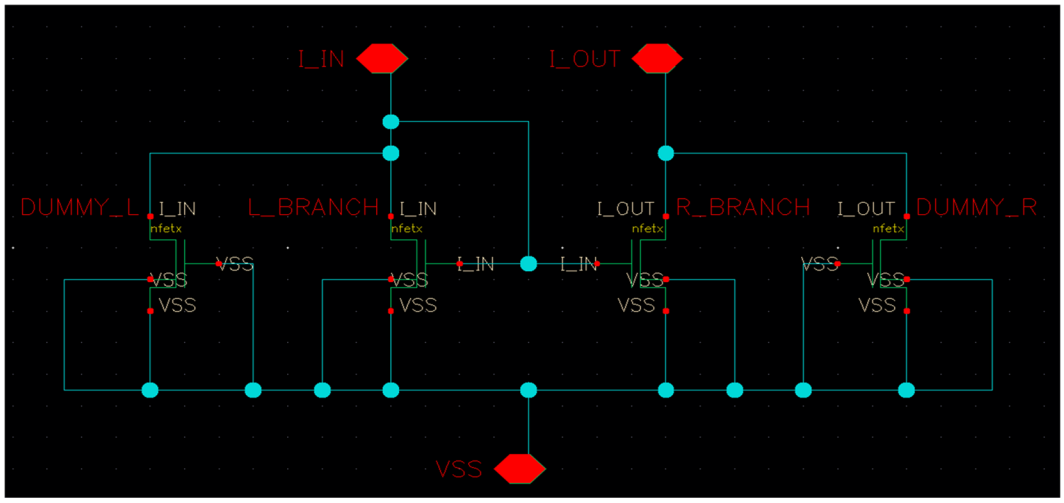

Figure 3-7: Current Mirror Schematic

Next you need to decide what the dimensions of the physical current mirror shall be by setting the total width and modifying the number of fingers. Such dimensions are (in row by column format):

- 1x64 (2 dummies needed)
- 2x32 (4 dummies needed)
- 4x16 (8 dummies needed)
- 8x8 (16 dummies needed)
- 16x4 (32 dummies needed)
- 32x2 (64 dummies needed)
- 64x1 (128 dummies needed).

This will determine your number of fingers and overall width of each row of transistors, so now choose your dimensions and draw your floor plan to match.

Layout Techniques for Capacitors

A capacitor is formed when an insulator separates two conducting sheets. Various types of monolithic capacitors using MOSFET, MIM (metal-insulator-metal), poly-to-poly, MOM (metal-oxide-metal), etc. can be fabricated on integrated circuits. In this lab, MOM capacitors will be utilized. A MOM capacitor is a coplanar structure formed by interdigitated fingers within individual metal layers to create lateral capacitance between plates as shown in Figure 3-8. The MOM capacitor has been widely used due to the following characteristics.

- High capacitance density (refer to the design manual)
- Low parasitic capacitance
- Good linearity with dimension
- Symmetric plate design, thus good matching characteristics
- No additional masks or other fabrication process, i.e. freely available with modern CMOS

MOM capacitors can be constructed from any number of consecutive metal levels connected in parallel with vias. The model supports variable dimensions for width (W) and length (L). Normally, the lowest metal layers (e.g. M1 - M5) with fixed metal line width and spacing are used in order to allow maximum capacitance density and high yield. In order to reduce parasitic capacitance induced between the bottom metal layer and the substrate, a lower level of metal could be removed by trading off capacitance density.

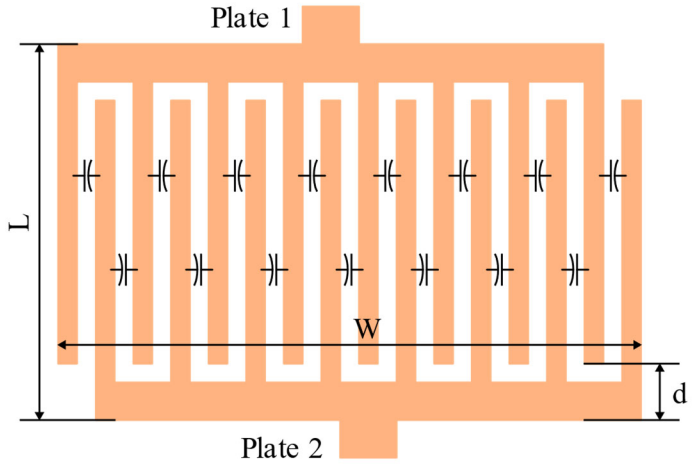

Figure 3-8: Top view of one layer of a Metal-Oxide-Metal Capacitor

Thus the total capacitance can be calculated by

$$C_{total} = C_f \times W \times (L - 2d)$$

where:

C_f = capacitance density in fF/μm^2 (refer to the design manual)
W = total width in μm
L = total length in μm

Similar to matched MOSFETS, the common-centroid layout technique can be employed for matched capacitors. A simplified floor plan for two equally sized, well-matched capacitors is shown in Figure 3-9.

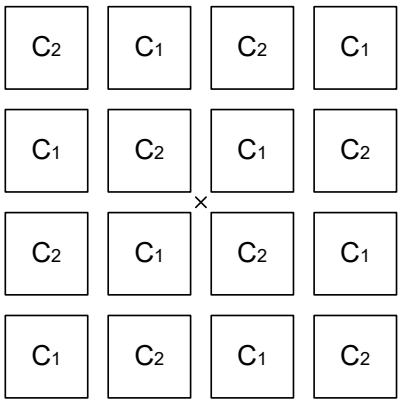

Figure 3-9: Common-Centroid Capacitor Layout

Remember, the purpose of using the unit capacitor is to keep the ratio of the areas and perimeters the same. This prevents (delta) variations in capacitor dimensions from changing the capacitor ratio (see the lecture notes on the layout techniques for proof). If a non-integer number of unit capacitors are required then the perimeters and areas can still be kept the same. If the ratio of capacitors is:

$$\frac{C_1}{C_2} = \frac{I_1 C_u}{I_2 C_u + N C_u}$$

where $1 < N < 2$, then we can add a non-unit capacitor $C_{nu} = NC_u$ to form C_2 and have equal perimeter/area. I_1 and I_2 are both integers representing the number of unit caps in C_1 and C_2, respectively. The unit capacitor has side length L_0 and the non-unit capacitor has length L_{nu} and width W_{nu}. Use the following formulas to calculate the side lengths of the non-unit capacitor:

$$L_{nu} = L_0 \left(N + \sqrt{N(N-1)}\right)$$

$$W_{nu} = N \frac{L_0^2}{L_{nu}}$$

Keep the unit capacitor side length L_0 in the range from 10 μm-25 μm. Also, within the capacitor array, use a consistent method of routing lines between the capacitor segments. Each unit capacitor should be surrounded by similar routing lines. Use multiple contacts to lower series resistance. For capacitors near the edge of the array, use "dummy" routing lines. Also, be sure that parasitic capacitance formed by overlapping conductors is the same for the matched capacitors.

Additional Notes on Capacitors

In this lab, you will also be asked to create an interdigitized capacitor array, complete with dummy capacitors. Figure 3-10 shows the schematic view of one possible configuration of the capacitor array that needs to be laid out. The capacitors to be used are called **vncapx** and they are found in the **cmhv7sf** library. Once the capacitor array has been laid out, a via from RX_M1 surrounded by a layer of BP is required. **Remember that the BP layer is needed to create a p+ region that provides good ohmic contact between the p- substrate material and the metal layers used for routing. Be sure to label this via "VSS" (Figure 3-11).**

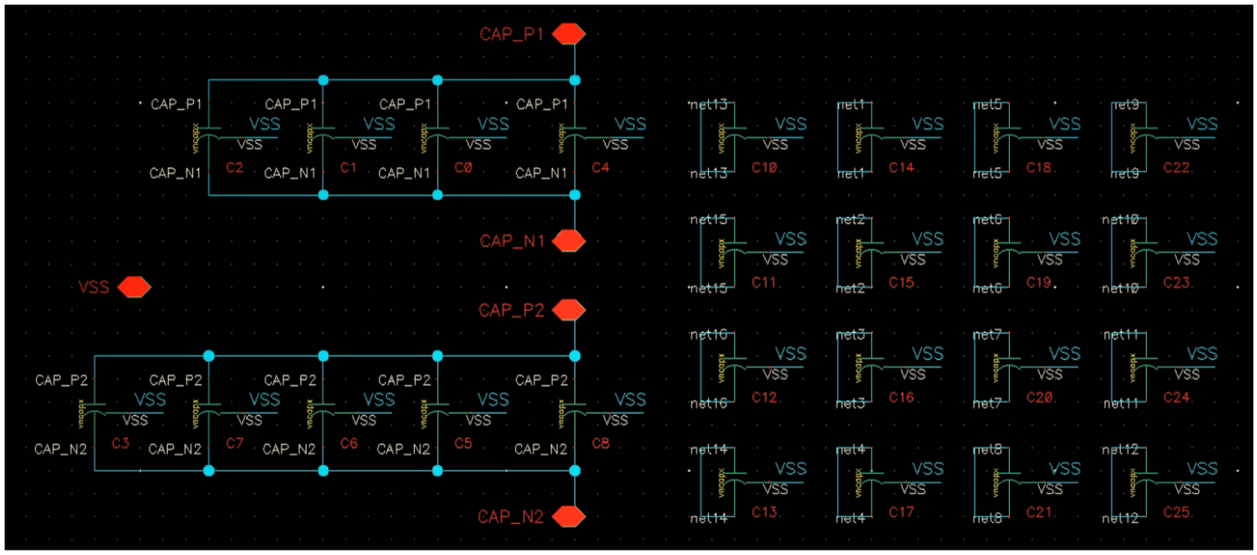

Figure 3-10: Schematic View of the Capacitor Array

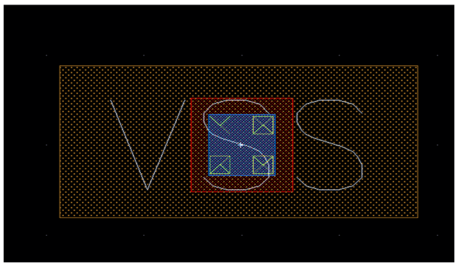

Figure 3-11: Voltage Reference for the Layout

Typically, capacitors are considered to have two pins (i.e. they are viewed as “one-port” devices), but in practice there is an implicit third terminal due to the parasitic capacitors created between each pin and the substrate. Although the substrate is not a strong conductor compared to the metal used for the on-chip routing, it is conductive enough to create another plate of a capacitor (the resistance of the substrate will lead to a larger equivalent series resistance for the parasitic capacitors compared to the desired capacitance). In other words, each capacitor instance in the schematic actually consists of three separate capacitors: the pin-to-pin capacitor, the pin-to-substrate capacitor at pin 1, and the pin-to-substrate capacitor at pin 2. In this PDK, the substrate terminal of the capacitor instances is referred to as the “backplate” node. Current will flow through these parasitic pin-to-substrate capacitors, so a return path must be provided for these currents. To provide this return path, it is necessary to connect the backplate to the same net as the substrate material underneath the capacitor. This is why the schematic instance of the capacitor has a third terminal and why it must be connected to the same potential as the substrate (VSS in this case).

Layout Techniques for Resistors

Many different types of resistors are available in integrated circuits. Other than active devices biased to act as resistors, we can use the inherent resistivity of the polysilicon for diffusions to create resistors. As an example, Table 3-1 shows the typical values of a poly resistance for the IBM 180 nm process that we will be using to design circuits.

Table 3-1: Typical Resistivity Values for the Polysilicon Layer

Process Parameter	Description	OPRPPRES			
		Min	Nominal	Max.	Unit
Rs	Sheet Resistance(0V,25°C)	0.1518	0.165	0.1782	kΩ/sq
Rcon	Contact Resistance	0.005	0.015	0.050	kΩ-µm

The total resistance of a monolithic resistor is the sum of the contact resistance and the ohmic resistance of the diffusion material. The following formula can be used to estimate resistance of polysilicon and diffusion resistors:

$$R_{nom} = R_s \times \frac{L}{W} + 2 \times \frac{R_{con}}{W}$$

where:

R_s = resistance per square [kΩ/sq] for the chosen resistor type
L = length [µm] of the resistor
W = width [µm] of the resistor
R_{con} = contact [kΩ-µm] resistance

A layout of one resistor made out of polysilicon from the design kit is shown in Figure 3-12. The resistor is built in by containing a strip of poly and poly-M1 contacts. The length of the OP mask determines the length of the OP resistor.

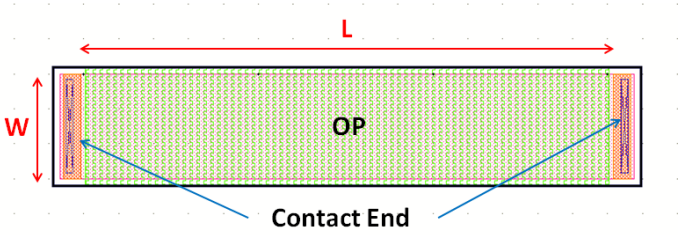

Figure 3-12: Poly Resistor (OPRPPRES) Layout

If the circuit operation depends on the ratio of resistances, then good matching can be obtained by using interdigitized or common-centroid techniques. When matching resistors, be sure to keep device orientation and sizes the same. Also, since contacts contribute resistance, keep the contacts in the same ratio. An interdigitized layout of resistors is illustrated in Figure 3-13. Notice that the interconnecting metal is overlapping the resistor array and non-overlapping the resistor array in equal lengths for the two resistors.

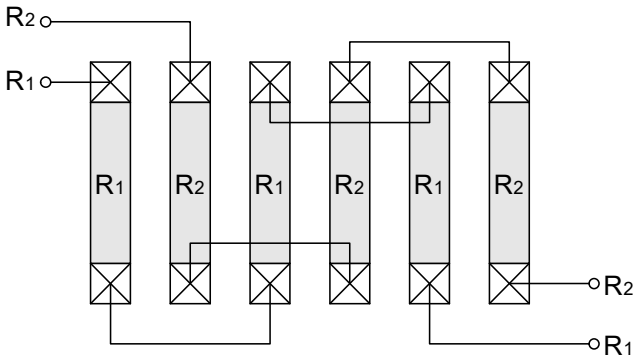

Figure 3-13: Interdigitized Resistor Layout

Additional Notes on Resistors

In this lab, you will create an interdigitized resistor pair as well. Figure 3-14 shows a schematic of one possible configuration of the resistor pair to be laid out. The resistors to be used are called **oprppresx** and they are found in the **cmhv7sf** library. The green boxes with X's on them are an element called **noConn** found in the **basic** library. The **noConn** element is used for the dummy elements since the pins are left floating, but individual **noConn** elements are not connected to each other. The **noConn** element suppresses a warning from the schematic editor for the floating nets. Also, for the layout, a via from RX_M1 is needed with the label "VSS" similarly to what was needed for the capacitors. Do not forget to surround the via with a layer of BP (refer back to Figure 3-11).

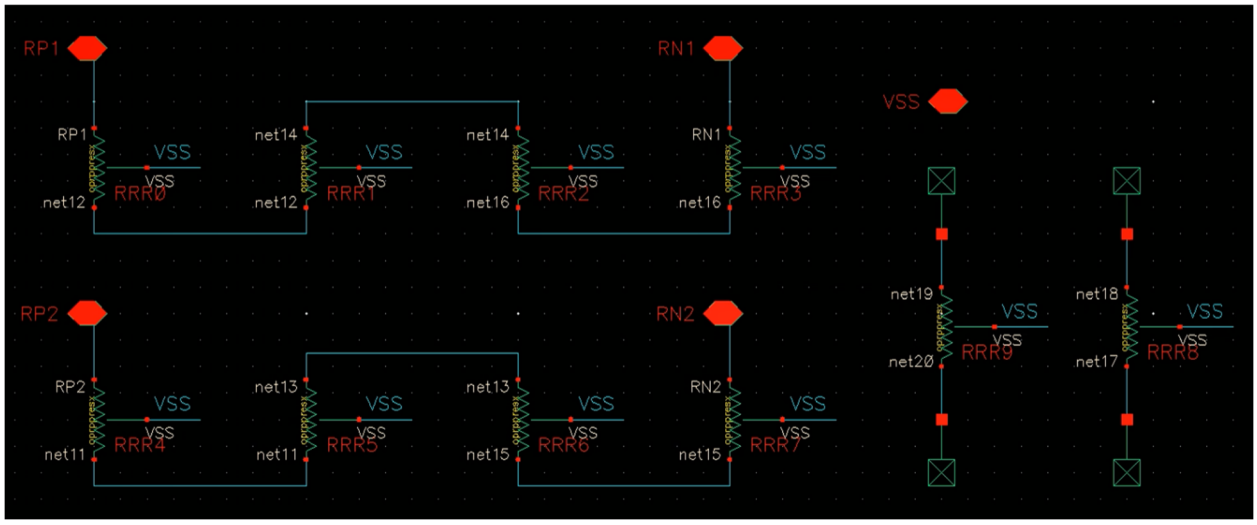

Figure 3-14: Schematic View of the Resistor Array

Similarly to the capacitors, the resistors also have a backplate node connection because parasitic capacitors and resistors can be created between the pins of the resistor and the substrate (similarly resulting in the resistor being a three-terminal device rather than a two-terminal device). As with the capacitors, a return path must be provided for the current through these parasitic elements. For this reason, the **oprppresx** component has a third terminal that must be connected to the same net (VSS in this case) as the substrate material that surrounds the resistors.

Prelab

Answer the following questions, no computer work is required for this prelab.

1. What are the absolute minimum dimensions of a transistor? Explain your reasoning. Remember to consider minimum contact size. Do we actually use this minimum size or do we use a slightly larger size for convenience?

2. Draw a common-centroid layout of a simple current mirror with equal size transistors of L = 180 nm and W = 16 µm. Use a finger width of 500 nm for each transistor segment. Remember to draw the drain, source, gate and bulk connections. Use dummy transistors and all other good layout techniques learned in the lab. Include a floor plan.

3. Design a common-centroid layout for a MOM capacitor array. The capacitors have a ratio of 1.3:1. The capacitor array should consist of eight unit capacitors (i.e. $I_1 = I_2 = 4$) and one non-unit capacitor. Determine the form of the common-centroid layout and interconnect the capacitors. Each unit capacitance should have a separate top and bottom plate. Do not use a common bottom plate. Use the techniques described in the lab manual to give good matching. Also, give the size of the non-unit capacitor. The unit capacitor is 10.56 µm x 10.56 µm (W x L).

4. Design two matched polysilicon (oprppresx) resistors to realize a total resistance of 12 kΩ each. Remember to account for contact resistance. Determine the approximate length and width of the diffusion. Use an interdigitized layout with four resistance segments for each resistor. Use good layout techniques.

Lab Report

1. Practice good layout techniques by laying out the following
   - **a.** Current mirror from prelab question #2
   - **b.** Capacitor array from prelab question #3
   - **c.** Matched resistors from prelab question #4

2. Include in the lab report
   - **a.** Schematic printout
   - **b.** Layout printout
   - **c.** LVS printout showing that the layout matches the schematic. **Note: the alternative LVS method described in Lab 2 must be used for the capacitor and resistor array layouts to get a passing LVS.**
     (Remember to include the NetID and timestamp in the screen capture.)