ECEN 474/704 Lab 6: Differential Pairs

Introduction

Differential pairs are used as the input stages of operational amplifiers and operational transconductance amplifiers, common-mode feedback circuits, and analog multipliers. As with the other fundamental building blocks, a good understanding of differential pairs is required for successful analog circuit design.

A differential pair consists of two well matched, source-coupled transistors as shown in Figure 6-1. An input voltage between the two gate terminals produces an output current in the drain terminals.

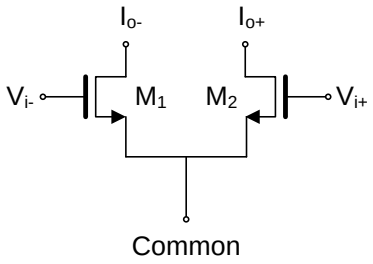

Figure 6-1: Basic Differential Pair

The most common application for a differential pair is the differential amplifier. Figure 6-2 shows the basic differential amplifier. It consists of a differential pair which is biased by the tail current source I_{tail}. Resistor R_{tail} models the output resistance of a real current source. Load resistors R_{D1} and R_{D2} allow the amplifier to develop an output voltage. The output voltage can be differential or single ended. A differential output is developed between the two output terminals, while the single ended output is taken between one output and ground.

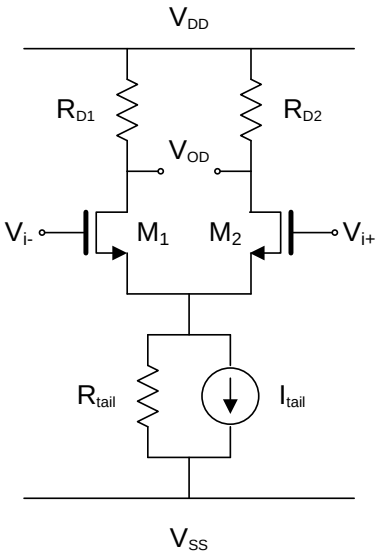

Figure 6-2: Basic Differential Amplifier

The task of the differential amplifier is to amplify the difference between its two input signals. The signals can be decomposed into two components. The first component is called the differential mode voltage V_{DM} and is given by:

$$V_{DM} = V_1 - V_2$$

The second component is called the common-mode voltage V_{CM} and is given by:

$$V_{CM} = \frac{V_1 + V_2}{2}$$

Assuming M_1 and M_2 are in saturation, neglecting the effects channel length modulation, and assuming perfectly matched transistors, the large signal characteristics can be analyzed as follows:

$$V_{DM} = V_{G1} - V_{G2} = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_{D1}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}}$$

$$I_{tail} = I_{D1} + I_{D2}$$

where $\beta = KP_N\,(W/L)$. Assuming $\beta = \beta_1 = \beta_2$ and combining both equations, we can obtain two equations describing the drain currents:

$$I_{D1} = \frac{I_{tail}}{2} + \frac{I_{tail}}{2}\sqrt{\frac{\beta V_{DM}^2}{I_{tail}} - \frac{\beta V_{DM}^4}{4I_{tail}^2}} \qquad I_{D2} = \frac{I_{tail}}{2} - \frac{I_{tail}}{2}\sqrt{\frac{\beta V_{DM}^2}{I_{tail}} - \frac{\beta V_{DM}^4}{4I_{tail}^2}}$$

These equations are only valid when M_1 and M_2 in saturation and the following relationship is satisfied:

$$|V_{DM}| \leq \sqrt{\frac{2I_{tail}}{\beta}}$$

This means that when V_{DM} is greater than or equal to the above expression, only one of the transistors is conducting and the other is off. Figure 6-3 illustrates the large signal effects as previously described.

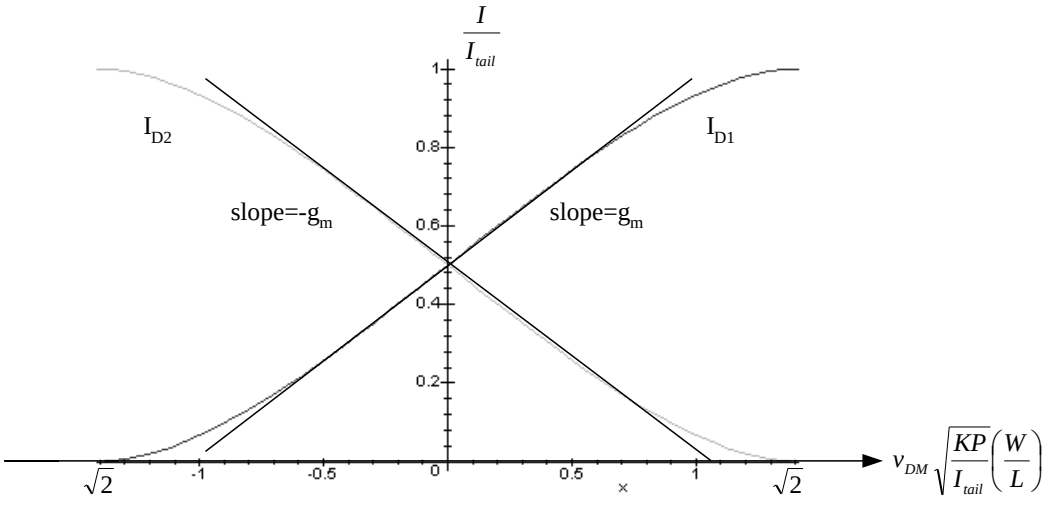

Figure 6-3: Normalized Large Signal Transconductance Characteristic of a MOS Differential Amplifier

The desired behavior of the differential amplifier is to amplify the differential-mode voltage and attenuate the common-mode voltage. The differential gain A_{DM} of an amplifier with a differential output is defined as:

$$A_{DM} = \frac{V_{OD,diff}}{V_{DM}}$$

where $V_{OD,diff}$ is the differential output voltage. For a single-ended differential amplifier, the gain is defined as:

$$A_{DM} = \frac{V_{OS}}{V_{DM}}$$

where V_{OS} is the single-ended output voltage. For an amplifier with a differential output, the common-mode gain is defined as:

$$A_{CM} = \frac{V_{OD,comm}}{V_{CM}}$$

Where $V_{OD,comm}$ is the common-mode level between the differential outputs and V_{CM} is the common-mode signal appearing at the differential inputs. And for an amplifier with a single ended output, the common-mode gain is defined as:

$$A_{CM} = \frac{V_{OS}}{V_{CM}}$$

For a symmetrical amplifier such as the fully differential amplifier, that is an amplifier with a differential output and a differential input, the common-mode voltage gain will be zero if the differential pair is perfectly matched. Due to mismatches in the differential pair or in the loads, a common-mode input voltage can cause a differential output voltage. A figure of merit for differential amplifiers is the common-mode rejection ratio (CMRR). The CMRR is defined as the ratio of the differential gain and common-mode gain:

$$CMRR = 20\log_{10}\left(\left|\frac{A_{DM}}{A_{CM}}\right|\right)$$

CMRR is, in general, frequency-dependent, like Figure 6-4 below. Therefore, plotting CMRR as a function of signal frequency requires both the differential gain response and common-mode gain responses *at the same time*. One of the simplest ways to do this is to create two instances of the amplifier in the schematic test bench, one for the differential-mode tests and one for common-mode tests, and then use the calculator to combine the results to get the CMRR plot.

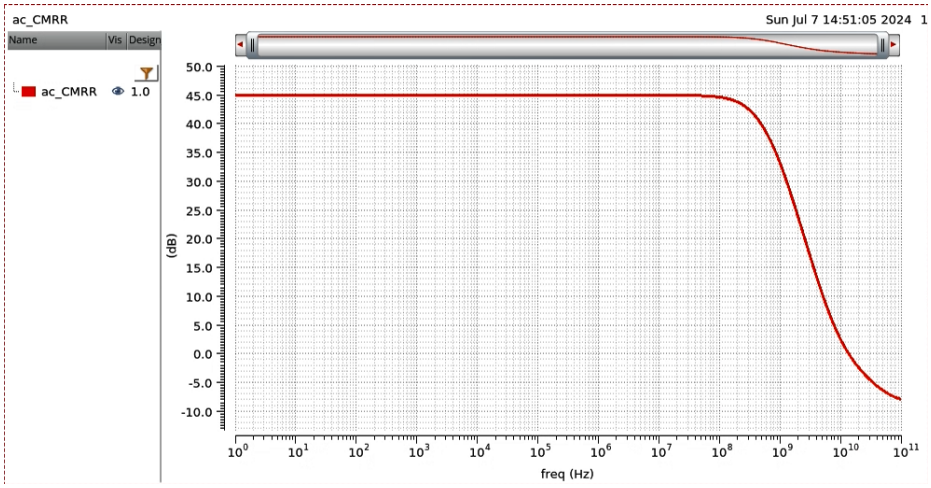

Figure 6-4: Example CMRR plot

The input common-mode voltage is limited in magnitude. The inputs must not force any of the transistors out of saturation. The limitation on the common-mode voltage creates a commo-mode voltage range for the amplifier. When the common-mode voltage increases above the upper limit, the transistors in the differential pair will leave the saturation region and enter the linear region. If the common-mode voltage decreases below the lower limit, then the transistors in the tail current source will be forced out of saturation. The common-mode voltage range can be found by considering the saturation voltages for differential pair transistors and current source transistors. Remember, for a transistor to be in saturation the overdrive voltage must not exceed the saturation voltage:

$$V_{DS,sat} = V_{GS} - V_{T0} = \sqrt{\frac{2I_D}{KP_N \frac{W}{L}}}$$

The output voltage range is also limited. For a single ended amplifier with symmetrical power supplies, the magnitude of the output signal is limited to the supply rails:

$$V_{OS} \leq |V_{DD}|$$

However, for fully differential amplifiers the output signal can be twice this amplitude. Each output can swing to a supply rail, giving a differential output voltage that is twice as large as either rail. As with all amplifiers, another limit on the output voltage swing is the allowable distortion. An output signal swing which comes within 200 mV of the supply rails may have 10% THD. And a signal which comes within 500 mV may have only 1% THD in the same circuit. The output voltage range is dictated by the distortion requirement.

The input-output characteristic curves of the differential amplifier are shown in Figure 6-5. The region where the input is approximately zero volts is linear. The size of the linear region is determined by the transistor sizes. Decreasing the transistor sizes will decrease the transconductance and increase the size of the linear region.

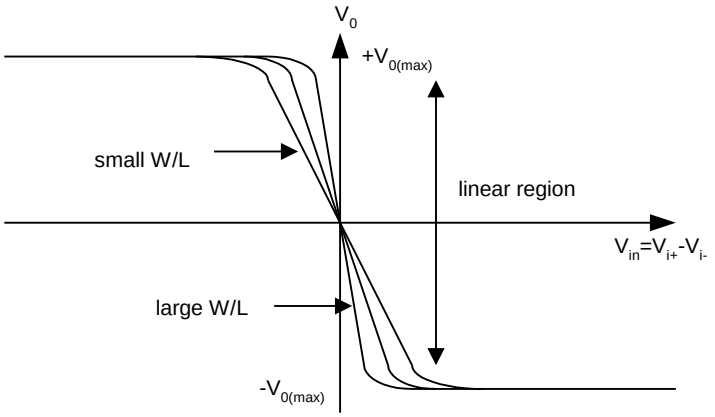

Figure 6-5: Input-Output Characteristic Curves for a Differential Amplifier

The amplifier also has an input and output impedance. The differential input resistance and the common-mode input resistance are large for MOSFET differential amplifiers. The differential input resistance is the resistance between the two input terminals. The common-mode input resistance is the resistance measured between the two interconnected inputs and ground.

The output impedance can also be measured in two different ways. For fully differential amplifiers, the differential output resistance is the resistance between the two output terminals. For single ended amplifiers, the common-mode output resistance is the resistance measured between the output and ground.

Another figure of merit for the differential amplifier is its power supply rejection ratio (PSRR). This ratio indicates the effect of power supply variations or noise on the output voltage. For fully differential amplifiers with perfect matching in the differential pair and load, the PSRR is infinity. PSRR is given by:

$$PSRR^{+} = 20\log_{10}\left(\left|\frac{A_{DM}}{V_0/V_{DD}}\right|\right) \qquad PSRR^{-} = 20\log_{10}\left(\left|\frac{A_{DM}}{V_0/V_{SS}}\right|\right)$$

The slew rate is a measure of how quickly the output of the differential amplifier can change in response to an instantaneous rail-to-rail (large signal) change in the input voltage.

Due to process variations, the differential pair will not be perfectly matched. As a result, for equal input voltages, the drain currents will not be equal. Also, if the load is asymmetrical, then a non-zero output voltage will exist. The voltage at the input which forces the output voltage to zero is called the input offset voltage.

Simple Differential Amplifier

Figure 6-6 illustrates the simple differential amplifier. This circuit consists of a differential pair biased by a simple current mirror. The active load is a PMOS current mirror.

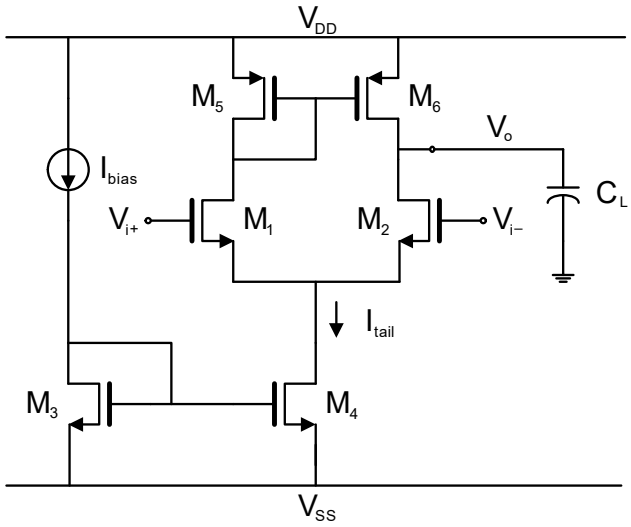

Figure 6-6: Simple Differential Amplifier

Differential Gain:

The differential gain of this circuit is given by:

$$A_{DM} = G_m R_{out} = g_{m1}(r_{02}||r_{06})$$

Slew Rate:

Slewing is a condition during which the rate of change in the output voltage is limited to approximately a fixed rate. Slewing is a large-signal behavior rather than a small-signal one. For this circuit, slewing occurs when the differential input voltage is large enough such that one of the transistors in the input pair is turned off, thereby steering all of the I_{tail} current through the other transistor in the pair. This leads to a fixed current (neglecting variations caused by channel-length modulation) charging or discharging the output capacitor which results in a fixed rate of change for the voltage across the capacitor. The biasing current and the amount of load capacitance determine the slew rate (SR), which is given by:

$$SR = \frac{I_{tail}}{C_L}$$

Gain-Bandwidth Product and Dominant Pole:

Since the output node is a high impedance node, the dominant pole is located at:

$$\omega_{p1} = \frac{1}{R_{out}C_L}$$

The gain-bandwidth product is given by:

$$\omega_{GBW} = A_{DM}\omega_{p1} = \frac{G_m R_{out}}{R_{out}C_L} = \frac{g_{m1}}{C_L}$$

Common-Mode Voltage Range:

As mentioned previously, the common-mode voltage range is the range of input voltages which keep the current source and active load transistors in saturation. The common-mode voltage range is determined by the sizes of the transistors. To increase the common-mode voltage range, the sizes of the transistors must be increased. The common-mode voltage range is given by:

$$V_{SS} + \sqrt{\frac{2I_{tail}}{KP_N\left(\frac{W}{L}\right)_{3,4}}} + \sqrt{\frac{I_{tail}}{KP_N\left(\frac{W}{L}\right)_{1,2}}} + V_{TN} < V_{in(CM)} < V_{DD} - \sqrt{\frac{I_{tail}}{KP_P\left(\frac{W}{L}\right)_{5,6}}} - |V_{TP}| + V_{TN}$$

To quantify the common-mode voltage range, the "region" parameter of the transistors can be used to determine when they enter the active region. Refer to the Lab 5 manual for more information regarding how to plot the region parameter from a DC sweep simulation. Then, sweep the DC level of the common-mode input voltage of the amplifier from one supply voltage to the other and find the region for which the transistors are in the active region. **The common-mode input voltage range must be determined for an amplifier before additional simulations to ensure that the DC operating point of the amplifier is appropriately set, thereby allowing the amplifier to function properly.**

Common-Mode Gain:

To design for common-mode, we can no longer assume that there exists an AC signal ground at the source of M_1 and M_2. This current source must be substituted by a resistor of value equal to the output resistance of the current mirror. To help in the development of the design equations, Figure 6-7 is used.

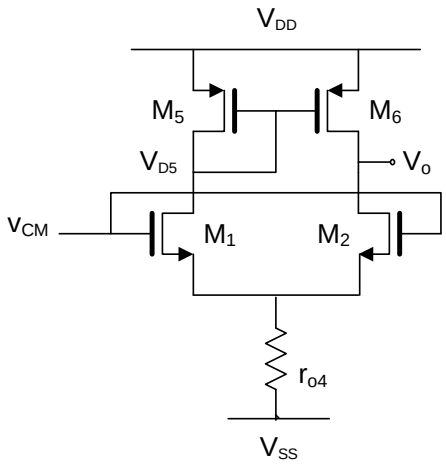

Figure 6-7: Differential Amplifier Used to Determine CMRR

From this figure, the voltage gain from V_{CM} to V_{D5} can be found as:

$$\frac{V_{D5}}{V_{CM}} \approx \frac{-\frac{1}{g_{m5}}}{2r_{o4}+\frac{1}{g_{m1}}} \approx -\frac{1}{2r_{o4}g_{m5}}$$

Assuming perfect matching between M_1 & M_2, and M_5 & M_6, it can be shown that V_o=V_{D5}. Therefore, the common-mode gain is given by:

$$A_{CM} = \frac{V_o}{V_{CM}} = -\frac{1}{2r_{o4}g_{m5}}$$

As can be seen from this equation, the CMRR can be improved by increasing the output impedance of the tail current source:

$$CMRR = 20\log_{10}\left(\left|\frac{A_{DM}}{A_{CM}}\right|\right) = 20\log_{10}(|g_{m1}(r_{02}||r_{06})2r_{04}g_{m5}|)$$

Simple Differential Amplifier with Cascode Current Mirror as the Active Load and Tail Current

The second differential amplifier is shown in Figure 6-8. This circuit utilizes low-voltage cascode current mirrors as the tail current source and the active load. The design equations for this structure are the same as the previous structure except the output impedance of the amplifier and current source are now larger. This will increase differential-mode gain while decreasing common-mode gain, thus a vastly improved CMRR. The main drawback of this circuit is a reduced input common-mode range and output swing.

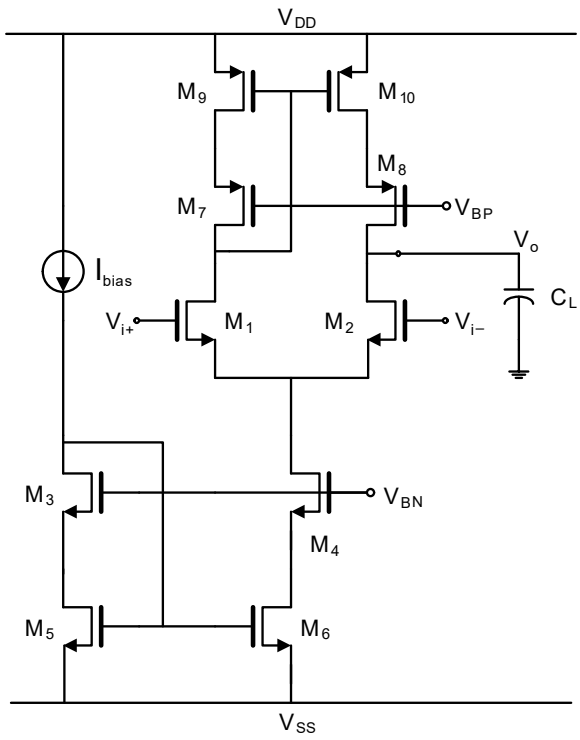

Figure 6-8: Differential Amplifier with Cascode Current Mirror as the Active Load and Tail Current

Differential Gain:

The differential gain of this circuit is given by:

$$A_{DM} = G_m R_{out} = g_{m1}\left(r_{02} || (r_{08} + r_{010} + g_{m8} r_{08} r_{010})\right) \approx g_{m1} r_{02}$$

Slew Rate:

As with the previous circuit, slewing occurs when the differential input signal is large to turn off one of the transistors in the input pair and steer all of I_{tail} through one branch of the circuit. The biasing current and the amount of load capacitance determine the slew rate (SR), which is given by:

$$SR = \frac{I_{tail}}{C_L}$$

Gain-Bandwidth Product and Dominant Pole:

Since the output node is a high impedance node, the dominant pole is located at:

$$\omega_{p1} = \frac{1}{R_{out} C_L}$$

The gain-bandwidth product is given by:

$$\omega_{GBW} = A_{DM} \omega_{p1} = \frac{G_m R_{out}}{R_{out} C_L} = \frac{g_{m1}}{C_L}$$

Common-Mode Voltage Range:

The common-mode voltage range for this differential amplifier is given by:

$$V_{in(CM)} > V_{SS} + \sqrt{\frac{2I_{tail}}{KP_N\left(\frac{W}{L}\right)_6}} + \sqrt{\frac{2I_{tail}}{KP_N\left(\frac{W}{L}\right)_4}} + \sqrt{\frac{I_{tail}}{KP_N\left(\frac{W}{L}\right)_1}} + V_{TN1}$$

$$V_{in(CM)} < V_{DD} - \left(\sqrt{\frac{I_{tail}}{KP_P\left(\frac{W}{L}\right)_9}} + |V_{TP9}|\right) + V_{TN1}$$

Common-Mode Gain:

The common-mode gain can be expressed as:

$$A_{CM} \approx -\frac{1}{2R_{SS}g_{m9}} \quad , \qquad R_{SS} = r_{04} + r_{06} + g_{m4}r_{04}r_{06}$$

Therefore, the CMRR can be found as:

$$CMRR = 20\log_{10}\left(\left|\frac{A_{DM}}{A_{CM}}\right|\right) \approx 20\log_{10}(2g_{m1}g_{m4}g_{m9}r_{02}r_{04}r_{06})$$

Schematic Test Bench Setup Information

To get the required measurements for this lab, both differential and common-mode signals will need to be applied to the inputs of the two amplifiers discussed above. One of the simpler methods of implementing these kinds of signals in the simulation test bench environment is with the use of the **ideal_balun** component from the **analogLib** library, as shown in Figure 6-9.

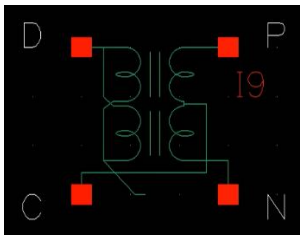

Figure 6-9: ideal_balun component from the **analogLib** library for applying differential and common-mode signals in a schematic test bench

The **ideal_balun** component has four terminals, as shown. Although it is drawn like a center-tapped transformer, the **ideal_balun** component works with both DC and AC signals. The terminal labeled "D" is the differential input terminal. A signal applied to the D terminal will be converted into two signals, one at the "P" terminal and one at the "N" terminal. Each signal that is generated will have half the original signal amplitude and will be 180° out of phase from each other. The P terminal is the in-phase signal (i.e. the phase of the P terminal's signal aligns with the phase of the original signal at the D terminal). The "C" terminal is the common-mode input terminal. A signal applied to the C terminal will appear at both the P

and N terminals without modification. Therefore, the signal at the C terminal sets the average value (i.e. the common-mode level) between the P and N output terminals, and as mentioned this signal can contain both DC and AC components. One voltage source can be connected to each of the balun's input terminals in order to easily control both the differential-mode and common-mode signals applied to the circuits. However, when simulating the circuits, only one kind of signal (differential-mode or common-mode) can be present to characterize the respective response. I.e. characterization of the differential-mode gain requires that there be no AC common-mode component at the circuit's input. Likewise, characterization of the common-mode gain requires that there be no AC differential-mode component at the input.

The slew rate needs to be measured from simulations. Because slewing is a large-signal behavior, it cannot be determined from AC simulations. Instead, transient simulations must be used because transient simulations utilize the complete model of the circuit elements at every timestep and therefore incorporate the large-signal behaviors. Recall that the small-signal analysis done by hand and the AC analyses performed in the simulator are linearizations of nonlinear devices, and these linearizations are performed around the circuit's DC operating point. However, the circuit elements themselves are always operating according to the large-signal model. Small-signal analysis is a mathematical tool for building intuition of the circuit's behavior under certain operating conditions.

To determine the slew rate, a signal with either a large enough amplitude or having a high enough frequency (or an appropriate combination of the two) must be applied to the inputs of the circuits. If a sine wave input is used, then the result of slewing will cause the steady-state output voltage of the circuit to be distorted into a signal that resembles a triangle wave, like what is shown in Figure 6-10. The slew rate can then be measured as the maximum rate of change (i.e. the slope) of the triangular output waveform.

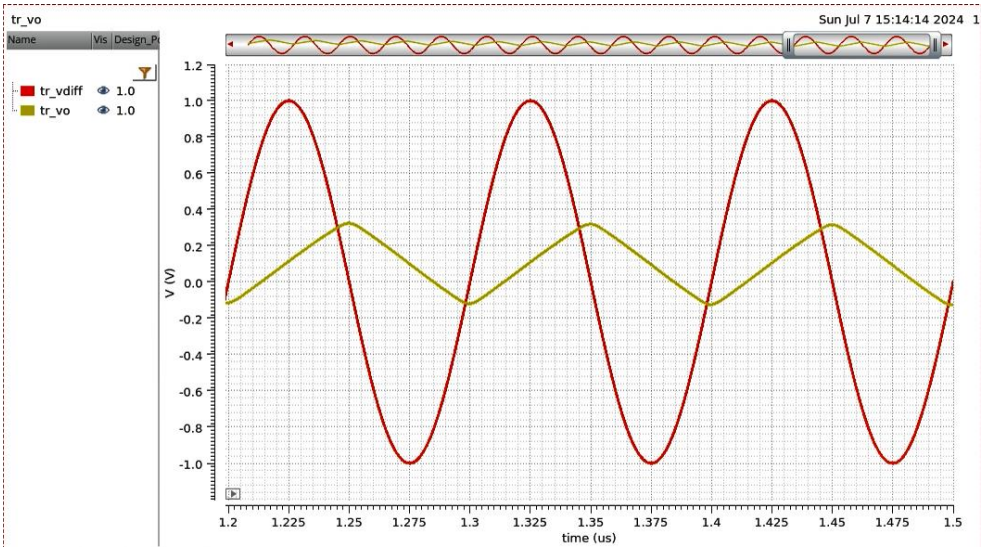

Figure 6-10: example transient simulation demonstrating slew-rate limitations at the output voltage

When setting up AC and transient simulations recall that, as mentioned in Lab 1, the AC magnitude field is treated separately from other amplitude fields in sources that provide a transient waveform. For these sources, there are multiple amplitude fields. One of them is the "AC magnitude" field. The other may refer simply to an amplitude (like in the sinusoidal, or **vsin**, source), without mention of an analysis type. If the other fields do not mention "AC" (or some other analysis type) in the parameter name, then they are generally for transient simulations. **In other words, a source's magnitude in AC simulations and its magnitude in transient simulations are completely independent from each other.**

Prelab

1. Compare the two single-ended differential amplifiers discussed in this lab. Rate the differential gain, common-mode gain, output voltage swing range, CMRR and common-mode input voltage range. Include expressions for each design specification.
2. Design the simple differential amplifier in Figure 6-6 to obtain the following specifications:

Slew Rate	> 10 V/µs
Gain-Bandwidth Product	> 5 MHz
Common-mode Input Voltage Range	> 0.5 V
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V
Load Capacitance	10 pF

3. Design the differential amplifier with cascode current mirrors in Figure 6-8 to obtain the following specifications:

Slew Rate	> 10 V/µs
Gain-Bandwidth Product	> 5 MHz
CMRR	> 60 dB
Power Supply	$V_{DD} = -V_{SS} = 0.9$ V
Load Capacitance	10 pF

You may assume that VBP and VBN are bias voltages that are provided to the amplifier at the level of the test bench (i.e. these voltages do not need to be generated within the amplifier schematic and layout). They can be additional pins on the amplifier schematic symbol.

Lab Report

1. Simulate the designs from the prelab, measure (include formulas used, do not derive them) and plot (use markers, remember the "m" hotkey):

   a) Common-mode range
   b) Differential-mode gain
   c) Common-mode gain
   d) CMRR
   e) GBW
   f) Dominant pole f_{p1}
   g) Slew rate

   Use any analysis necessary to obtain the most accurate measurements. Modify your design as necessary to meet the given specifications. Include these results in the lab report.

2. Layout the final designs. Use good layout techniques. Repeat the above measurements. Be sure to include parasitic capacitance in the layout extraction. Include these results in your lab report as well as the LVS report (again NetID and time stamp required for credit).