

24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab7: Frequency Response of Inverting Amplifiers

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Section:601

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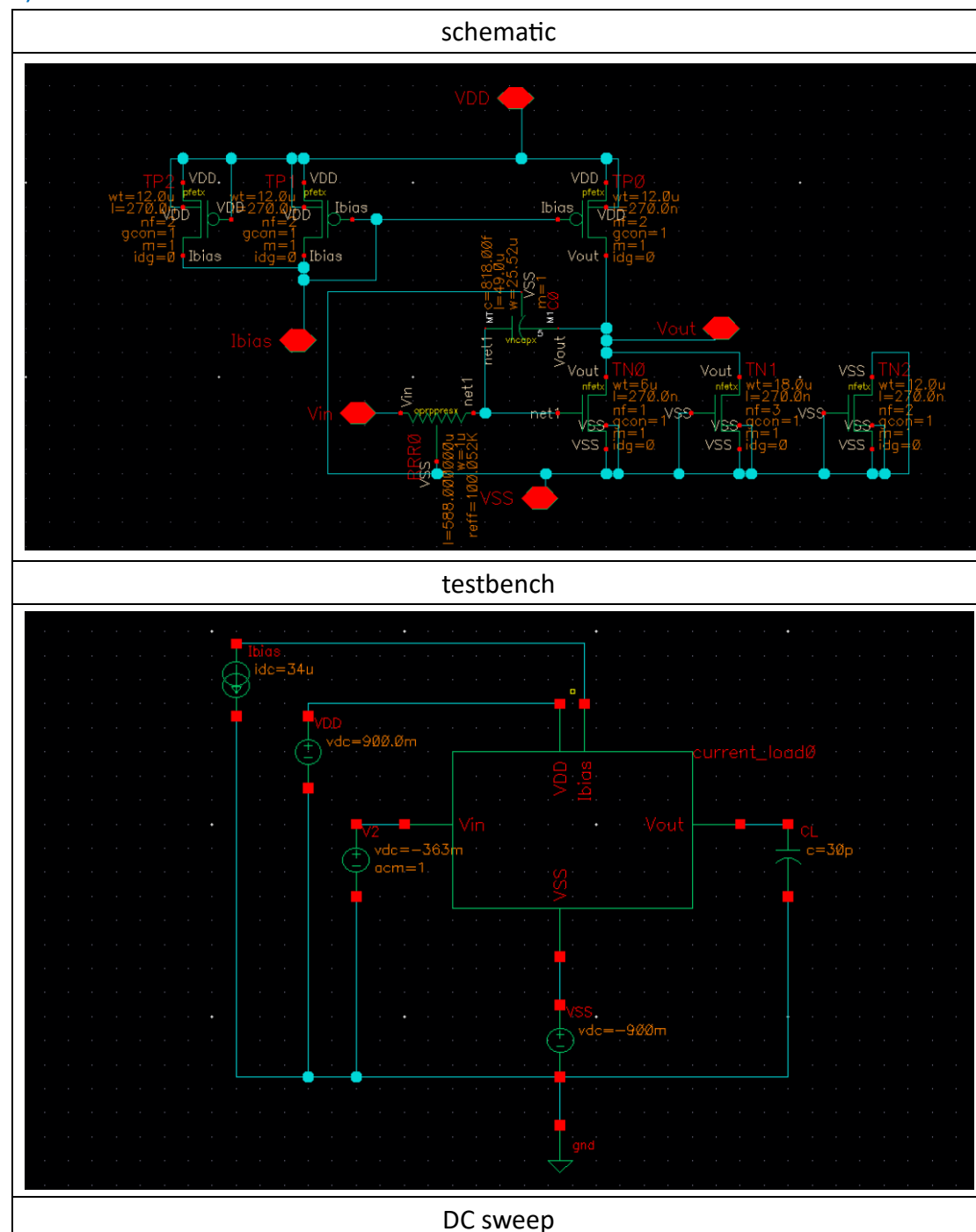
TA: Troy Buhr

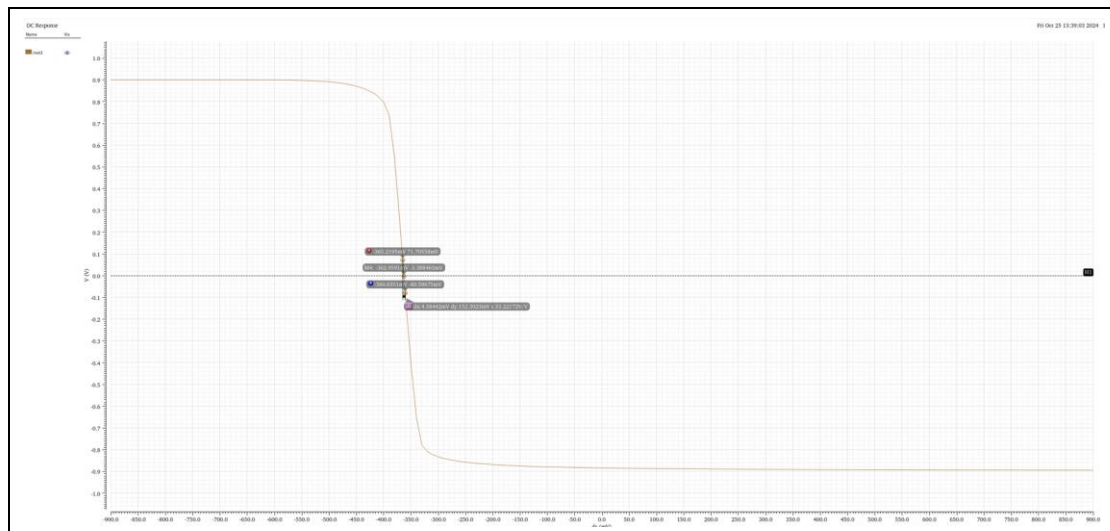
Description:

Lab 7 emphasizes the importance of analyzing and designing inverting amplifiers. Inverting amplifiers are essential components in electronic circuit design, serving key roles in applications such as gain stages in operational amplifiers and NOT gates in digital circuits. Understanding their frequency response is crucial for designing circuits that function reliably across different frequencies.

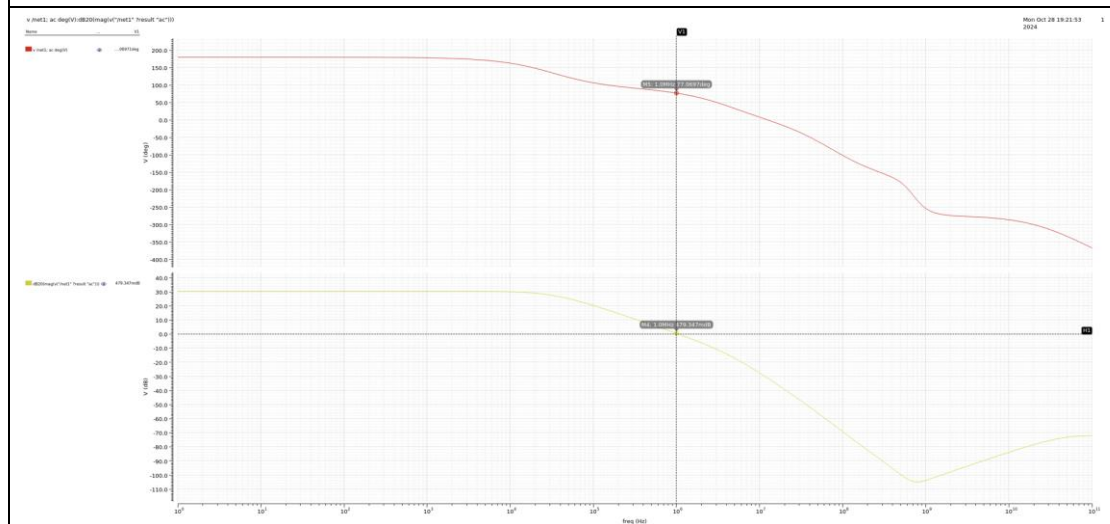
Design & result

a) Current mirror load inverter



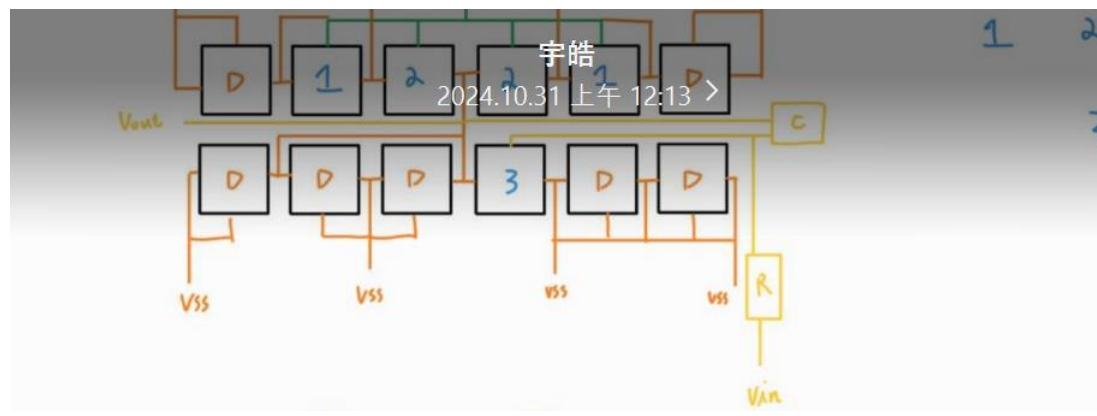


AC Freq

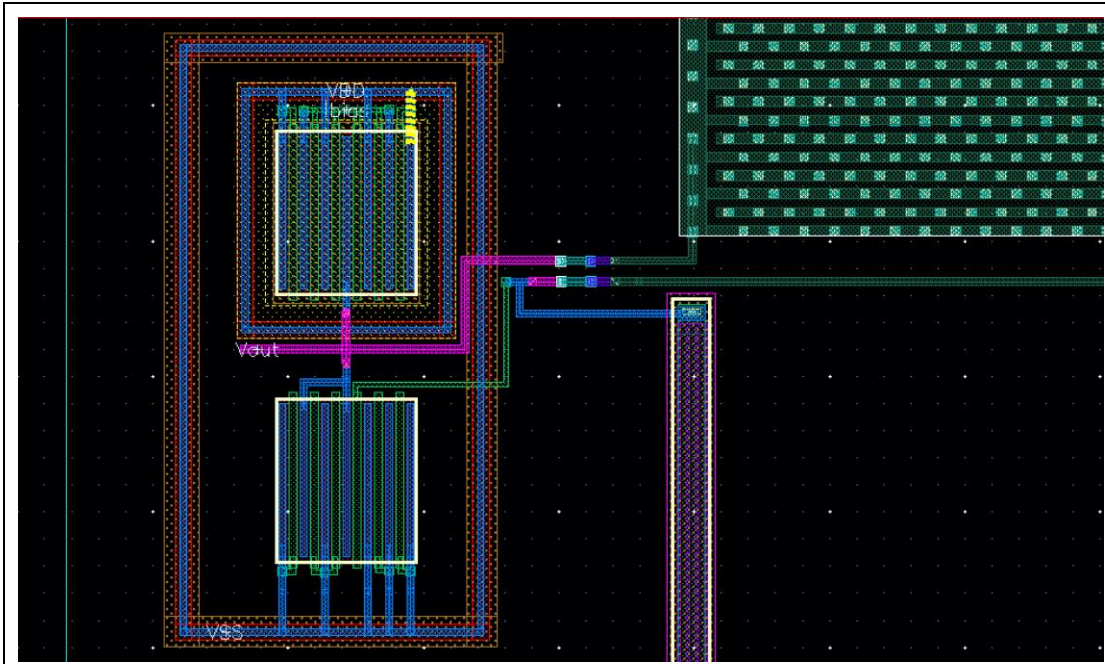


- Phase margin = 180 – phase shift -> phase margin = 77 phase shift = 103

Floor Plan



Layout



LVS

Virtuoso® Schematic Editor: L Editing: lab7 current_mirror_load schematic@n03-poseidon.olympus.ece.tamu.edu

Launch File Edit View Create Check Options Window Calibre IBM_PDK Help

Basic

File Settings Configurations Help

Rules
Inputs
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current_mirror_load.lvs.report

```

#####
10 #####
11 #####
12 #####
13 #####
14 REPORT FILE NAME: current_mirror_load.lvs.report
15 LAYOUT NAME: current_mirror_load.sp ('current_mirror_load')
16 SOURCE NAME: /home/grads/h/harrison900531/LVS/
17 current_mirror_load.netlist.lvs ('current_mirror_load')
18 RULE FILE: cmhv7sf.lvs.cal
19 CREATION TIME: Mon Oct 28 21:36:46 2024
20 CURRENT DIRECTORY: /home/grads/h/harrison900531/CAL
21 USER NAME: harrison900531
22 CALIBRE VERSION: v2024.2_29.16 Thu May 2 07:35:42 PDT 2024
23
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```

OVERALL COMPARISON RESULTS

```

#####
30 #####
31 #####
32 #####
33 #####
34 #####
35 #####
36 #####

```

Run LVS

Show RVE

Calibre - RVE v2024.2_29.16: svdb current_mirror_load

File View Highlight Tools Window Setup Help

Search

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Results
Extraction Results
Comparison Results
ERC
ERC Results
Reports
Extraction Report
LVS Report
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Rules File
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Comparison Results

Layout Cell / Type	Source Cell	Nets	Instances	Ports
current_mirror_load	current_mirror_load	6L, 6S	SL, SS	SL, SS

Cell current_mirror_load Summary (Clean)

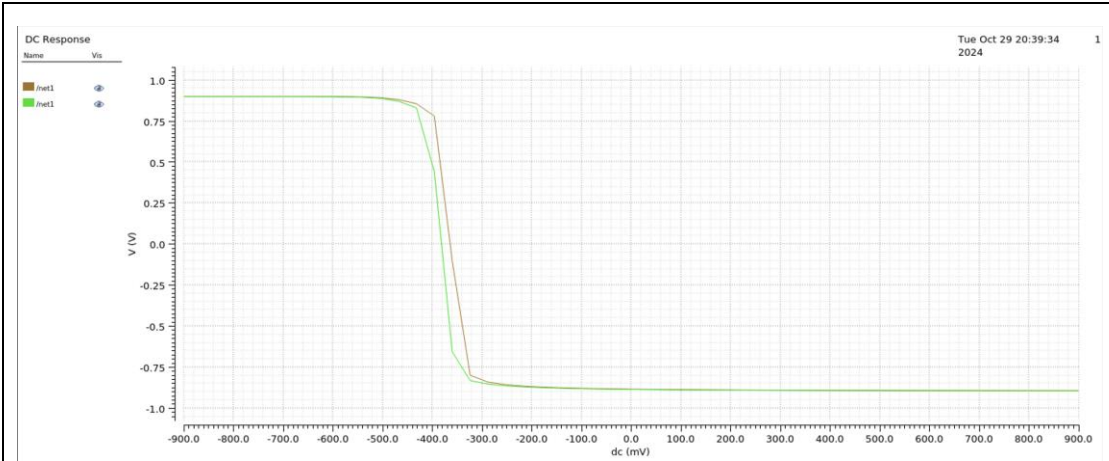
CELL COMPARISON RESULTS (TOP LEVEL)

LAYOUT CELL NAME: current_mirror_load
SOURCE CELL NAME: current_mirror_load

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	5	5	
Nets:	6	6	
Instances:	6	3	MN (4 pins)
	6	3	MP (4 pins)

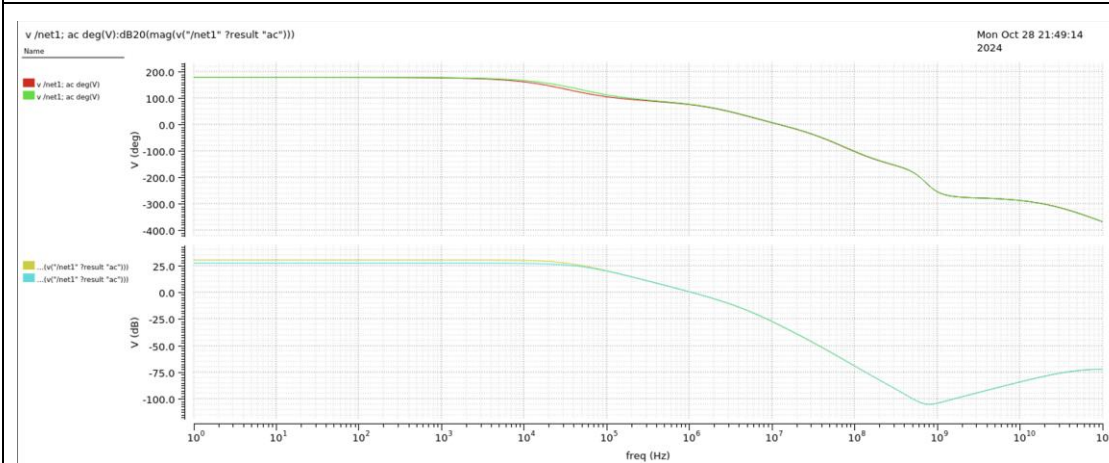
Post layout



Red line: schematic

Green line: layout

Post layout



Red line: schematic phase

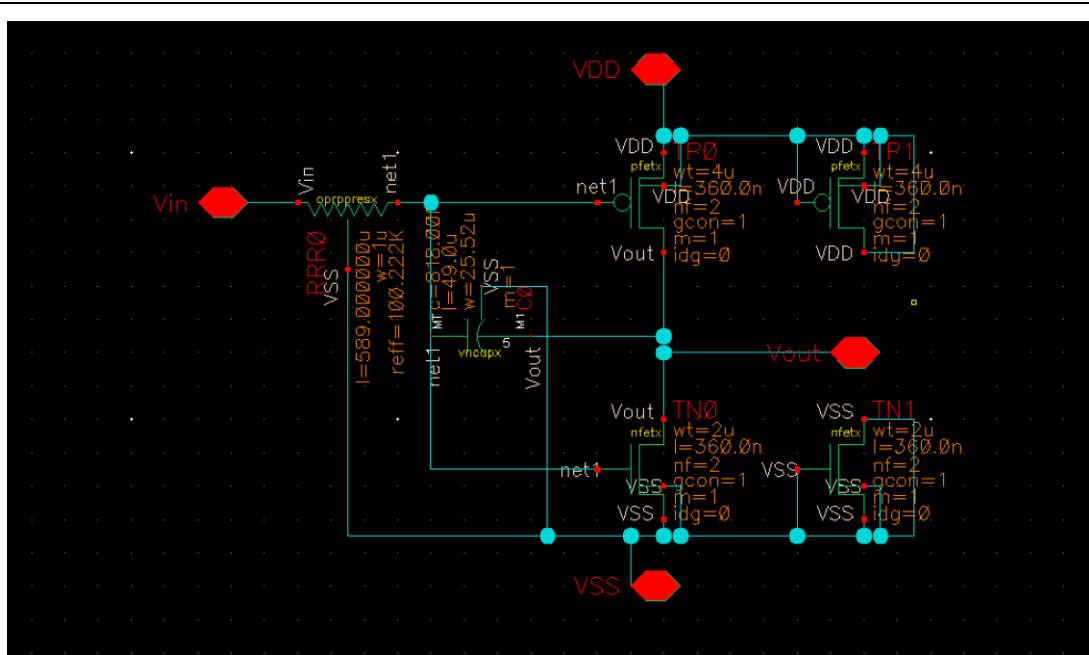
Green line: layout phase dB

Yellow line: schematic AC gain dB

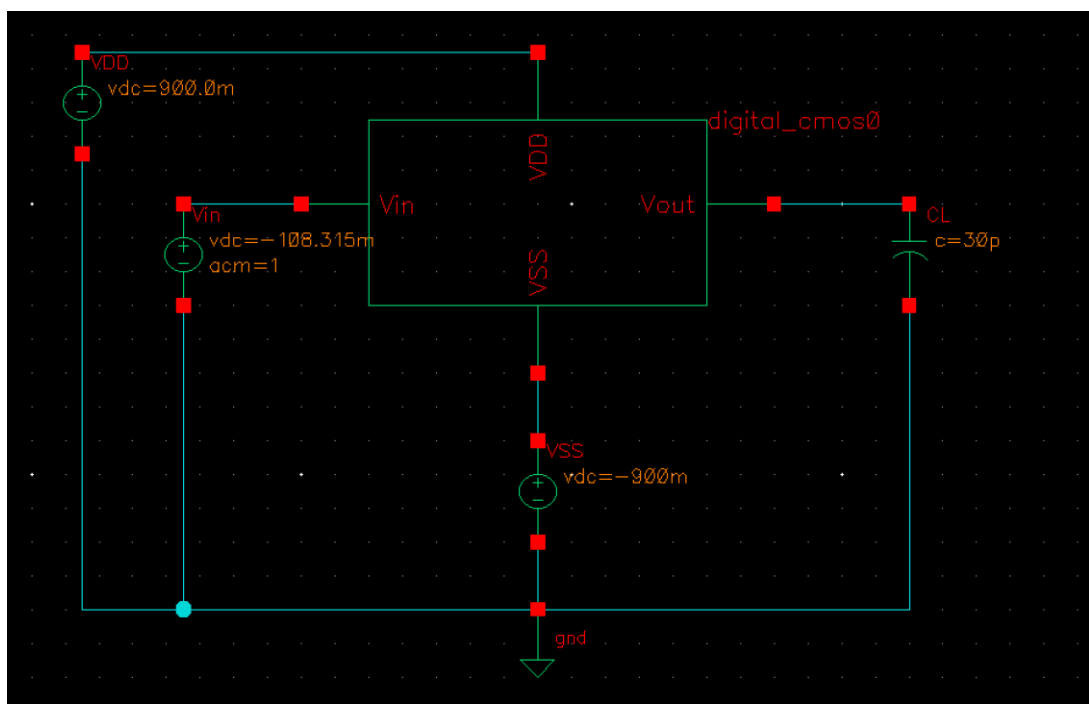
Blue line: layout AC gain dB

b) Digital CMOS inverter

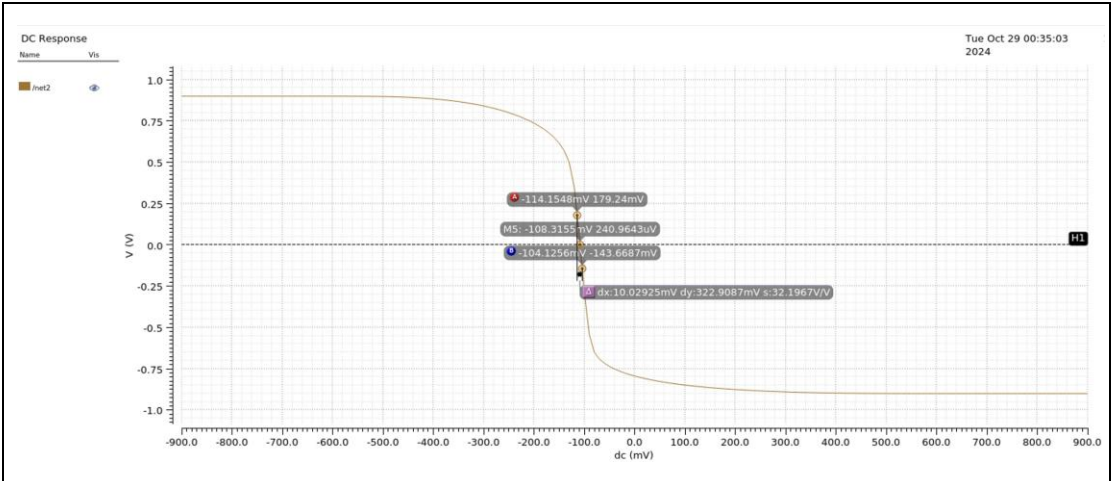
schematic



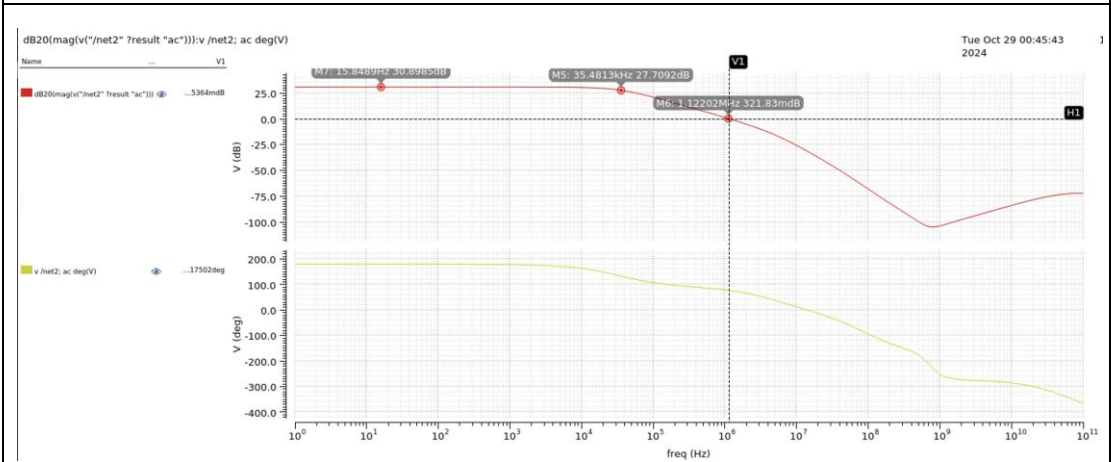
testbench



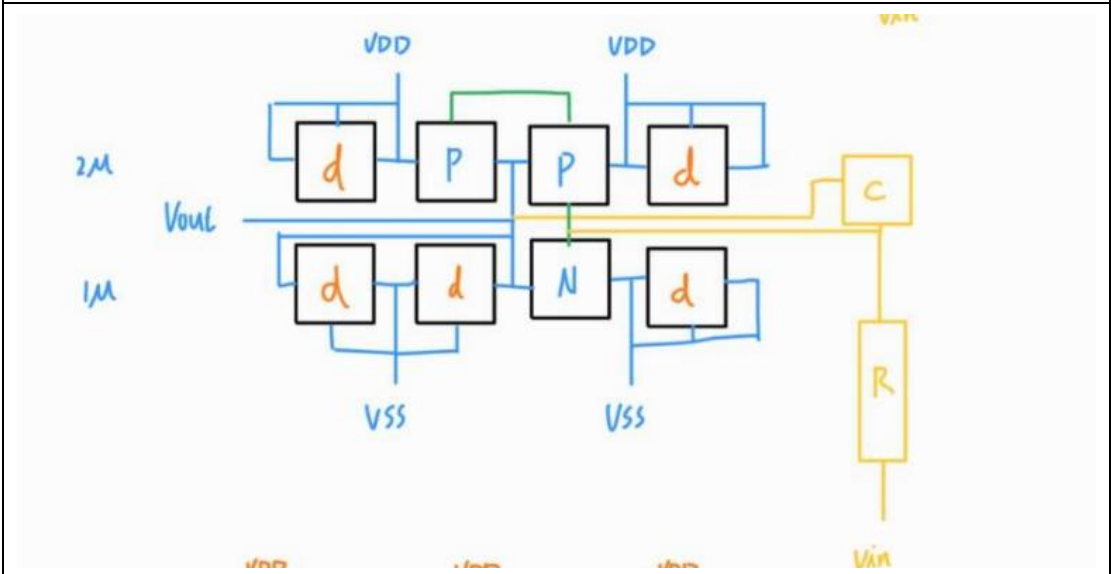
DC sweep



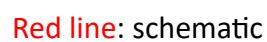
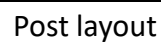
AC Freq



Floor Plan

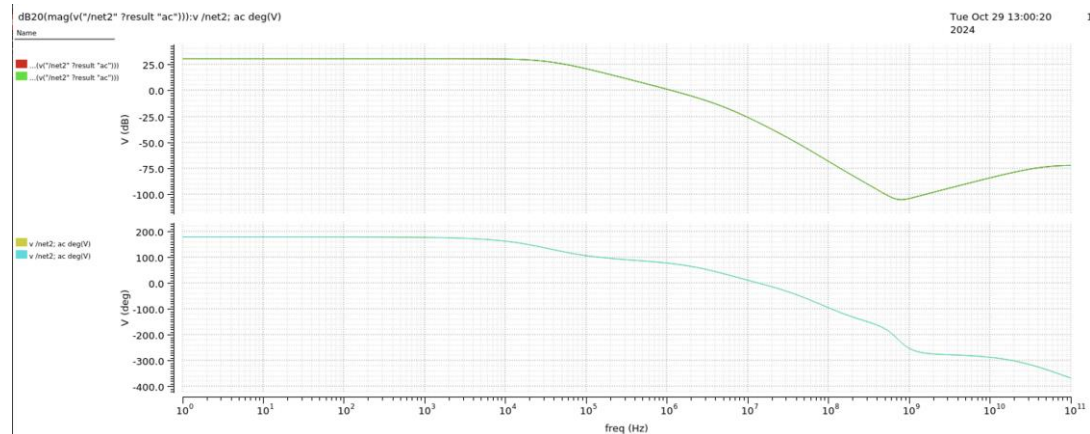


Layout



Green line: layout

Post layout



Red line: schematic AC gain dB

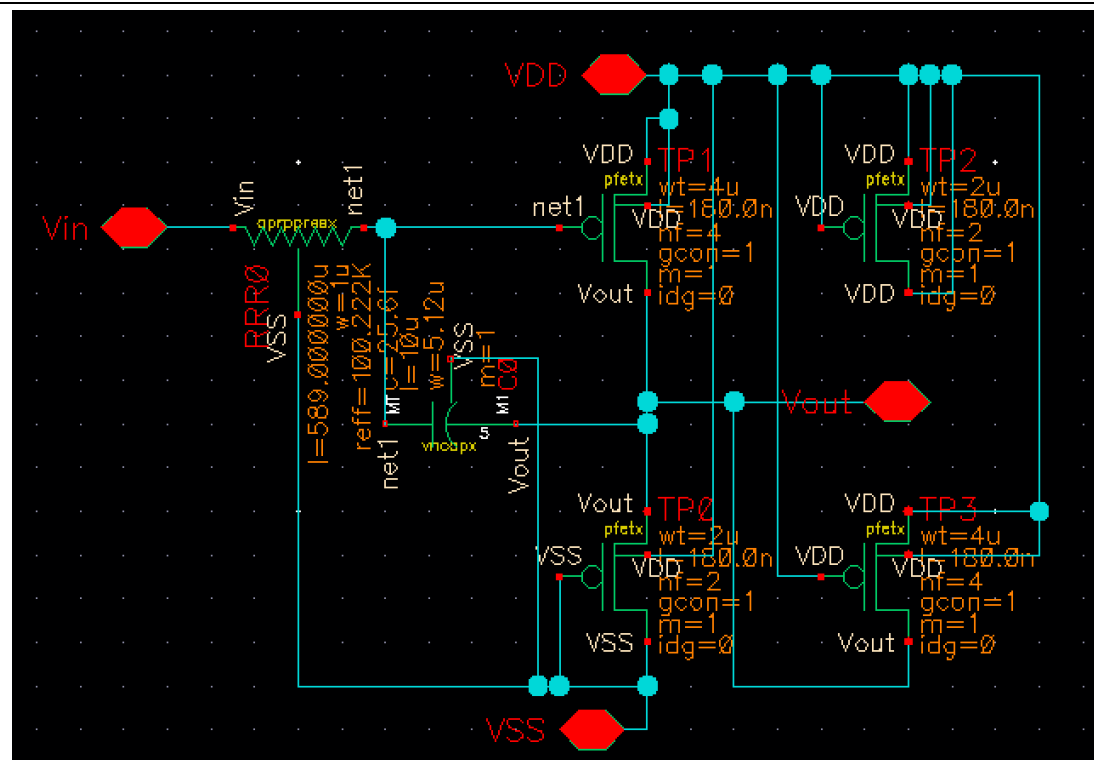
Green line: layout AC gain dB

Yellow line: schematic phase

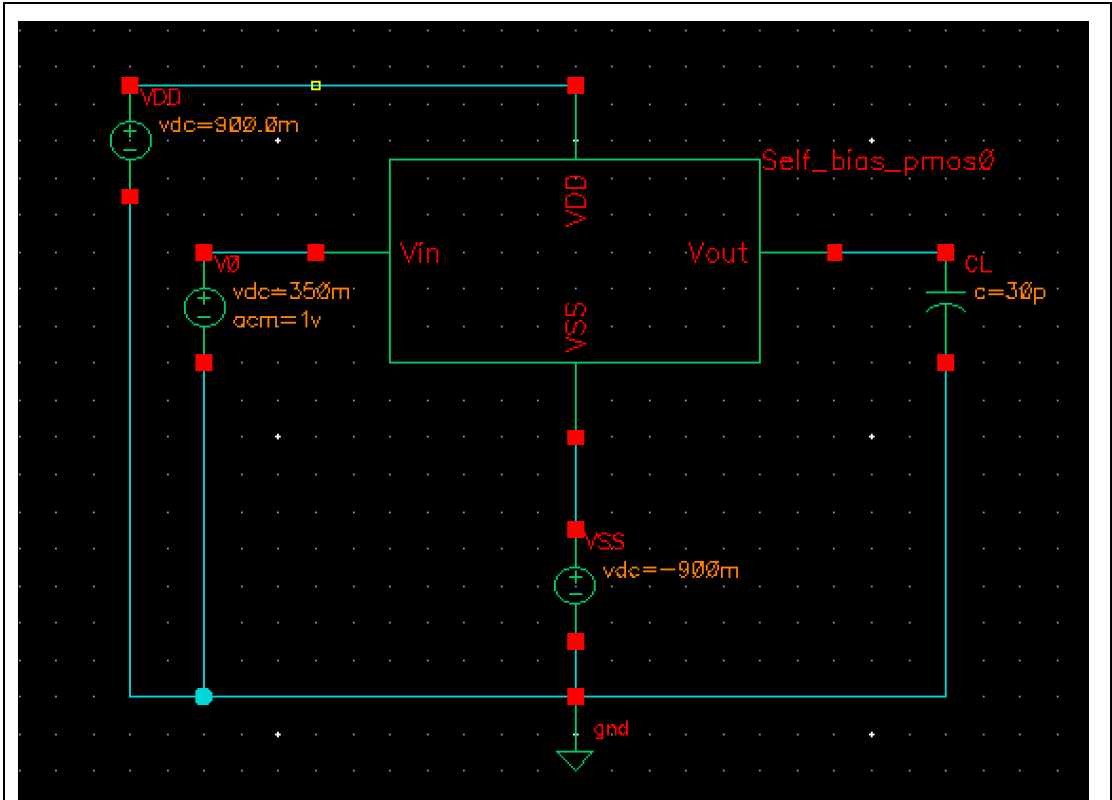
Blue line: layout phase

c)

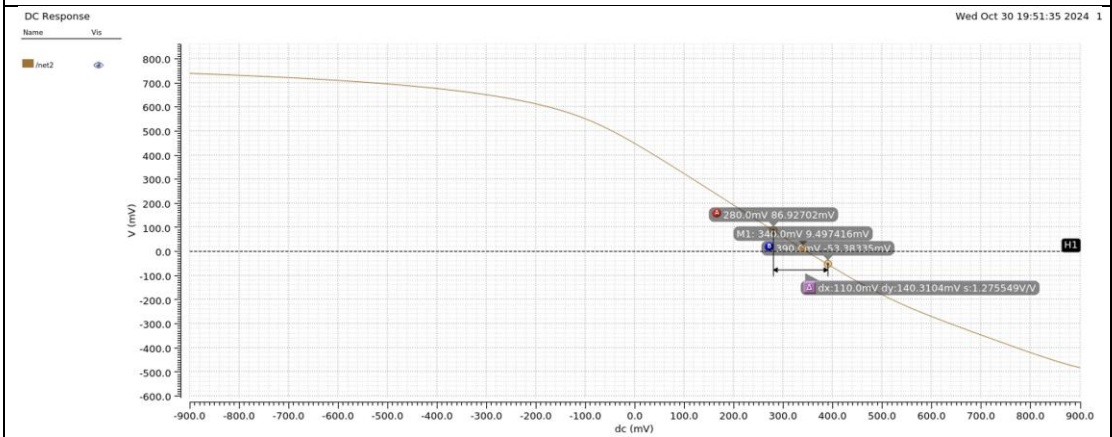
schematic



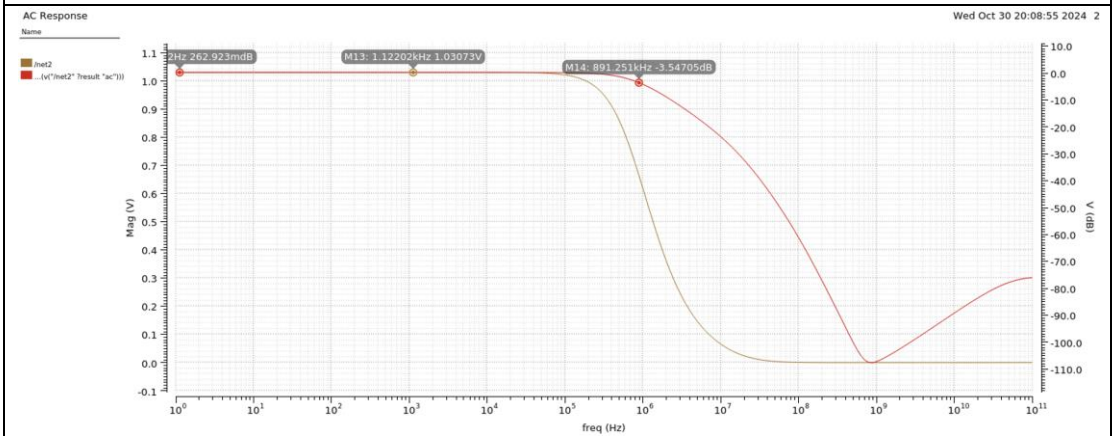
testbench



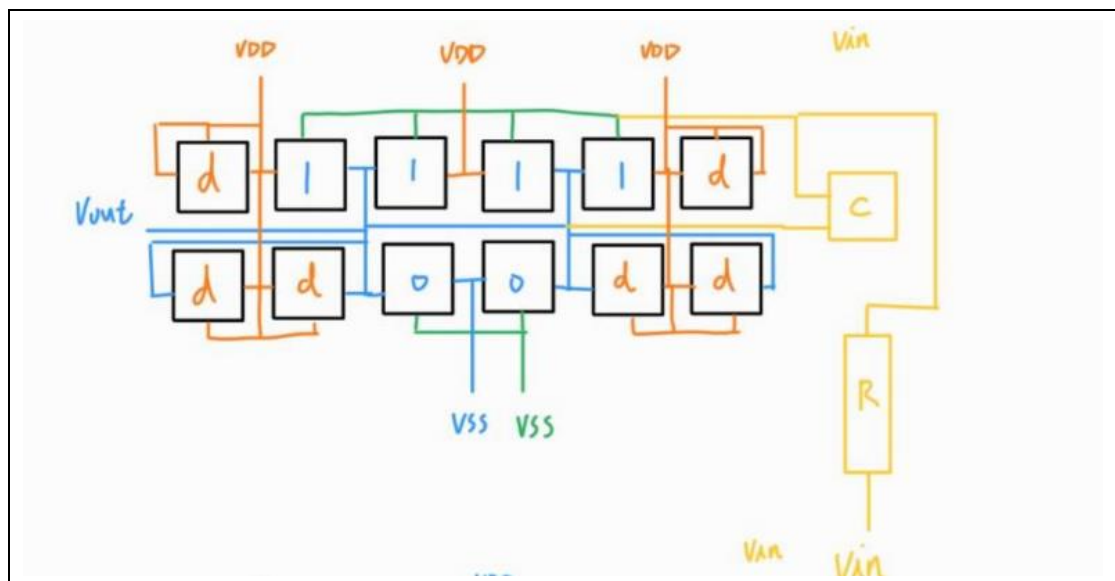
DC sweep



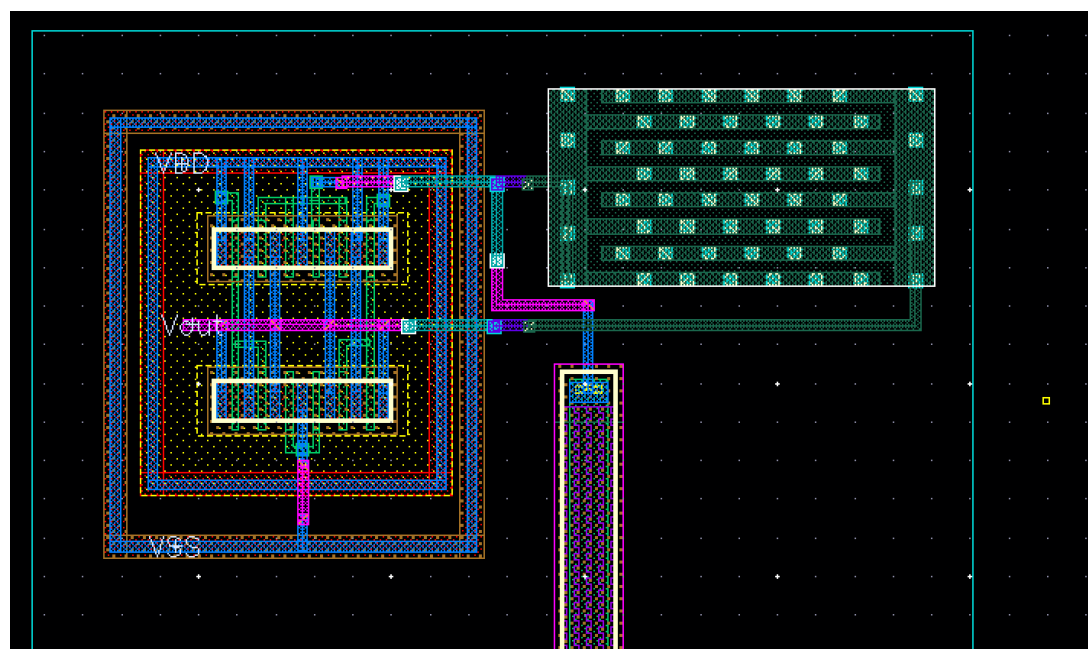
AC Freq



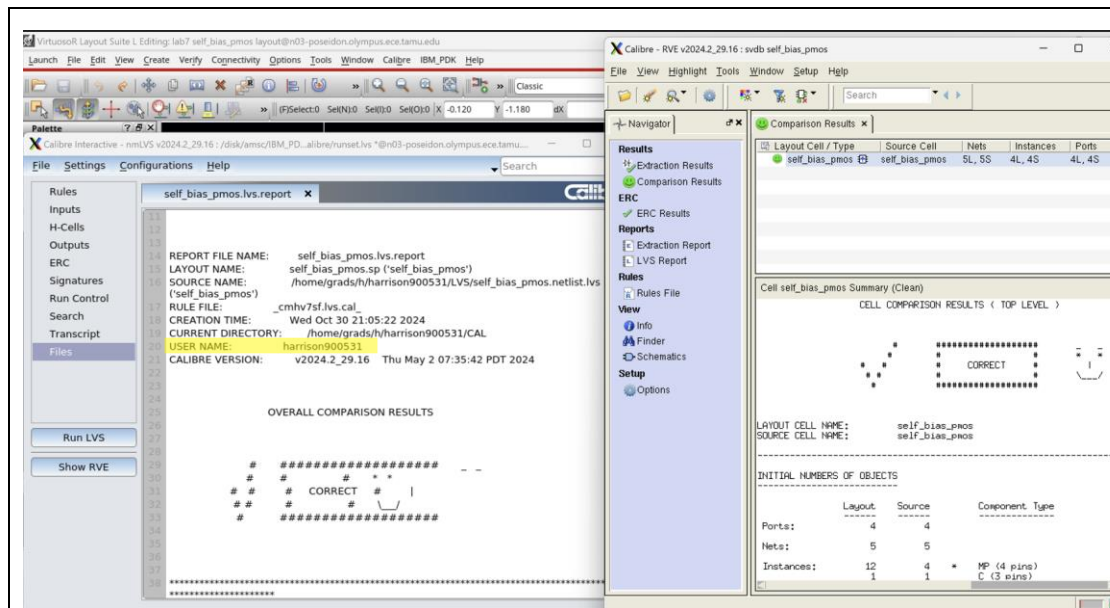
Floor Plan



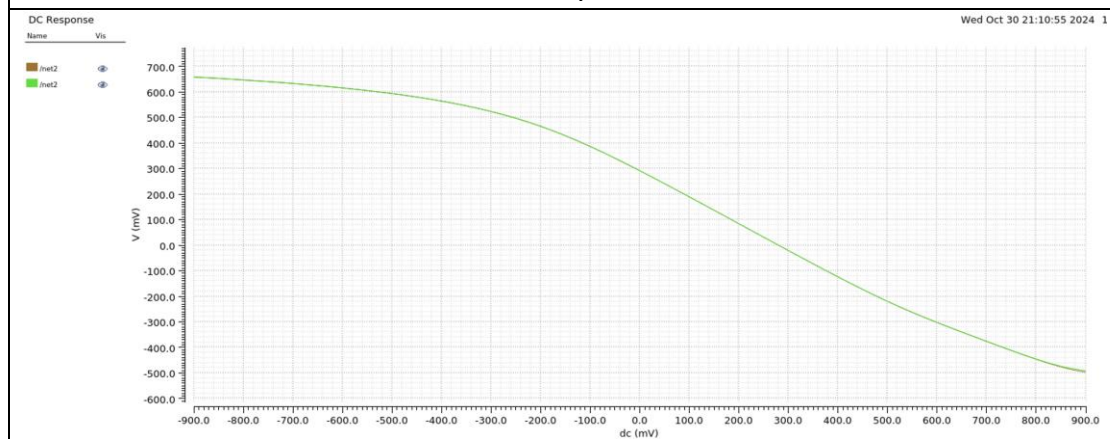
Layout



LVS



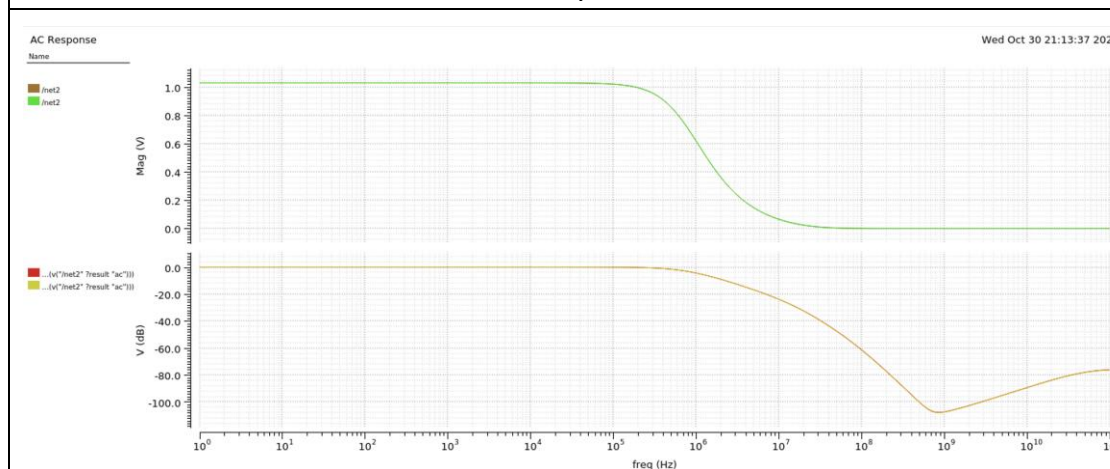
Post layout



Brown line: schematic

Green line: layout

Post layout



Brown line: schematic AC gain

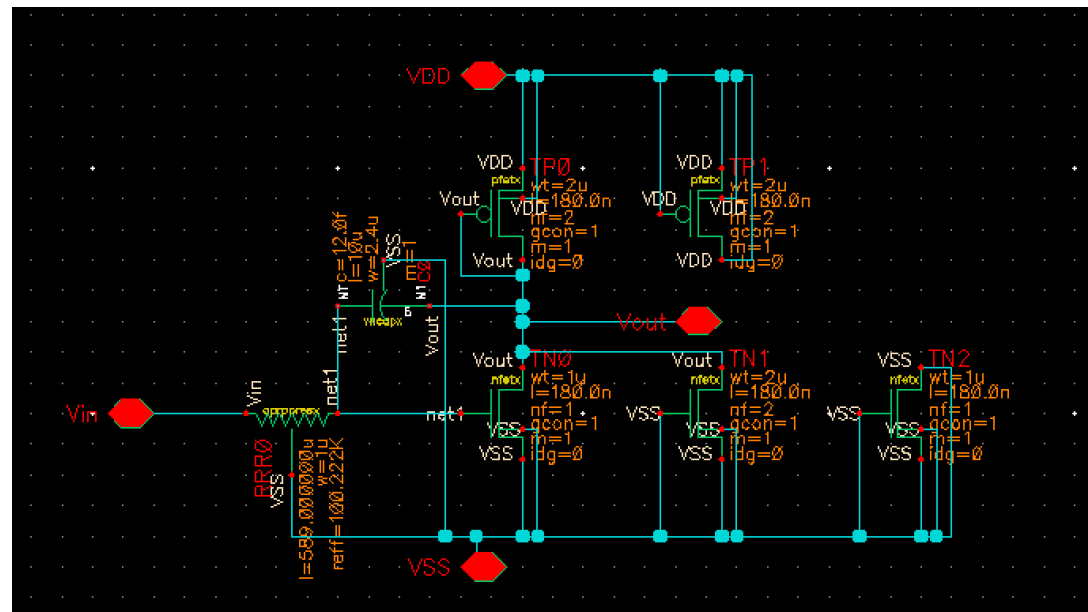
Green line: layout AC gain

Red line: schematic AC gain dB

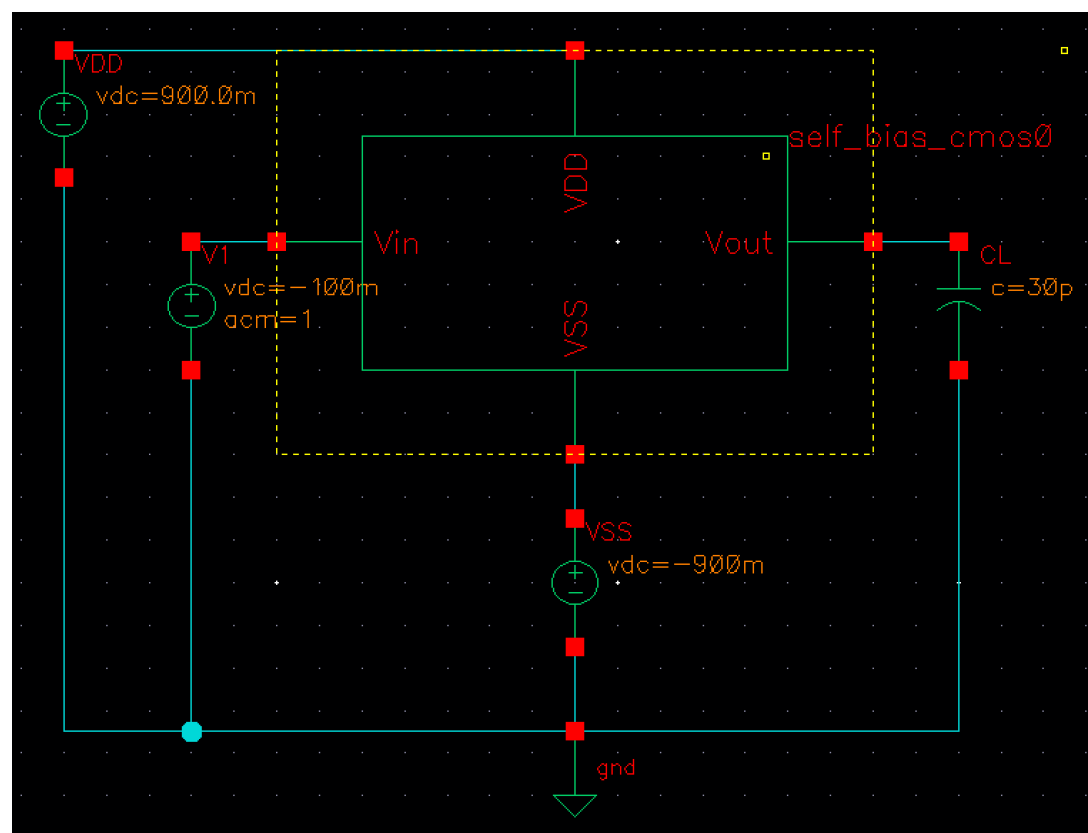
Yellow line: layout AC gain dB

d) Self-biased CMOS inverter

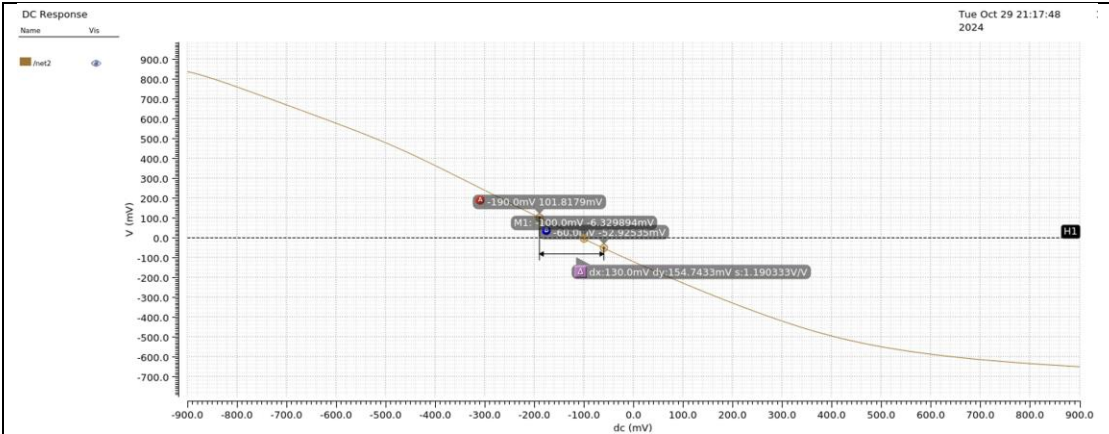
schematic



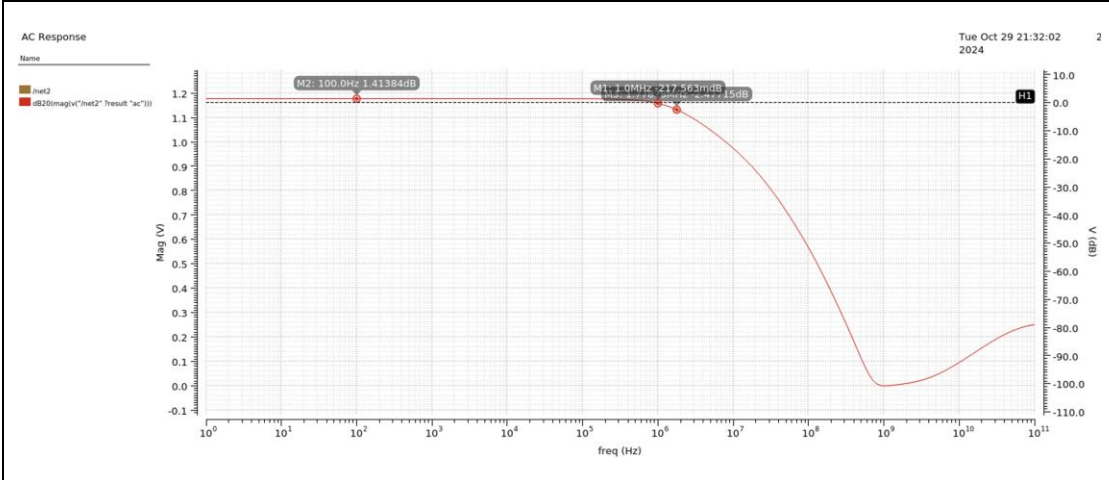
testbench



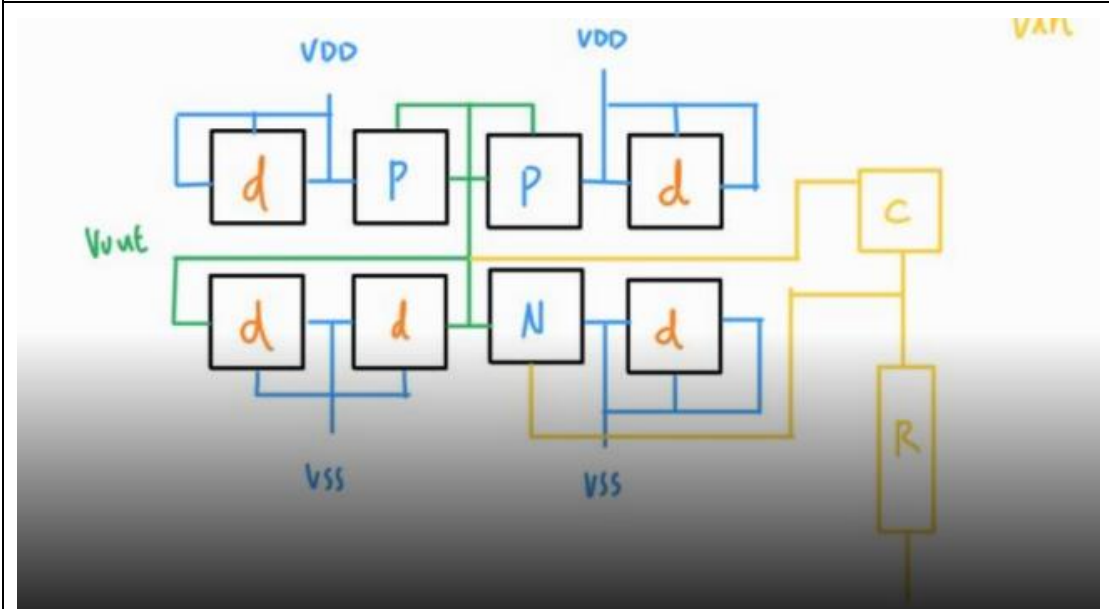
DC sweep



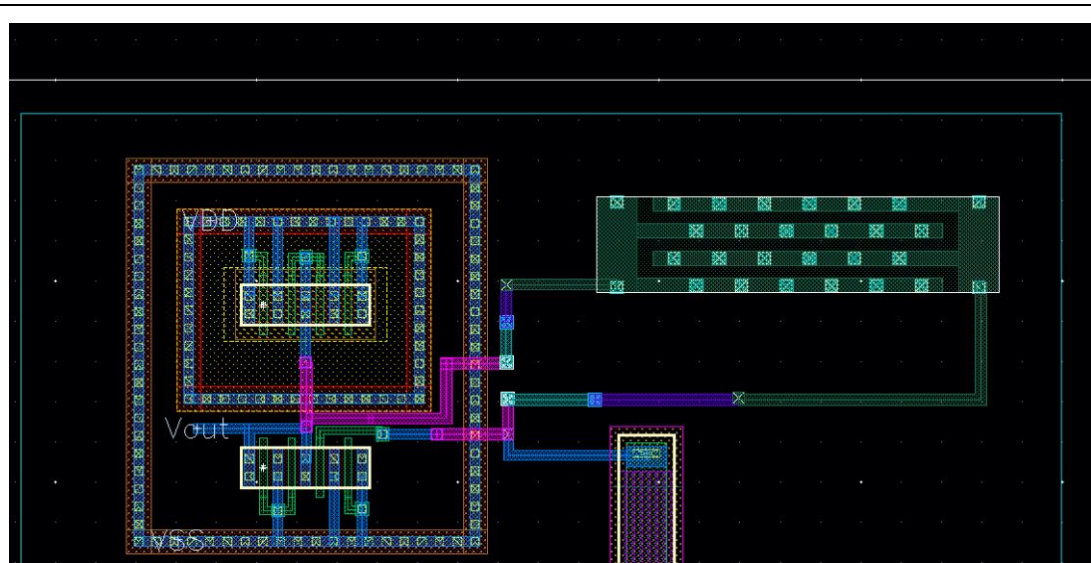
AC Freq



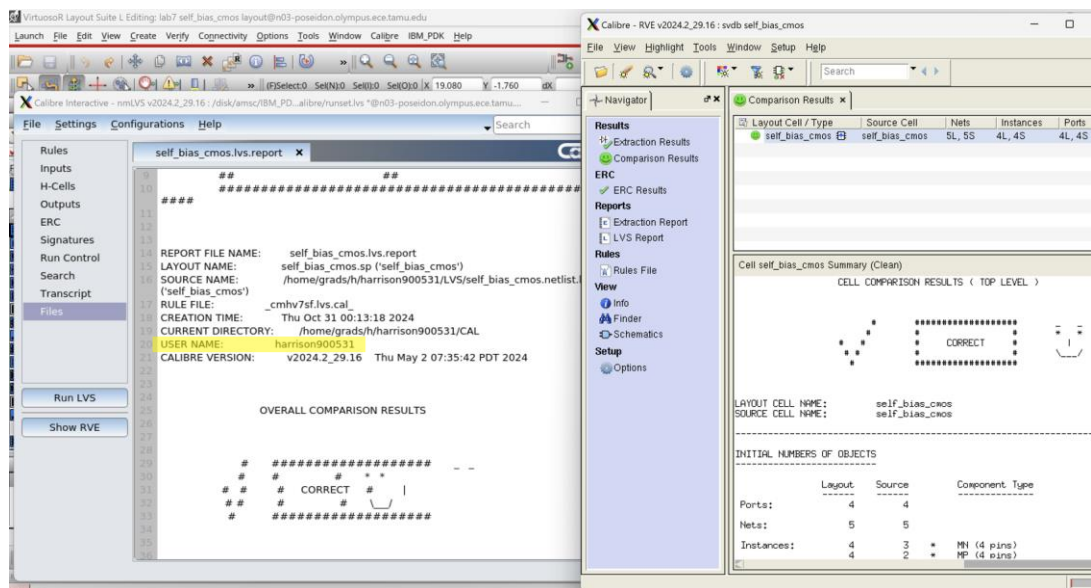
Floor Plan



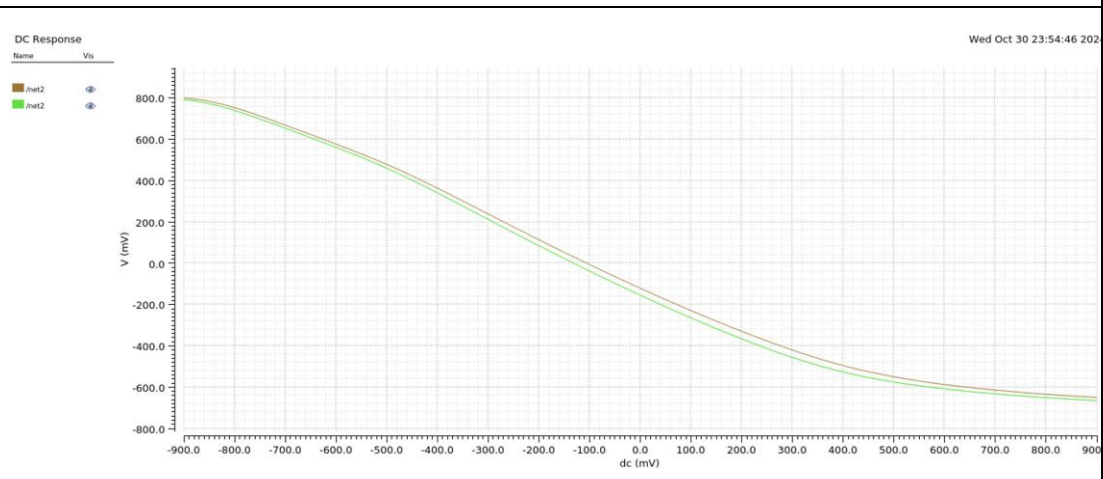
Layout



LVS



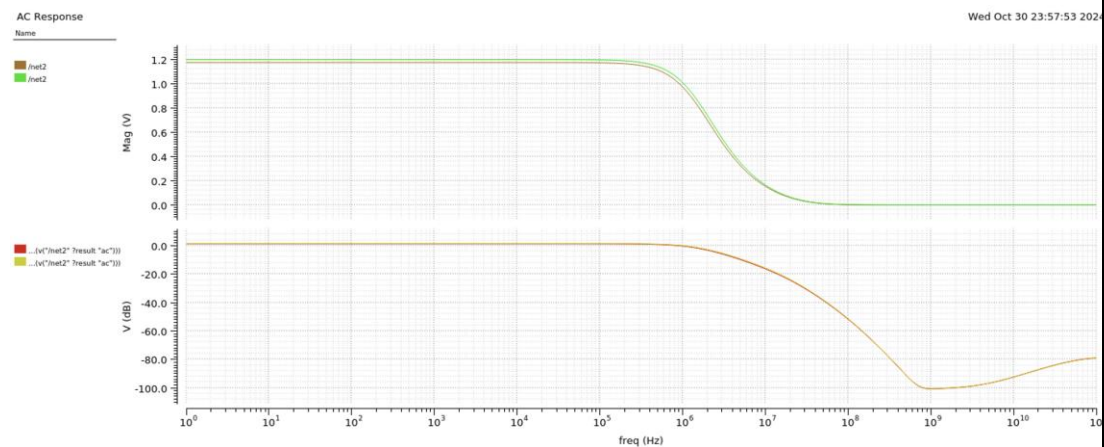
Post layout



Brown line: schematic

Green line: layout

Post layout



Brown line: schematic AC gain

Green line: layout phase AC gain

Red line: schematic AC gain dB

Yellow line: layout AC gain dB

Discussion:

When I was drawing the layout, I discovered that placing a PC layer over the RX_M1 would create a instance "PCDCAP". To resolve this issue, I attempted to change the PC layer to a different metal layer, which successfully solved the problem. Although I couldn't find information about "PCDCAP", I suspect it is related to the differences in materials between the PC layer and the metal layer.

I remember the professor discussing in class that the second pole (fp_2) will always affect the dominant pole (fp_1). If fp_2 is much greater than fp_1 ($fp_2 \gg fp_1$), then fp_1 will be approximately equal to the -3 dB point. Conversely, if fp_1 is not equal to -3 dB, the relationship changes. Plotting the first two questions is easier because we can determine fp_1 by locating the -3 dB point of the AV0 dB point. However, the last two questions are more challenging since AV0 is already approximately equal to 0 dB (the Gain-Bandwidth Product point). If we use the -3 dB point method to find fp_1 , then fp_1 multiplied by AV0 will not equal the Gain-Bandwidth Product (GBW). In this case, fp_1 will be greater than GBW, which I find peculiar.

Another consideration is that since the $wp_1 = 2\pi \cdot fp_1 = 1/AV_0 \cdot R \cdot C$, $fp_1 = 1/2\pi \cdot AV_0 \cdot R \cdot C$, and C is the only variable that affects fp_1 . However, when I use this equation to calculate the approximate value of fp_1 it significantly differs from the value I

mentioned earlier the f_{p1} = AV0 -3dB point.

Conclusion:

After completing Lab 7, we will have a solid understanding of designing inverting amplifiers, especially in high-frequency applications. This lab highlights the effects of capacitance and other factors that influence the amplifier's poles, impacting high-frequency response. By studying these elements, we can estimate high-frequency characteristics like the dominant pole, even when multiple factors interact. Through hand calculations and analysis, we gain practical insights into predicting and controlling amplifier behavior at higher frequencies, which is essential for accurate and reliable circuit design.