ECEN 474/704 Lab 5: Current Mirrors

Introduction

Current mirrors are fundamental building blocks of analog integrated circuits. Operational amplifiers, operational transconductance amplifiers and biasing networks are examples of circuits that are composed of current mirrors. Analog integrated circuit implementation techniques such as current-mode and switch-current use current mirrors as the basic circuit element. The design and layout of current mirrors is therefore an important aspect of successful analog circuit design.

In the simplest form, a current mirror is composed of only two transistors as shown in Figure 5-1. Transistor M_1 is diode connected and acts as the low-impedance input of the current mirror. The drain of M_2 is the output of the current mirror.

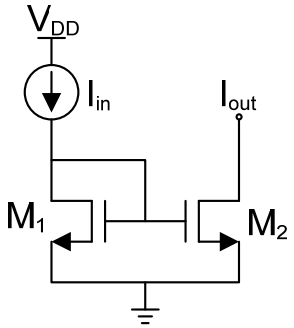

Figure 5-1: Simple Current Mirror

Since the gate-to-source voltage is the same for both transistors, according to the first-order MOSFET model, the drain currents will be equal. This assumes that the transistor sizes are equal as well as the process parameters.

A current mirror is used to mirror the input current into the output branch. A current (I_{in}) entering the diode-connected transistor establishes a gate voltage (V_{GS}), which causes I_{out} to flow through the output transistor. Notice that the input transistor will show a low small-signal resistance ($1/g_m$) and the output transistor will exhibit a high small-signal resistance (r_0).

If the ratio of the transistors is changed, then the current-mirror acts as a current amplifier. The gain of the amplifier is given by:

$$A_i = \frac{W_2/L_2}{W_1/L_1}$$

The above analysis assumes ideal operation of the current mirror, meaning that the drain currents are independent of V_{DS}. However, due to channel length modulation we know that this is not true. The following equation illustrates the dependence of drain current on V_{DS}:

$$I_D = \frac{1}{2} KP \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

The excess current due to differences in V_{DS1} and V_{DS2} will cause a difference between I_{D1} and I_{D2}. To reduce "lambda" effects, the drain-to-source voltage of the two transistors needs to be held equal.

Another non-ideality of current mirrors is the limited range of V_{DS2}. M_1 remains in saturation for all input currents due to its diode connected configuration and M_2 will enter the triode region if its drain-to-source voltage drops too low, resulting in the output current being much less than what is desired. The minimum output voltage required for the current mirror is sometimes referred to as the compliance voltage. For the simple current mirror, the compliance voltage is $V_{DS,sat2}$.

The ratio of the input to output currents is also process dependent. Because of this process dependency, good layout techniques such as interdigitized and common-centroid methods are used to layout current mirrors.

As previously mentioned, to obtain good matching between input and output currents, the drain-to-source voltages of M_1 and M_2 must be held equal. One way to achieve this is by using a cascode current mirror which is shown in Figure 5-2.

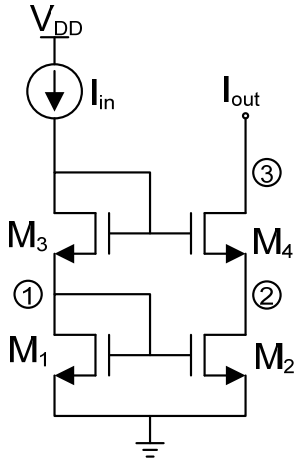

Figure 5-2: Cascode Current Mirror

Transistors M_1 and M_2 determine the ratio of the input and output currents. M_3 biases M_4 which is used to control the drain voltage of M_2. If designed correctly, V_{DS1} is approximately equal to V_{DS2}. The benefits of the cascode current mirror are better matching of output currents and larger output resistance. The disadvantage is that a larger compliance voltage is needed to keep both M_2 and M_4 in saturation. To find the compliance voltage, loop and node analysis will be used as follows:

- **Node 1:** The voltage here is $V_{GS1} = V_T + V_{DS,sat1}$.
- **Node 2:** For good matching between input and output currents, we want V_{DS1} and V_{DS2} to be equal. Thus, the voltage at Node 2 is also $V_T + V_{DS,sat1}$.
- **Node 3:** The minimum compliance voltage will be the minimum voltage to keep M_4 in saturation. This will be $V_T + V_{DS,sat1} + V_{DS,sat2}$.

Adding the cascode transistor does not just increase the required compliance voltage by one $V_{DS,sat}$, it also increases the threshold voltage. If the overdrive voltage is 200 mV for all transistors with threshold voltages of 700 mV, the output voltage will have to be greater than 1.1 V. This makes cascode current mirrors not desirable for modern processes, since the required supply voltage is already small.

In order to have the good current matching capabilities of the cascode current mirror, while not having such a large compliance voltage, we can use the low-voltage cascode current mirror as shown in Figure 5-3. If designed correctly, M_1 and M_2 will be biased such that they are at the edge of saturation with $V_{DS} \approx V_{DS,sat}$, therefore the compliance voltage drops to $V_{DS,sat2} + V_{DS,sat4}$. This is one whole threshold voltage less than

the regular cascode current mirror of Figure 5-2. M_B will usually have a small W/L ratio, and should have a $V_{DS,sat} = V_{DS,sat1} + V_{DS,sat3}$.

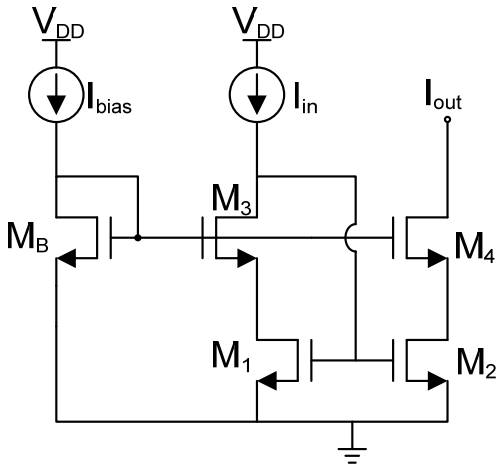

Figure 5-3: Low-Voltage Cascode Current Mirror

Simulating Current Mirrors

Once a current mirror has been designed using hand calculations, use the test configuration in Figure 5-4, where I_{in} is the reference DC current and V_{out} is a DC voltage source that will be varied in a DC sweep simulation. After running the simulation, plot I_{D2} (if necessary, refer back to Lab 1 for more information regarding the plotting of signals). The resulting I_{D2} versus V_{out} plot should resemble Figure 5-5. The compliance voltage will be the point on the plots where the slope of I_{out} begins to change rapidly, indicating that the output transistor is entering the active region of operation (see the "Operating Region of Transistors in Cadence" section for a method of quantifying this boundary). On the plot, mark the compliance voltage and the voltage at which I_{D2} is equal to the desired output current level. **Note that you will likely want to utilize a smaller step size in the DC sweep to get greater resolution of the compliance voltage. Change the "sweep type" setting in the DC sweep setup to "Linear" rather than "Automatic" and set the step size or number of steps to a suitable value for more clearly determining whether your current mirror satisfies the specifications.** The choice of variable step size can be thought of as a sampling problem: consider the approximate width (in terms of the sweep variable or x-axis variable) of the feature you are trying to identify, then select a step size which is *less than* half of that feature width to gain enough resolution in the sweep for accurately viewing the desired features of the plot.

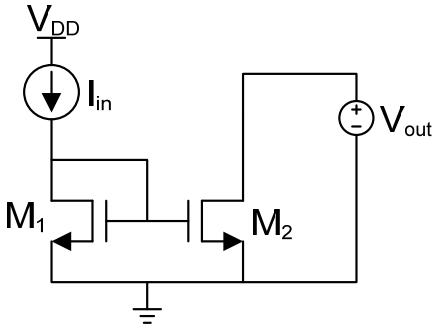

Figure 5-4: Current Mirror Test Configuration

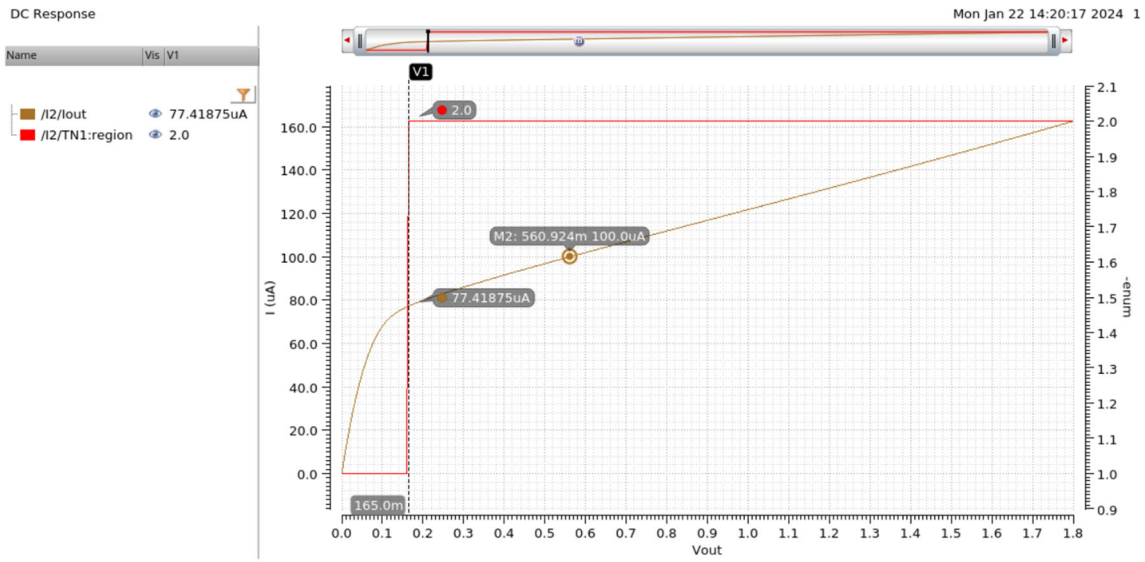

Figure 5-5: Current Mirror Simulation Results for Compliance Voltage

In order to find the output impedance, an AC simulation needs to be run. First, in the ADE L state, save the output voltage of the current mirror and the current at the (-) terminal of the V_{out} voltage source on the schematic (refer to Lab 1 if needed). Then, assign the V_{out} source a DC voltage greater than $V_{DS,sat}$ (say 1 V) with an AC magnitude of 1 V. Then, go to *Launch* → *ADE L* and click on the *"AC, DC, Trans"* button (or *Analyses* → *Choose*). Click on *"ac"*, set *Start* to *1* and *Stop* to *100G* for the *Sweep Range.* Change *Sweep Type* to *Logarithmic* and set *Points Per Decade* to *20,* then click *OK* and run the simulation.

To plot the output impedance, go to *Tools* → *Calculator.* First, click on *"vf"* on the Calculator and then the output node (wire) on the schematic. Second, click on *"if"* on the Calculator and then the (-) terminal of the voltage source V_{out} on the schematic. Finally, click on *"/"* on the calculator, and then *Tools* → *Plot.* Refer to the Appendix in the Lab 1 manual for more information regarding the saving and construction of output expressions. The output impedance plot should resemble Figure 5-6. In this example the output impedance is about 20 kΩ at low frequencies with a pole in the response located slightly below 600 MHz.

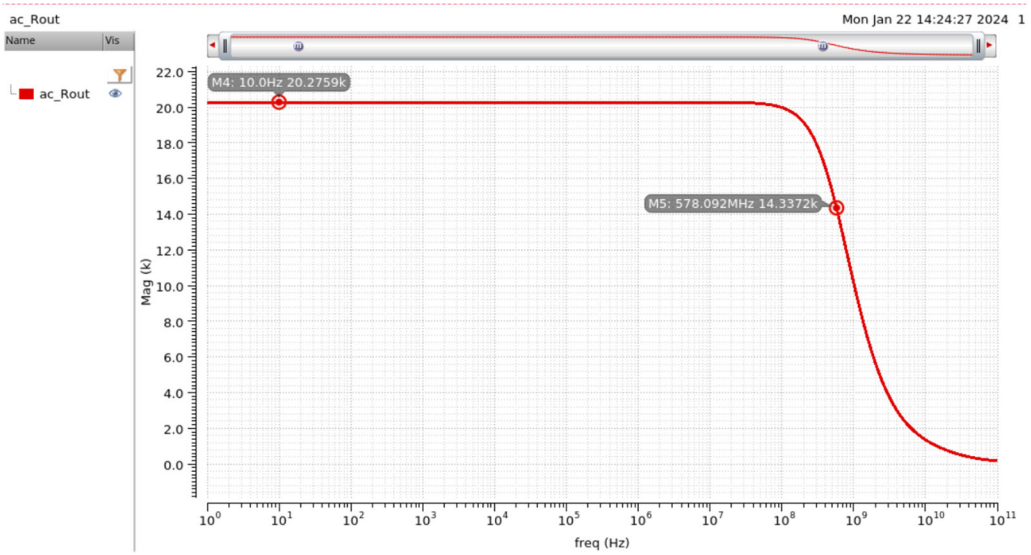

Figure 5-6: Plot of Simple Current Mirror Output Impedance

Operating Region of Transistors in Cadence

Cadence has a function that can test a transistor's region of operation. Testing transistors' regions of operation versus a DC sweep of one parameter can be very useful, as will be shown in this lab and future labs focused on the design of amplifier circuits.

The first step in plotting the region of operation is to choose a circuit parameter (the input voltage source in this case) and run a DC sweep of that parameter. Make sure the "Save DC Operating Point" option is enabled in the DC simulation setup before running the simulation. Now we're ready to plot the region of operation. Go to *Tools* → *Calculator* → *<select "OS">* → *<select the transistor to test>* → *<select "Region" from the drop down menu>* → *plot.* Note that when you select the transistor, the selection window may disappear. It only goes down to the task bar; just click it to pull it up again and then select "Region" as previously instructed. Save this expression to the list of outputs in your ADE L state.

If difficulties are encountered attempting to save the operating point data using the above method with the OS function, retry the process using the OP function. If the desired OP function is displayed in the calculator buffer, replace the "P" with "S" to convert it to the OS function (the OP and OS functions have the same syntax; see the Appendix in the Lab 1 manual for more information about the differences between the OP and OS functions). Alternatively, the region parameter data (and other DC operating point data) can be saved directly in ADE L. Go to *Outputs* → *To Be Saved…* → *Select OP Parameters* in the ADE L window. Then, go to the schematic window and click on the transistor instances for which you want to save the operating point information. **Note: when selecting transistors from a test bench schematic, use the "X" or "Shift-X" hotkeys to descend into a sub-circuit schematic instance. A window appears to determine how the lower-level sub-circuit will be viewed. To ascend back to a higher level of the schematic hierarchy (e.g. back to the test bench level), use the "B" hotkey.** Tap the Esc key when finished selecting instances to end the selection process. A new tab will appear at the bottom of the "Outputs" portion of the ADE L window. Selecting this tab will show the devices for which the operating point data is saved. In the field to the right of the instance name, type "region" and then tap the enter key. Alternatively, click the "…" button, populate the window that appears by clicking the "Get from Simulation" button, and then select the desired operating point parameters from the list (hold the Ctrl key while selecting to save multiple operating point parameters).

You may need to rerun the DC simulation after creating the output expression in order to get the region parameter data. Once your plot has been generated, it should resemble Figure 5-7 which was generated for a cascode current mirror. The plot shows a waveform that holds a constant number within different ranges. The values and the corresponding regions of operation are described in Table 5-1.

Table 5-1: Values for Regions of Operation

0	Cutoff
1	Triode
2	Saturation
3	Sub-Threshold
4	Breakdown

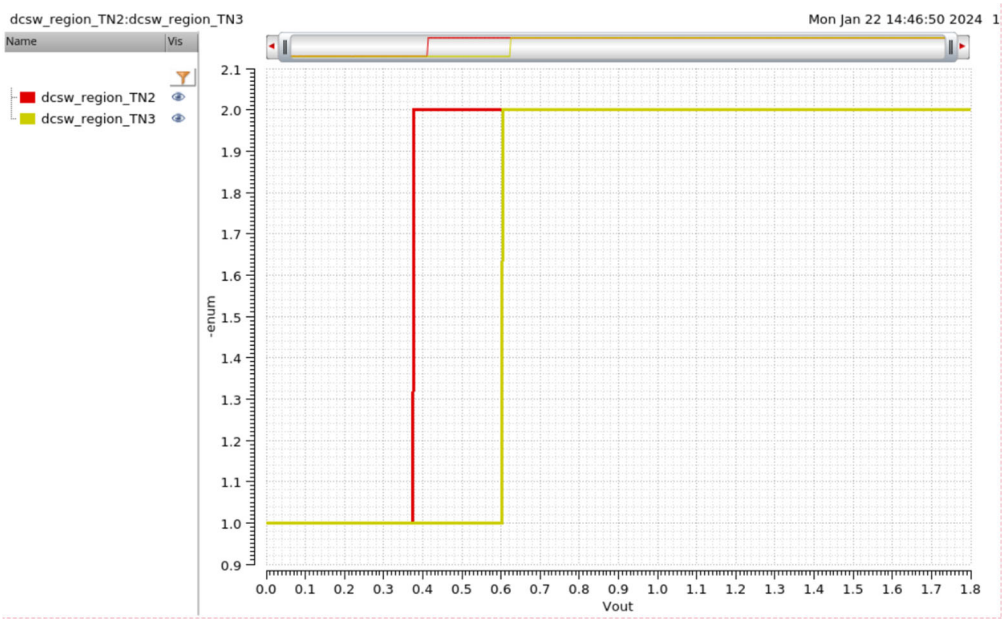

Figure 5-7: Region of Operation Plot for the output transistors of a Cascode Current Mirror

Note that the region parameter is created from a series of logical/binary operations in the transistor model. The decisions made in evaluating the region of operation are a component of the transistor model and cannot be changed. However, as a designer, you should not rely too heavily on the region parameter as the defining factor of whether your transistors are in the correct region of operation, particularly when you expect a device to operate near the edge between two regions (for example, between triode and saturation, or between sub-threshold and saturation). As a circuit designer, you should consider whether the other voltages and currents in the circuit, along with the circuit's behavior, confirm or contradict the information provided by the models. **You should not sacrifice your intuition for the sake of the simulator's results. But if there is a difference between the simulator output and your intuition, you should deeply investigate what causes the difference and whether your intuitions need to be refined or if you have encountered an area in which the models are lacking.**

Plotting the Region Parameter for Post-layout Simulations

The region parameter can still be viewed in post-layout simulation results, but some changes need to be made during parasitic extraction (PEX) to simplify the process.

When the layout is completed and passes LVS, begin the normal PEX process. Near the end of the PEX process, the "Calibre View Setup" window should appear, like what is shown in Figure 5-8. Change the "Calibre View Type" option to "schematic" and then click OK. Changing this option to "schematic" will cause the calibre view to be displayed with a schematic-like window when it is opened (whereas the default option opens in a layout-like window).

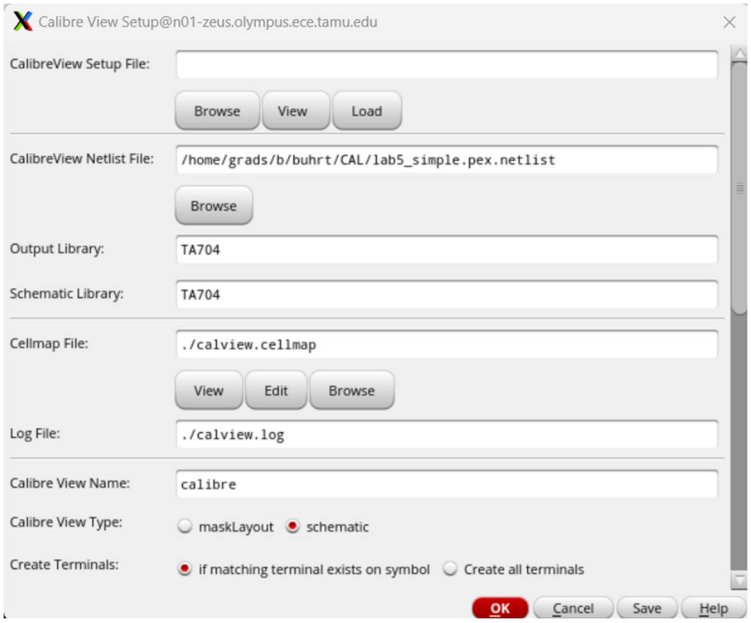

Figure 5-8: Calibre View Setup window

With this option selected, the calibre view can be more easily viewed when descended into from a test bench schematic. After configuring the post-layout simulations, the same procedures mentioned above can be used for saving the region operating point parameter. However, when descending into the current mirror instance with the "X" or "Shift-X" hotkeys, the window that appears should instead display "calibre" as the view type rather than "schematic," as in Figure 5-9.

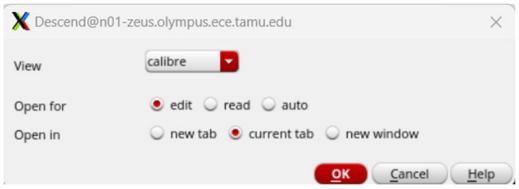

Figure 5-9: Descend into calibre view of instance

While looking at the calibre view, each finger of a transistor is treated as a separate instance, but the name of the parent instance is preserved. In other words, if a transistor instance was named "TN0" in the original schematic, the corresponding transistors in the calibre view will also contain "TN0" in the instance name. Note, however, additional information is appended to the end of the instance name to distinguish each finger of the larger transistor. Additionally, PEX prepends an additional letter to the beginning of an instance name for the devices in the calibre view (e.g. MOSFET instances are typically prepended with "M" in the instance name before repeating the instance name as it originally appeared in the schematic). These prepended and appended portions of the instance name are controlled by PEX, and you should not attempt to modify them.

Once you have descended into the calibre view of the current mirror, you can select a single finger of the output device(s) to save the region parameter using one of the procedures mentioned previously. Use the "Navigator" sub-window on the left side of the calibre view window to help you find the needed devices. Only one finger of each device needs to be selected. Due to the relative simplicity of the circuits, it can be assumed that the other fingers of the corresponding device are acting identically and would therefore display the same values of the region parameter or of other DC operating point parameters.

Prelab

1. Make a table which lists the three current mirror topologies described in this lab. Rate each topology using good, medium and bad for the following design considerations: R_{out}, accuracy, complexity, and compliance voltage.

2. Design a simple 1:1 current mirror that has a compliance voltage of 100 mV to 150 mV. The output current should be 100 μA. Determine W/L for each transistor and what the expected output impedance should be.

3. Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 1 MΩ. Assume a 50 μA input current.

Lab Report

1. Simple current mirror
   a) Design in Cadence the simple current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   b) Generate the plots of Figure 5-5 and Figure 5-6 for this design. Determine the compliance voltage, low frequency output impedance, and comment on accuracy.
   c) Layout the current mirror. Remember to use good layout techniques. Run post layout simulations. Include plots of both layout and schematic simulation in your lab report.
2. Low-voltage current mirror
   a) Design in Cadence the low-voltage cascode current mirror from the prelab. If needed, modify the design so that it meets the given specifications.
   b) Generate the plots of Figure 5-5 and Figure 5-6 for this design. Determine the compliance voltage, low frequency output impedance and comment on the accuracy.
   c) Layout the current mirror. Remember to use good layout techniques. Run post layout simulations. Include plots of both layout and schematic simulations in your lab report.
3. Be sure to include in your report the LVS results showing that the layout matches the schematic (again NetID and time stamp required for credit).