24 Fall ECEN 704: VLSI Circuit Design

Design Pre-lab Report

Lab5: Current Mirrors

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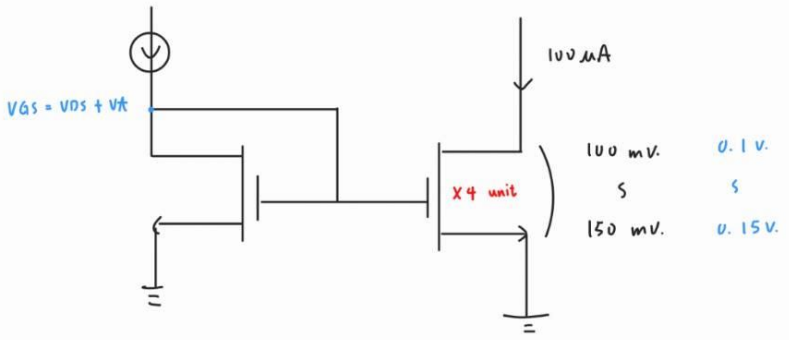
1. Make a table which lists the three current mirror topologies described in this lab. Rate each topology using good, medium and bad for the following design considerations: Rout, accuracy, complexity, and compliance voltage.
2. Design a simple 1:1 current mirror that has a compliance voltage of 100 mV to 150 mV. The output current should be 100 µA. Determine W/L for each transistor and what the expected output impedance should be.
3. Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 1 MΩ. Assume a 50 µA input current.

1.

	Rout	Accuracy	Complexity	Compliance Voltage
simple	bad	bad	good	good
casecode	good	medium	medium	bad
low -voltage	medium	good	bad	medium

2.



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS})$$

$$100\mu A = \frac{1}{2}\times 189.99\,\mu\times\frac{5\,\mu}{0.27\,\mu}\times 4\,(V_{DS})^2\times(1+0.196\times V_{DS})$$

$$100 = 1754.53\times 4\,X^2\cdot(1+0.196\,X)$$

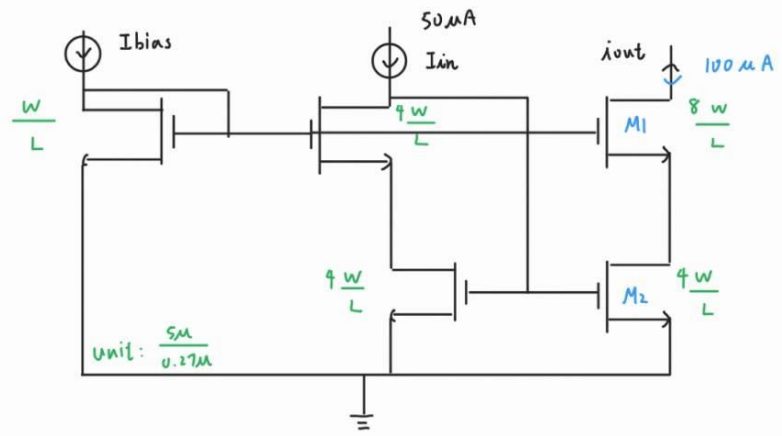
$$100 = 256.16\times 4\,X^3+1754.53\times 4\,X^2$$

$$X = -6.84\ /\ 0.118\ /\ -0.12$$

$$\frac{W}{L} = \frac{4\times 5\,\mu}{0.27\,\mu}$$

output impendence : $r_{ds} = \frac{1}{\lambda I_D} = 68.493\,k\Omega$

3.



output impedenie ≥ 1 MΩ

Rout : $g_{m1}' r_{ds1} r_{ds2} + r_{ds1} + r_{ds2}$ $\quad r_{ds} = \frac{1}{\lambda I_D}$

$g_{m1}' = g_{m1} + g_s = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} + \chi g_m$

$r_{ds1} = 68.493k \quad r_{ds2} = 68.493k$

$g_{m1} = \sqrt{2 \times 189.49 \times \frac{8 \times 5\mu}{0.27\mu} \times 100\mu} = 2.369\,m$

$g_{m1}' = 2.369m + 0.71\,m = 3.079$

$|R_{out} = 14.581\,M\Omega$