25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

Lab1: Transmission Lines

Name: Yu-Hao Chen

UIN:435009528

Section:700

Professor: Sam Palermo

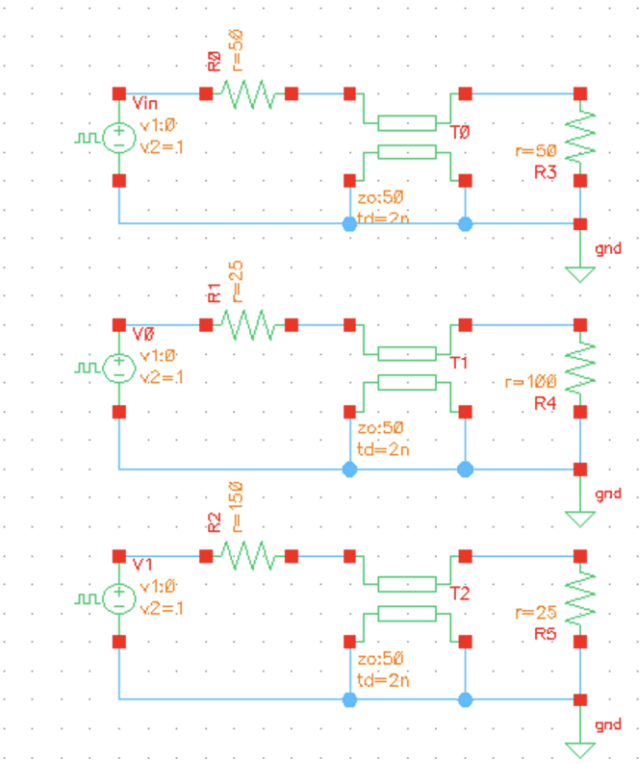
TA: Srujan Kumar Kaile

Description:

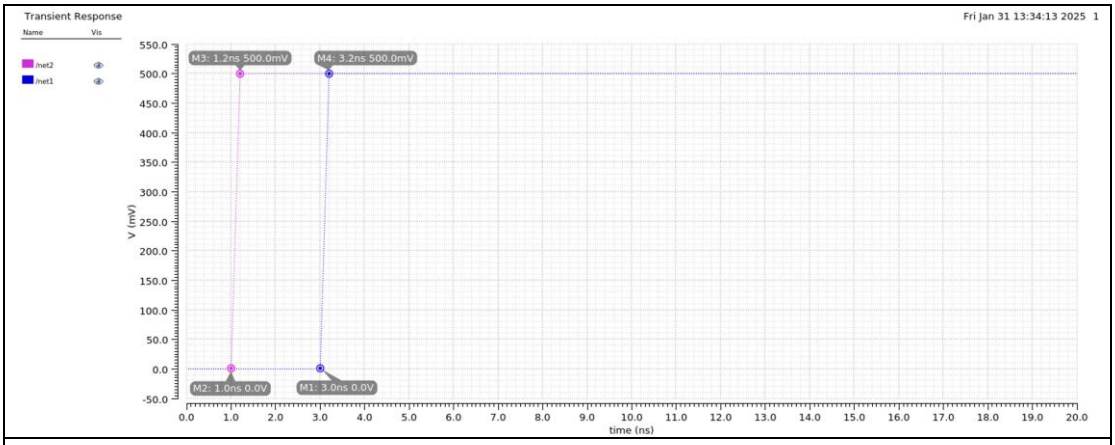
Wires transmit clocks and data signals. In baseband chip design, they are treated as lumped parasitic loads, while in high-speed data communication, they act as transmission lines requiring proper termination to prevent reflections. This lab explores transmission line characteristics, termination techniques, and the use of a time-domain reflectometer (TDR) to analyze step response.

Design & results

1. LC Transmission Line Termination Repeat the pre-lab question. Please work out the waveforms for the terminated transmission line circuit as shown in Figure 8. Please compare these three cases in terms of signal integrity. What is the final value in each case?
   - Case 1: RS=50Ω RT=50Ω Z0=50Ω
   - Case 2: RS=25Ω RT=100Ω Z0=50Ω
   - Case 3: RS=150Ω RT=25Ω Z0=50Ω



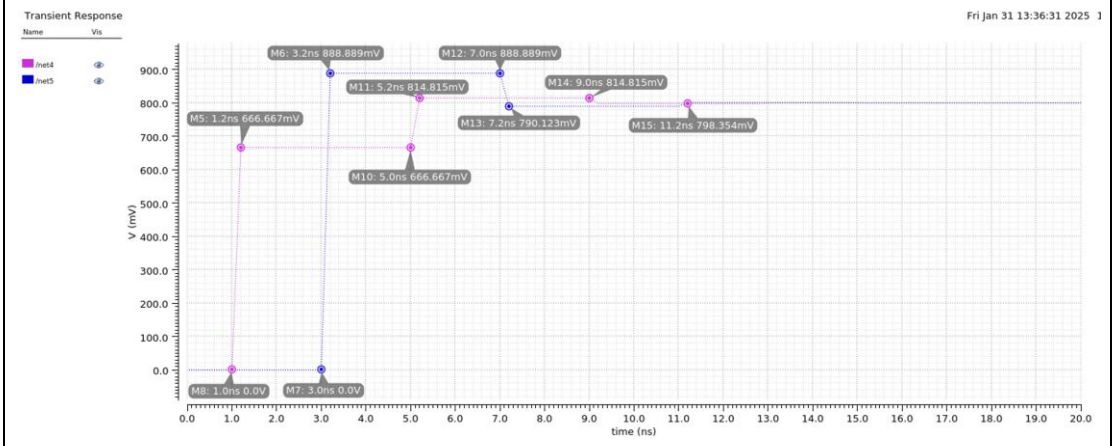
Top: case1 Mid :case2 Bottom :case3



Result for case1 (Reflection Coefficient KrS & KrT =0)

Pink line for Vsource and Blue line for Vterminal.

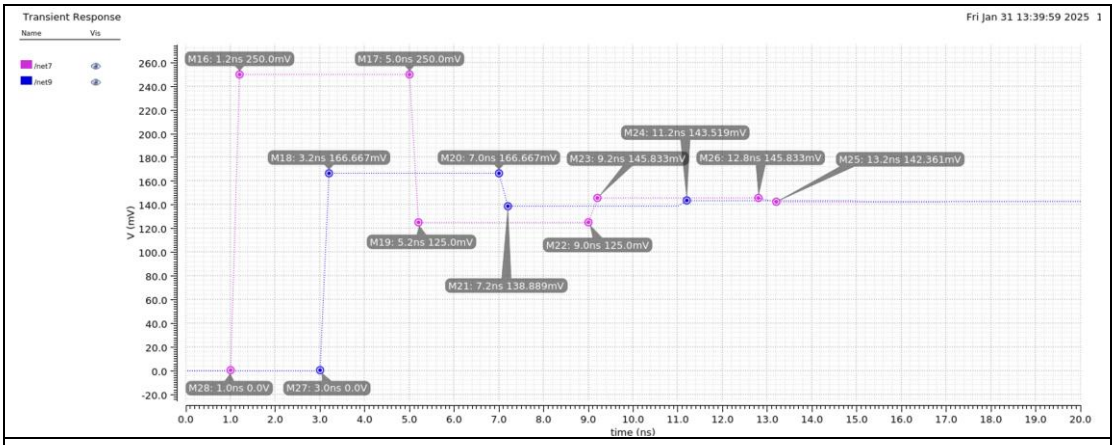
1V input signal pulse, after 1ns delay get partial by Rs =50 Ω & Z0 =50 Ω, after 2ns transmission delay get to Terminal and didn't reflect back to transmission line.



Result for case2 (Reflection Coefficient KrS =-0.33 & KrT =0.33)

Pink line for Vsource and Blue line for Vterminal.

1V signal pulse, after 1ns delay get partial by Rs =25 Ω & Z0 =50 Ω, after 2ns transmission delay get to Terminal (the value at t=3ns= partial signal 0.66+ reflection signal (0.66*KrT)=0.88) and total signal reflect back to transmission line to source. After 2ns Vsource=t=3ns total signal 0.88+ reflection signal (Krs*(0.66*KrT))=0.814 and reflect back to terminal and so on.

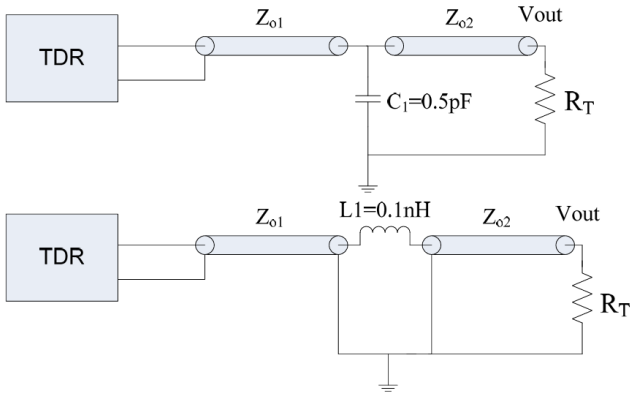


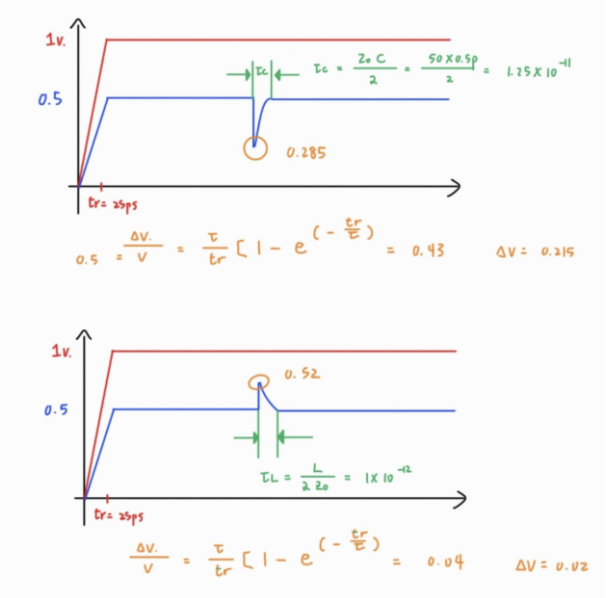
Result for case3 (Reflection Coefficient KrS =0.5 & KrT =-0.33)

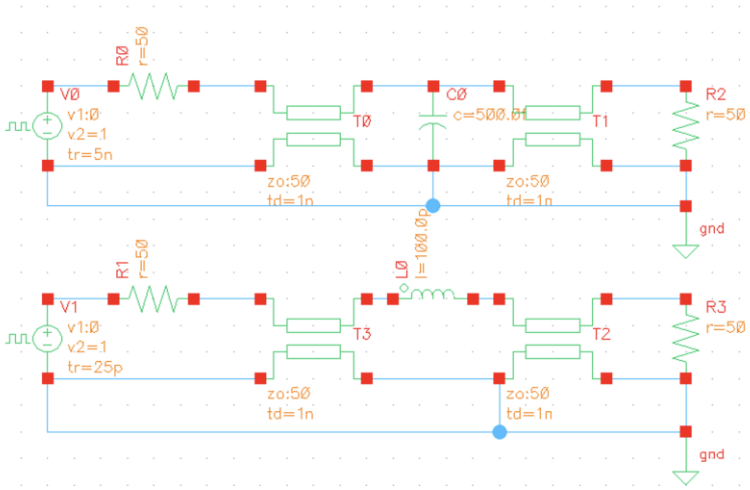
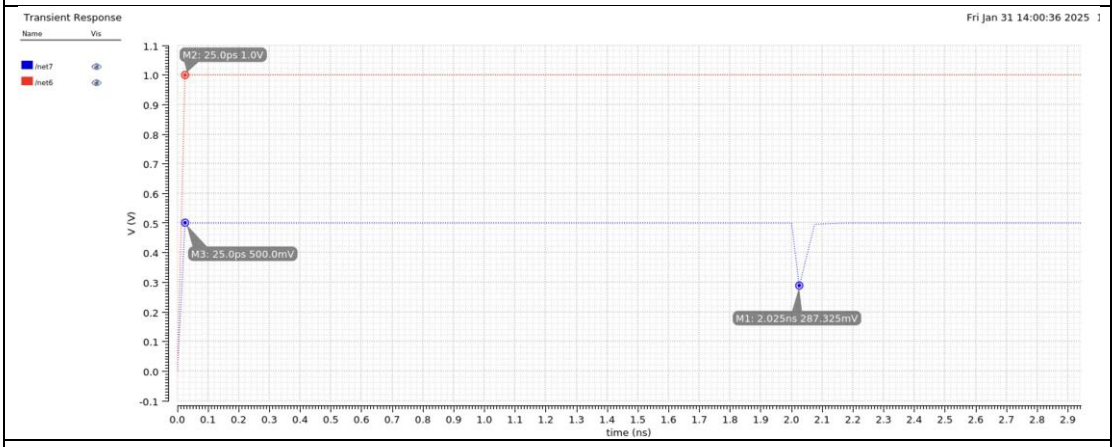
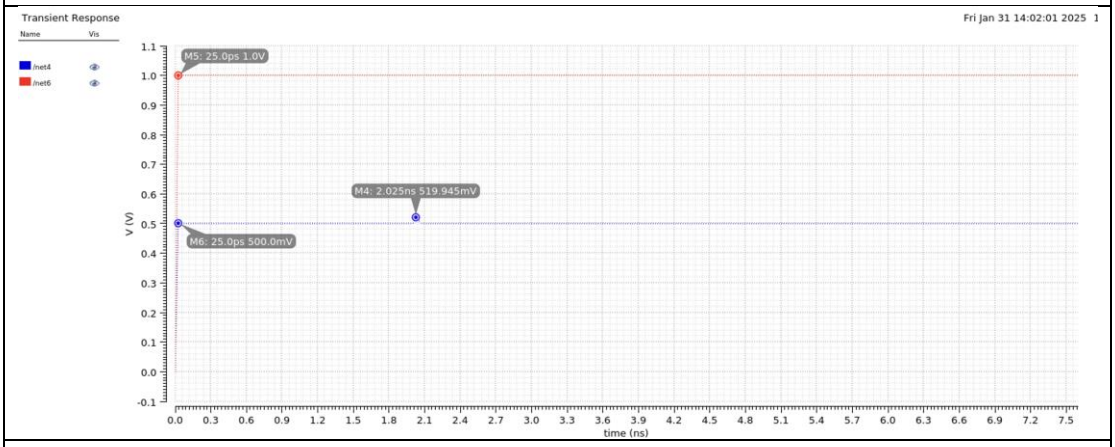
Pink line for Vsource and Blue line for Vterminal.

Same operational way with case2 but with different KrS and KrT.

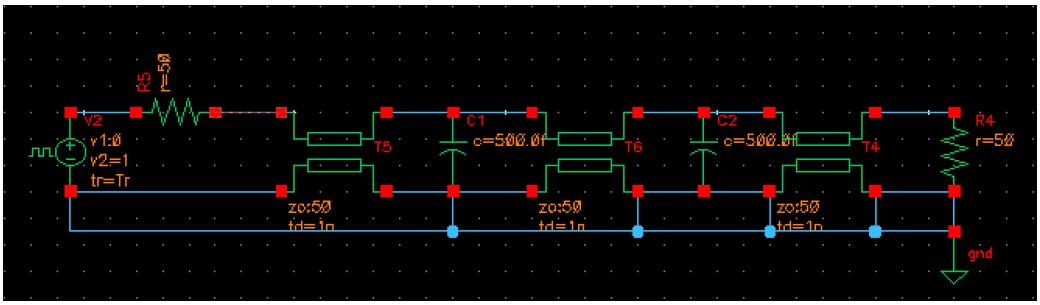
2. TDR is used to characterize interconnect for any impedance discontinuities.
   a. Please hand draw the TDR responses for the circuits shown in Figure 10 with an input step of 25ps rise time. Verify your results using Cadence. Z01=Z02=RT=50Ω. Tdelay=1ns.





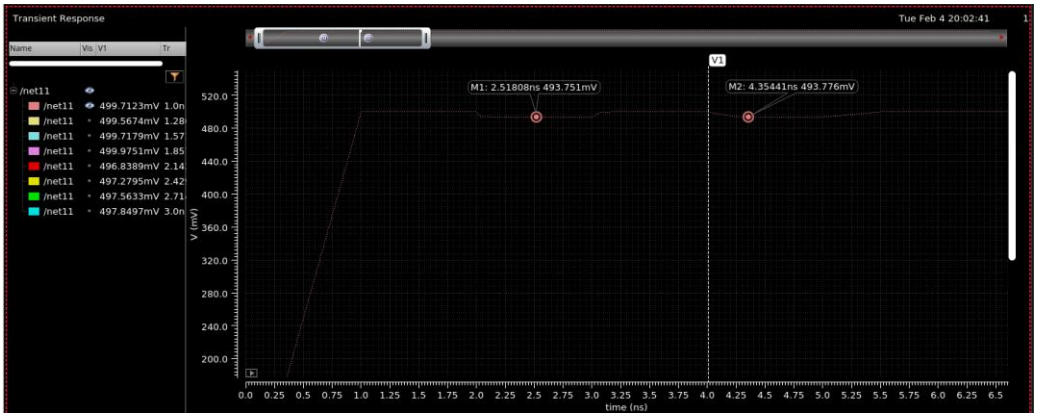
Hand calculation

Top: shunt C discontinuity Bottom: series L discontinuity

shunt C discontinuity

series L discontinuity

b. TDR spatial resolution is set by the rise time of the step signal. Assuming a TDR generates a 1V step signal and measures its response using a 10-bit ADC. Please derive the minimum required step rising time versus TDR minimum lumped capacitance resolution curve.

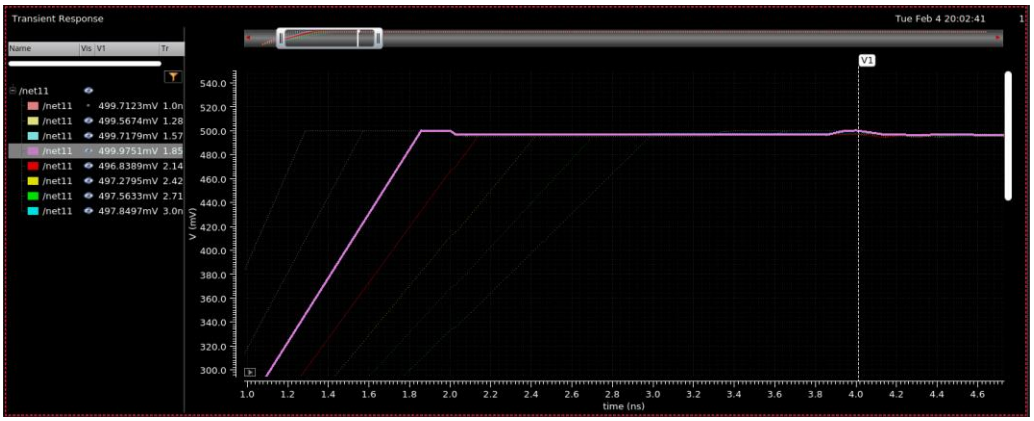


Assuming the two C are the first and second C for 10bits ADC (10 C), if the tr is enough for the first two bit to determine, which need the fastest response time, than others (3rd bits…) will be fast enough to quantify.

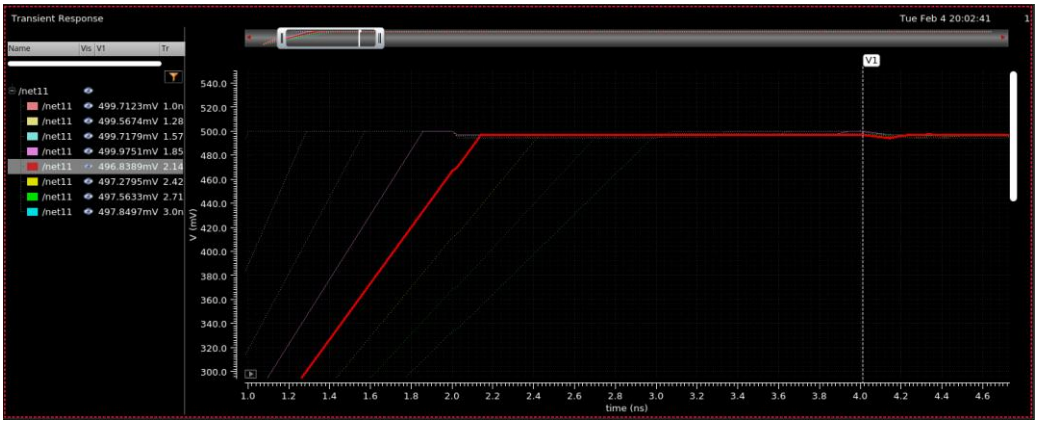
When Tr> Tround-trip (Tdelay*2)= 2ns



The first 2 bits of ADC response



Near the limitation (tr= 2ns)



Over the 2ns, overlapping

3. In a digital circuit, an open drain PMOS transistor functions as a buffer to drive a 50Ω testing probe as shown in Figure 11. The testing probe provides a 50 Ω termination with respect to ground. The output pad and pin parasitic capacitance can be estimated to be 0.5pF each. Assuming 3mm bond wire, the bond wire parasitic resistance and inductance are 1Ω/mm and 1nH/mm. For 90nm technology, please use nominal 1.1V supply.

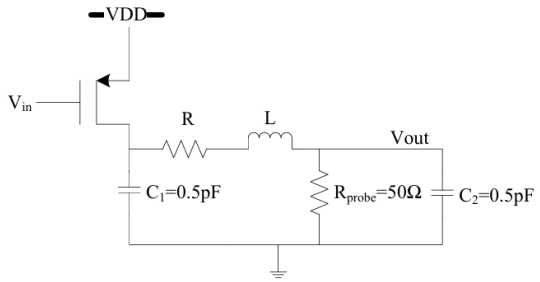
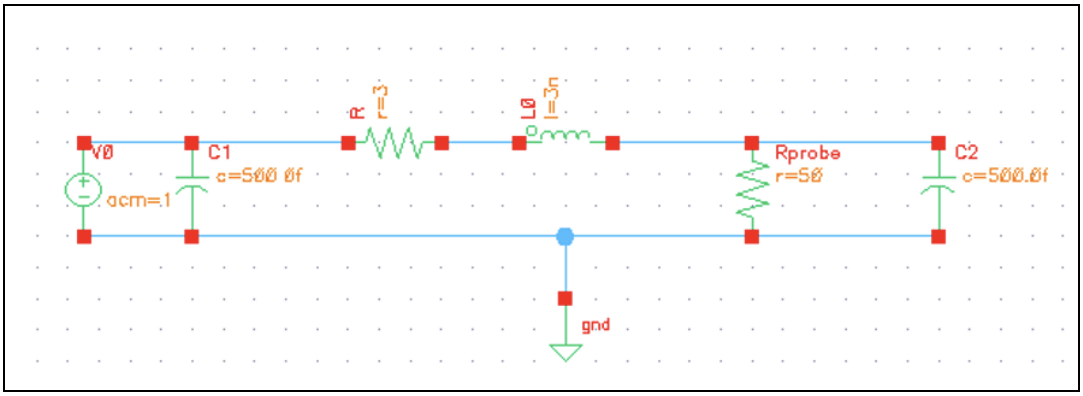
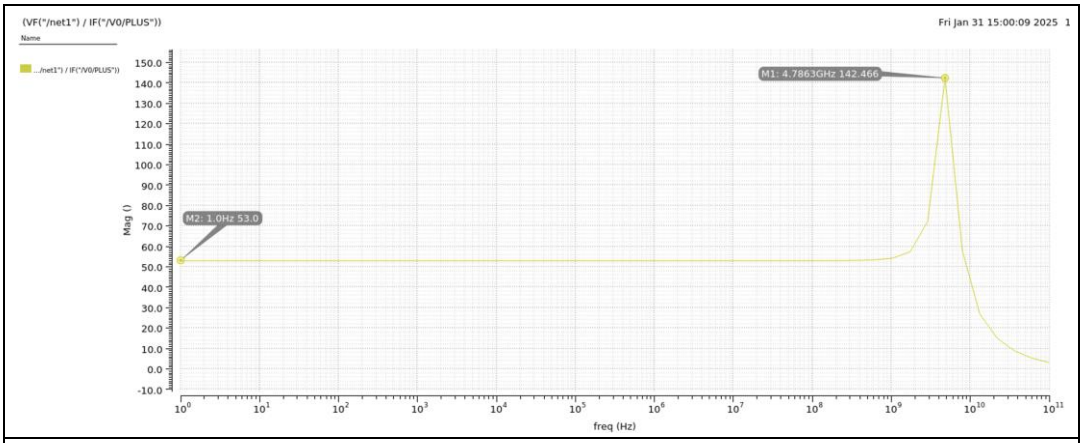


Figure 11 PMOS Open Drain Driver

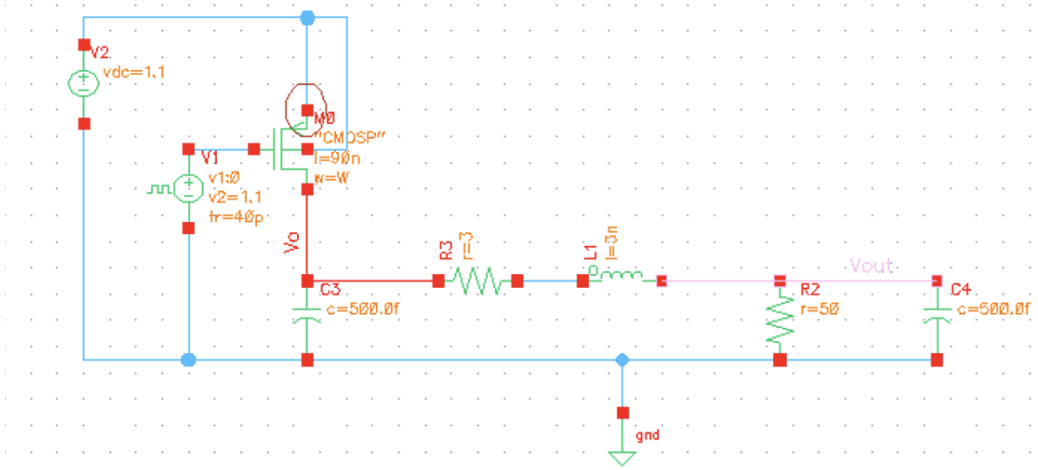
a. Please measure the frequency response (impedance) of the PMOS transistor load and show and explain briefly the results.





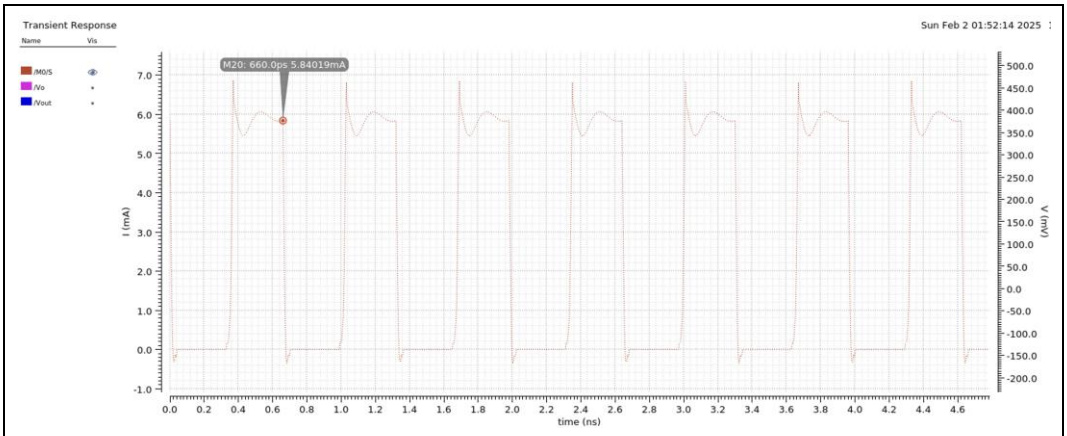
For low frequence L=0 C=infinite Z=R probe 50 Ω in series with R =1 Ω *3 (Assuming 3mm bond wire, the bond wire parasitic resistance and inductance are 1Ω/mm and 1nH/mm)

b. Design the open drain driver to output 300mVpp using 1.5GHz full swing square wave input signal (40ps rise time). Compare the output signal with the ideal case (no parasitic). Explain the effect of parasitic resistance, capacitance and inductance. What happens if 200MHz input signal is used? Does rising and falling times affect the output signal? Change the input to a 7-bit 2.5Gb/s PRBS (pseudo random bits) input data, comment on the output signal and its ripple.

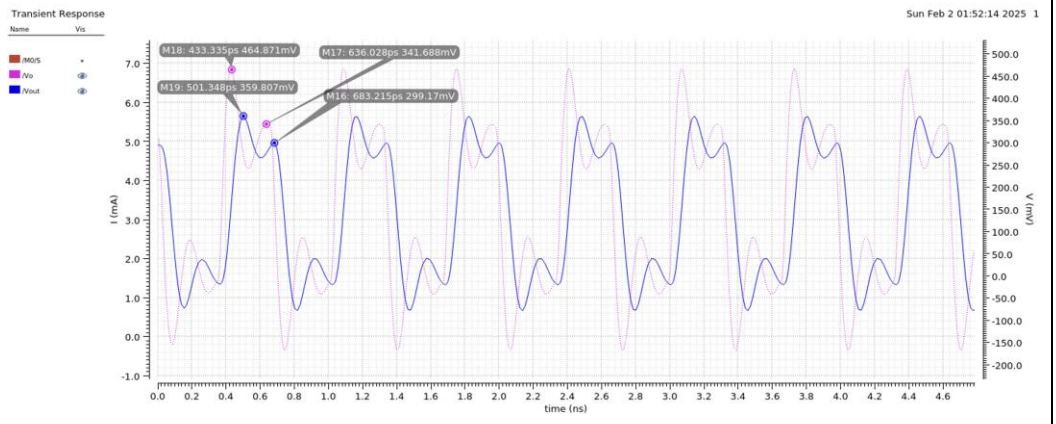


Z load (1.5G) =56 Ω, Z load (200M) =53 Ω

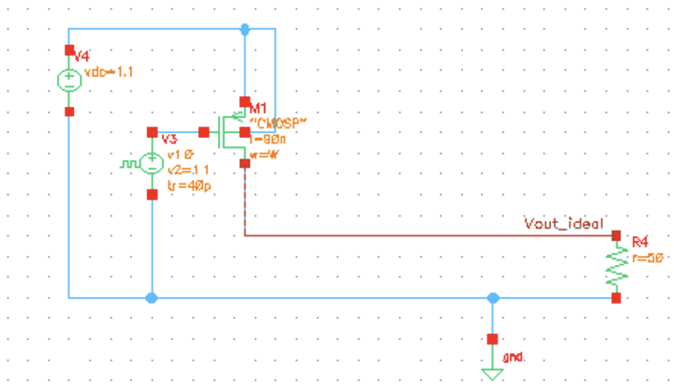
For Vo =300mV we can get the equation 300mV =Id*(rds//Z load), which Id=0.5*uncox*W/L/(Vgs-Vt) ^{2}(Id =5.89m under rds//Z load =56 Ω), take the average of uncox =100u/V, Vt=0.5v, we can get the W/L (using the minimum for L = 0.9n, W=40u).



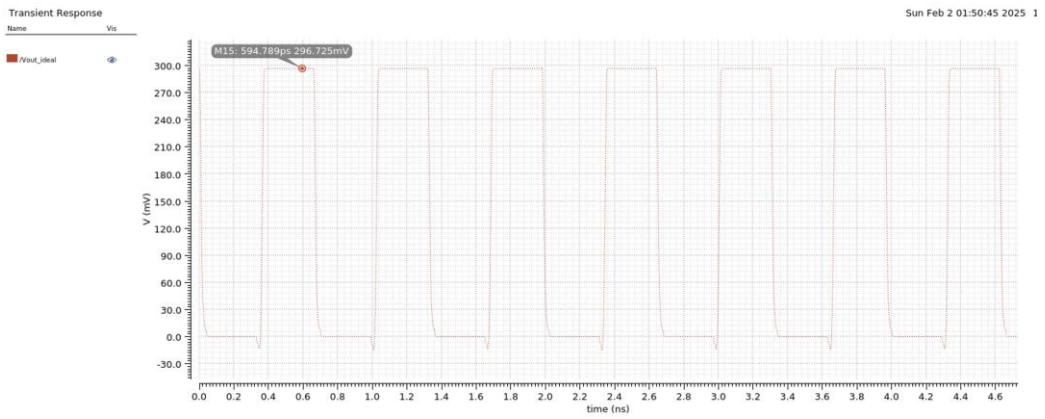
Current Id



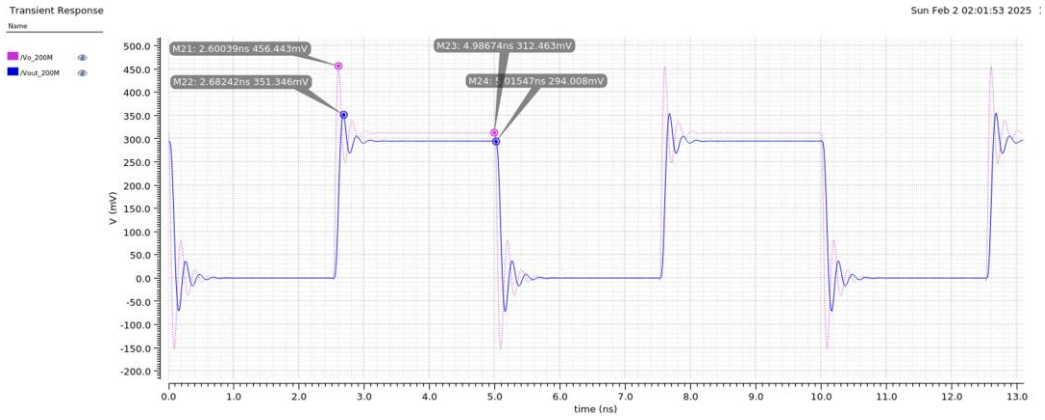
1.5G Vo at Mos and Vout at load



Ideal case



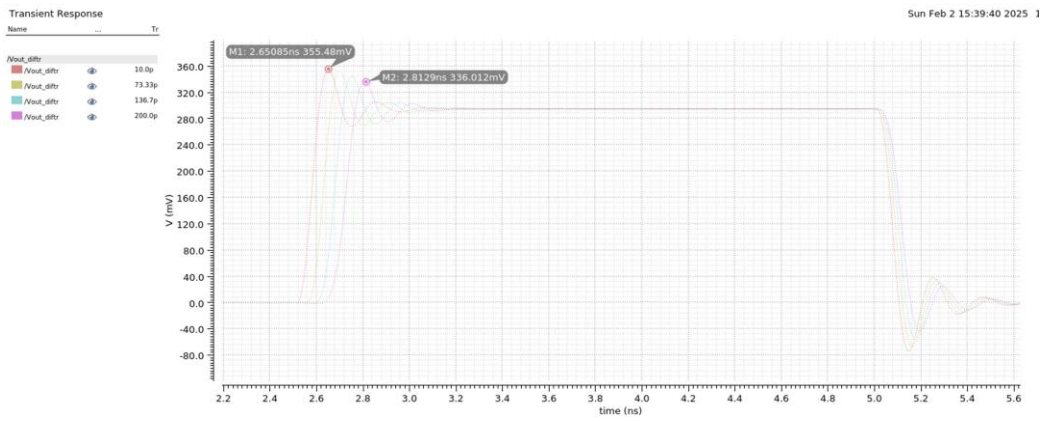
Vo for ideal case (no effect of LC)



Vo for Vin=200M (the)

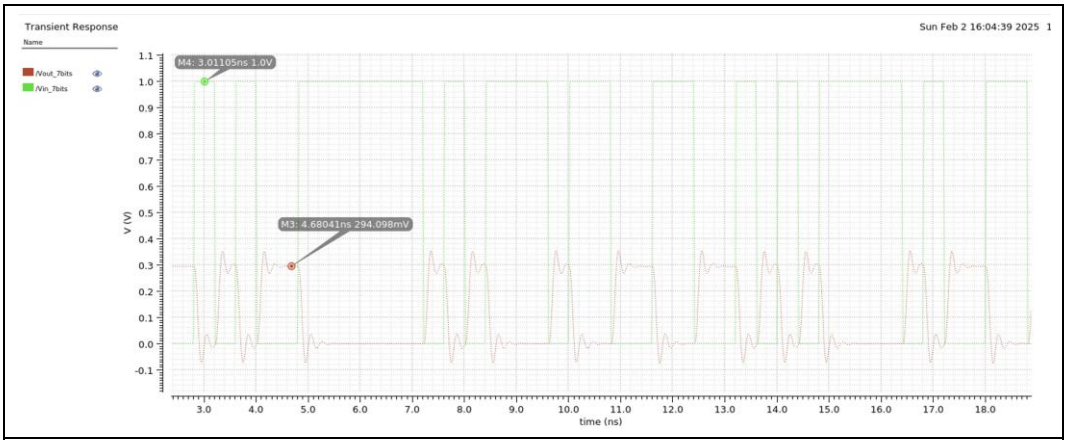
The τ for L&C= Z0*C/2 or L/2*Zo, doesn't relate to Vin frequency, which means the τ happens time won't change.

Since the Vin frequencey is lower (period is longer), after the τ happens time, there are more time (period) to present the stable state compare to high Vin frequency.



Changing the tr for Vin will affect the peak for peak voltage

Peak voltage spike magnitude: $$\frac{\Delta V}{V} = \left(\frac{\tau}{t_r}\right)\left[1 - e^{\left(\frac{-t_r}{\tau}\right)}\right]$$



7-bit 2.5Gb/s PRBS (pseudo random bits) input data

For mos it is acting like a switch (Vin= 1 Vo= 0)

Same with the case in low freq Vin, if the Vin got 2 same digit ,for instance, 0011101, there will be more time to repersent the stable state after thet for LC

c. Suppose the same buffer is used to transmit the signal through two segments of PCB trace as shown in Figure 12. Z01 is 50 Ω and Z02 is 80 Ω. Please use only resistors to design the termination so that there are no reflections from a wave traveling from left to right. What kind of modification is needed to output a 300mVpp signal at Vout?

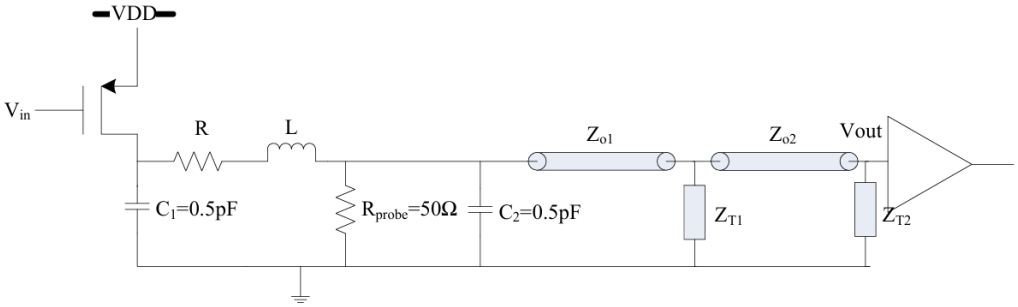
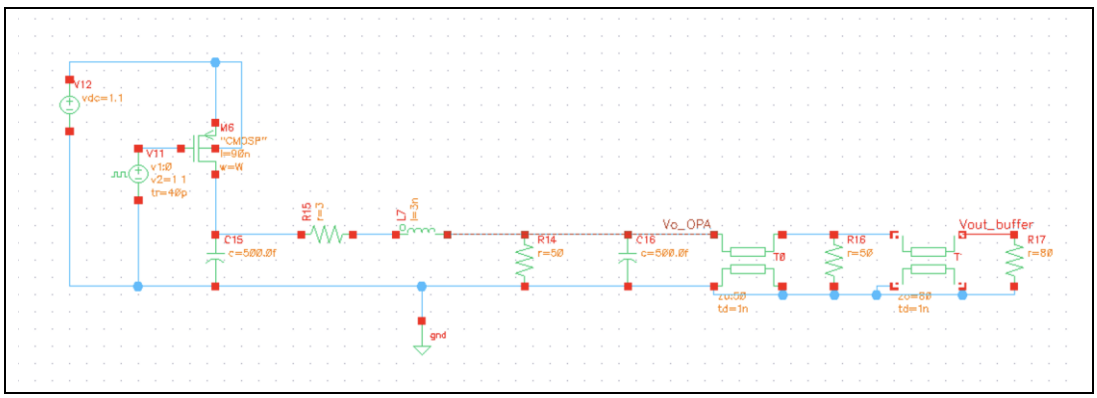
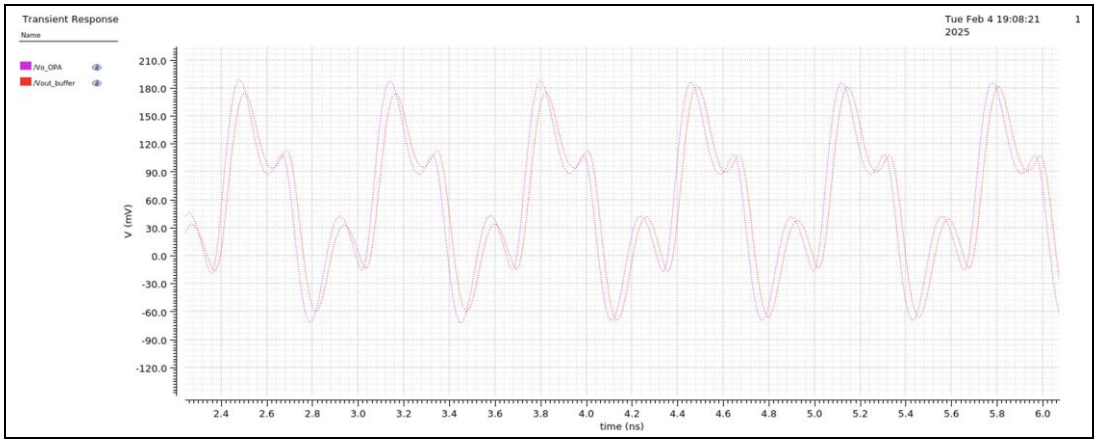


Figure 12 Transmission Line Matching Network





d. The signal at the output contains ripple (inter symbol interference (ISI)). What kind of problems it may introduce to the receiver stage?

- ISI causes overlapping between symbols, making it harder for the receiver to distinguish between consecutive bits, leading to an increased **Bit Error Rate (BER)**.
- Ripple distorts signal transitions, causing **timing uncertainty (jitter)**, which affects clock recovery and sampling accuracy in **high-speed receivers**.
- ISI distorts the signal waveform, reducing the **eye opening** in an **eye diagram**, indicating poor signal integrity and difficult bit detection.

4. Please develop a model circuit composed of ideal transmission lines, inductors, resistors, and capacitors which generates the same response as Figure 13. The input rise time is 0.1ns. Please show your model circuits and Cadence simulation result.

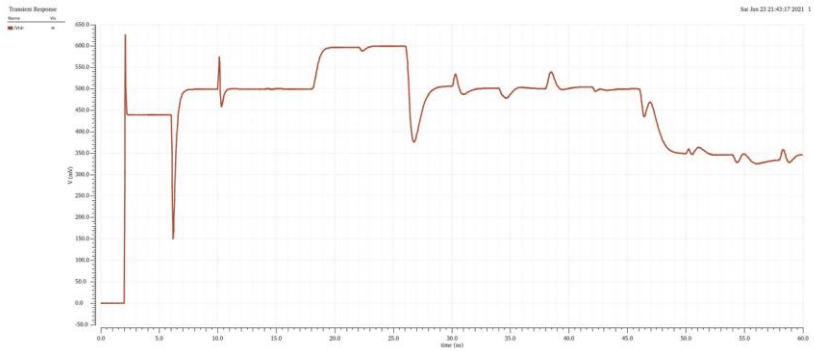
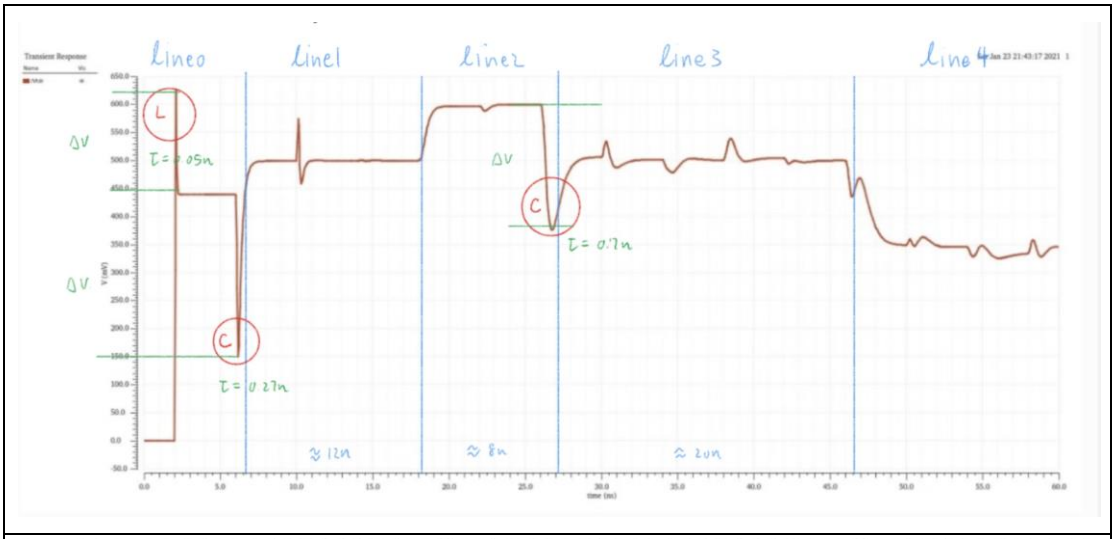
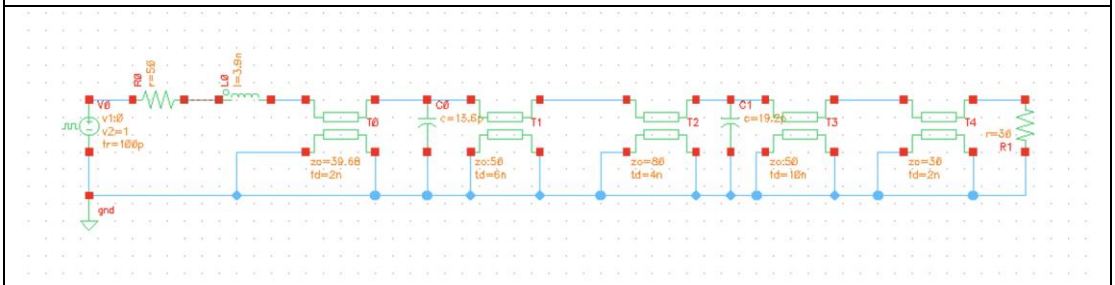
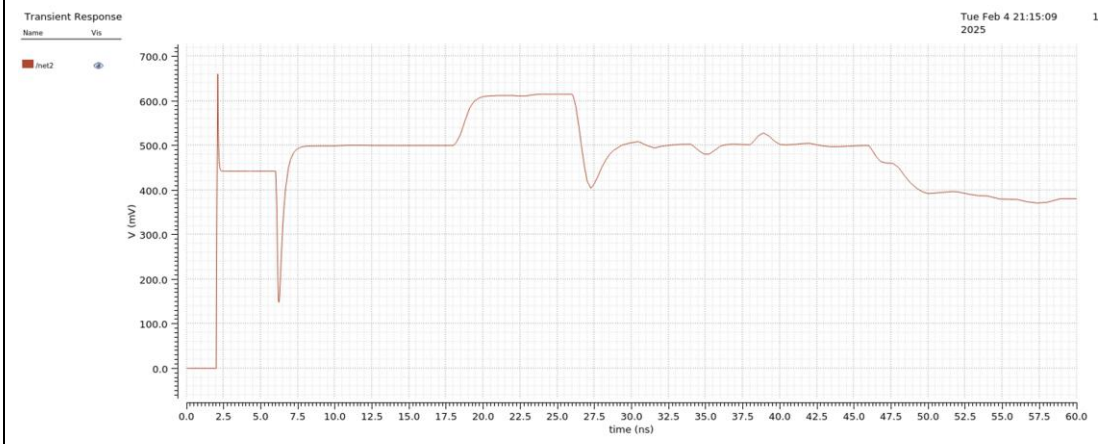


Figure 13 TDR Response







The reflection for the transmission line will be partial Vin (line0) – krT1> 0 (ZT line1> Zo line0) – krT2> 0 (ZT line2> Zo line1) – krT3< 0 (ZT line3< Zo line2) – krT4> 0 (ZT line4< Zo line3)

The high peak represents a L and low peak represent C (if the DC level after the peak change, if didn't change, than it might cause of reflection)

The delay time can be count by the Tround-trip= Tdealy*2, knowing the DC level continued time/2 can get the delay time of transmission line.