25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab4: Receiver Circuits

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Section:700

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1. Generally, circuits are designed to handle a minimum variation range of ±3σ, where σ is the standard deviation of the variable under study. What is the yield rate for ±σ, ±2σ, ±3σ, and ±4σ assuming a Gaussian distribution?

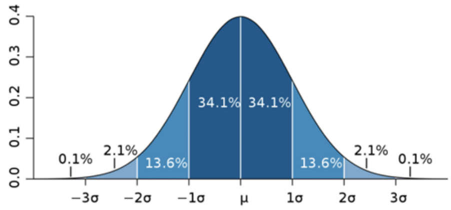


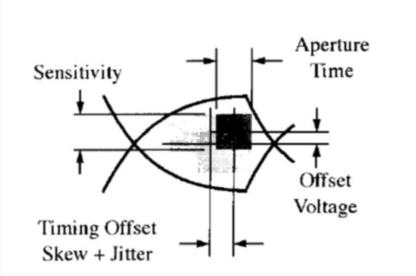
Figure 8 Gaussian distribution

Range (±σ)	Coverage Probability	Yield Rate (%)
±1σ	68.27%	68.27%
±2σ	95.45%	95.45%
±3σ	99.73%	99.73%
±4σ	99.93%	99.93%

- If a circuit design allows ±3σ variation, the yield rate is approximately 99.73%, meaning **around 27 out of 10,000 units might be out of spec**.
- If the design tolerates ±4σ, the yield increases to 99.9937%, ensuring almost all products meet specifications.

2. A receiver is characterized by its input sensitivity which represents the voltage resolution, and by the set-up and hold times (tS and tH) which represent the timing resolution as illustrated with the light rectangle in Figure 1. The center of the dark rectangle is shifted by the offset time and offset voltage from the center of the light rectangle. Input sensitivity consists of input voltage offset, input referred noise, and minimum latch resolution voltage. A Strong-Arm latch input static voltage offset is 10mV, minimum latch resolution from hysteresis is bounded to 2mV, and 2mV sigma of input referred noise. The aperture time and the combined set-up and hold time (tS+tH) of the latch are 10ps and 20ps, respectively. Also assume that the receiver sampling clock has a 10ps timing offset and 1ps sigma of random jitter. The target BER is 10-12 (Hint: how many standard deviations does this imply?)

On the 6Gb/s NRZ eye diagram obtained in Lab 2 over B12 backplane channel (either from MATLAB or CADENCE), draw the window that the incoming signal needs to avoid such that the receiver will reliably translate the voltage waveform received from the channel into logic 1's or 0's under worst-case combinations of offsets and resolution.



$BER = 10^{-12}$

CDF cumulative distribution function $P(X > k\sigma) = 1 - \Phi(k)$

$\phi(k) = CDF$

$1 - \phi(k) = 10^{-12}$ $\phi(7) \approx 1 - 10^{-12}$ $k \approx 7$

7σ standard deviation

time : aperture time 10ps setup hold on 20ps

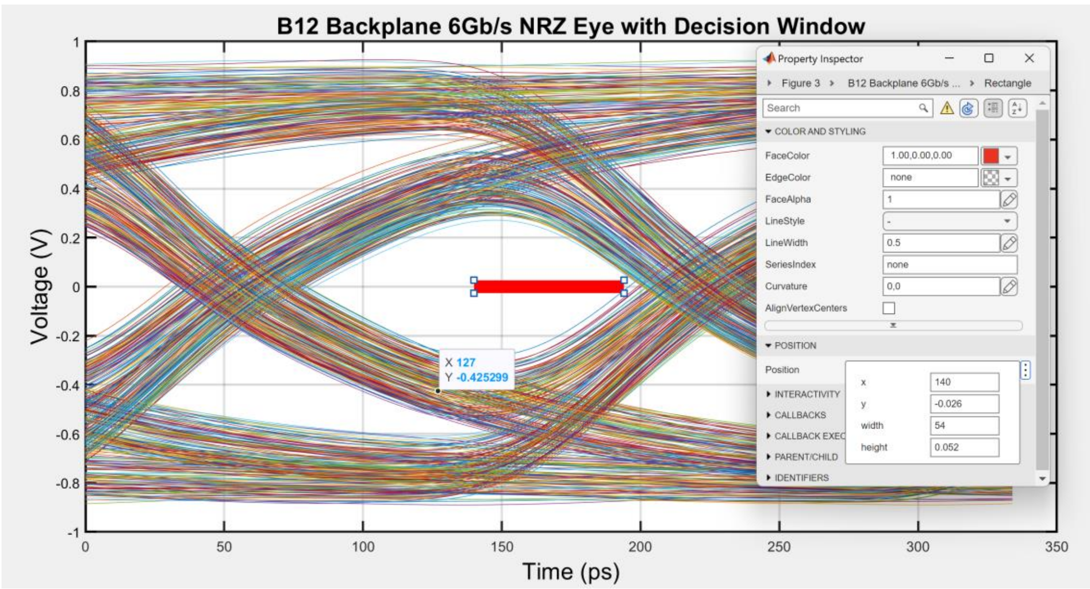
timing offset 10ps random jitter σ = 1ps

10ps + 7ps + 10ps = 27ps

voltage : input offset 10mV. min latch resolution 2m

input noise σ = 2m

10 mV. + 14mV. + 2mV. = 26mV.



3. Demultiplexer (DeMUX) is often used to deserialize a stream of high speed data. It can be implemented after the receiver circuit to generate lower speed data. Please design a 1:4 binary-tree DeMUX that deserializes 6Gb/s data into 1.5Gb/s data. Figure 9 is an example of 1:2 De-MUX, please refer to [3] as a reference. You may use behavioral models to implement the building blocks in the DeMUX. Plot the simulation results that verify the operation of DeMUX.

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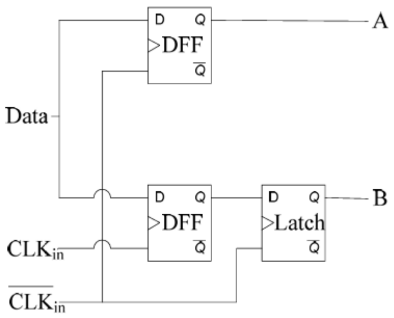
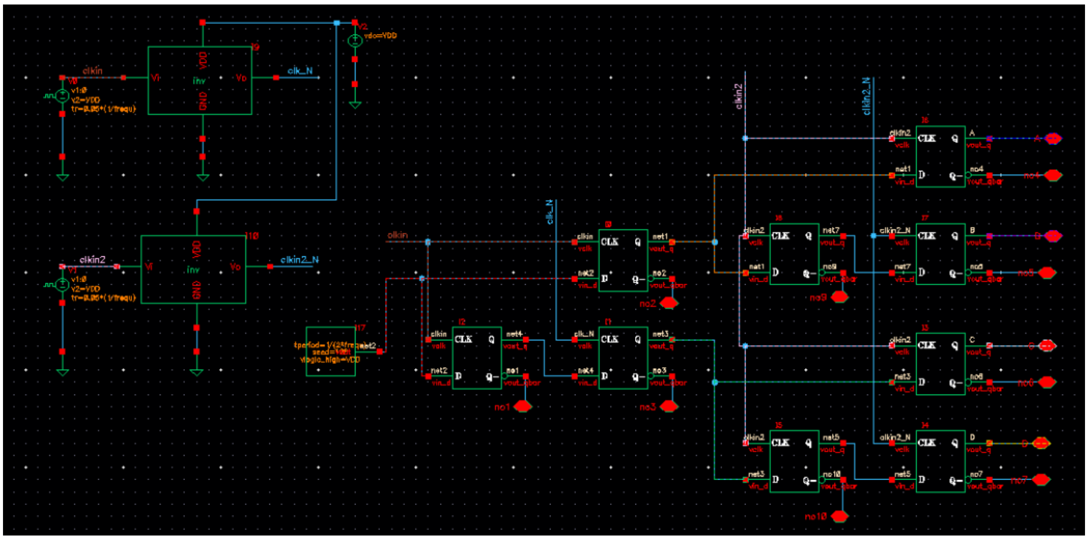
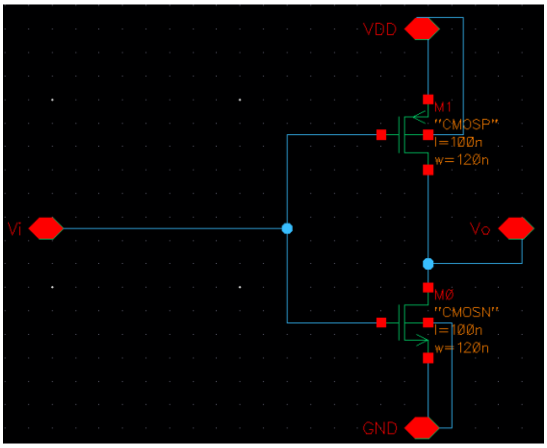
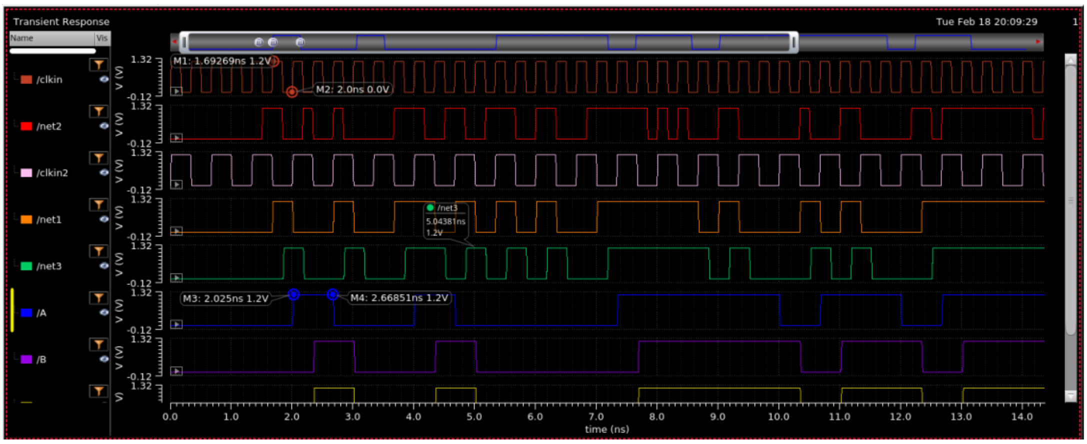


Figure 9 1:2 Data De-MUX [3]



Using 3G for first stage decoding, and 1.5G for second stage decoding





- Appendix

channel_data.m
channel_data_lab.m
channel_prelab4.asv
channel_prelab4.m
data_channel.mat
ir_B12.mat
peters_01_0605_B12_thru.s4p
read_sparam.m
xfr_fn_to_imp.m

Details

```
% === 參數設定 ===
aperture_time = 10;      % 10 ps Aperture time
setup_hold_time = 20;    % 20 ps Setup + Hold time
timing_offset = 10;      % 10 ps Timing offset
jitter_sigma = 1;        % 1 ps Random jitter
voltage_offset = 10e-3;     % 10 mV Static voltage offset
latch_resolution = 2e-3;    % 2 mV Minimum latch resolution
input_noise_sigma = 2e-3;   % 2 mV Input referred noise
BER_target_sigma = 7;       % BER = 10^-12 (7σ)

% === window range ===
total_timing_offset = timing_offset + BER_target_sigma * jitter_sigma;
decision_time_width = 2 * (aperture_time + total_timing_offset);
% 27ps*2
total_voltage_offset = voltage_offset + latch_resolution;
decision_voltage_height = 2 * (total_voltage_offset + BER_target_sigma * input_noise_sigma);
% 26mv*2

% === eyedigram center ===
decision_time_center = bit_period ; % time center
decision_voltage_center = 0; % NRZ signal center

% === plot window ===
rectangle('Position', [decision_time_center - decision_time_width / 2 , decision_voltage_center - decision_voltag
          'FaceColor', [1, 0, 0, 0.3], 'EdgeColor', 'none'); % 半透明紅色矩形
```

```
102  _time_center - decision_time_width / 2 , decision_voltage_center - decision_voltage_height/2, decision_time_width, decision_voltage_height],...
103  ), 0.3], 'EdgeColor', 'none'); % 半透明紅色矩形
```