

25 Spring ECEN 720: High-Speed Links: Circuits and
Systems Post-lab Report

Lab3: Transmitter Circuits

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- Transmitters can operate in voltage-mode or current-mode with single-ended termination or differential termination as shown in Figure 10. Please calculate the power consumption for (a) current-mode with single-ended, (b) current-mode with differential, (c) voltage-mode with single-ended, and (d) voltage-mode with differential termination, assuming V_d is the output swing and termination is 50Ω .

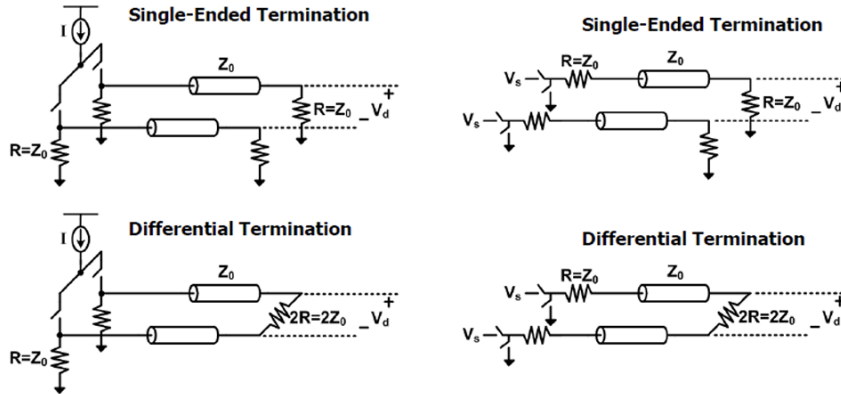


Figure 10 Current Mode and Voltage Mode Transmitters

- $V_{d,1} = (I/2) R$ $V_{d,0} = -(I/2)R$ $V_{d,pp} = IR$ $\text{Power} = I^2 R$
- $V_{d,1} = (I/4) 2R$ $V_{d,0} = -(I/4)2R$ $V_{d,pp} = IR$ $\text{Power} = I^2 R$
- $V_{d,1} = (V_s/2) R$ $V_{d,0} = -(V_s/2)R$ $V_{d,pp} = V_s$ $I = (V_s/2R)$ $\text{Power} = V_s^2/2R$
- $V_{d,1} = (V_s/2) R$ $V_{d,0} = -(V_s/2)R$ $V_{d,pp} = V_s$ $I = (V_s/4R)$ $\text{Power} = V_s^2/4R$

- A multiplexer (MUX) is often used to serialize parallel low speed data into one single stream of high speed data. It can be implemented before the transmitter output driver stage. Design a 4:1 MUX that serializes 4 parallel 2.5Gb/s data into a 10Gb/s bit-stream. Figure 11 is an example of 2:1 MUX with re-timer (please refer to [4] as a reference).

a. Use behavioral models for D-flip flops and latches. The AB select can be implemented using a transmission gate 2:1 MUX. Design the AB selector in transistor level.

b. Verify the MUX operation and show your schematic and simulation results.

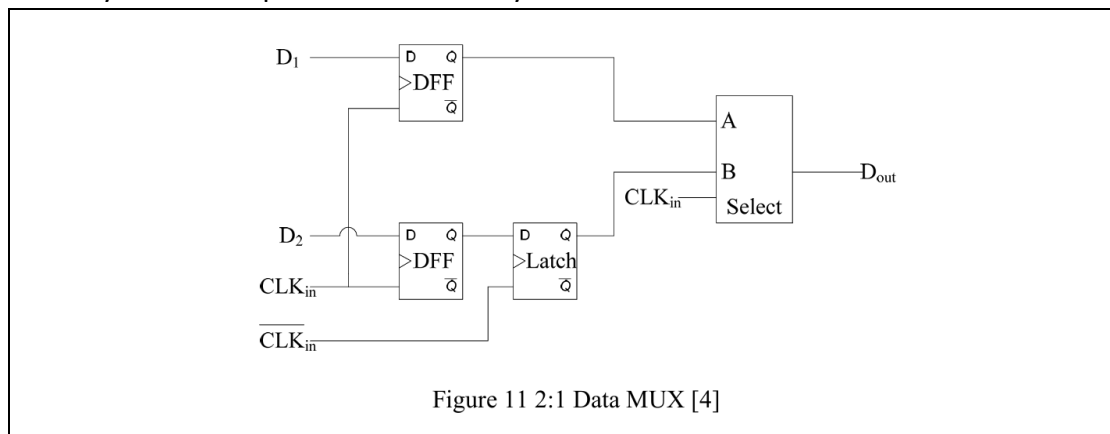
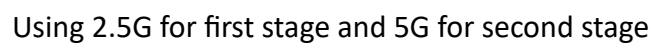
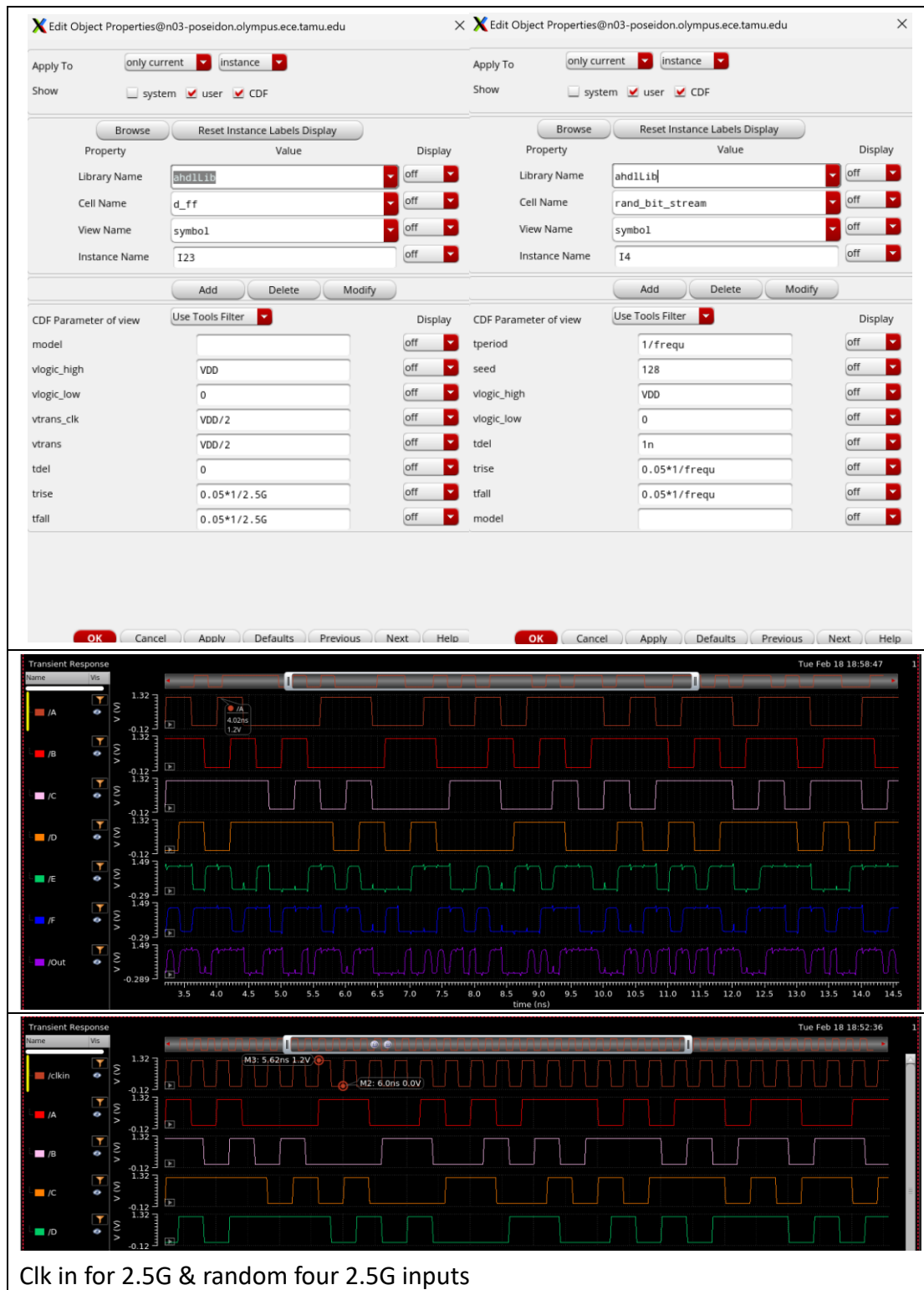
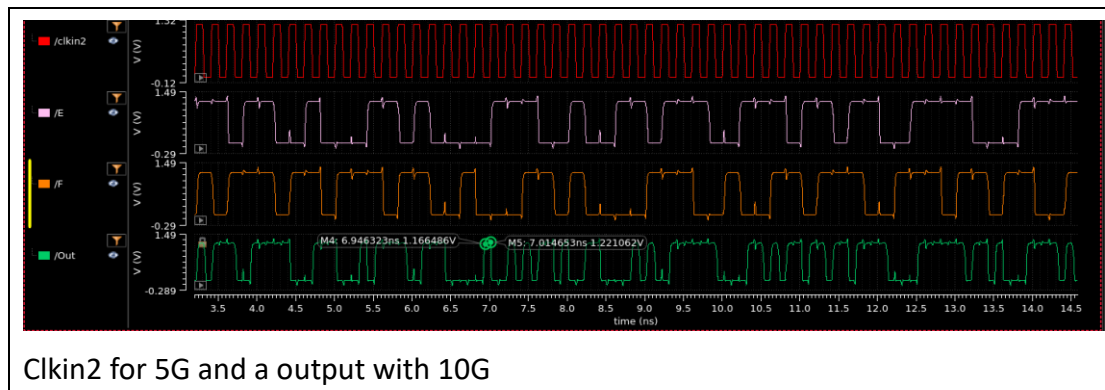


Figure 11 2:1 Data MUX [4]







3. 10Gb/s Low-Swing Driver and Termination Design. 8

- a. Design both a differential current-mode CML driver and a differential low-swing voltage-mode driver to support an output swing of 300mVppd. For the Low-Swing Voltage-Mode Driver, please refer to [2] [3]. i. ii. For the CML driver, the output tail current source should be implemented at the transistor level, but you may use a current mirror that has an ideal current source to produce the bias for the output stage tail current source. For the voltage-mode driver, design the regulator and driver circuit. If op-amps are needed, feel free to use behavioral op-amp models.
- b. Include one pre-driver stage (in transistor level) before the driver output stage. This may be a simple inverter pre-driver or something more complex if you want.
- c. The driver should be terminated on-chip both at the transmitter and the receiver as shown in Figure 12. The termination should be designed to handle a temperature variation from 0 to 100°C OR a variation of $\pm 30\%$ from the nominal 27°C value if the temperature variation simulation doesn't work. Passive termination may be used, however a realistic model including parasitic capacitance must be used, i.e., from a design kit or taken from the table in lecture 5. Choose whichever termination scheme you think is most appropriate (AC vs DC-coupled, single-ended vs differential) and briefly explain your choice.
- d. Since the emphasis of this problem is the driver design, in your simulations use a simple channel consisting of TX output cap = RX input cap = 100fF and an ideal 50 Ω , 1ns transmission line.
- e. Turn-in the following for your design i. ii. iii. iv. Schematics with details of transistor sizing. A 10Gb/s eye diagram at the RX. Use a pseudo-random input sequence of 27-1 or higher to produce the eye diagram. Plot the return loss versus frequency looking back into the transmitter at 0, 27, and 100°C. For this, program the termination to yield the best performance at each temperature. Note: if your temperature variation simulations don't work, then just turn in one plot at 27°C and data showing that your termination can tune $\pm 30\%$. Compare the power consumption of the two drivers. Break down the power into pre-driver and output stage power.

