25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab3: Transmitter Circuits

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a. Figure 8. The easiest way to do this is to run a DC sweep with $|V_{GS}|$ varying from 0 to VDD and plot the following equation.

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{1}$$

Where C_{gg} is the total gate capacitance. Comment on the results. For the f_T plot versus $|V_{GS}|$, use a linear scale for both axes. For the f_T plot versus $|I_{DS}|$, use a log scale for the x-axis (current) and a linear scale for the y-axis (frequency). Discuss how this characterization data impacts the design of high-speed circuits.

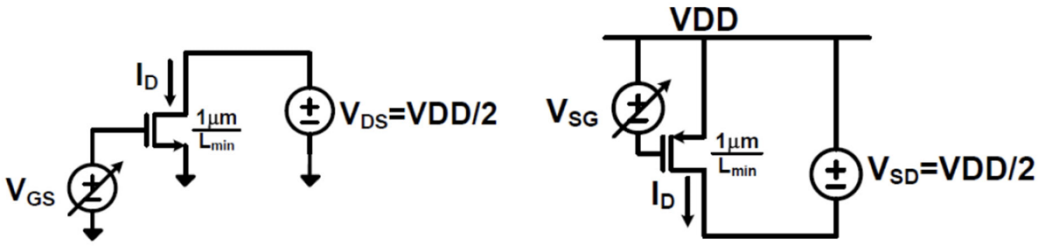
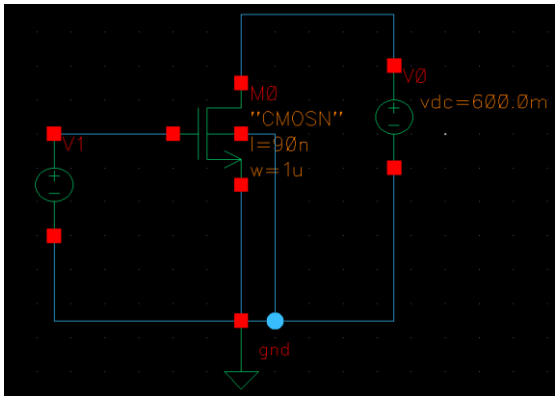
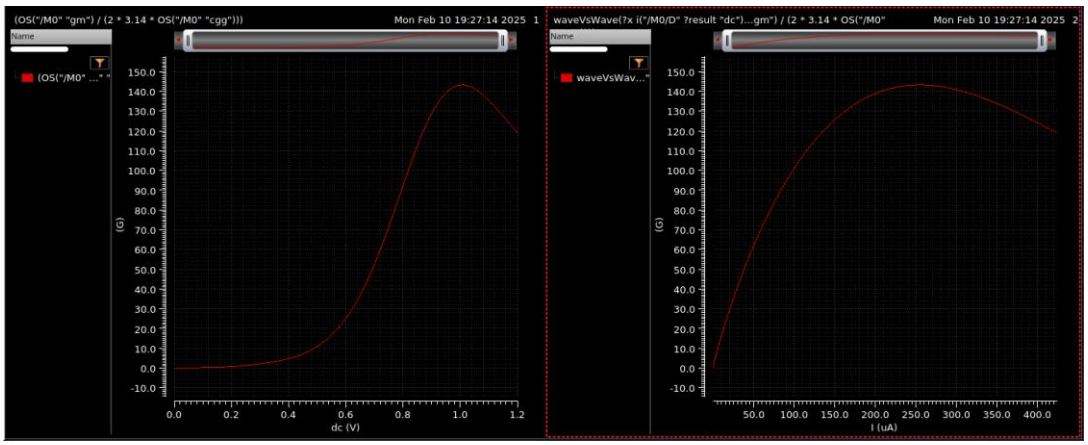
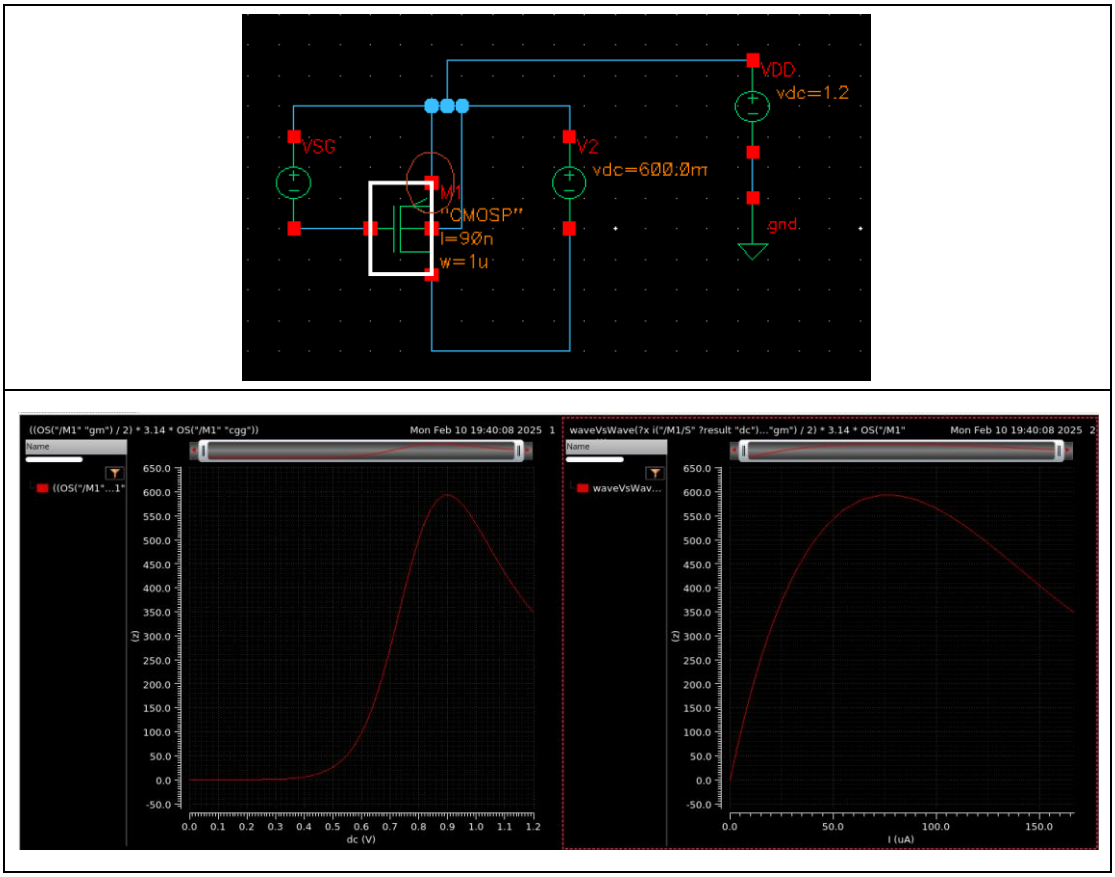


Figure 8 (a) NMOS f_T Test Circuit (b) PMOS f_T Test Circuit







b. Find the FO4 inverter delay. The bit-rate of transmitters is often limited by the bandwidth of clock buffering. For minimum propagation delay to drive a given capacitive load, a fan-out of four inverter buffer chain (FO4 inverter delay) is often used [5]. Refer to the instructions on how to use the default 90nm CMOS technology models for more details on how to setup the test circuit. For the inverters use minimum channel length and an NMOS unit finger width of 1µm. Size the PMOS/NMOS ratio of the inverter for equal rise and fall delays, measured from 50% of the input to 50% of the output. However, don't exceed a PMOS/NMOS ratio of 3, i.e., if the simulations show that a ratio greater than 3 is required for equal delay then just use 3 and accept the slight delay difference.

Sweep the supply voltage (VDD) from 0.7V to 1.2V with 50mV step size in order to include FO4 delay [ps] vs. VDD [V].

For the design of half-rate TX architecture, find optimal VDD for maximizing power efficiency at 5Gb/s data rate.

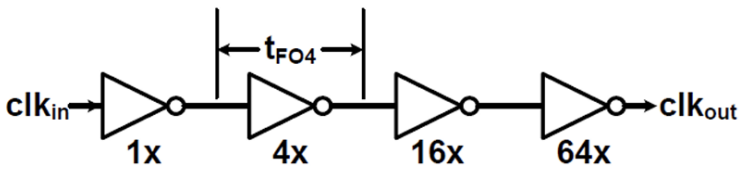
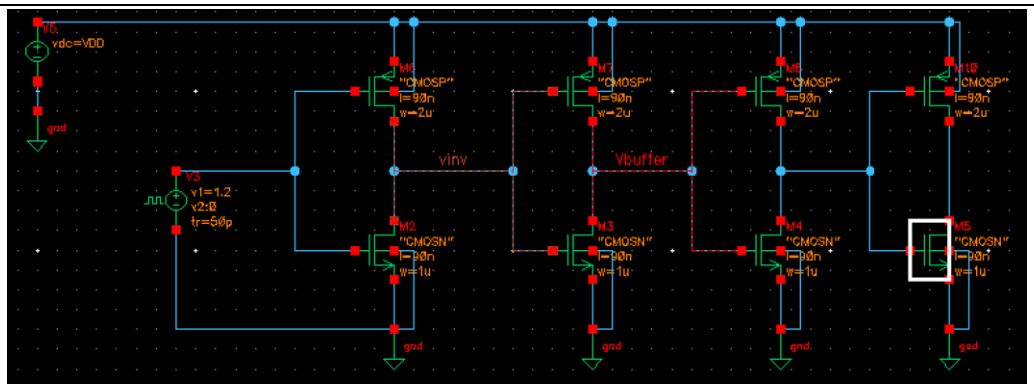


Figure 9 FO4 Delay Test Circuit


V5
vdc=VDD
gnd
V3
v1=1.2
v2=0
tr=50p
M6
"CMOSP"
l=90n
w=2u
M7
"CMOSP"
l=90n
w=2u
M8
"CMOSP"
l=90n
w=2u
M18
"CMOSP"
l=90n
w=2u
vinv
Vbuffer
M2
"CMOSN"
l=90n
w=1u
M3
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w=1u
M4
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w=1u
M5
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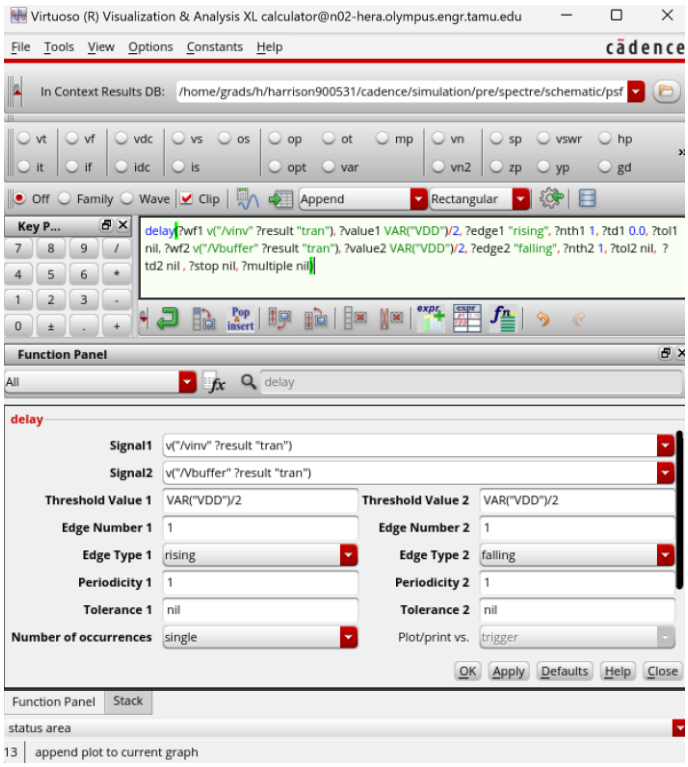
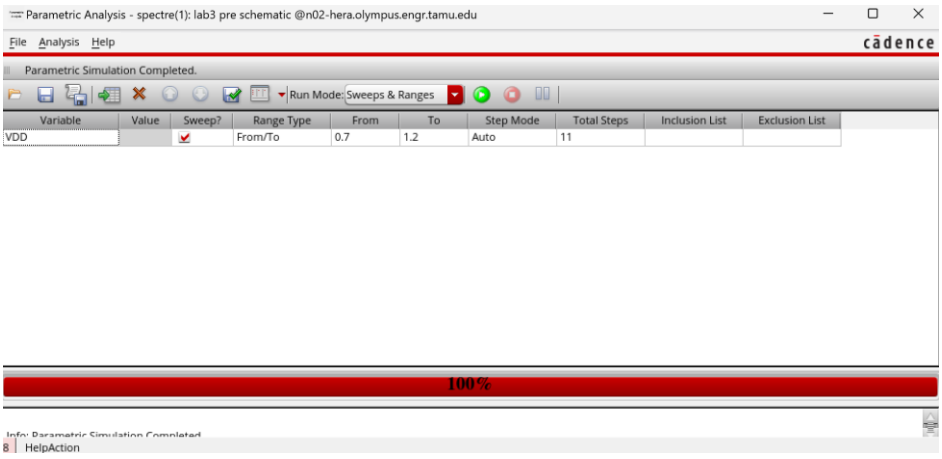
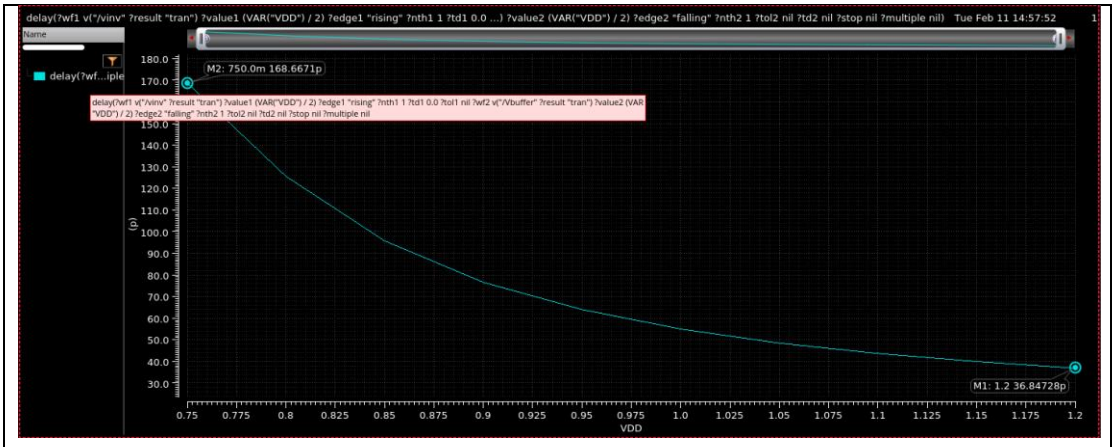
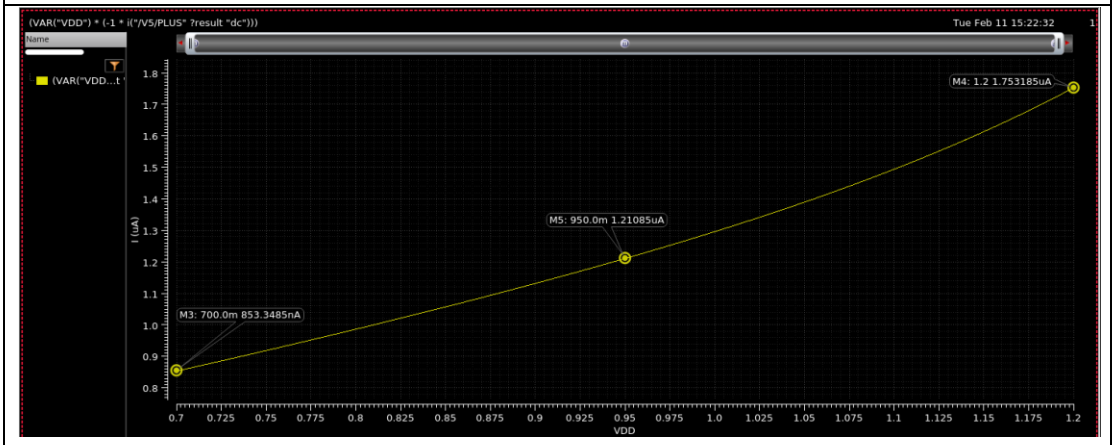
l=90n
w=1u
gnd
gnd
gnd
gnd


Virtuoso (R) Visualization & Analysis XL calculator@n02-hera.olympus.engr.tamu.edu
File Tools View Options Constants Help
cadence
In Context Results DB: /home/grads/h/harrison900531/cadence/simulation/pre/spectre/schematic/psf
vt vf vdc vs os op ot mp vn sp vswr hp
it if idc is opt var vn2 zp yp gd
Off Family Wave Clip Append Rectangular
Key P...
delay(?wf1 v("/vinv" ?result "tran"), ?value1 VAR("VDD")/2, ?edge1 "rising", ?nth1 1, ?td1 0.0, ?tol1 nil, ?wf2 v("/Vbuffer" ?result "tran"), ?value2 VAR("VDD")/2, ?edge2 "falling", ?nth2 1, ?tol2 nil, ?td2 nil , ?stop nil, ?multiple nil
Function Panel
All
delay
delay
Signal1 v("/vinv" ?result "tran")
Signal2 v("/Vbuffer" ?result "tran")
Threshold Value 1 VAR("VDD")/2
Threshold Value 2 VAR("VDD")/2
Edge Number 1 1
Edge Number 2 1
Edge Type 1 rising
Edge Type 2 falling
Periodicity 1 1
Periodicity 2 1
Tolerance 1 nil
Tolerance 2 nil
Number of occurrences single
Plot/print vs. trigger
OK Apply Defaults Help Close
Function Panel Stack
status area
13 append plot to current graph


Parametric Analysis - spectre(1): lab3 pre schematic @n02-hera.olympus.engr.tamu.edu
File Analysis Help
cadence
Parametric Simulation Completed.
Run Mode: Sweeps & Ranges
Variable Value Sweep? Range Type From To Step Mode Total Steps Inclusion List Exclusion List
VDD From/To 0.7 1.2 Auto 11
100%
8 HelpAction



FO4 sweep



The power

	VDD	(IS("/V5/...("/VDD"))	FO4
1	700.0E-3	77.62E-9	142.0E-12
2	750.0E-3	88.48E-9	102.2E-12
3	800.0E-3	100.3E-9	79.88E-12
4	850.0E-3	113.2E-9	66.86E-12
5	900.0E-3	127.4E-9	58.48E-12
6	950.0E-3	143.2E-9	53.10E-12
7	1.000	160.7E-9	49.21E-12
8	1.050	180.4E-9	46.35E-12
9	1.100	202.9E-9	44.16E-12
10	1.150	228.8E-9	42.36E-12
11	1.200	258.8E-9	41.00E-12

Finding the best operation point by power * FO4 (which is 0.9v)