25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

Lab4: Receiver Circuits

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Section:700

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Questions

1. High-Speed Comparator Design. This problem involves the design of four different high-speed comparators to meet the following specifications:

a. clk → Dout delay ≤ 150ps with a 10mV static differential input voltage (Din+−Din-) at a common mode voltage of 80% VDD. Measure delay from when the clock is at 50% VDD to Dout+ is at 50% VDD for an output rising transition. Please refer to Figure 18 in the Appendix.

b. Clock frequency = 3GHz. Use at least one inverter-based buffer to clock your circuit for realistic clock waveforms.

c. Load capacitance on Dout+ and Dout- is 10fF.

d. Input referred offset σ ≤ 10mV. Here you can optimistically assume that the input referred offset is just due to the input differential pair Vt (threshold voltage) mismatch and use the mismatch equation given in the notes, i.e., no need to run Monte Carlo simulations (although if you have access to a PDK that includes accurate statistical models of the CMOS devices you are encouraged to use Monte Carlo analysis).

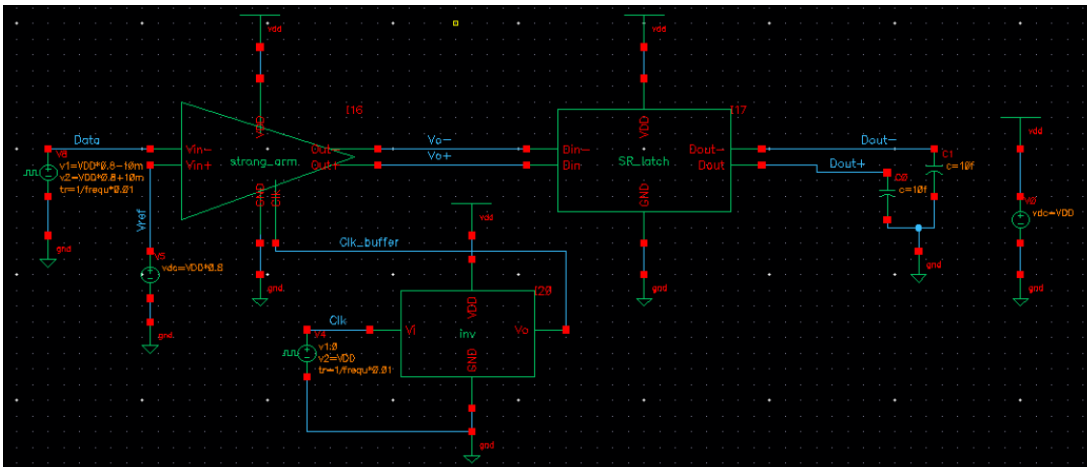
e. Optimize the design for power consumption, i.e., don't overdesign the comparator for a super small delay. Try to minimize total capacitance while still meeting the ≤ 150ps delay and σoffset ≤ 10mV offset specifications.

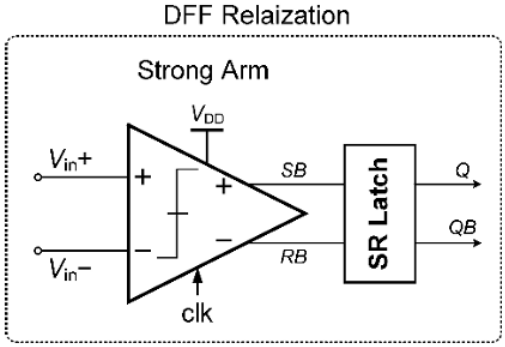
The comparators should realize a flip-flop function.

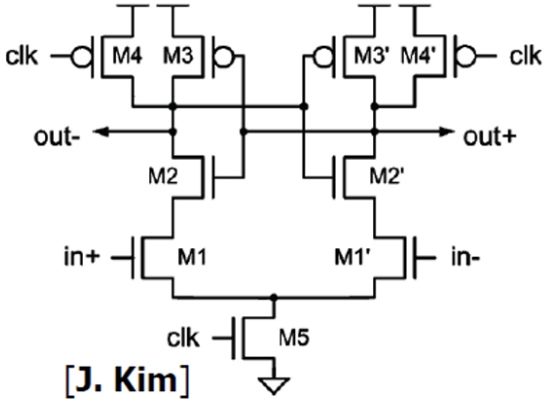
a. As shown in Figure 10, for the Strong-Arm type latches (1, 3, and 4) follow it with the optimized SR-latch shown in Figure 11. For more details on the optimized SR latch, refer to [8]. Note: for architecture (3) you will need to modify this optimized SR-latch – as the sense-amp pre-charges to GND (vs. VDD in 1 & 4).

b. To realize a CML flip-flop with architecture (2), simply cascade two CML latches to realize a master-slave flip-flop

a. Conventional Strong-Arm Latch. For an example schematic, refer to Figure 3(a). Feel free to change the pre-charge transistors configuration.







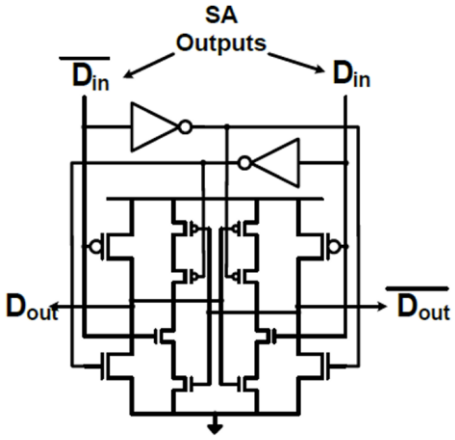
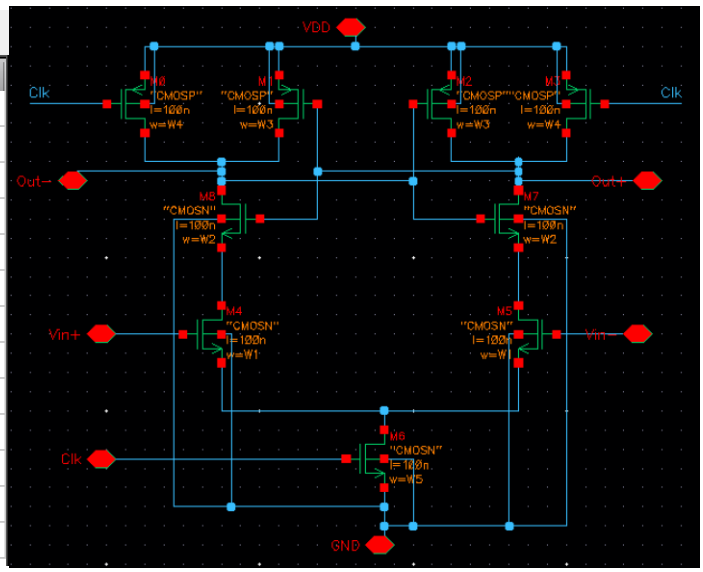
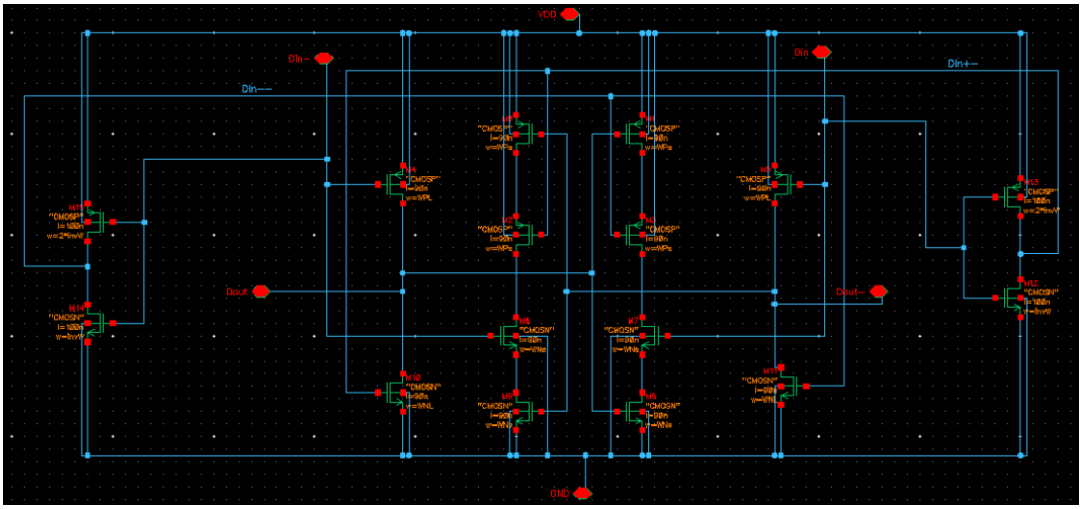


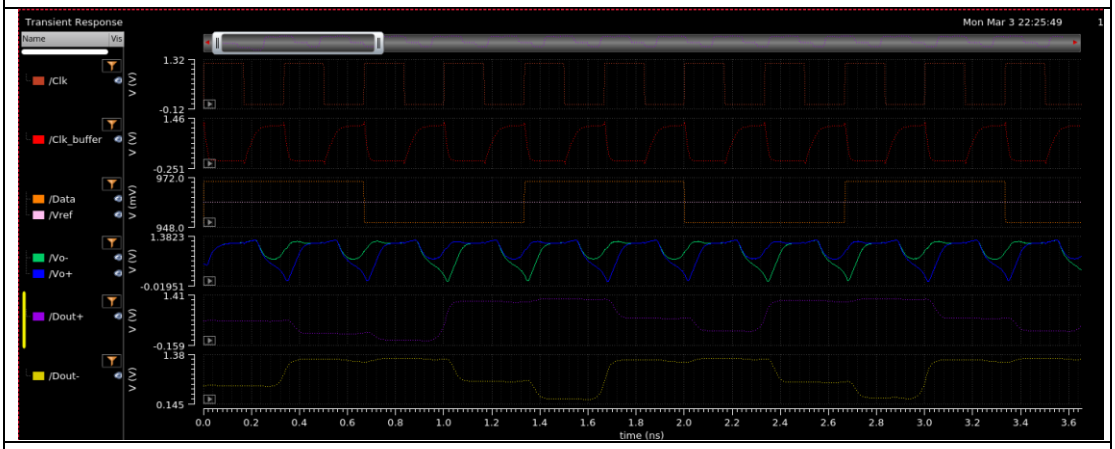
Figure 11 Optimized SR Latch [8]

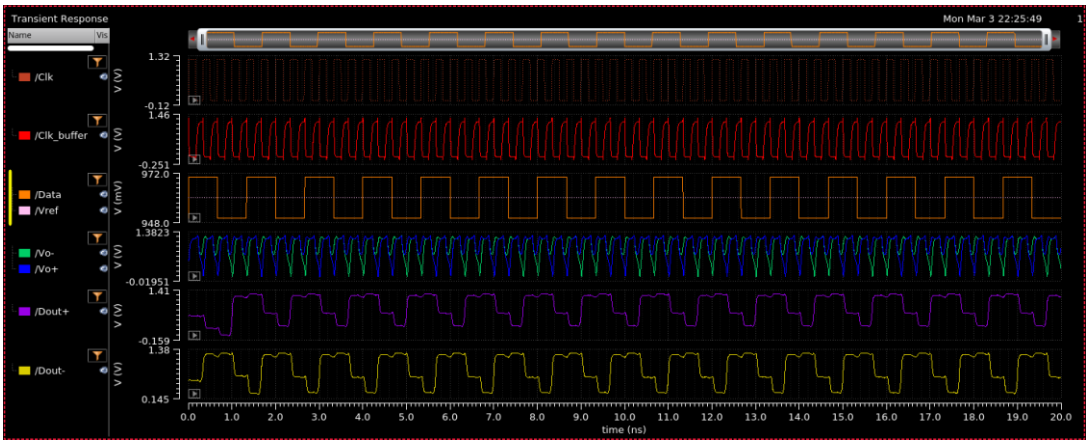
Design Variables

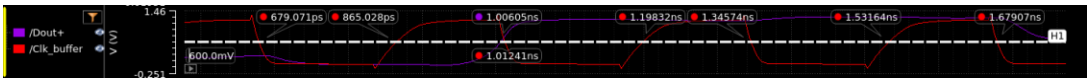
	Name	Value
1	W_buffer	2u
2	invW	120n
3	frequ	3G
4	VDD	1.2
5	W1	10u
6	W2	2u
7	W3	4u
8	W4	4u
9	W5	4u
10	WNL	2u
11	WNs	120n
12	WPL	4u
13	WPs	240n





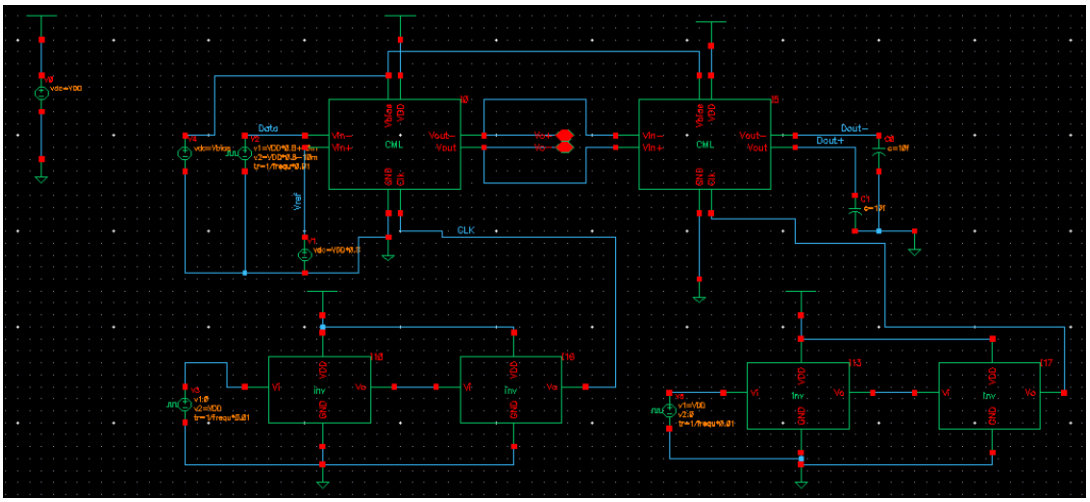


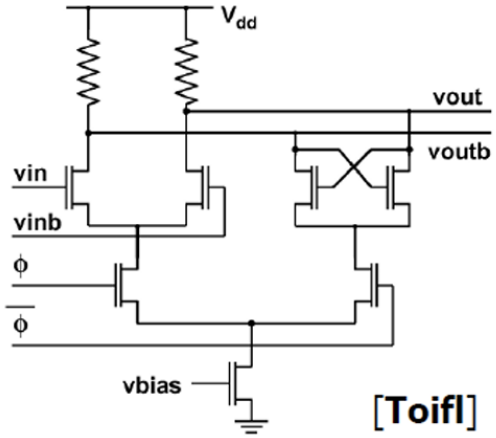




Delay: 141ps

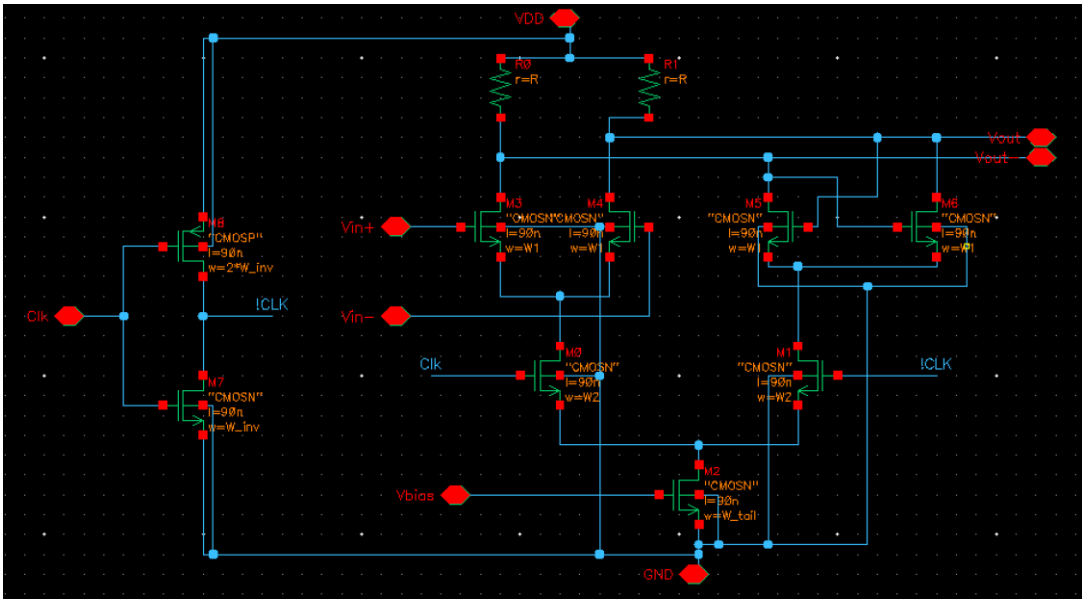
b. CML Latch. For an example schematic, refer to Figure 3(b).

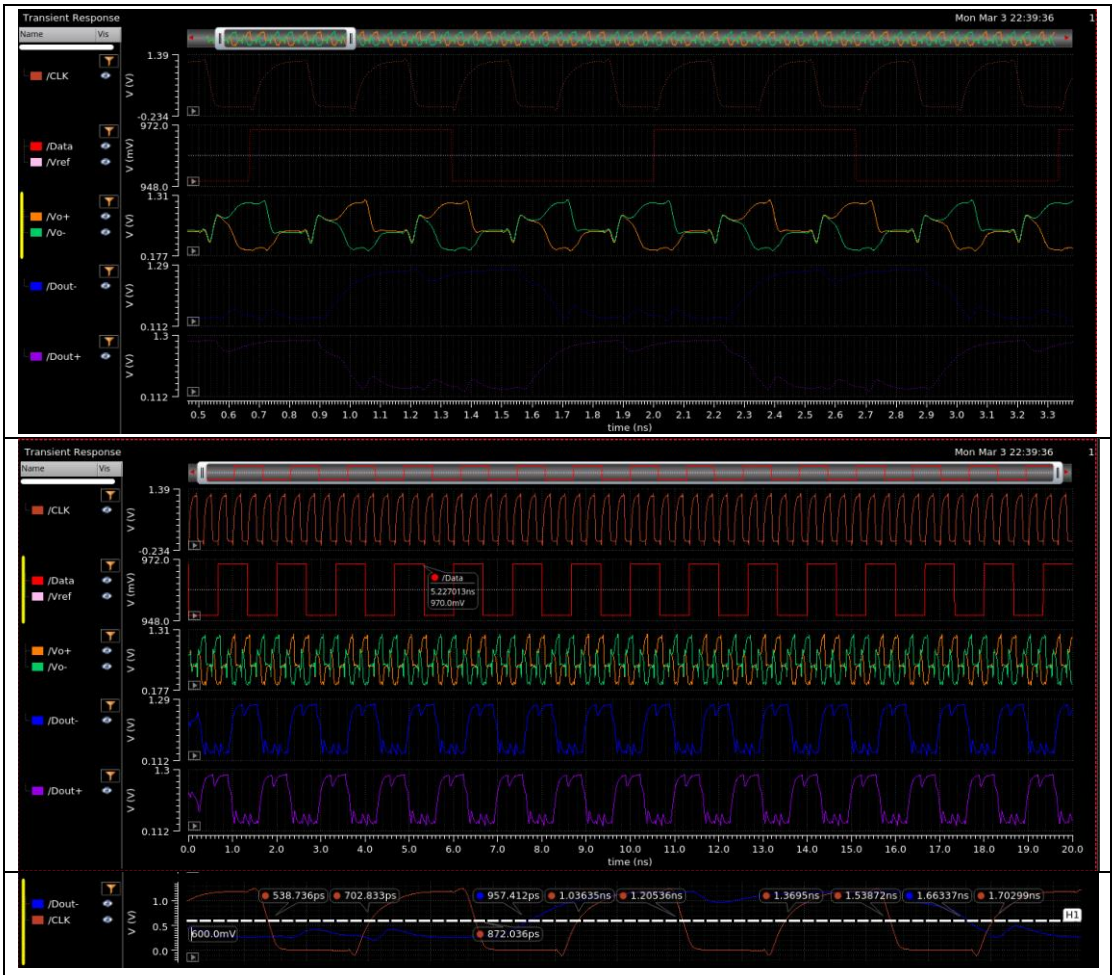




Design Variables

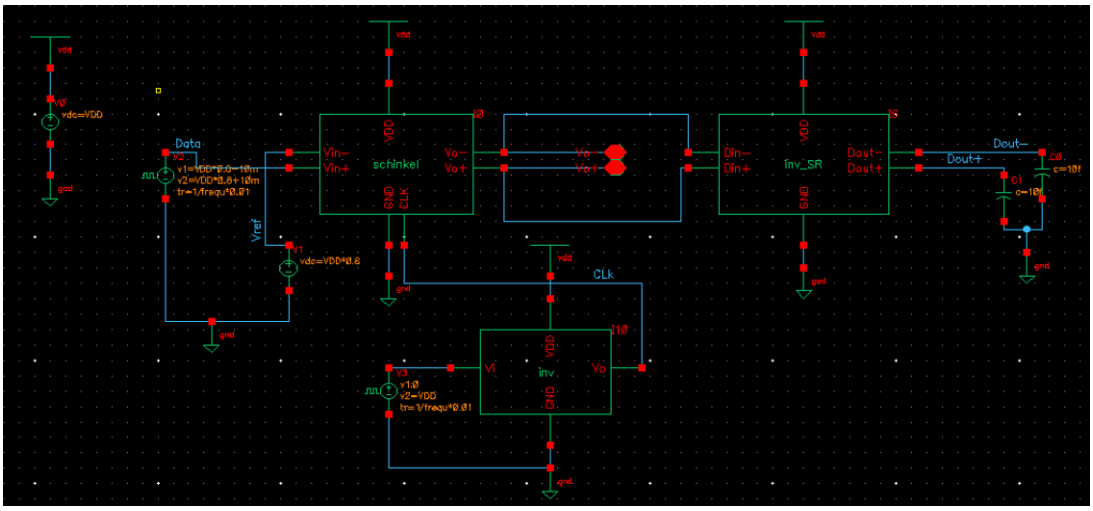
	Name	Value
1	R	5K
2	Vbias	900m
3	W_buffer	2u
4	frequ	3G
5	VDD	1.2
6	W_inv	2u
7	W1	1u
8	W2	8u
9	W_tail	4u

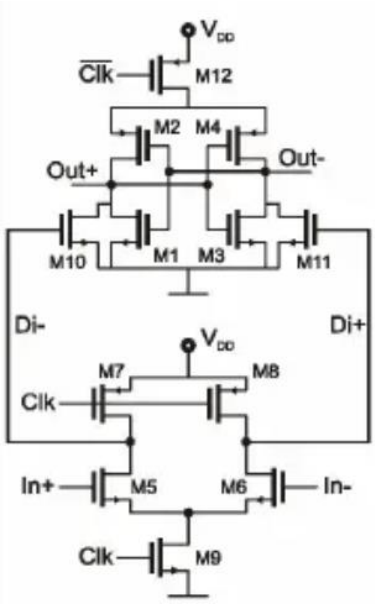




Delay: 254ps

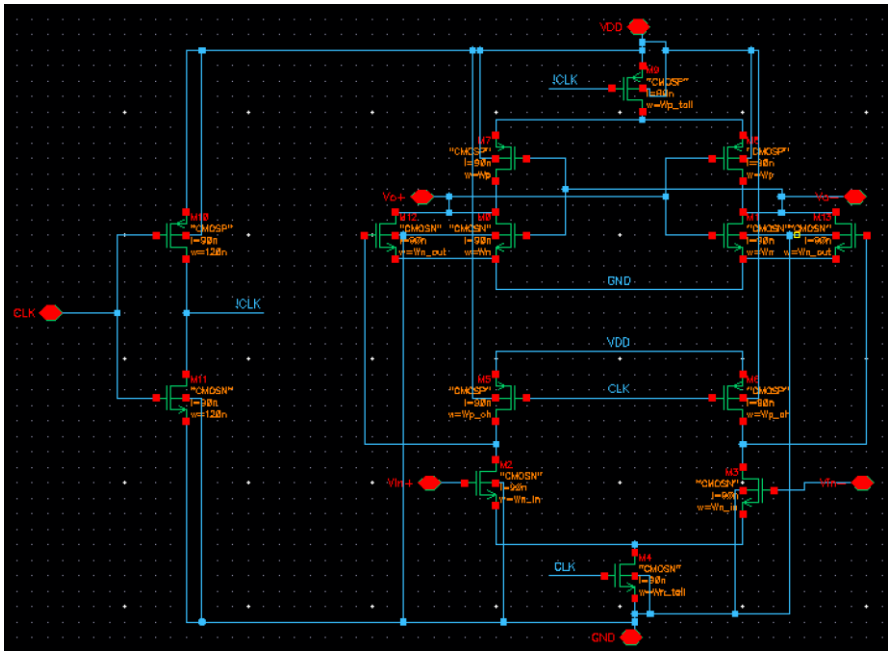
c. Schinkel Low-Voltage Latch. For an example schematic, refer to Figure 2 in [6].

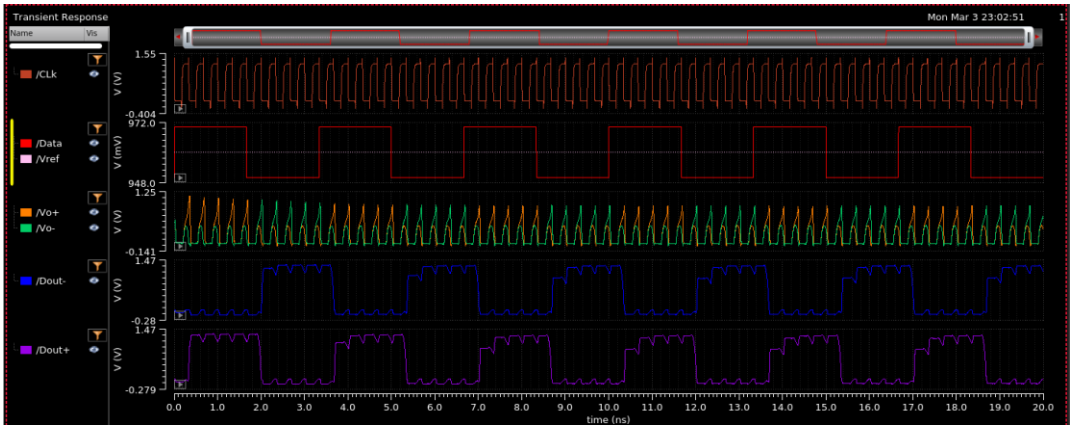


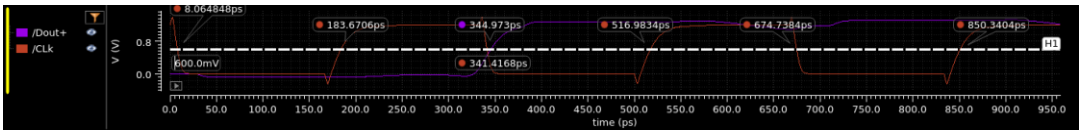


Design Variables

	Name	Value
1	W_buffer	40u
2	Wns	100n
3	WpL	4u
4	Wps	200n
5	WnL	8u
6	frequ	3G
7	VDD	1.2
8	W_inv	4u
9	Wp_ch	20u
10	Wn_out	30u
11	Wn	20u
12	Wn_in	20u
13	Wp	20u
14	Wp_tail	40u
15	Wn_tail	40u

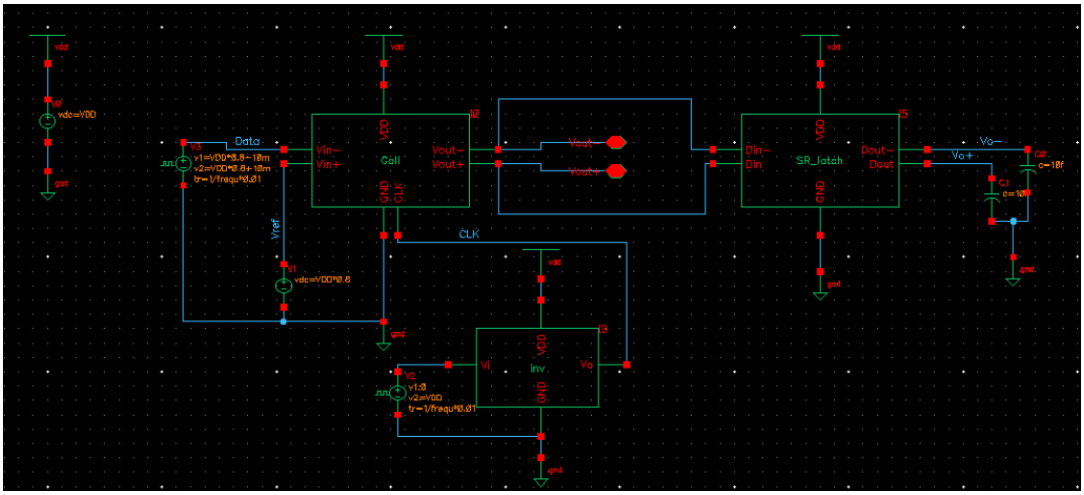


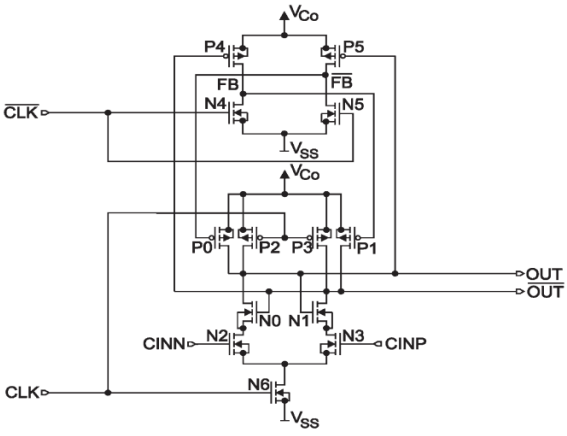




Delay time: 161.3 ps

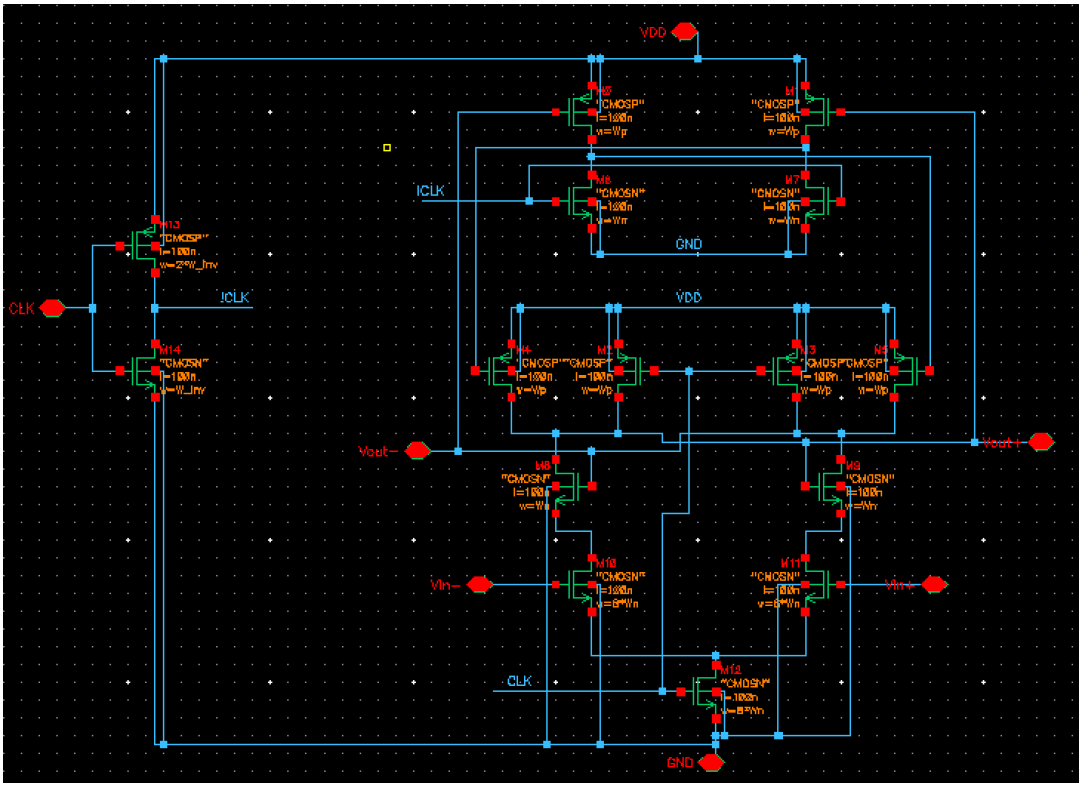
d. Goll Low-Voltage Latch. For an example schematic, refer to Figure 2 in [7].

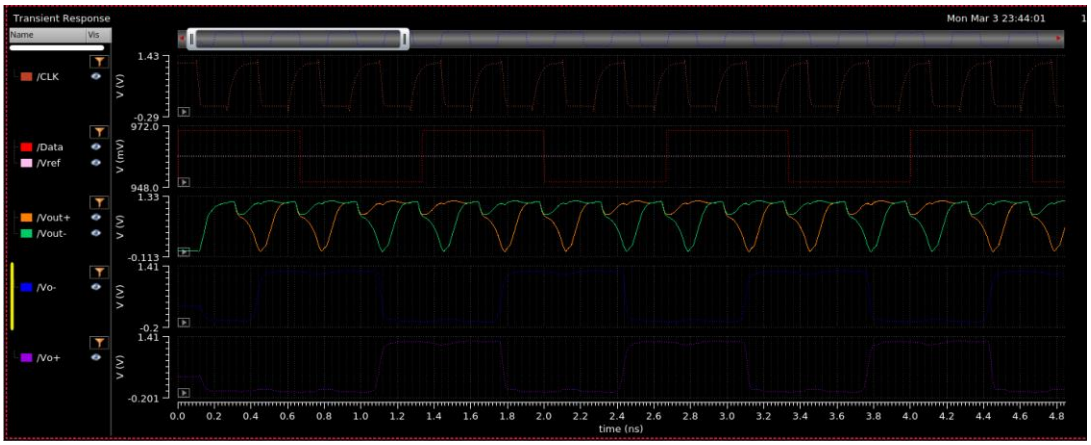


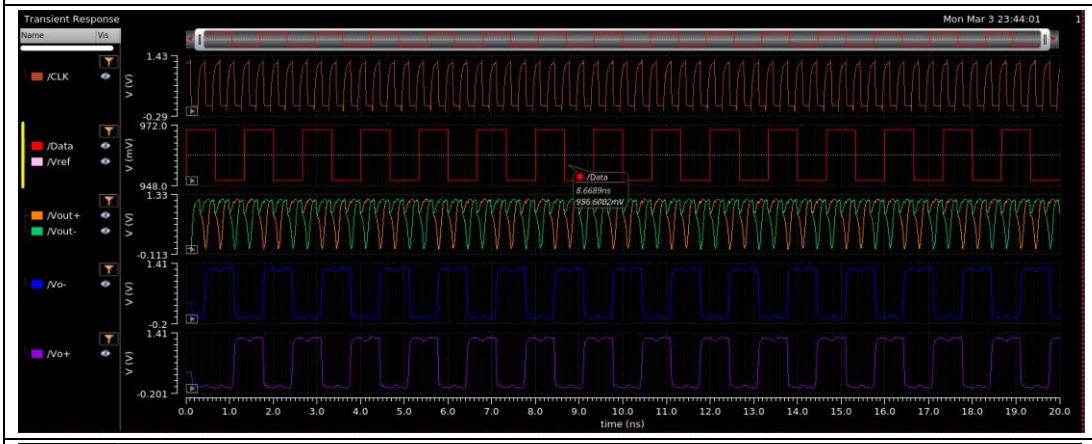


Design Variables

	Name	Value
1	W_buffer	4u
2	frequ	3G
3	VDD	1.2
4	WPL	4u
5	invW	2u
6	WNL	2u
7	Wn	2u
8	Wp	2u
9	W_inv	1u
10	WPs	200n
11	WNs	100n


VDD
ICLK
GND
CLK
!CLK
Vout-
Vout+
Vin-
Vin+


Transient Response
Mon Mar 3 23:44:01
/CLK
/Data
/Vref
/Vout+
/Vout-
/Vo-
/Vo+
V (V)
V (mV)
time (ns)


Transient Response
Mon Mar 3 23:44:01
/CLK
/Data
/Vref
/Vout+
/Vout-
/Vo-
/Vo+
V (V)
V (mV)
time (ns)


/Vo-
/CLK
V (V)
113.7773ps
293.8862ps
435.4299ps
627.3035ps
780.4365ps
960.5084ps
600.0mV
447.0621ps
1.119733ns

Delay time: 141.543ps

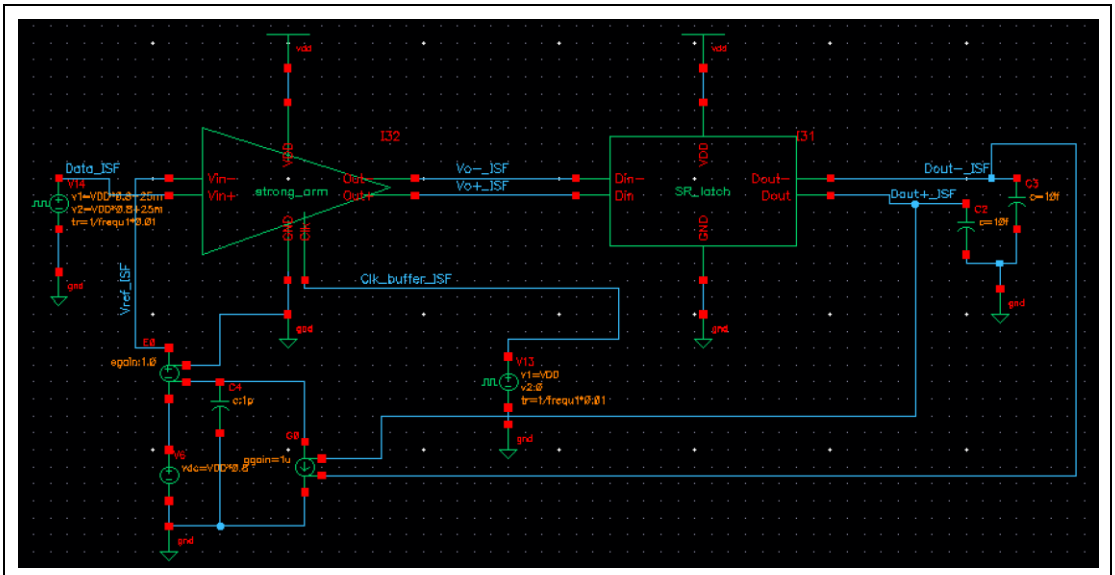
2. High-Speed Comparator Characterization. Please simulate all four comparators and produce the following using 500MHz (or less if necessary) clock signal:

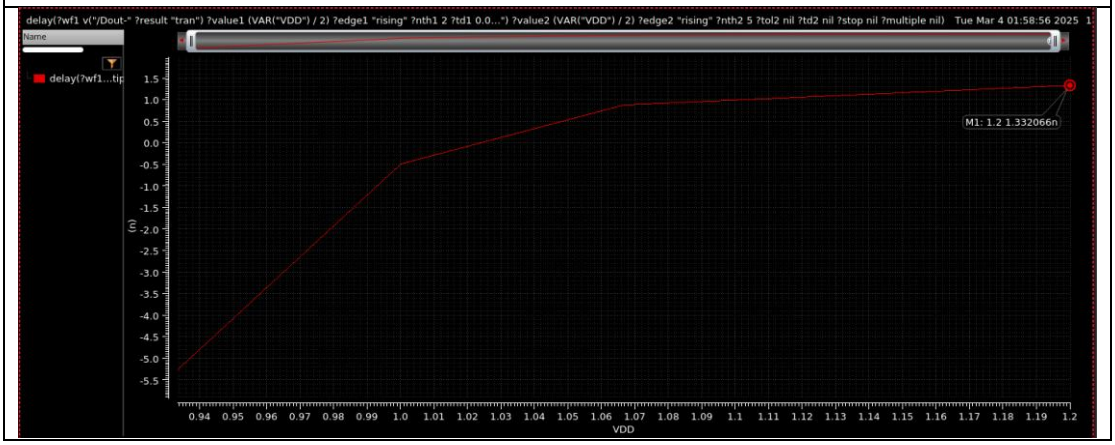
a. Plot comparator delay vs. VDD for VDD varying from 50% of nominal VDD to 100% VDD. For this keep the input common mode equal to 80% of the supply, i.e., sweep the input common-mode along with the supply. Also scale the clock input signal level with VDD.

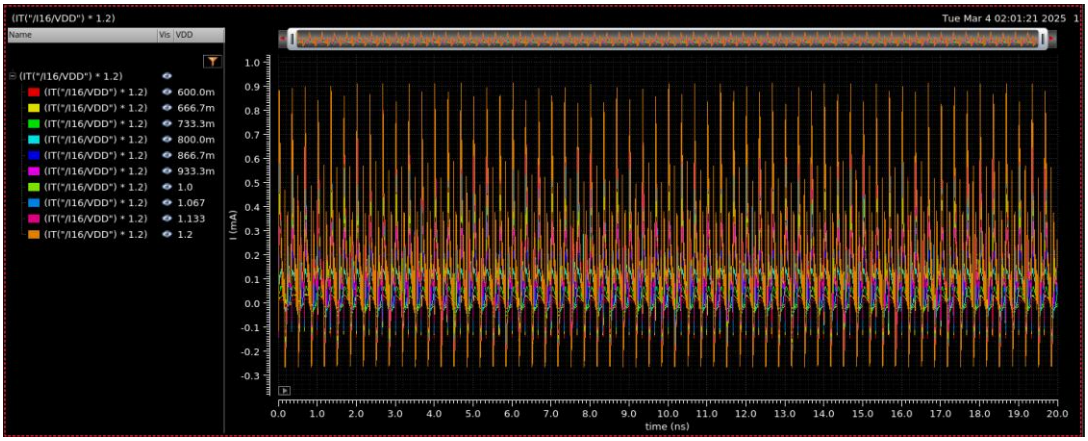
b. Plot comparator power vs. VDD in a similar manner.

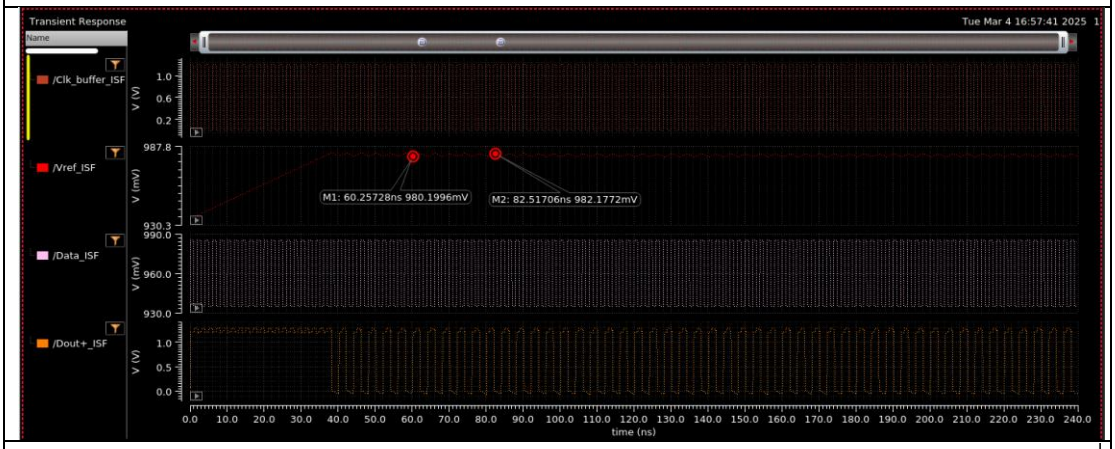
c. Generate the comparator Impulse Sensitivity Function (ISF) at the nominal VDD, 80%VDD, and 60%VDD (3 curves). Again, track the input common-mode with VDD (for more details refer to [2]). For the ISF-based characterization use an input differential step of 50mV, i.e., VCM±25mV for the differential input signals. Report the comparator aperture time, by measuring the 10%-90% “rise-time” based on the simulation results. Please refer to [9] for the aperture time measurement.

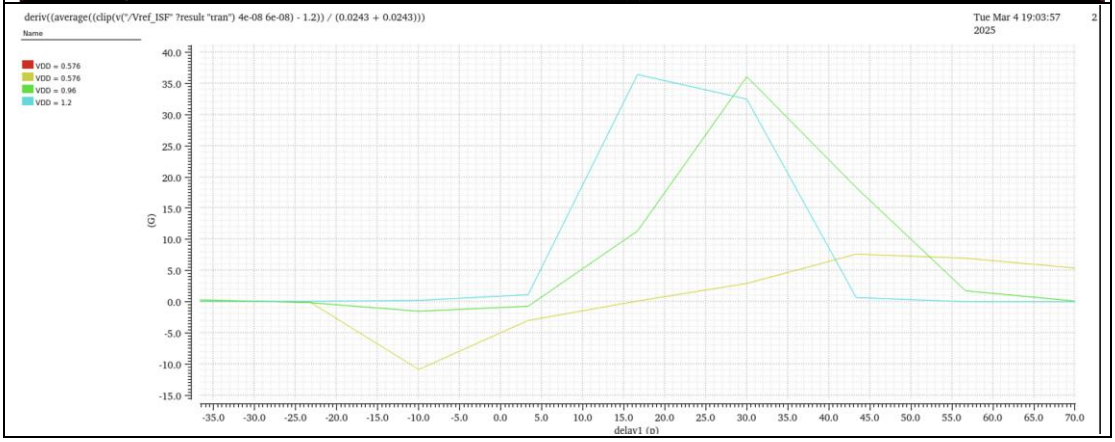
d. Compare the design of these four latches (you can refer to [2]).

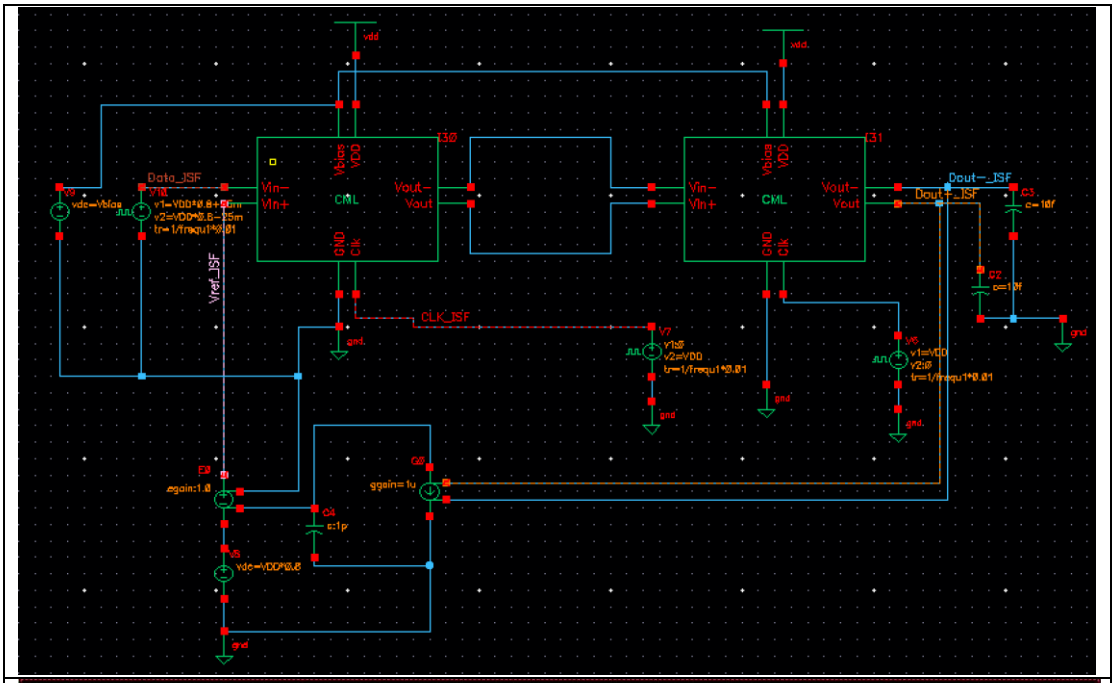


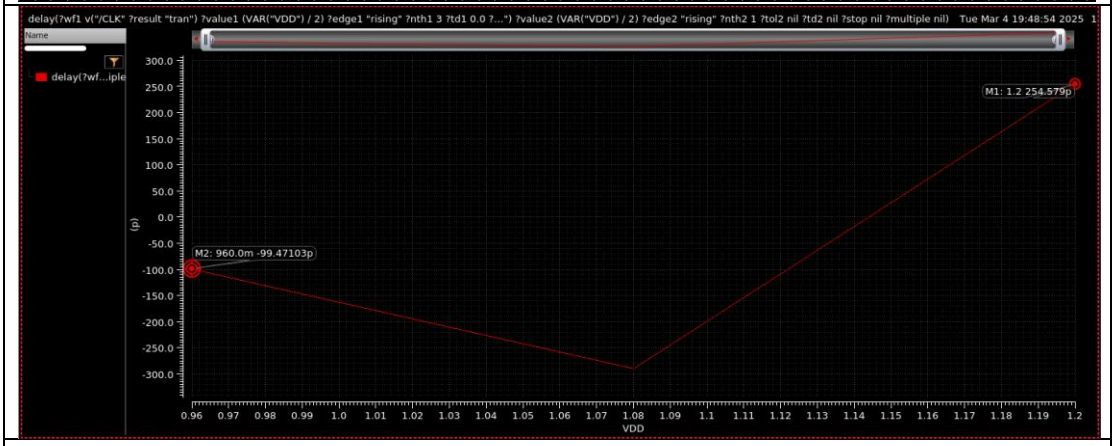


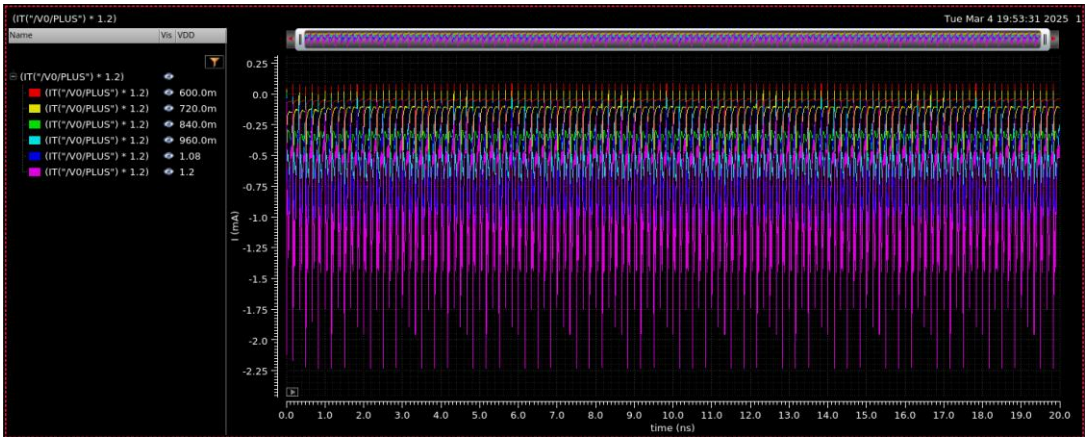

(IT("/I16/VDD") * 1.2)
Tue Mar 4 02:01:21 2025
Name
Vis
VDD
(IT("/I16/VDD") * 1.2)
(IT("/I16/VDD") * 1.2) 600.0m
(IT("/I16/VDD") * 1.2) 666.7m
(IT("/I16/VDD") * 1.2) 733.3m
(IT("/I16/VDD") * 1.2) 800.0m
(IT("/I16/VDD") * 1.2) 866.7m
(IT("/I16/VDD") * 1.2) 933.3m
(IT("/I16/VDD") * 1.2) 1.0
(IT("/I16/VDD") * 1.2) 1.067
(IT("/I16/VDD") * 1.2) 1.133
(IT("/I16/VDD") * 1.2) 1.2
I (mA)
time (ns)

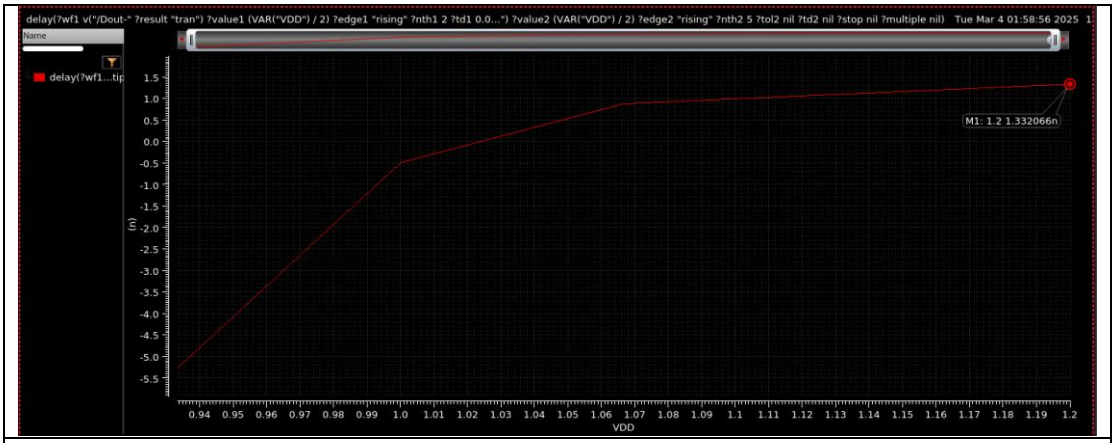

Transient Response
Tue Mar 4 16:57:41 2025
Name
/Clk_buffer_ISF
/Vref_ISF
/Data_ISF
/Dout+_ISF
V (V)
V (mV)
M1: 60.25728ns 980.1996mV
M2: 82.51706ns 982.1772mV
time (ns)

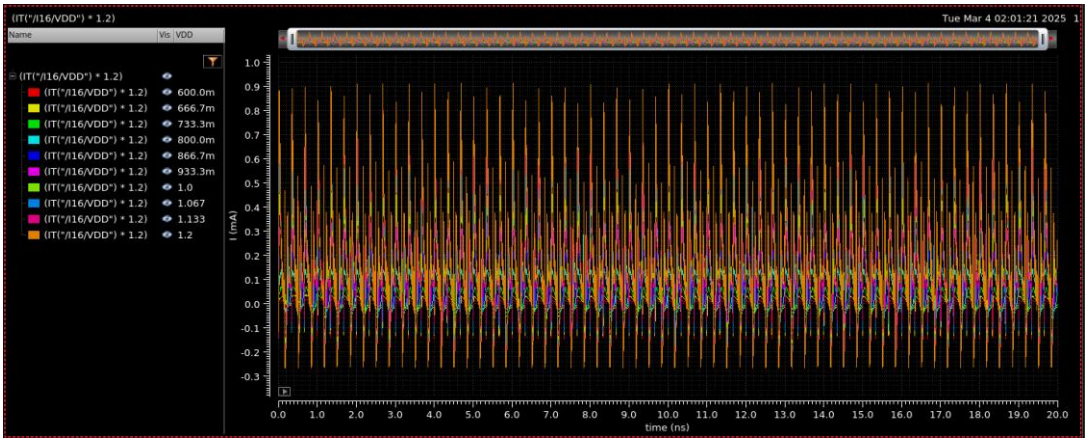

deriv((average((clip(v("/Vref_ISF" ?result "tran") 4e-08 6e-08) - 1.2)) / (0.0243 + 0.0243)))
Tue Mar 4 19:03:57 2025
Name
VDD = 0.576
VDD = 0.576
VDD = 0.96
VDD = 1.2
(G)
delay1 (p)

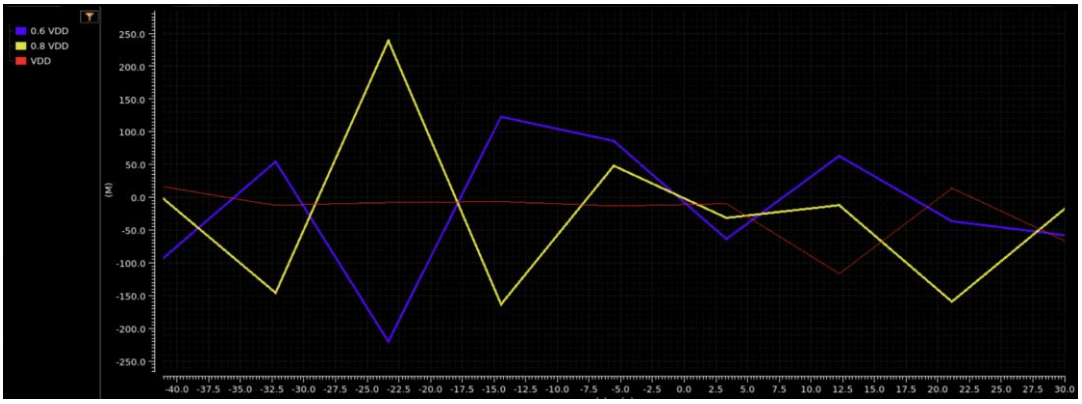

vdd
Data_JSF
Vref_JSF
CLK_JSF
Vin-
Vin+
CML
Vout-
Vout
Vbias
VDD
GND
Clk
Dout-_JSF
Dout+_JSF
C3
c=1df
C4
c=1p
gain=1u
gnd

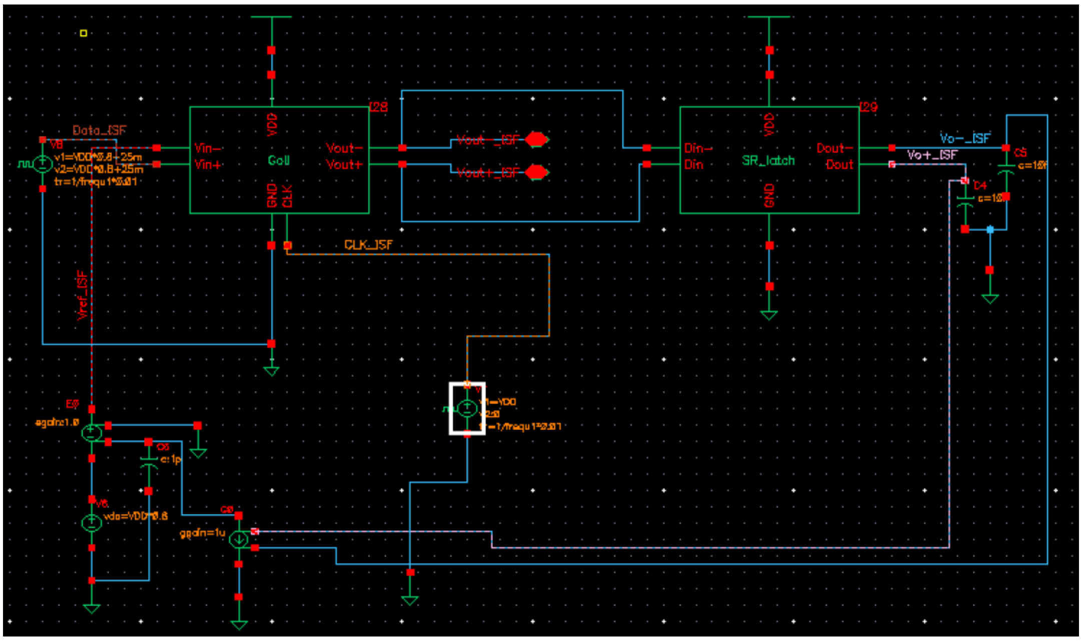

delay(?wf1 v("/CLK" ?result "tran") ?value1 (VAR("VDD") / 2) ?edge1 "rising" ?nth1 3 ?td1 0.0 ?...") ?value2 (VAR("VDD") / 2) ?edge2 "rising" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?multiple nil) Tue Mar 4 19:48:54 2025
M1: 1.2 254.579p
M2: 960.0m -99.47103p
(p)
VDD

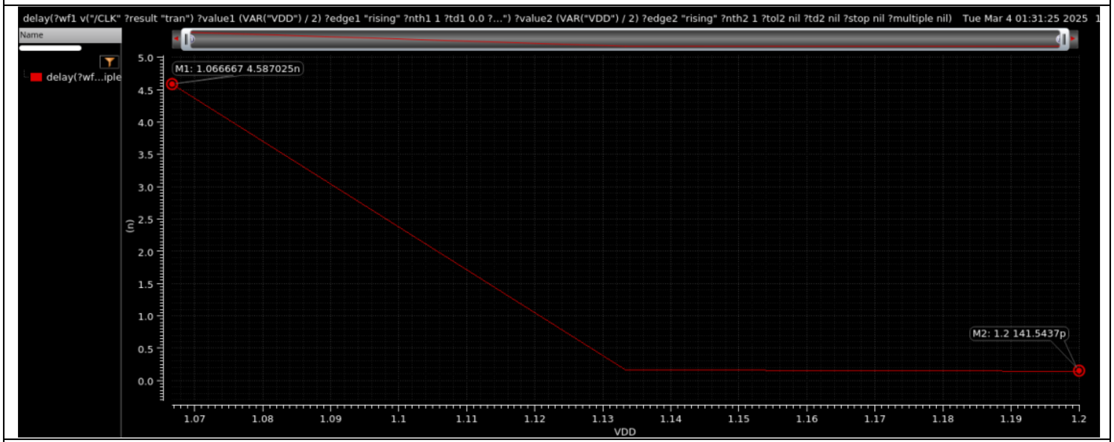

(IT("/V0/PLUS") * 1.2)
Tue Mar 4 19:53:31 2025
(IT("/V0/PLUS") * 1.2) 600.0m
(IT("/V0/PLUS") * 1.2) 720.0m
(IT("/V0/PLUS") * 1.2) 840.0m
(IT("/V0/PLUS") * 1.2) 960.0m
(IT("/V0/PLUS") * 1.2) 1.08
(IT("/V0/PLUS") * 1.2) 1.2
I (mA)
time (ns)

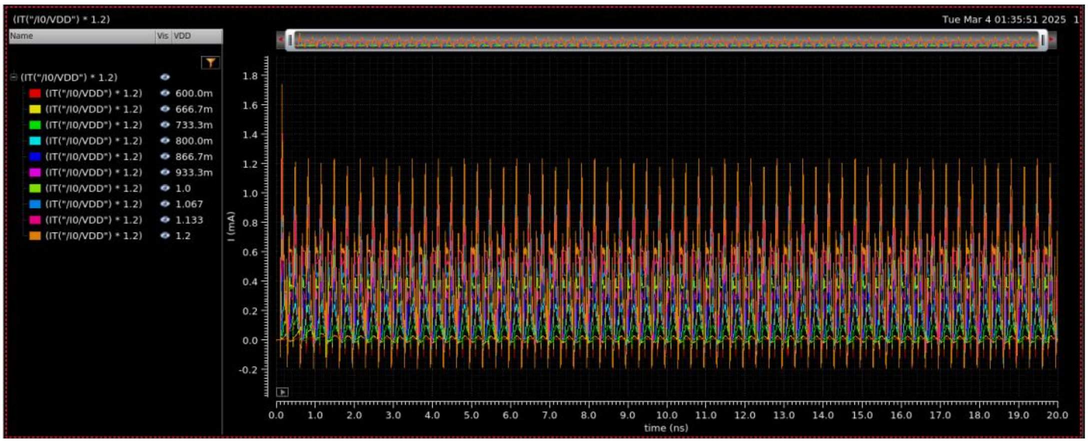

delay(?wf1 v("/Dout-" ?result "tran") ?value1 (VAR("VDD") / 2) ?edge1 "rising" ?nth1 2 ?td1 0.0...") ?value2 (VAR("VDD") / 2) ?edge2 "rising" ?nth2 5 ?tol2 nil ?td2 nil ?stop nil ?multiple nil) Tue Mar 4 01:58:56 2025
Name
delay(?wf1...tip
M1: 1.2 1.332066n
(n)
VDD

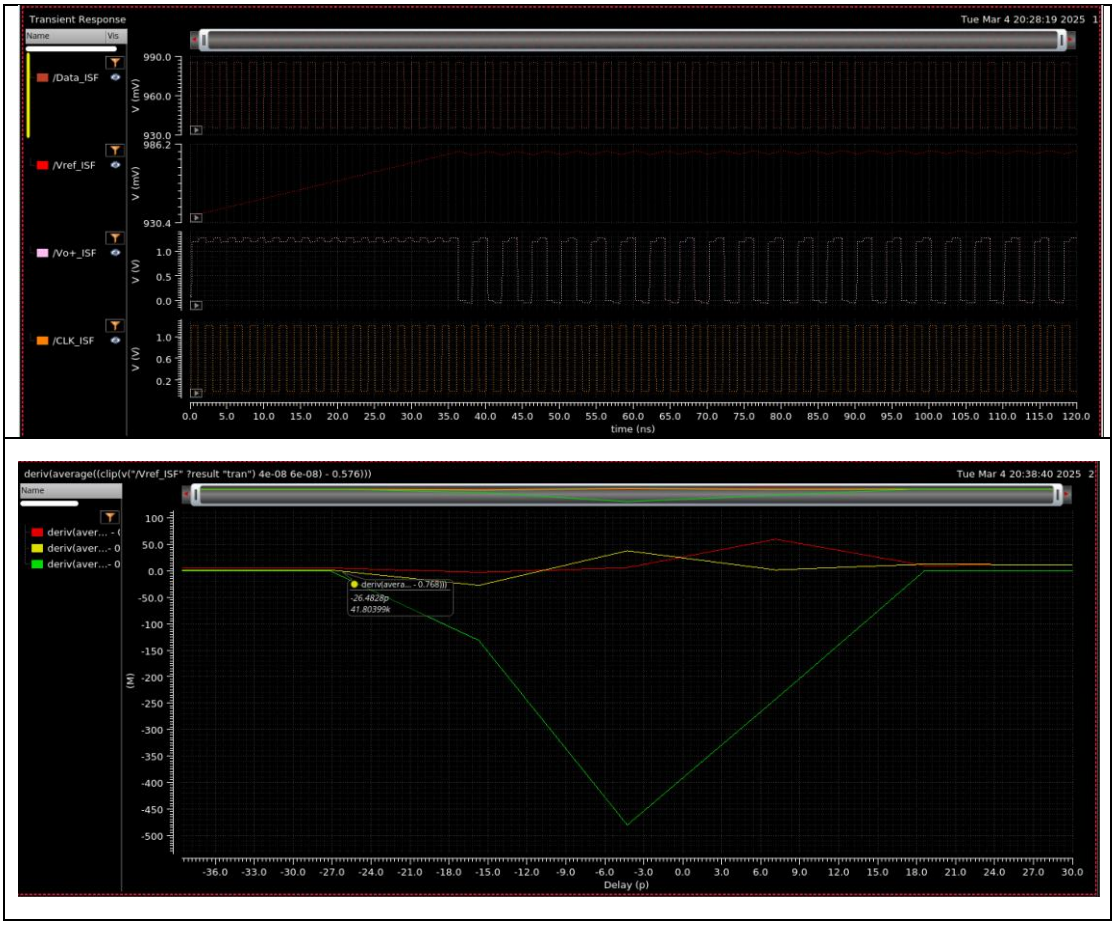

(IT("/I16/VDD") * 1.2)
Tue Mar 4 02:01:21 2025
Name
Vis
VDD
(IT("/I16/VDD") * 1.2)
(IT("/I16/VDD") * 1.2) 600.0m
(IT("/I16/VDD") * 1.2) 666.7m
(IT("/I16/VDD") * 1.2) 733.3m
(IT("/I16/VDD") * 1.2) 800.0m
(IT("/I16/VDD") * 1.2) 866.7m
(IT("/I16/VDD") * 1.2) 933.3m
(IT("/I16/VDD") * 1.2) 1.0
(IT("/I16/VDD") * 1.2) 1.067
(IT("/I16/VDD") * 1.2) 1.133
(IT("/I16/VDD") * 1.2) 1.2
I (mA)
time (ns)


0.6 VDD
0.8 VDD
VDD
(M)


Data_ISF
Vin−
Vin+
Vout−
Vout+
VDD
GND
CLK
I28
I29
Din−
Din
SR_latch
Dout−
Dout
Vo−_ISF
Vo+_ISF
CLK_ISF
Vref_ISF


delay(?wf1 v("/CLK" ?result "tran") ?value1 (VAR("VDD") / 2) ?edge1 "rising" ?nth1 1 ?td1 0.0 ?...") ?value2 (VAR("VDD") / 2) ?edge2 "rising" ?nth2 1 ?tol2 nil ?td2 nil ?stop nil ?multiple nil) Tue Mar 4 01:31:25 2025
M1: 1.066667 4.587025n
M2: 1.2 141.5437p
VDD


(IT("/I0/VDD") * 1.2)
Tue Mar 4 01:35:51 2025
600.0m
666.7m
733.3m
800.0m
866.7m
933.3m
1.0
1.067
1.133
1.2
I (mA)
time (ns)



(a) Strong-Arm	Classic design, no static power, simple structure	High speed, but better at higher supply voltages	Extremely low (no DC consumption)	Flash ADC, general high-speed comparators
(b) CML Latch	Current-mode switching, small output swing	Ultra-high speed (10–40+ Gb/s)	Has static current, relatively high power	High-speed SerDes, backplane links, ultra-high-speed I/O
(c) Schinkel Low-Voltage	Modified Strong-Arm, fewer stacked transistors, suited for low voltage	Relatively fast, outperforms standard SA at the same supply voltage	No static current, moderate power	Low-voltage high-speed applications (UDSM CMOS)
(d) Goll Low-Voltage	Extends SA design by	High (0.6–5 GHz)	No static current	High-speed, low-voltage

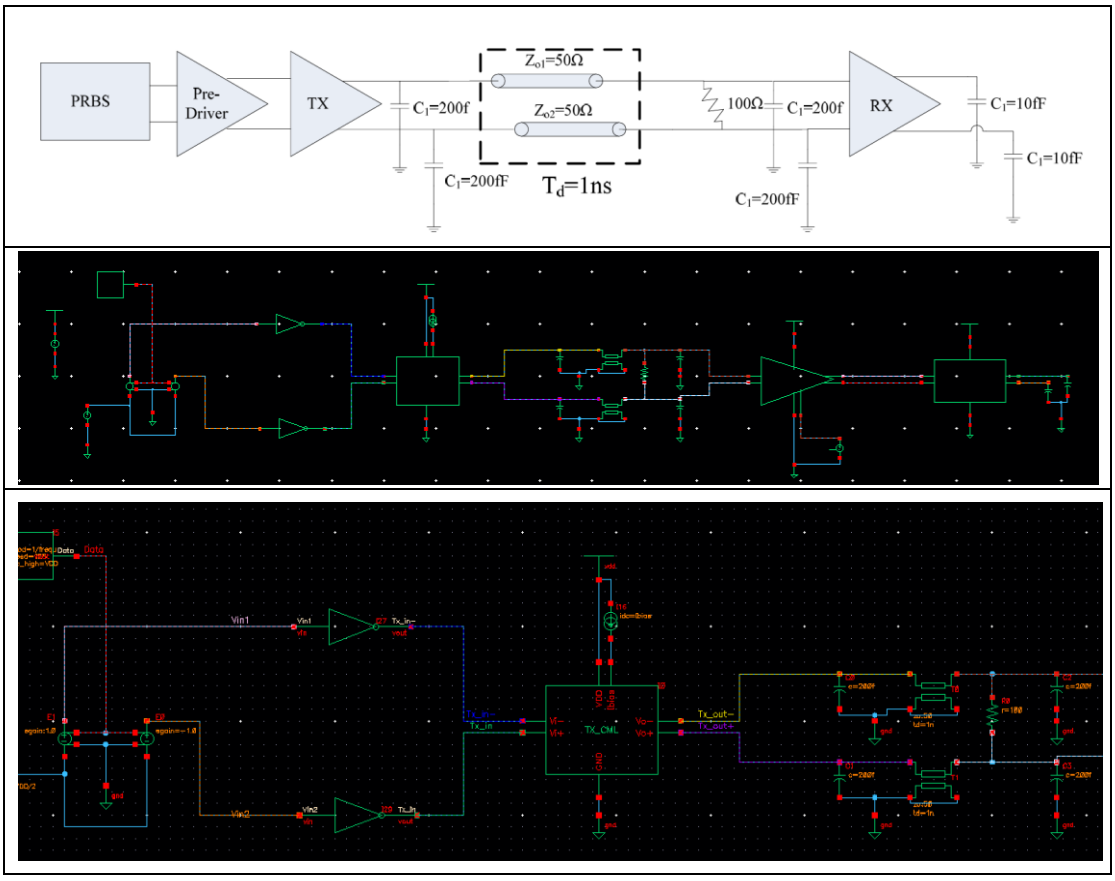
	adding P4/P5 for feedback acceleration			comparators in UDSM CMOS

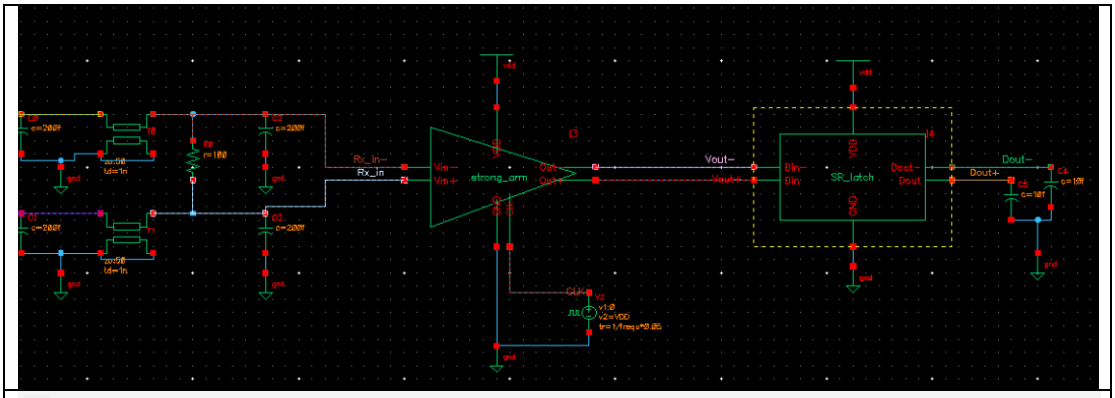
3. Link Verification. The designed comparator can be considered as a basic receiver. Build a 6Gb/s link system by using the transmitter designed either in voltage mode or current mode and the comparator which you've chosen for the best performance. Please refer to Figure 12 for the full test circuit. Use 50Ω transmission line with 1ns delay. Add 200fF parasitic caps at the output of your transmitter and input of the receiver. Feel free to choose the best termination and coupling schemes.

a. Show the circuit schematic including coupling and termination.

b. Explain your choice of coupling and termination schemes.

c. Please show simulation results and eye diagrams that verify the link functionality and performance.





ADE L (1) - lab4 Link_test schematic@n03-poseidon.olympus.ece.tamu.edu

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help cadence

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Design Variables

	Name	Value
1	VDD	1.2
2	Ibias	6m
3	frequ	6G
4	W_TX	72u
5	invW	2u
6	W1	16u
7	W2	2u
8	W3	3u
9	W4	8u
10	W5	8u
11	WNL	2u
12	WPL	4u
13	WNs	100n
14	WPs	200n

Analyses

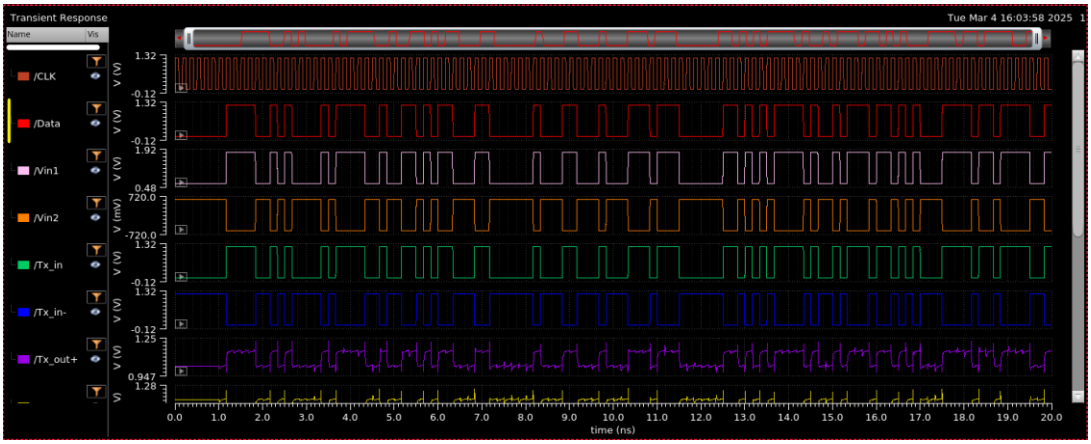
	Type	Enable	Arguments
1	tran	☑	0 20n

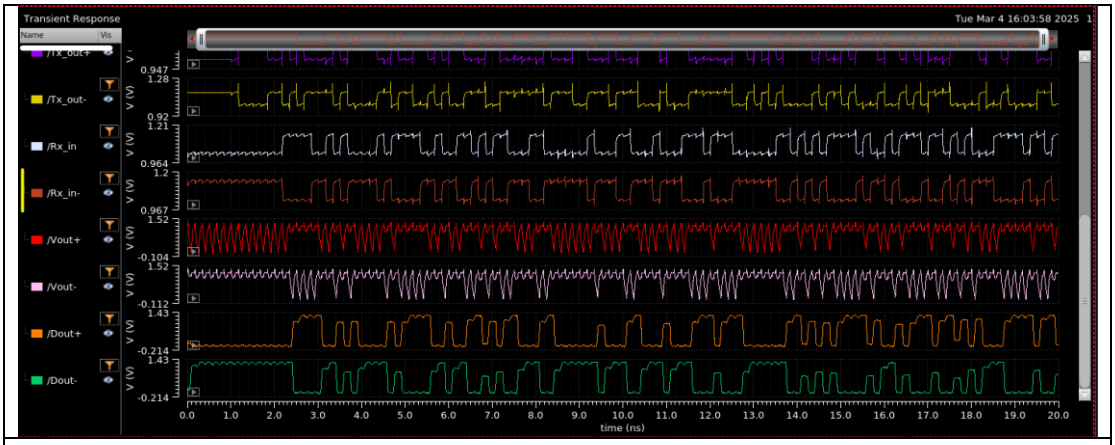
Outputs

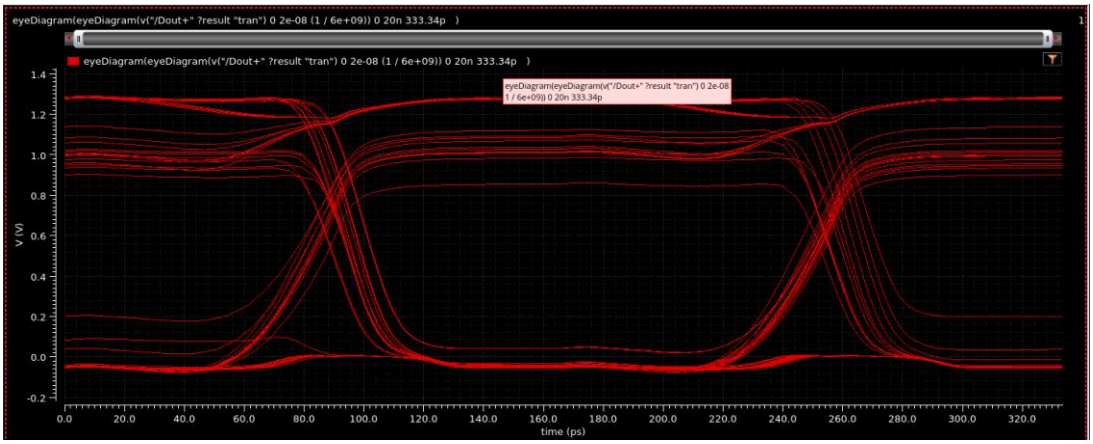
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	CLK		☑	☑	allv
2	Data		☑	☑	allv
3	Vin1		☑	☑	allv
4	Vin2		☑	☑	allv
5	Tx_in		☑	☑	allv
6	Tx_in-		☑	☑	allv
7	Tx_out+		☑	☑	allv
8	Tx_out-		☑	☑	allv
9	Rx_in		☑	☑	allv

Plot after simulation: Auto Plotting mode: Replace

> Results in ...ison900531/cadence/simulation/L




Transient Response
Tue Mar 4 16:03:58 2025
/Tx_out+
/Tx_out-
/Rx_in
/Rx_in-
/Vout+
/Vout-
/Dout+
/Dout-
V (V)
time (ns)


eyeDiagram(eyeDiagram(v("/Dout+" ?result "tran") 0 2e-08 (1 / 6e+09)) 0 20n 333.34p)
V (V)
time (ps)