25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

Lab2: Channel Models

Name: Yu-Hao Chen

UIN:435009528

Section:700

Professor: Sam Palermo

TA: Srujan Kumar Kaile

Description:

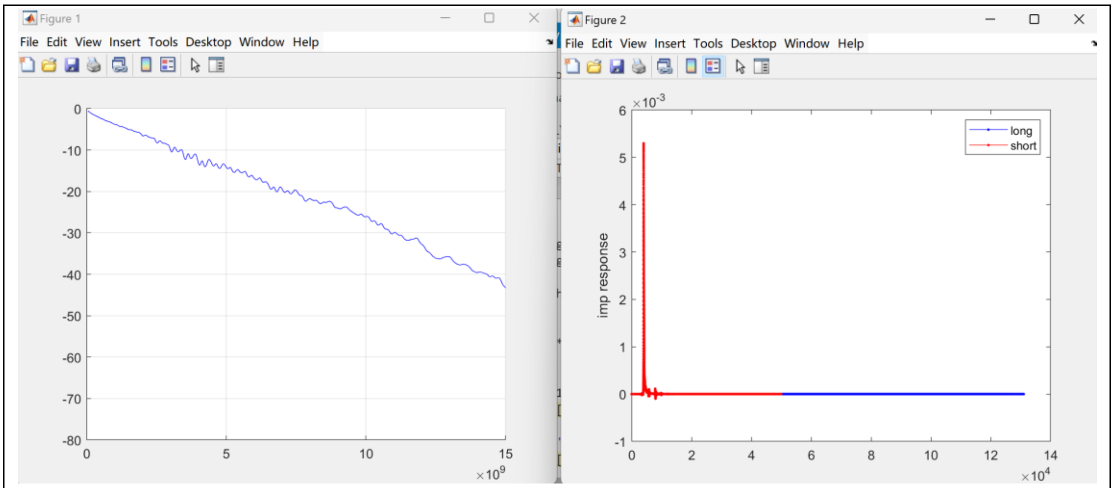
This lab explores S-parameter modeling of transmission lines, vias, and connectors, analyzing ISI, peak distortion, modulation schemes, and termination design. Channel impulse responses are derived via inverse Fourier transform, enabling eye diagram generation through MATLAB and Cadence simulations.

Design & results

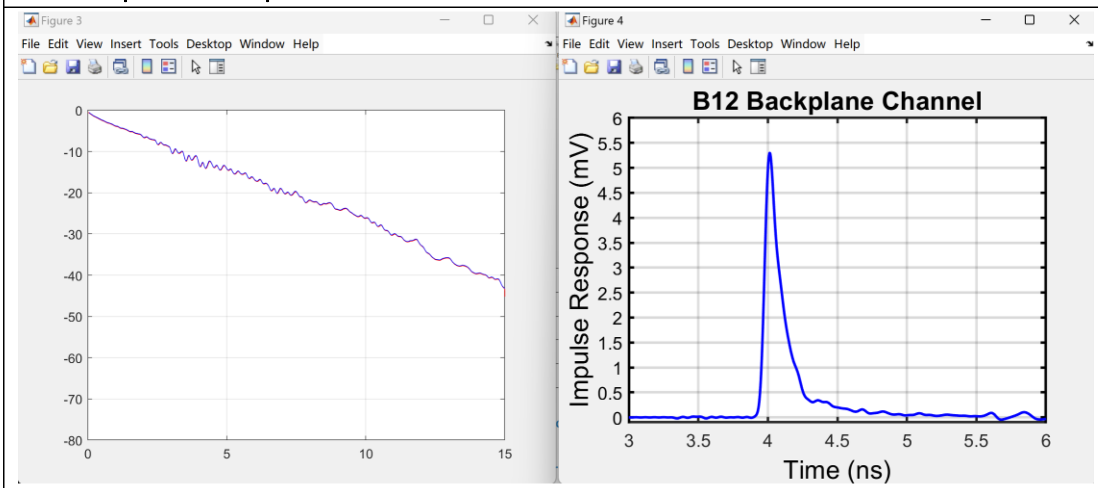
1. Channel Transient Simulation. The objective of this problem is to use measured channel S-parameters data to produce an impulse response and perform a transient simulation in MATLAB involving sending random NRZ data across this channel.

a. Download the S-parameters file for a 12” Backplane channel, “peters_01_0605_B12_thru.s4p”

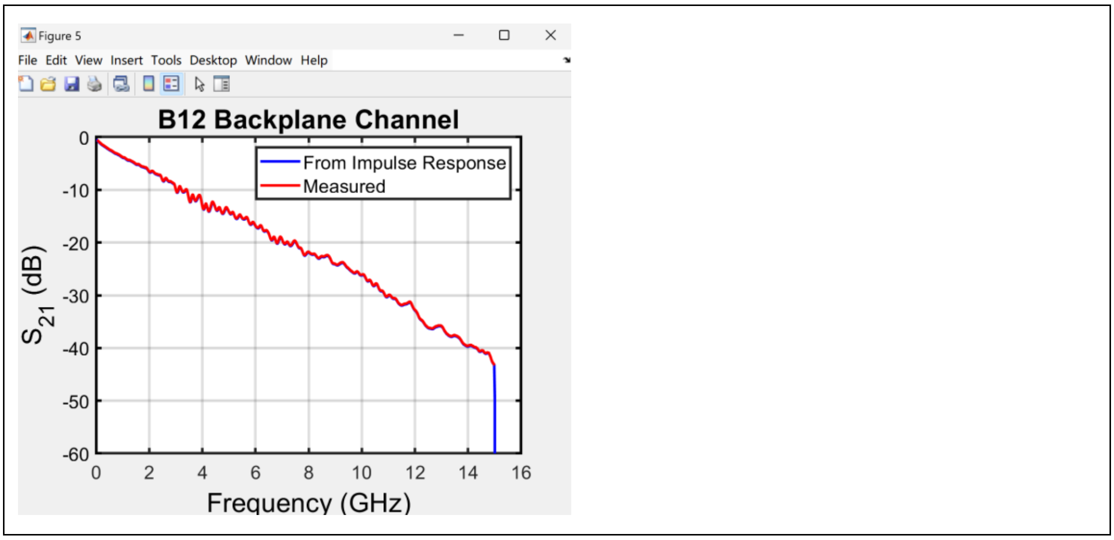
b. Use the MATLAB file “read_sparam.m” to produce an impulse response. Note this code requires the function “xfr_fn_to_imp.m”.



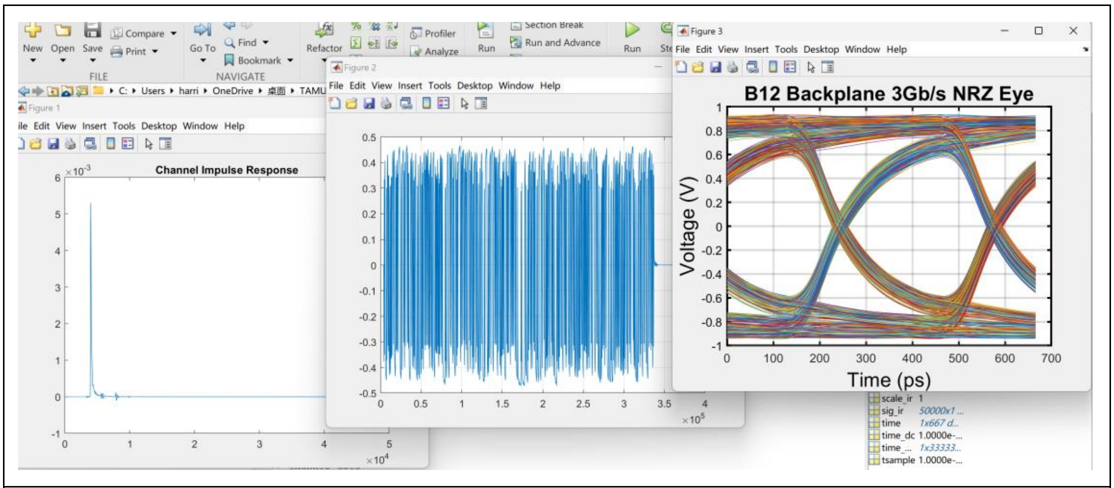
- Frequency Response
- Impulse Response

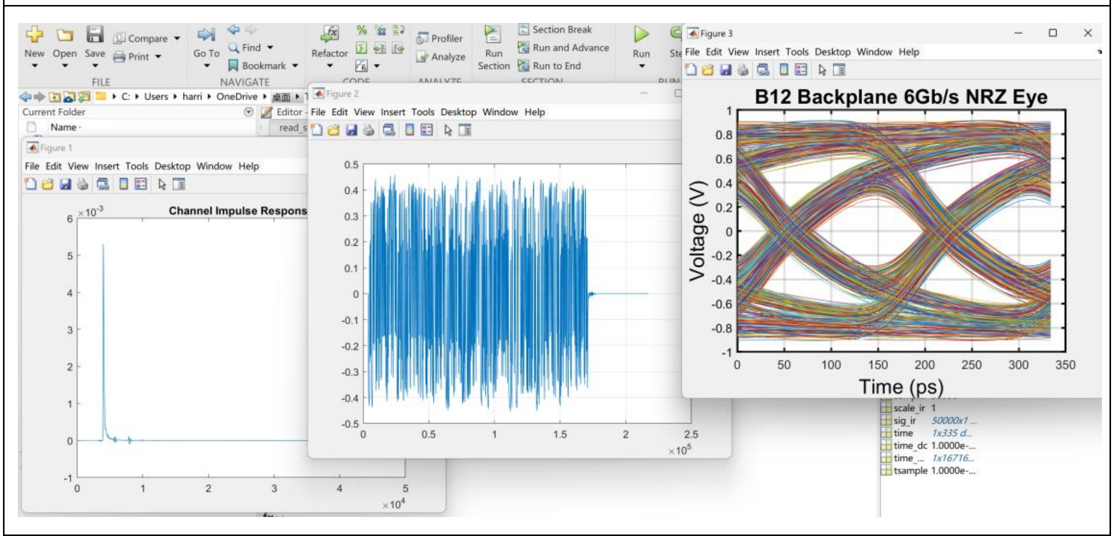


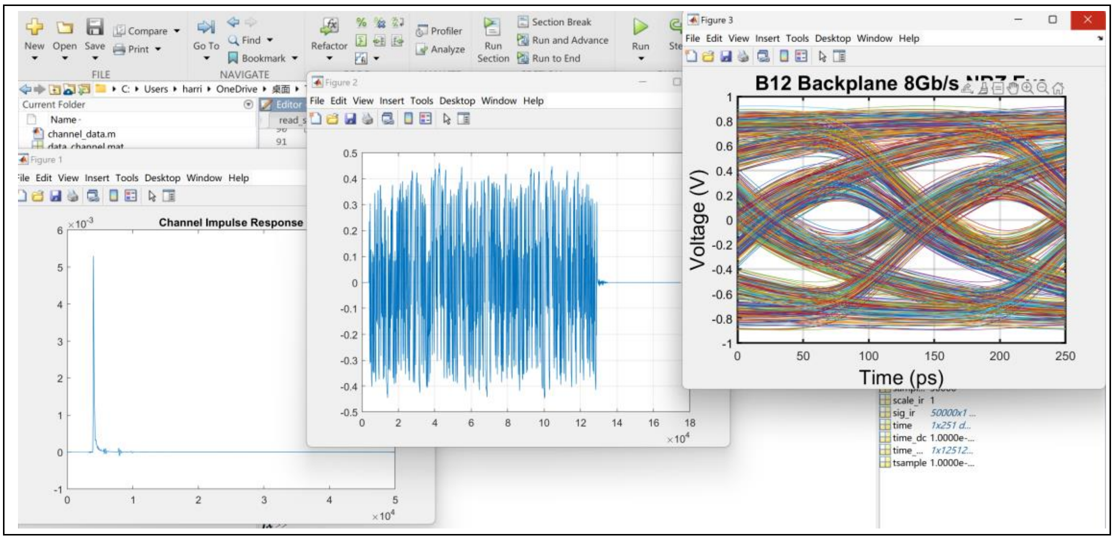
- Frequency Response (filter)
- Impulse Response



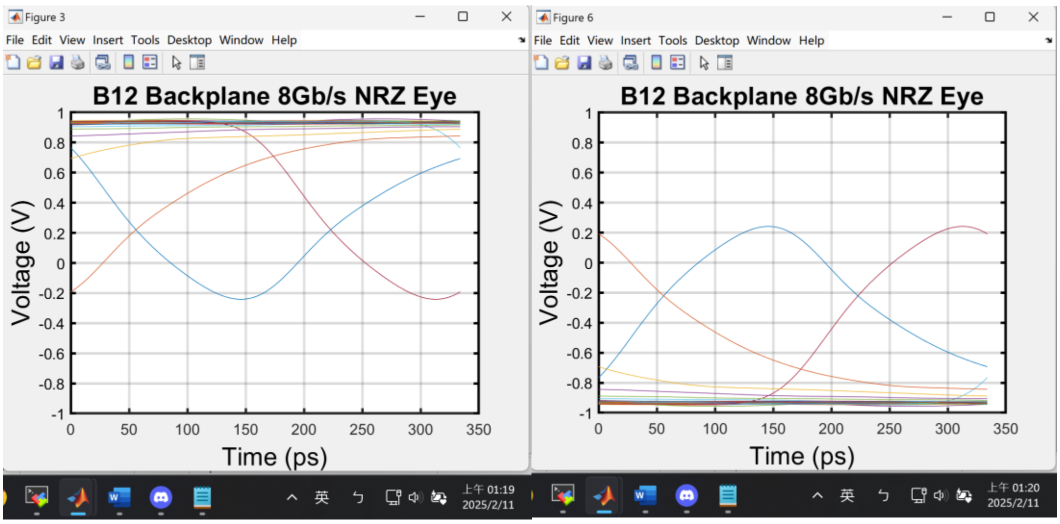
c. Use the produced impulse response to perform transient simulations. Plot eye diagrams with 10k random bits at 3, 6, and 8Gbps. Example code for this is the file "channel_data.m".







d. Using peak distortion analysis generate the worst case bit pattern and plot the worst case eye at 6 and 8Gbps. In generating the worst case bit pattern, truncate the pulse response such that there are 10 pre-cursor samples and 100 post-cursor samples.



Worst case 0 & worst-case 1

2. Use measured channel S-parameters data to produce a pulse response and perform a transient simulation in Cadence. Use a 12" Backplane channel, "peters_01_0605_B12_thru.s4p" and transfer the file to ECEN720 directory where you run Cadences. Perform a pulse response simulation using an ideal 1V pulse (differential) with 1ps rise/fall time and 125ps pulse width (for 8Gbps). The channel needs to be terminated at both input and output. The pulse response can be obtained by measuring Vout. The circuit setup is shown in Figure 11. Refer to the Appendix on how to use channel model in Cadence.

a. Show your schematic and simulation results.

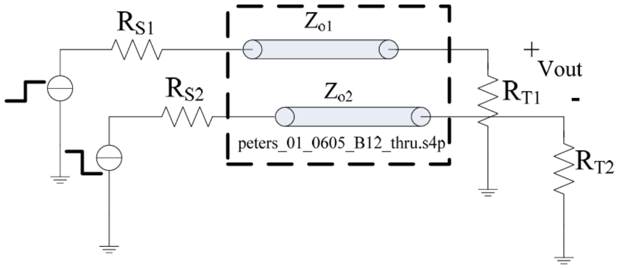
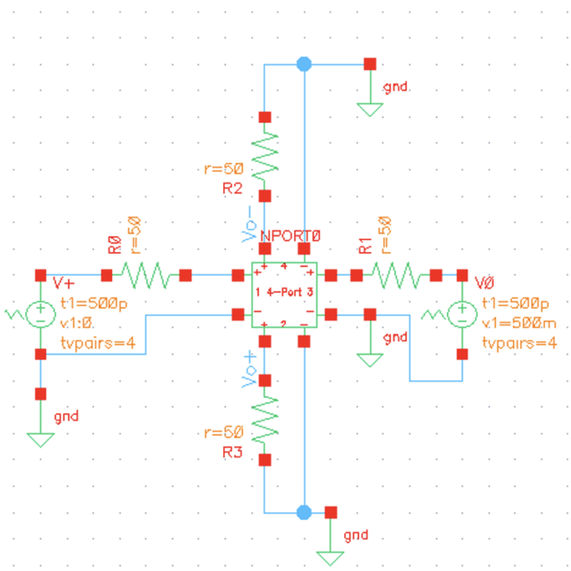
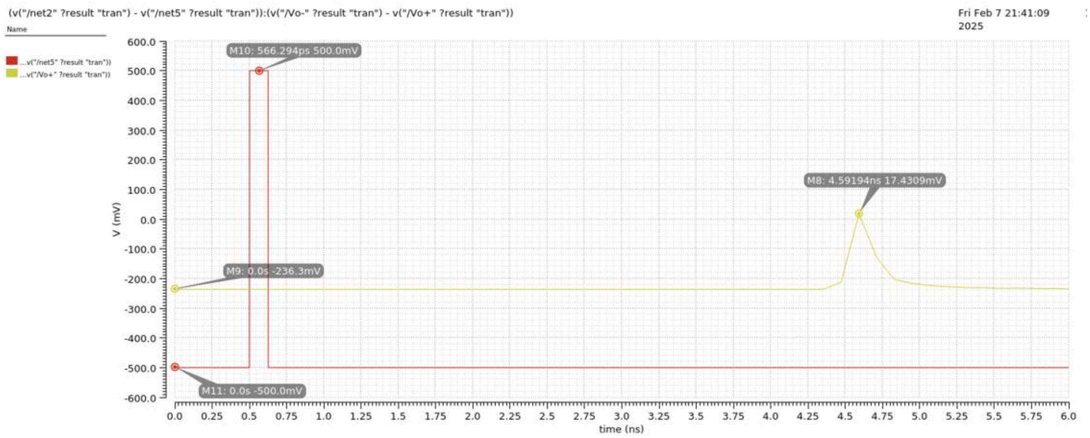
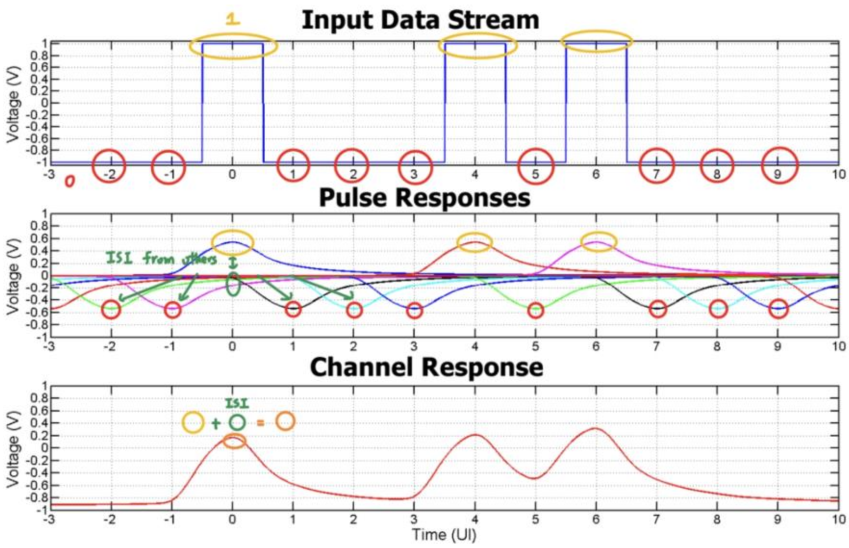


Figure 11 Circuit Setup for Impulse Response



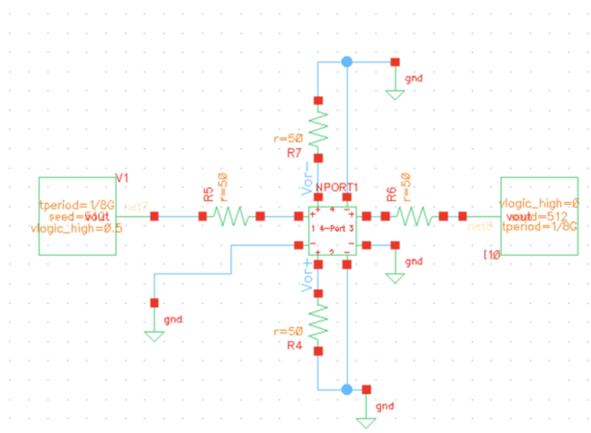


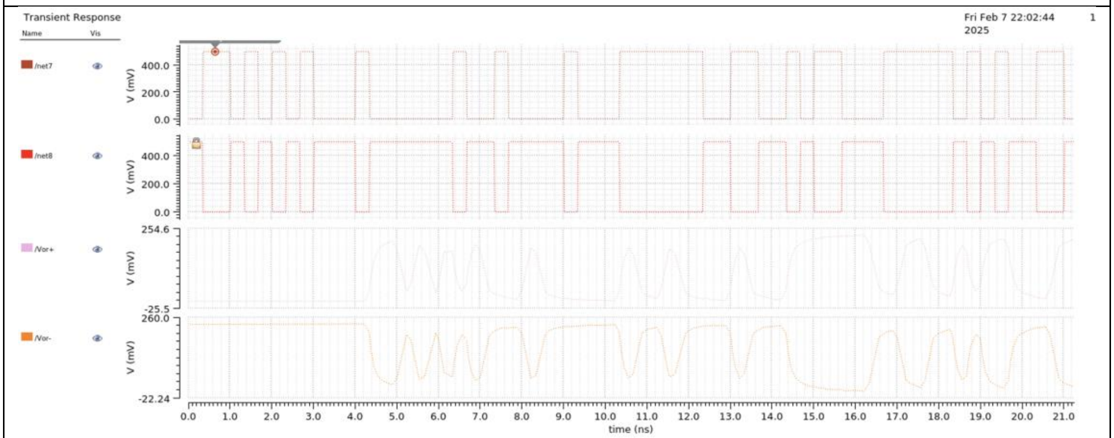
- Pulse response distortion can caused by reflections, channel resonances and channel loss (dispersion)



By analyzing the input data and pulse response, we can predict the output result, which determines how easily the input data can be recovered from the output.

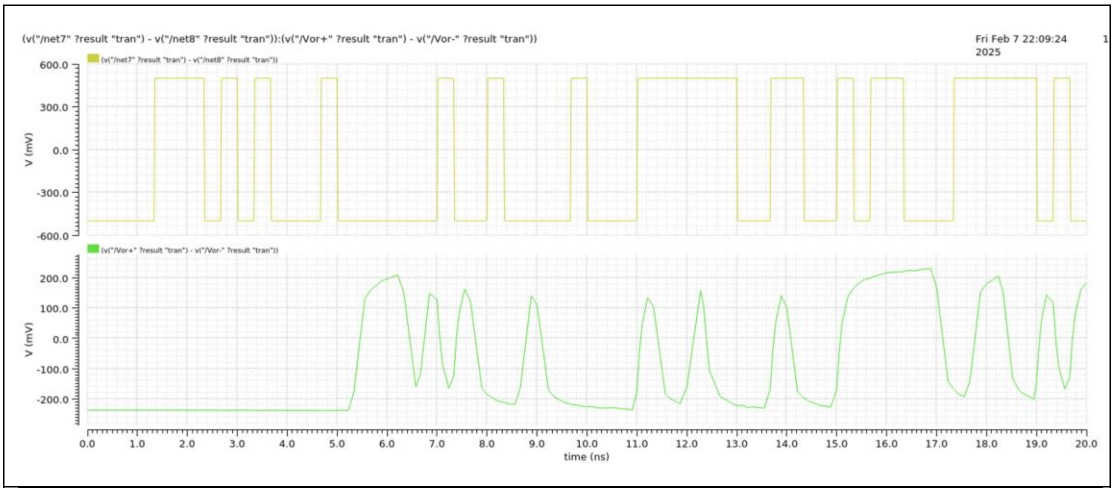
b. Perform transient simulation using a PRBS input pattern at 3Gbps, 6Gbps, and 8Gbps. Refer to the Appendix for PRBS generation in Cadence.

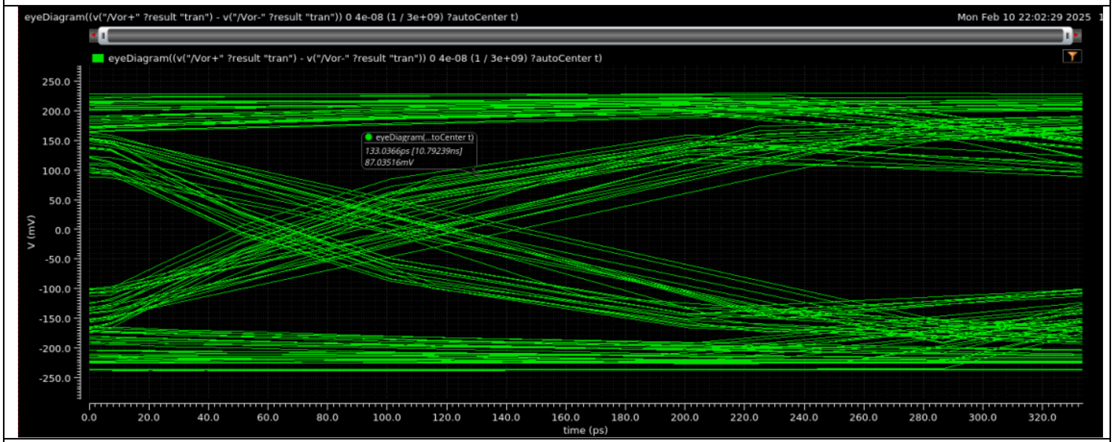




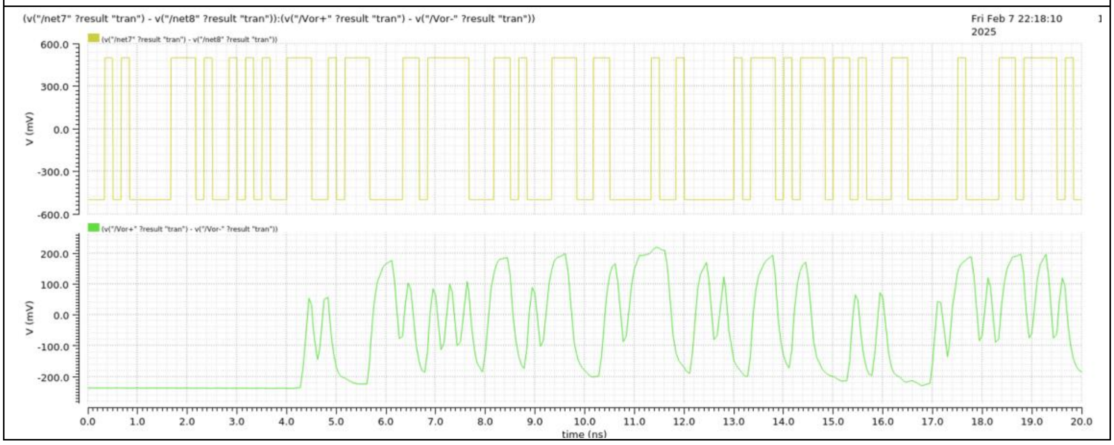
c. Plot eye diagrams at these data rates using Cadence's calculator. Refer to the Appendix on how to plot an eye diagram.

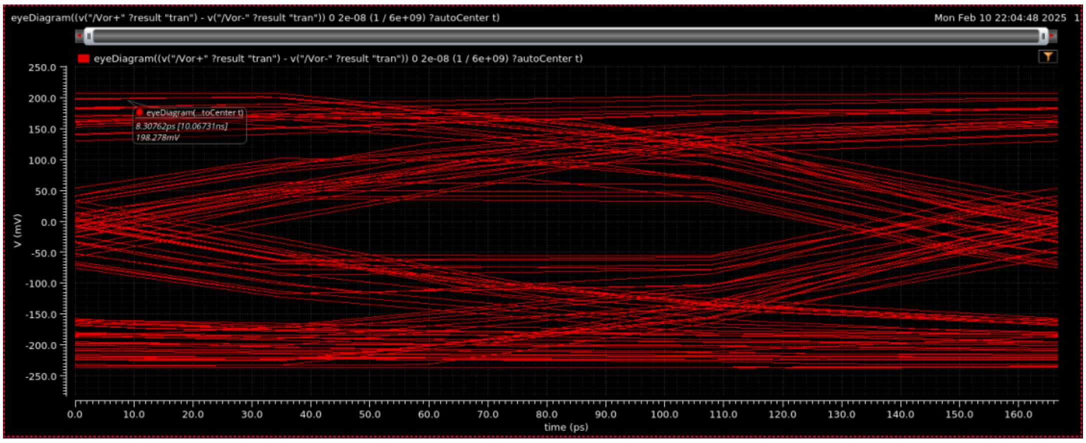
input pattern at 3Gbps



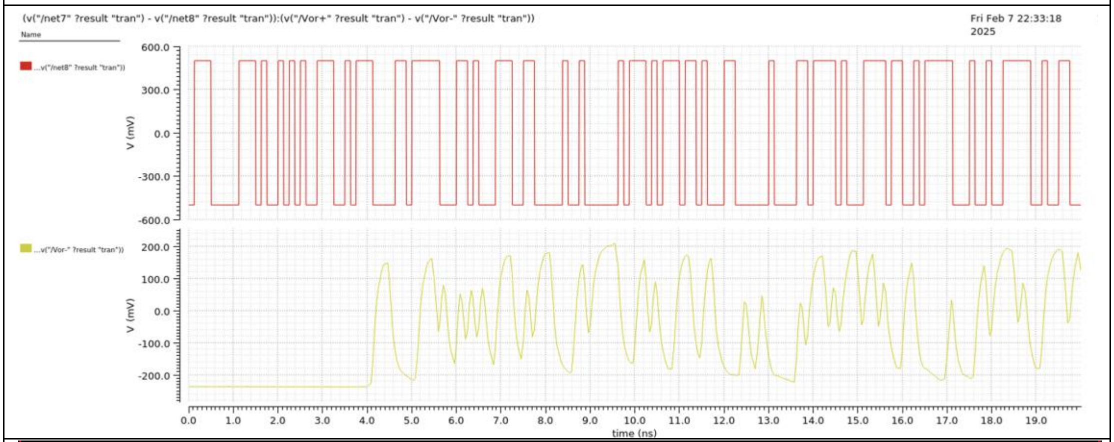


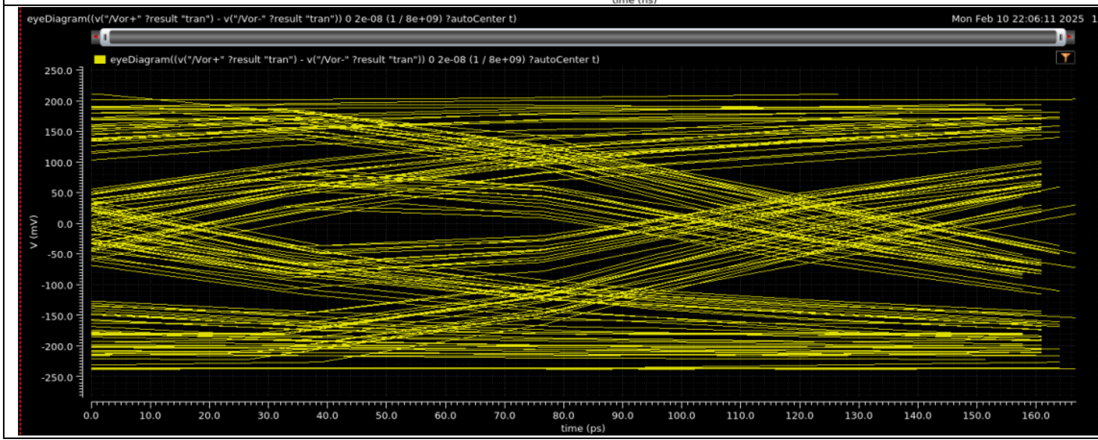
input pattern at 6Gbps





input pattern at 8Gbps





- The amount of the margin can be used to calculate the receiver's sensitivity requirement. The timing margin is often used to estimate a digital system timing budget or the receiver's aperture time.
- Inter-symbol interference (ISI) is a form of a signal distortion which is caused by reflections, channel resonances and channel loss (dispersion). It is the **interference between symbols** where the current bit (symbol) could distort its subsequent and previous bits (symbol).
- The higher input pattern rate means more bits (data) in the same period, which means the interference between symbols can be more drastically (under the

same channel impulse response)

3. Peak Distortion Analysis. For the 1-bit pulse response shown in Figure 13, find the worst-case input bit pattern, assuming the ISI is ZERO for samples outside the plot range. Also, find the worst-case eye height.

Pulse Response	
Time (UI)	Sample (V)
-3	0.02
-2	-0.03
-1	0.03
0	0.33
1	0.25
2	0.15
3	0.06
4	0
5	-0.05
6	0.03
7	-0.02
8	0.02
9	0.01

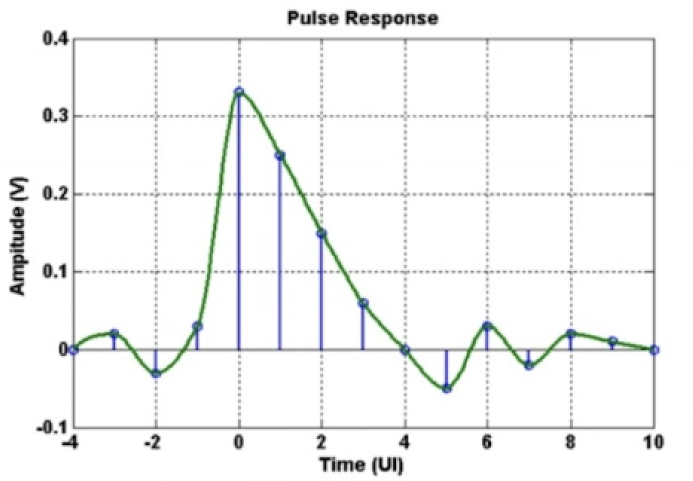


Figure 12 Pulse Response for Peak Distortion Analysis

---

			cursor										
	-3	-2	-1	0	1	2	3	4	5	6	7	8	9
	0.02	-0.03	0.03	0.33	0.25	0.15	0.06	0	-0.05	0.03	-0.02	0.02	0.01
	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3
	0.01	0.02	-0.02	0.03	-0.05	0	0.06	0.15	0.25	0.33	0.03	-0.03	0.02
worst 1	0	0	1	0	1	0	0	0	0	1	0	1	0
worst 0	1	1	0	1	0	0	1	1	1	0	1	0	1

$$S(t) = 2\left\{ y_0^{1}(t) + \sum_{k=-4}^{10} y^{(t)}(t-kT)\Big|_{y(t-kT)<0} - \sum_{k=-4}^{10} y^{(t)}(t-kT)\Big|_{y(t-kT)>0} \right\}$$

$y(t-kT) < 0 = -0.1$

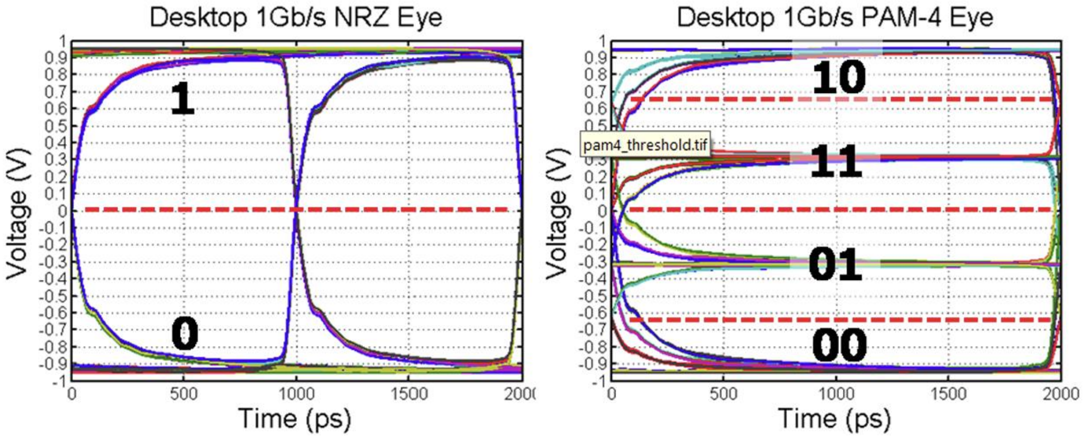
$y(t-kT) > 0 = 0.57$

worst case $2(0.33 - 0.1 - 0.57)$

4. Modulation Schemes. NRZ is the most commonly used modulation format. PAM-4

transmits 2 bits/symbol at half the speed.

a. Explain the difference between the NRZ and PAM4 schemes.



NRZ (Non-Return-to-Zero)

- **Binary signaling (2 levels, "0" and "1")**.
- Each symbol represents **1 bit**, meaning the baud rate (symbol rate) is equal to the data rate.
- **Higher voltage margin** between the two levels.
- **Simpler receiver design** with only one decision threshold.
- **More resilient to noise and channel loss** due to its larger signal amplitude.

PAM-4 (Pulse Amplitude Modulation-4)

- **4-level signaling ("00", "01", "11", "10")**.
- Each symbol represents **2 bits**, meaning the baud rate is **half the data rate**.
- Reduces required bandwidth but introduces **smaller voltage margins** between signal levels.
- More **susceptible to noise and distortion** due to closer voltage levels.
- Requires **more complex equalization and receiver circuits**.

Key Trade-off:

- **NRZ requires twice the bandwidth of PAM-4** but has **better signal integrity**.
- **PAM-4 transmits more data per symbol**, reducing bandwidth needs, but suffers from increased **ISI (Inter-Symbol Interference), noise sensitivity, and reduced voltage margin**.

b. Assuming the channel loss at 2.5GHz is 7dB and at 5GHz is 14dB, which modulation scheme (NRZ or PAM-4) would have better voltage margin?

- NRZ would have a better voltage margin despite higher channel loss because it has fewer signal levels and a larger separation between them.
- PAM-4 benefits from lower bandwidth requirements but struggles with ISI and noise sensitivity.)

5. Termination Circuit. 10 a. Briefly list the pros and cons of these termination schemes:

(a) Off-chip vs. on chip, (b) series vs. parallel, and (c) DC vs. AC coupling.

	Pro	Con
Off-chip Termination	Can handle higher power dissipation	Increases parasitics and trace inductance
	More accurate resistor values	Slower response due to board-level interconnects
On-chip Termination	Better high-speed signal integrity	
	Lower parasitics and reflections	
Series Termination	Reduces signal overshoot and ringing	Causes signal delay and affects rise time
	Lower power consumption (no continuous current flow)	suited for point-to-point transmission, not multi-drop systems
Parallel Termination	Provides strong signal damping (reduces reflections)	Higher power dissipation (continuous current draw)
	Works well in multi-drop bus systems	Requires precise matching of termination resistor
DC Coupling	Works well for low-frequency and DC-balanced signals	Cannot block DC offset between transmitter and receiver
	Simpler design	Potential issues with common-mode voltage mismatches
AC Coupling	Blocks DC offset, allowing different voltage levels between transmitter and receiver	Requires AC-coupling capacitors, which introduce high-pass filtering (can distort low-frequency content)

b. Design three 50Ω active terminations and characterize the resistance of these three active termination schemes as shown in Figure 9. For configurations in Figures 10(a) and (b) use once only PMOS and then only NMOS transistors. Sweep the input voltage from GND to VDD and show the resistance curves vs. input voltage. If 90nm CMOS process is used, the nominal supply voltage is 1.2V (use the nominal VDD for any other CMOS process you use as well).

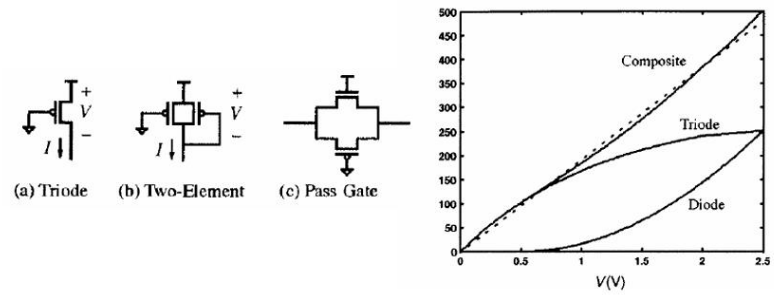
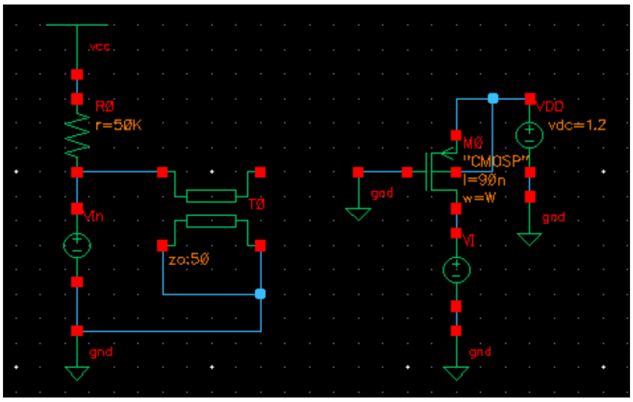
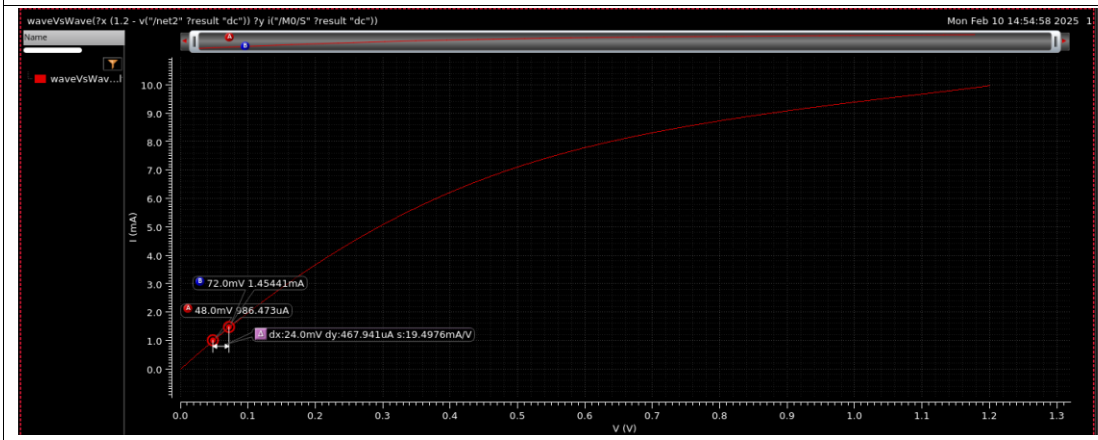
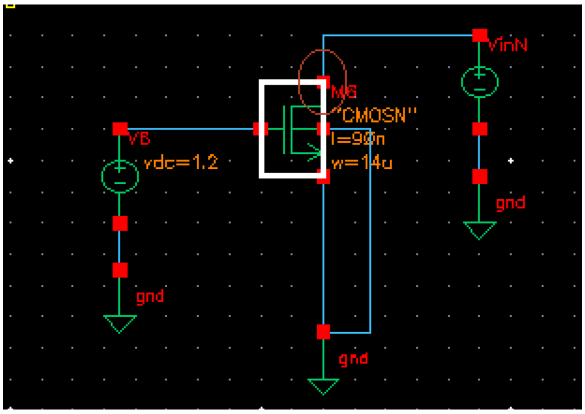
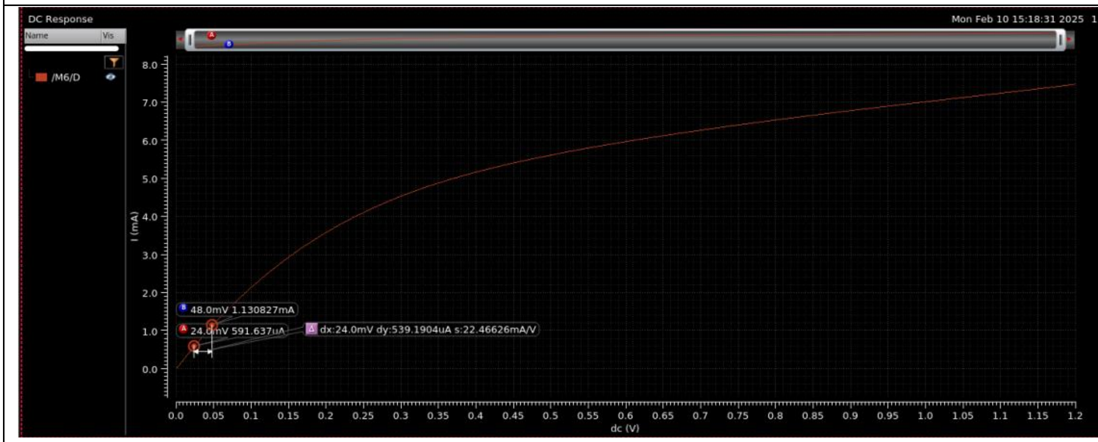


Figure 9 Active Termination Schemes [Dally]

Triode

Represent at the right figure for the 50k active termination The actual use is equal to left figure
 Yaxis-Id vs Xaxis-VDD-Vin=VSD 1/slope= I/V= 1/R

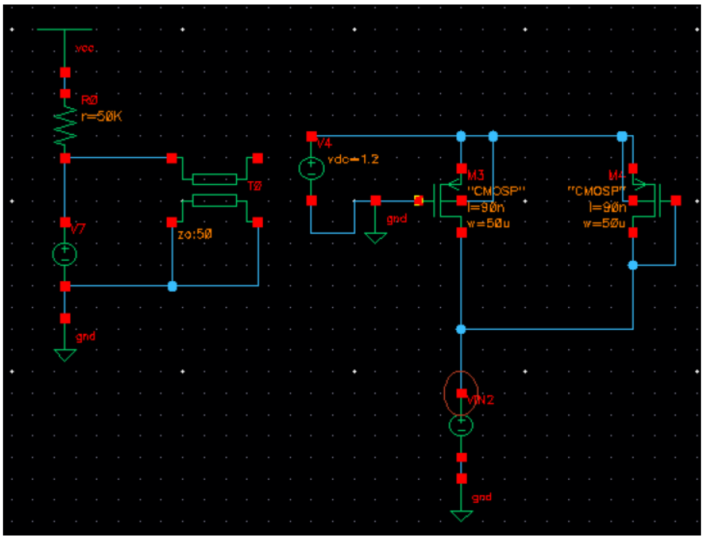


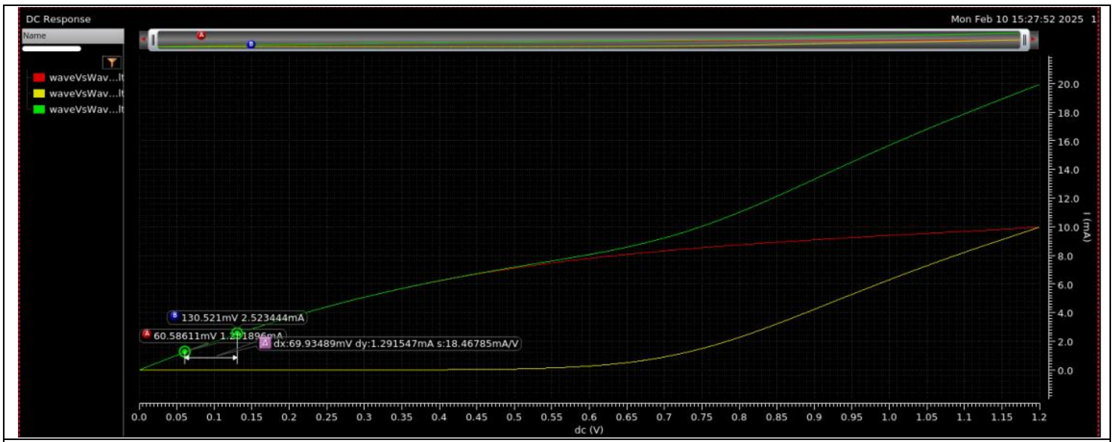


Yaxis-Id vs Xaxis-VDS=Vin

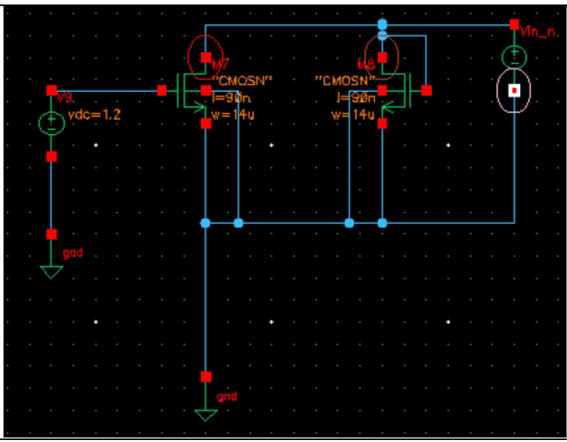
1/slope= I/V= 1/R

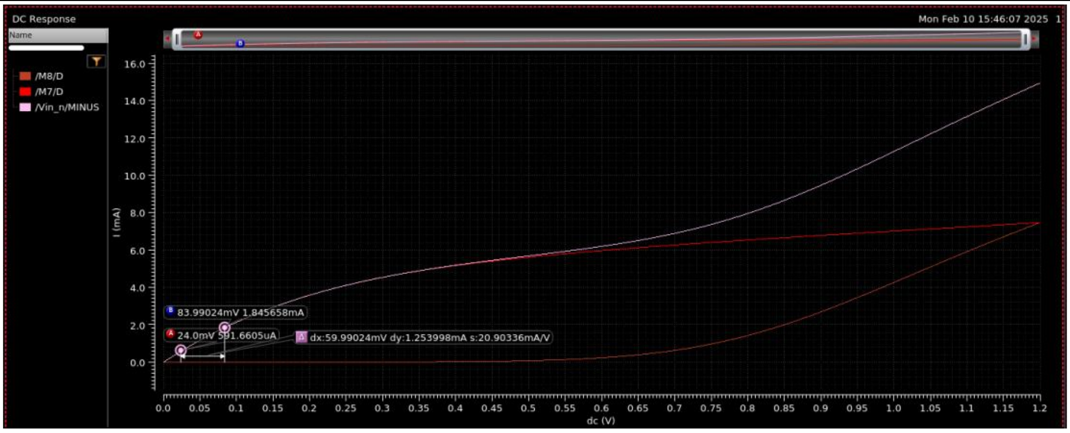
Two-element



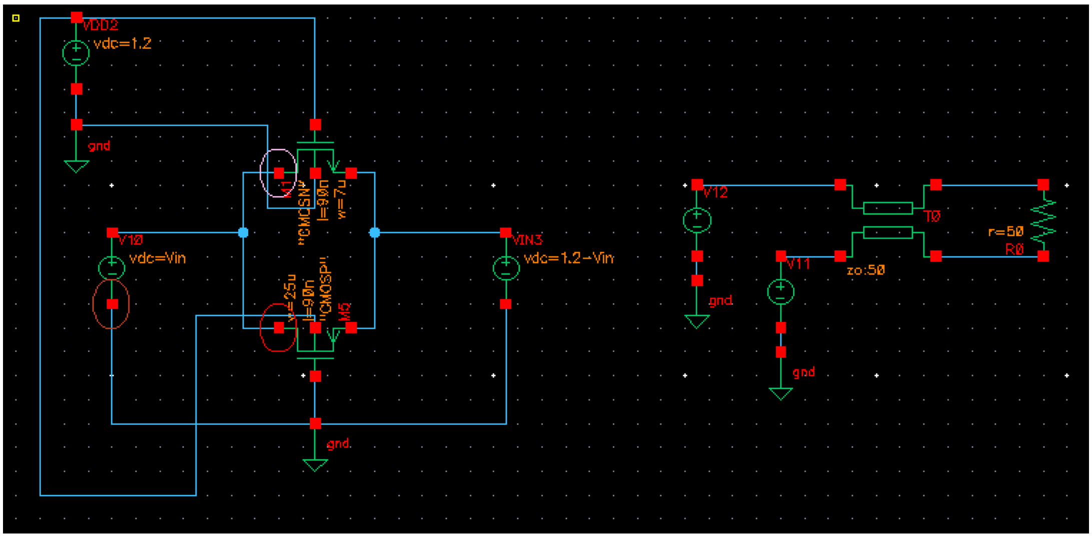


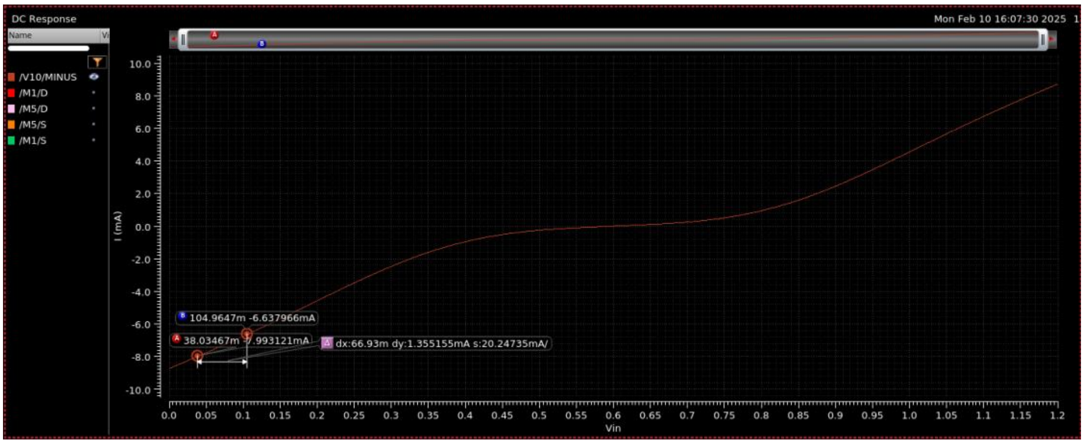
- Y-axis Id vs X-axis Vdd-Vin (VSD)
- Red line by M3 (saturate in the end 1.2-VS=Vin > Vov)
- Yellow line by M4 (diode connect)





PASSGATE


VDD2
vdc=1.2
gnd
V10
vdc=Vin
"CMOSN"
l=90n
w=7u
w=25u
l=90n
"CMOSP"
M5
VIN3
vdc=1.2-Vin
gnd
V12
gnd
T0
zo:50
r=50
R0
V11
gnd


DC Response
Mon Feb 10 16:07:30 2025
Name
/V10/MINUS
/M1/D
/M5/D
/M5/S
/M1/S
I (mA)
Vin
104.9647m -6.637966mA
38.03467m -7.993121mA
dx:66.93m dy:1.355155mA s:20.24735mA/