

-----TX-----

```

13  > covergroup cover_htax_packet;
14  | option.per_instance = 1;
15  | option.name = "cover_htax_packet";
16
17
18  | // Coverpoint for htax packet field : destination port
19  | DEST_PORT : coverpoint tx_mon_packet.dest_port {
20  | | bins dest_port[] = {[0:3]};
21  | }
22
23  | // TO DO : Coverpoint for htax packet field : vc (include vc=0 in illegal bin)
24  | | //VC :
25  | | VC : coverpoint tx_mon_packet.vc {
26  | | | bins valid_vc[] = {[1:VC-1]}; // 合法 VC 值
27  | | | illegal_bins illegal_vc = {0}; // VC=0 是非法值
28  | | }
29
30
31  | // TO DO : Coverpoint for htax packet field : length (Divide range [3:63] into 16 bins)
32  | | //LENGTH :
33  | | LENGTH : coverpoint tx_mon_packet.length {
34  | | | bins length_bins[16] = {[3:7], [8:12], [13:17], [18:22],
35  | | | | [23:27], [28:32], [33:37], [38:42],
36  | | | | [43:47], [48:52], [53:57], [58:63]};
37  | | }

```

```

39 // Coverpoints for Cross
40 // TO DO : DEST_PORT cross VC
41 DEST_PORT_cross_VC : cross DEST_PORT, VC;
42
43 // TO DO : DEST_PORT cross LENGTH
44 DEST_PORT_cross_LENGTH : cross DEST_PORT, LENGTH;
45
46 // TO DO : VC cross LENGTH
47 VC_cross_LENGTH : cross VC, LENGTH;
48
49 endgroup
50
51 covergroup cover_htax_tx_intf;
52 option.per_instance = 1;
53 option.name = "cover_htax_tx_intf";
54
55 // TO DO : Coverpoint for tx_outport_req: covered all the values 0001,0010,0100,1000
56 TX_OUTPORT_REQ : coverpoint htax_tx_intf.tx_outport_req {
57     bins valid_values[] = {4'b0001, 4'b0010, 4'b0100, 4'b1000};
58 }
59 // TO DO : Coverpoint for tx_vc_req: All the VCs are requested atleast once. Ignore what is not allowed, or put it as illegal
60 TX_VC_REQ : coverpoint htax_tx_intf.tx_vc_req {
61     bins valid_vc_req[] = {[1:'VC-1]}; // 合法 VC 值
62     illegal_bins illegal_vc_req = {0}; // 非法 VC 请求
63 }
64 // TO DO : Coverpoint for tx_vc_gnt: All the virtual channels are granted atleast once.
65 TX_VC_GNT : coverpoint htax_tx_intf.tx_vc_gnt {
66     bins valid_vc_gnt[] = {[1:'VC-1]}; // 合法 VC 授予
67     illegal_bins illegal_vc_gnt = {0}; // 非法 VC 授予
68 }
69
70 endgroup

```

-----RX-----

```

18 // TO DO : Create covergroup for htax_rx_inf and add at least one coverpoint
19 covergroup cover_htax_packet;
20 option.per_instance = 1;
21 option.name = "cover_htax_packet";
22
23 data0 : coverpoint rx_mon_packet.data[0] {
24     bins value[3] = {[0:127], [128:256], [256:$]]; // 具體 bins 根據需求定義
25 }
26
27 endgroup

```

Cover Groups | Assertions

Ex: Utl Name Overall Average Grade Overall Covered Enclosing Entity

Utl	Name	Overall Average Grade	Overall Covered	Enclosing Entity
	(no filter)	(no filter)	(no filter)	(no filter)
	cover_htax_packet	100%	105 / 10...	uvm_pkg.uvm_test_top.tb.tx_port[1]d
	cover_htax_tx_intf	100%	6 / 6 (10...	uvm_pkg.uvm_test_top.tb.tx_port[1]d

Showing 2 items

Items | cover_htax_tx_intf

Ex: Utl Name Overall Average Grade Overall Covered

Utl	Name	Overall Average Grade	Overall Covered
	(no filter)	(no filter)	(no filter)
	TX_OUTPUT_REQ	100%	4 / 4 (100%)
	TX_VC_REQ	100%	1 / 1 (100%)
	TX_VC_GNT	100%	1 / 1 (100%)

Showing 3 items

TX_OUTPUT_REQ

Abstract | Expand

Ex: Utl Name Overall Average Grade Overall Covered Score

Utl	Name	Overall Average Grade	Overall Covered	Score
	(no filter)	(no filter)	(no filter)	(no filter)
	valid_values[1]	100%	1 / 1 (100%)	382
	valid_values[2]	100%	1 / 1 (100%)	392
	valid_values[4]	100%	1 / 1 (100%)	375
	valid_values[8]	100%	1 / 1 (100%)	351

Showing 4 items

Details | TX_OUTPUT_REQ

Attributes | Source

Col # Name Value

Col #	Name	Value
	(no filter)	(no filter)
	At Least	1
	Combined Average Grade	100%
	Combined Covered	4.0
	Combined Covered Grade	100%
	Combined Total	4.0
	Combined Total Weighted Coverage	4.0

Cover groups

Ex: Utl Name Overall Average Grade Overall Covered Enclosing Entity

Utl	Name	Overall Average Grade	Overall Covered	Enclosing Entity
	(no filter)	(no filter)	(no filter)	(no filter)
	cover_htax_packet	100%	105 / 10...	uvm_pkg.uvm_test_top.tb.tx_port[1]d
	cover_htax_tx_intf	100%	6 / 6 (10...	uvm_pkg.uvm_test_top.tb.tx_port[1]d

Showing 2 items

Items | cover_htax_packet

Ex: Utl Name Overall Average Grade Overall Covered

Utl	Name	Overall Average Grade	Overall Covered
	(no filter)	(no filter)	(no filter)
	DEST_PORT	100%	4 / 4 (100%)
	VC	100%	1 / 1 (100%)
	LENGTH	100%	16 / 16 (100%)
	DEST_PORT_cross_VC	100%	4 / 4 (100%)
	DEST_PORT_cross_LENGTH	100%	64 / 64 (100%)
	VC_cross_LENGTH	100%	16 / 16 (100%)

Showing 6 items

LENGTH

Abstract | Expand

Ex: Utl Name Overall Average Grade Overall Covered Score

Utl	Name	Overall Average Grade	Overall Covered	Score
	(no filter)	(no filter)	(no filter)	(no filter)
	length_bins[7]	100%	1 / 1 (100%)	70
	length_bins[8]	100%	1 / 1 (100%)	59
	length_bins[9]	100%	1 / 1 (100%)	73
	length_bins[10]	100%	1 / 1 (100%)	68
	length_bins[11]	100%	1 / 1 (100%)	76
	length_bins[12]	100%	1 / 1 (100%)	67
	length_bins[13]	100%	1 / 1 (100%)	77
	length_bins[14]	100%	1 / 1 (100%)	73
	length_bins[15]	100%	1 / 1 (100%)	399

Showing 16 items

Details | LENGTH

Attributes | Source

Col # Name Value

Col #	Name	Value
	(no filter)	(no filter)
	At Least	1
	Combined Average Grade	100%
	Combined Covered	16.0
	Combined Covered Grade	100%
	Combined Total	16.0
	Combined Total Weighted Coverage	16.0

--- UVM Report catcher Summary ---

Number of demoted UVM_FATAL reports : 0
 Number of demoted UVM_ERROR reports : 0
 Number of demoted UVM_WARNING reports: 0
 Number of caught UVM_FATAL reports : 0
 Number of caught UVM_ERROR reports : 0
 Number of caught UVM_WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity

UVM_INFO : 9017

UVM_WARNING : 0

UVM_ERROR : 0

UVM_FATAL : 0

** Report counts by id

[RNTST] 1

[SCOREBOARD] 6005

[TEST_DONE] 1

[TOP] 5

[UVMTOP] 1

[htax tx_driver_c] 3000

[simple_random_seq] 3

[simple_random_test] 1

Simulation complete via \$finish(1) at time 1475710 NS + 45

/opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_root.svh:457

\$finish;

xcelium> exit