

# Lab 4

## HTAX Verification Plan & vPlanner

Due date

Sep 23, 2024 11:59 PM CST

Table of content

Academic Integrity.....	2
Introduction.....	2
<b>Design Under Test.....</b>	<b>2</b>
<b>Environment Setup.....</b>	<b>2</b>
<b>To-do.....</b>	<b>5</b>
<b>Deliverables.....</b>	<b>6</b>

## Academic Integrity


The following actions are strictly prohibited and violate the honor code. The minimum penalty for plagiarism is a grade of zero and a report to the Aggie honor system office.

- Sharing your solutions with a classmate.
- Uploading assignments to external websites or tutoring websites
- Copying solutions from external websites or tutoring websites
- Copying code from a classmate or unauthorized sources and submitting it as your

## Introduction

In this lab, you will learn how to write a verification plan.

## Design Under Test

The DUT is the HyperTransport Advanced X-Bar whose specifications are mentioned in this document:  HyperTransport Advanced X-Bar HTAX Specification.pdf .

## Environment Setup

1. Accept the assignment's repository on GitHub Classroom:  
<https://classroom.github.com/a/B844mhlA>.
2. Clone your lab repository on the Linux server.
3. Setup your environment

```
source setupX.bash
```

4. Run

```
> ncroot
```

You should see “/opt/coe/cadence/XCELIUM” printed out.

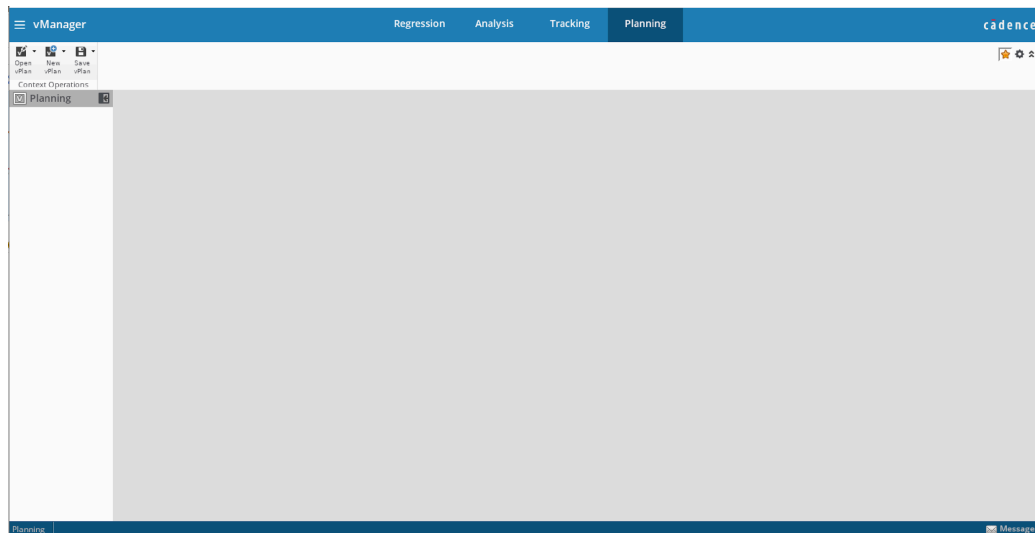
5. Type the following command (the first time you access vManager):

```
> /opt/coe/cadence/VMANAGER/bin/vmanager -server 192.168.2.4:8081
```

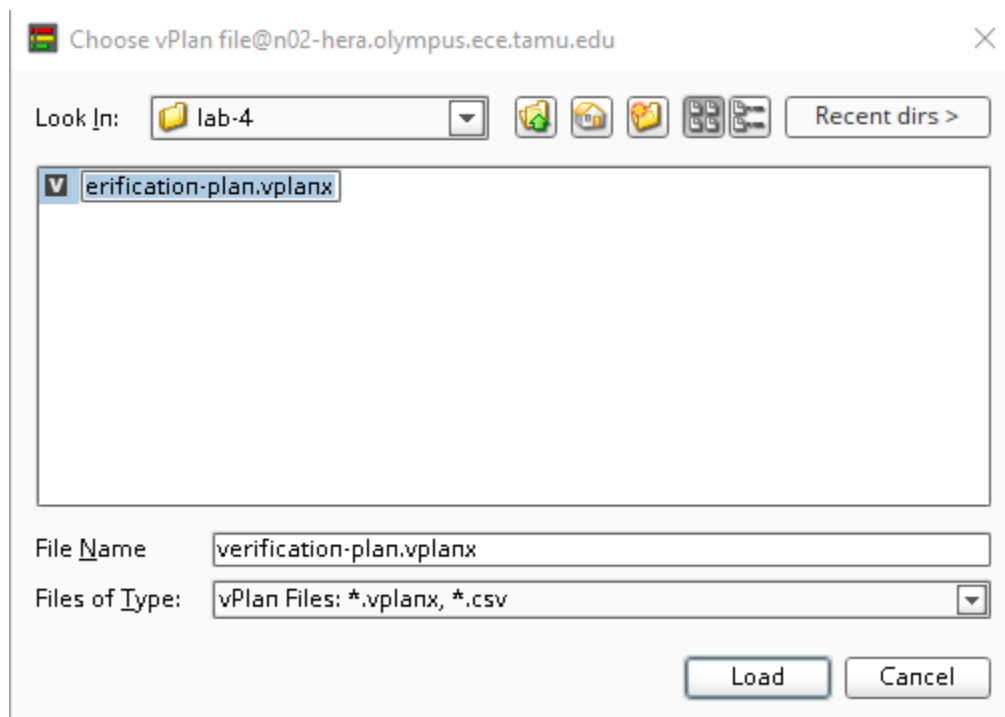
For the second time you access vManager, just type:

```
> vmanager
```

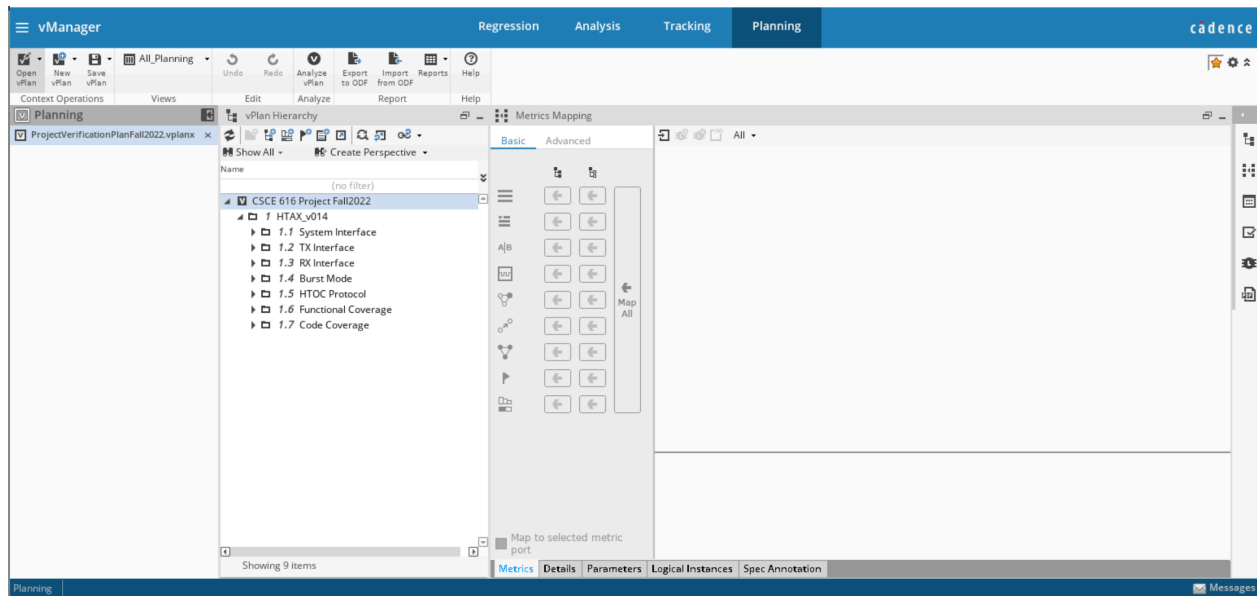
6. When the vManager GUI finishes loading, click on “Planning” in the blue bar at the top. It should invoke the following window (read the vManager Users Guide for how to use all sections/capabilities in this Planning window):



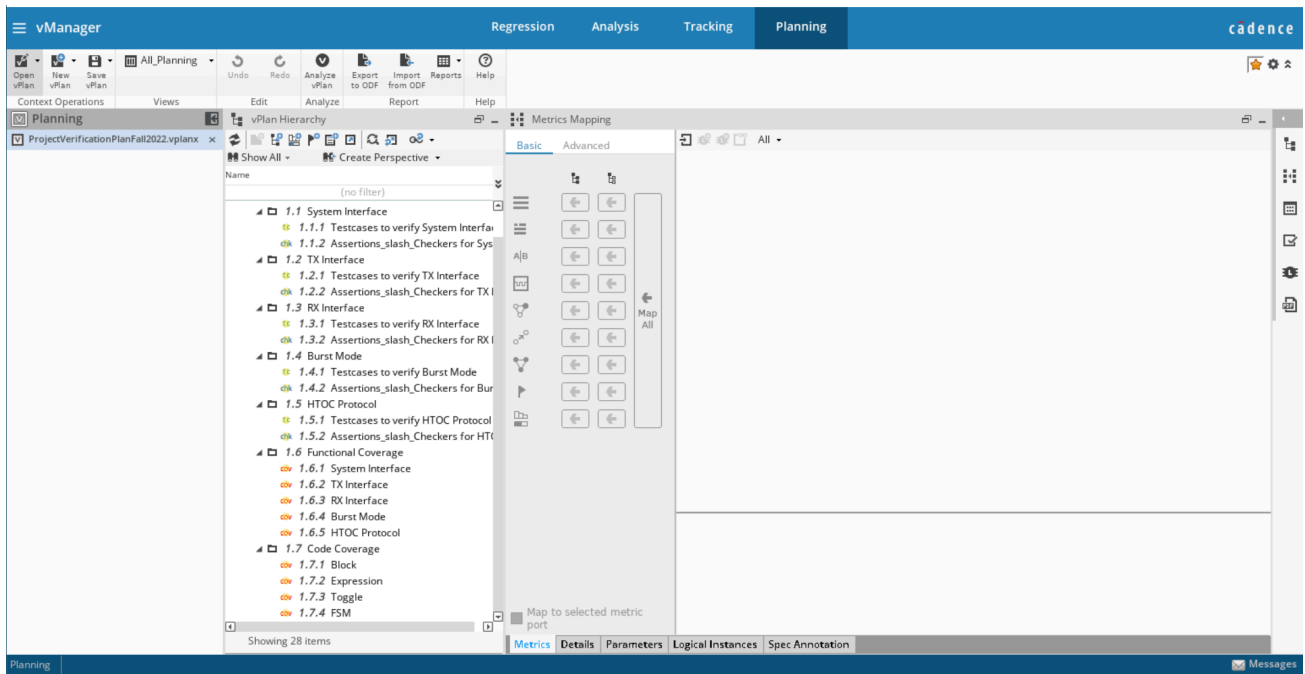
7. To load the default project vPlan (verification-plan.vplanx) click on the “Open vPlan” button at the top-left of the Planning window, and in the resulting pop-up window (shown below) select the vPlan (.vplanx) file and then click “Load” (in the pop-up window shown below).



This will result in the following vManager Planning display:



Expanding the CSCE 616 Project Fall2024 contents results in this display:



8. Create a subsection under the TX Interface section for test cases and add test cases along with a description.

e.g.

- Simple Port-Port test (Test with fixed TX port i and fixed RX port j)
- Short Packet test (Test with packet data length between 3 and 10)
- Random test (Test with random TX port, RX port, delay, and data)

9. Create a subsection under the RX Interface section for test cases and add test cases along with a description. Note: You can repeat the test cases from the TX interface as they also target the RX interface.
10. Create a subsection under the TX Interface section for Assertions/Checkers and add the assertions and a description.

e.g.

- tx\_output\_req is one-hot (tx\_output\_req is a one-hot encoded signal, and its width depends on the number of outputs connected to the HTAX)
- tx output and vc req assert (tx\_output\_req and tx\_vc\_req are asserted simultaneously)
- tx output and vc req deassert (tx\_output\_req and tx\_vc\_req are de-asserted simultaneously)

11. Create a subsection under the RX Interface section for Assertions/Checkers and add assertions and a description.
12. Create a subsection TX Interface under the Functional Coverage section, add coverage and a description.

e.g.

- In port (TX or sender port 0,1,2,3)
- Output Request (RX or receiver port 0,1,2,3)
- Packet Data Length (Packet with all possible data length 3-60)

13. Create a subsection RX Interface under the functional coverage section and add coverage along with a description.
14. Save your verification plan as <your\_name>-verification-plan.vplanx.

## To-do

1. Add at least 2 more test cases (apart from the mentioned examples) for the TX interface
2. Add at least 2 more test cases (apart from the mentioned examples) from the TX interface to the RX interface
3. Add at least 3 more Assertions/Checkers (apart from the mentioned examples) for the TX Interface
4. Add at least 2 more Assertions/Checkers (apart from the mentioned examples) for the RX Interface
5. Add at least 2 more Coverage (apart from the mentioned examples) for the TX Interface
6. Add at least 1 more Coverage (apart from the mentioned examples) for the RX Interface

## Deliverables

Commit and push all your changes to your remote repository.

Your repository must include the following:

- The Verification plan (<your\_name>-verification-plan.vplanx)

Important note: To get full credit, you must upload all the required files and directories and strictly name your files according to the requirements.