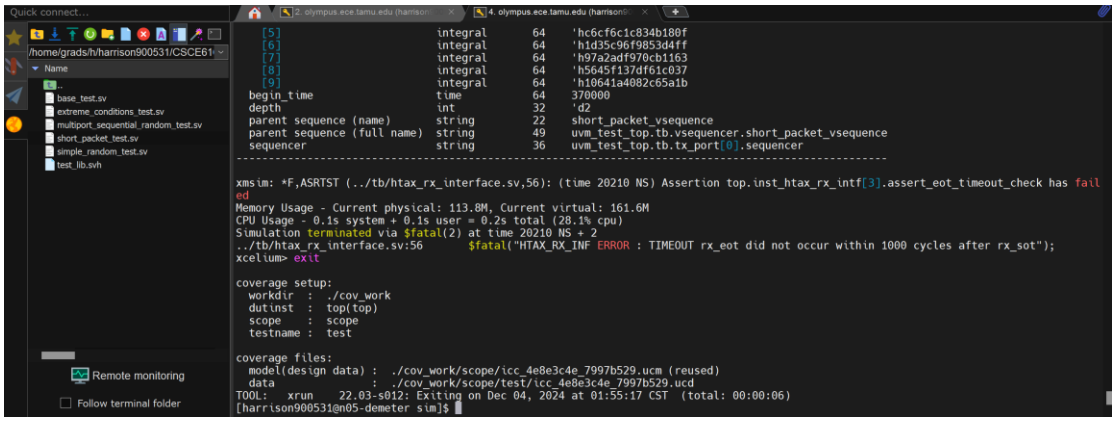
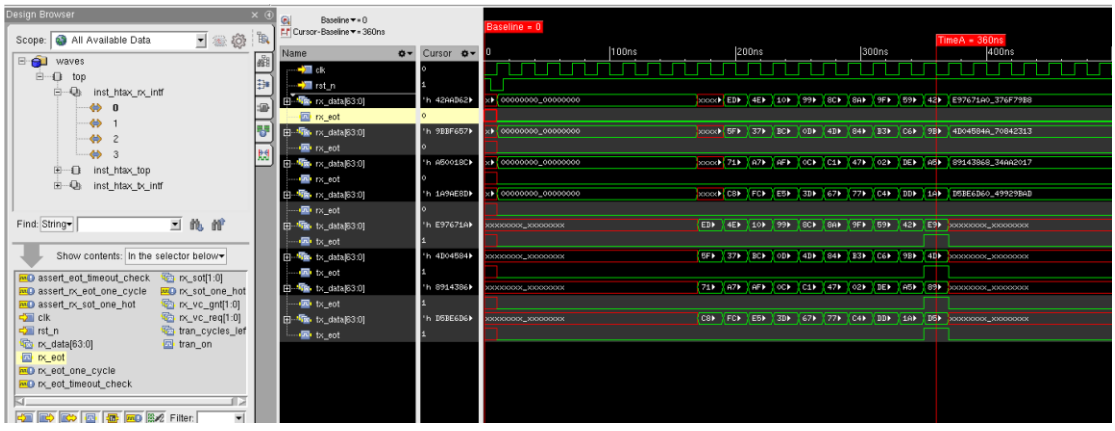


The bug “TIMEOUT rx_eot did not occur within 1000 cycles after rx_sot"happen” when testing the “short pkt”

(xrun -f run.f +UVM_TESTNAME=short_packet_test)

```
23  class short_packet_vsequence extends htax_base_vseq;
25    uvm_object_utils(short_packet_vsequence)
26
27    htax_packet_c req0,req1,req2,req3;
28
29    function new (string name = "random_vsequence");
30      super.new(name);
31    endfunction : new
32
33    task body();
34      // Exectuing 10 TXNs on ports {0,1,2,3} randomly
35      repeat(200) begin
36    fork
37    begin
38      `uvm_info(get_type_name(),"Starting test on port 0", UVM_NONE)
39
40      `uvm_do_on_with(req0,p_sequencer.htax_seqr[0], {req0.dest_port == 0; req0.length ==10; req0.delay ==4;})
41    end
42
43    begin
44      `uvm_info(get_type_name(),"Starting test on port 1", UVM_NONE)
45      `uvm_do_on_with(req1,p_sequencer.htax_seqr[1], {req1.dest_port == 1; req1.length ==10; req1.delay ==4;})
46    end
47
48    begin
49      `uvm_info(get_type_name(),"Starting test on port 2", UVM_NONE)
50      `uvm_do_on_with(req2,p_sequencer.htax_seqr[2], {req2.dest_port == 2; req2.length ==10; req2.delay ==4;})
51    end
52
53    begin
54      `uvm_info(get_type_name(),"Starting test on port 3", UVM_NONE)
55      `uvm_do_on_with(req3,p_sequencer.htax_seqr[3], {req3.dest_port == 3; req3.length ==10; req3.delay ==4;})
56    end
57
```



- rx_eot is never received

- The bug occurred when tx_eot was set for all destination ports, particularly during a fork-join operation. Tracing eot_in to htax_output_data_mux showed that when all tx_eot were asserted, eot_in became 4'b1111. This caused selected_eot (linked to rx_eot) to be set to 0, triggering an assertion failure at the rx_interface.
- Correcting

```
15  )(
20      input [NUM_PORTS-1:0]     eot_in,
21      input wire [(VC*NUM_PORTS)-1:0] sot_in,
22      output reg [WIDTH-1:0]    data_out,
23      output reg          eot_out,
24      output reg [VC-1:0]     sot_out
25  );
26
27      reg                   any_gnt_reg;
28      reg [NUM_PORTS-1:0]   inport_sel_reg;
29      reg [VC-1:0]selected_sot;
30      wire        selected_eot;
31
32      always @( * )
33      begin
34          (* full_case *) (* parallel_case *)
35          casex (inport_sel)
36              4'b1xxx: selected_sot = sot_in[((4*VC)-1):(3*VC)];
37              4'bx1xx: selected_sot = sot_in[((3*VC)-1):(2*VC)];
38              4'bxx1x: selected_sot = sot_in[((2*VC)-1):(1*VC)];
39              4'bxxx1: selected_sot = sot_in[((1*VC)-1):(0*VC)];
40          endcase
41      end
42
43      //assign selected_eot = |(eot_in & inport_sel_reg) & ~(&(eot_in));
44      assign selected_eot = |(eot_in & inport_sel_reg);
45
46      `ifdef ASYNC_RES
47      always @(posedge clk or negedge res_n) `else
48      always @(posedge clk) `endif
49      begin
50      if (!res_n) begin
51        inport_sel_reg <= {NUM_PORTS{1'b0}};
52        any_gnt_reg    <= 0;
53      end else begin
```

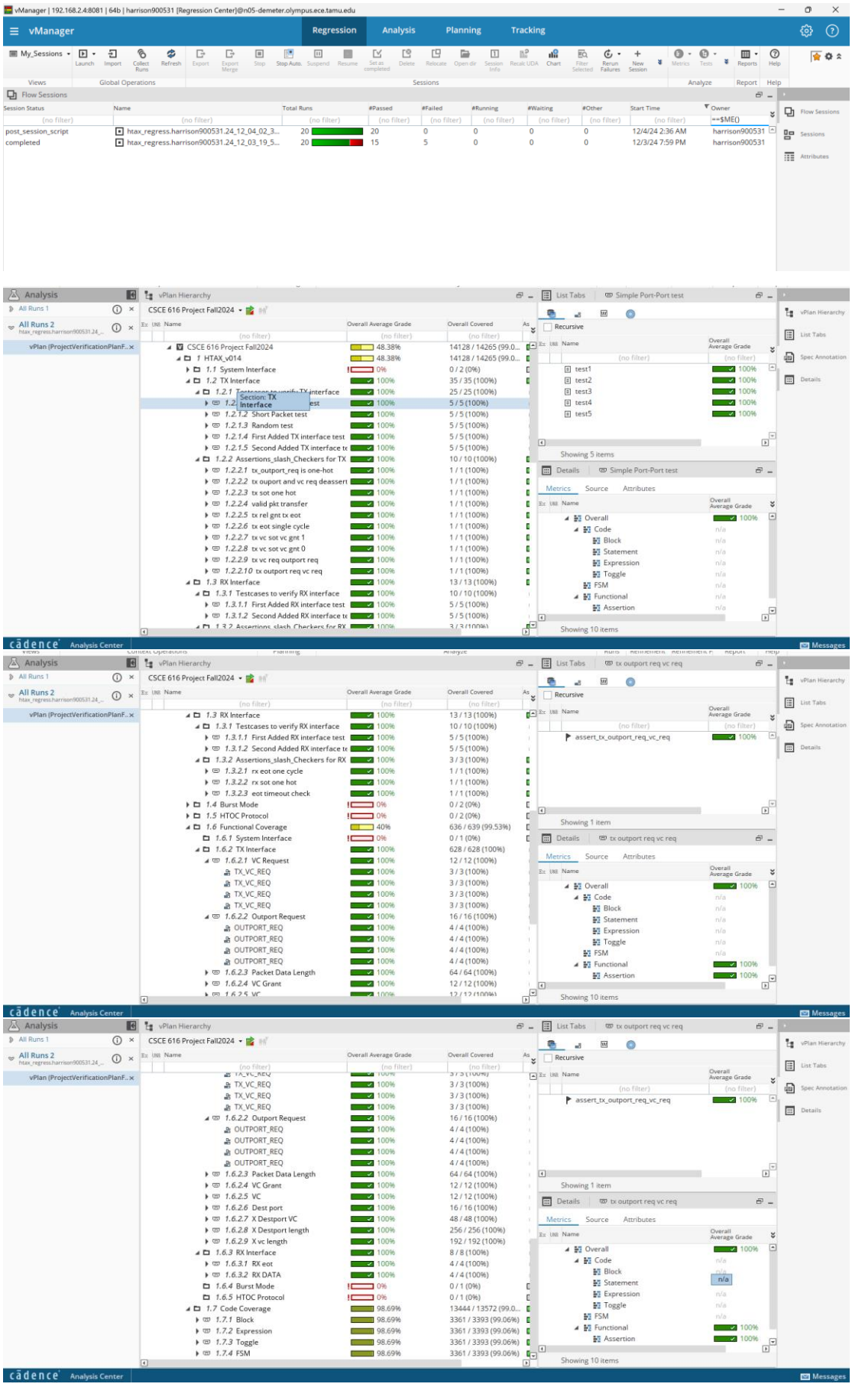
```
/home/grads/h/harrison900531/CSCE61
Name
design
regression
sim
tb
test
mdv.log
vmanager.log
Remote monitoring
Follow terminal folder

Number of demoted UVM_FATAL reports  :    0
Number of demoted UVM_ERROR reports  :    0
Number of demoted UVM_WARNING reports:    0
Number of caught UVM_FATAL reports   :    0
Number of caught UVM_ERROR reports   :    0
Number of caught UVM_WARNING reports :    0

--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 5616
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[RNTST]     1
[SCOREBOARD]  3205
[TEST_DONE]     1
[TOP]     5
[UVMTOP]     1
[htax_tx_driver_c]  1600
[short_packet_test]     1
[short_packet_vsequence]   802
Simulation complete via $finish(1) at time 122010 NS + 45
/opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_root.svh:457     $finish;
xcelium> exit

coverage setup:
  workdir  :  ./cov_work
```


vManager | 192.168.2.4:8081 | 64b | harrison900531 [Regression Center]@n05-demeter.olympus.ece.tamu.edu
vManager
Regression
Analysis
Planning
Tracking
Flow Sessions
Session Status
Name
Total Runs
#Passed
#Failed
#Running
#Waiting
#Other
Start Time
Owner
post_session_script
htax_regress.harrison900531.24_12_04_02_3...
12/4/24 2:36 AM
harrison900531
completed
htax_regress.harrison900531.24_12_03_19_5...
12/3/24 7:59 PM
harrison900531
Analysis
All Runs 1
All Runs 2
vPlan (ProjectVerificationPlanF...
vPlan Hierarchy
CSCE 616 Project Fall2024
Overall Average Grade
Overall Covered
CSCE 616 Project Fall2024 48.38% 14128 / 14265 (99.0...
1 HTAX_v014 48.38% 14128 / 14265 (99.0...
1.1 System Interface 0% 0 / 2 (0%)
1.2 TX Interface 100% 35 / 35 (100%)
1.2.1 Testcases to verify TX interface 100% 25 / 25 (100%)
1.2.1.2 Short Packet test 100% 5 / 5 (100%)
1.2.1.3 Random test 100% 5 / 5 (100%)
1.2.1.4 First Added TX interface test 100% 5 / 5 (100%)
1.2.1.5 Second Added TX interface te 100% 5 / 5 (100%)
1.2.2 Assertions_slash_Checkers for TX 100% 10 / 10 (100%)
1.2.2.1 tx_outport_req is one-hot 100% 1 / 1 (100%)
1.2.2.2 tx ouport and vc req deassert 100% 1 / 1 (100%)
1.2.2.3 tx sot one hot 100% 1 / 1 (100%)
1.2.2.4 valid pkt transfer 100% 1 / 1 (100%)
1.2.2.5 tx rel gnt tx eot 100% 1 / 1 (100%)
1.2.2.6 tx eot single cycle 100% 1 / 1 (100%)
1.2.2.7 tx vc sot vc gnt 1 100% 1 / 1 (100%)
1.2.2.8 tx vc sot vc gnt 0 100% 1 / 1 (100%)
1.2.2.9 tx vc req outport req 100% 1 / 1 (100%)
1.2.2.10 tx outport req vc req 100% 1 / 1 (100%)
1.3 RX Interface 100% 13 / 13 (100%)
1.3.1 Testcases to verify RX interface 100% 10 / 10 (100%)
1.3.1.1 First Added RX interface test 100% 5 / 5 (100%)
1.3.1.2 Second Added RX interface te 100% 5 / 5 (100%)
List Tabs
Simple Port-Port test
Recursive
test1 100%
test2 100%
test3 100%
test4 100%
test5 100%
Showing 5 items
Details
Metrics
Source
Attributes
Overall 100%
Code
Block
Statement
Expression
Toggle
FSM
Functional
Assertion
Showing 10 items
cadence Analysis Center
Messages
1.3 RX Interface 100% 13 / 13 (100%)
1.3.1 Testcases to verify RX interface 100% 10 / 10 (100%)
1.3.1.1 First Added RX interface test 100% 5 / 5 (100%)
1.3.1.2 Second Added RX interface te 100% 5 / 5 (100%)
1.3.2 Assertions_slash_Checkers for RX 100% 3 / 3 (100%)
1.3.2.1 rx eot one cycle 100% 1 / 1 (100%)
1.3.2.2 rx sot one hot 100% 1 / 1 (100%)
1.3.2.3 eot timeout check 100% 1 / 1 (100%)
1.4 Burst Mode 0% 0 / 2 (0%)
1.5 HTOC Protocol 0% 0 / 2 (0%)
1.6 Functional Coverage 40% 636 / 639 (99.53%)
1.6.1 System Interface 0% 0 / 1 (0%)
1.6.2 TX Interface 100% 628 / 628 (100%)
1.6.2.1 VC Request 100% 12 / 12 (100%)
TX_VC_REQ 100% 3 / 3 (100%)
1.6.2.2 Outport Request 100% 16 / 16 (100%)
OUTPORT_REQ 100% 4 / 4 (100%)
1.6.2.3 Packet Data Length 100% 64 / 64 (100%)
1.6.2.4 VC Grant 100% 12 / 12 (100%)
List Tabs
tx outport req vc req
assert_tx_outport_req_vc_req 100%
Showing 1 item
1.6.2.5 VC 100% 12 / 12 (100%)
1.6.2.6 Dest port 100% 16 / 16 (100%)
1.6.2.7 X Destport VC 100% 48 / 48 (100%)
1.6.2.8 X Destport length 100% 256 / 256 (100%)
1.6.2.9 X vc length 100% 192 / 192 (100%)
1.6.3 RX Interface 100% 8 / 8 (100%)
1.6.3.1 RX eot 100% 4 / 4 (100%)
1.6.3.2 RX DATA 100% 4 / 4 (100%)
1.6.4 Burst Mode 0% 0 / 1 (0%)
1.6.5 HTOC Protocol 0% 0 / 1 (0%)
1.7 Code Coverage 98.69% 13444 / 13572 (99.0...
1.7.1 Block 98.69% 3361 / 3393 (99.06%)
1.7.2 Expression 98.69% 3361 / 3393 (99.06%)
1.7.3 Toggle 98.69% 3361 / 3393 (99.06%)
1.7.4 FSM 98.69% 3361 / 3393 (99.06%)
n/a