## ----------original outcome (with bug)----------

```
Asynch Memory Reset
xmsim: *W,OLDURR: The default algorithm for $urandom_range and randcase is used. It can have distribution problems..
Write Address : 8 with data : c6
Read Address : 8 with data : c6
[time:60] [correct] addr[8] (correct_data: c6) data: c6
Write Address : 24 with data : be
Read Address : 24 with data : be
[time:100] [correct] addr[24] (correct_data: be) data: be
Write Address : 4 with data : 2c
Read Address : 4 with data : 2c
[time:140] [correct] addr[4] (correct_data: 2c) data: 2c
Write Address : 10 with data : f0
Read Address : 10 with data : f0
[time:180] [correct] addr[10] (correct_data: f0) data: f0
Write Address : 22 with data : 91
Read Address : 22 with data : 91
[time:220] [correct] addr[22] (correct_data: 91) data: 91
Write Address : 2 with data : 46
Read Address : 2 with data : 46
[time:260] [correct] addr[2] (correct_data: 46) data: 46
Write Address : 15 with data : 31
Read Address : 15 with data : 31
[time:300] [correct] addr[15] (correct_data: 31) data: 31
Write Address : 19 with data : da
Read Address : 19 with data : da
[time:340] [correct] addr[19] (correct_data: da) data: da
Write Address : 12 with data : b9
Read Address : 12 with data : b9
[time:380] [correct] addr[12] (correct_data: b9) data: b9
Write Address : 13 with data : 3f
Read Address : 13 with data : 3f
[time:420] [correct] addr[13] (correct_data: 3f) data: 3f
Write Address : 5 with data : c5
Read Address : 5 with data : c5
[time:460] [correct] addr[5] (correct_data: c5) data: c5
Write Address : 12 with data : 52
Read Address : 12 with data : 52
Read Address : 12 with data : 52
[time:500] [correct] addr[12] (correct_data: 52) data: 52
Write Address : 24 with data : b
Read Address : 24 with data : 0
[time:540] [ERROR] addr[24] (correct_data: b) data: 0
Write Address : 17 with data : d1
Read Address : 17 with data : d1
[time:580] [correct] addr[17] (correct_data: d1) data: d1
Write Address : 4 with data : 55
Read Address : 4 with data : 55
[time:620] [correct] addr[4] (correct_data: 55) data: 55
Write Address : 31 with data : ae
Read Address : 31 with data : ae
[time:660] [correct] addr[31] (correct_data: ae) data: ae
Write Address : 21 with data : 31
Read Address : 21 with data : 31
[time:700] [correct] addr[21] (correct_data: 31) data: 31
Write Address : 18 with data : 21
Read Address : 18 with data : 21
[time:740] [correct] addr[18] (correct_data: 21) data: 21
Write Address : 3 with data : 69
Read Address : 3 with data : 69
[time:780] [correct] addr[3] (correct_data: 69) data: 69
Write Address : 15 with data : 80
Read Address : 15 with data : 80
[time:820] [correct] addr[15] (correct_data: 80) data: 80
Write Address : 10 with data : 31
Read Address : 10 with data : 31
[time:860] [correct] addr[10] (correct_data: 31) data: 31
Write Address : 19 with data : cf
Read Address : 19 with data : cf
[time:900] [correct] addr[19] (correct_data: cf) data: cf
Write Address : 1 with data : 23
Read Address : 1 with data : 23
[time:940] [correct] addr[1] (correct_data: 23) data: 23
Write Address : 3 with data : 17
Read Address : 3 with data : 17
[time:980] [correct] addr[3] (correct_data: 17) data: 17
Write Address : 21 with data : ec
Read Address : 21 with data : ec
Read Address : 21 with data : ec
[time:1020] [correct] addr[21] (correct_data: ec) data: ec
Write Address : 15 with data : 78
Read Address : 15 with data : 78
[time:1060] [correct] addr[15] (correct_data: 78) data: 78
Write Address : 6 with data : c3
Read Address : 6 with data : c3
[time:1100] [correct] addr[6] (correct_data: c3) data: c3
Write Address : 31 with data : fe
Read Address : 31 with data : 0
[time:1140] [ERROR] addr[31] (correct_data: fe) data: 0
Write Address : 25 with data : 9f
Read Address : 25 with data : 9f
[time:1180] [correct] addr[25] (correct_data: 9f) data: 9f
Write Address : 23 with data : 34
Read Address : 23 with data : 34
[time:1220] [correct] addr[23] (correct_data: 34) data: 34
Write Address : 5 with data : 26
Read Address : 5 with data : 26
[time:1260] [correct] addr[5] (correct_data: 26) data: 26
Write Address : 27 with data : 7b
Read Address : 27 with data : 7b
[time:1300] [correct] addr[27] (correct_data: 7b) data: 7b
Simulation complete via $finish(1) at time 1300 NS + 0
../tb/cache_mem_tb.sv:42        $finish;
xcelium> exit
TOOL:   xrun    22.03-s012: Exiting on Sep 07, 2024 at 03:15:32 CDT  (total: 00:00:01)
bash-4.4$
```

---------- testing specific condition with bug----------

```
Asynch Memory Reset
Write Address : 24 with data : 0
Read Address : 24 with data : 0
[time:60] [correct] addr[24] (correct_data: 0) data: 0
Write Address : 24 with data : 1
Read Address : 24 with data : 0
[time:100] [ERROR] addr[24] (correct_data: 1) data: 0
Write Address : 24 with data : 2
Read Address : 24 with data : 0
[time:140] [ERROR] addr[24] (correct_data: 2) data: 0
Write Address : 24 with data : 3
Read Address : 24 with data : 0
[time:180] [ERROR] addr[24] (correct_data: 3) data: 0
Write Address : 24 with data : 4
Read Address : 24 with data : 0
[time:220] [ERROR] addr[24] (correct_data: 4) data: 0
Write Address : 24 with data : 5
Read Address : 24 with data : 0
[time:260] [ERROR] addr[24] (correct_data: 5) data: 0
Write Address : 24 with data : 6
Read Address : 24 with data : 0
[time:300] [ERROR] addr[24] (correct_data: 6) data: 0
Write Address : 24 with data : 7
Read Address : 24 with data : 0
[time:340] [ERROR] addr[24] (correct_data: 7) data: 0
Write Address : 24 with data : 8
Read Address : 24 with data : 0
[time:380] [ERROR] addr[24] (correct_data: 8) data: 0
Write Address : 24 with data : 9
Read Address : 24 with data : 0
[time:420] [ERROR] addr[24] (correct_data: 9) data: 0
```

----------Bug fix----------

```
Asynch Memory Reset
Write Address : 24 with data : 0
Read Address : 24 with data : 0
[time:60] [correct] addr[24] (correct_data: 0) data: 0
Write Address : 24 with data : 1
Read Address : 24 with data : 1
[time:100] [correct] addr[24] (correct_data: 1) data: 1
Write Address : 24 with data : 2
Read Address : 24 with data : 2
[time:140] [correct] addr[24] (correct_data: 2) data: 2
Write Address : 24 with data : 3
Read Address : 24 with data : 3
[time:180] [correct] addr[24] (correct_data: 3) data: 3
Write Address : 24 with data : 4
Read Address : 24 with data : 4
[time:220] [correct] addr[24] (correct_data: 4) data: 4
Write Address : 24 with data : 5
Read Address : 24 with data : 5
[time:260] [correct] addr[24] (correct_data: 5) data: 5
Write Address : 24 with data : 6
Read Address : 24 with data : 6
[time:300] [correct] addr[24] (correct_data: 6) data: 6
Write Address : 24 with data : 7
Read Address : 24 with data : 7
[time:340] [correct] addr[24] (correct_data: 7) data: 7
Write Address : 24 with data : 8
Read Address : 24 with data : 8
[time:380] [correct] addr[24] (correct_data: 8) data: 8
```