

```

(5)      integral      64      'hc6cf6c1c834b180f
(6)      integral      64      'hd35c96f083d4ff
(7)      integral      64      'h57a2adf970eb1163
(8)      integral      64      'h5645f137df61c037
(9)      integral      64      'h10641a4082c65a1b
begin_time      time      64      370000
depth      int      32      02
parent sequence (name)      string      22      short_packet_vsequence
parent sequence (full name)      string      49      uvm_test_top.tb.vsequencer.short_packet_vsequence
sequencer      string      36      uvm_test_top.tb.tx_port[0].sequencer
-----
xmsim: *F,ASRTST ( ../tb/htax_rx_interface.sv,56): (time 20210 NS) Assertion top.inst_htax_rx_intf[3].assert_eot_timeout_check has fail
ed
Memory Usage - Current physical: 113.8M, Current virtual: 161.6M
CPU Usage = 0.1s system + 0.1s user = 0.2s total (20.1% cpu)
Simulation terminated via $fatal(2) at time 20210 NS + 2
../tb/htax_rx_interface.sv:56      $fatal("HTAX_RX_INF ERROR : TIMEOUT rx_eot did not occur within 1000 cycles after rx_sot");
xcelium> exit

coverage setup:
workdir : ./cov_work
dutinst : top(top)
scope : scope
testName : test

coverage files:
model(design data) : ./cov_work/scope/icc_4e8e3c4e_7997b529.ucm (reused)
data : ./cov_work/scope/test/icc_4e8e3c4e_7997b529.ucd
Tool: xrun 22.03-s012: Exiting on Dec 04, 2024 at 01:55:17 CST (total: 00:00:06)
[harrison900531@n05-demeter sim]$

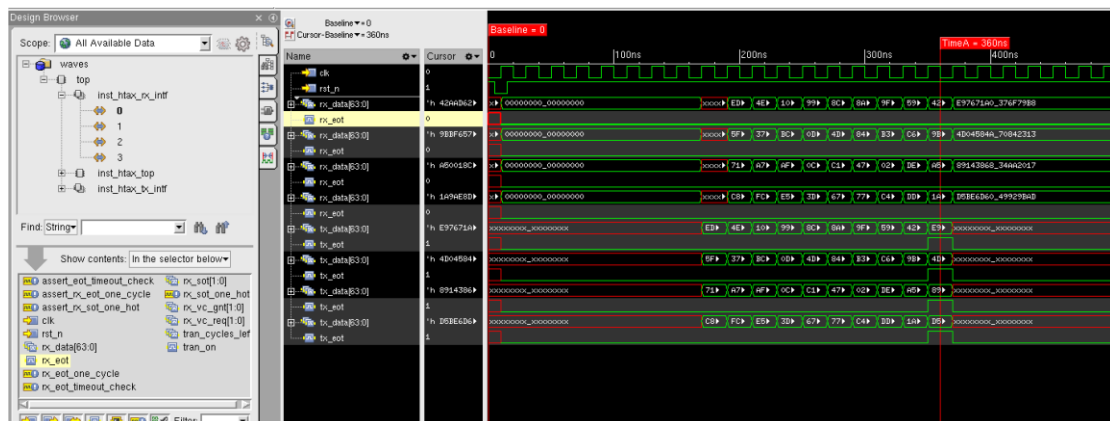
```

The bug “**TIMEOUT rx\_eot did not occur within 1000 cycles after rx\_sot**” happen” when testing the “short pkt”  
(xrun -f run.f +UVM\_TESTNAME=short\_packet\_test)

```

23 class short_packet_vsequence extends htax_base_vseq;
24     uvm_object_utils(short_packet_vsequence)
25
26     htax_packet_c req0, req1, req2, req3;
27
28     function new (string name = "random_vsequence");
29         super.new(name);
30     endfunction : new
31
32     task body();
33         // Exectuing 10 TXNs on ports {0,1,2,3} randomly
34         repeat(200) begin
35             fork
36             begin
37                 `uvm_info(get_type_name(),"Starting test on port 0", UVM_NONE)
38                 `uvm_do_on_with(req0, p_sequencer.htax_seqr[0], {req0.dest_port == 0; req0.length == 10; req0.delay == 4;});
39             end
40
41             begin
42                 `uvm_info(get_type_name(),"Starting test on port 1", UVM_NONE)
43                 `uvm_do_on_with(req1, p_sequencer.htax_seqr[1], {req1.dest_port == 1; req1.length == 10; req1.delay == 4;});
44             end
45
46             begin
47                 `uvm_info(get_type_name(),"Starting test on port 2", UVM_NONE)
48                 `uvm_do_on_with(req2, p_sequencer.htax_seqr[2], {req2.dest_port == 2; req2.length == 10; req2.delay == 4;});
49             end
50
51             begin
52                 `uvm_info(get_type_name(),"Starting test on port 3", UVM_NONE)
53                 `uvm_do_on_with(req3, p_sequencer.htax_seqr[3], {req3.dest_port == 3; req3.length == 10; req3.delay == 4;});
54             end
55         end
56     end
57

```



- rx\_eot is never received

- The bug occurred when tx\_eot was set for all destination ports, particularly during a fork-join operation. Tracing eot\_in to htax\_output\_data\_mux showed that when all tx\_eot were asserted, eot\_in became 4'b1111. This caused selected\_eot (linked to rx\_eot) to be set to 0, triggering an assertion failure at the rx\_interface.
- Correcting

```

15  )(
20      input [NUM_PORTS-1:0] eot_in,
21      input wire [(VC*NUM_PORTS)-1:0] sot_in,
22      output reg [WIDTH-1:0] data_out,
23      output reg eot_out,
24      output reg [VC-1:0] sot_out
25  );
26
27      reg any_gnt_reg;
28      reg [NUM_PORTS-1:0] inport_sel_reg;
29      reg [VC-1:0] selected_sot;
30      wire selected_eot;
31
32      always @( * )
33      begin
34          (* full_case *) (* parallel_case *)
35          casex (inport_sel)
36              4'b1xxx: selected_sot = sot_in[((4*VC)-1):(3*VC)];
37              4'bx1xx: selected_sot = sot_in[((3*VC)-1):(2*VC)];
38              4'bxx1x: selected_sot = sot_in[((2*VC)-1):(1*VC)];
39              4'bxxx1: selected_sot = sot_in[((1*VC)-1):(0*VC)];
40          endcase
41      end
42
43      //assign selected_eot = |(eot_in & inport_sel_reg) & ~(&(eot_in));
44      assign selected_eot = |(eot_in & inport_sel_reg);
45
46      `ifdef ASYNC_RES
47      always @(posedge clk or negedge res_n) `else
48      always @(posedge clk) `endif
49      begin
50          if (!res_n) begin
51              inport_sel_reg <= {NUM_PORTS{1'b0}};
52              any_gnt_reg <= 0;
53          end else begin

```

```

/home/grads/h/harrison900531/CSCCE61
Number of demoted UVM_FATAL reports : 0
Number of demoted UVM_ERROR reports : 0
Number of demoted UVM_WARNING reports : 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 5616
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[RUNST] 1
[SCOREBOARD] 3205
[TEST_DONE] 1
[TOP] 5
[UVMTOP] 1
[htax_tx_driver.c] 1600
[short_packet_test] 1
[short_packet_vsequence] 802
Simulation complete via $finish(1) at time 122010 NS + 45
/opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
xcelium> exit

coverage setup:
workdir : ../cov_work

```

vManager | 192.168.2.4081 | 64b | harrison900531 [Regression Center]@n05-demeter.olympus.ece.tamu.edu

Regression Analysis Planning Tracking

My\_Sessions Launch Collect Runs Refresh Export Merge Step Step Auto Suspended Resume Serial completed Delete Resource Operate Operate Info Recall LDA Chart Filter Selected Filter Failures New Session Monitor Tests Reports Help

Views Global Operations Sessions

Session Status	Name	Total Runs	#Passed	#Failed	#Running	#Waiting	#Other	Start Time	Owner
(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)	(no filter)
post_session_script completed	htax_regress.harrison900531.24_12_04_02_3...	20	20	0	0	0	0	12/4/24 2:36 AM	harrison900531
	htax_regress.harrison900531.24_12_03_19_5...	20	15	5	0	0	0	12/3/24 7:59 PM	harrison900531

Flow Sessions

Flow Sessions Sessions Attributes

Analysis

All Runs 1 All Runs 2

vPlan (ProjectVerificationPlanF..x

CSCE 616 Project Fall2024

Ex: (No) Name	Overall Average Grade	Overall Covered
CSCE 616 Project Fall2024	48.38%	14128 / 14265 (99.0%)
HTAK_v014	48.38%	14128 / 14265 (99.0%)
1.1 System Interface	0%	0 / 2 (0%)
1.2 TX Interface	100%	35 / 35 (100%)
1.2.1 Testcases to verify TX interface	100%	25 / 25 (100%)
1.2.1.1 Test TX interface	100%	5 / 5 (100%)
1.2.1.2 Short Packet test	100%	5 / 5 (100%)
1.2.1.3 Random test	100%	5 / 5 (100%)
1.2.1.4 First Added TX interface test	100%	5 / 5 (100%)
1.2.1.5 Second Added TX interface test	100%	5 / 5 (100%)
1.2.2 Assertions_slash_Checkers for TX	100%	10 / 10 (100%)
1.2.2.1 tx_output_req is one-hot	100%	1 / 1 (100%)
1.2.2.2 tx_output and vc_req deassert	100%	1 / 1 (100%)
1.2.2.3 tx_sot one hot	100%	1 / 1 (100%)
1.2.2.4 valid pkt transfer	100%	1 / 1 (100%)
1.2.2.5 tx_rel gnt tx_eot	100%	1 / 1 (100%)
1.2.2.6 tx_eot single cycle	100%	1 / 1 (100%)
1.2.2.7 tx_vc_sot vc_gnt 1	100%	1 / 1 (100%)
1.2.2.8 tx_vc_sot vc_gnt 0	100%	1 / 1 (100%)
1.2.2.9 tx_vc_req output req	100%	1 / 1 (100%)
1.2.2.10 tx_output_req vc_req	100%	1 / 1 (100%)
1.3 RX Interface	100%	13 / 13 (100%)
1.3.1 Testcases to verify RX interface	100%	10 / 10 (100%)
1.3.1.1 First Added RX interface test	100%	5 / 5 (100%)
1.3.1.2 Second Added RX interface test	100%	5 / 5 (100%)
1.3.2 Assertions_slash_Checkers for RX	100%	3 / 3 (100%)
1.3.2.1 rx_eot one cycle	100%	1 / 1 (100%)
1.3.2.2 rx_sot one hot	100%	1 / 1 (100%)
1.3.2.3 eot timeout check	100%	1 / 1 (100%)
1.4 Burst Mode	0%	0 / 2 (0%)
1.5 HTOC Protocol	0%	0 / 2 (0%)
1.6 Functional Coverage	40%	636 / 639 (99.53%)
1.6.1 System Interface	0%	0 / 1 (0%)
1.6.2 TX Interface	100%	628 / 628 (100%)
1.6.2.1 VC Request	100%	12 / 12 (100%)
1.6.2.1.1 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.1.2 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.1.3 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.2 Output Request	100%	16 / 16 (100%)
1.6.2.2.1 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.2 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.3 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.3 Packet Data Length	100%	4 / 4 (100%)
1.6.2.4 VC Grant	100%	64 / 64 (100%)
1.6.2.5 VC	100%	12 / 12 (100%)
1.6.2.6 Dest port	100%	16 / 16 (100%)
1.6.2.7 X_Destport VC	100%	48 / 48 (100%)
1.6.2.8 X_Destport length	100%	256 / 256 (100%)
1.6.2.9 X_vc length	100%	192 / 192 (100%)
1.6.3 RX Interface	100%	8 / 8 (100%)
1.6.3.1 RX_eot	100%	4 / 4 (100%)
1.6.3.2 RX_DATA	100%	4 / 4 (100%)
1.6.4 Burst Mode	0%	0 / 1 (0%)
1.6.5 HTOC Protocol	0%	0 / 1 (0%)
1.7 Code Coverage	98.69%	13444 / 13572 (99.0%)
1.7.1 Block	98.69%	3361 / 3393 (99.06%)
1.7.2 Expression	98.69%	3361 / 3393 (99.06%)
1.7.3 Toggle	98.69%	3361 / 3393 (99.06%)
1.7.4 FSM	98.69%	3361 / 3393 (99.06%)

Recursive

test1 test2 test3 test4 test5

Showing 5 items

Details Simple Port-Port test

Metrics Source Attributes

Overall Average Grade

Overall 100%

Code n/a

Block n/a

Statement n/a

Expression n/a

Toggle n/a

FSM n/a

Functional 100%

Assertion 100%

Showing 10 items

cadence Analysis Center

Analysis

All Runs 1 All Runs 2

vPlan (ProjectVerificationPlanF..x

CSCE 616 Project Fall2024

Ex: (No) Name	Overall Average Grade	Overall Covered
CSCE 616 Project Fall2024	100%	13 / 13 (100%)
1.3 RX Interface	100%	10 / 10 (100%)
1.3.1 Testcases to verify RX interface	100%	5 / 5 (100%)
1.3.1.1 First Added RX interface test	100%	5 / 5 (100%)
1.3.1.2 Second Added RX interface test	100%	5 / 5 (100%)
1.3.2 Assertions_slash_Checkers for RX	100%	3 / 3 (100%)
1.3.2.1 rx_eot one cycle	100%	1 / 1 (100%)
1.3.2.2 rx_sot one hot	100%	1 / 1 (100%)
1.3.2.3 eot timeout check	100%	1 / 1 (100%)
1.4 Burst Mode	0%	0 / 2 (0%)
1.5 HTOC Protocol	0%	0 / 2 (0%)
1.6 Functional Coverage	40%	636 / 639 (99.53%)
1.6.1 System Interface	0%	0 / 1 (0%)
1.6.2 TX Interface	100%	628 / 628 (100%)
1.6.2.1 VC Request	100%	12 / 12 (100%)
1.6.2.1.1 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.1.2 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.1.3 TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.2 Output Request	100%	16 / 16 (100%)
1.6.2.2.1 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.2 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.3 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.3 Packet Data Length	100%	4 / 4 (100%)
1.6.2.4 VC Grant	100%	64 / 64 (100%)
1.6.2.5 VC	100%	12 / 12 (100%)
1.6.2.6 Dest port	100%	16 / 16 (100%)
1.6.2.7 X_Destport VC	100%	48 / 48 (100%)
1.6.2.8 X_Destport length	100%	256 / 256 (100%)
1.6.2.9 X_vc length	100%	192 / 192 (100%)
1.6.3 RX Interface	100%	8 / 8 (100%)
1.6.3.1 RX_eot	100%	4 / 4 (100%)
1.6.3.2 RX_DATA	100%	4 / 4 (100%)
1.6.4 Burst Mode	0%	0 / 1 (0%)
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1.7.2 Expression	98.69%	3361 / 3393 (99.06%)
1.7.3 Toggle	98.69%	3361 / 3393 (99.06%)
1.7.4 FSM	98.69%	3361 / 3393 (99.06%)

Recursive

assert\_tx\_output\_req\_vc\_req

Showing 1 item

Details tx\_output\_req\_vc\_req

Metrics Source Attributes

Overall Average Grade

Overall 100%

Code n/a

Block n/a

Statement n/a

Expression n/a

Toggle n/a

FSM n/a

Functional 100%

Assertion 100%

Showing 10 items

cadence Analysis Center

Analysis

All Runs 1 All Runs 2

vPlan (ProjectVerificationPlanF..x

CSCE 616 Project Fall2024

Ex: (No) Name	Overall Average Grade	Overall Covered
CSCE 616 Project Fall2024	100%	97 / 97 (100%)
TX_VC_REQ	100%	3 / 3 (100%)
TX_VC_REQ	100%	3 / 3 (100%)
TX_VC_REQ	100%	3 / 3 (100%)
1.6.2.2 Output Request	100%	16 / 16 (100%)
1.6.2.2.1 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.2 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.2.3 OUTPUT_REQ	100%	4 / 4 (100%)
1.6.2.3 Packet Data Length	100%	64 / 64 (100%)
1.6.2.4 VC Grant	100%	12 / 12 (100%)
1.6.2.5 VC	100%	12 / 12 (100%)
1.6.2.6 Dest port	100%	16 / 16 (100%)
1.6.2.7 X_Destport VC	100%	48 / 48 (100%)
1.6.2.8 X_Destport length	100%	256 / 256 (100%)
1.6.2.9 X_vc length	100%	192 / 192 (100%)
1.6.3 RX Interface	100%	8 / 8 (100%)
1.6.3.1 RX_eot	100%	4 / 4 (100%)
1.6.3.2 RX_DATA	100%	4 / 4 (100%)
1.6.4 Burst Mode	0%	0 / 1 (0%)
1.6.5 HTOC Protocol	0%	0 / 1 (0%)
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1.7.1 Block	98.69%	3361 / 3393 (99.06%)
1.7.2 Expression	98.69%	3361 / 3393 (99.06%)
1.7.3 Toggle	98.69%	3361 / 3393 (99.06%)
1.7.4 FSM	98.69%	3361 / 3393 (99.06%)

Recursive

assert\_tx\_output\_req\_vc\_req

Showing 1 item

Details tx\_output\_req\_vc\_req

Metrics Source Attributes

Overall Average Grade

Overall 100%

Code n/a

Block n/a

Statement n/a

Expression n/a

Toggle n/a

FSM n/a

Functional 100%

Assertion 100%

Showing 10 items