# Lab 9

# HTAX Functional Coverage

#### Reminder:

Please take a few minutes of your time to evaluate the course anonymously on <a href="https://tamu.aefis.net/">https://tamu.aefis.net/</a> - Your feedback is valuable.

Note: the deadline to submit your course evaluation is **December 4th, 2024**.

#### Due date

Nov 18, 2024 11:59 PM

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# **Academic Integrity**

The following actions are strictly prohibited and violate the honor code. The minimum penalty for plagiarism is a grade of zero and a report to the Aggie honor system office.

- Sharing your solutions with a classmate.
- Uploading assignments to external websites or tutoring websites
- Copying solutions from external websites or tutoring websites
- Copying code from a classmate or unauthorized sources and submitting it as yours

#### Introduction

In this lab, you will learn to code and measure Coverage for the HyperTransport Advanced X-Bar design specification.

# Design Under Test

The DUT is the HyperTransport Advanced X-Bar whose specifications are mentioned in this document: 

HyperTransport Advanced X-Bar HTAX Specification.pdf.

# **Environment Setup**

- Accept the assignment's repository on GitHub Classroom: https://classroom.github.com/a/b2SJR55W
- 2. Source the setup file.

source setupX.bash cd work

- 3. We have now a full UVM-TB for HTAX design in place (from lab8). Go through all the files in lab9/ directory.
- 4. <u>TX Functional Coverage:</u> Open tb/htax\_tx\_monitor\_c.sv. You need to complete the covergroups cover\_htax\_packet and cover\_htax\_tx\_intf.
- 5. <u>RX Functional Coverage:</u> Open tb/htax\_rx\_monitor\_c.sv. Create covergroup for htax\_rx\_inf and add at least one coverpoint.

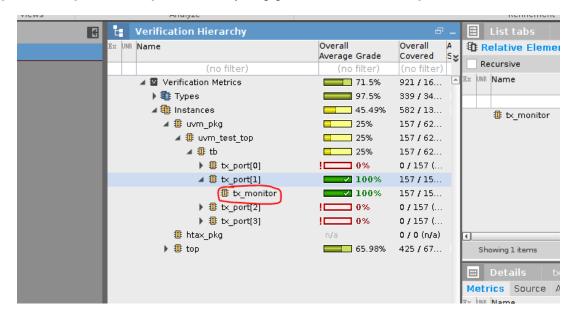
Add as many meaningful cover points as you can think of. There is no limit on number of coverpoints.

6. Simple random test: This test runs sequence - simple\_random\_seq on port[1] sequencer. Run this test using below command:

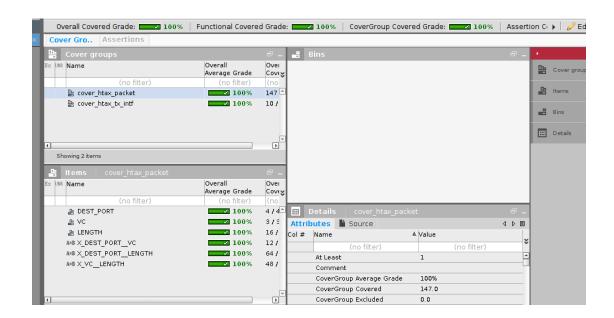
```
cd sim
xrun -f run.f +UVM_TESTNAME=simple_random_test
```

7. <u>Coverage in imc</u>: Open imc and load the database. (look for directions in previous lab manuals)

Navigate through hierarchy to find tx\_port[1]-tx\_monitor coverage.



Right click on it and select "Cover Group Analysis". Once you write all the covergroups and coverpoints they will be listed in the tool window.



8. <u>tx\_port[1]-tx\_monitor coverage:</u> Next you need to modify your tb/sequence(s) (htax\_seqs.sv file) to achieve 100% coverage for tx\_port[1]-tx\_monitor, as shown above. *Hint: You can modify existing simple\_random\_seq sequence.* 

## To-do

- 1. In the htax\_tx\_monitor\_c.sv, complete the following tasks
  - 1.1. Coverpoint for htax packet field: vc (include vc=0 in illegal bin)
  - 1.2. Coverpoint for htax packet field: length (Divide range [3:63] into 16 bins)
  - 1.3. DEST PORT cross VC
  - 1.4. DEST PORT cross LENGTH
  - 1.5. VC cross LENGTH
  - 1.6. Coverpoint for tx outport reg: covered all the values 0001,0010,0100,1000
  - 1.7. Coverpoint for tx\_vc\_req: All the VCs are requested at least once. Ignore what is not allowed, or put it as illegal
  - 1.8. Coverpoint for tx\_vc\_gnt: All the virtual channels are granted at least once

(The above covergroups are instantiated in constructor and sampled in different part of driver logic.)

- 2. In the **htax\_rx\_monitor\_c.sv**, complete the following tasks
  - 2.1. Create covergroup for htax\_rx\_inf and add at least one coverpoint

3. In the IMC, take a screenshot to show you have achieved **100% coverage** for tx\_port[1] - tx\_monitor (as shown in step 7).

NOTE: You have to add coverage screenshot only for tx monitor coverage and not for rx monitor coverage. Total 2 screenshots (1 screenshot for htax\_packet covergroup and 1 screenshot for htax\_intf covergroup).

4. Make a lab report that includes your htax\_tx\_monitor\_c.sv and htax\_rx\_monitor\_c.sv code, UVM summary/simulation output that shows that there are no UVM\_FATAL/UVM\_ERROR/Assertion failures, coverage screenshot (as described in the previous TO-DO) and name it lab\_report.pdf.

#### **Deliverables**

Commit and push all your changes to your remote repository.

Your repository must include the following:

- The test directory
- The sim directory containing lab\_report.pdf
- The tb directory containing updated files.

Important note: To get full credit, you must upload all the required files and directories and strictly name your files according to the requirements.