CSCE 616 – Hardware Design Verification

Lab – 6 TX/RX Interface and SV Assertions

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Objective – Code SV-Assertions for RX/TX interface signals

- Assertions
- SV Assertion example
- UVM Interface connection

Assertions

An assertion is the check embedded in the design.

An assertion is a statement about your design that you expect to be always true.

Assertions are useful in both Formal Verification and Simulation Based Verification.

Assertions checks for the expected behavior and reports forbidden behavior.

Example: tx_outport_req and tx_vc_req should assert simultaneously.

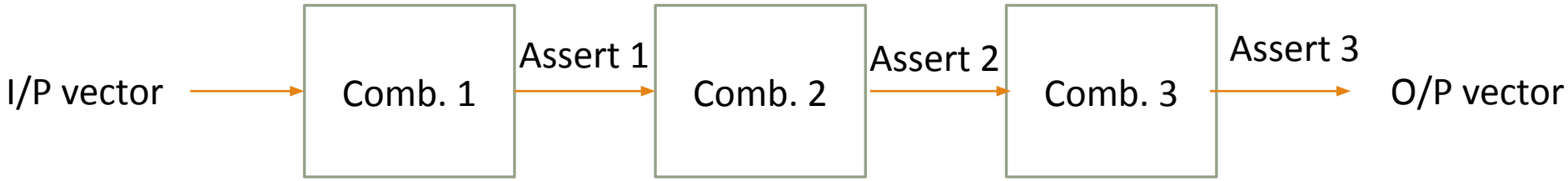
Why do we need Assertions?

Improves observability of DUT.

Example: To verify a DUT, we apply input vectors and observe at the output.

- Between the path from input to output there is combo logic. If there is a bug in that combo logic, it will be propagated to output. To know the reason of incorrect output, we need to back trace from output till we hit the bug.
- So to avoid the long back tracing, we add assertions at intermediate points which will be able to catch the bugs much before it appears at output.

Assertions help us get closer to source of bug => Less Debug



Types of Assertions

Immediate Assertions:

- These are simple assertion statements that are checked whenever visited in procedural code.
- These assertions cannot checks conditions that require passage of time.
- Immediate assertions are evaluated whenever they are visited inside a procedural code.
- Suitable for only Simulation Based Verification.

  e.g. if (grant == 1) begin assert (grant && request)

Concurrent Assertions:

- These are the assertion statements that are always evaluated relative to one or more clocks.
- These assertions describe behavior that spans time.
- Must include a clocking event
- Suitable for both Simulation Based and Formal Verification

Concurrent Assertions and Properties

- We make use of properties to write assertions.
- Properties uses sequences.
- Sequences is combinations of various Boolean expressions

Example: tx_outport_req and tx_vc_req should assert simultaneously.

```
property tx_outport_req_with_vc_req;
    @(posedge clk) disable iff(!res_n)
    (|tx_outport_req) |-> (|tx_vc_req) ;
endproperty
assert_tx_outport_req_with_vc_req : assert property(tx_outport_req_with_vc_req)
else
    $error("HTAX_TX_INF ERROR : tx_outport_req and tx_vc_req not asserted simultaneously");
```

UVM Interface connection (source UVM cookbook)

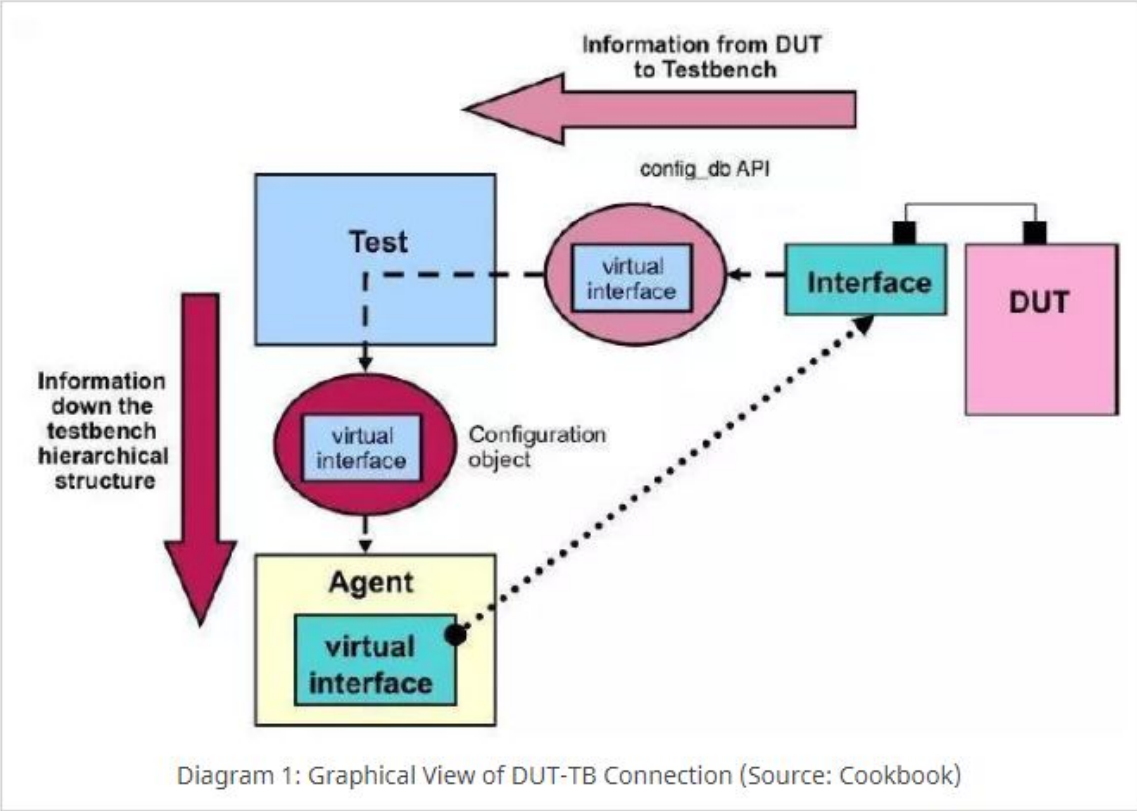


Diagram 1: Graphical View of DUT-TB Connection (Source: Cookbook)

Thank you