25 Spring ECEN 607: Advanced Analog Circuit Tech Design Post-lab Report

Lab4: Op Amp Design - I

Name: Yu-Hao Chen

UIN:435009528

Section:601

Professor: Jose Silva-Martinez

TA: Yoon, Sung J

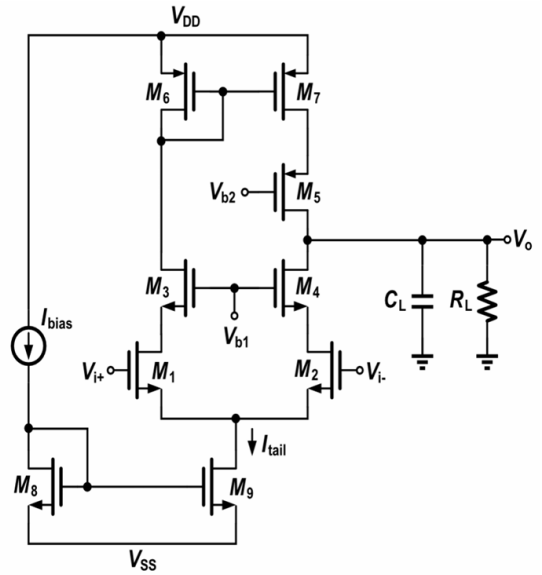


Figure 2-2: Telescopic single stage amplifier

V_{DD}-V_{SS}	5.5 V
A_{v0}	> 70 dB
GBW	> 2 MHz
PM	> 45°
Output Swing @ gain>40dB	> 0.8 V
C_L	2 pF
R_L	100kΩ
Power Dissipated	< 300 µW
Input referred noise (10 Hz – 2 MHz)	<30 µVrms

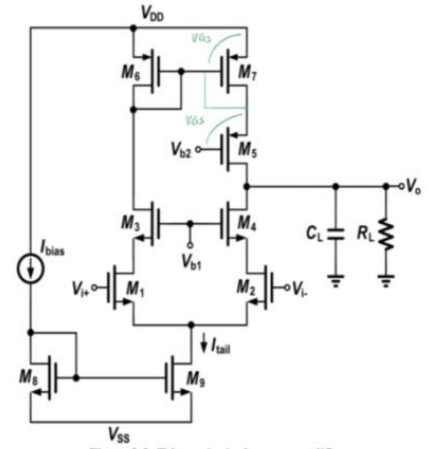


Figure 2-2: Telescopic single stage amplifier

Table 2-2: Design specifications

$$I_{max} = 54.5\mu A$$

$$Id_2\,\max = 27.25\mu A$$

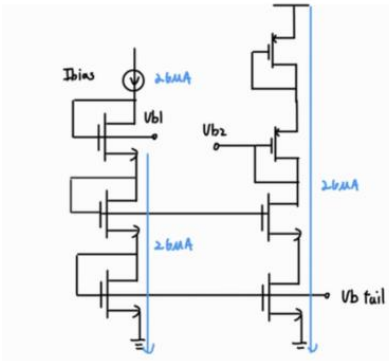
$$Set\ Id_2 = 26uA$$

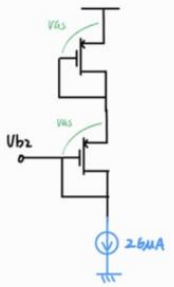
$$GBW = \frac{gm_2}{2\pi CL} > 2M$$

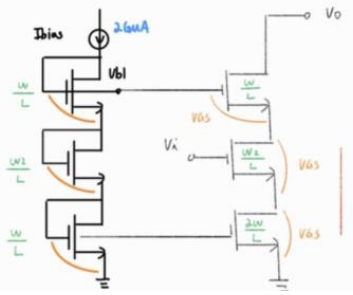
$$\frac{gm_2}{Idz} = 16 \quad gm_2 = 25.12\mu \quad Idz = 26\mu A$$

$$w_2 = 82.92\mu \qquad w_4 = 24.07\mu \qquad w_5 = 121.49\mu \qquad w_9 = 48.14\mu$$

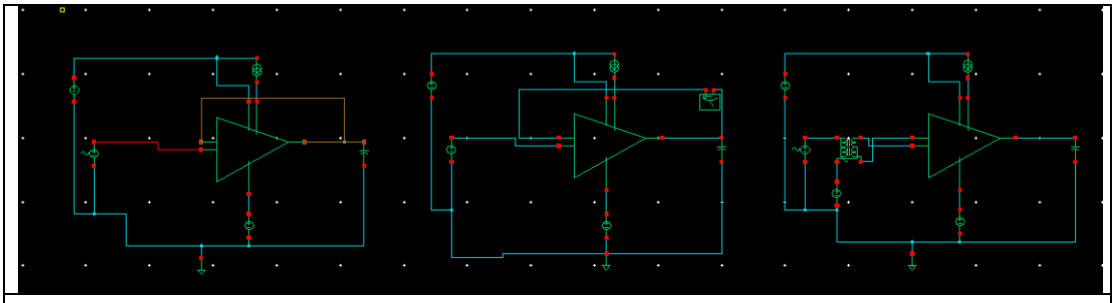
$$\frac{gm}{ID} = 10$$

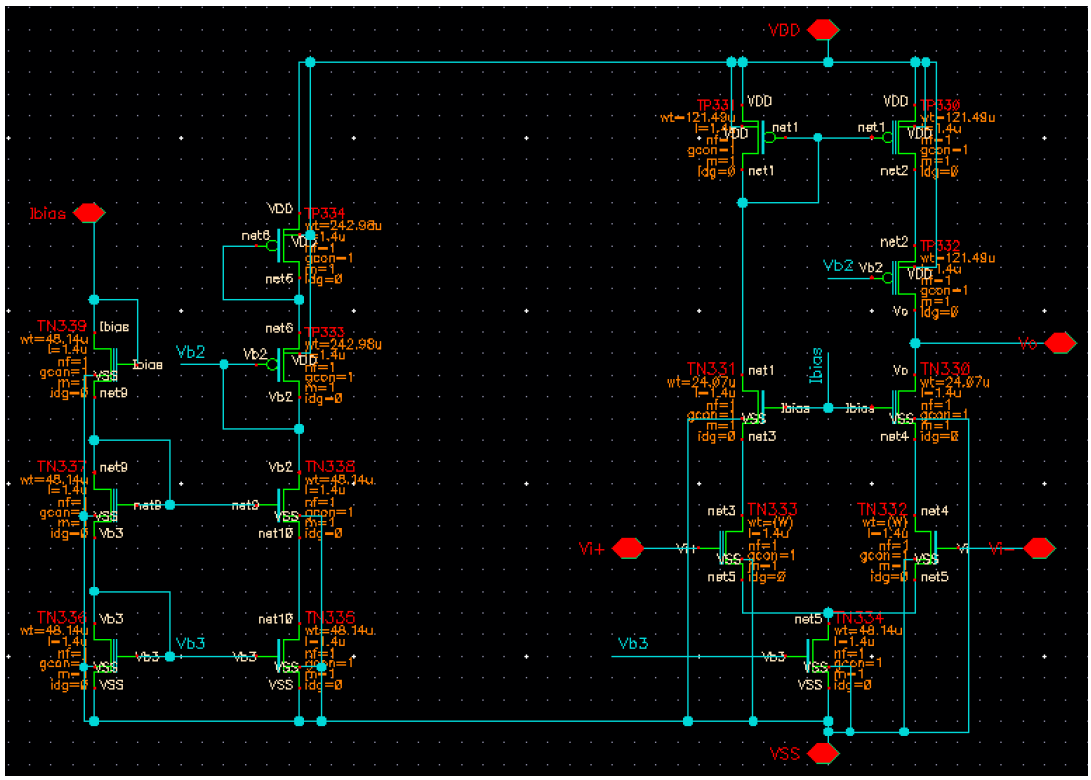


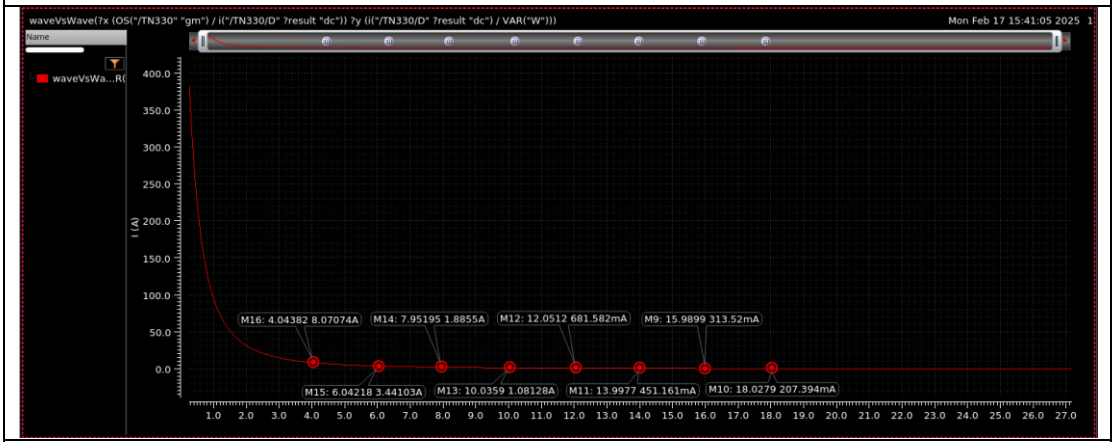




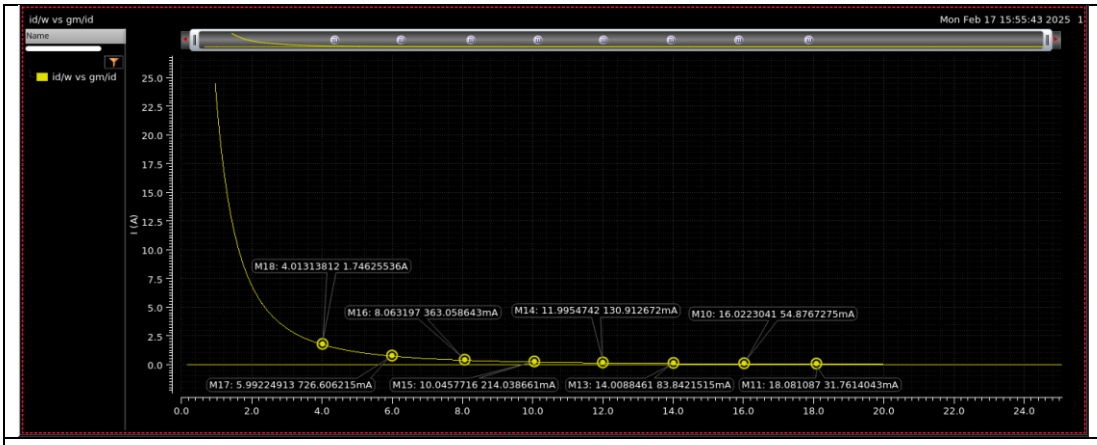
$$Id = \frac{1}{2}\,\mu n cox \frac{w}{L}(VGs - vt)^2$$





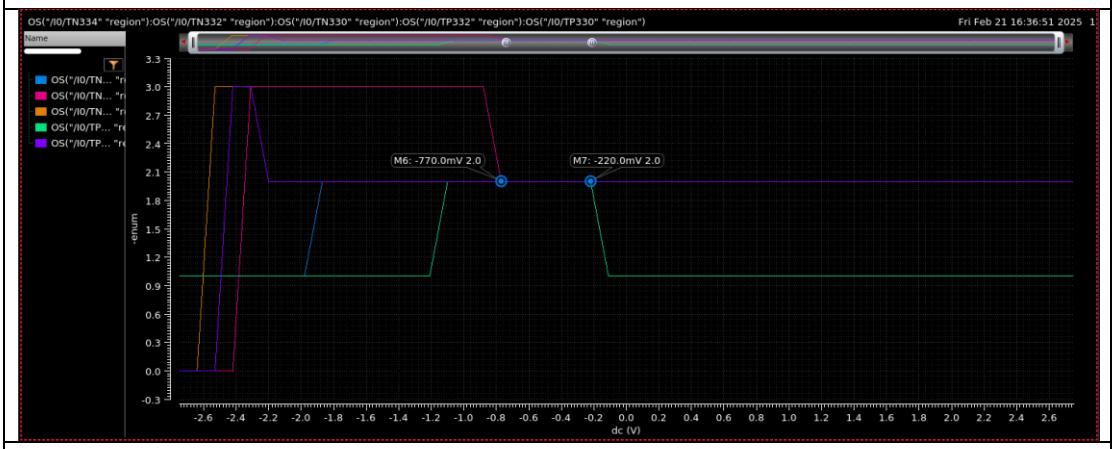


NFETMX current density (L=1.4u)

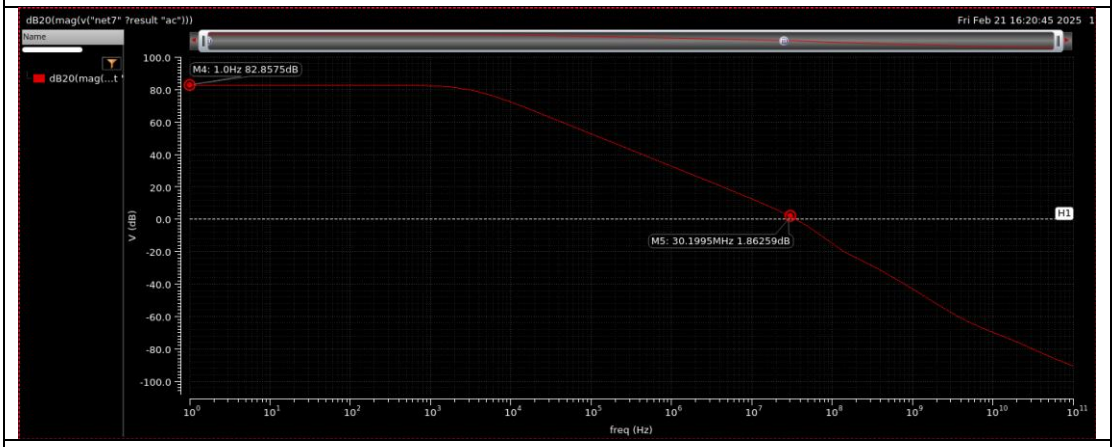


PFETMX current density (L=1.4u)

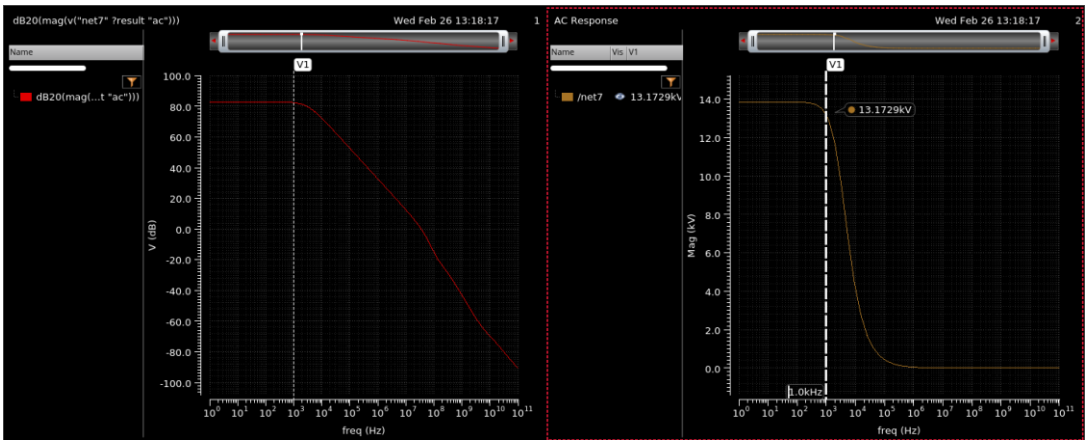
1. Simulate the circuit from the prelab and adjust the transistor sizes accordingly until all specifications are met. Provide necessary plots such that you clearly show the specs are met. The output swing specification should be tested with a transient simulation.



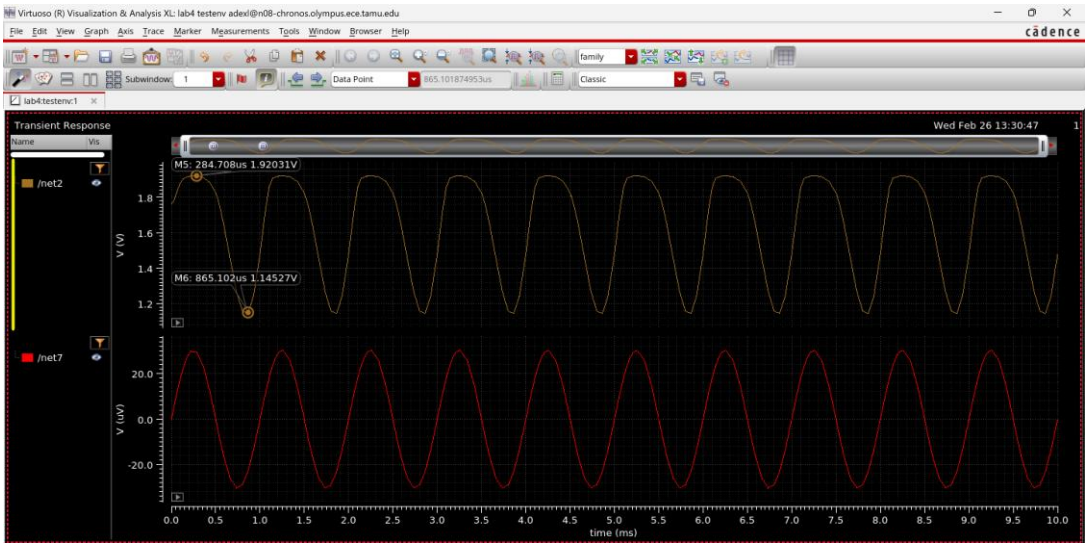
Vcm (Vin Dc operation)range



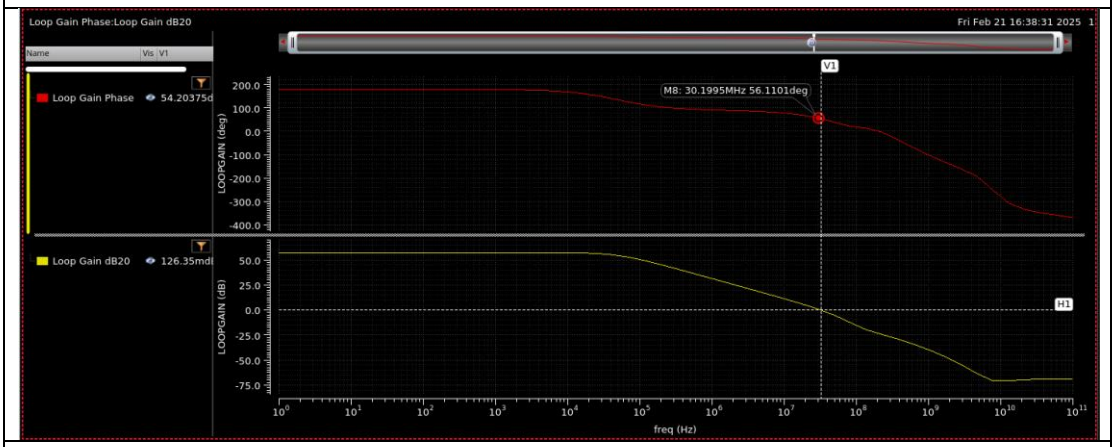
DC gain= 82dB & GBW= 30.19M Hz



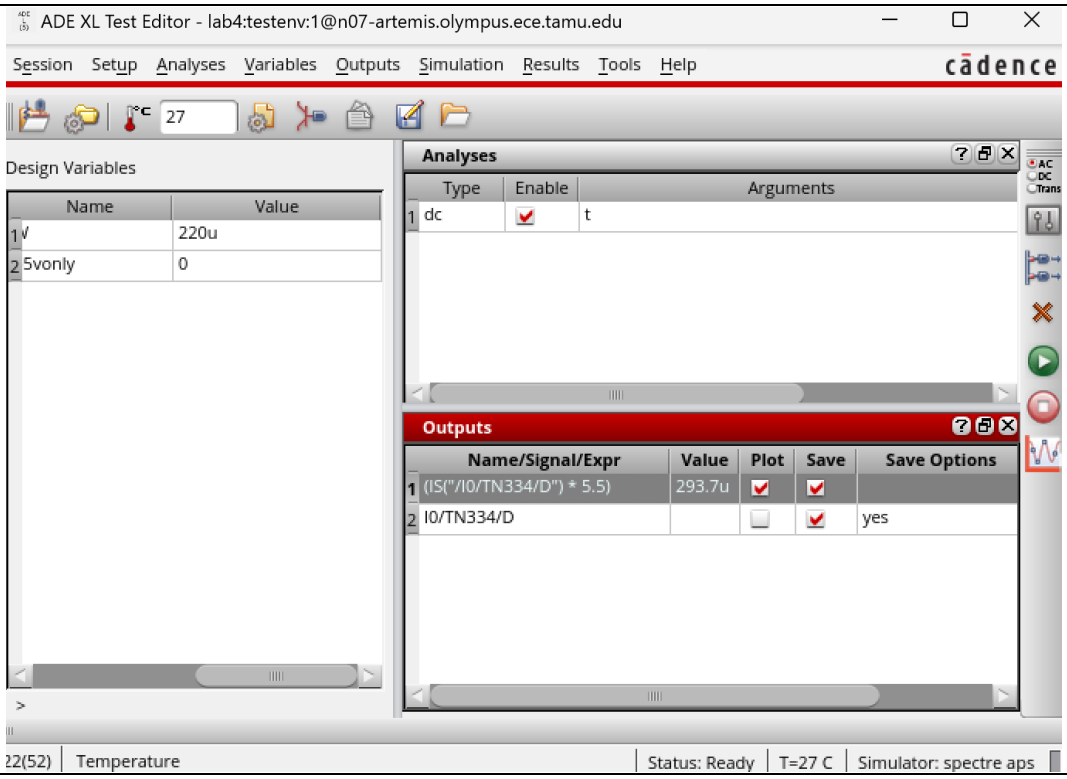
Vo= 0.4-0.4 sin, /AV=13.172k, Vi=30.387u @1k



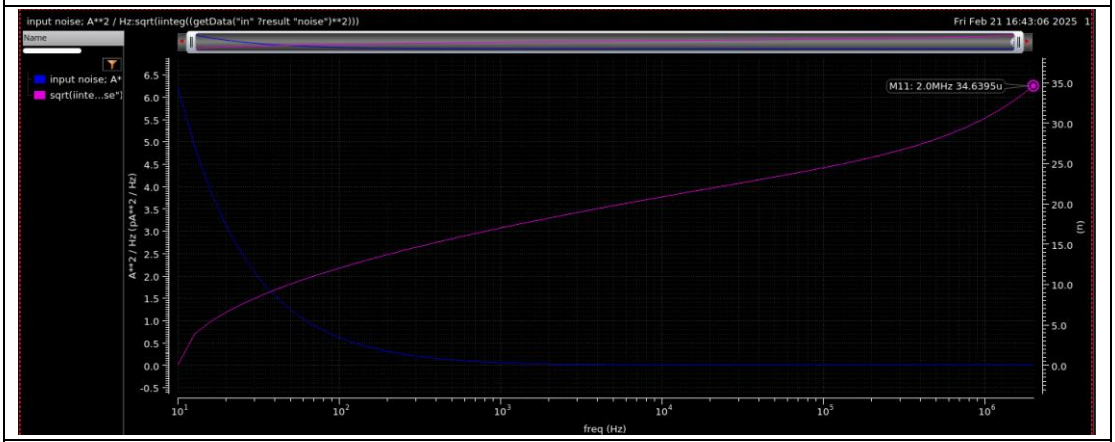
Output swing



PM= 56.11 deg



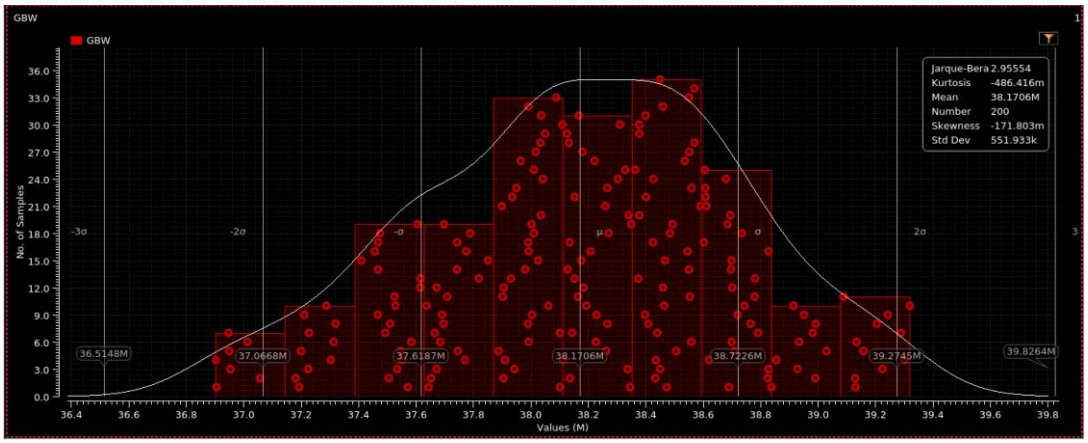
Power Dissipated= 293uW

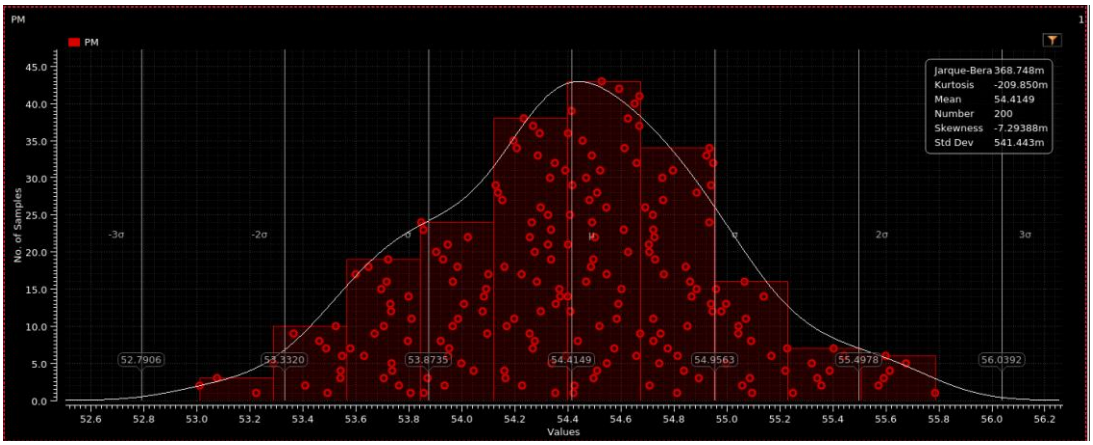


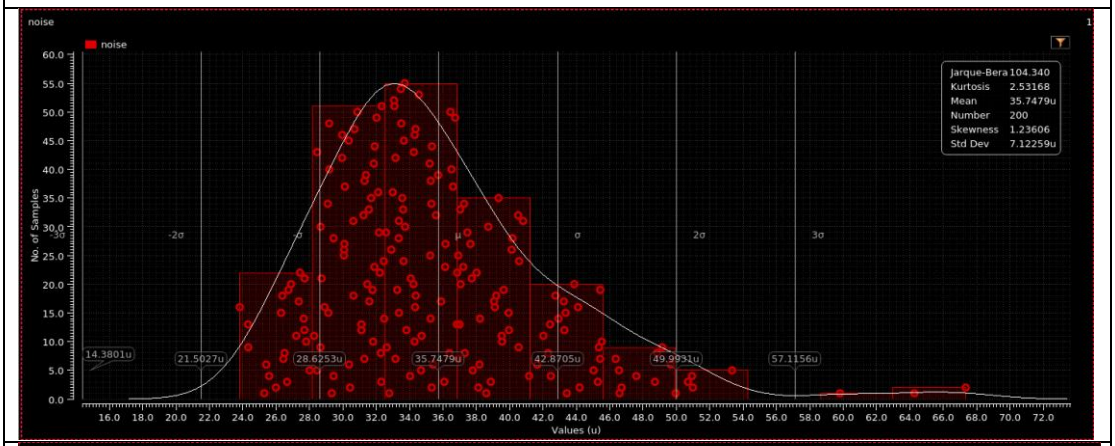
Input referred noise

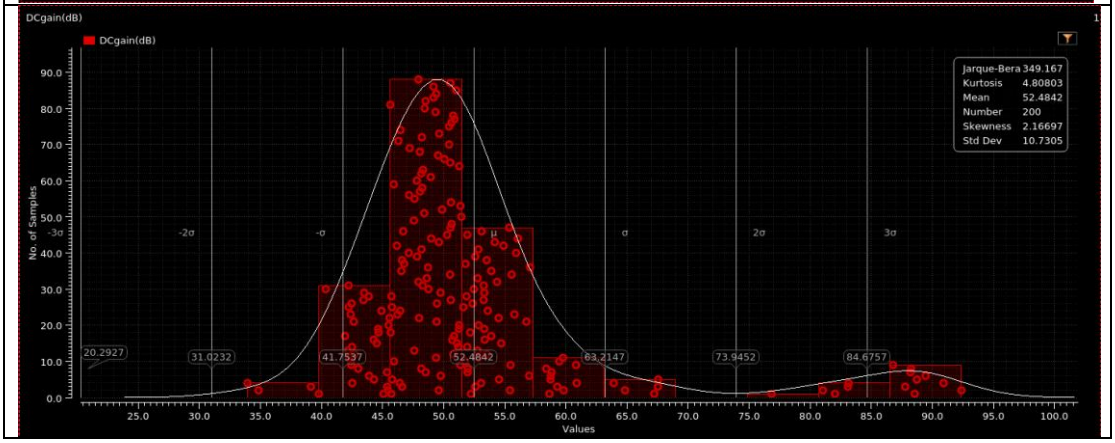
test	noise	34.64u			
test	DCgain(dB)	82.86			
test	GBW	38.17M			
test	PM	54.48			

2. Run a statistical simulation (Monte Carlos) and provide the worst-case DC Gain, GBW, Phase Margin and input referred noise. You do not have to adjust the design if the specs are not met. Comment the results.

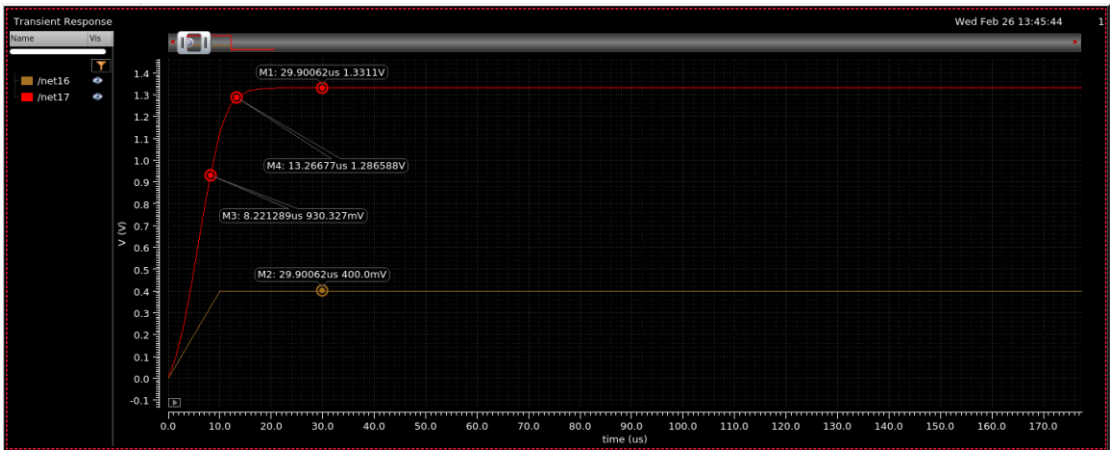

GBW
GBW
Jarque-Bera 2.95554
Kurtosis -486.416m
Mean 38.1706M
Number 200
Skewness -171.803m
Std Dev 551.933k
No. of Samples
Values (M)
-3σ
-2σ
-σ
μ
σ
2σ
3σ
36.5148M
37.0668M
37.6187M
38.1706M
38.7226M
39.2745M
39.8264M


PM
PM
Jarque-Bera 368.748m
Kurtosis -209.850m
Mean 54.4149
Number 200
Skewness -7.29388m
Std Dev 541.443m
No. of Samples
Values
-3σ
-2σ
-σ
μ
σ
2σ
3σ
52.7906
53.3320
53.8735
54.4149
54.9563
55.4978
56.0392


noise
noise
Jarque-Bera 104.340
Kurtosis 2.53168
Mean 35.7479u
Number 200
Skewness 1.23606
Std Dev 7.12259u
No. of Samples
Values (u)
-3σ
-2σ
-σ
μ
σ
2σ
3σ
14.3801u
21.5027u
28.6253u
35.7479u
42.8705u
49.9931u
57.1156u


DCgain(dB)
DCgain(dB)
Jarque-Bera 349.167
Kurtosis 4.80803
Mean 52.4842
Number 200
Skewness 2.16697
Std Dev 10.7305
No. of Samples
Values
-3σ
-2σ
-σ
μ
σ
2σ
3σ
20.2927
31.0232
41.7537
52.4842
63.2147
73.9452
84.6757

3. Configure a unity-gain buffer and apply a differential pulse of 1 KHz, 0.4 Vpp. Show the screen shots and provide comments on the step response; 30% and 1% settling time? Ringing? Comment on the results.



30% settling time = Vo*0.3

4. Provide a comparison table of hand-calculated vs. final transistor sizes including the required specs vs. simulated specs.

Pre (including RL 100k)	Post (without RL 100k)	Spec
M1&M2: 6.28m/1.4u	M1&M2:220u/1.4u	Av0: 82.86dB
M3&M4: 1.82m/1.4u	M3&M4: 24.07u/1.4u	GBW: 38.17M
M5: 9.2m/1.4u	M5: 121.49u/1.4u	PM: 55.48
M6&M7:9.2m/1.4u	M6&M7:121.49u/1.4u	Noise: 34.64u
M9: 1.82m/1.4u	M9: 48.14u/1.4u	Swing:
		Power: 293.7uW

5. Conclusion

The **Cascode NFETMX Amplifier** is a high-gain, high-bandwidth design widely used in analog circuits due to its superior performance in voltage gain, output impedance, and frequency response. It combines a **common-source (CS)** stage with a **common-gate (CG)** configuration, leveraging the strengths of both configurations. Just as the usual amplifier, for the low noise we need to increase the Id and Gm of the input stage. The stability will be stable compare to other amplifier because the dominant pole at output is dominate by CL which is large than pole2 (Cgs Cgd…), so the two will be separate widely.