

# ECEN-607: Advanced Analog IC Design

## Assignment #2:

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Due: 02/06/2025

Instructor: Jose Silva-Martinez

Design at transistor level a two-stage amplifier; use the following specifications:

$V_{DD} = 1.8\text{ V}$

$V_{SS} = 0\text{ V}$

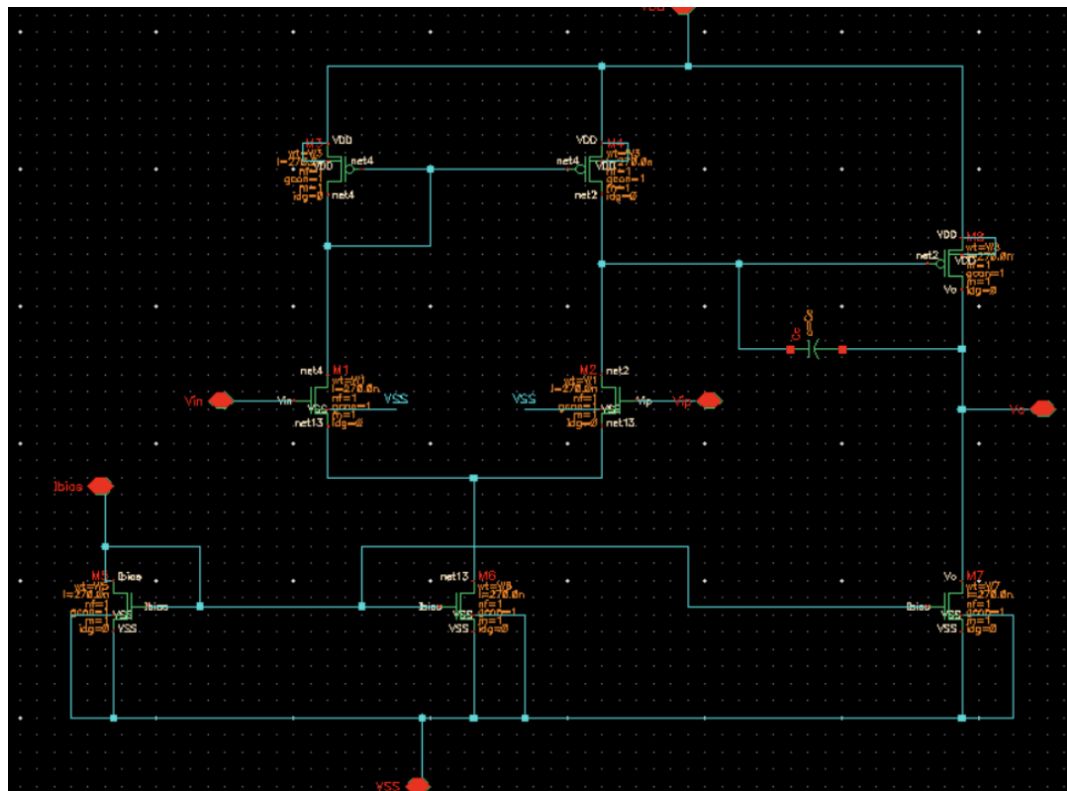
Gain > 40 dB

Employ loop compensation; phase margin > 45°

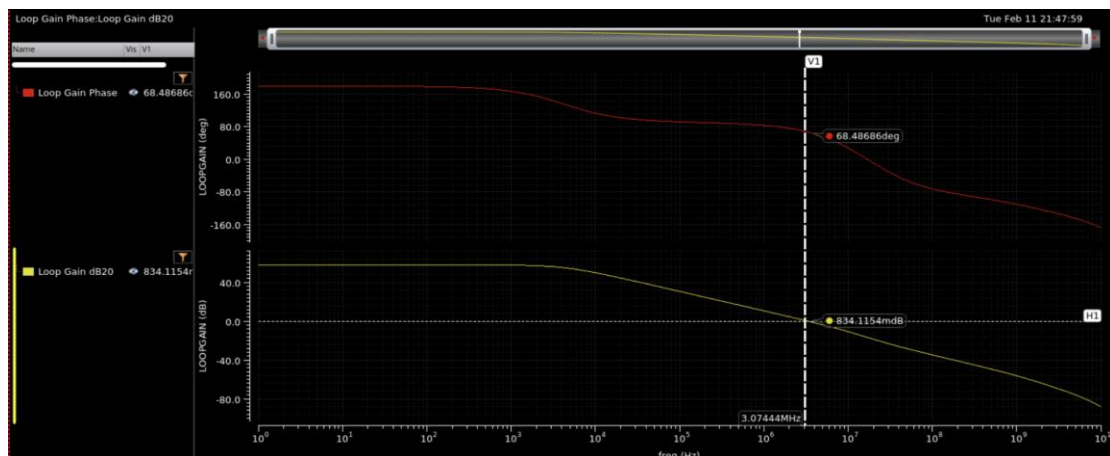
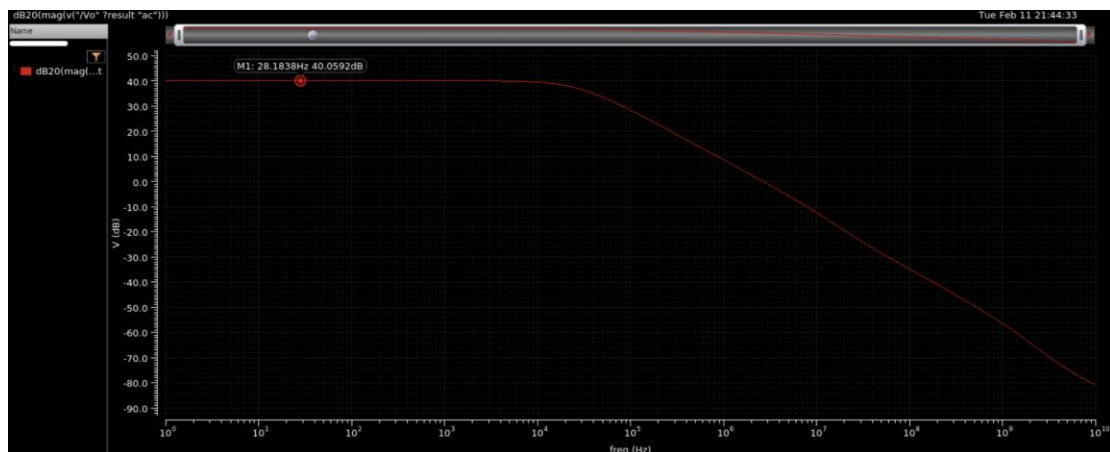
GBW > 4 MHz

Load Capacitor = 10 pF

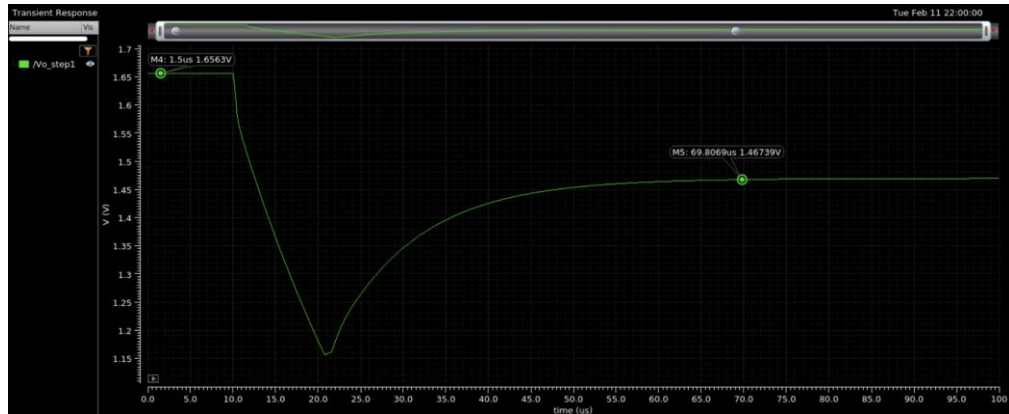
- i) Show amplifier's functionality. Simulate the amplifier and plot both magnitude and phase response. Report screen shots.



Design Variables		
	Name	Value
1	Cc	5p
2	Ibias	36u
3	VCM	828m
4	VDM	0
5	W1	2u
6	W3	2u
7	W5	2u
8	W6	1u
9	W7	4u
10	W8	22u
11	p5vonly	0



- ii) Implement a capacitive amplifier with an inverting gain of 6dB,  $\beta=1/3$ ; minimum capacitor used in the amplifier must be  $\geq 100\text{fF}$ . You may need to connect a large resistor ( $>1\text{Mohm}$ ) in parallel with the feedback capacitor; why? a. Plot the loop gain; simulate the amplifier and report both magnitude and phase response. b. Plot the step response for an input step of 0 to 100mV variation. Report the 1% settling time and value of the settling error. Ideal output voltage variation should be -200mV. c. Comment on the results.



- iii) Repeat ii) for the case of an inverting amplifier with gain=12dB; evidently the feedback factor is different now. For the transient simulation, reduce the size of the input step to 0.50mV.

