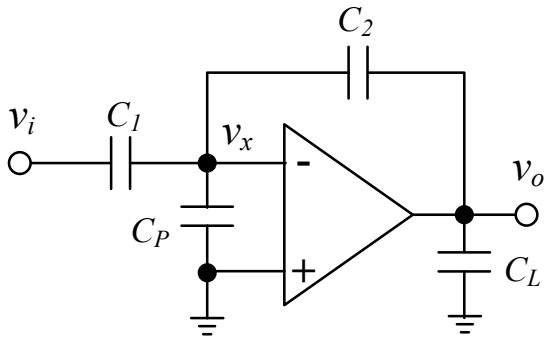
February 27, 2025

ECEN-607: Advanced Analog IC Design
Assignment #4

Due: March 18, 2025
Submit your assignments through Canvas
Homework will not be received after due.
Instructor: Dr. Jose Silva-Martinez

Repeat your assignment 3, but use the following architecture:

- DC gain >50dB
- Total power must be limited to 5mWatts; reduce as much as possible the slew-rate and linear settling.
- C1=800fF, C2=100fF, CL=200fF; CP represents the parasitic capacitors of the amplifier and should not be added (CP=0).
- The circuit must be fully-differential, then a common-mode feedback engine must be included.



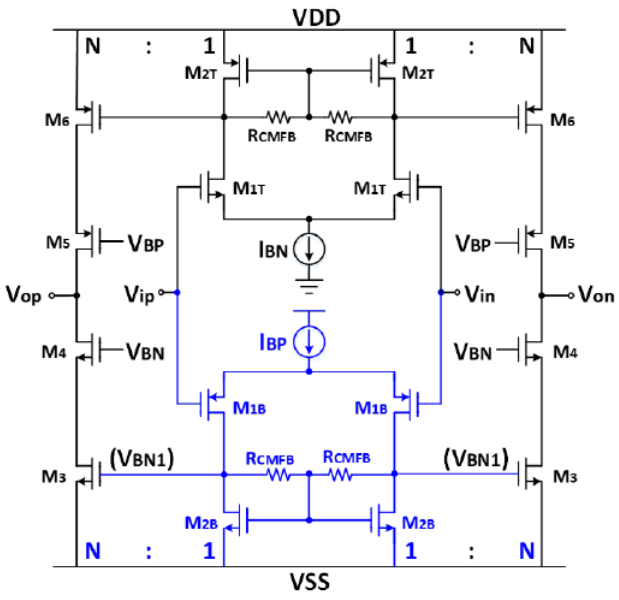


Fig. 3. Proposed dual inputs two stage amplifier architecture (D2SA)

i) Measure the AC properties of the loop gain; do your best for the stabilization of the architecture. Report the magnitude and phase response and measure the phase and gain margin.

ii) Measure the 100mV step response. Report the steady state settling error and the 1% settling time.

iii) Compare the results for this architecture and the ones obtained with the ring amplifier used in assignment 3.

Prepare a report of no more than 4 pages. **Your report must be concrete but clear; include relevant screen shots!**