ECEN-607: Advanced Analog IC Design

Assignment #4:

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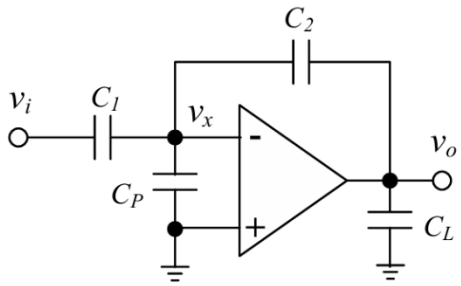


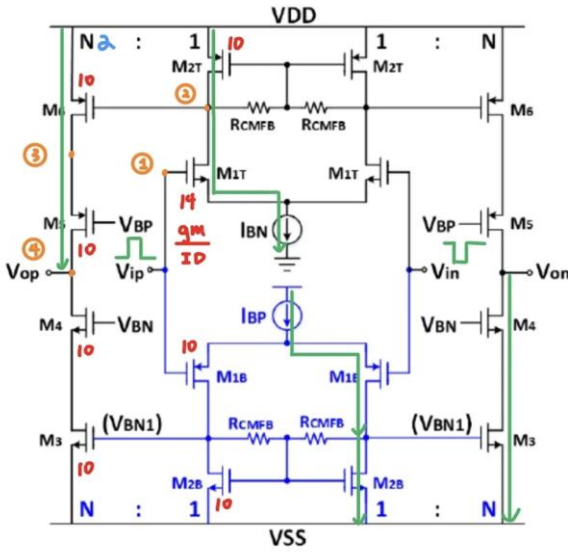


Fig. 3. Proposed dual inputs two stage amplifier architecture (D2SA)

• DC gain >50dB

• Total power must be limited to 5mWatts; reduce as much as possible the slew-rate and linear settling.

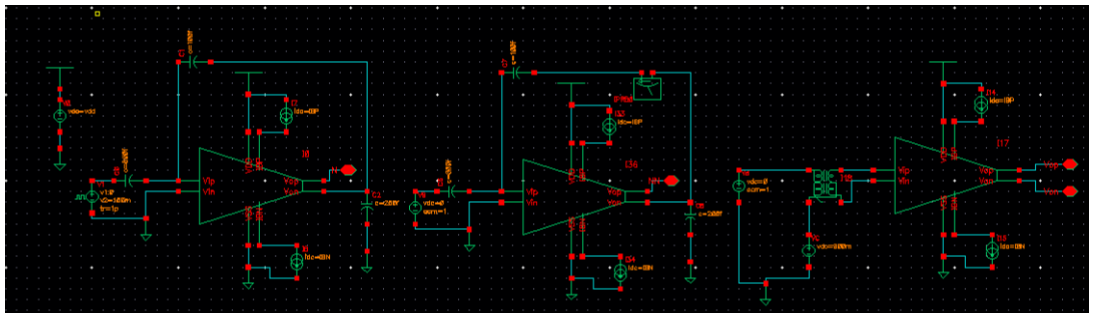
• C1=800fF, C2=100fF, CL=200fF; CP represents the parasitic capacitors of the amplifier and should not be added (CP=0).

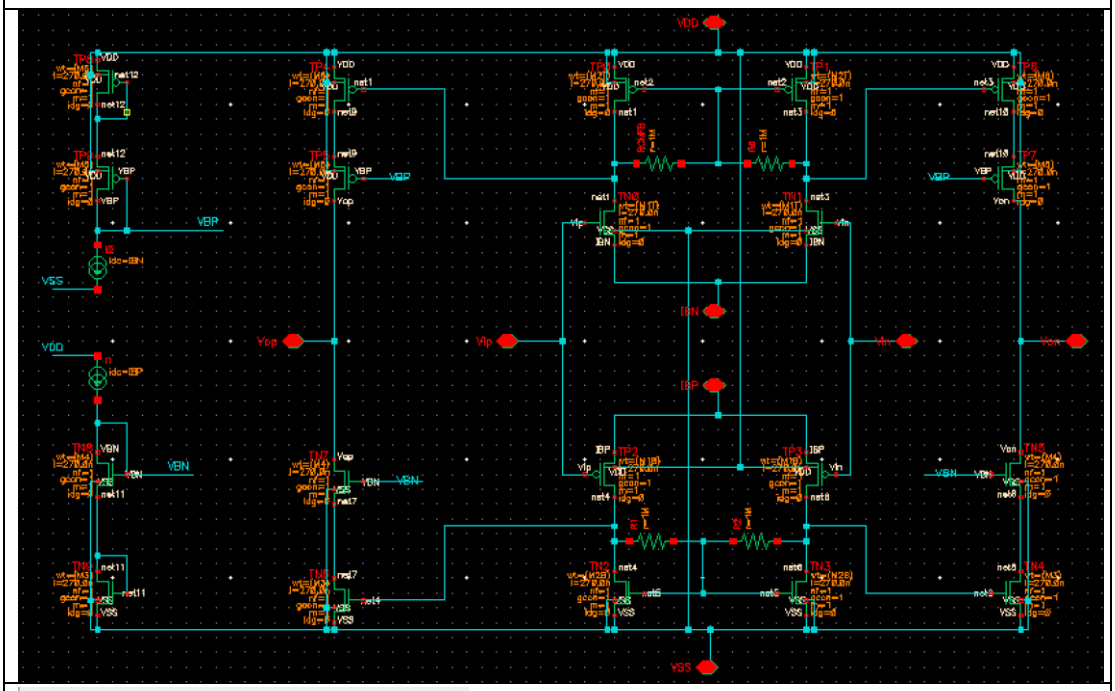
• The circuit must be fully differential, then a common-mode feedback engine must be included.

i) Measure the AC properties of the loop gain; do your best for the stabilization of architecture. Report the the magnitude and phase response and measure the phase and gain margin.

ii) Measure the 100mV step response. Report the steady state settling error and the 1% settling time.

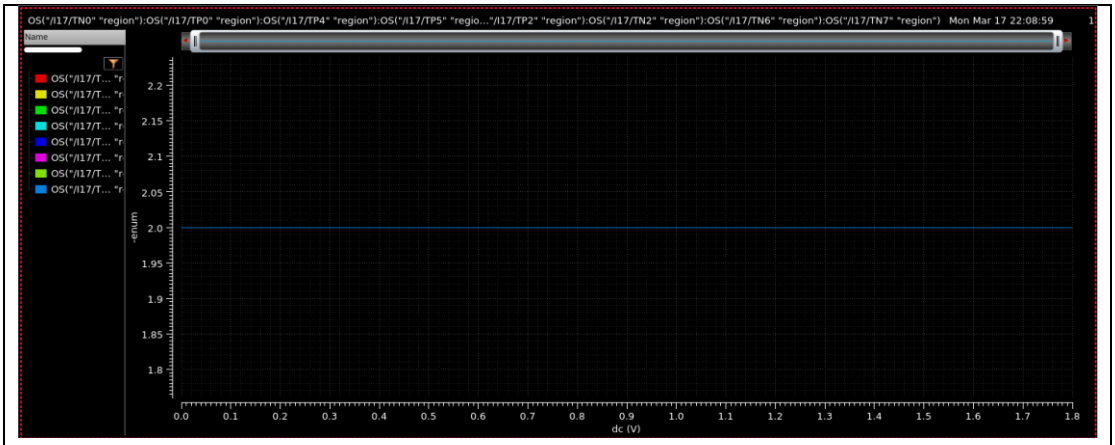
iii) Compare the results for this architecture and the ones obtained with the ring amplifier used in assignment 3.



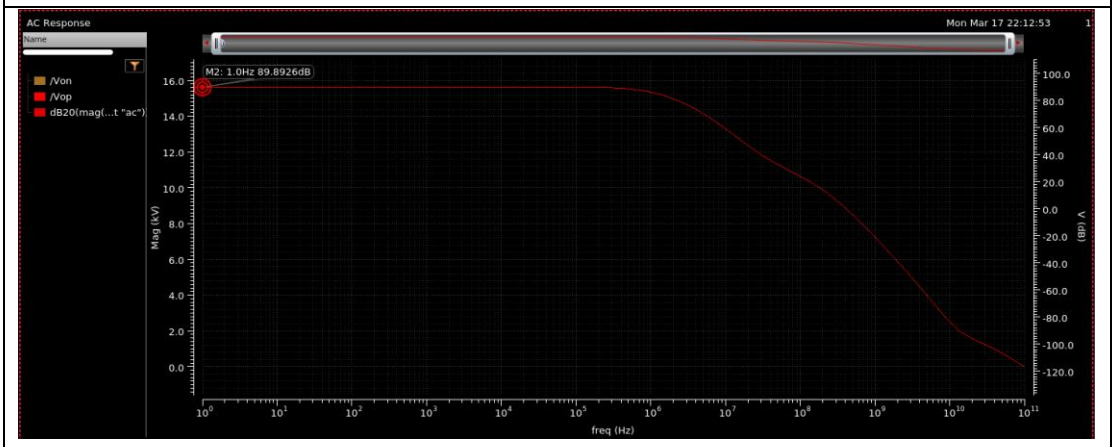


Design Variables

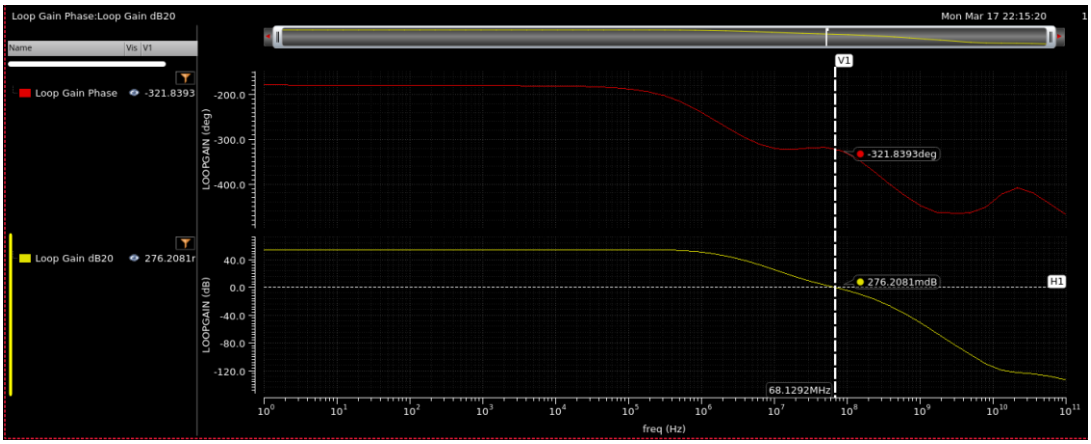
	Name	Value
1	vdd	1.8
2	IBN	1m
3	IBP	1m
4	M2T	368u
5	M1T	165u
6	M1B	368u
7	M2B	70.4u
8	M3	140.8u
9	M4	140.8u
10	M5	736u
11	M6	736u
12	p5vonly	0



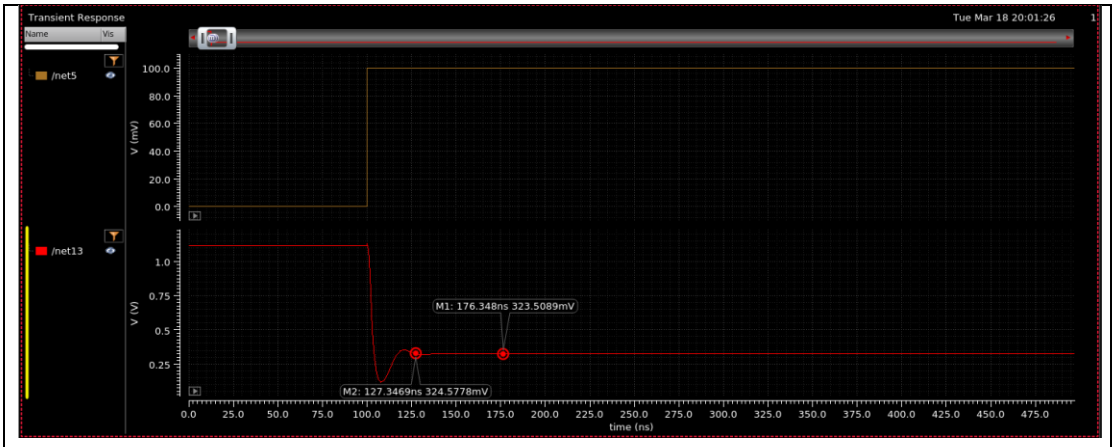
VCM range



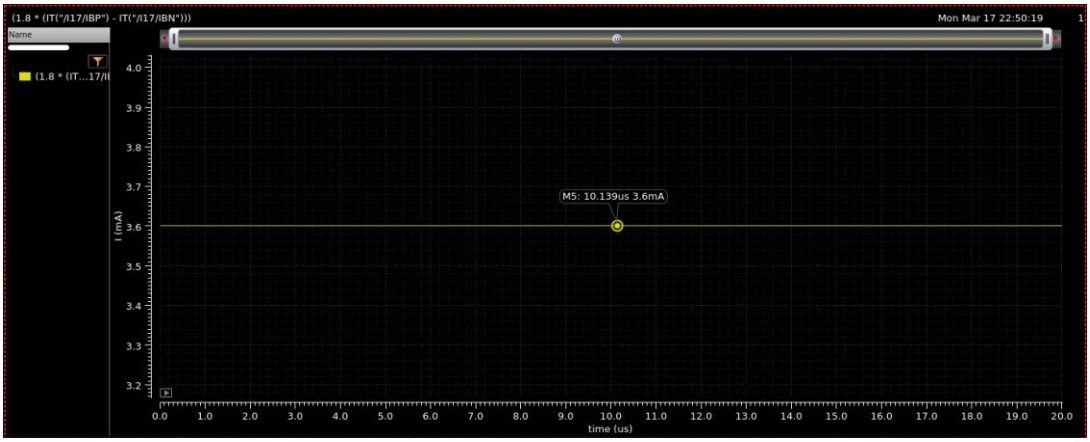
DC gain



PM: 39deg



Settle time: 127ns



Power:3.6mW

	D2SA	Ring amplifier
DC gain	89 dB	
Power	3.6mW	
Settle time	127ns	
PM	39 deg	

	D2SA	Ring Amplifier
Power Consumption	High power (static biasing)	Low power
Output Swing	Larger	smaller
Response Speed	Slower	Fast (suitable for high-speed applications)
Linearity	Higher	lower
	high-precision amplification	Low-power ADCs