25 Spring ECEN 607: Advanced Analog Circuit Tech

Design Post-lab Report

Lab2: Two-Stage Amplifier Design with 3𝜎 Driven Statistical Corner Extraction

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**Objectives:**

1. Design and simulate a two-stage Miller-compensated amplifier.

2. Observe the effect of voltage and temperature variations.

3. Verify the design with Monte-Carlo simulation.

**Design & results:**

1. Simulate the design from the prelab and adjust the transistor sizes accordingly until all specifications are met. Notice that most relevant transistors are M1=M2 and M8. Check the slides discussed lecture 01/30/2024.

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| * Vcm range the dc operation point (-0.9~-0.54) |
| * Output swing (under Vcm=-600m) 0.52-(-0.7)= 1.2 * Show the small range for Vd-linear because of the high gain and open loop |
| * Gain= 43dB, GBW=2.3M |
| * PM= Gain=1’s phase= 180-80.6 degree |

1. Plot and report (from simulations) the input referred noise density (what this does mean?) and find RMS voltage noise integrated in the band (10 Hz – 2 MHz).

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* In analog circuit design (such as op-amps and ADCs), the **input-referred noise density** represents all noise sources **referred back to the input**, making it easier to evaluate their impact on the signal.
* Input-Referred Noise Density= Total Output Noise Density / Gain ²
* **Top Curve (pV²/Hz)** → **Input-Referred Noise Density**

At **low frequencies (~10 Hz)**, noise is higher, which is mainly due to **1/f (Flicker) noise**.

At **high frequencies (~2 MHz)**, the noise density stabilizes, dominated by **thermal noise**.

* **Bottom Curve (nV)** → **Integrated RMS Noise**

**This curve represents the cumulative noise across the 10 Hz to 2 MHz band.**

**As frequency increases, total integrated noise accumulates**, leading to a higher noise voltage.

1. In addition, provide comparison tables of hand-calculated vs. final transistor sizes, and required specs (Table 1-1) vs. simulated specs. Comment on your results.

Due to the miscalculation of PM and didn’t consider about the Vcm range, I redesign the circuit into following size

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|  | Pre | Post |  | Pre | Post |
| Ibais | 20u | 20u | Av | 196 | 146 |
| Cc | 16p | 3p | GBW | 2.48M | 2.3M |
| M1 | 10u/0.18u | 2u/0.27u | PM | 60.18(mis) | 80 |
| M2 | 10u/0.18u | 2u/0.27u | Swing | 1.56 | 1.2 |
| M3 | 5u/0.18u | 2u/0.27u |  |  |  |
| M4 | 5u/0.18u | 2u/0.27u |  |  |  |
| M5 | 5u/0.18u | 2u/0.27u |  |  |  |
| M6 | 5u/0.18u | 1u/0.27u |  |  |  |
| M7 | 10u/0.18u | 10u/0.27u |  |  |  |
| M8 | 10u/0.18u | 20u/0.27u |  |  |  |

1. Plot the magnitude and phase response of your amplifier. Measure the phase margin and unity gain frequency from simulations.

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1. Simulate statistical simulation, Monte-Carlo, for GBW, Phase Margin and DC gain at least 200 points. Plot the histograms.

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1. Close the loop to implement a unity gain buffer (b factor =1) and measure the step response for an input step of 20mV. Report the results.

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1. Close the loop with two resistors of 100kΩ and/or larger to implement a 6dB gain inverting amplifier. Report the 250mV step response. Any ringing? Explain your results.

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* **PM > 60°** → Smooth response, minimal overshoot or ringing.
* **PM 30° ~ 60°** → Some overshoot and slight ringing.
* **PM < 30°** → Significant overshoot, potential sustained oscillation