ECEN 607: Advanced Analog Circuit Tech

Lab 4: Op Amp Design - I

Pre-lab or Lab Report

Name: FirstName LastName
UIN: ******Last Four Digits

Objectives

- To be able to identify the dominant noise sources.
- To study and design a single-ended telescopic op amp.

Recommendation:

Start building common testbench setups for finding op amp parameters such as DC Gain, unity gain frequency, slew rate etc. This can be re-used for different op-amps that you will be designing in this course and later, hence saving a lot of time.

Prelab

- **In this prelab, 5.5 V NFETs and PFETs will be used.**
- **Do not forget to show a detailed design procedure for each design.**
- **The following op amp must be tested in unity feedback configuration.**

Design the telescopic amplifier with output dominant pole shown in Fig. 2-2. Identify the dominant noise source and find the expression for the input referred noise due to the dominant noise sources. Show the hand-calculations for the input referred noise and report the estimated value.
The specifications are set in Table 2-2. Also, add the biasing circuit that generates Vb1 and Vb2, i.e. modify the circuit such that it presents just one current source (Ibias) and two voltage sources (VDD and VSS).

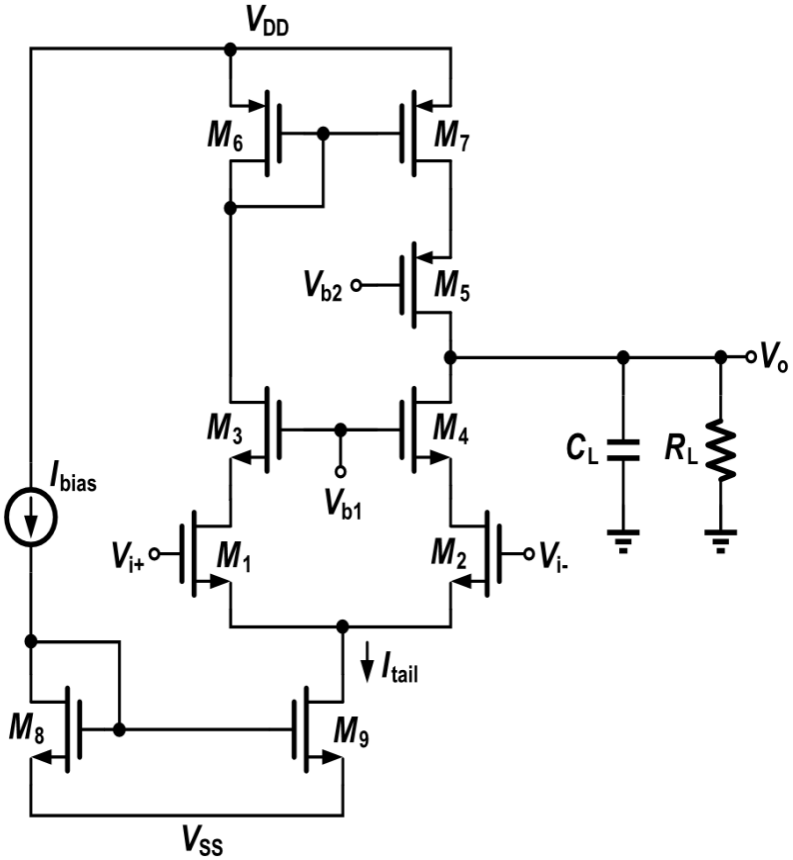

Figure 2-2: Telescopic single stage amplifier

Table 2-2: Design specifications

V_{DD}-V_{SS}	5.5 V
A_{v0}	> 70 dB
GBW	> 2 MHz
PM	> 45°
Output Swing @ gain>40dB	> 0.8 V
C_L	2 pF
R_L	100kΩ
Power Dissipated	< 300 µW
Input referred noise (10 Hz – 2 MHz)	<30 µVrms

Lab Report

Design:

1. Simulate the circuit from the prelab and adjust the transistor sizes accordingly until all specifications are met. Provide necessary plots such that you clearly show the specs are met. The output swing specification should be tested with a transient simulation.
2. Run a statistical simulation (Monte Carlos) and provide the worst-case DC Gain, GBW, Phase Margin and input referred noise. You do not have to adjust the design if the specs are not met. Comment the results.
3. Configure a unity-gain buffer and apply a differential pulse of 1 KHz, 0.4 Vpp. Show the screen shots and provide comments on the step response; 30% and 1% settling time? Ringing? Comment on the results.
4. Provide a comparison table of hand-calculated vs. final transistor sizes including the required specs vs. simulated specs.
5. Comment on your learning from this lab.