**ECEN-607: Advanced Analog IC Design**

**Assignment #4:**

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• DC gain >50dB

• Total power must be limited to 5mWatts; reduce as much as possible the slew-rate and linear settling.

• C1=800fF, C2=100fF, CL=200fF; CP represents the parasitic capacitors of the amplifier and should not be added (CP=0).

• The circuit must be fully differential, then a common-mode feedback engine must be included.

1. Measure the AC properties of the loop gain; do your best for the stabilization of architecture. Report the the magnitude and phase response and measure the phase and gain margin.
2. Measure the 100mV step response. Report the steady state settling error and the 1% settling time.
3. Compare the results for this architecture and the ones obtained with the ring amplifier used in assignment 3.

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| VCM range |
| DC gain |
| PM: 39deg |
| Settle time: 127ns |
| Power:3.6mW |

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| --- | --- | --- |
|  | D2SA | Ring amplifier |
| DC gain | 89 dB |  |
| Power | 3.6mW |  |
| Settle time | 127ns |  |
| PM | 39 deg |  |

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| --- | --- | --- |
|  | D2SA | Ring Amplifier |
| Power Consumption | High power (static biasing) | Low power |
| Output Swing | Larger | smaller |
| Response Speed | Slower | Fast (suitable for high-speed applications) |
| Linearity | Higher | lower |
|  | high-precision amplification | Low-power ADCs |