

# 25 Spring ECEN 610: Mixed-Signal Interfaces

## Lab5: Data Conversion Basics

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[https://github.com/Yu-HaoChen/TAMU\\_ECEN610\\_Mixed\\_signal/tree/main/lab5](https://github.com/Yu-HaoChen/TAMU_ECEN610_Mixed_signal/tree/main/lab5)

1. A 200mV rms value sinusoidal signal is applied to an ideal 12 bits ADC. The full range peak-to-peak voltage of the ADC is 1.2V.
  - a. Find the SNR of the ADC output.
  - b. Now the input sinusoidal is full range but comes with an additive Gaussian noise with standard deviation of 0.5 V. What is the SNR of the input signal? What is the SNR of the ADC output bits?
  - c. Repeat b assuming that the noise added to the sinewave is uniformly distributed with peak-to-peak value of 1V.

$$V_{FS} = 1.2$$

$$V_{FS \text{ rms}} = \frac{1.2^2}{2\sqrt{2}} \approx 0.424 \text{ V.}$$

$$\Delta = \frac{V_{FS}}{2^{12}} = 0.293 \text{ mV.}$$

$$(a). \quad V_{in \text{ rms}} = 0.2 \text{ V.}$$

$$P_{\text{signal}} = (0.2)^2 = 0.04$$

$$P_q = \frac{\Delta^2}{12} = \frac{(0.293 \text{ m})^2}{12}$$

$$SNR = 10 \log \frac{P_{\text{signal}}}{P_q} = 67.5 \text{ dB}$$

$$(b). \quad V_{in} = 1.2 \text{ V.}$$

$$V_{in \text{ (rms)}} = 0.424 \text{ V.}$$

$$P_s = 0.424^2 \approx 0.18 \text{ V.}$$

$$\text{noise } \sigma = 0.5 \quad P_n = (0.5)^2 = 0.25$$

$$SNR = 10 \log \frac{P_s}{P_n} = -1.43 \text{ dB} \quad (\text{noise} > \text{signal})$$

$$\text{after ADC (quantization)} \quad P_q = \frac{(0.293 \text{ m})^2}{12} < 6^2$$

$$SNR \approx \text{same}$$

$$(c.) \quad V_{p-p} = 1$$

$$G = \frac{A}{\sqrt{3}} = \frac{0.5}{\sqrt{3}} = 0.2887$$

$$P_n = (0.2887)^2 = 0.08333$$

$$SNR = \frac{P_s (0.424)^2}{P_n} = 3.34 \text{ dB}$$

2. Assume that an ADC uses an oversampling factor  $K = f_s / (2B)$ , where  $f_s$  is the sampling rate and  $B$  is the signal bandwidth. Then  $K=1$  is Nyquist rate and  $K>1$  means oversampling. The quantization noise variance is  $\sigma_e = \Delta^2 / 12$  as we defined in

class for the additive noise model. As you may recall also, this noise is uniformly distributed and white, i.e. is flat in the frequency range  $[0, f_s/2]$ . Then the noise power spectral density will be  $\sigma_e/f_s$ , so the integral in the range  $[-f_s/2, f_s/2]$  is  $\sigma_e$ . Now assume that a perfect low-pass filter is used that selects the signal bandwidth  $B$  and rejects all the out of band noise. Find an expression for the output SNR of this oversampled ADC+low-pass filter combination.

$$\begin{aligned} \sigma_e^2 &= \frac{\Delta^2}{12} & \text{PSD } S_{ee}(f) &= \frac{\sigma_e^2}{f_s} \quad (\text{V}^2/\text{Hz}) \\ K &= \frac{f_s}{2B} & 2B &= \frac{f_s}{K} \\ \sigma_e^2 \text{ (in band)} &= \int_{-B}^B S_{ee}(f) df = \frac{\sigma_e^2}{f_s} \cdot 2B = \sigma_e^2 \cdot \frac{2B}{f_s} \\ &= \sigma_e^2 \cdot \frac{1}{K} \quad (\text{noise}) \\ \text{SNR}_{\text{out}} &= 10 \log \left( \frac{P_s}{\frac{\sigma_e^2}{K}} \right) \\ &= 10 \log K + 10 \log \frac{P_s}{\sigma_e^2} \\ \text{when } K &\rightarrow 2K \text{ SNR improve by } 3 \text{ dB} \end{aligned}$$

3. A 3-bit D/A converter were designed for an ideal LSB level of 100 mV. The following output voltages levels were measured for the real D/A for thee codes 000 to 111 respectively: -0.01V 0.105V 0.195V 0.28V 0.37V 0.48V 0.6V 0.75V a. Find the offset & full-scale error in units of LSBs b. Find the end-point ideal & actual gain in LSB/code and compute the gain error in LSB/code c. Find the end point corrected codes and compute DNL & INL for all the codes. d. What is the maximum DNL and INL?

$$3 \text{ bit} = 2^3 = 8 \text{ levels}$$

	ideal	real	
000	0.0V.	-0.01V.	ideal LSB = 100mV. = 0.1V.
001	0.1V.	0.105	VS ideal = 0.7 V.
010	0.2	0.195	
011	0.3	0.28	
100	0.4	0.37	
101	0.5	0.48	
110	0.6	0.6	
111	0.7	0.75	

(a.)

$$\text{offset} : V_{000}(\text{real}) - \text{ideal} = -0.01V. = -0.1 \text{ LSB}$$

$$\text{FS error} : V_{111}(\text{real}) - \text{ideal} = +0.05V. = +0.5 \text{ LSB}$$

(b.)

$$\text{Slope error} : \frac{V_{111}(\text{real}) - V_{000}(\text{real})}{7} = 0.108571 \text{ V/code}$$

$$\text{Gain error} : \frac{\text{slope error} - \text{LSB}(\text{ideal})}{\text{LSB}(\text{ideal})} = +0.0857 \text{ LSB/code}$$

(c.)  $V_{\text{end point}} = V_{000 \text{ (real)}} + k \times \text{slope error}$   
 $k = 0, 1, \dots, 7$

	VEP	INL (k)	$\frac{V(\text{real}) - \text{VEP}}{\Delta_{\text{ideal}}}$ (LSB)
000	-0.01	0	
001	0.0986	0.064	
010	0.2071	-0.121	
011	0.3157	-0.357	
100	0.4243	-0.543	
101	0.5329	-0.529	
110	0.6414	-0.414	
111	0.75	0	

	$V_k - V_{k-1}$	DNL (k)	$\frac{V_k - V_{k-1}}{\text{slope}} - 1$ (LSB)
001	0.115	0.059	
010	0.09	-0.171	
011	0.085	-0.217	
100	0.09	-0.171	
101	0.11	0.013	
110	0.12	0.105	
111	0.15	0.382	

(d.)

DNL (max) = 0.382 LSB  $k=7$

INL (max) = 0.543 LSB  $k=4$

4. A ramp histogram is used to characterize a 4-bit ADC, the following vector is found:  
 43 115 85 101 122 170 75 146 125 60 95 95 115 40 120 242 I suggest you do this in Matlab: a.) Calculate the DNL and INL b.) What are the peak DNL and INL values? c.) Is this ADC monotonic? Hint: Recall that you use as a reference the straight line that connects the end points of the transfer function provided by the histogram. This is needed to eliminate offset errors and full scale errors. There is a trivial way to eliminate these errors. How?

=== 4-bit ADC Histogram Linearity ===

Total samples : 1749  
Ideal counts / code : 109.3125

Code	Counts	DNL (LSB)	INL (LSB)
0	43	-0.607	-0.607
1	115	0.052	-0.555
2	85	-0.222	-0.777
3	101	-0.076	-0.853
4	122	0.116	-0.737
5	170	0.555	-0.182
6	75	-0.314	-0.496
7	146	0.336	-0.160
8	125	0.144	-0.017
9	60	-0.451	-0.468
10	95	-0.131	-0.599
11	95	-0.131	-0.730
12	115	0.052	-0.678
13	40	-0.634	-1.312
14	120	0.098	-1.214
15	242	1.214	0.000

Results:

Peak |DNL| = 1.214 LSB

Peak |INL| = 1.312 LSB

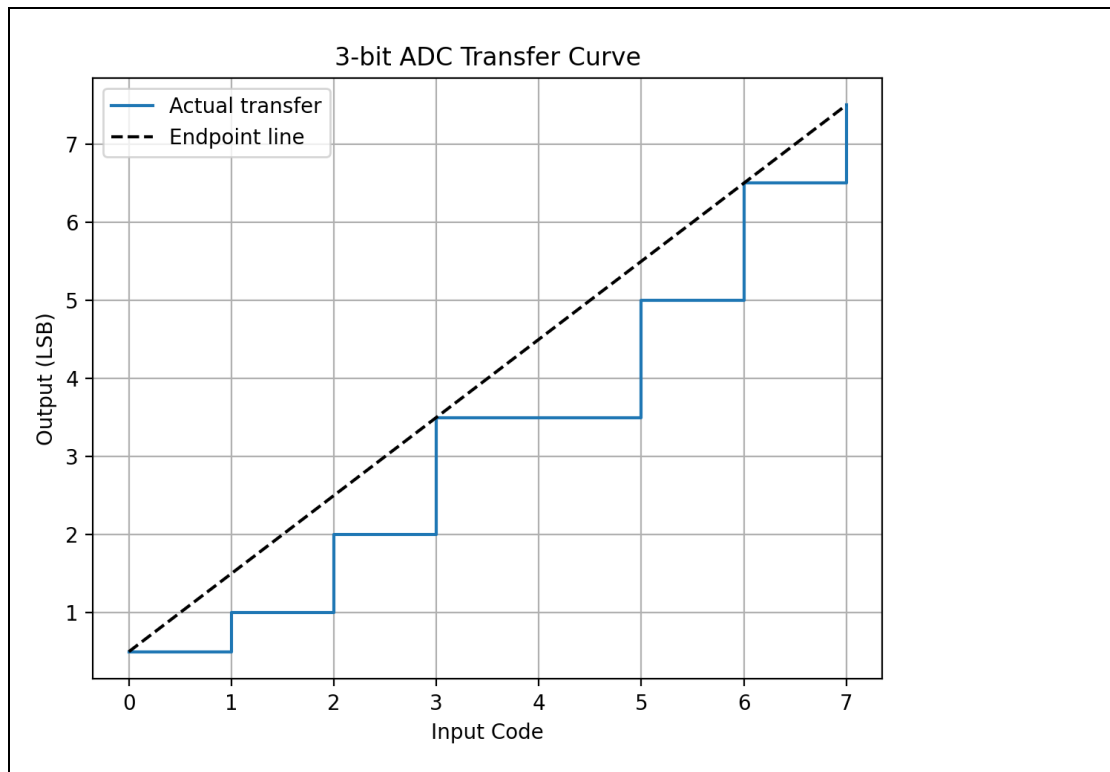
Monotonic : YES

5. The end point DNL for a 3-bit ADC is measured to be: DNL: 0 -0.5 0 +0.5 -1 +0.5 +0.5 0 (all numbers in terms of LSB) The ADC exhibits offset and full-scale error: Offset error = +0.5LSB Full scale error = +0.5LSB a) Find the INL for this ADC b) Draw the transfer curve of this ADC.

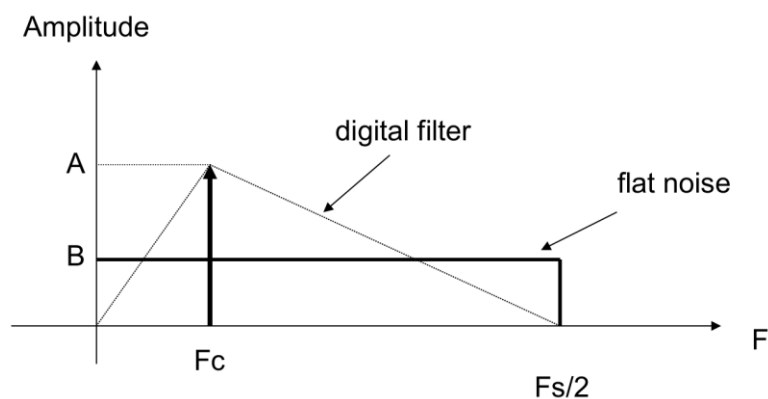
3-bit ADC Linearity Analysis:

Code	DNL (LSB)	Actual V (LSB)	INL (LSB)
0	0.00	0.50	0.00
1	-0.50	1.00	-0.50
2	0.00	2.00	-0.50
3	0.50	3.50	0.00
4	-1.00	3.50	-1.00
5	0.50	5.00	-0.50
6	0.50	6.50	0.00
7	0.00	7.50	0.00

Peak |INL| = 1.00 LSB



6. A tone at frequency  $F_c$  is sampled at frequency  $F_s$  and quantized with  $N$  bits. The resulting quantization noise is white (flat in frequency, see the figure). a. (5%) What is the peak (full scale) signal to quantization noise ratio  $SQNR(dB)$ ? b. (25%) Assume that an  $L$  point DFT of the sampled tone is calculated and plotted in a linear scale. Assume that resultant noise floor is perfectly flat. From the range  $[0 \pi]$  of the DFT plot, the linear  $SNQR$  is calculated as the power of the sinewave frequency bin divided by the power of all the other bins. What is the height difference in dB between the sinewave frequency bin and the noise floor? c. (5%) What are necessary conditions in the previous problem for the DFT noise to be flat? Are these conditions sufficient for the noise to be completely flat? d. (25%) The digital filter shown in the figure is used to filter out the signal from the quantization noise. What is the  $SNR$  at the output of the filter?



(a.)

$$SNR = 6.02 N + 1.76$$

(b.)

$$[0, \pi] \rightarrow \frac{L}{2} \text{ bin}$$

$$\text{single bin SNR} \frac{P_{\text{sin}}}{P_{q, \text{bin}}} = SNR \times \frac{L}{2}$$

$$\Delta \text{dB} = 10 \log(SNR) + 10 \log\left(\frac{L}{2}\right) \approx (6.02N + 1.76) + 10 \log \frac{L}{2}$$

### Necessary conditions

1. **White noise:** quantisation error must be i.i.d. and spectrally white.
2. **Coherent sampling & rectangular window:** prevents spectral leakage that would otherwise tilt the floor.
3. **Large LLL** (or sufficient averaging): so the statistical fluctuations of each bin average out.

$$H(x) = \begin{cases} \frac{x}{\alpha} & 0 \leq x \leq \alpha \\ \frac{1-x}{1-\alpha} & \alpha \leq x \leq 1 \end{cases}$$

(d.) by a L.P.F.

$$SNR_{\text{out}} = (6.02N + 1.76) + 10 \log(3)$$

$$H(f) = \begin{cases} \frac{f}{F_c} & 0 \leq f \leq F_c \\ \frac{\frac{F_s}{2} - f}{\frac{F_s}{2} - F_c} & F_c \leq f \leq \frac{F_s}{2} \end{cases}$$

$$\alpha = \frac{F_c}{\frac{F_s}{2}} \quad x = \frac{f}{\frac{F_s}{2}}$$

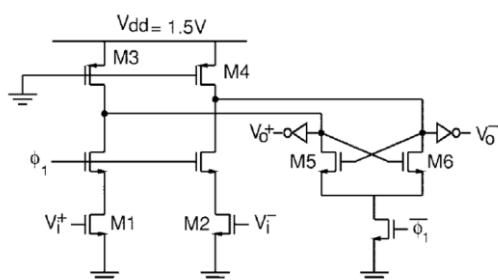
$$P_{q, \text{out}} = N_0 \frac{F_s}{2} \int_0^1 H(x)^2 dx$$

$$= N_0 \frac{F_s}{2} \times \frac{1}{3}$$

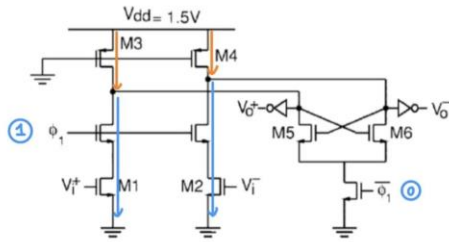
$$SNR_{\text{in}} = \frac{P_{\text{sin}}}{P_q}$$

$$SNR_{\text{out}} = \frac{P_{\text{sin}}}{P_{q, \text{out}}} = SNR_{\text{in}} \times 3$$

7. Consider the preamplifier/latch topology below. (a) Please explain the circuit dynamics for  $1\Phi$  and  $1\Phi$ . Clearly indicate the region of operation of the transistors (i.e., OFF, triode, saturation) (b) Find an expression of the input vs the output that takes into account the gains and the positive regeneration of the circuit. (c) Explain the advantages and disadvantages between dynamic and static latches? (d) Is this latch a static, dynamic or a semi-dynamic latch? Why?







(a.)  $\phi_1$  high : M1 & M2 sat  
M3 & M4 tri  
M5 & M6 off

$\overline{\phi_1}$  high : M1 & M2 off  
M3 & M4 tri  
M5 & M6 sat

$$A_{pre} = \frac{V_{od}(t_0)}{V_{id}} \approx \frac{g_{m1}}{g_{ds3} + g_{ds4}}$$

$$\frac{dV_{od}}{dt} = \frac{g_{m5} + g_{m6}}{C_L} V_{od} \quad V_{od}(t) = V_{od}(t_0) e^{-\frac{t}{\tau}}$$

$$\tau = \frac{C_L}{g_{m5} + g_{m6}}$$

$$V_{od}(t) = A_{pre} e^{-\frac{t}{\tau}} V_{id}$$

c.

Dynamic latch	Static latch
Very fast, no static power, small area	Slightly slower (extra devices), static power through loads
Charge on internal capacitors (dynamic node)	Cross-coupled feedback holds state indefinitely
Careful clocking, race and kick-back noise issues	Simpler timing, but consumes more head-room

d.

The outputs are **pre-charged to  $V_{DD}$  every  $\phi_1 = 0$  phase** by the always-on PMOS loads, i.e. they do **not keep their state once the clock returns to the reset phase**. The decision is made only while  $\phi_1$  is high, and the result must be captured by a following stage before the next reset

It combines a dynamic pre-charge **and** a static-like cross-coupled pair during evaluation

Semi-dynamic