25 Spring ECEN 610: Mixed-Signal Interfaces

Lab4: Sampler Error Modeling and Correction

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<https://github.com/Yu-HaoChen/TAMU_ECEN610_Mixed_signal/tree/main/lab4>

1. First order model of a ZOH sampling circuit Construct a model for a sampling circuit shown in Fig. 1.

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When the NMOS switch M1 is ON (Vsw = 1), the sampling circuit behaves as a series RC circuit and the input Vin is sampled on the capacitor. When the switch turns OFF (Vsw = 0), the voltage on the capacitor is held constant until the beginning of the next sampling phase. If the ON resistance of the switch is R, then the time constant of the sampler, τ, is R\*C.

1. For an input sinusoidal signal of frequency 1 GHz, a sampling frequency of 10 GHz and time constant of 10 ps, plot the output of the sampling circuit.

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1. Sampling Error Sampling error is the difference between an ideally sampled signal (delta train) and a signal sampled with a finite time constant sampling circuit.
2. Assume a NRZ (Non Return to Zero) input of amplitude 0.5 V and data rate of 10 Gb/s. Sample the input signal once in the middle of every bit period. Assuming a 50% duty cycle for Vsw in Fig. 1, what should the time constant be for the maximum sampling error to be less than 1 LSB for a 7-bit ADC with a full scale range of 1 V. Justify with an equation the obtained time constant value.

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1. Assume a multi-tone signal input with frequencies of 0.2 GHz, 0.58 GHz, 1 GHz, 1.7 GHz and 2.4 GHz and a sampling frequency of 10 GHz. What should the time constant be for the sampling error to be less than 1 LSB for a 7-bit ADC? Is it different from the time constant in 2.a? Why?

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* For NRZ signals, although there is no concept of frequency, the data rate of 10 Gb/s determines the duration of each bit (100 ps), and the charging time is about 50 ps (because of the 50% duty cycle).
* For multi-audio signals, the impact of each frequency component (especially the highest frequency component) on the RC charging error needs to be considered.

1. Sampling Error Estimation Construct an ADC model by adding an N-bit quantizer (N=7) at the output of the sampling circuit.
2. Let the input to the ADC be the multitone signal generated in 2.b. At the ADC output, find the error, E, between the quantized signal sampled with a sampling circuit having the time constant derived 2.a and an ideally sampled signal. What is the variance of E? What is ratio of the variance of E to the variance of the uniform quantization noise?

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1. In this model, the ADC output at time instant i has both a sampling error and a quantization error. Using least squares estimation, construct an M-tap FIR filter that estimates the sampling error at the ADC output using M-1 previous ADC output values. Add the estimated error to the ADC output and compute the error signal, E, defined in 3.a. Plot the ratio of the variance of E to the variance of uniform quantization noise as M is varied from 2 to 10. What do you infer from this plot?

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* After using FIR filter (tap number from 2 to 10) for error compensation, as the tap number increases, the compensated sampling error can be significantly reduced, and the total error variation can approach the lower limit determined only by quantization noise. This shows that the use of digital post-compensation technology can effectively compensate for the errors caused by finite time constants in the RC sampling circuit.

4. Calibration of Errors in a Two-Channel TI-ADC

a. Construct a simulation of a 2-way TI-ADC that includes time, offset and bandwidth mismatches between the channels. Provide SNDR plots following the setup in 2(a) for the design of the input signal.

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b. Construct a calibration technique capable of compensating the time, offset and bandwidth mismatches between the channels following the techniques described in the references.

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* Appendix

Q1

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Q4

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