

24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab1: Introduction to Cadence and MOS Device
Characterization

Name: Yu-Hao Chen

UIN:435009528

Section:601

Professor: Aydin Karsilayan

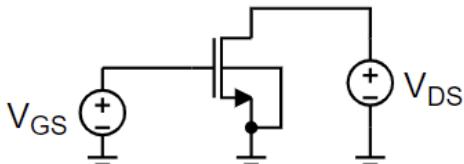
TA: Troy Buhr

Description:

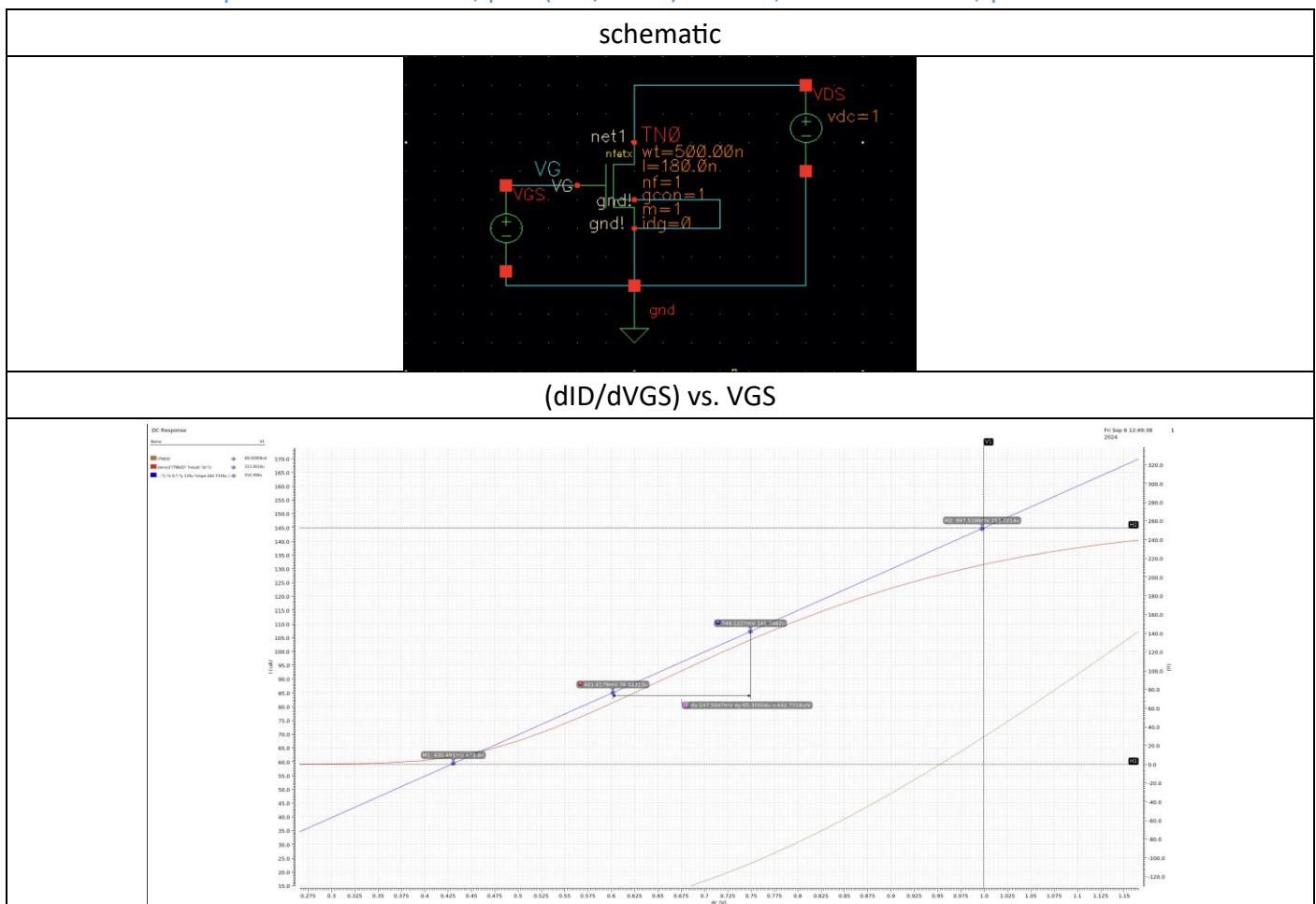
In this lab, we learn how to use Cadence Virtuoso to plot and measure some basic characteristics of the different parameters (W/L, finger) of NMOS and PMOS. Generating the waveform plot and examine the result.

Design & result

- Construct the circuit below using nfetx transistor with W/L=0.5μ/0.18μ using 1 finger.



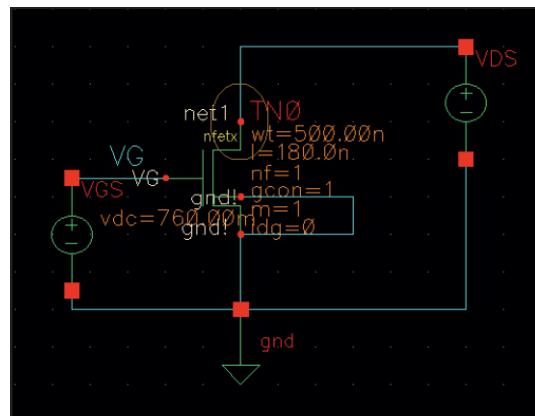
- $V_{DS}=1V$. Sweep V_{GS} from 0 to 1.8V, plot $(dID/dVGS)$ vs. V_{GS} , and extract V_{tn} , $\mu nCox$ and θ .



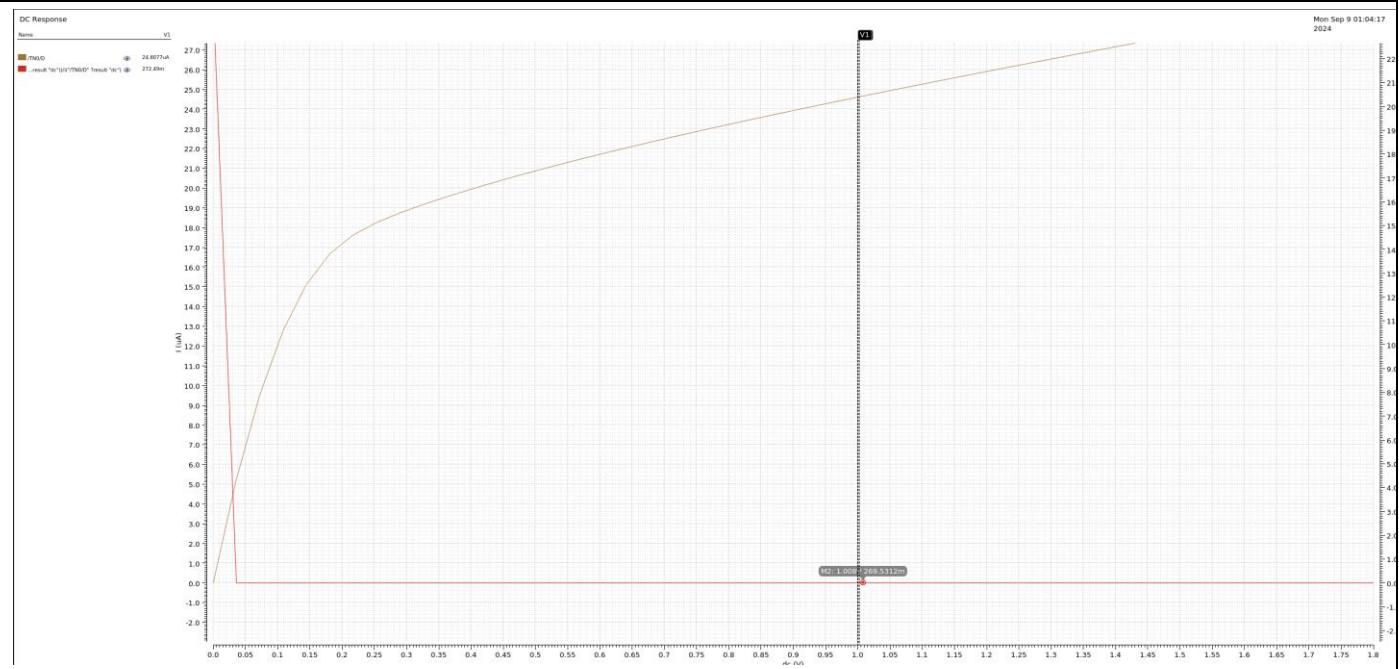
- The red line equals to $(dID/dVGS)$, and by selecting two points on the red line we can approximately get the tan of red line, which is represent in blue line.
- By finding the intersection point of the blue line and the minimum horizon line of the red line, we can find the V_{th} which is $V_{th}=0.43V$
- By finding the slope of the red line, which is blue line, we can get the $\mu nCox * W/L = 442.731 \mu A/V$, while $W/L = 0.5\mu/0.18\mu$, $\mu nCox = 159.83 \mu A/V$
- By finding the intersection point of the blue line and the maximum horizon line of the red line, we can find the $V_{th} + (1/2\theta)$, and θ will be $\theta = 0.881$

- b. $VGS = Vtn + 50mV + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $VDS=1V$. Additionally, find the unity-gain frequency (f_t) using AC simulations.

schematic

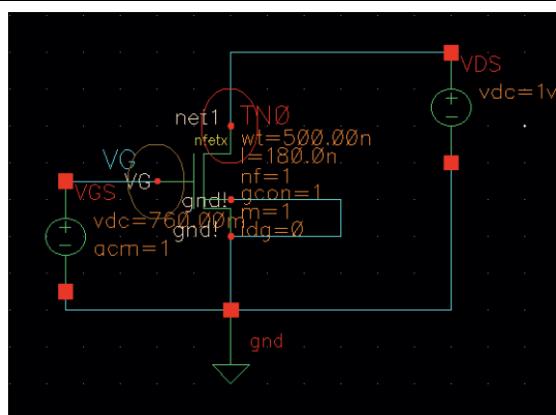


$(dID/dVDS)/ID$ vs. VDS

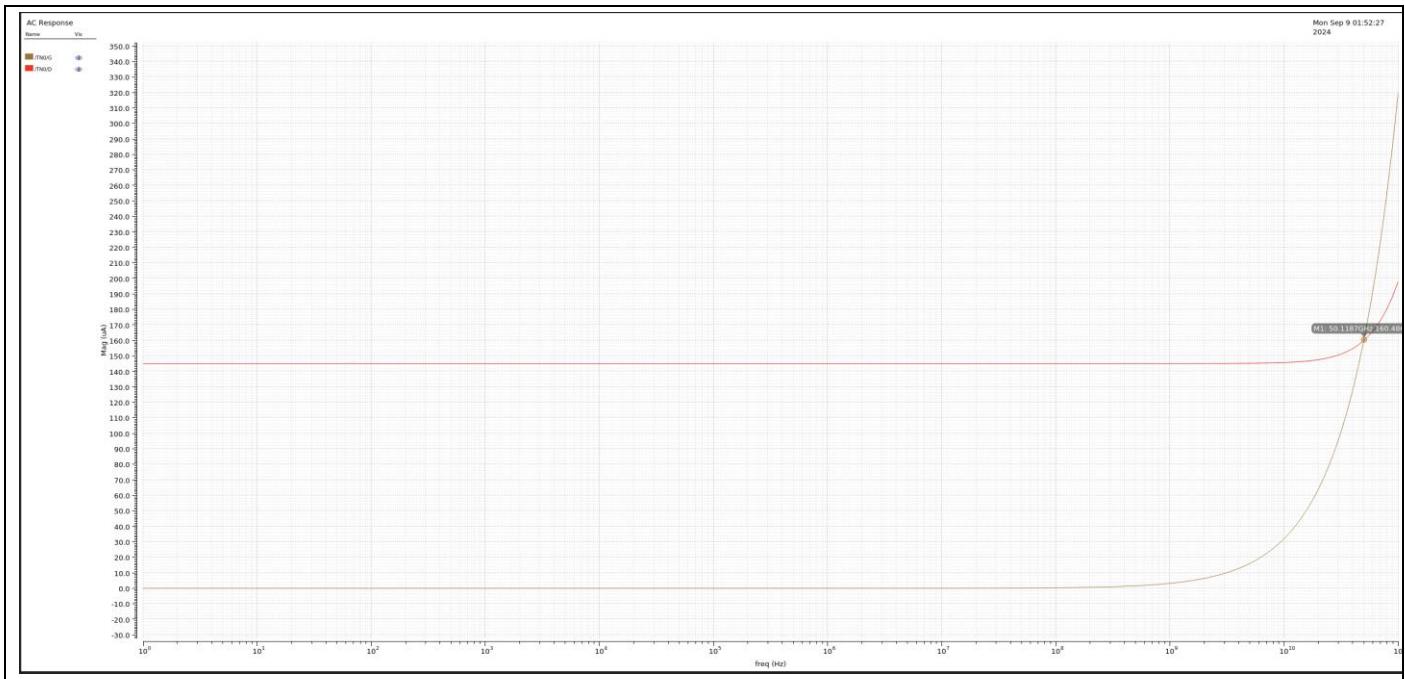


- The brown line = ID vs VDS (0-1.8) and red line = $(dID/dVDS)/ID$ vs. VDS
- When $VGS = Vtn + 50mV + 1/(4\theta) = 0.76V$ and $VDS = 1V$, the point $y = 269.5312m = \lambda/1+\lambda VDS$, which $VDS = 1$, so $\lambda = 0.367$

schematic

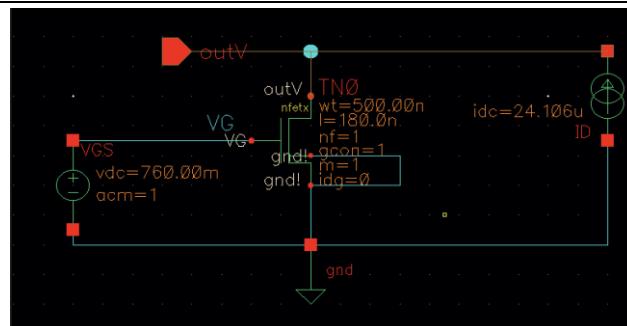


(AC) IG&ID vs Freq

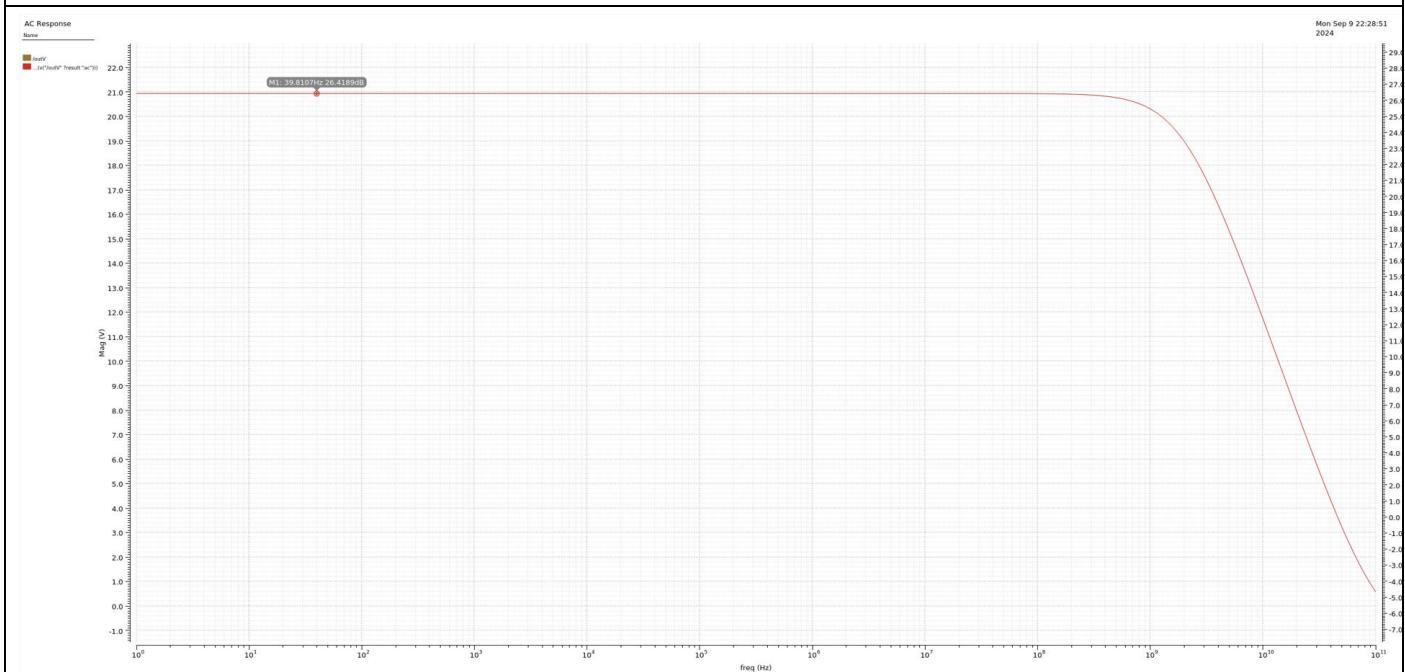


- Find the unity-Gain frequency (ft) using AC simulations. The brown line = IG, red line = ID
- We can get the ft when current gain=1 ,which is $IG=ID$ (the intersection), $ft=50.118\text{GHz}$
- c. Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations when $VDS=1\text{V}$ and $VGS=Vtn+50\text{mV}+1/(40)$.

schematic

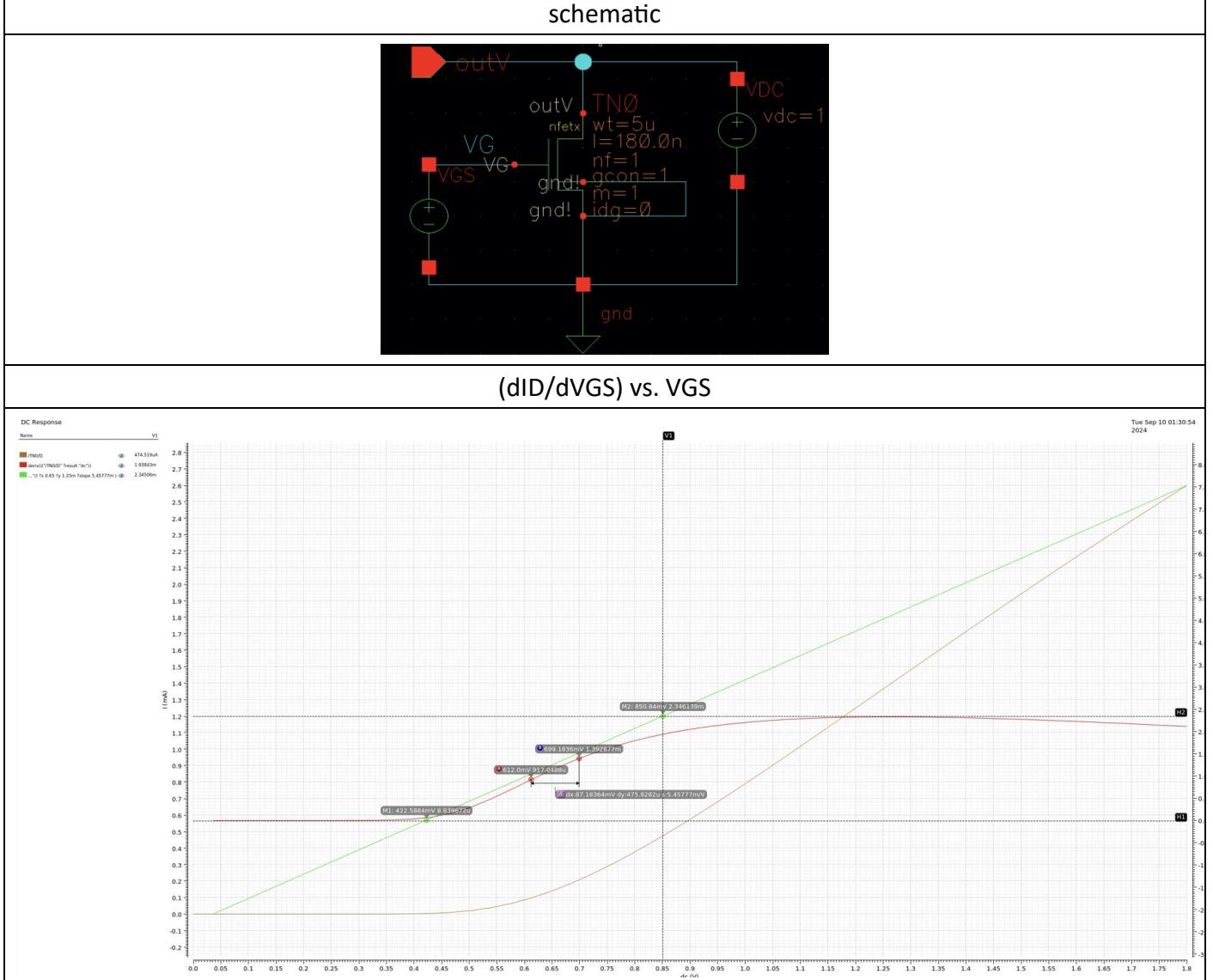


Vout(dB) vs freq



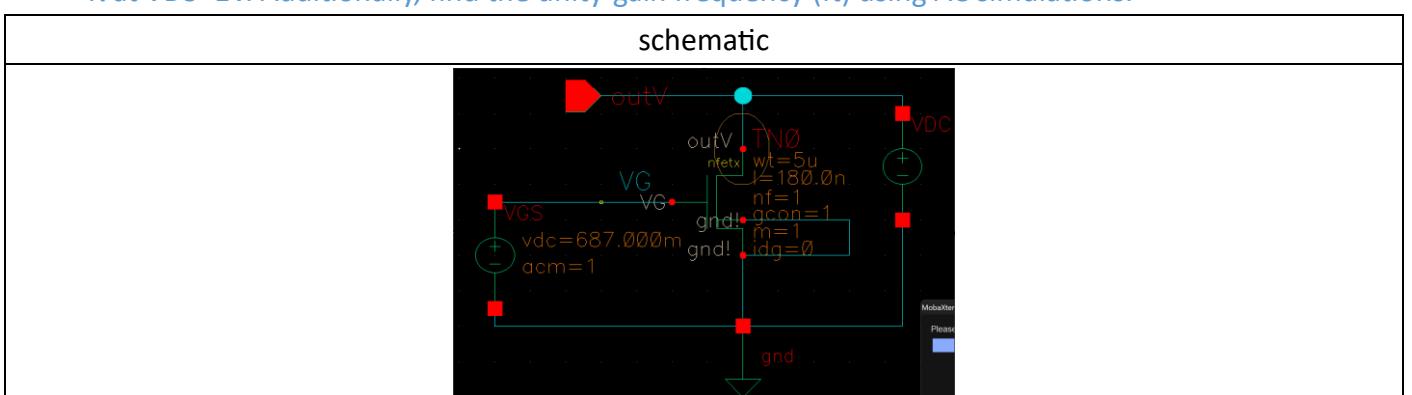
- Adding a current source (by square equation) which makes VDS close to 1V.
 $ID = 1/2 * \mu nCox * W/L (VGS - VT)^2$ [(1 + λ VDS) approximate 1] = $0.5 * 442.731u/V * (0.76 - 0.43)^2 * 1 = 24.106uA$
- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 26.418dB$
- 2. For the nfetx transistor with $W/L=5\mu/0.18\mu$ using 1 finger.

a. $VDS=1V$. Sweep VGS from 0 to 1.8V, plot $(dID/dVGS)$ vs. VGS , and extract V_{th} , $\mu nCox$ and θ .

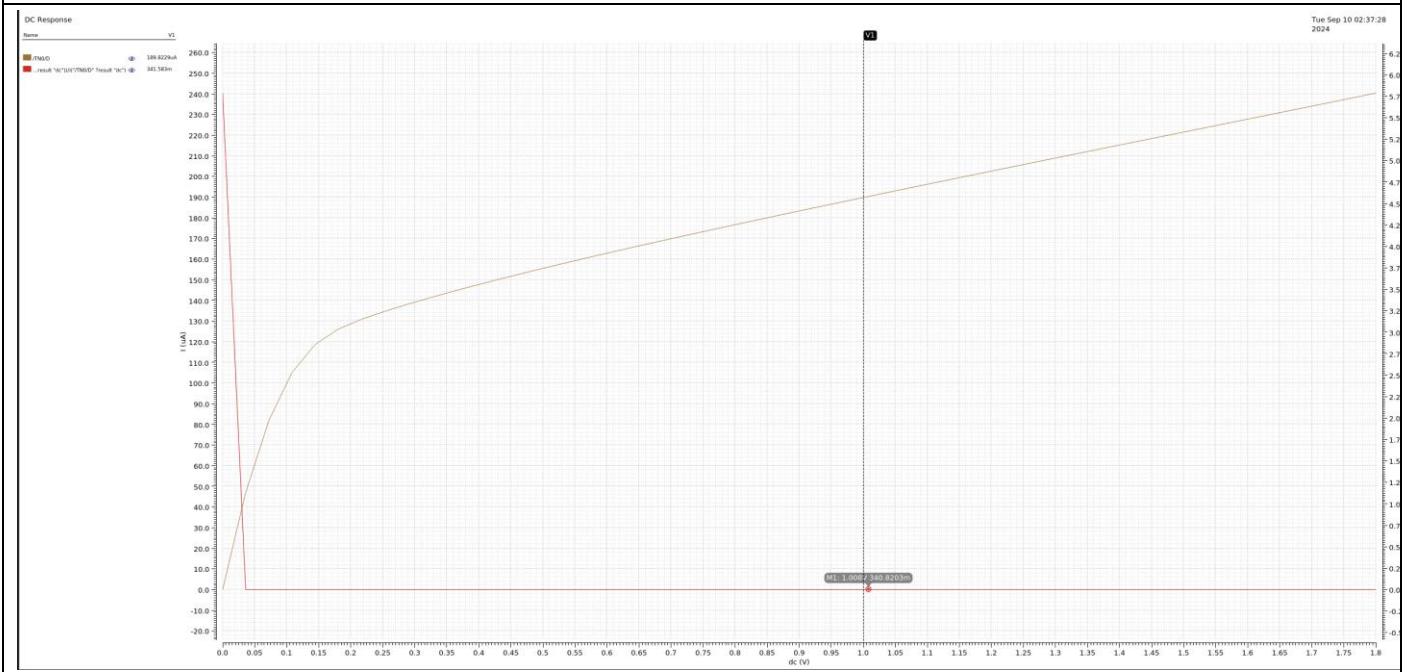


- $V_{th}=0.422V$
- $\mu nCox * W/L = 5.45777m/V$, while $W/L=5\mu/0.18\mu$, $\mu nCox=202.13u/V$
- $V_{th}+(1/2\theta)=850.84mV$, and θ will be $\theta=1.16$

b. $VGS=V_{th}+50mV+1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $VDS=1V$. Additionally, find the unity-gain frequency (f_t) using AC simulations.

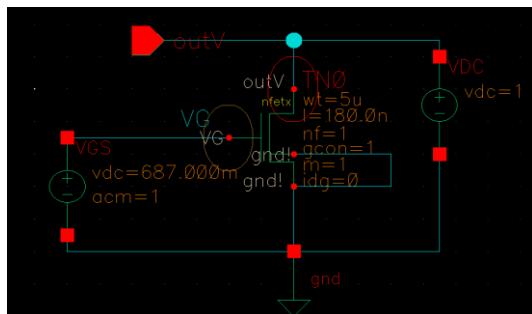


(dID/dVDS)/ID vs. VDS

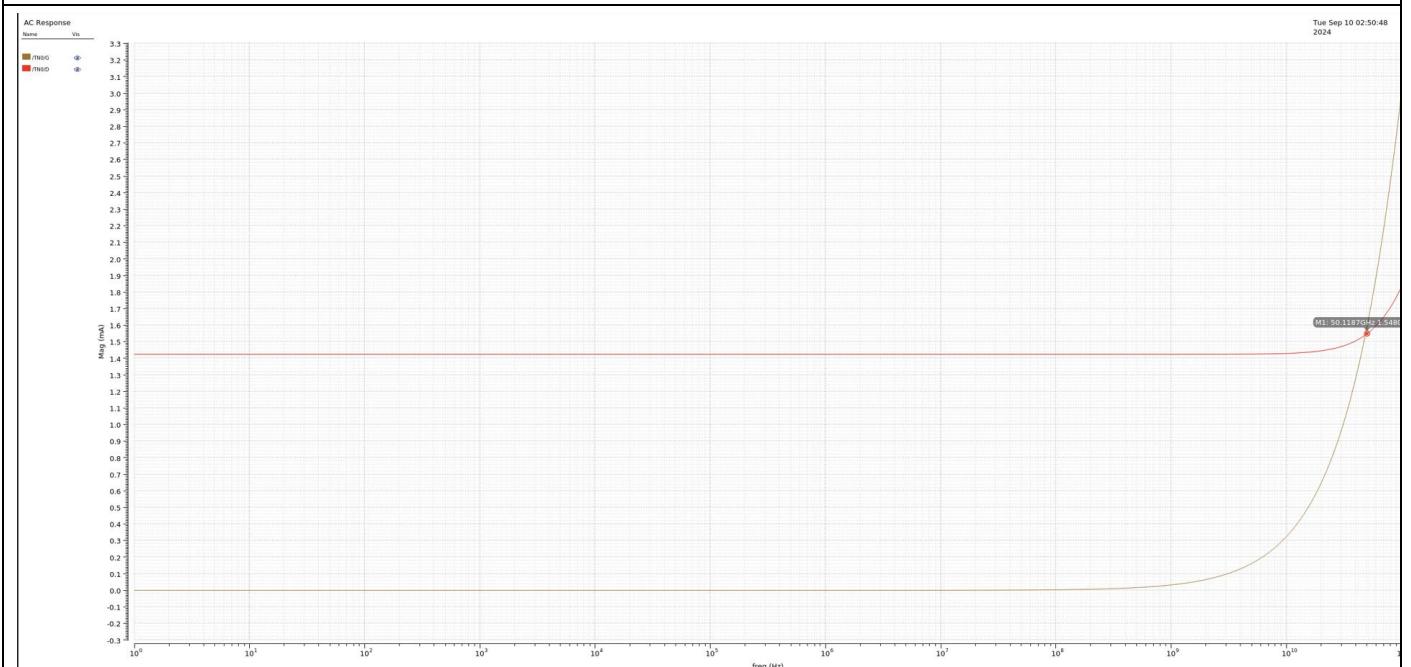


- When $VGS = V_{tn} + 50mV + 1/(4\theta) = 0.687V$ and $VDS = 1V$, the points $y = 340.82m = \lambda/1+\lambda VDS$, which $VDS = 1$, so $\lambda = 0.515$

schematic

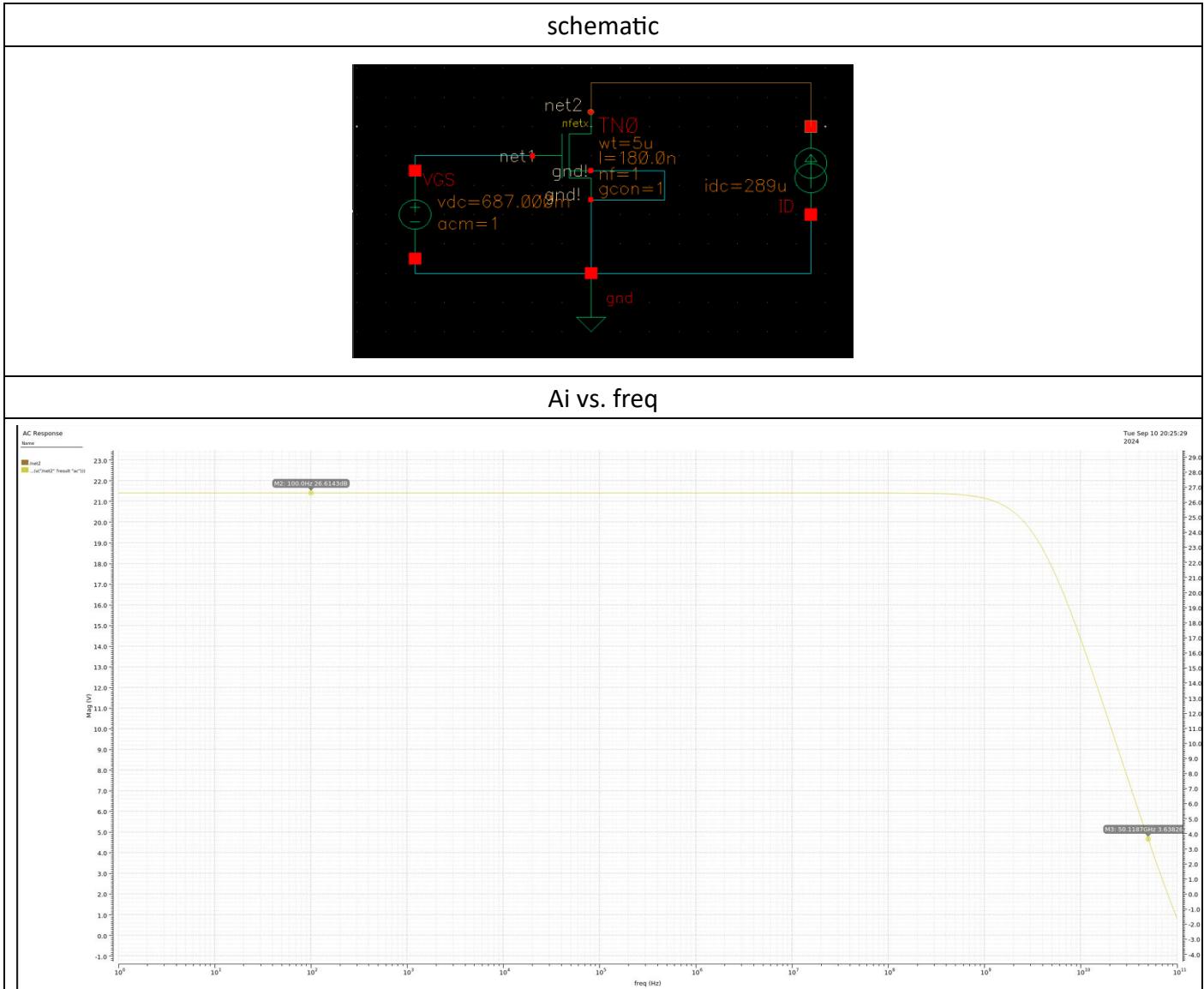


(AC) IG&ID vs Freq



- We can get the f_t when current gain=1 ,which is $IG=ID$ (the intersection), $f_t=50.118GHz$
 - Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations

when $V_{DS}=1V$ and $V_{GS}=V_{tn}+50mV+1/(4\theta)$.

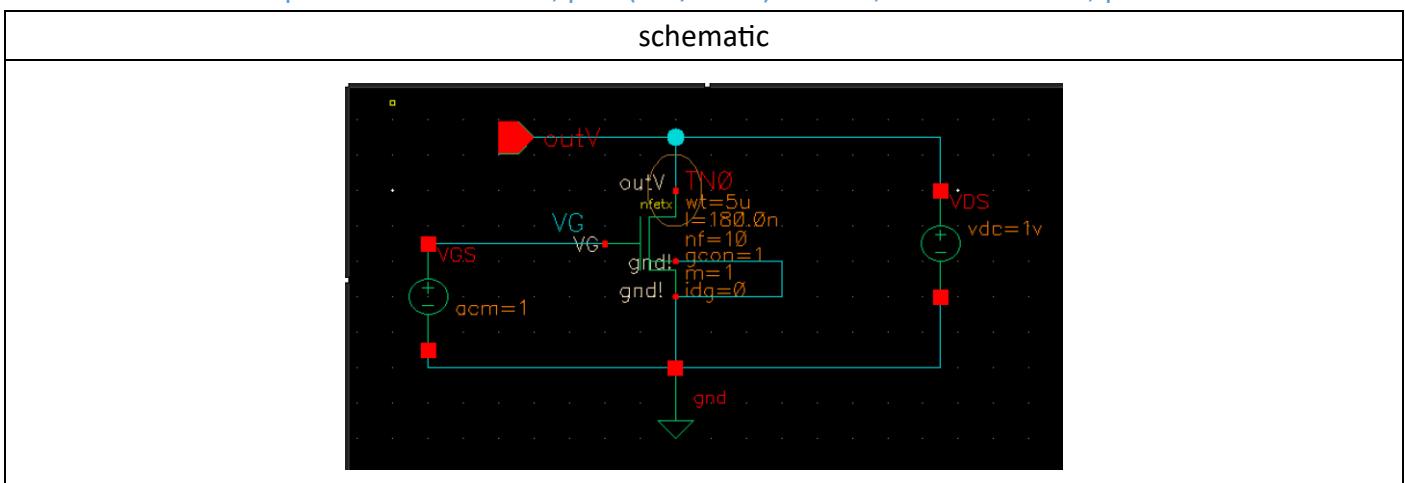


- Adding a current source (by square equation) which makes VDS close to 1v.

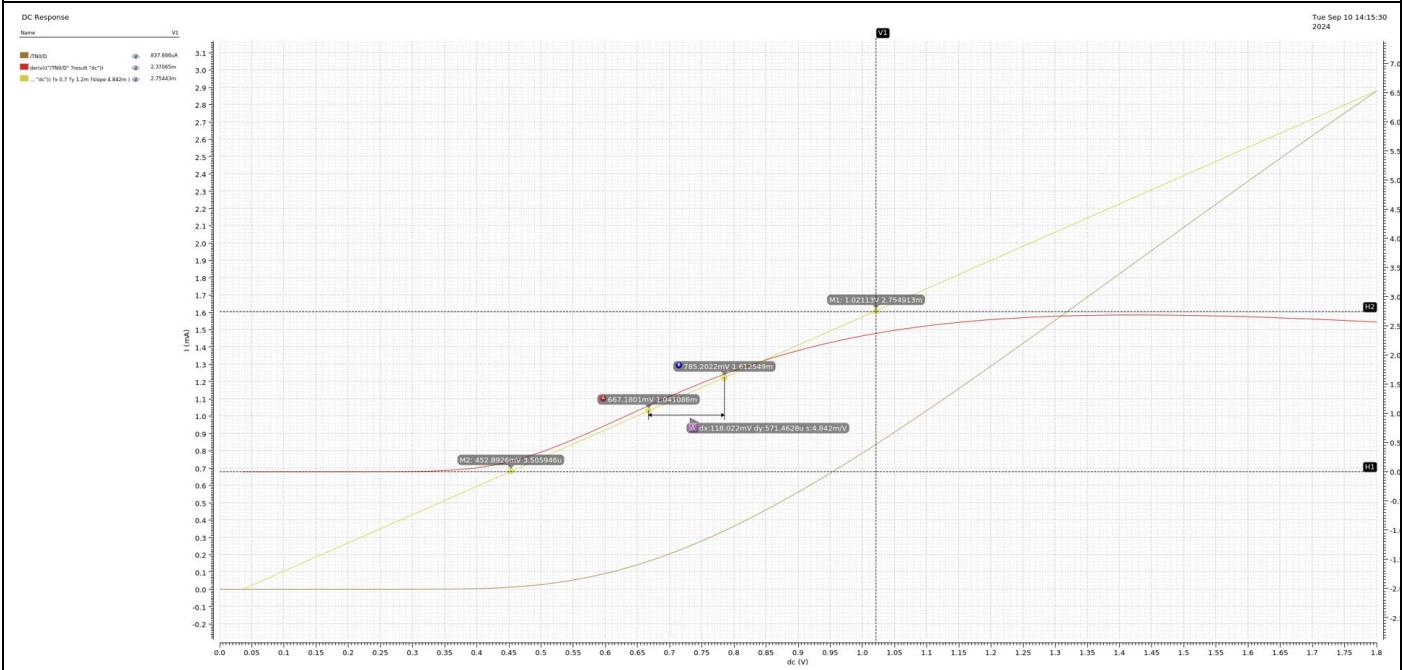
$$ID = \frac{1}{2} \mu nCox * W/L (VGS - VT)^2 (1 + \lambda VDS) = 0.5 * 5457.77 u/v * (0.687 - 0.422)^2 * (1 + 0.515) = 289 uA$$
 - By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 26.614 \text{dB}$

3. Repeat (1) for the nfetx transistor with $W/L = 5\mu/0.18\mu$ using 10 fingers (i.e. “width all fingers” = 5μ while “width single finger” = 0.5μ).

a. $VDS = 1V$. Sweep VGS from 0 to 1.8V, plot $(dID/dVGS)$ vs. VGS , and extract V_{tn} , $\mu nCox$ and θ .



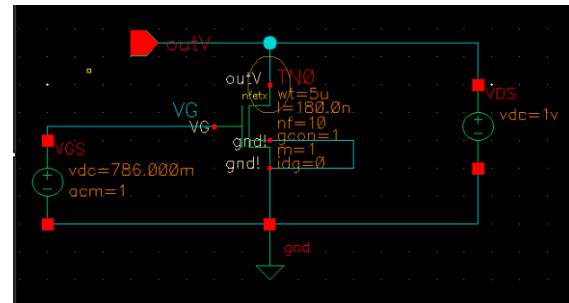
(dID/dVGS) vs. VGS



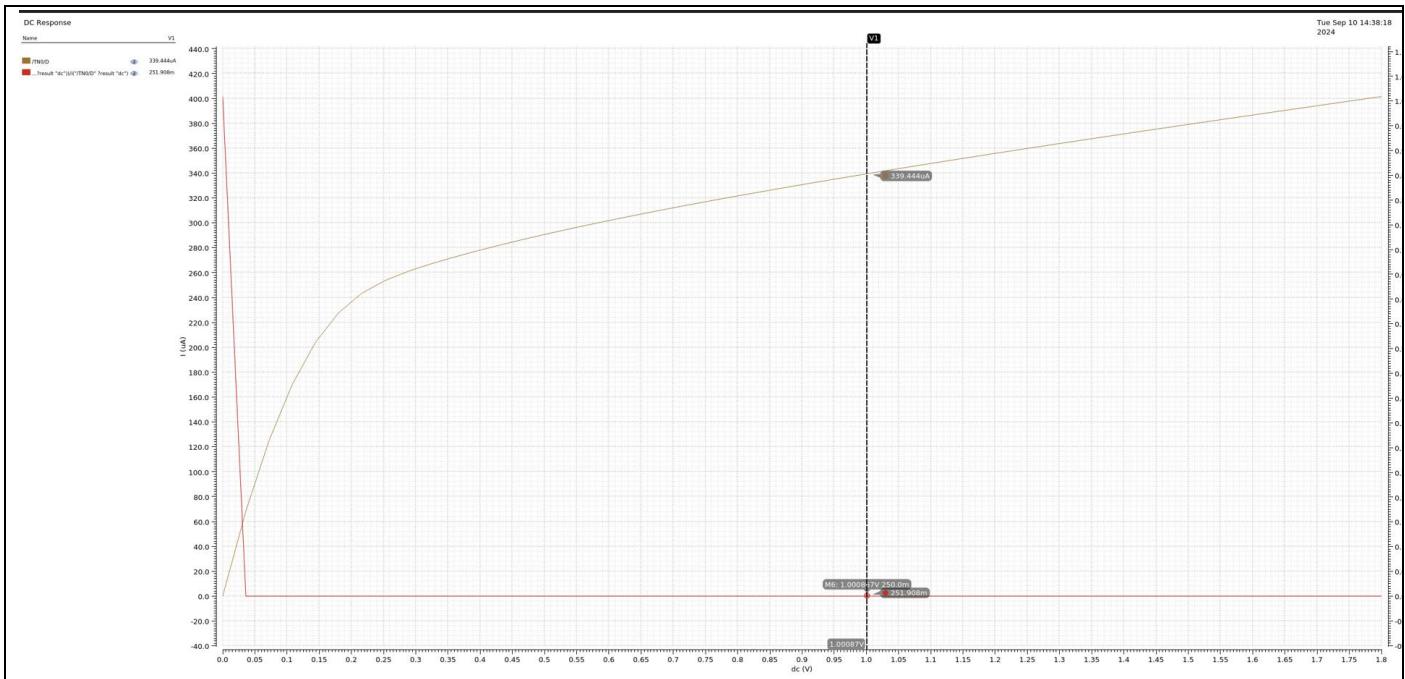
- $V_{th}=0.452\text{V}$
- $\mu nCox \cdot W/L = 4.842\text{m/V}$, while $W/L = 5\mu/0.18\mu$, $\mu nCox = 174.31\mu/\text{V}$
- $V_{th} + (1/2\theta) = 1.021\text{mV}$, and θ will be $\theta=0.878$

b. $V_{GS}=V_{tn}+50\text{mV}+1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $VDS=1\text{V}$. Additionally, find the unity-gain frequency (f_t) using AC simulations.

schematic

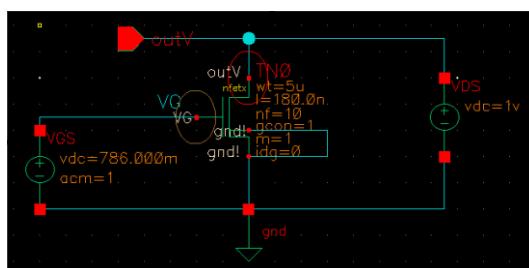


$(dID/dVDS)/ID$ vs. VDS

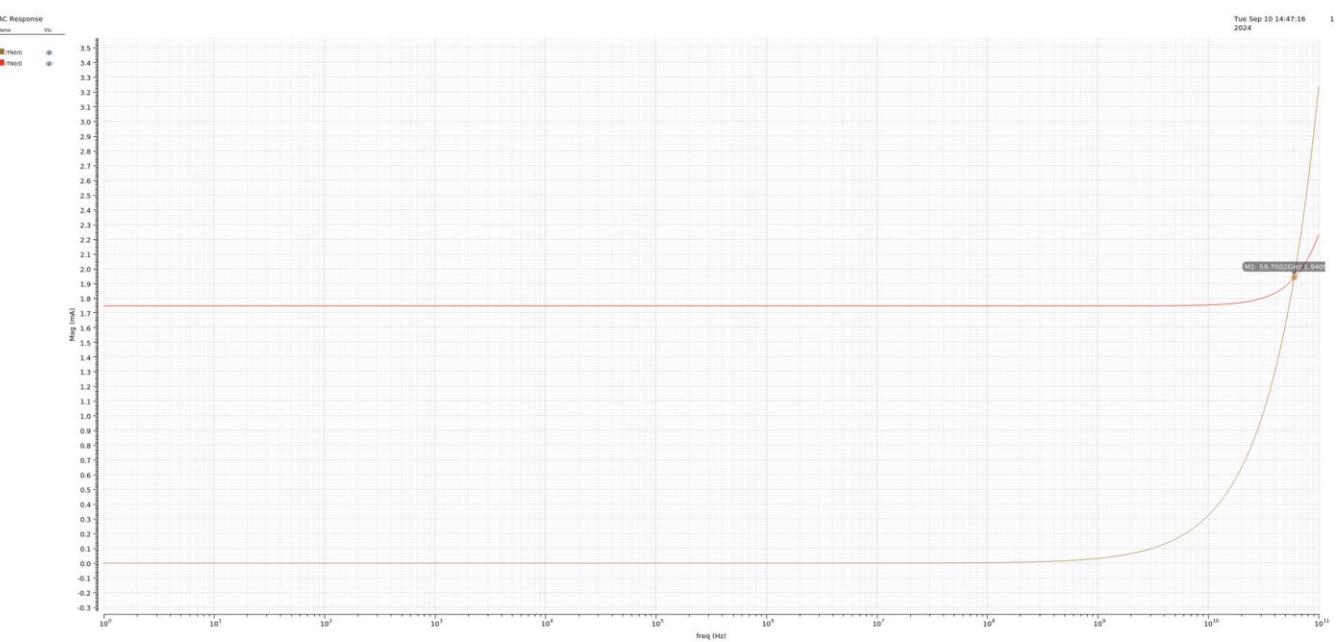


- When $V_{GS} = V_{tn} + 50mV + 1/(4\theta) = 0.786V$ and $V_{DS} = 1V$, the points $y = 251.908m = \lambda/1+\lambda V_{DS}$, which $V_{DS} = 1$, so $\lambda = 0.335$

schematic

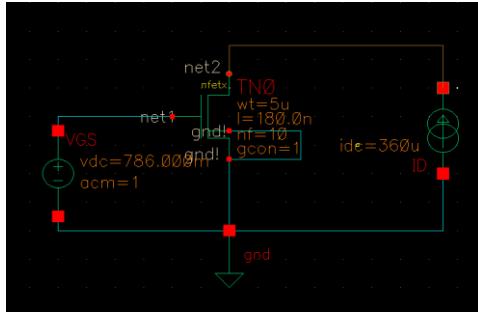


(AC) IG&ID vs Freq

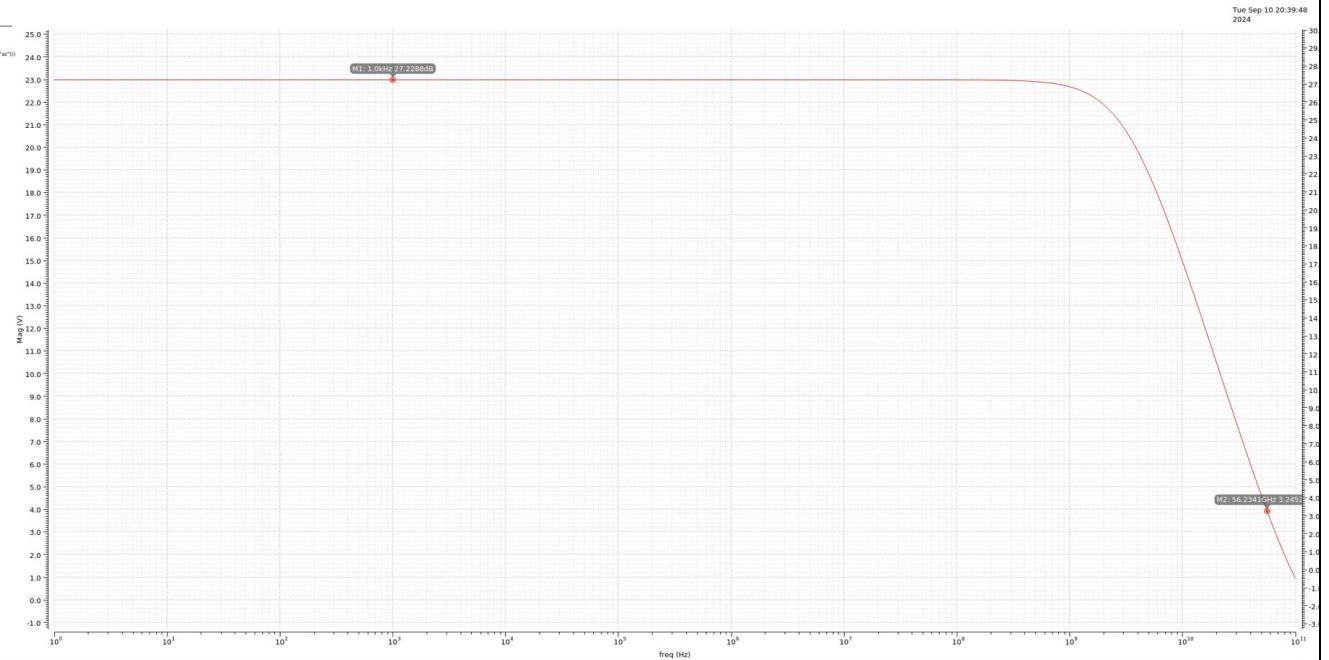


- We can get the f_t when current gain=1 ,which is $IG=ID$ (the intersection), $f_t=59.7GHz$
 - Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations when $V_{DS}=1V$ and $V_{GS}=V_{tn}+50mV+1/(4\theta)$.

schematic

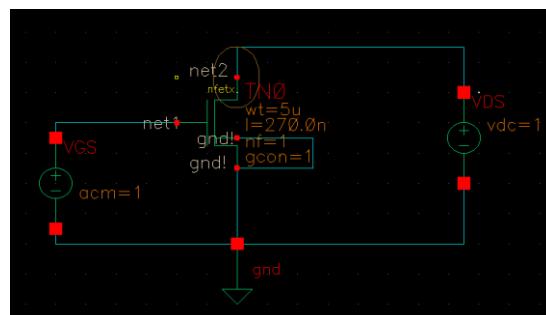


$(dID/dVDS)/ID$ vs. VDS

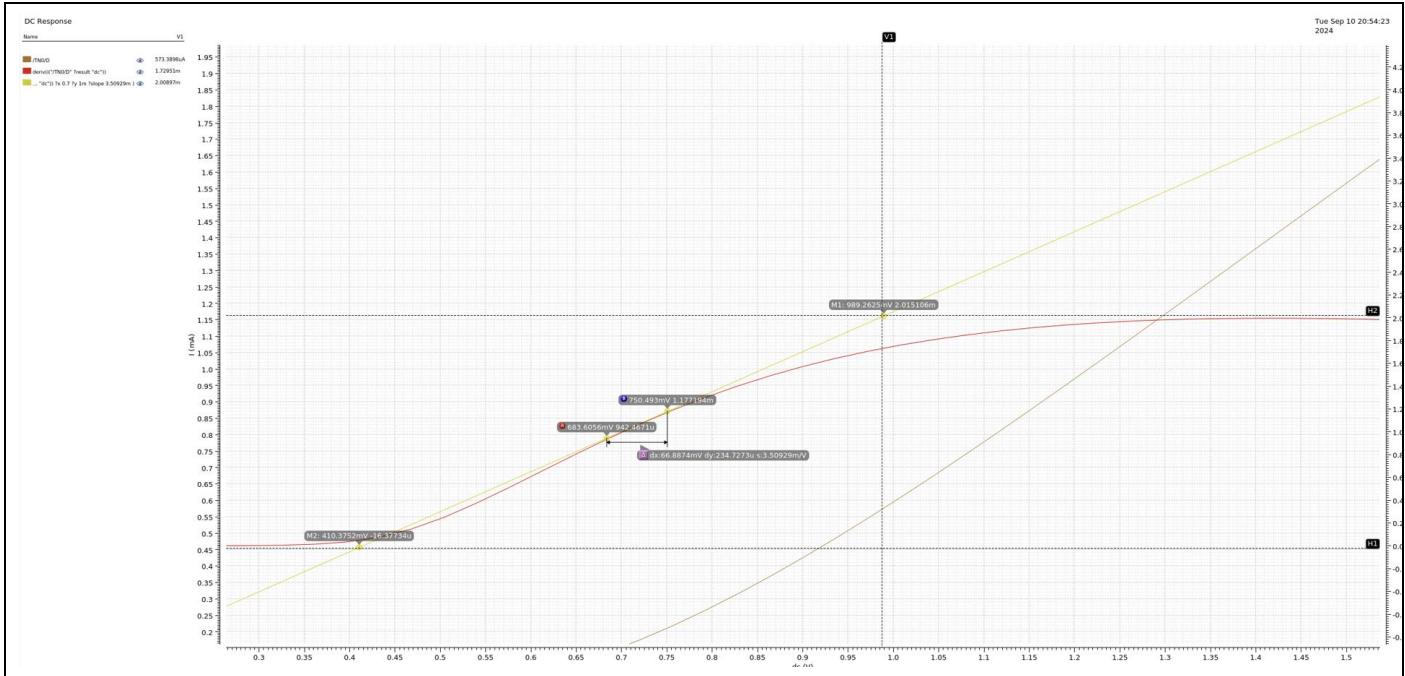


- Adding a current source (by square equation) which makes VDS close to 1V.
 $ID = 1/2 * \mu n C_{ox} * W/L (VGS - VT)^2 (1 + \lambda VDS) = 0.5 * 4.842 m/v * (0.786 - 0.452)^2 * (1 + 0.335) = 360 \mu A$
- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 27.228 \text{ dB}$
- 4. Repeat (1) for the nfetx transistor with $W/L = 5\mu/0.27\mu$ using 1 finger.
 - $VDS = 1V$. Sweep VGS from 0 to 1.8V, plot $(dID/dVGS)$ vs. VGS, and extract V_{tn} , $\mu n C_{ox}$ and θ .

schematic



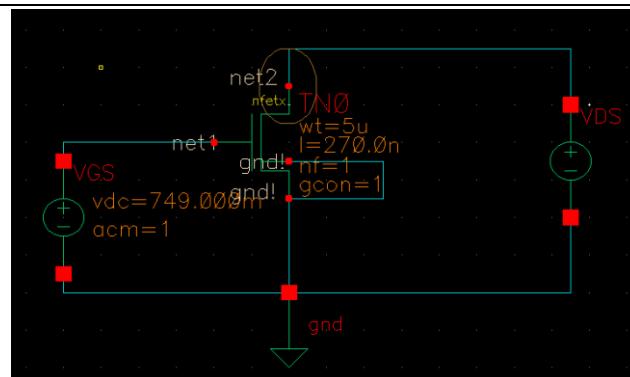
$(dID/dVGS)$ vs. VGS



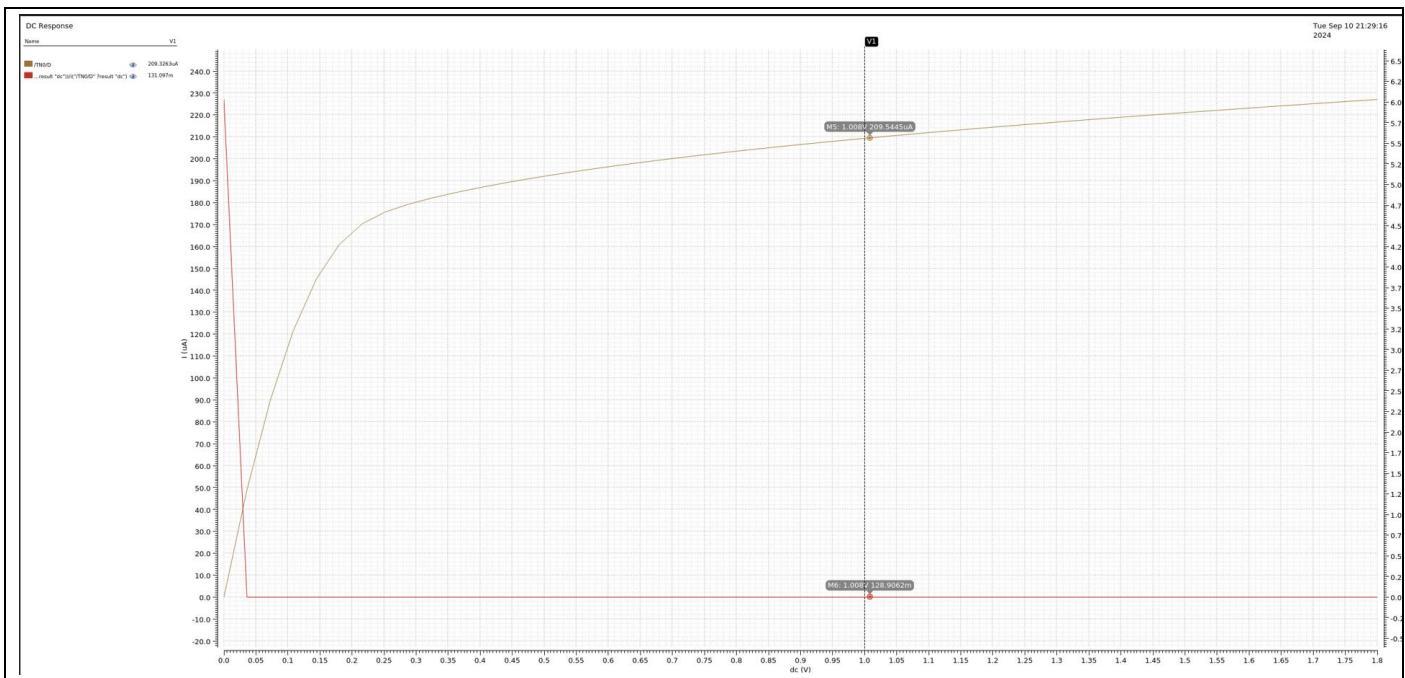
- $V_{th}=0.41V$
- $\mu nCox * W/L = 3.509m/V$, while $W/L = 5u/0.27u$, $\mu nCox = 189.49u/V$
- $V_{th} + (1/2\theta) = 0.989mV$, and θ will be $\theta=0.863$

b. $VGS = V_{tn} + 50mV + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $VDS=1V$. Additionally, find the unity-gain frequency (f_t) using AC simulations.

schematic

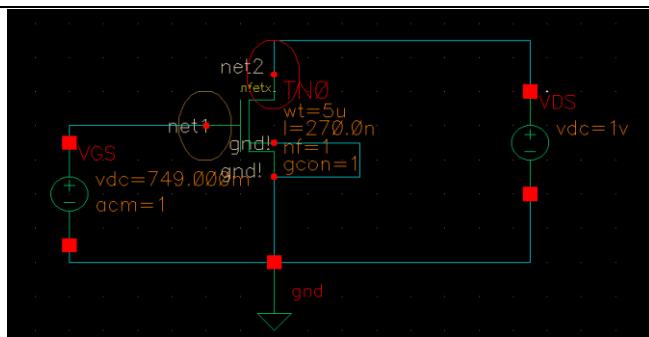


$(dID/dVDS)/ID$ vs. VDS

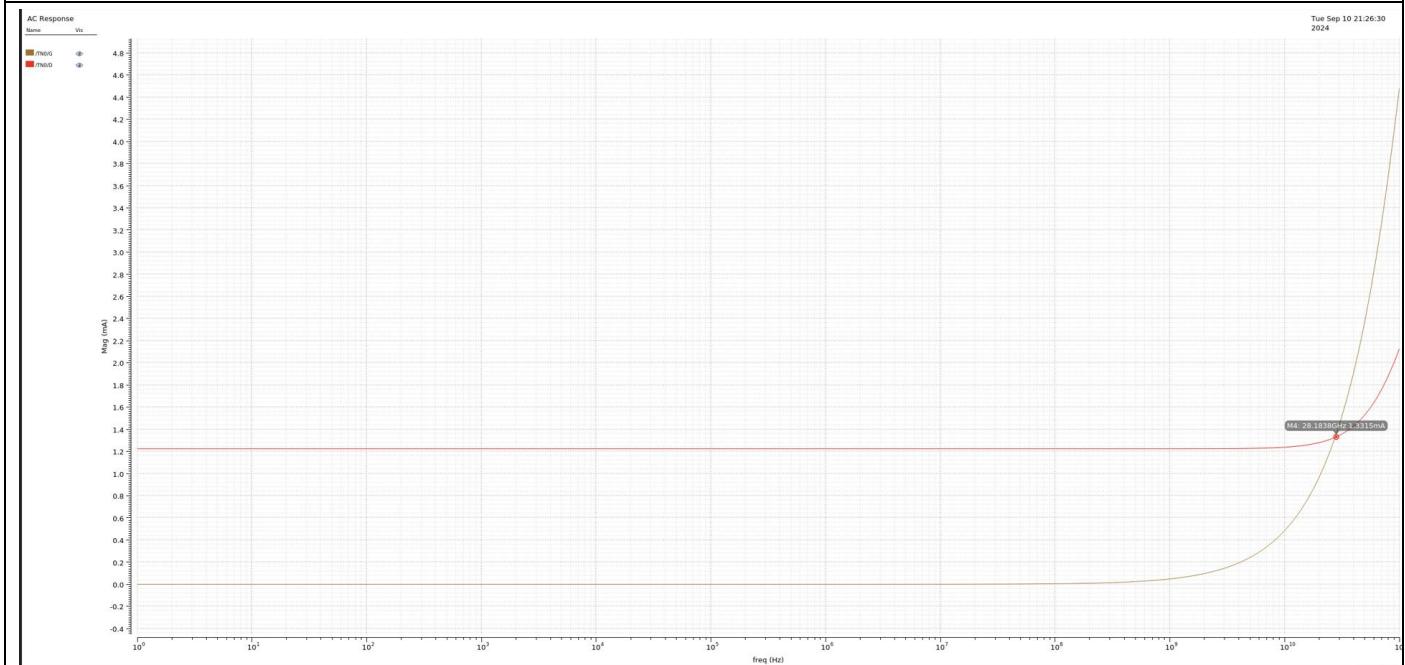


- When $V_{GS} = V_{tn} + 50mV + 1/(4\theta) = 0.749V$ and $V_{DS} = 1V$, the points $y = 111.328m = \lambda/1+\lambda V_{DS}$, which $V_{DS} = 1$, so $\lambda = 0.146$

schematic

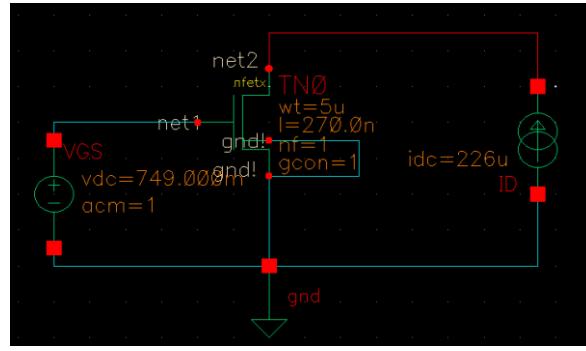


(AC) IG&ID vs Freq

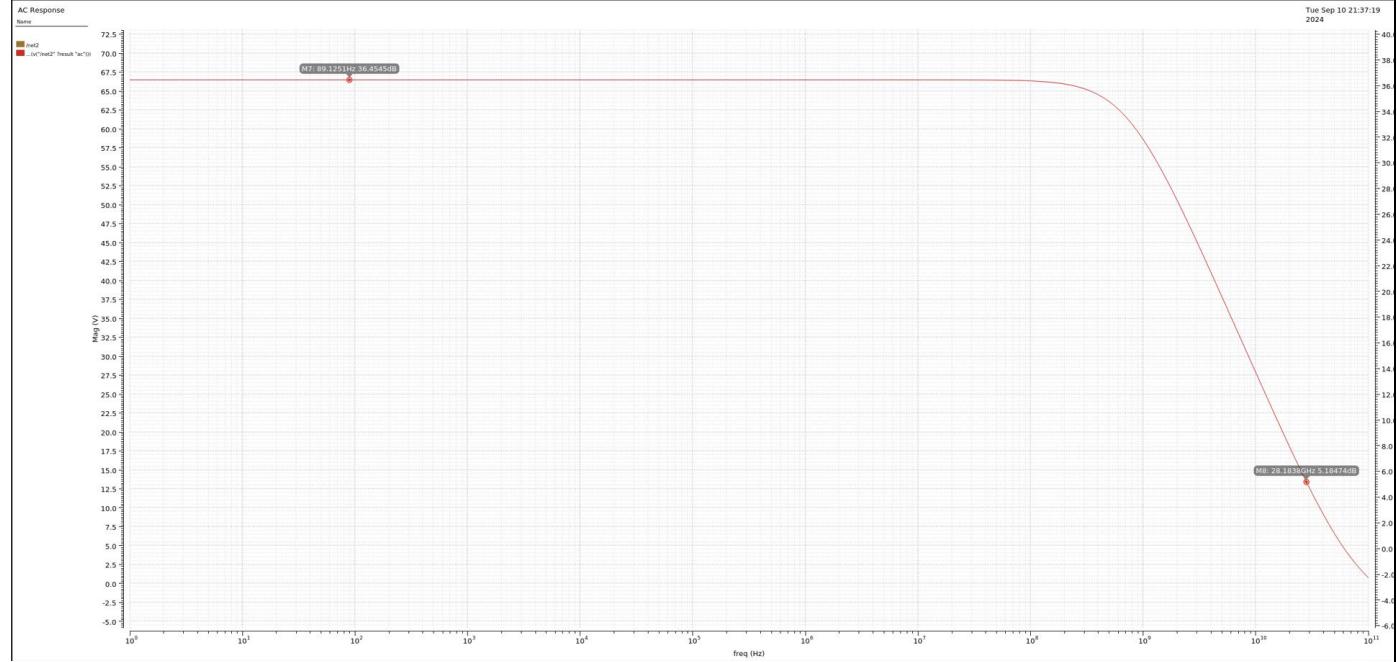


- We can get the f_t when current gain=1 ,which is $IG=ID$ (the intersection), $f_t=28.18GHz$
 - Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations when $V_{DS}=1V$ and $V_{GS}=V_{tn}+50mV+1/(4\theta)$.

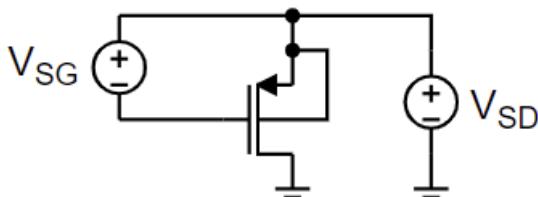
schematic



(dID/dVGS)/ID vs. VDS

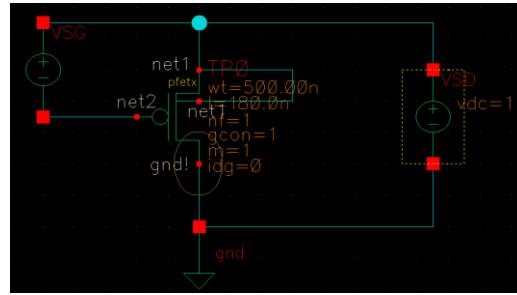


- Adding a current source (by square equation) which makes VDS close to 1v.
 $ID = 1/2 * \mu n C_{ox} * W/L (VGS - VT)^2 (1 + \lambda VDS) = 0.5 * 3.509 m/v * (0.749 - 0.41)^2 * (1 + 0.124) = 226 \mu A$
- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 36.454 \text{ dB}$
- 5. Construct the circuit below using pfetx transistor with $W/L = 0.5\mu/0.18\mu$ using 1 finger.

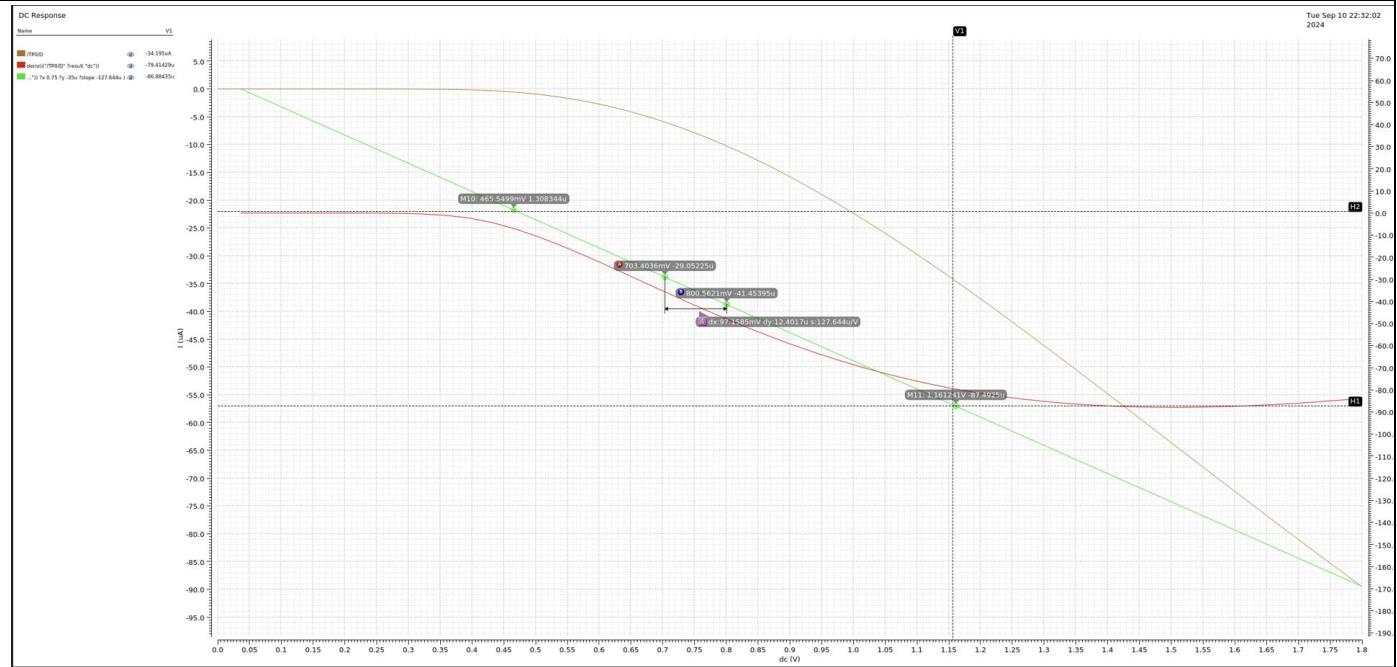


- a. $VDS = 1V$. Sweep VGS from 0 to 1.8V, plot $(dID/dVGS)$ vs. VGS , and extract V_{tn} , $\mu n C_{ox}$ and θ .

schematic



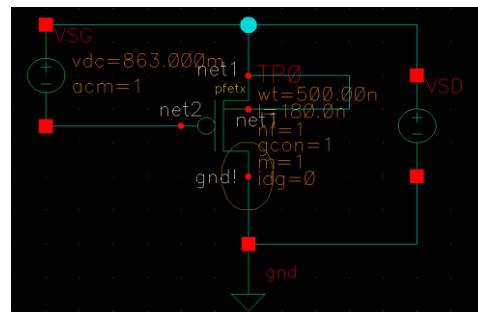
(dID/dVSG) vs. VSG



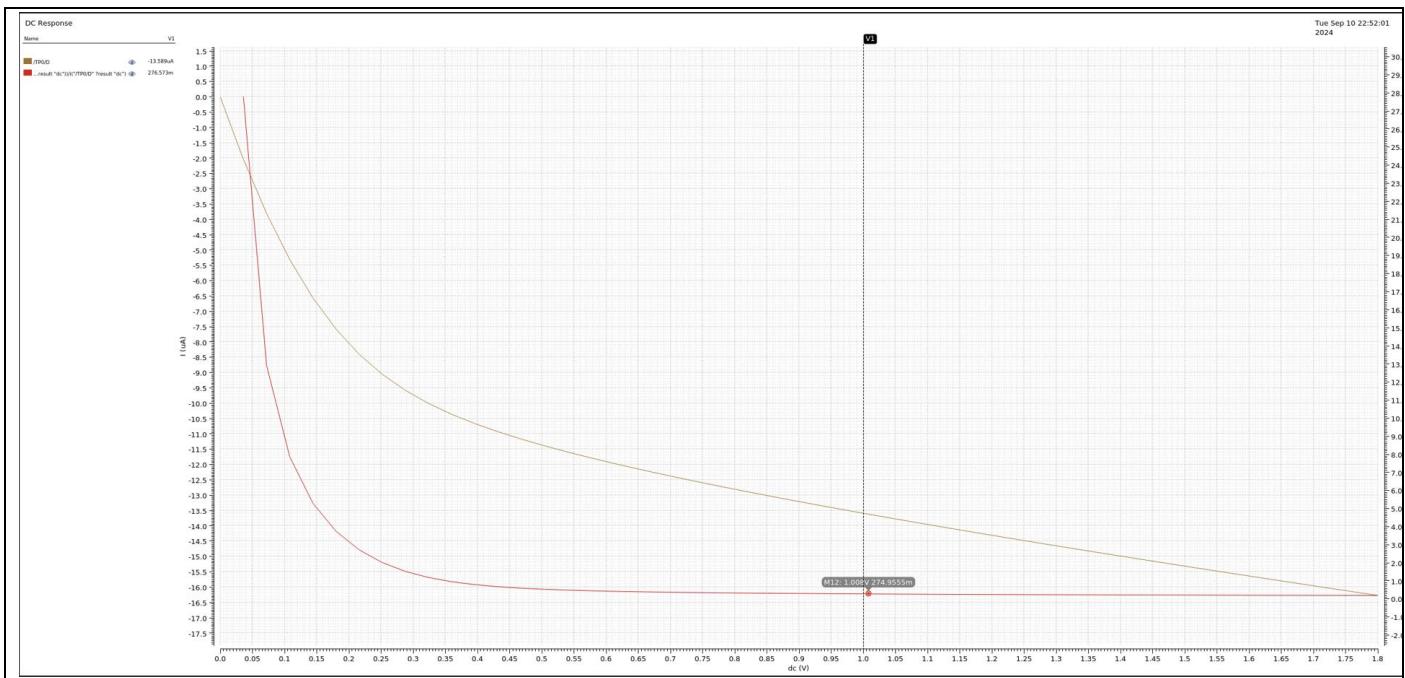
- $|V_{th}| = V_{SG} = 0.465V = -(V_{GS} = -0.465V)$
- $\mu n C_{ox} * W/L = -127.644u/V$, while $W/L = 0.5u/0.18u$, $\mu n C_{ox} = 46.08u/V$
- $V_{th} + (1/2\theta) = 1.161$, and θ will be $\theta = 0.718$

b. $V_{GS} = V_{tn} + 50mV + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $V_{DS}=1V$. Additionally, find the unity-gain frequency (f_T) using AC simulations.

schematic

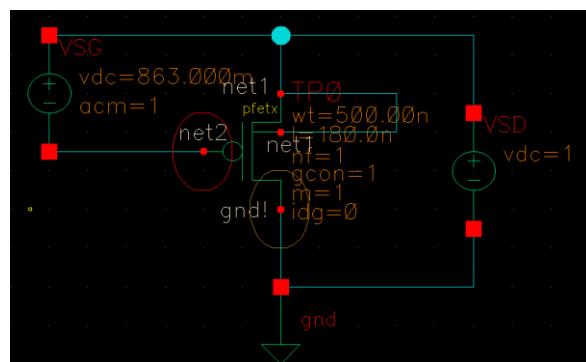


$(dID/dVSD)/ID$ vs. VSD

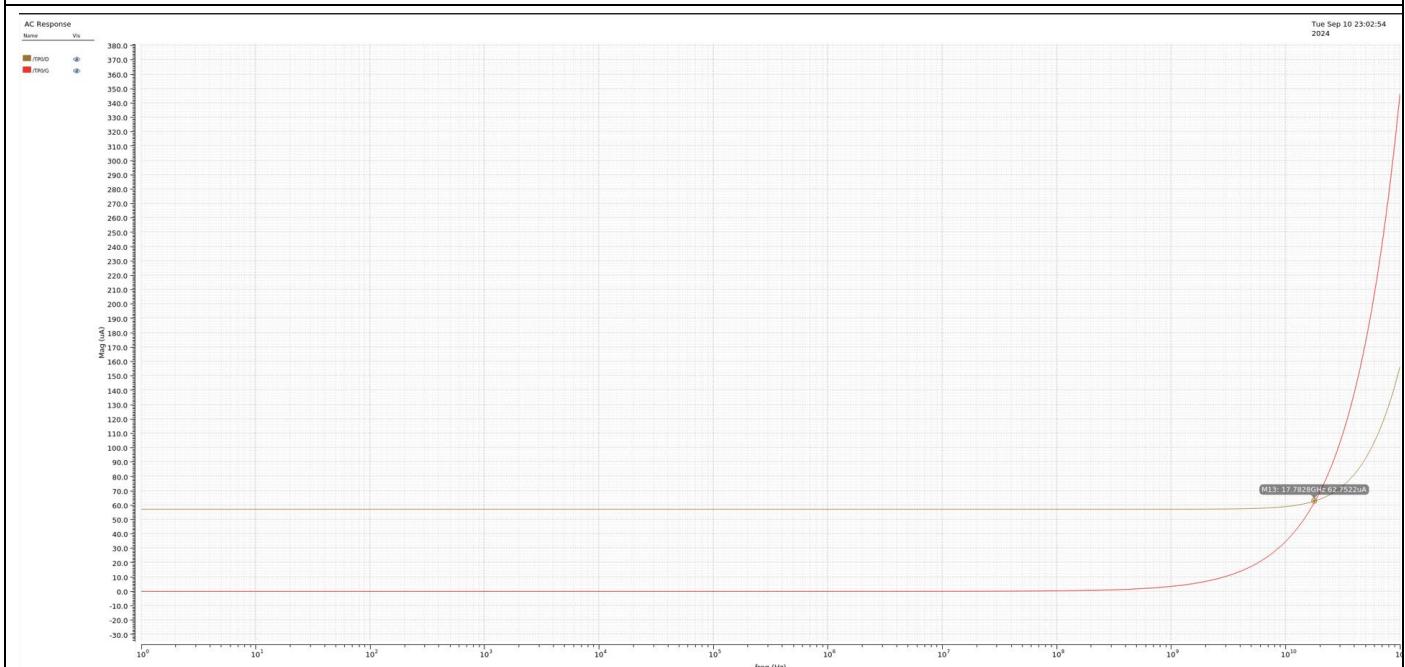


- When $VGS = Vtn + 50mV + 1/(4\theta) = 0.863V$ and $VDS = 1V$, the points $y = 274.955m = \lambda/1+\lambda VDS$, which $VDS = 1$, so **0.377**

schematic

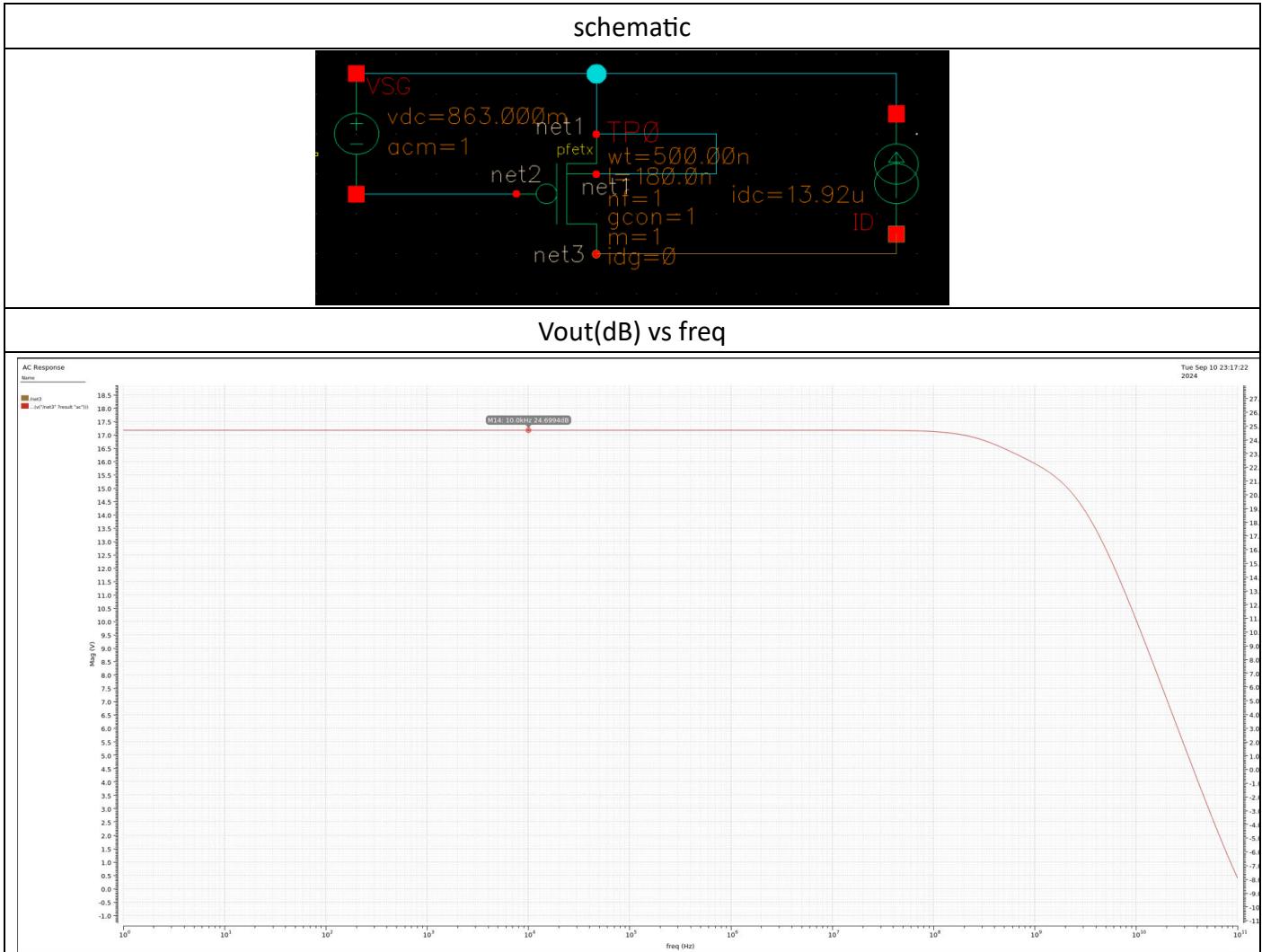


(AC) IG&ID vs Freq



- We can get the ft when current gain=1 ,which is $IG=ID$ (the intersection), **ft=17.782GHz**
- c. Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations

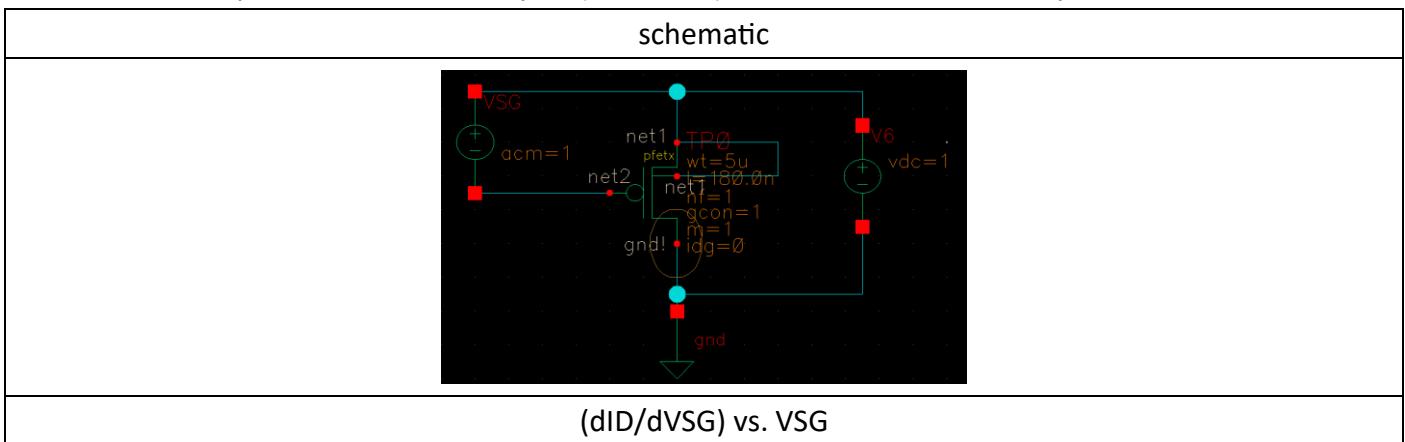
when VDS=1V and VGS=Vtn+50mV+1/(4θ).

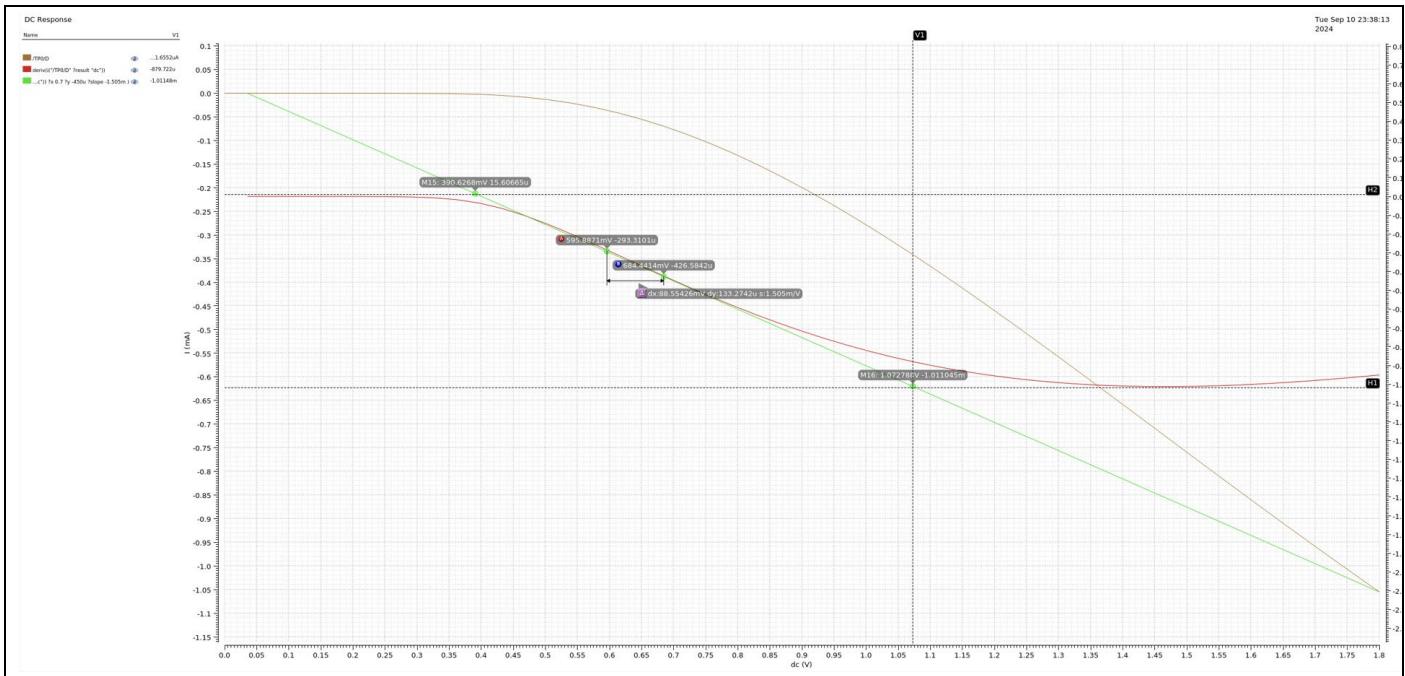


- Adding a current source (by square equation) which makes VDS close to 1v.
 $ID = 1/2 * \mu n Cox * W/L (VGS - VT)^2$ [(1+λVDS) approximate 1] = $0.5 * 127.644u/v * (0.863 - 0.465)^2 * 1.377 = 13.92uA$
- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 24.699dB$

6. Repeat (5) for the pfetx transistor with $W/L = 5\mu/0.18\mu$ using 1 finger.

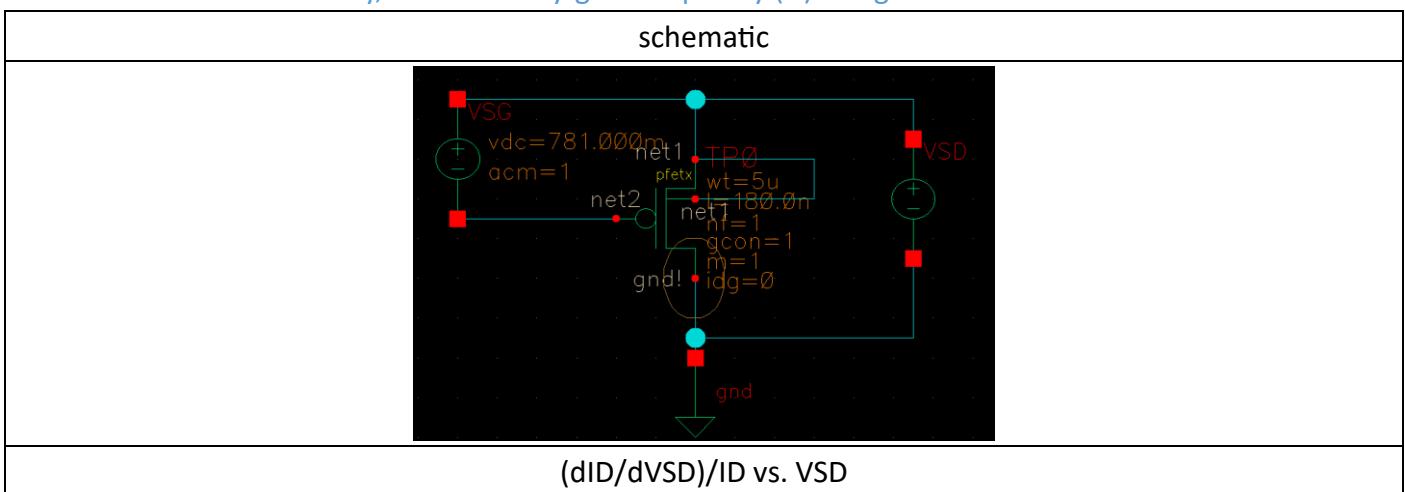
a. $VDS=1V$. Sweep VGS from 0 to 1.8V, plot $(dID/dVGS)$ vs. VGS , and extract V_{tn} , $\mu n Cox$ and θ .

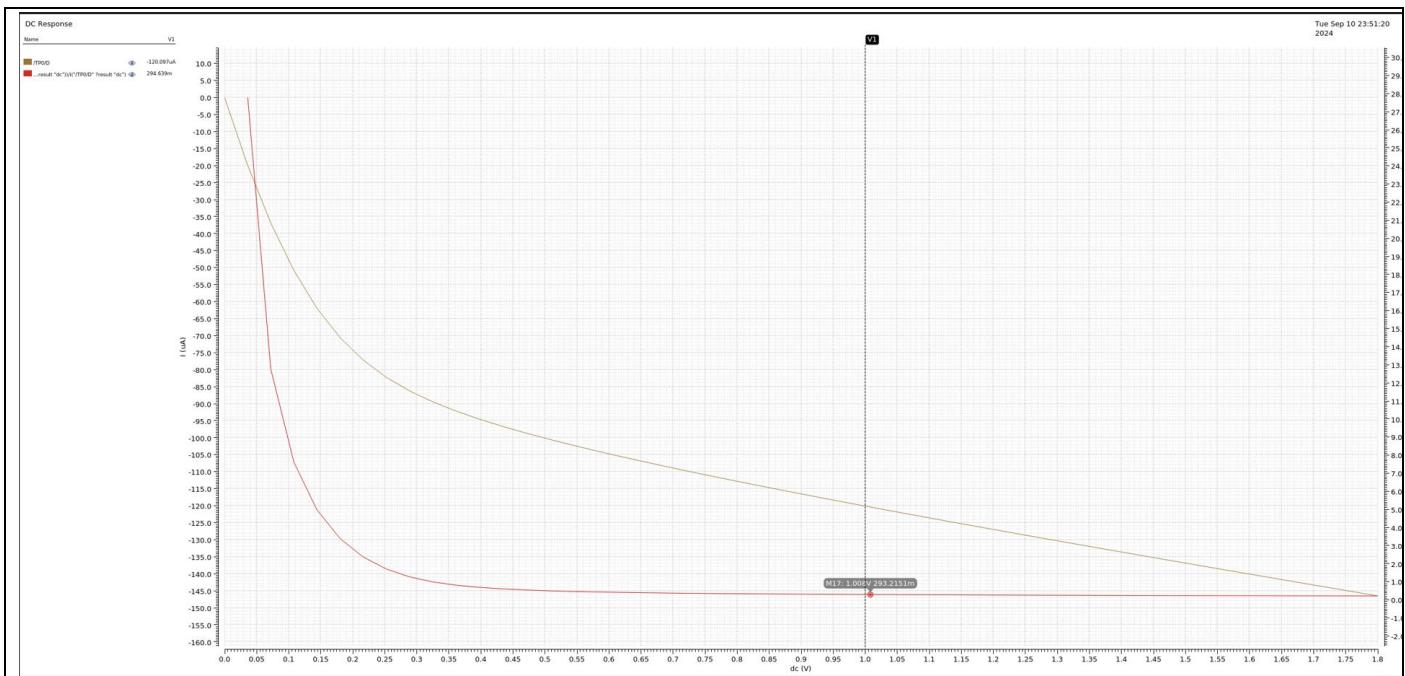




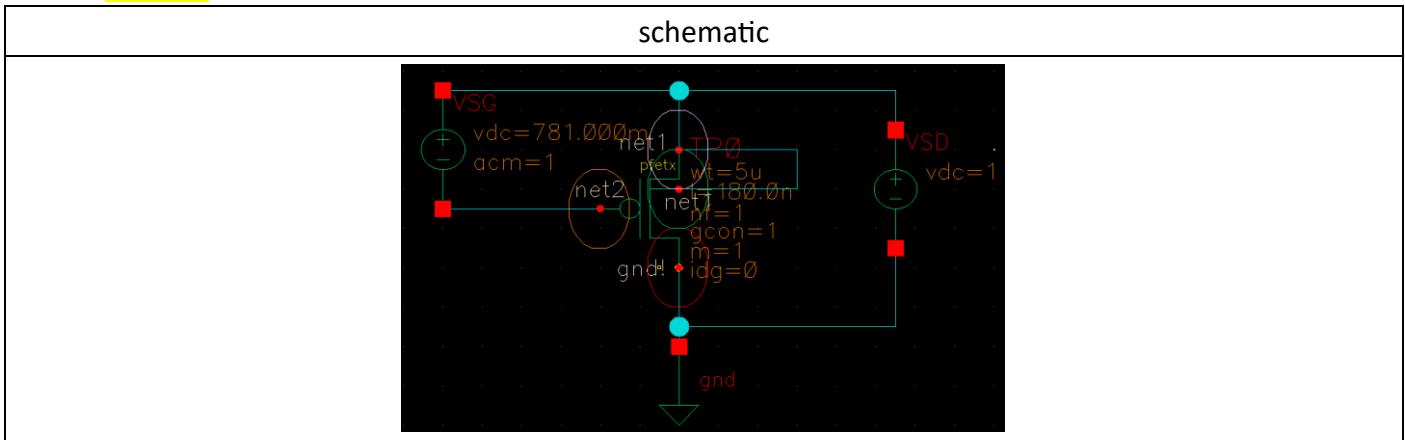
- $|V_{th}| = V_{SG} = 0.39V = (V_{GS} = -0.39V)$
- $\mu nCox * W/L = -1.505m/v$, while $W/L = 5u/0.18u$, $\mu nCox = 54.19u/V$
- $V_{th} + (1/2\theta) = 1.072$, and θ will be $\theta = 0.733$

b. $V_{GS} = V_{tn} + 50mV + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dI/D/dVDS)/ID$ vs. VDS and extract λ at $VDS=1V$. Additionally, find the unity-gain frequency (f_t) using AC simulations.





- When $VGS = Vtn + 50mV + 1/(4\theta) = 0.781V$ and $VDS = 1V$, the points $y = 293.21m = \lambda/1+\lambda VDS$, which $VDS = 1$, so **0.414**

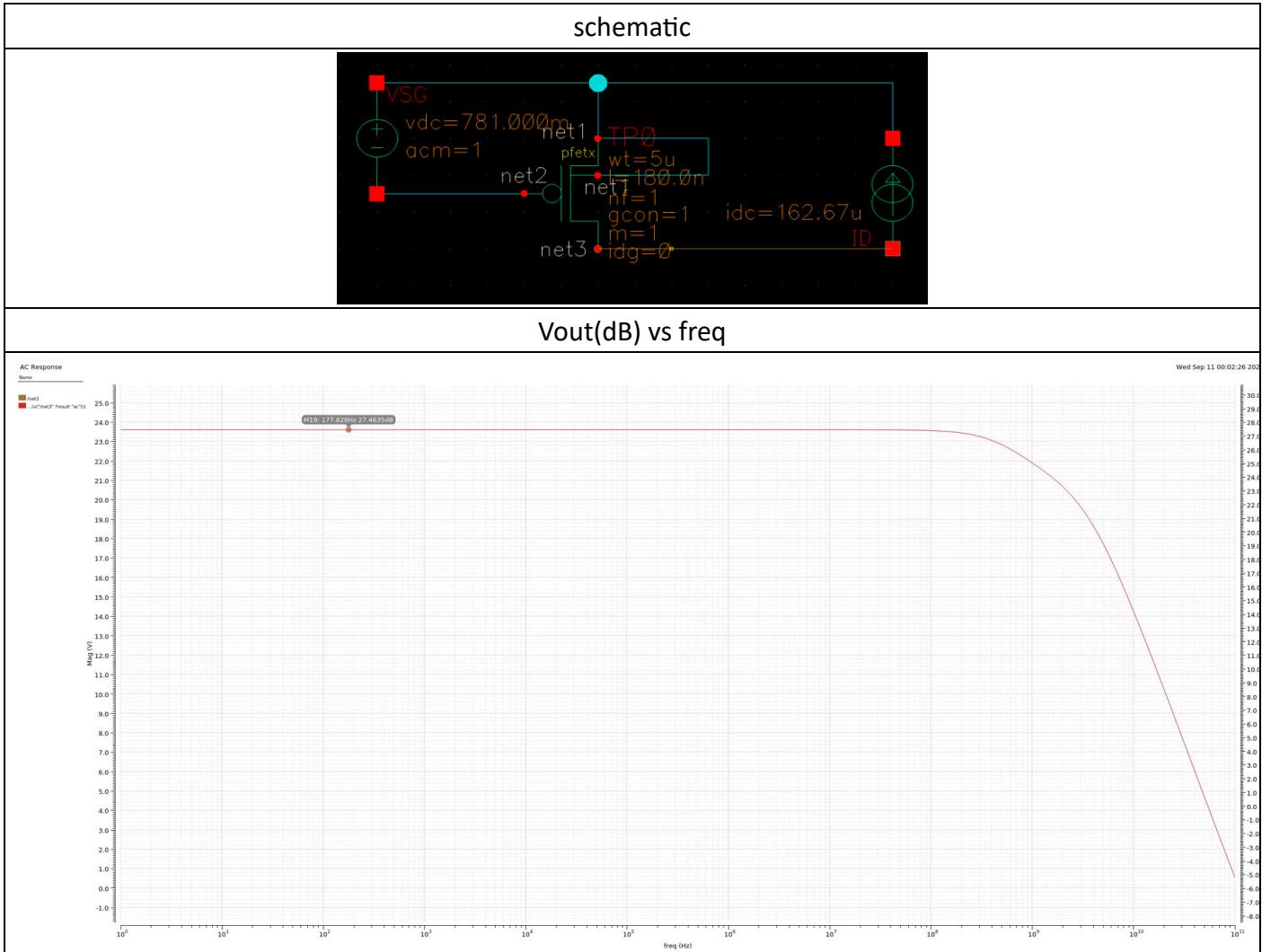


(AC) IG&ID vs Freq



- We can get the ft when current gain=1 ,which is $IG=ID$ (the intersection), **ft=17.782GHz**
- c. Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations

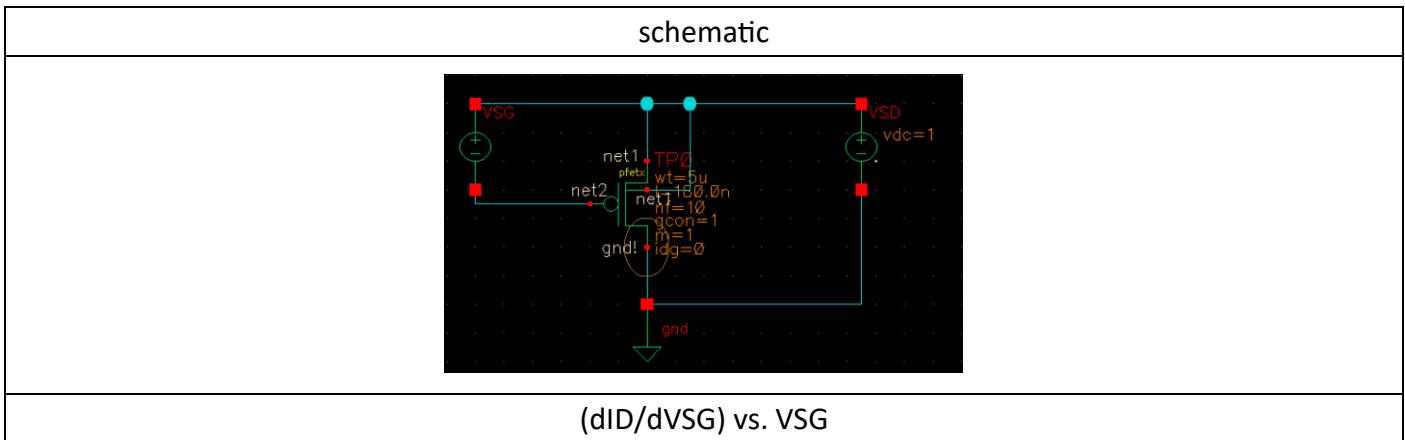
when VDS=1V and VGS=Vtn+50mV+1/(4θ).

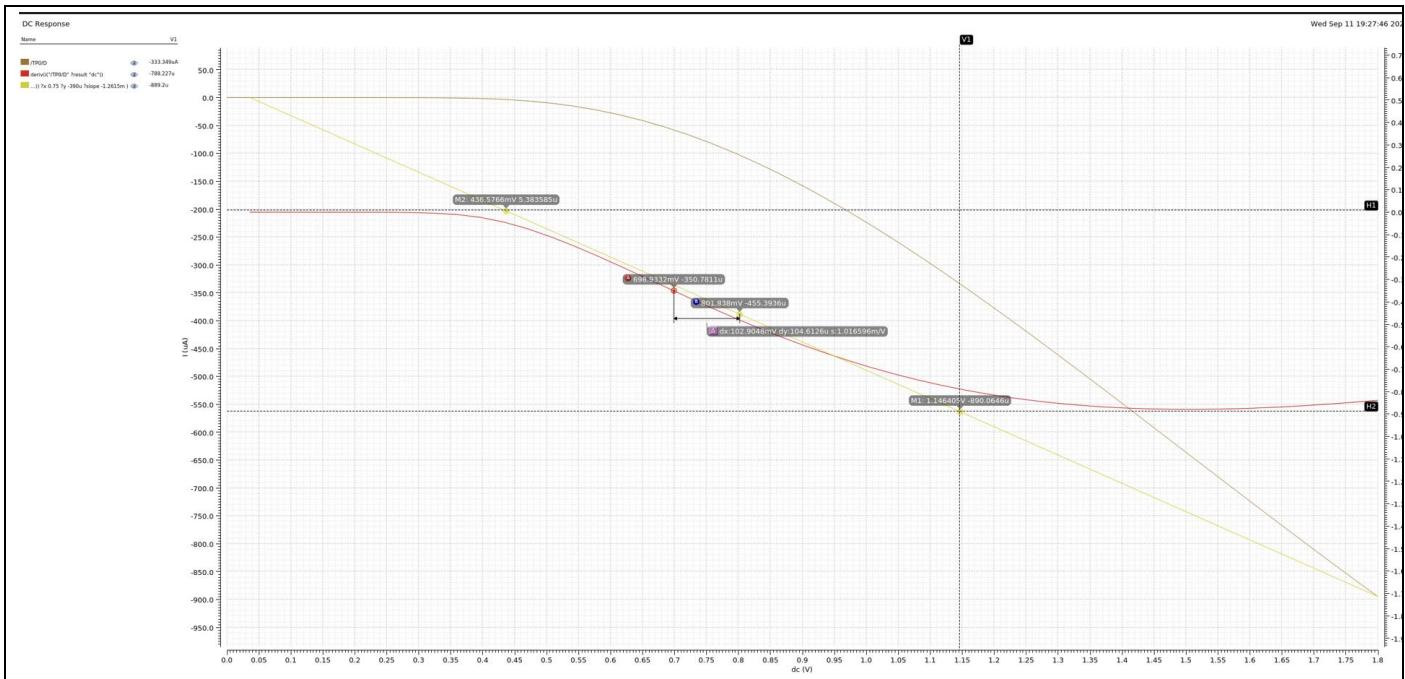


- Adding a current source (by square equation) which makes VDS close to 1v.
 $ID = 1/2 * \mu n Cox * W/L(VGS - VT)^2$ [(1+λVDS) approximate 1] = $0.5 * 1.505m/v * (0.781 - 0.39)^2 * 1.414 = 162.67\mu A$
- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 27.463\text{dB}$

7. Repeat (5) for the pfetx transistor with W/L 5μ/0.18μ using 10 fingers

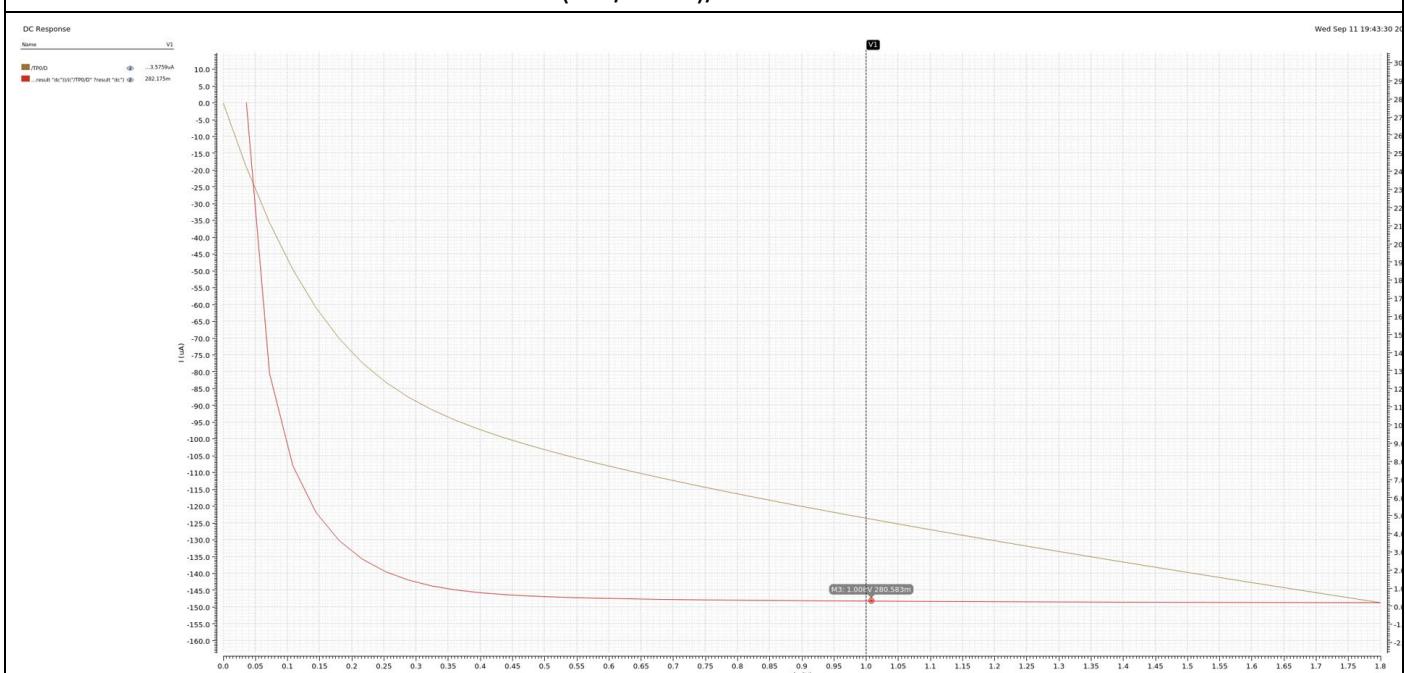
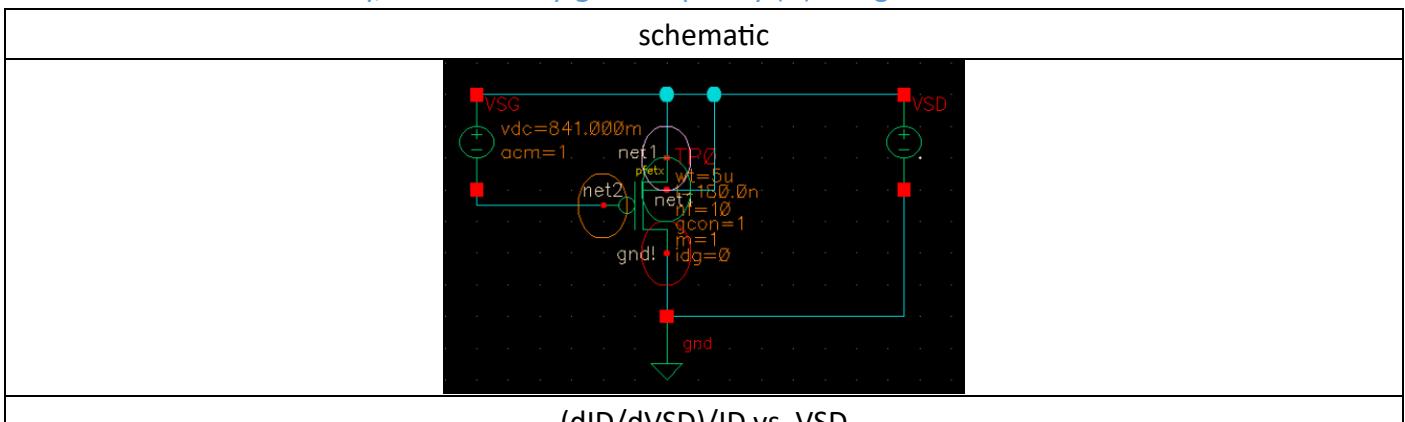
a. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.





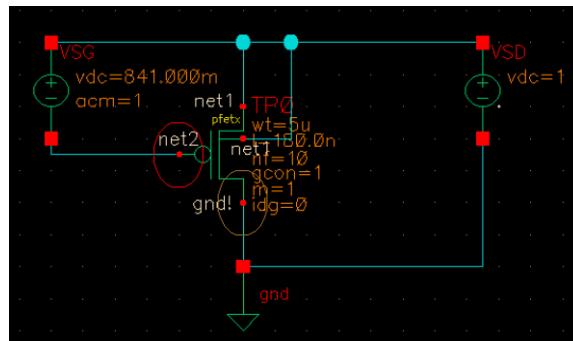
- $|V_{th}| = V_{SG} = 0.436 \text{ V} = (V_{GS} = -0.436 \text{ V})$
- $\mu nCox * W/L = -1.016 \text{ m/V}$, while $W/L = 5\text{u}/0.18\text{u}$, $\mu nCox = 36.58 \text{ u/V}$
- $V_{th} + (1/2\theta) = 1.146$, and θ will be $\theta = 0.704$

b. $V_{GS} = V_{tn} + 50 \text{ mV} + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $V_{DS}=1\text{V}$. Additionally, find the unity-gain frequency (f_T) using AC simulations.

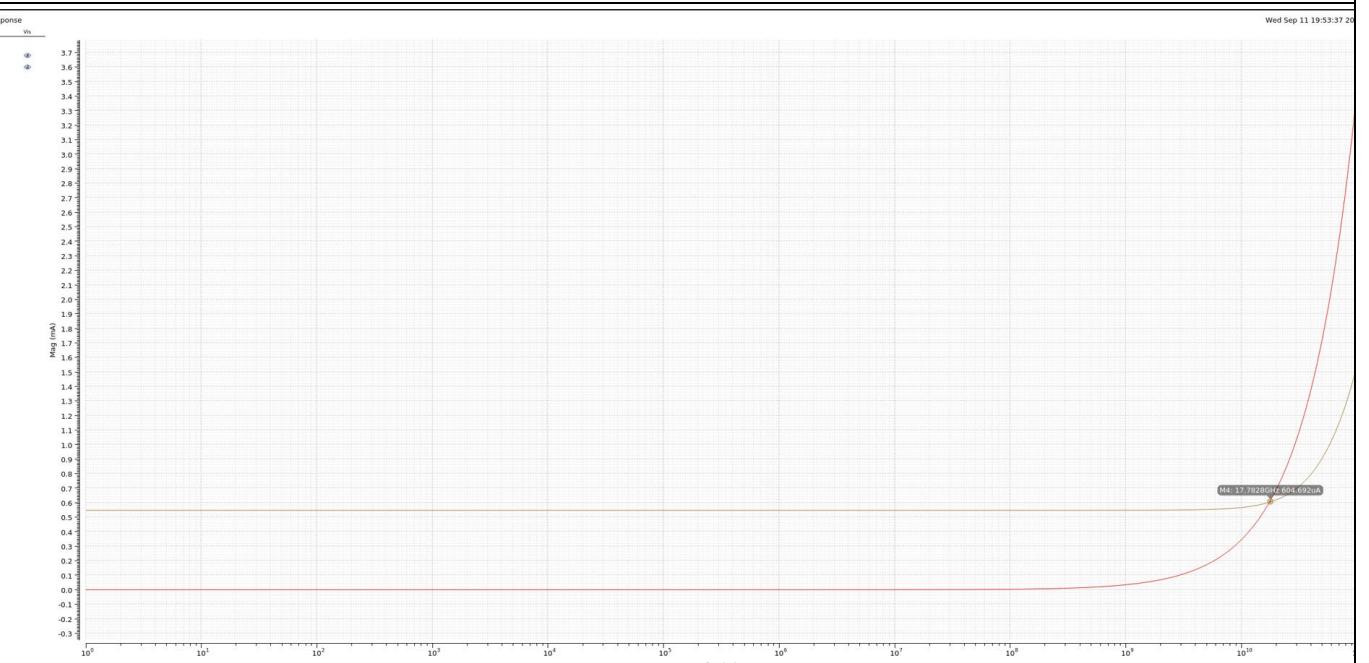


- When $VGS = Vtn + 50mV + 1/(4\theta) = 0.841v$ and $VDS=1v$, the points $y= 280.583m = \lambda/1+\lambda VDS$, which $VDS=1$, so $\lambda=0.388$

schematic

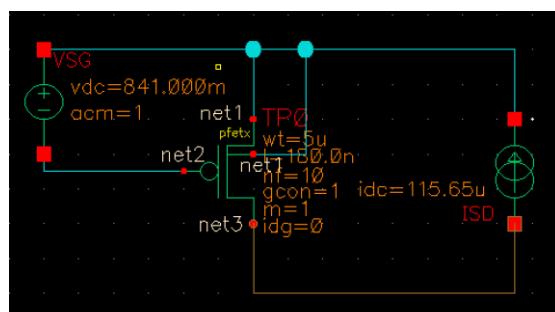


(AC) IG&ID vs Freq

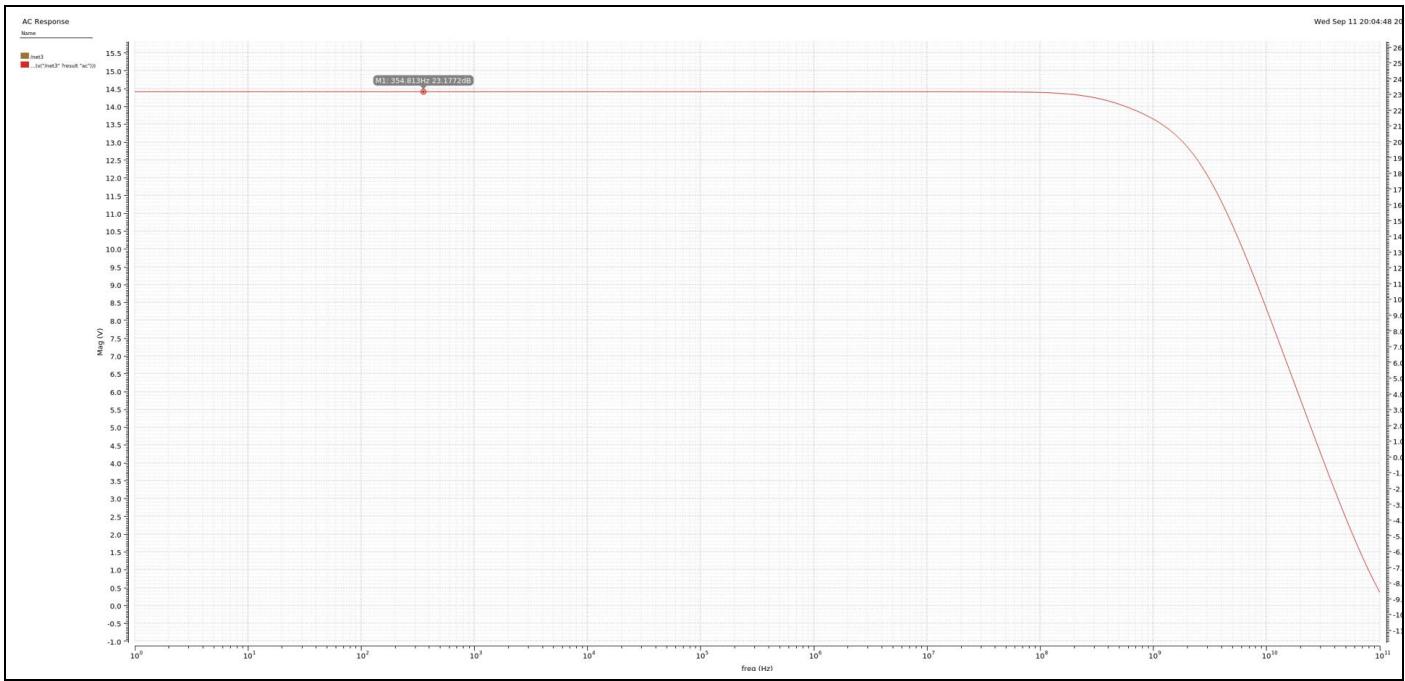


- We can get the ft when current gain=1 ,which is $IG=ID$ (the intersection), $ft=17.782\text{GHz}$
- c. Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations when $VDS=1V$ and $VGS=Vtn+50mV+1/(4\theta)$.

schematic



Vout(dB) vs freq



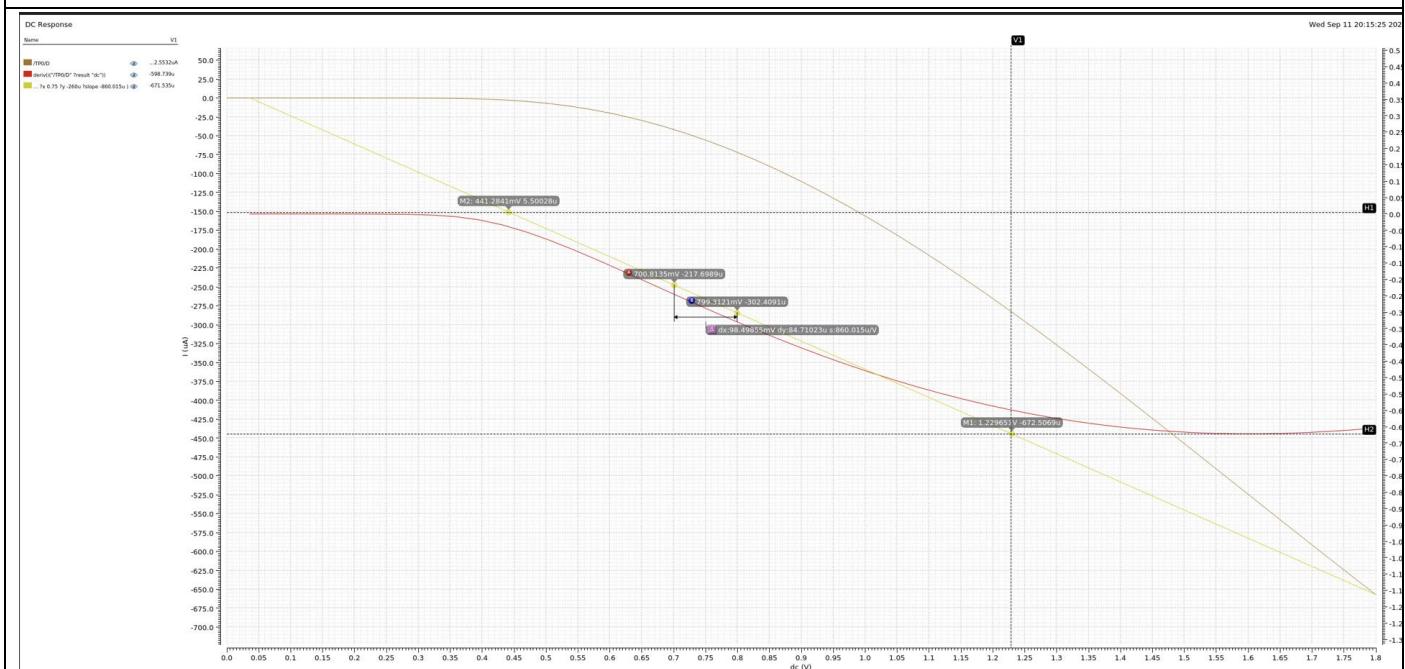
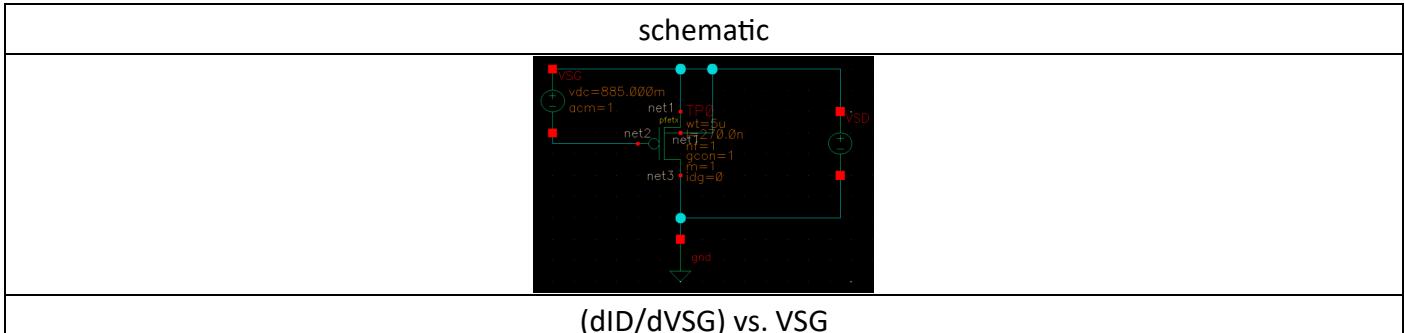
- Adding a current source (by square equation) which makes VDS close to 1v.

$$ID = \frac{1}{2} \mu nCox * W/L (VGS - VT)^2 [(1 + \lambda VDS) \text{ approximate } 1] = 0.5 * 1.016 \mu A / V * (0.841 - 0.436)^2 * 1.388 = 115.65 \mu A$$

- By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain **Ai= 23.177dB**

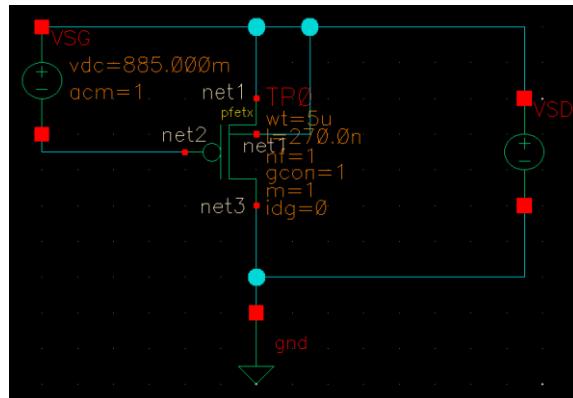
8. Repeat (5) for the pfetx transistor with W/L=5μ/0.27μ using 1 finger.

a. **VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.**

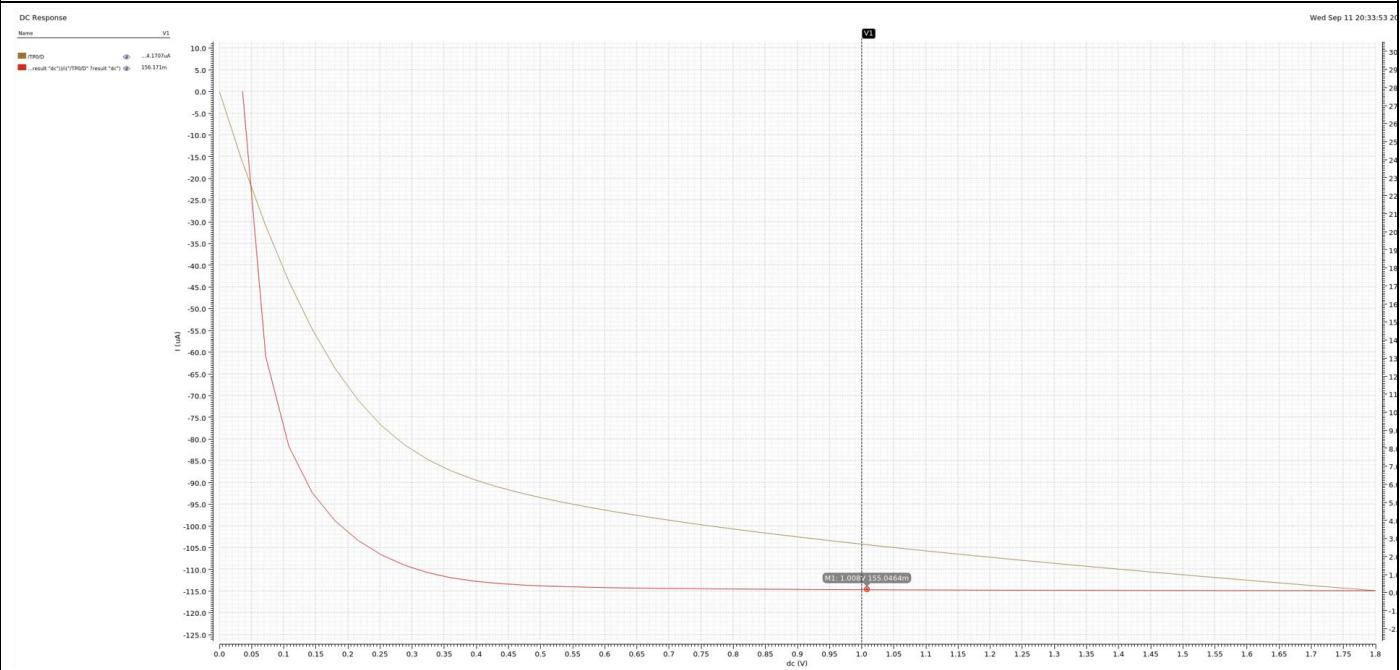


- $|V_{th}| = V_{SG} = 0.441V = (V_{GS} = -0.441V)$
 - $\mu nCox * W/L = -860.015u/V$, while $W/L = 5u/0.27u$, $\mu nCox = 46.46u/V$
 - $V_{th} + (1/2\theta) = 1.229$, and θ will be $\theta = 0.634$
- b. $V_{GS} = V_{tn} + 50mV + 1/(4\theta)$. Sweep VDS from 0 to 1.8V, plot $(dID/dVDS)/ID$ vs. VDS and extract λ at $VDS=1V$. Additionally, find the unity-gain frequency (f_t) using AC simulations.

schematic

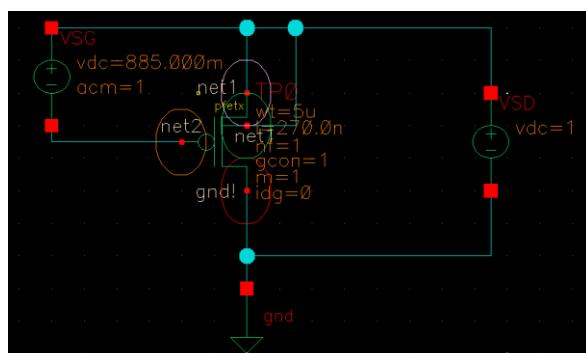


$(dID/dVDS)/ID$ vs. VSD

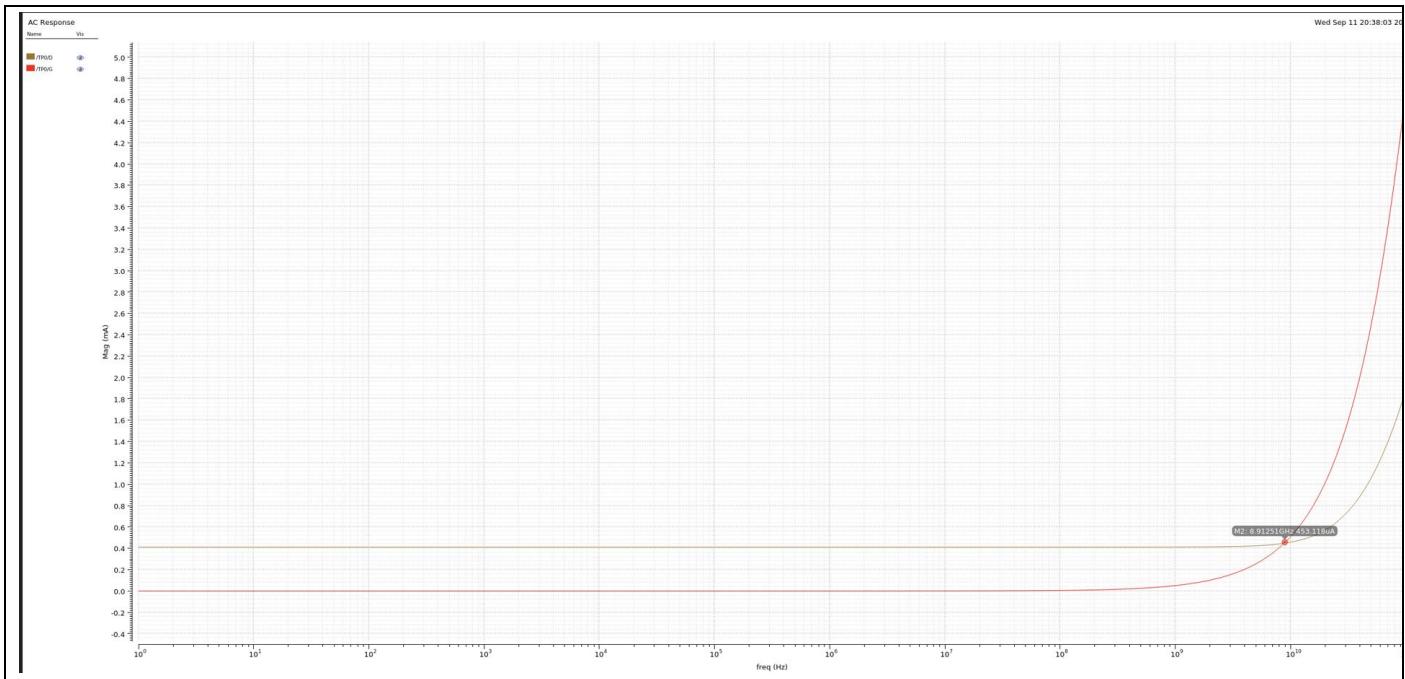


- When $V_{GS} = V_{tn} + 50mV + 1/(4\theta) = 0.885V$ and $VDS = 1V$, the points $y = 155.046m = \lambda/1 + \lambda VDS$, which $VDS = 1$, so $\lambda = 0.183$

schematic

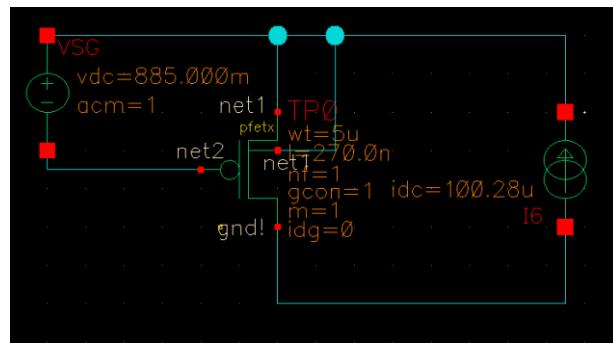


(AC) IG&ID vs Freq

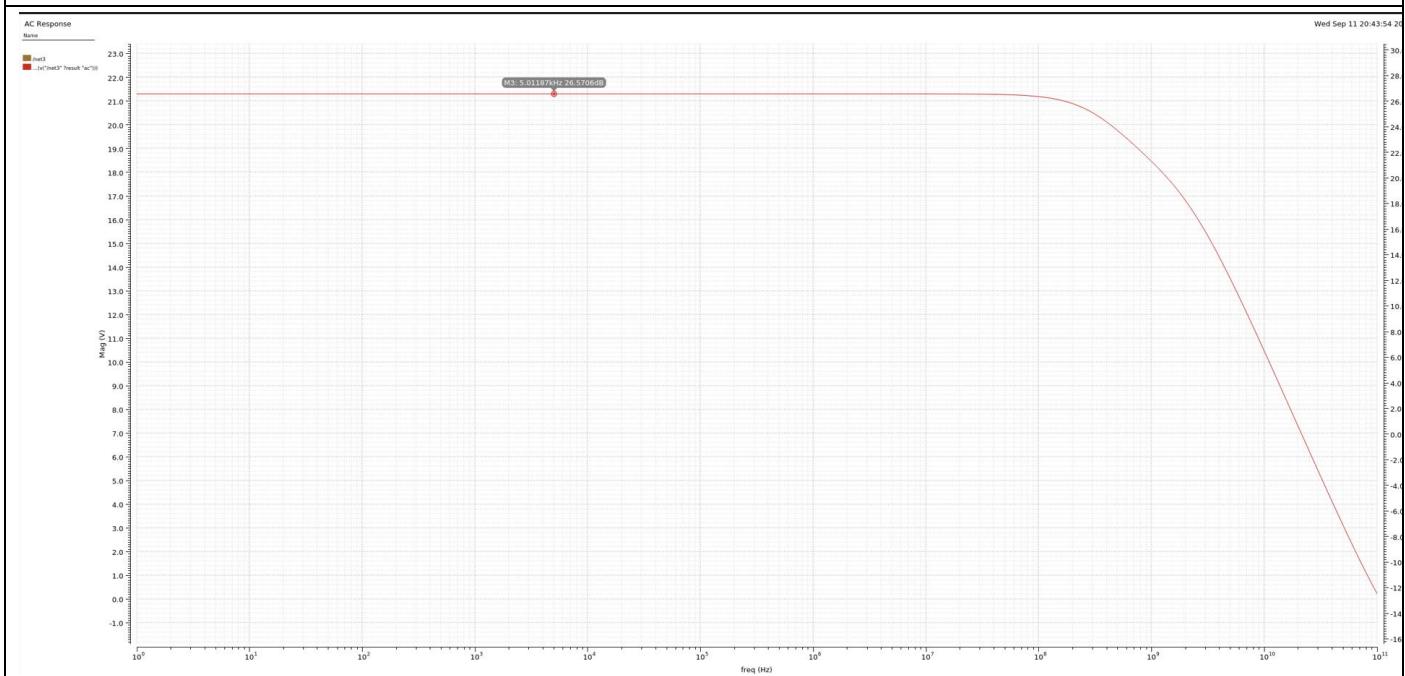


- We can get the f_t when current gain=1 ,which is $IG=ID$ (the intersection), $f_t=8.912\text{GHz}$
- c. Reconfigure the circuit if necessary and find the intrinsic gain (A_i) using AC simulations when $VDS=1\text{V}$ and $VGS=V_{tn}+50\text{mV}+1/(40)$.

schematic



$V_{out}(\text{dB})$ vs freq



- Adding a current source (by square equation) which makes VDS close to 1v.

$$ID = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot W/L \cdot (V_{GS} - V_T)^2 [(1 + \lambda V_{DS}) \approx 1] = 0.5 \cdot 860.015 \cdot u / v \cdot (0.885 - 0.441)^2 \cdot 1.183 = 100.28 \mu A$$

By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain $A_i = 26.57 \text{ dB}$

Conclusion

In this lab, we learn how to operate Virtuoso under Cadence to find the basic characteristics of the different parameters of NMOS and PMOS. Just like what the professor mentioned in class, understanding how to identify the basic characteristics of MOS transistors is essential for an engineer. Using ADE L, we can also compare the simulated values of the MOS transistors with the values obtained from hand calculations. In conclusion, we have gained a foundational understanding of how to use Virtuoso and have identified the basic characteristics of MOS transistors, which can be applied in future lab.