24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab1: Introduction to Cadence and MOS Device  
Characterization

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**Description:**

In this lab, we learn how to use Cadence Virtuoso to plot and measure some basic characteristics of the different parameters (W/L, finger) of NMOS and PMOS. Generating the waveform plot and examinate the result.

**Design & result**

1. Construct the circuit below using nfetx transistor with W/L=0.5μ/0.18μ using 1 finger.

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自動產生的描述

1. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVGS) vs. VGS |
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* The red line equals to (dID/dVGS), and by selecting two points on the red line we can approximately get the tan of red line, which is represent in blue line.
* By finding the intersection point of the blue line and the minimum horizon line of the red line, we can find the Vth which is Vth=0.43v
* By finding the slope of the red line, which is blue line, we can get the μnCox\*W/L=442.731u/v, while W/L=0.5u/0.18u, μnCox=159.83u/V
* By finding the intersection point of the blue line and the maximum horizon line of the red line, we can find the Vth+(1/2θ), and θ will be θ=0.881

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVDS)/ID vs. VDS |
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* The brown line = ID vs VDS (0-1.8) and red line = (dID/dVDS)/ID vs. VDS
* When VGS=Vtn+50mV+1/(4θ) = 0.76v and VDS=1v, the points y= 269.5312m =λ/1+λVDS, which VDS=1, so λ=0.367

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| schematic |
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| (AC) IG&ID vs Freq |
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* Find the unity-Gain frequency (ft) using AC simulations. The brown line = IG, red line =ID
* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=50.118GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Vout(dB) vs freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²[(1+λVDS) approximate 1]=0.5\*442.731u/v\*(0.76-0.43) ²\*1= 24.106uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 26.418dB

1. For the nfetx transistor with W/L=5μ/0.18μ using 1 finger.
2. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVGS) vs. VGS |
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* Vth=0.422v
* μnCox\*W/L=5.45777m/v, while W/L=5u/0.18u, μnCox=202.13u/V
* Vth+(1/2θ)=850.84mv, and θ will be θ=1.16

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVDS)/ID vs. VDS |
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* When VGS=Vtn+50mV+1/(4θ) = 0.687v and VDS=1v, the points y= 340.82m =λ/1+λVDS, which VDS=1, so λ=0.515

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=50.118GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Ai vs. freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²(1+λVDS)=0.5\*5457.77u/v \*(0.687-0.422) ²\*(1+0.515)= 289uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 26.614dB

1. Repeat (1) for the nfetx transistor with W/L 5μ/0.18μ using 10 fingers (i.e. “width all fingers”=5μ  
   while “width single finger”=0.5μ).
2. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVGS) vs. VGS |
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* Vth=0.452v
* μnCox\*W/L=4.842m/v, while W/L=5u/0.18u, μnCox=174.31u/V
* Vth+(1/2θ)=1.021mv, and θ will be θ=0.878

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVDS)/ID vs. VDS |
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* When VGS=Vtn+50mV+1/(4θ) = 0.786v and VDS=1v, the points y= 251.908m =λ/1+λVDS, which VDS=1, so λ=0.335

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=59.7GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| (dID/dVDS)/ID vs. VDS |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²(1+λVDS)=0.5\*4.842m/v \*(0.786-0.452) ²\*(1+0.335)= 360uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 27.228dB

1. 4. Repeat (1) for the nfetx transistor with W/L=5μ/0.27μ using 1 finger.
2. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVGS) vs. VGS |
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* Vth=0.41v
* μnCox\*W/L=3.509m/v, while W/L=5u/0.27u, μnCox=189.49u/V
* Vth+(1/2θ)=0.989mv, and θ will be θ=0.863

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVDS)/ID vs. VDS |
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* When VGS=Vtn+50mV+1/(4θ) = 0.749v and VDS=1v, the points y= 111.328m =λ/1+λVDS, which VDS=1, so λ=0.146

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=28.18GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| (dID/dVGS)/ID vs. VDS |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²(1+λVDS)=0.5\*3.509m/v \*(0.749-0.41) ²\*(1+0.124)= 226uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 36.454dB

1. Construct the circuit below using pfetx transistor with W/L=0.5μ/0.18μ using 1 finger.

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自動產生的描述

1. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVSG) vs. VSG |
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* |Vth|=VSG =0.465v =-(VGS=-0.465v)
* μnCox\*W/L=-127.644u/v, while W/L=0.5u/0.18u, μnCox=46.08u/V
* Vth+(1/2θ)=1.161, and θ will be θ=0.718

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVSD)/ID vs. VSD |
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* When VGS=Vtn+50mV+1/(4θ) = 0.863v and VDS=1v, the points y= 274.955m =λ/1+λVDS, which VDS=1, so λ=0.377

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=17.782GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Vout(dB) vs freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²[(1+λVDS) approximate 1]=0.5\*127.644u/v\*(0.863-0.465) ²\*1.377= 13.92uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 24.699dB

6. Repeat (5) for the pfetx transistor with W/L=5μ/0.18μ using 1 finger.

1. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVSG) vs. VSG |
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* |Vth|=VSG =0.39v = (VGS=-0.39v)
* μnCox\*W/L=-1.505m/v, while W/L=5u/0.18u, μnCox=54.19u/V
* Vth+(1/2θ)=1.072, and θ will be θ=0.733

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVSD)/ID vs. VSD |
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* When VGS=Vtn+50mV+1/(4θ) = 0.781v and VDS=1v, the points y= 293.21m =λ/1+λVDS, which VDS=1, so λ=0.414

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=17.782GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Vout(dB) vs freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²[(1+λVDS) approximate 1]=0.5\*1.505m/v\*(0.781-0.39) ²\*1.414= 162.67uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 27.463dB

7. Repeat (5) for the pfetx transistor with W/L 5μ/0.18μ using 10 fingers

1. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVSG) vs. VSG |
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* |Vth|=VSG =0.436v = (VGS=-0.436v)
* μnCox\*W/L=-1.016m/v, while W/L=5u/0.18u, μnCox=36.58u/V
* Vth+(1/2θ)=1.146, and θ will be θ=0.704

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVSD)/ID vs. VSD |
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* When VGS=Vtn+50mV+1/(4θ) = 0.841v and VDS=1v, the points y= 280.583m =λ/1+λVDS, which VDS=1, so λ=0.388

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=17.782GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Vout(dB) vs freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²[(1+λVDS) approximate 1]=0.5\*1.016m /v\*(0.841-0.436) ²\*1.388= 115.65uA

* By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 23.177dB

8. Repeat (5) for the pfetx transistor with W/L=5μ/0.27μ using 1 finger.

a. VDS=1V. Sweep VGS from 0 to 1.8V, plot (dID/dVGS) vs. VGS, and extract Vtn, μnCox and θ.

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| schematic |
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| (dID/dVSG) vs. VSG |
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* |Vth|=VSG =0.441v = (VGS=-0.441v)
* μnCox\*W/L=-860.015u/v, while W/L=5u/0.27u, μnCox=46.46u/V
* Vth+(1/2θ)=1.229, and θ will be θ=0.634

1. VGS=Vtn+50mV+1/(4θ). Sweep VDS from 0 to 1.8V, plot (dID/dVDS)/ID vs. VDS and extract  
   λ at VDS=1V. Additionally, find the unity-gain frequency (ft) using AC simulations.

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| schematic |
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| (dID/dVSD)/ID vs. VSD |
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* When VGS=Vtn+50mV+1/(4θ) = 0.885v and VDS=1v, the points y= 155.046m =λ/1+λVDS, which VDS=1, so λ=0.183

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| schematic |
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| (AC) IG&ID vs Freq |
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* We can get the ft when current gain=1 ,which is IG=ID (the intersection), ft=8.912GHz

1. Reconfigure the circuit if necessary and find the intrinsic gain (Ai) using AC simulations  
   when VDS=1V and VGS=Vtn+50mV+1/(4θ).

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| schematic |
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| Vout(dB) vs freq |
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* Adding a current source (by square equation) which makes VDS close to 1v.

ID=1/2\*μnCox\*W/L(VGS-VT) ²[(1+λVDS) approximate 1]=0.5\*860.015u /v\*(0.885-0.441) ²\*1.183= 100.28uA

By measuring Vout (setting VGS AC magnitude= 1), we can get intrinsic gain Ai= 26.57dB

**Conclusion**

In this lab, we learn how to operate Virtuoso under Cadence to find the basic characteristics of the different parameters of NMOS and PMOS. Just like what the professor mentioned in class, understanding how to identify the basic characteristics of MOS transistors is essential for an engineer. Using ADE L, we can also compare the simulated values of the MOS transistors with the values obtained from hand calculations. In conclusion, we have gained a foundational understanding of how to use Virtuoso and have identified the basic characteristics of MOS transistors, which can be applied in future lab.