

ECE 474/704 Lab 4: Advanced Layout Design Techniques

Guard Rings

When laying out sensitive analog blocks, we need to help minimize the effect of substrate noise. One way to do this is with a guard ring, which is an array of substrate contacts that is connected to a clean supply (VDD, VSS or ground).

An example of a guard ring is shown in Figure 4-1. This example shows a ring with a single line of contacts. For more isolation, this ring can be made wider with more substrate contacts.

It is also important to note that the PMOS devices have an n-well contact ring surrounding them. This is good practice because it helps to act as an additional guard ring while also minimizing the possibility of latch-up between the n-well and substrate.

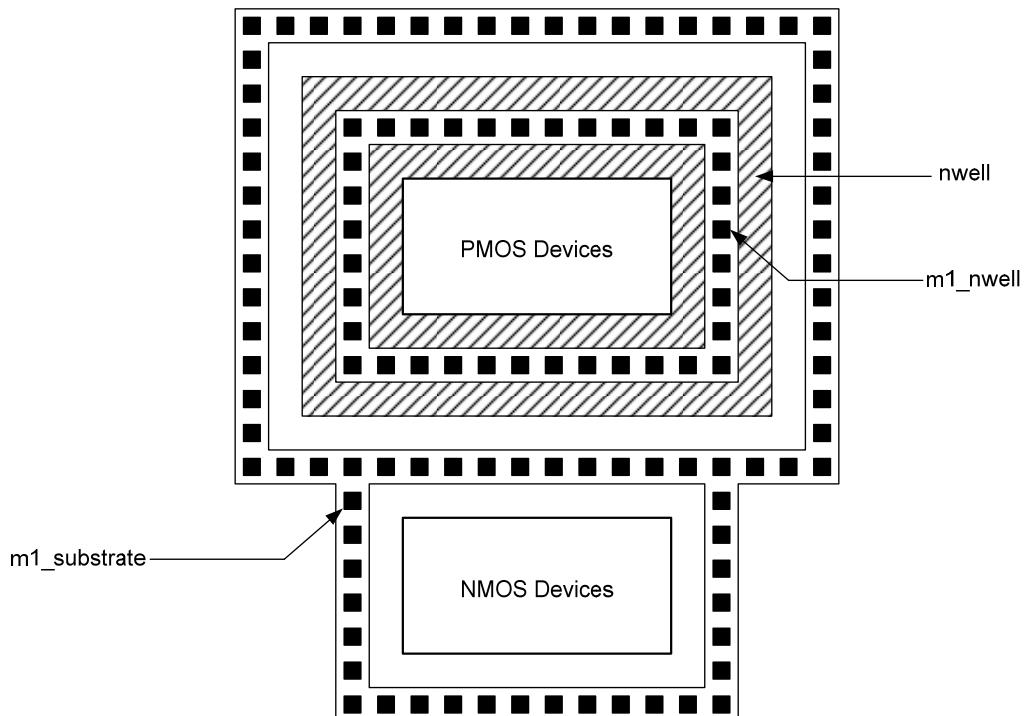


Figure 4-1: Guard Ring Illustration

For this lab, you will design a layout for the two-stage op-amp schematic in Figure 4-2 using good layout techniques with guard rings. Table 4-1 lists the transistor sizes and the capacitor value for the op-amp, whereas Figure 4-3 shows a suggested floor plan to use (note that the area for the capacitor is not drawn to scale). In this floor plan, each transistor has a finger width of 500 nm. One possible configuration for the placement of the dummy transistors is shown in Figure 4-4.

During the implementation of guard rings, if overlapping vias are used, they need to be exactly on top of each other if they are on the same metal layer (i.e. the "X" in the center should be perfectly aligned with the "X" of the other via to be stacked). Figure 4-5 shows an example of how the guard ring vias should intersect, and Figure 4-6 shows an example of stacked vias from "MT" to "M2". Do not forget to wire your innermost via (the one in the N-well) to the positive power rail and the outermost rings to the negative rail.

Table 4-1: Component Sizes

Device	W	L
M1	2u	270n
M2	2u	270n
M3	2u	270n
M4	2u	270n
M5	2u	270n
M6	1u	270n
M7	4u	270n
M8	20u	270n

C_c | 4pF

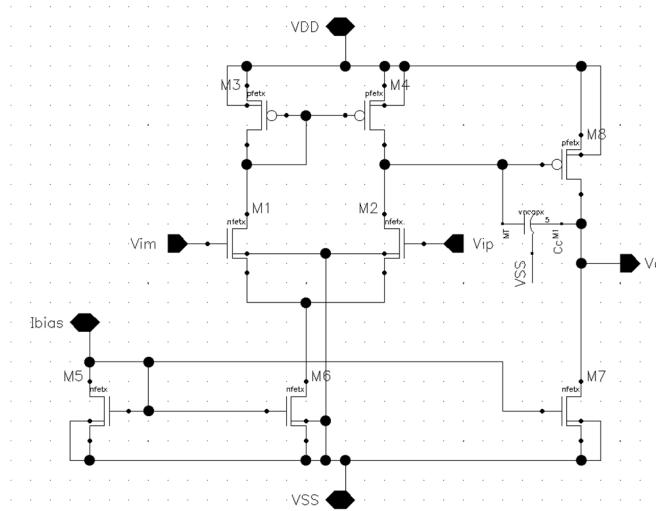


Figure 4-2: Two-Stage Op-Amp schematic.

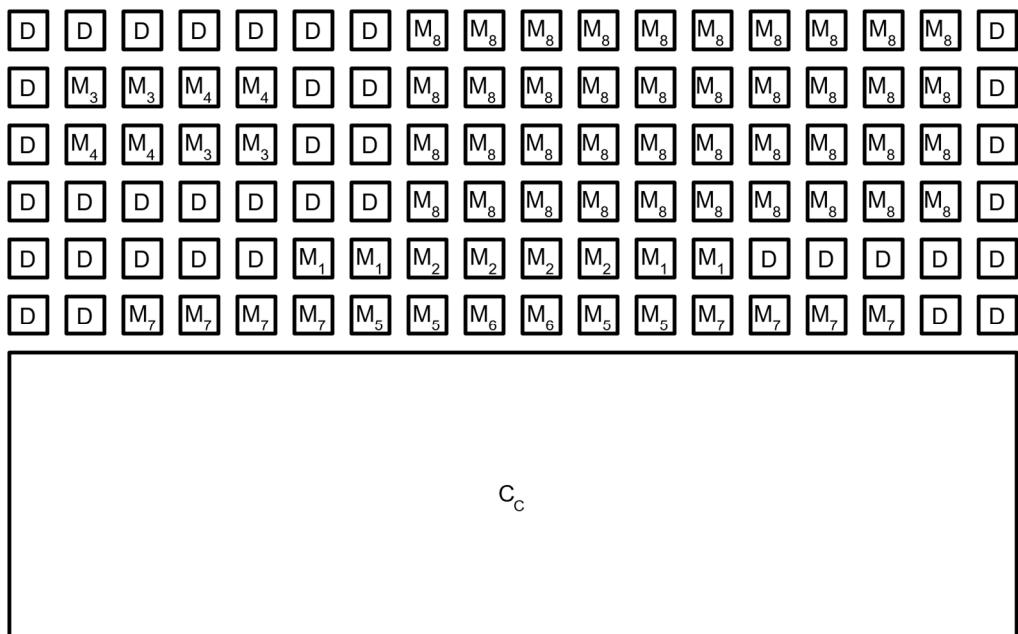


Figure 4-3: Floor Plan for Two-Stage Op-Amp. Space for capacitor is not drawn to scale.

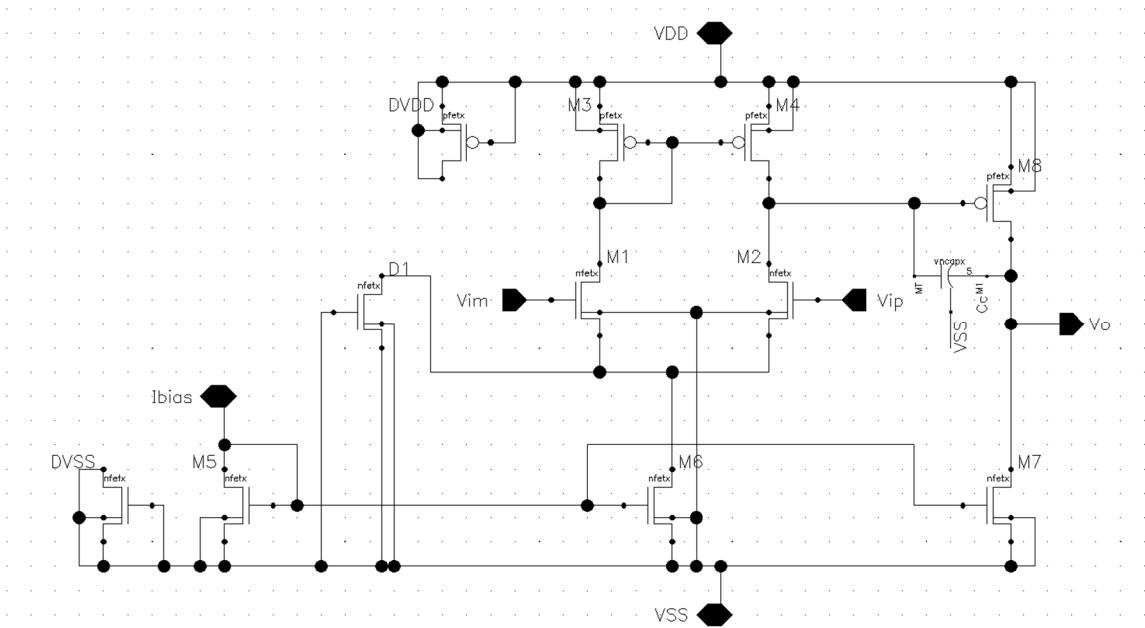


Figure 4-4: Op-amp Schematic showing Dummy Transistor placement

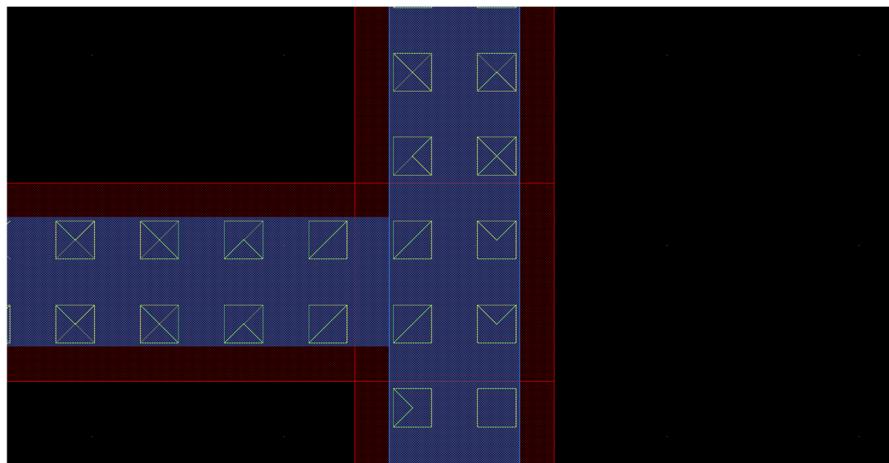


Figure 4-5: Intersection of Guard Rings

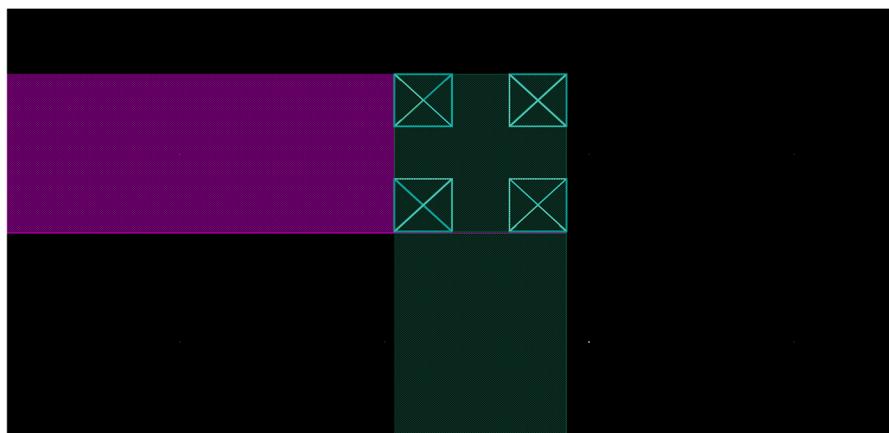


Figure 4-6: Example of Properly Stacked Vias

Note that a “finger” of a transistor in the floor plan is considered to be one gate terminal with a drain and source terminal on either side of it. Additionally, keep in mind that drains and sources can share the same diffusion area if they are connected to the same net in the schematic. But, it is not required that the same type of terminal be connected to the same net (e.g. a drain of one transistor and source of another are permitted to share the same diffusion area if they are connected to the same net).

To implement the capacitor in the layout, select **vncapx** from the **cmhv7sf** library, and set the "Bottom Level Metal" field to "M1" and the "Top Level Metal" to "MT". This will greatly reduce the size of the capacitor needed for the layout at the expense of using more metal layers in the process stack-up. Note that guard rings also need to be implemented for the capacitors. Refer back to Lab 3 for more information regarding the additional connections needed for the capacitor.

The guard rings are implemented with the M1_RX or M1_NW vias, depending on whether they surround the NMOS or PMOS devices, respectively. The guard ring serves as the substrate contact (the bulk connection) for the transistors in the same way as the M1_RX and M1_NW vias were used in Lab 2 to create the supply pins and transistor bulk connections in the inverter layout.

Before moving on to the next sections, create a layout of the amplifier that is clean of DRC violations (the layer of GRLOGIC will need to be added at this step to ensure that all errors are resolved). The remaining sections of this lab will add components that will also add DRC violations that should be resolved. Beginning with a clean layout before these additions will avoid confusion about the origin of the DRC violations. Once the initial layout is clean of DRC violations, a copy of the cell or of the individual cell views can be created for the below modifications. Creating a copy will provide you with a backup to which you can revert in the event that anything goes wrong or if any changes are too complicated to undo.

Input/Output (I/O) Pads

In order for the IC to interface with the outside world, pads need to be added to the layout. Because the ICs are often quite small, the IC will often be placed in a package which houses the IC to make it easier to handle, and the on-chip pads will then be connected by bond wires to another set of pads within the package. The package can be more easily placed on a PCB or breadboard to use the IC as part of a larger circuit. However, other methods of packaging and assembling ICs also exist depending on complexity and requirements regarding parasitic impedances.

The on-chip pad in this process is called **Pad** and exists in the **cmhv7sf** library. This cell does not have a schematic symbol associated with it, so it will only appear in the layout. The layout cell for the **Pad** component is shown in Figure 4-7.

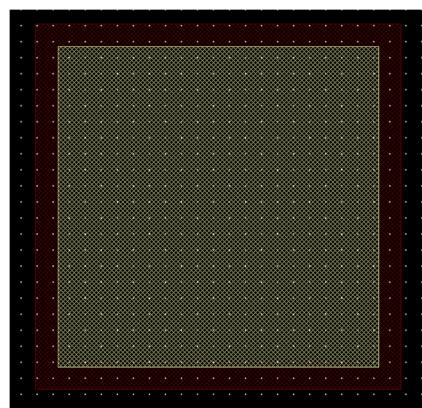


Figure 4-7: Layout view of the **Pad** cell for the IBM 180nm PDK

This pad is composed of two layers. The red layer in Figure 4-7 is the top-most metal layer, called “AM” in this process. The second layer is called “DV” and marks an opening in the passivation that covers the top of the chip. This opening exposes the top-most metal layer to the air so that electrical connections can be made to the pad.

Set the length and width of the pad to 114 μm . The “Pad Type” parameter should be set to “WB,” the “DV within AM Rule” parameter should be set to 7.0 μm , and the “WB pad size rules” should be set to the “Regular” option. **Begin by placing only two pads in the layout:** one for the VDD net and one for VSS. Try to avoid covering the amplifier or the capacitor with the pads. Placing pads above key components of the circuit can alter some of their electrical properties and/or affect the circuit’s reliability. This is due to the mechanical stress from the pads that is transferred to parts of the circuit in lower layers of the process. As such, it is often preferred not to cover parts of the circuit with a pad. In some instances (particularly with much denser and more complicated circuits), this cannot be avoided, in which case the mechanical stresses from the pad placement can lead to additional circuit variations that should be considered in design and testing, similar to process, voltage, and temperature (PVT) variations.

Once the pads are placed, connect them to the rest of the circuit with vias and metal routing. A “via stack” can be utilized to simplify the process of adding multiple layers of vias to traverse multiple layers in the PDK. From the via creation menu (“O” hotkey), select the “Stack” option for the “Mode” parameter at the top of the window. This will adjust the window so that you can select the start (lowest) and end (highest) layers that you want to connect in the process. The “end layer” should be set to AM if connecting to the pads. When traversing multiple metal layers at once, you should increase the number of rows and columns in the via stack to provide more than the minimum metal area needed in each of the intermediate metal layers (other PDKs may automatically handle this minimum area issue for via stacks). Connect the pads to the rest of the amplifier circuit and place a label on each pad corresponding to its pin in the schematic (remove any duplicate labels from elsewhere in the amplifier layout). You may need to create a rectangle of AM within the pad region to attach a label to it. After these steps are completed, you should have two pads, one labeled VDD and the other labeled VSS, and the pads should be connected to the rest of the amplifier layout, similar to what is shown in Figure 4-8.

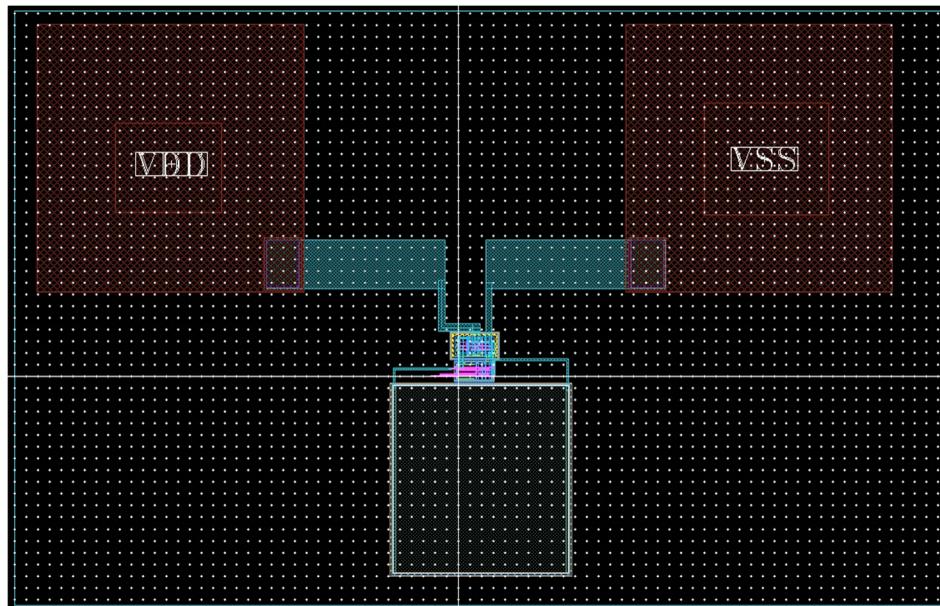


Figure 4-8: Example layout with two-stage amplifier and pads for VDD and VSS. The “VDD” and “VSS” labels have been highlighted and the DV layer ignored for better visibility.

Note that the addition of pads will increase the total capacitance at a net. Much like the parasitic capacitance between a capacitor's pins and the substrate (as described in Lab 3), a capacitor is created between the pad and the substrate. Particularly for high-performance and/or high-frequency circuits, this extra capacitance should be anticipated during the design process. Depending on how much parasitic capacitance is allowable in a design, a different, lower-capacitance pad structure may need to be used. However, for these labs the standard **Pad** cell will satisfy our requirements.

After the two power supply pads are added to the layout and connected to the circuit, you should find that additional DRC violations have appeared. Many of the DRC violations may be related to antenna rules (resulting from the increased metal area on some nets because of the pads) and/or to electrostatic discharge (ESD). ESD protection circuits must be added to the pads on the chip to protect the chip from damage during manufacturing, assembly, and testing. Additional details regarding ESD events and the circuits that must be added for ESD protection (and to resolve the new DRC violations) are discussed in the next section. We will return to the remaining I/O pads after setting up the ESD protections specific to the supply pads.

ESD Protections

ESD is an event during which a large current flows through the designed circuit, causing permanent damage to the chip. These events can completely disable a chip so that it does not function at all, disable some of the chip's functionality (depending on the size of the system), or greatly degrade the performance of the chip. In any of the cases, the chip will almost certainly need to be replaced with a new part if proper ESD protections are not in place.

ESD events occur when one or more of the chip pads accumulates a voltage (much greater than the breakdown voltages of the standard devices in the circuit) and finds a discharge path through the circuit to dissipate that voltage, thereby creating a large current that damages the chip. In order to mitigate the damage from ESD events, special devices and circuits must be placed on the chip to protect the main circuit from these events. Diodes are a common ESD protection device, among others, and serve to provide an alternative discharging path for the current while also limiting the voltage across the chip, thereby protecting the main circuit from damage. However, ESD protection circuits also add capacitance to pads or other pins in the circuit which can affect the circuit's performance, particularly for high-speed circuits. Therefore, the effects of this additional parasitic capacitance must be accounted for, and the process of adding ESD protections may have a trade-off with respect to certain aspects of the circuit's performance.

Students are encouraged to read the “ESD Reference Guide” for the IBM 180nm PDK for more information about the causes and models of ESD events and other ESD protection circuits. The type of ESD protection and/or the parameters of the protection circuits can also depend on the kind of ESD event that occurs. There are a few different types of ESD event models that are related to the different voltage levels and/or different processes that cause the voltage to accumulate and then discharge on the IC. Some of these models include the human body model (HBM) and the charged device model (CDM). Although the same core protection devices (i.e. diodes) can be used to accommodate both kinds of ESD events, the details of the setup may differ. The PDK documentation provides more details on the ESD event models, including the voltage levels involved, the mechanisms that cause them, and the different protections that may be needed.

While there are several kinds of ESD protection circuits, and the kinds that are available can vary between PDKs, in this lab we will primarily look at two common protection circuits: a double-diode network and a diode string. The double diode network is used for protection of I/O pads (with voltages between the high and low supply voltages) while the diode string is connected across the supply pads to provide a discharge path that does not pass through the main circuit. Example schematics for the two types of circuits are shown in Figure 4-9.

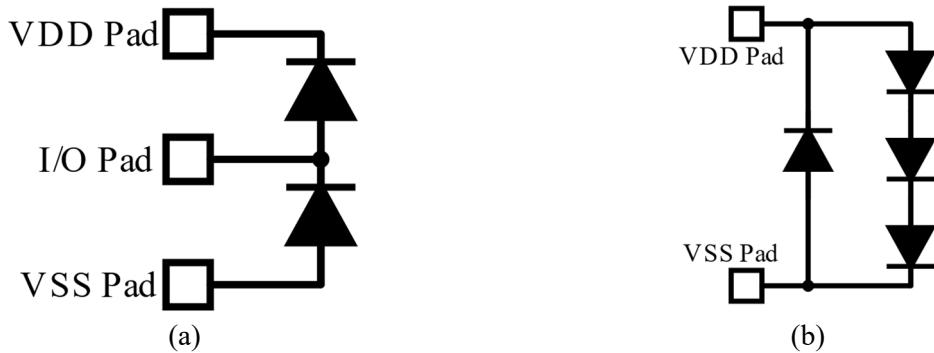


Figure 4-9: Schematics of (a) a double-diode network and (b) diode strings for ESD protections in the IBM 180nm PDK that will be used for this lab.

Before adding the necessary diodes, we need to label the power supply pads in the layout such that the DRC can identify the power supply pads for the ESD-specific rules. In the layer selection sub-window at the left of the layout viewer window, type “AM” into the search bar. In the list of AM layers that appears, select the AM layer with the “ESD” purpose, as shown in Figure 4-10.

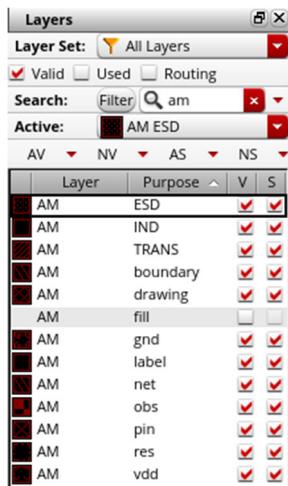


Figure 4-10: Selection of the AM layer with ESD purpose

Then, create a label (from *Create → Label...* or with the Shift-L hotkey), and in the label creation menu, type “ESD_POWER” for the label text, and select “use current entry layer.” You may also want to change the height (the font size) and/or font of the label to make it more visible. A height of 5 to 10 should be suitable, and the “roman” font may stand out more than the standard font option, but these changes are not necessary when creating the label. The label creation options may look like those shown in Figure 4-11. Once the label options are selected, hide the window and create two “ESD_POWER” labels, one attached to each power supply pad. Note that this method of marking the power supply nets for the ESD-related rules in DRC is unique to the IBM 180nm PDK. Different PDKs will, in general, have their own method of doing something similar to ensure ESD protections are properly implemented.

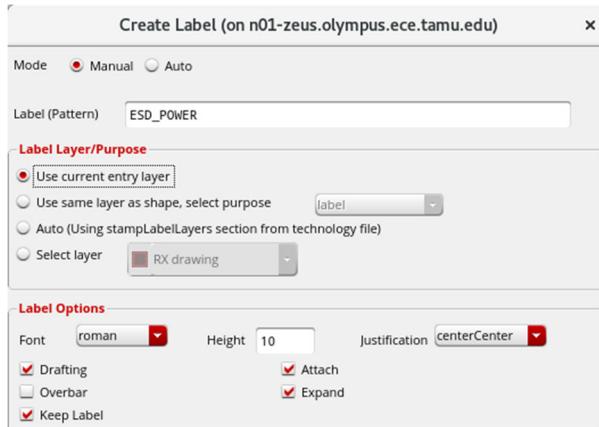


Figure 4-11: “ESD_POWER” label setup

Now we will add the diode strings to the schematic and layout. For the diode string, two different types of diodes should be used. The first is an N-well-to-substrate diode, for which we will use the **esdndsx** component from the **esd7hv** library. **See the Appendix for instructions regarding how to create the correct layout cell for this diode.** This diode will have the anode connected to VSS and the cathode connected to VDD (i.e. the diode will “point” from VSS to VDD). Normally, the dimensions of the diode should be chosen according to the voltage and current that could be expected in the ESD event. However, for the purposes of this lab we will begin by using the default dimensions of the diode. Place the diode in the schematic and layout, and connect it accordingly. The layout cell has “A” and “C” labels to mark the anode and cathode terminals, respectively. An N-well guard ring connected to VDD should be placed around the **esdndsx** diode.

For the other diode string connected in the direction from VDD to VSS, a second type of diode is needed which is a P+-to-N-well diode constructed in a deep N-well. The deep N-well provides more electrical isolation from the substrate at the expense of added capacitance at the junction between the deep N-well and the substrate. The component for this diode is called **esdpdidn** and is also found in the **esd7hv** library. **Enable the “external substrate ring” option to generate one of the correct forms of the layout instance for this diode.** This will also add a guard ring connected to the substrate around the diode, and this guard ring needs to be connected to VSS. When creating the **esdpdidn** components, you may find it helpful to enable the following options in the schematic and layout instance properties: “extend connection” and “connect terminals.” Enabling these properties will increase the metal contact area of the anode and cathode terminals and will join them together in the M3 metal layer. These options will increase the area of the device in the layout, but they may simplify the process of connecting the diodes to the rest of the layout.

3 diodes are needed for this second string from VDD to VSS. This causes the total forward voltage to be just above the nominal 1.8V supply before conduction will occur, allowing the circuit to operate normally without a significant increase in supply current while still providing protection from ESD events. For different processes, a different number of diodes would be needed to create a forward voltage that will provide appropriate protection without interfering with operation using the nominal supply voltage. Additionally, the diodes would typically need to be made larger (approximately 3 times larger) to maintain a similar total resistance in the discharge path created from the string of 3 diodes. However, for the purposes of this lab, we will ignore these considerations since this is intended to serve only as an introduction for the implementation of ESD protections.

Finish adding the diode strings to the schematic and layouts. The schematic should look similar to what is shown in Figure 4-12. Ensure that the DRC is clear and check that LVS passes before proceeding (make sure that the layout is still covered by a layer of GRLOGIC). Additionally, note that spacing between some

components (particularly between transistors) in the layout may need adjustments and additional guard rings may need to be added around the amplifier layout in order to clear the DRC violations. Because of the connections to I/O pads, additional rules are checked to ensure that the circuit will not experience damage in different forms. One form of damage that is of particular importance is latch-up – a condition where a pair of parasitic BJTs are activated and create a low-resistance path between the supply pins which will damage the integrated circuit.

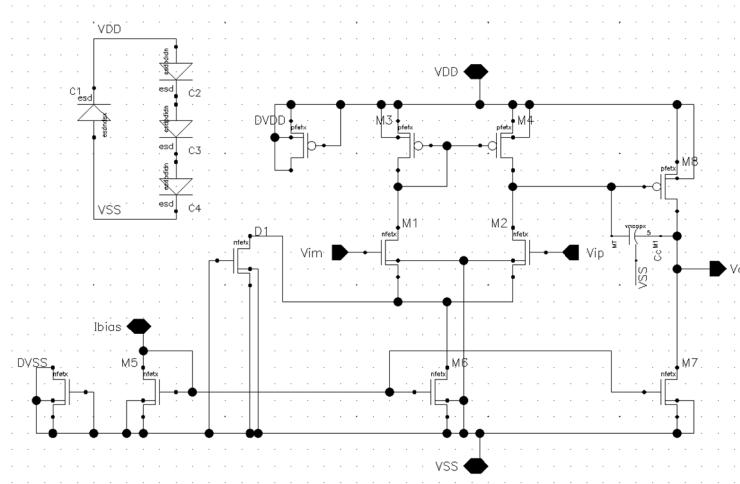


Figure 4-12: Amplifier schematic with addition of diode strings for ESD protection (recall that the **Pad** cell does not have an associated schematic symbol).

Now, we can begin to add the remaining I/O pads (Vip, Vim, Ibias, and Vo) and the associated double-diode networks. In the double-diode network, the **esdnidx** component is used for the connection between VSS and the I/O pad while the **esdpdidn** component is used for the connection between the I/O pad and VDD. As before, the **esdnidx** component in the layout needs to be surrounded by an N-well guard ring connected to VDD in order to prevent latch-up and satisfy latch-up-related design rules (there should be at least 3.5um of space between the P+ regions of the diode, made with the BP layer, and the N-well guard ring to satisfy some of these design rules). Begin by adding a double-diode network to the “Vo” net to the schematic, as shown in Figure 4-13. Add the corresponding pad, diodes, and connections to the layout as well. When placing the ESD diodes, it will be acceptable to place them underneath their respective pads in the layout to save space if needed. Once completed, the layout should have 3 pads with associated ESD. Before proceeding, make sure that you have a clean DRC and passing LVS.

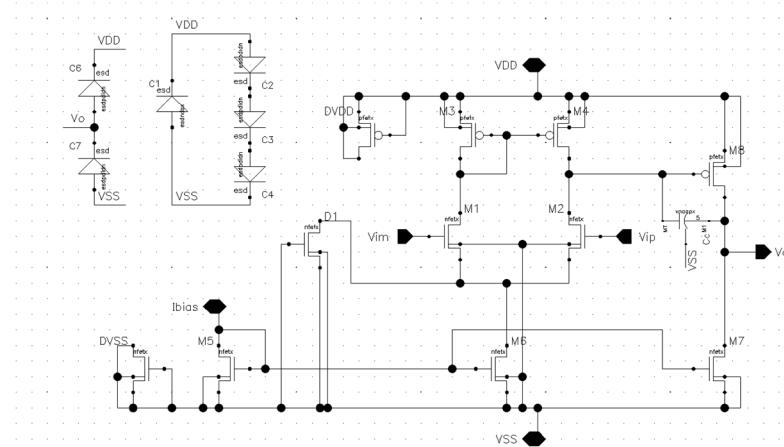


Figure 4-13: Schematic with the addition of double-diode network for “Vo” pin

The ESD circuits for the remaining I/O pads (Vip, Vim, and Ibias) require an additional set of steps. Because these pads are connected to gates of transistors, another layer of ESD protections is needed. The first layer is the same double-diode network that was implemented for the Vo pad. So, this double-diode network will still be connected directly to the I/O pad. This network protects the IC against ESD events that are better described as HBM events. The second layer of protection is a resistor followed by a second double-diode network. These components are designed to protect against CDM events. The combination of the two double-diode networks and the resistor will look like what is connected to the Vip, Vim, and Ibias pins in Figure 4-14. This shows an example of what the completed amplifier schematic should look like with all of the ESD circuits for the minimum necessary protection. Note that some of the pins in the schematic have moved positions to reflect the additional ESD circuits that are placed between the I/O pads and the signal's location on the original circuit (see Figure 4-2 and Figure 4-4).

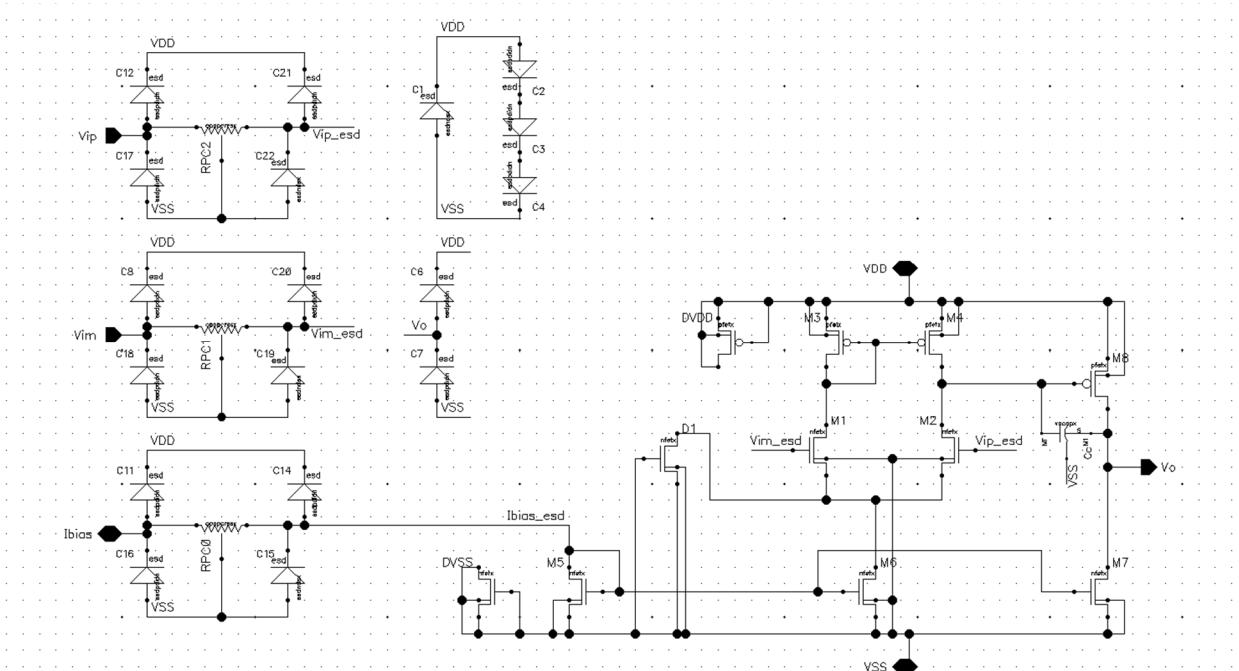


Figure 4-14: Op-amp schematic with all ESD circuits to accommodate the I/O pads in the layout

With the pads for each schematic pin added to the layout, begin by adding the first double-diode network, as was done previously for the Vo pad. The resistor that needs to be added for the CDM protection is the **oppccresx** component from the **cmhv7sf** library. Make sure that the resistor component has a third terminal, and connect this third terminal to the substrate potential (which should be VSS), as was done in Lab 3. As with the diodes, the dimensions of the resistor should be chosen according to the anticipated voltage and current levels that could be experienced during an ESD event. For the purposes of this lab the default dimensions and default value of the resistor should be suitable. Large currents can occur through the diodes during an ESD event. The addition of the resistor creates a voltage divider that results in a voltage at the gate which does not damage the transistors.

With the resistor added, the next double-diode network can be added to the schematic and layout. As before, connect the **esdnndsx** diode between VSS and the intermediate node (which is now connected to the resistor and the original pin location) and connect the **esdpdidn** diode between the intermediate node and VDD. Remember to include the N-well connected to VDD around the **esdnndsx** diode in the layout. However, in order to clear the related design rules for the CDM protection circuits, some properties of both diodes need to be altered. In the schematic and layout properties of both diodes for the CDM protections, check the box

next to “ESD HBM(nil) CDM(t)?” near the top of the properties list. In the layout, this will add a new layer around the diodes that marks them as CDM protection elements, thereby enabling DRC to verify that the CDM protection circuits are properly constructed.

Complete the process of adding the I/O pads and the necessary ESD protection circuits for all remaining pins of the amplifier. Adjust the layout and/or schematic until all DRC violations are cleared (with the exception of density violations) and make sure that LVS passes.

Lab Report

1. Schematic printout
2. Layout printouts. Include the following images: one of the whole layout area, a close-up showing the PMOS portion of the layout, and a close-up showing the NMOS portion of the layout (include guard rings in the images of the PMOS and NMOS portions).
3. Screenshot of DRC RVE window filtered to “show unresolved” (refer to Lab 2 if necessary).
4. LVS printout showing that layout and schematic match (remember to include the NetID and timestamp in the screen capture). **Recall that the use of the capacitor in the schematic and layout will require the alternative LVS method described in Lab 2 to get a passing LVS.**

Appendix: Instantiating the Correct ESD Diode Cells in Layout

There is a bug in the setup of the IBM 180nm PDK that causes ESD diodes used in this lab (**esdnndsx** and **esdpdidn**) to be incorrectly constructed when they are initially placed in the layout viewer. The incorrect layout cells look like what is shown in Figure 4-15. The problem is the guard ring that appears around the devices. It is not supposed to be present in the respective definitions for each cell, and it is placed too close to the anode and cathode diffusions for some of the design rules. This bug is a particular problem for the **esdnndsx** diode because there are no options for the instance that pertain to this guard ring.

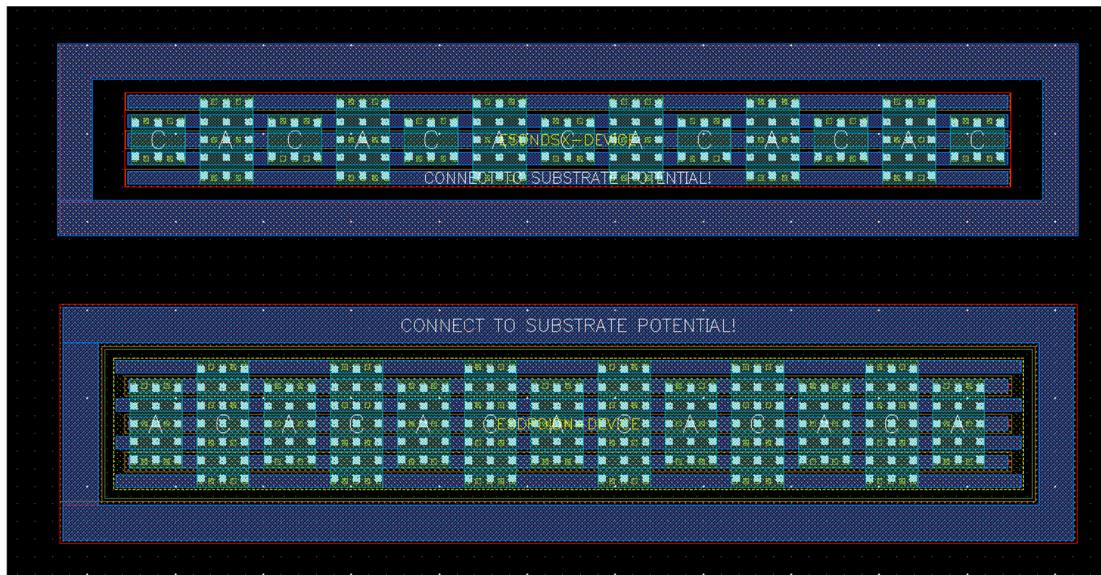


Figure 4-15: Incorrect layout cells for the **esdnndsx** diode (top) and the **esdpdidn** diode (bottom)

In order to get the correct layout cell of both diodes, we first need to create an instance of the **esdpdidn** diode. In the properties for this component, find the text saying “External Substrate Ring?” and check the associated box, then place the component in the layout. The **esdpdidn** diode layout cell should appear similar to what is shown in Figure 4-16. This is also one of the correct forms of the **esdpdidn** diode layout.

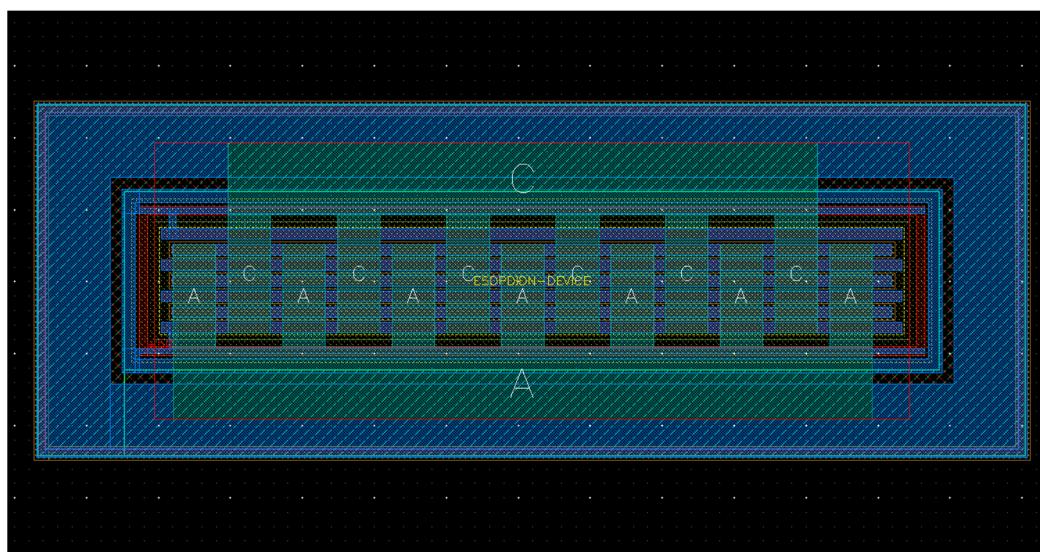


Figure 4-16: Example layout view of the **esdpdidn** diode cell with the external substrate ring

Now, select the **esdpdidn** diode that was just created (remember to use Ctrl-d to deselect all other elements), open the layout instance properties, go to the “Attribute” tab in the properties window, and then click the “Browse” button next to the “Library” line. A library browser window should appear. From this window, select the **esdndsx** component within the **esd7hv** library, make sure that the “layout” view is selected, and then click “Close” in the library browser window. Ensure that the “Cell” field of the instance properties now says **esdndsx** (the field should also be highlighted in blue to indicate that a change has been made), and if this is the case then click “OK” in the properties window. Depending on the other properties selected for the component, the **esdndsx** diode should appear similar to what is shown in Figure 4-17. Note that the substrate ring that was present in Figure 4-15 has disappeared. This is the correct layout view of the **esdndsx** diode.

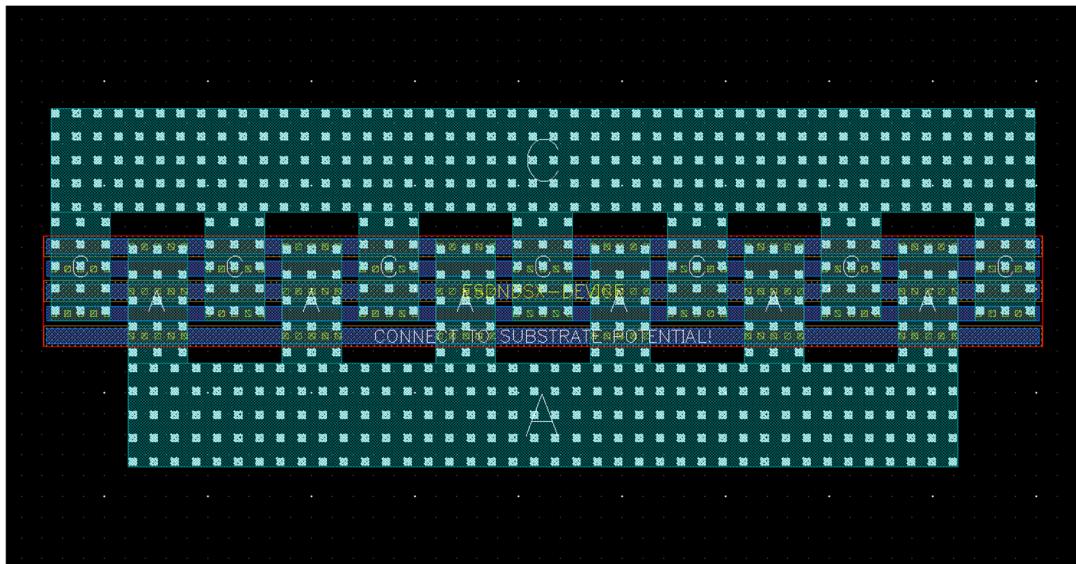


Figure 4-17: Example of the correct layout cell for the **esdndsx** diode

This procedure should only be needed once during a Cadence session. Once this step is completed, you should be able to correctly generate a layout instance of the **esdndsx** diode using the “I” hotkey for the remainder of the Cadence session, and the **esdndsx** diode that was just created can be deleted if it is not needed. If a new Cadence session is initialized, this procedure will likely need to be performed again to generate the correct form of the **esdndsx** diodes in the layout view.