25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

Lab5: Equalization Circuits

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1. TX FIR Equalization. This problem investigates TX FIR equalization using the 12” Backplane channel “peters\_01\_0605\_B12\_thru.s4p” from course website. For parts (a) and (b), use the example MATLAB code “channel\_data\_pulse\_pda.m” and produce the following 2 graphs:

a) Peak-Distortion Eye Height versus FIR tap number at 4G, 8G, and 16Gbps (3 lines). For the tap numbers, use 1-tap (no equalization), 2-tap (1-post), 3-tap (1-pre and 1-post), and 4-tap (1-pre, 2-post). Don’t restrict the TX equalizer resolution for this graph.

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| 4G-1tap (No equ) | 4G-2tap (1post) |
| 4G-3tap (1pre&1post) | 4G-4tap (1pre&2post) |
| 8G-1tap (No equ) | 8G-2tap (1post) |
| 8G-3tap (1pre&1post) | 8G-4tap (1pre&2post) |
| 16G-1tap | 16G-2tap (1post) |
| 16G-3tap (1pre&1post) | 16G-4tap (1pre&2post) |

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b) 8Gb/s Peak-Distortion Eye Height versus Equalizer Resolution with 2, 3, and 4-tap equalization (3-lines). For the tap resolution sweep, use 3, 4, 5, 6 bits, and also include the infinite resolution data. Note: The above MATLAB code also requires the “tx\_eq.m” function. Also, this MATLAB code is only a reference code. Feel free to modify and improve upon the code as you wish.

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| 8G 2tap (1post) 3bit resolution | 8G 2tap (1post) 4bit resolution |
| 8G 2tap (1post) 5bit resolution | 8G 2tap (1post) 6bit resolution |
| 8G 3tap (1post 1pre) 3bit resolution | 8G 3tap (1post 1pre) 4bit resolution |
| 8G 3tap (1post 1pre) 5bit resolution | 8G 3tap (1post 1pre) 6bit resolution |
| 8G 4tap (2post 1pre) 3bit resolution | 8G 4tap (2post 1pre) 4bit resolution |
| 8G 4tap (2post 1pre) 5bit resolution | 8G 4tap (2post 1pre) 6bit resolution |

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c) Design an 8Gb/s TX Driver with Equalization [4]. Modify one of your drivers from Lab3 to include FIR equalization.

i. The maximum output voltage swing can be anywhere from 300mVppd (min.) to 1Vppd (max.). This gives you the flexibility to choose whichever driver you wish – from low-swing voltage-mode to current-mode.

ii. Use the results from part (a) and (b) to justify your tap number and resolution.

iii. Include two 8Gb/s PRBS eye diagrams – one without equalization (all weight on main cursor) and one with the proper equalization taps enabled. Import the s parameter file into your Cadence simulation to produce the eye diagrams. Make sure the channel is properly terminated at both ends. Note, as you will have some additional driver capacitance, the equalization taps may change slightly.

iv. The driver and at least one pre-driver stage should be full-transistor level design. The other blocks (PRBS, delay elements, etc) can be macro-models.

v. Report transmitter power consumption, power efficiency (mW/Gb/s), and 8Gb/s eye height and width.

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2. RX CTLE Equalization. Design an 8Gb/s active CTLE to meet the following specifications:

a) Min peak gain at Nyquist (4GHz) of 6dB

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b) Zero frequency tunable from a minimum range of 500MHz to 1GHz

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c) Minimum tunable peaking (magnitude difference between Nyquist and low frequency response) range of 12dB (Example: +6dB at Nyquist frequency and -6dB at low frequency).

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d) Load capacitor = 25fF i. Produce frequency response plots showing the zero and peaking tunability. ii. Produce an 8Gb/s PRBS eye diagram with the 12” Backplane channel output as the input to the CTLE. Optimize the CTLE settings for optimal eye opening.

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| No CTLE |
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3. RX DFE Equalization. Design an 8Gb/s 2-tap DFE [2][3].

a) Use one of the comparators you designed in Lab4 in your design. Note, you probably have to speed this design up – as you will need a 4GHz clock if you implement a half rate design.

b) The only thing that has to be transistor level is the comparator. The rest of the blocks (summer, feedback taps, other logic) can be macro-models. Note, for the summer model make sure to capture the RC settling if you use a linear resistive load summer. Feel free to investigate an integrating architecture if you prefer.

c) Produce an 8Gb/s PRBS eye diagram at the summer output with the 12” Backplane channel output as the input to the DFE. Optimize the DFE settings for optimal eye opening at the input of the comparator (summer output).

d) Report DFE power, power efficiency (mW/Gb/s), and 8Gb/s eye height and width. e) Note, you have to synchronize the DFE with the incoming data stream. A good way to do this is with an initial “lone pulse” input pattern. Adjust your comparator clock to sample near the peak of the lone pulse. Then simulate with the PRBS data.

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