

25 Spring ECEN 720: High-Speed Links: Circuits and
Systems Post-lab Report

Lab6: Link Modeling with ADS

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Section:700

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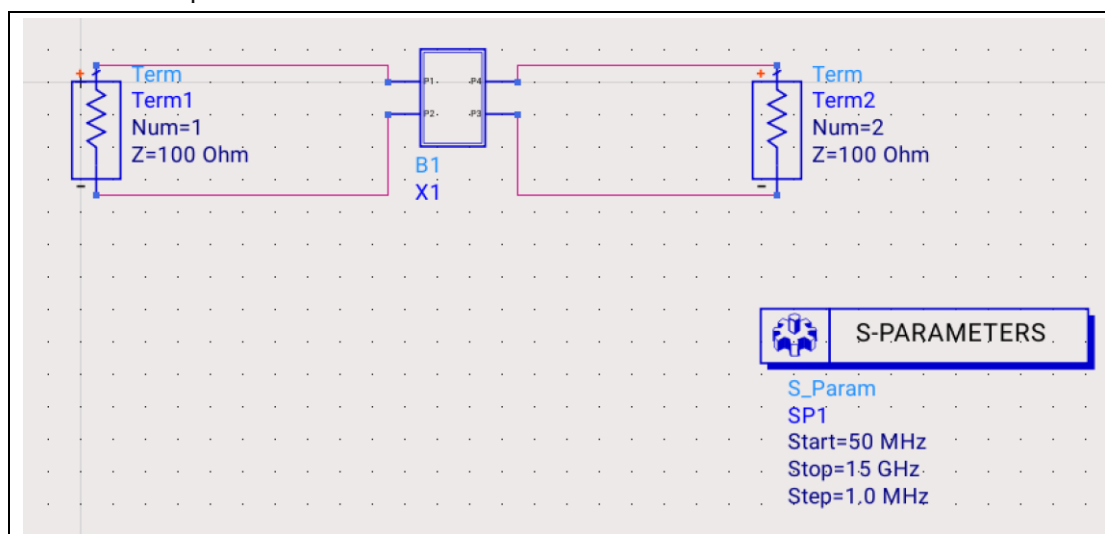
1. Using the ADS, analyze the following test cases. Use 1" Backplane s-parameter (B1). At 8Gb/s, include packaging parasitic as depicted in Figure 5 for chip-to-chip interconnect. Assume 500um Bonding wire with bonding pad capacitance of 200fF, and neglect the mutual wire inductance and pin parasitic for realistic termination modeling. Please, refer to [2] for step-by-step guide on using ADS for Signal Integrity Design. For all test cases use 1Vpp swing at TX.
 - (a) Using ADS, plot Insertion Loss and Return Loss from 50MHz to 15GHz. Compare with MATLAB plot.
 - (b) Show eye diagrams, and BER contours, and BER bathtub curves both in time and voltage for the following test cases. Include all schematics on the lab report. - - -

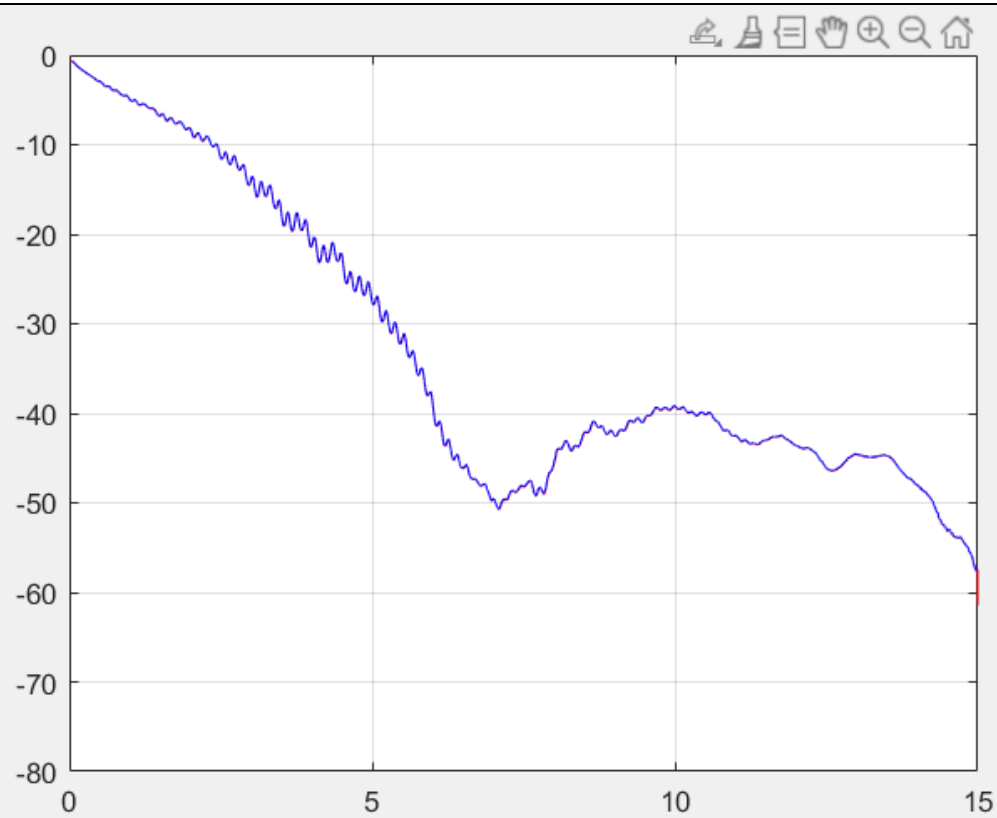
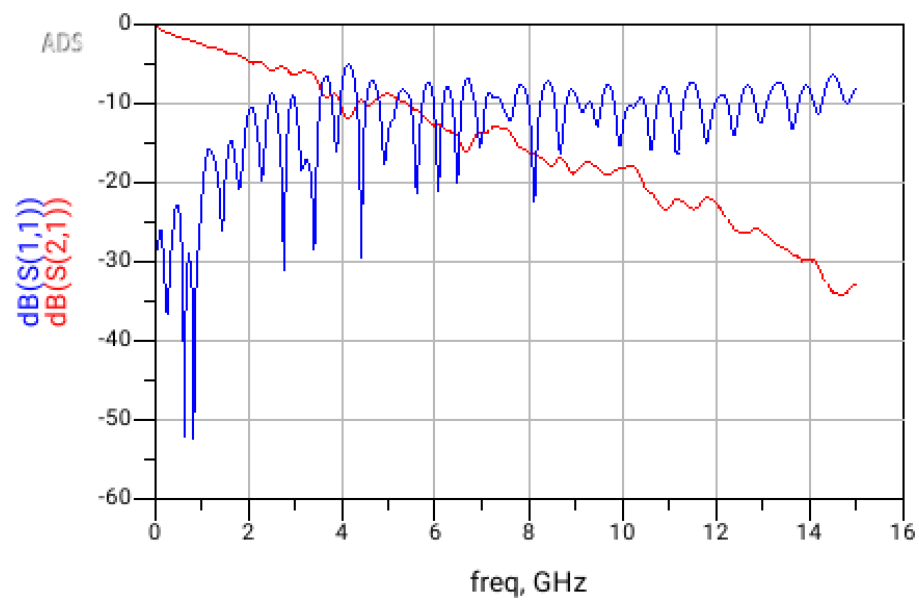
Case 1: Only the forward channel (thru channel) including TX and RX with ideal 100Ω differential terminations without any cross talk.

Case 2: Use the forward channel in Case 1 with an aggressor (FEXT1, NEXT1) terminated with an ideal 100Ω differential load.

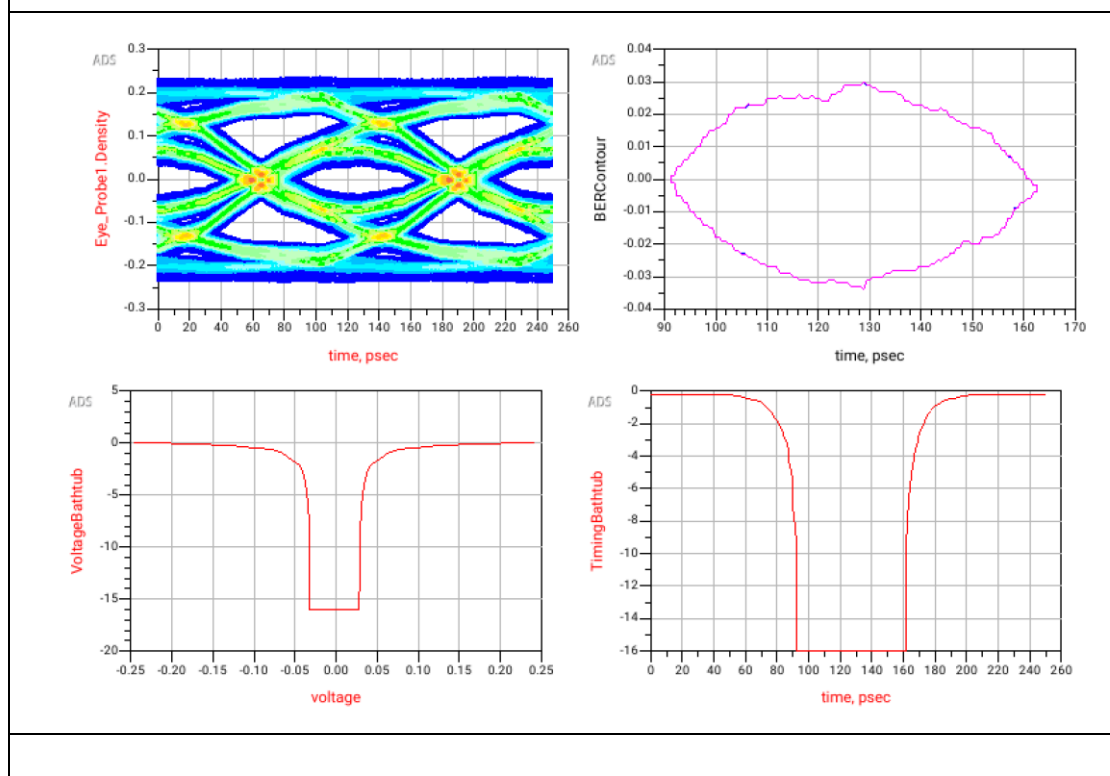
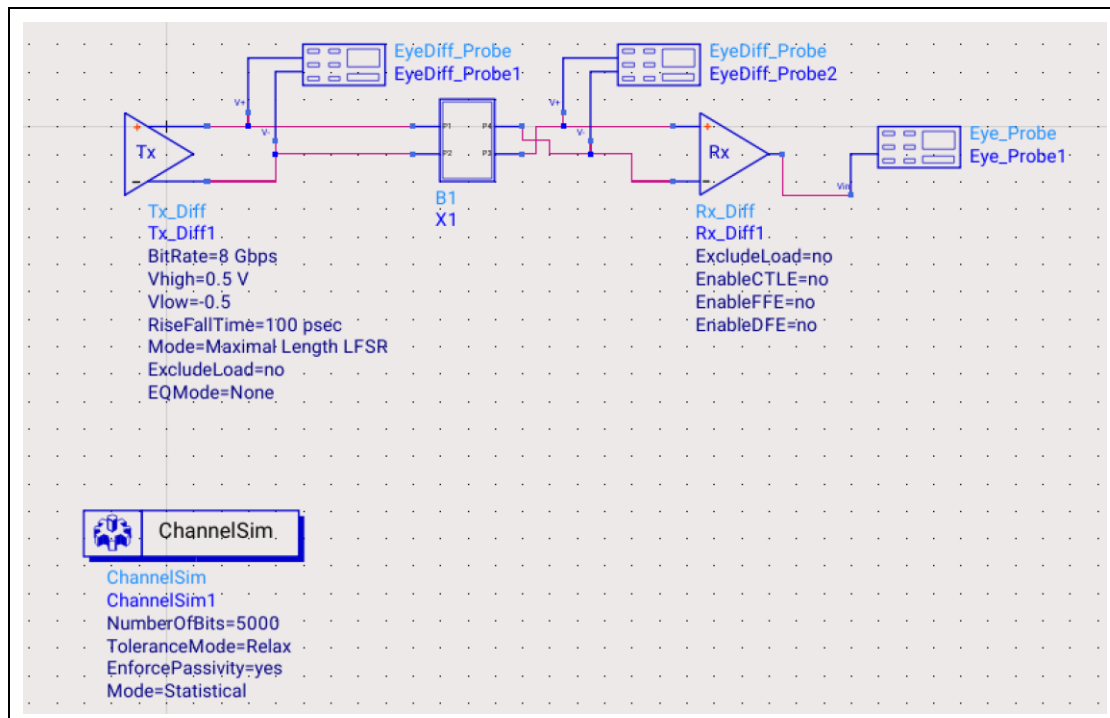
Case 3: Use the forward channel in Case 1 with realistic terminations (i.e. including parasitics).

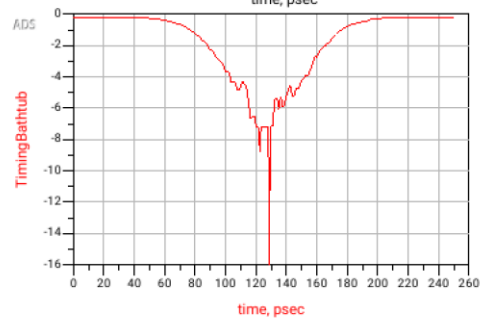
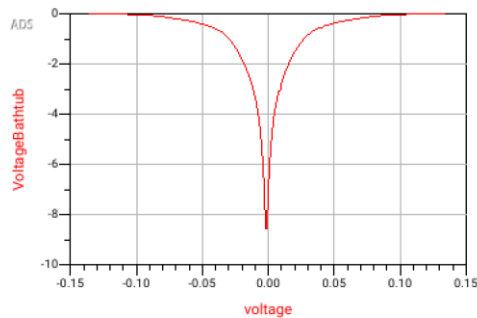
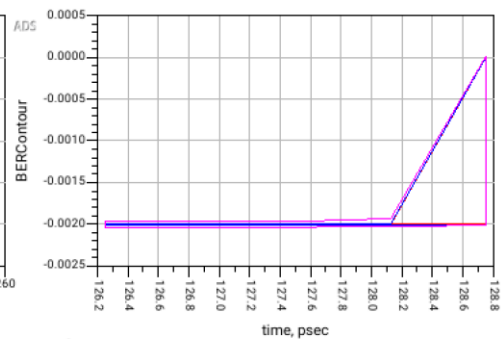
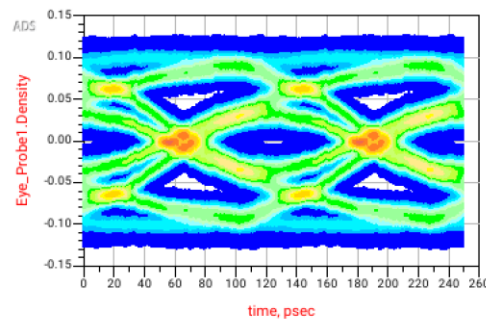
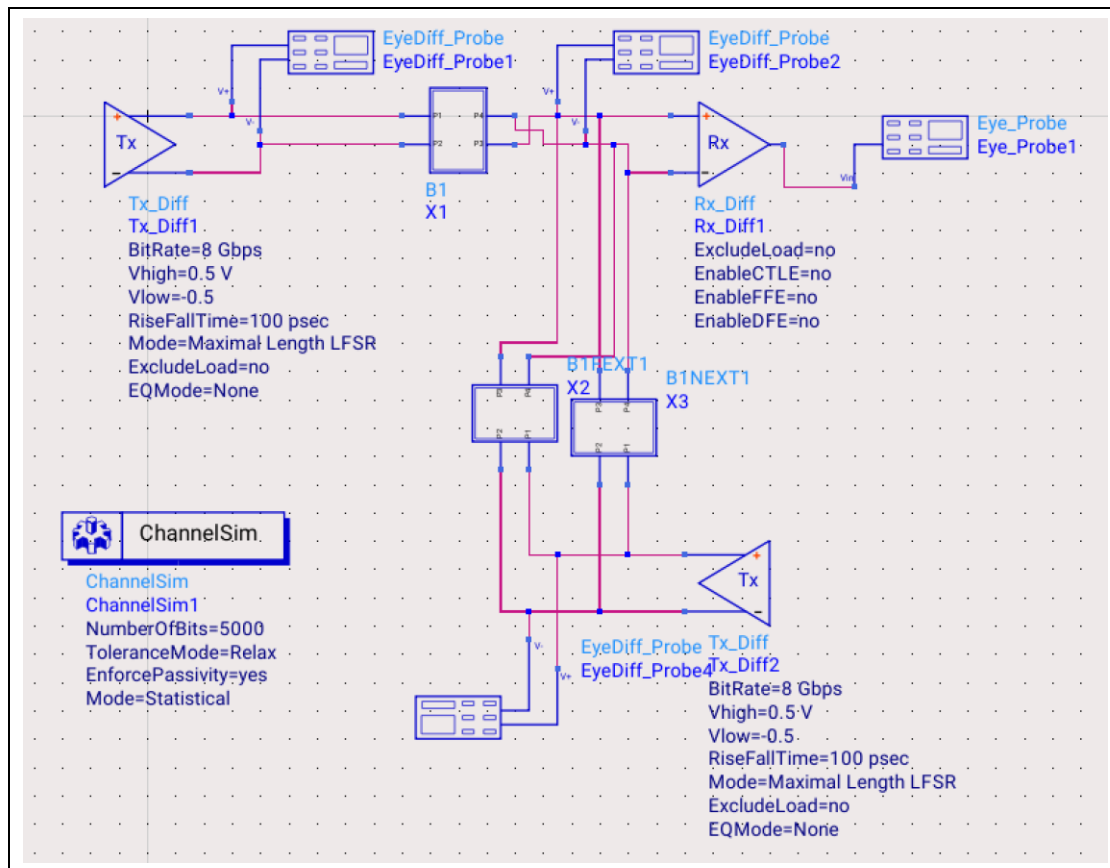
Case 4: Use the forward channel with an ideally terminated aggressor similar to Case 2 with realistic terminations (i.e. including parasitics).
 - (c) Repeat (b) with non-ideal transceiver jitter properties,
 - TX
 - DCD = 0.04UI; Clock DCD = 0.04UI
 - RJ = 0.01UI
 - Load = 100 Ohm
 - De-emphasis = 3dB
 - RX
 - No FFE, No DFE
 - Load = 100 Ohm
 - RJ = 0.01 Sigma
 - Amplitude noise = 1mV

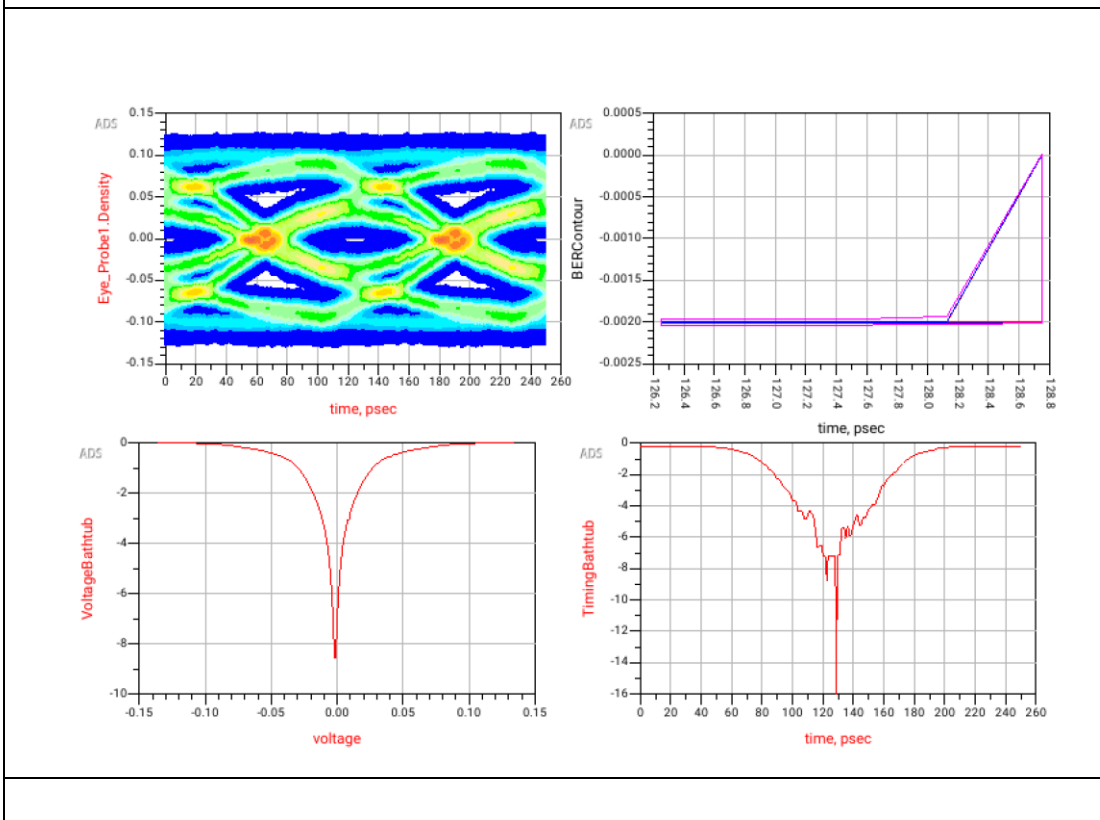
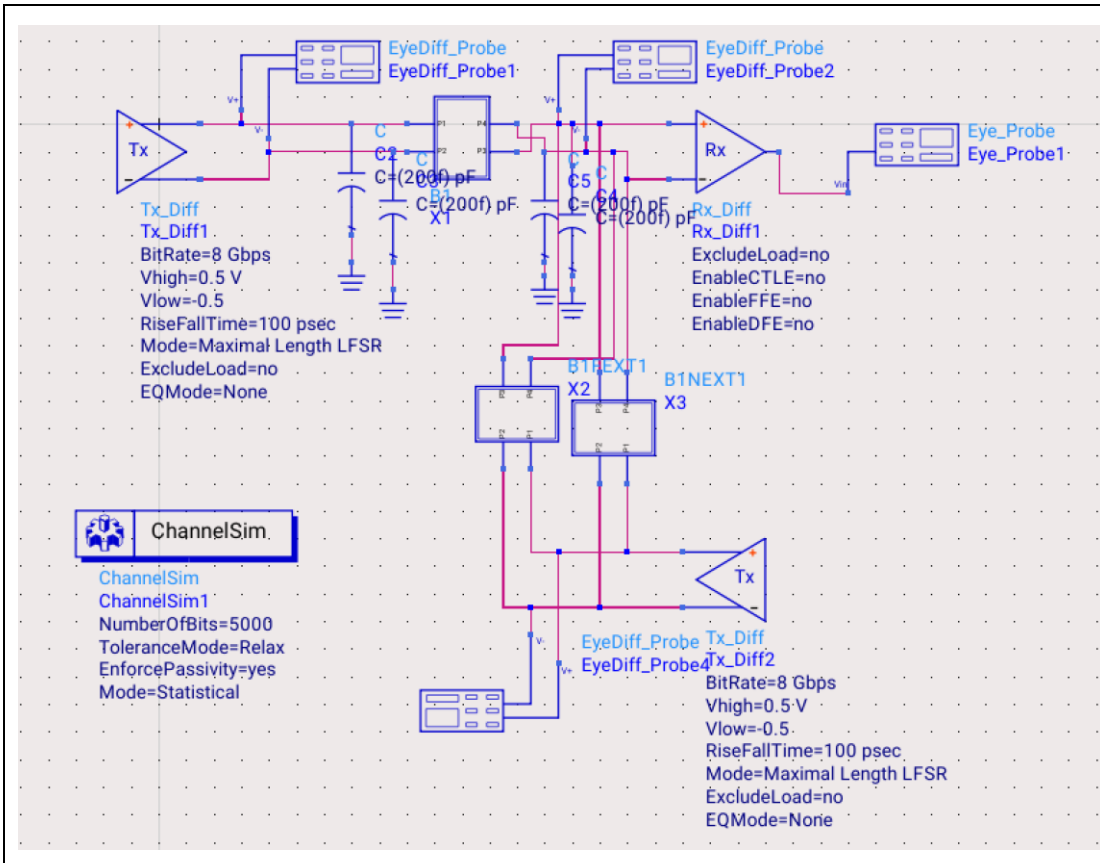


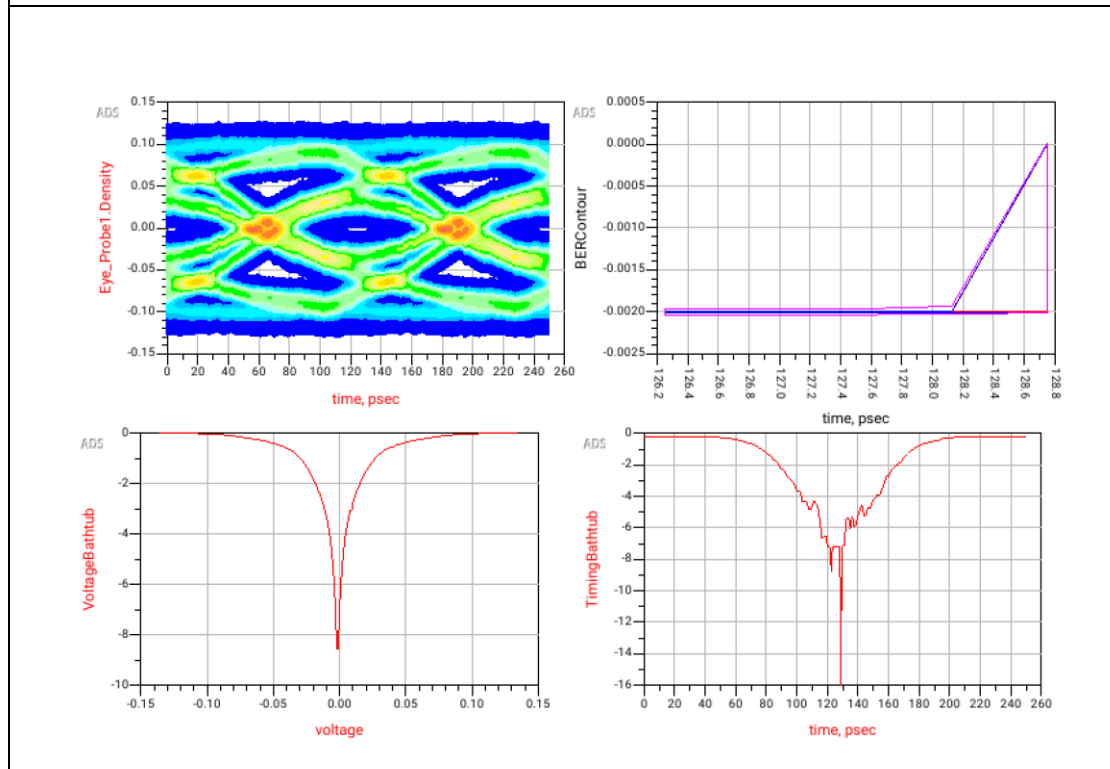
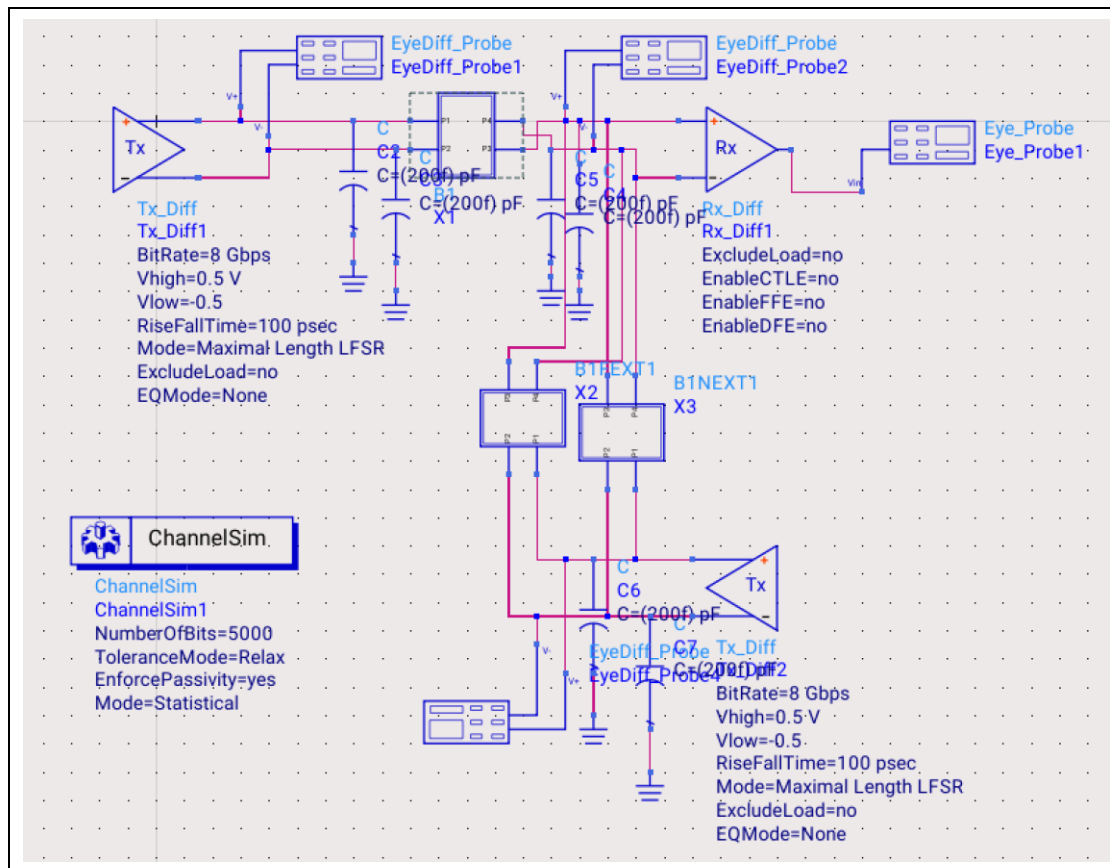


B

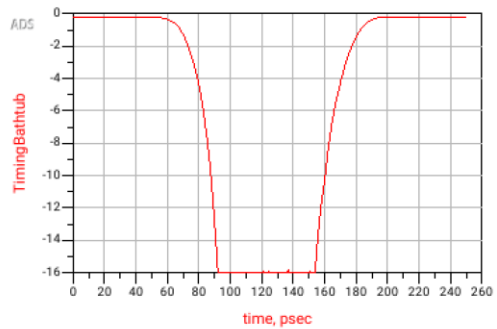
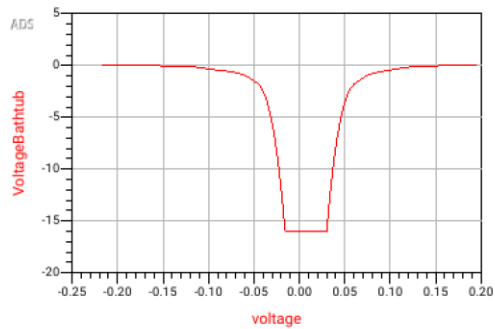
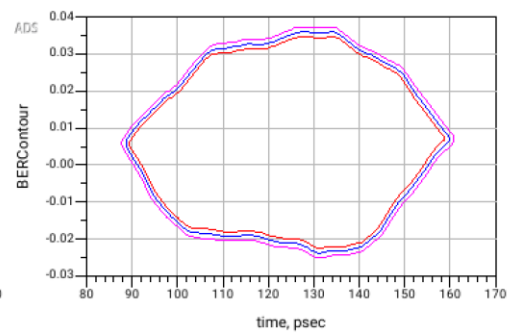
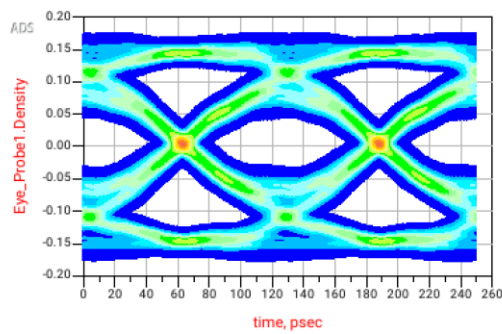
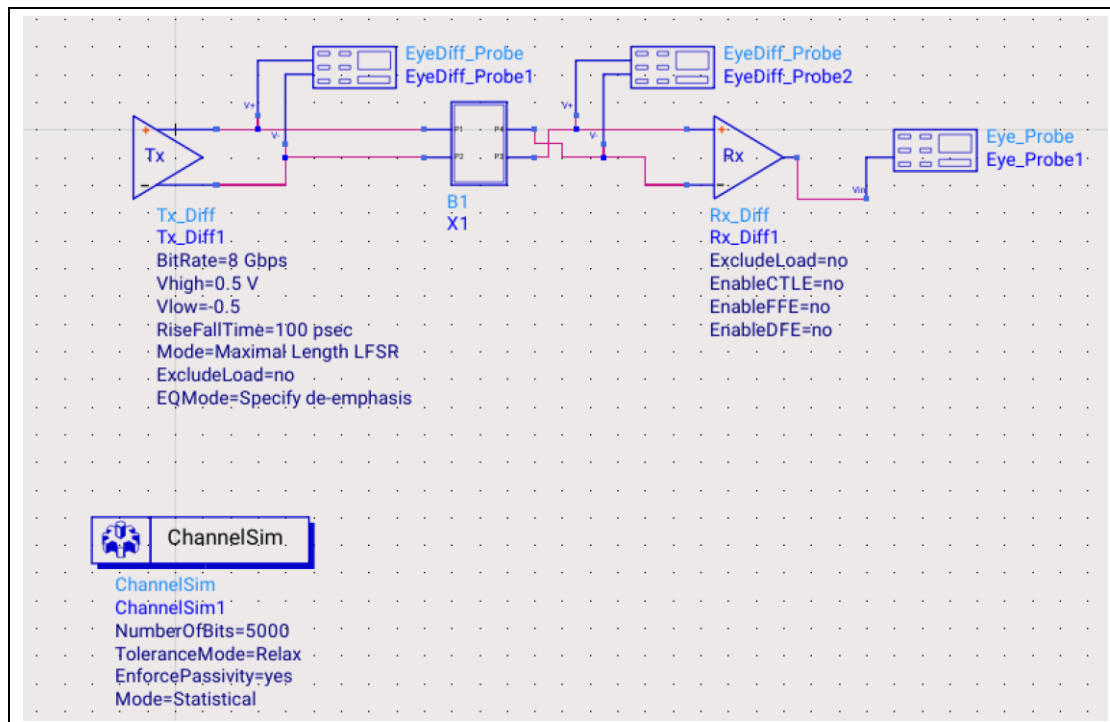


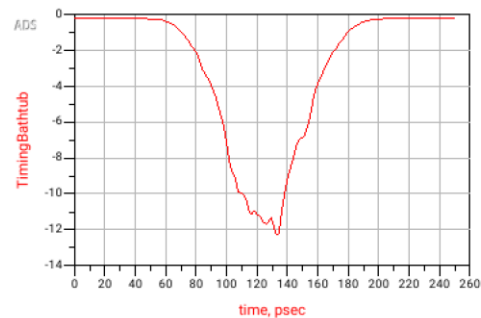
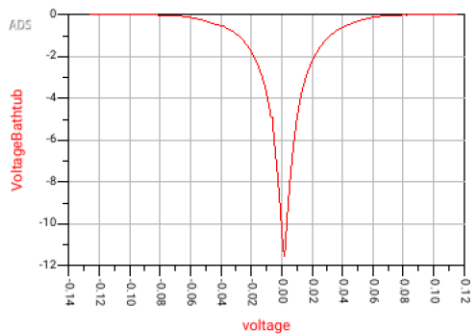
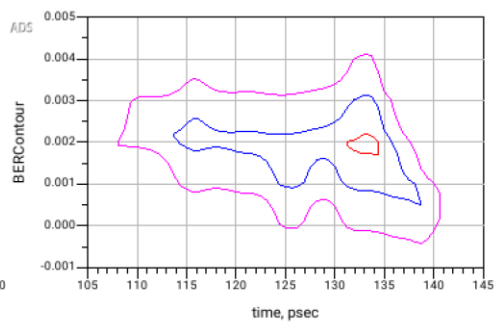
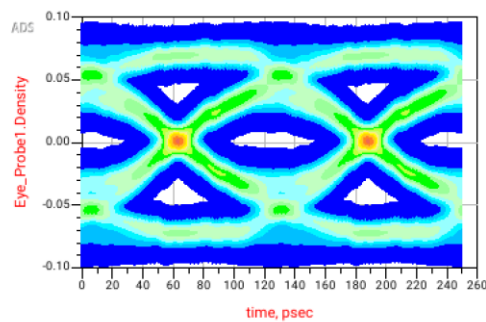
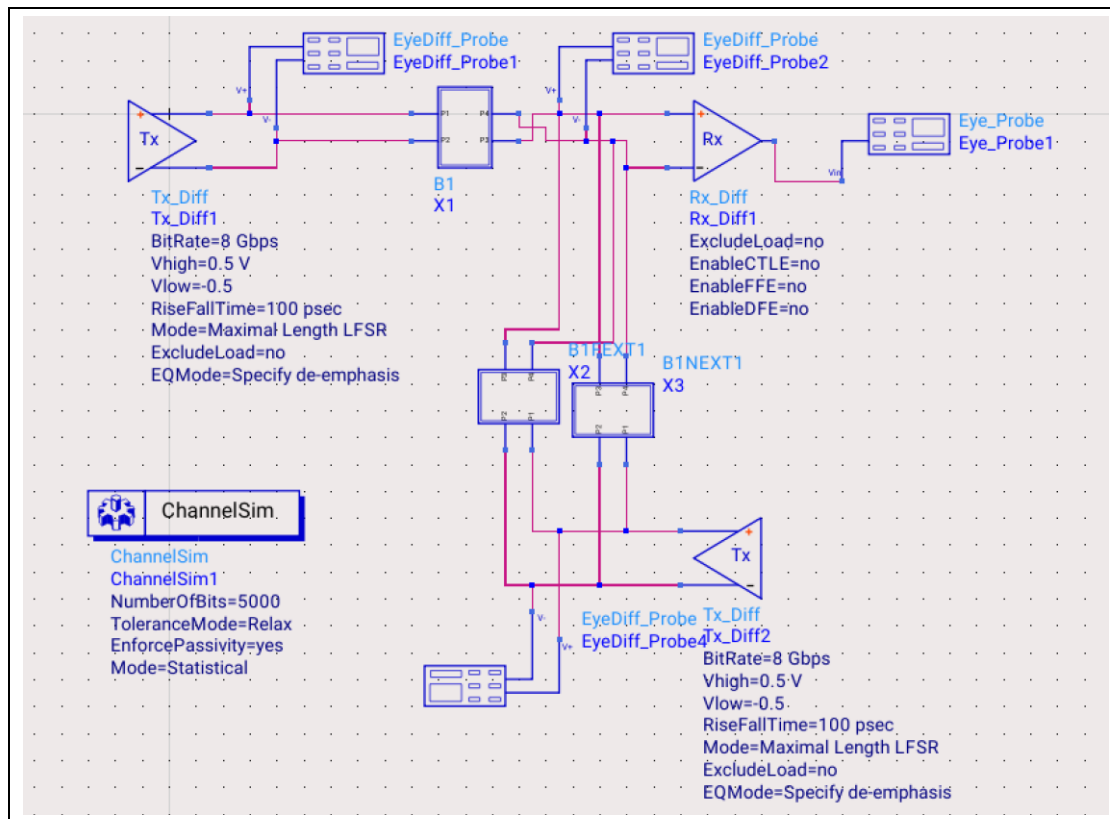


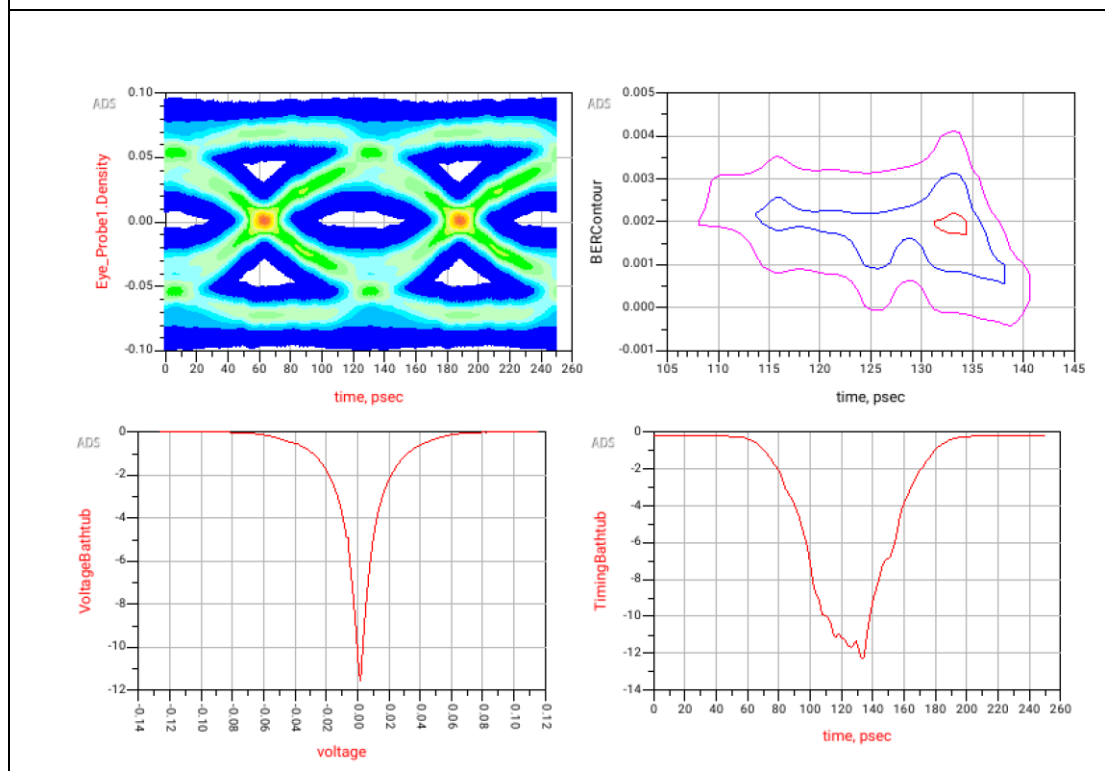
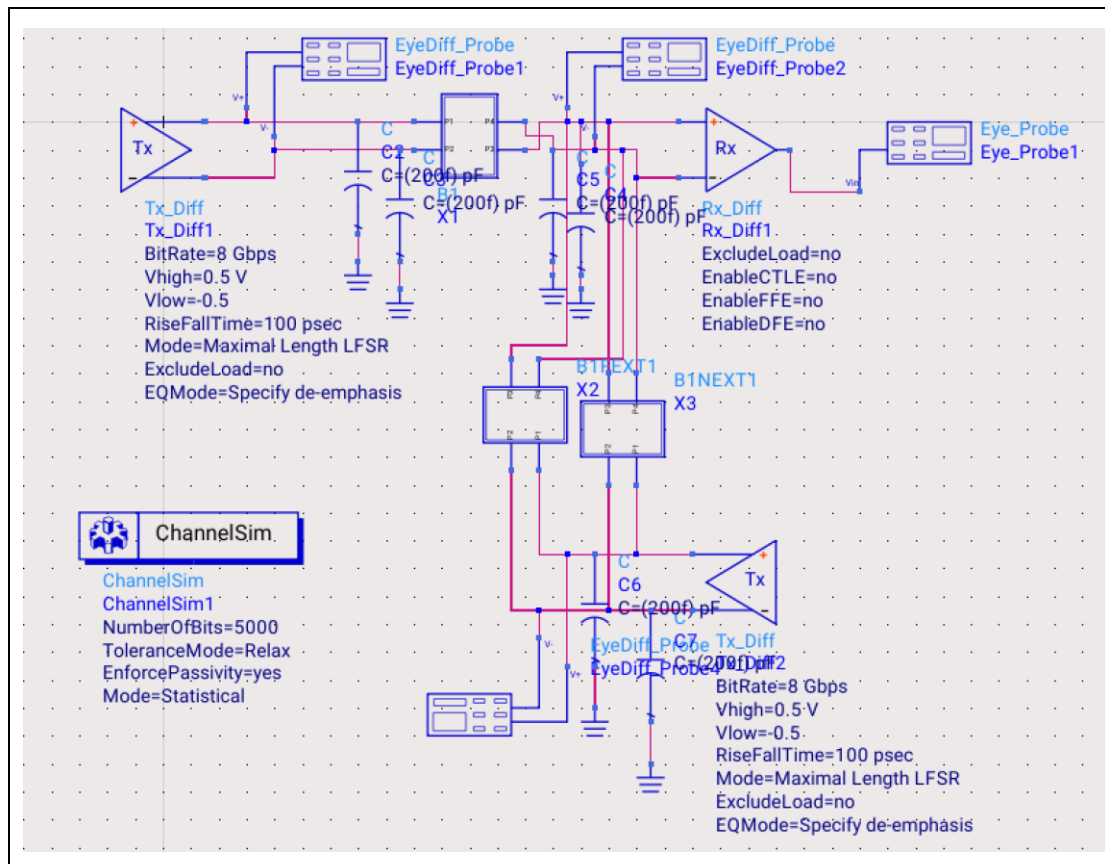




(c)







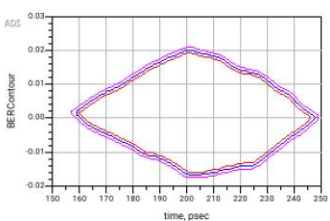
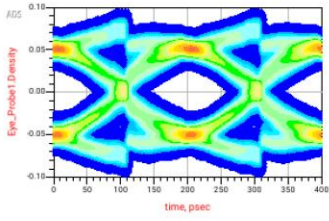
2. Use ADS to model a 5Gb/s link that operates on 20" BP channel (T20_thru) with various equalization schemes including crosstalk aggressors (NEXT1 & FEXT1). Include the same jitter properties and packaging parasitics as Problem 1 for all

test cases. You should provide your own CTLE poles and zero(s) in the RX block. Also, include TX FIR taps. For all test cases use 1Vpp swing at TX. Show eye diagrams, BER bathtub curves, BER contours in the following cases in Table 3. Plot the eye heights vs. Case # at BER of 10-12.

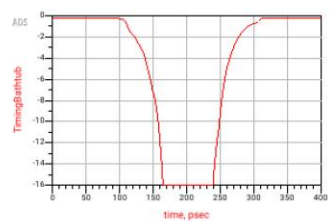
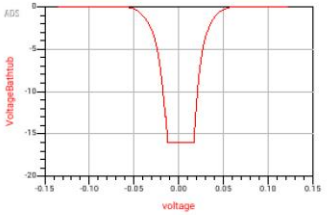
Table 3 Test Cases

	TX FIR	RX
case 1	1 Pre	2 Taps DFE
case 2	1 Post	1 Taps DFE
case 3	1 Pre	CTLE+1 Taps DFE
case 4	1 Post	CTLE+1 Taps DFE
case 5	1 Pre-1 Post	1 Taps DFE
case 6	1 Pre-1 Post	3 Taps DFE
case 7	1 Pre-1 Post	5 Taps DFE

CASE1

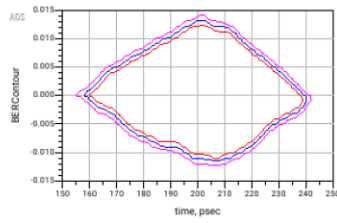
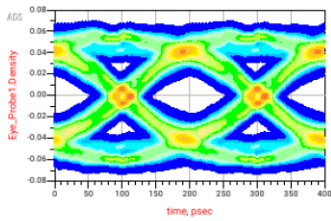


index	...ute(Eye_Probe1 Height)
0.000	0.055

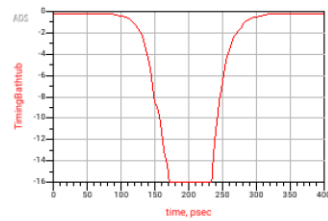
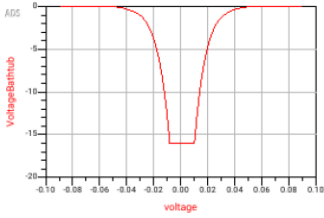


taps_quan =
-0.1429 0.8571 (3 bits resolution)

CASE2



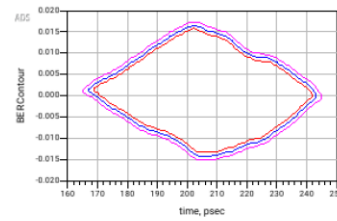
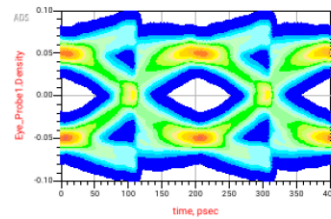
index	...ute(Eye_Probe1 Height)
0.000	0.035



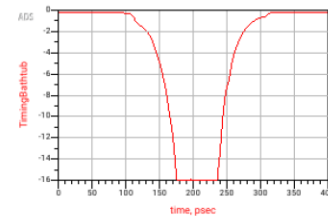
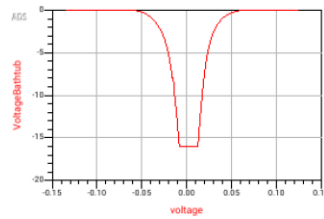
taps_quan =

0.7143 -0.2857 (3 bits resolution)

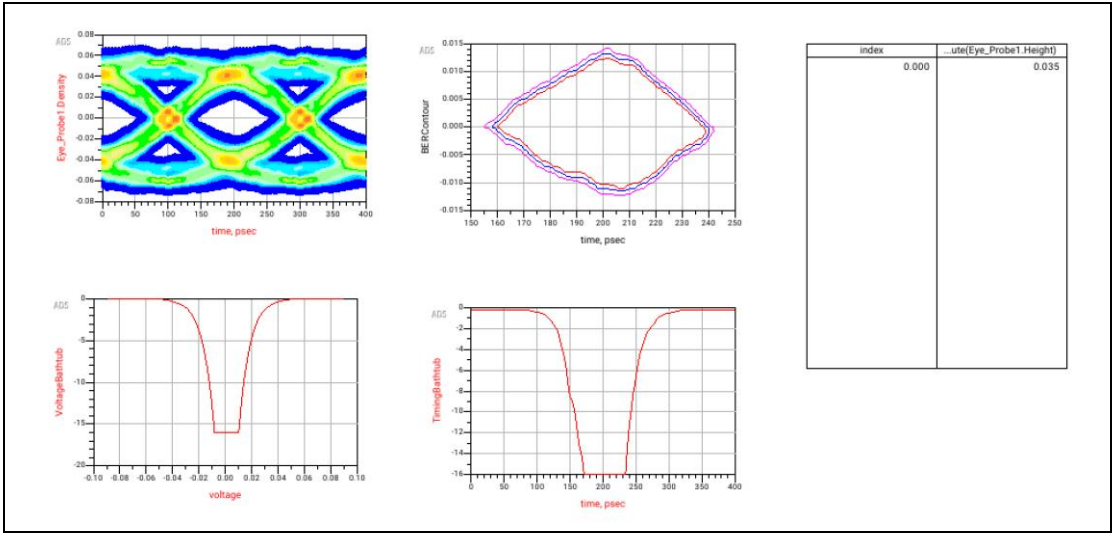
CASE3



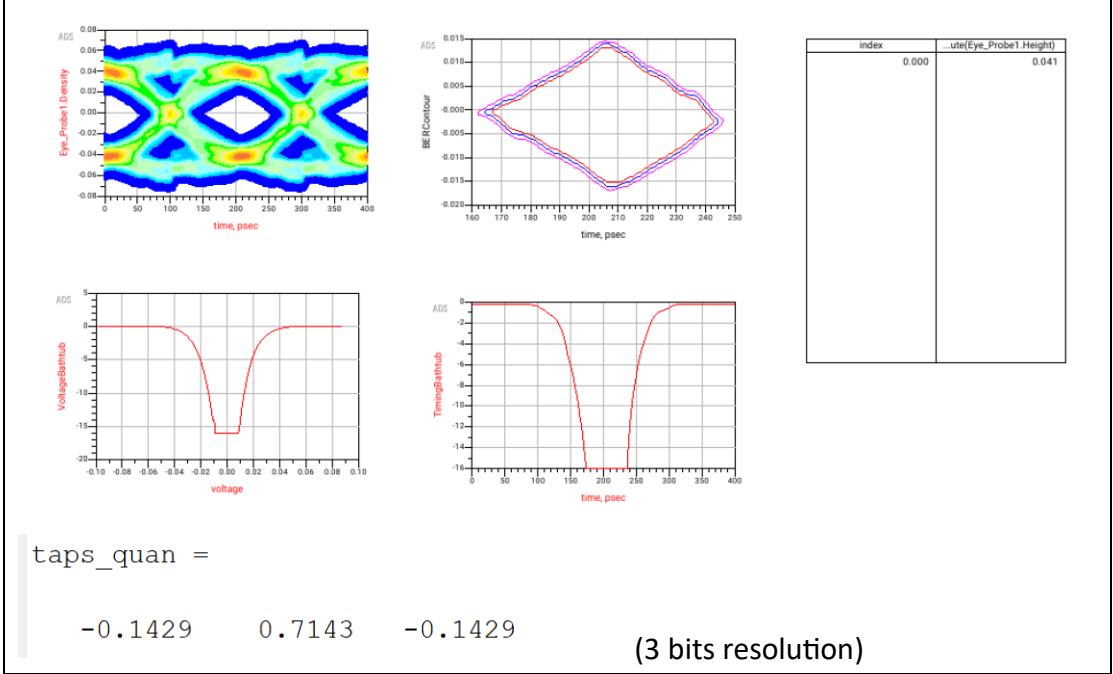
index	...ute(Eye_Probe1 Height)
0.000	0.047



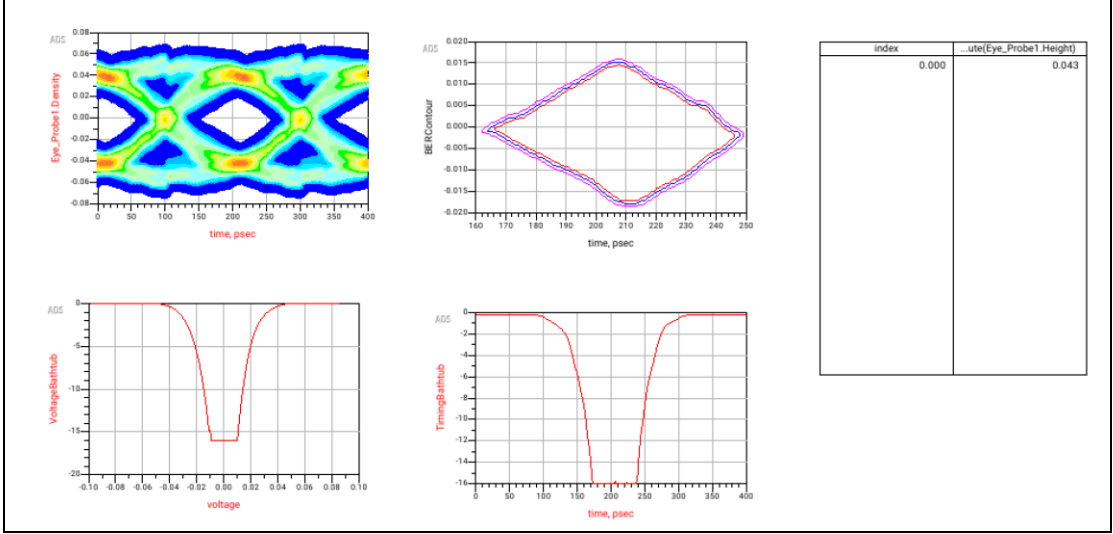
CASE4



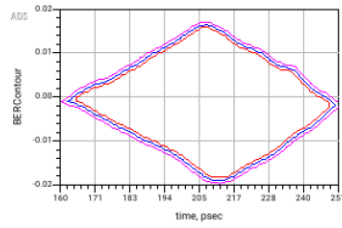
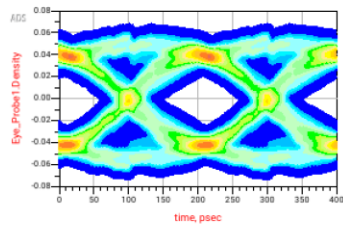
CASE5



CASE6



CASE7



index	...ute(Eye_Probe1 Height)
0.000	0.044

