25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

Lab4: Receiver Circuits

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Questions

1. High-Speed Comparator Design. This problem involves the design of four different high-speed comparators to meet the following specifications:

a. clk → Dout delay ≤ 150ps with a 10mV static differential input voltage (Din+−Din-) at a common mode voltage of 80% VDD. Measure delay from when the clock is at 50% VDD to Dout+ is at 50% VDD for an output rising transition. Please refer to Figure 18 in the Appendix.

b. Clock frequency = 3GHz. Use at least one inverter-based buffer to clock your circuit for realistic clock waveforms.

c. Load capacitance on Dout+ and Dout- is 10fF.

d. Input referred offset σ ≤ 10mV. Here you can optimistically assume that the input referred offset is just due to the input differential pair Vt (threshold voltage) mismatch and use the mismatch equation given in the notes, i.e., no need to run Monte Carlo simulations (although if you have access to a PDK that includes accurate statistical models of the CMOS devices you are encouraged to use Monte Carlo analysis).

e. Optimize the design for power consumption, i.e., don’t overdesign the comparator for a super small delay. Try to minimize total capacitance while still meeting the ≤ 150ps delay and σoffset ≤ 10mV offset specifications.

**The comparators should realize a flip-flop function.**

a. As shown in Figure 10, for the Strong-Arm type latches (1, 3, and 4) follow it with the optimized SR-latch shown in Figure 11. For more details on the optimized SR latch, refer to [8]. Note: for architecture (3) you will need to modify this optimized SR-latch – as the sense-amp pre-charges to GND (vs. VDD in 1 & 4).

b. To realize a CML flip-flop with architecture (2), simply cascade two CML latches to realize a master-slave flip-flop

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| **a. Conventional Strong-Arm Latch. For an example schematic, refer to Figure 3(a). Feel free to change the pre-charge transistors configuration.** |
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| Delay: 141ps |

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| b. CML Latch. For an example schematic, refer to Figure 3(b). |
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| Delay: 254ps |

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| c. Schinkel Low-Voltage Latch. For an example schematic, refer to Figure 2 in [6]. |
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| Delay time: 161.3 ps |

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| d. Goll Low-Voltage Latch. For an example schematic, refer to Figure 2 in [7]. |
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| Delay time: 141.543ps |

2. High-Speed Comparator Characterization. Please simulate all four comparators and produce the following using 500MHz (or less if necessary) clock signal:

a. Plot comparator delay vs. VDD for VDD varying from 50% of nominal VDD to 100% VDD. For this keep the input common mode equal to 80% of the supply, i.e., sweep the input common-mode along with the supply. Also scale the clock input signal level with VDD.

b. Plot comparator power vs. VDD in a similar manner.

c. Generate the comparator Impulse Sensitivity Function (ISF) at the nominal VDD, 80%VDD, and 60%VDD (3 curves). Again, track the input common-mode with VDD (for more details refer to [2]). For the ISF-based characterization use an input differential step of 50mV, i.e., VCM±25mV for the differential input signals. Report the comparator aperture time, by measuring the 10%-90% “rise-time” based on the simulation results. Please refer to [9] for the aperture time measurement.

d. Compare the design of these four latches (you can refer to [2]).

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| (a) Strong-Arm | Classic design, no static power, simple structure | High speed, but better at higher supply voltages | Extremely low (no DC consumption) | Flash ADC, general high-speed comparators |
| (b) CML Latch | Current-mode switching, small output swing | Ultra-high speed (10–40+ Gb/s) | Has static current, relatively high power | High-speed SerDes, backplane links, ultra-high-speed I/O |
| (c) Schinkel Low-Voltage | Modified Strong-Arm, fewer stacked transistors, suited for low voltage | Relatively fast, outperforms standard SA at the same supply voltage | No static current, moderate power | Low-voltage high-speed applications (UDSM CMOS) |
| (d) Goll Low-Voltage | Extends SA design by adding P4/P5 for feedback acceleration | High (0.6–5 GHz) | No static current | High-speed, low-voltage comparators in UDSM CMOS |

3. Link Verification. The designed comparator can be considered as a basic receiver. Build a 6Gb/s link system by using the transmitter designed either in voltage mode or current mode and the comparator which you’ve chosen for the best performance. Please refer to Figure 12 for the full test circuit. Use 50Ω transmission line with 1ns delay. Add 200fF parasitic caps at the output of your transmitter and input of the receiver. Feel free to choose the best termination and coupling schemes.

a. Show the circuit schematic including coupling and termination.

b. Explain your choice of coupling and termination schemes.

c. Please show simulation results and eye diagrams that verify the link functionality and performance.

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