TAMU 2025 Spring ECEN 720 : High-Speed Link Circuits and Systems

Voltage-Mode Transmitter with High-Resolution Equalization

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Introduction

In high-speed serial communication systems, signal integrity becomes a major concern due to inter-symbol interference (ISI) caused by channel losses. Without equalization, the transmitted signal can experience severe distortion, leading to significant eye closure at the receiver.. Such conditions make reliable data recovery virtually impossible. Therefore, transmitter-side equalization techniques, such as multi-tap FFE and other pre-emphasis methods, are essential to compensate for channel impairments, restore sufficient eye opening, and enable robust high-speed data transmission.

- **T20 channel**

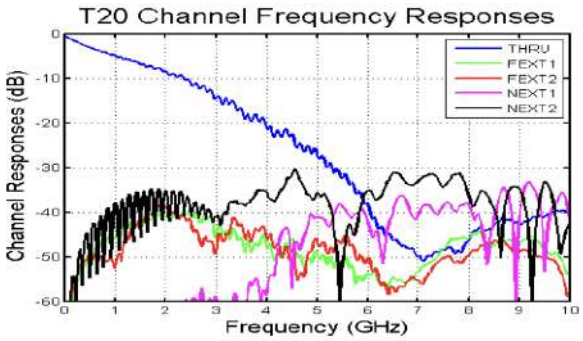


Fig 1. T20 channel response

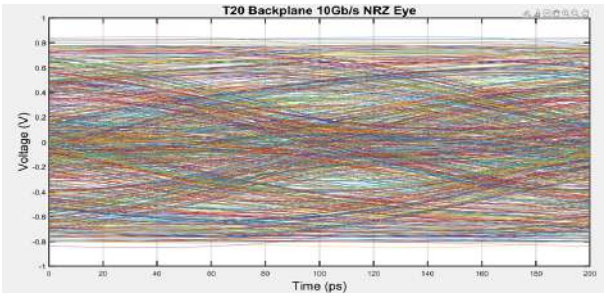


Fig 2. T20 Channel eye diagram without equalizer

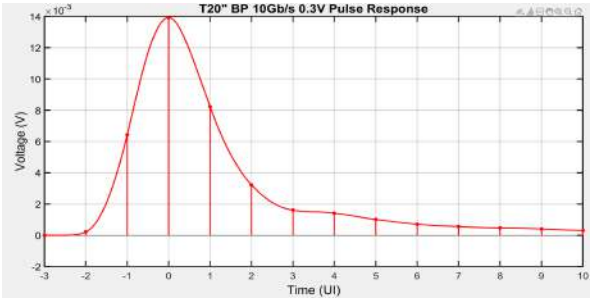


Fig 3. T20 pulse response for 10G Hz

- **B1 Channel**

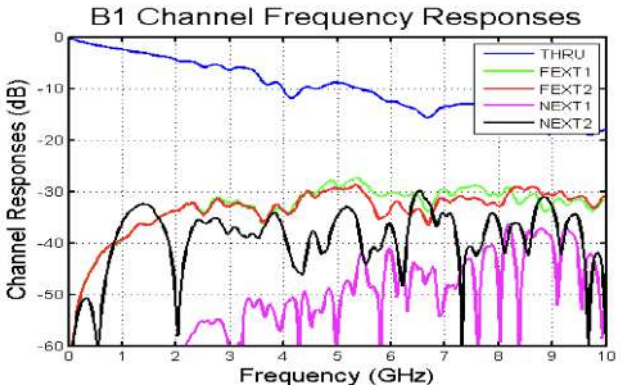


Fig 4. B1 channel response

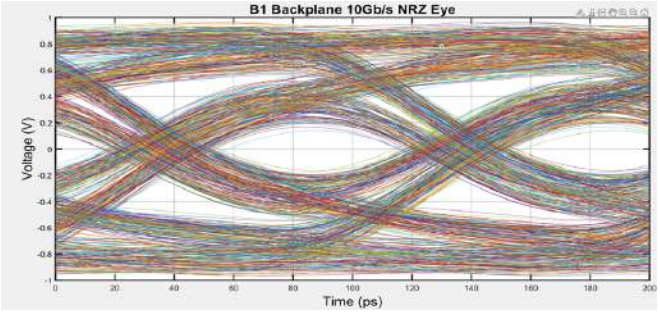


Fig 5. B1 Channel eye diagram without equalizer

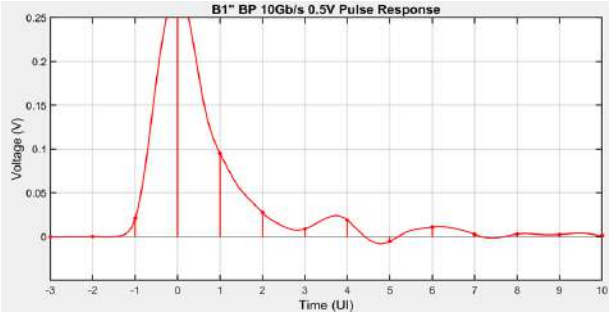


Fig 6. B1 pulse response for 10G Hz

- **C4 Channel**

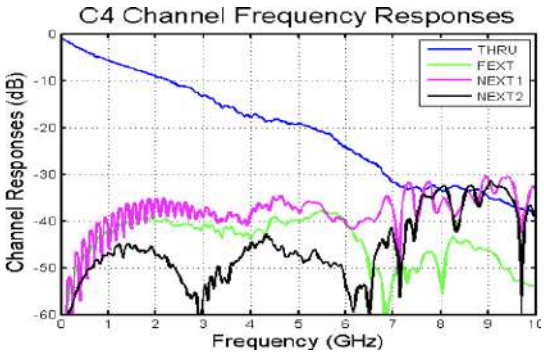


Fig 7. C4 channel response

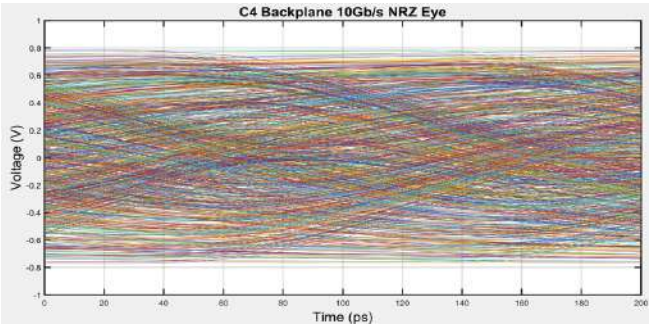


Fig 8. B1 Channel eye diagram without equalizer

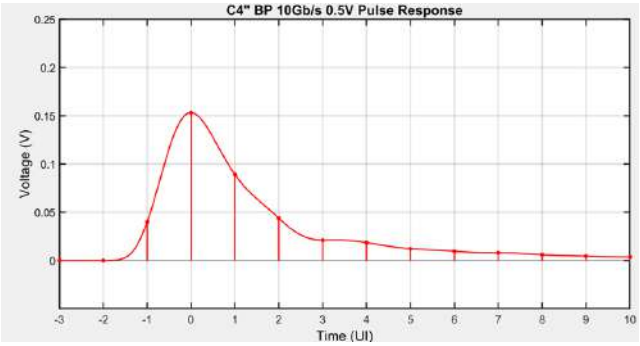


Fig 9. C4 pulse response for 10G Hz

DESIGN PROCEDURE

In this project, we use a voltage-mode driver combined with a transmitter-side equalizer to improve signal integrity. Under identical output swing conditions, the voltage-mode driver typically consumes less power than a current-mode logic (CML) driver because it avoids static current paths. However, it is more sensitive to impedance mismatches and swing inaccuracies, which can affect high-speed performance.

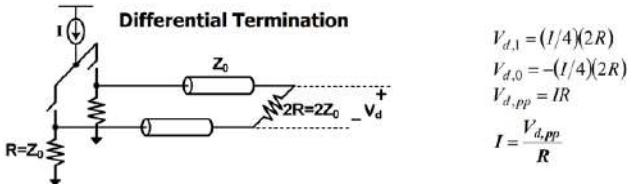


Fig 10-1. Current mode TX driver

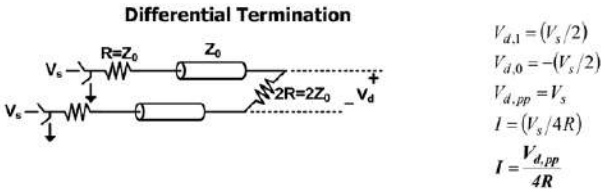


Fig 10-2. Voltage mode TX driver

➢ **TX voltage mode driver with regulator**

To achieve impedance matching with the 50-Ω channel, it is necessary to ensure the transistor resistance (RFET) matches this channel impedance. The transistor resistance is defined as:

RFET= $\frac{1}{uncox*\left(\frac{W}{L}\right)*(VGS-VT)}$. Since the gate-source voltage (VGS) of the transistor is directly set by the input voltage (Vin) of the voltage-mode driver, accurate impedance matching requires precise control of Vin. Consequently, a regulated reference voltage (Vr) is introduced to set Vin precisely at the level required to maintain RFET at 50 Ω, ensuring optimal channel matching.

Vs determines the output voltage swing at the transistor pads (PadN and PadP). For single-ended termination, the positive pad (PadP) voltage becomes Vs divided evenly by the transistor resistance (50 Ω RFET) and the channel receiver resistance (50 Ω), resulting in +Vs/2. Conversely, the negative swing path results in -Vs/2 at PadP, as illustrated in Figure 11.

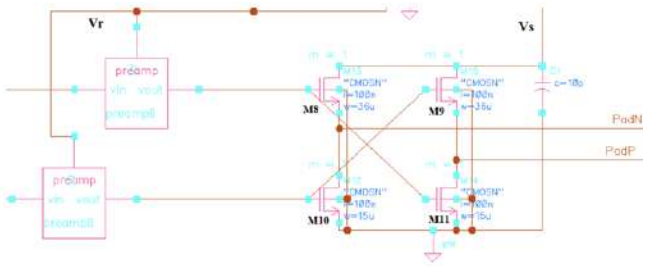


Fig 11. Schematic of one typical voltage mode driver

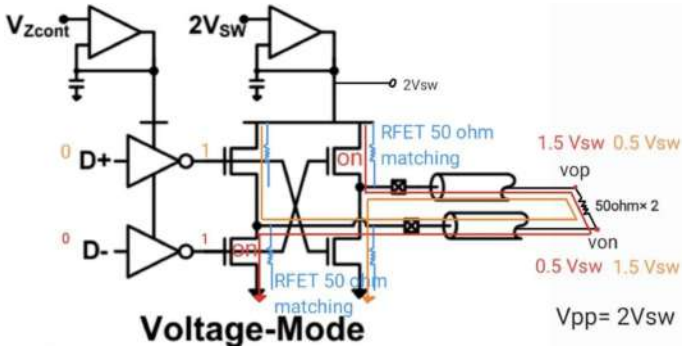


Fig 12. Driver includes two voltage regulating circuits

After the preamplifier stage, Vin is regulated to a fixed voltage Vr, ensuring a constant VGS and thus maintaining RFET at 50 Ω. The transistor pads (PadN and PadP) connect directly to the channel, enabling optimal impedance matching.

The circuit of current regulator & regulator & regulator are shown in figure2

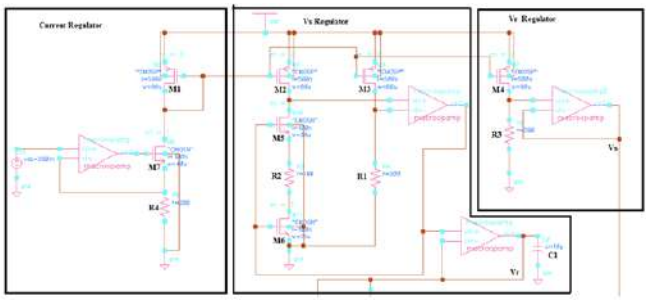


Fig 13. Schematic of the regulating circuits

➢ Regulator

Current Regulator

The current regulator sets the reference current I(Vin) to ensure that the sense voltage Vx accurately tracks the input voltage Vin, establishing a stable current-voltage relationship.

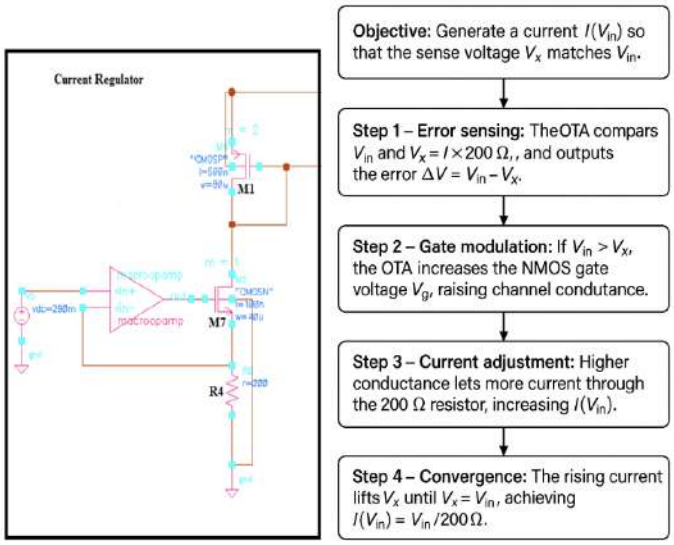


Fig 14. Schematic & flowchart of the current regulator

Vr Regulator

The Vr regulator tunes the gate bias of the output transistors, dynamically adjusting their conductance to maintain a precise 50 Ω output impedance for consistent signal integrity

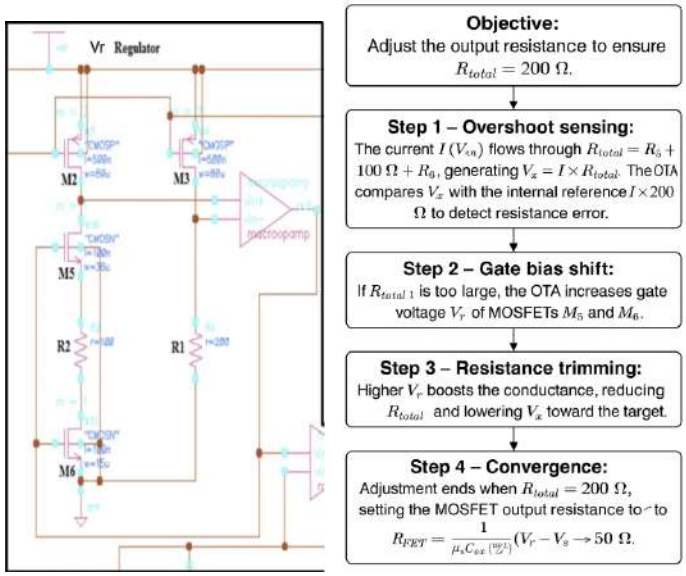


Fig 15. Schematic and flowchart of the Vr regulator

Vs Regulator

The Vs regulator adjusts the output single-ended swing so that Vs matches the desired voltage level, ensuring correct differential output across the termination resistors.

In this work we choose to use a 300mV Vpp for a low swing voltage driver.

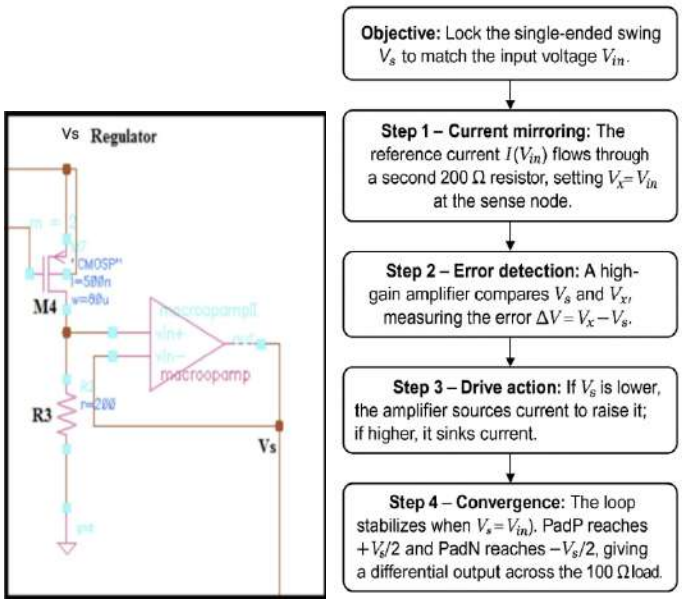


Fig 16. Schematic and flowchart of the Vs regulator

➢ **Equalizer**

Equalization goal is to flatten the frequency response out to the nyquist frequency and remove time-domain ISI (Fig 18.) Figure 17 is a typical FFE tx equalizer diagram[2][3].

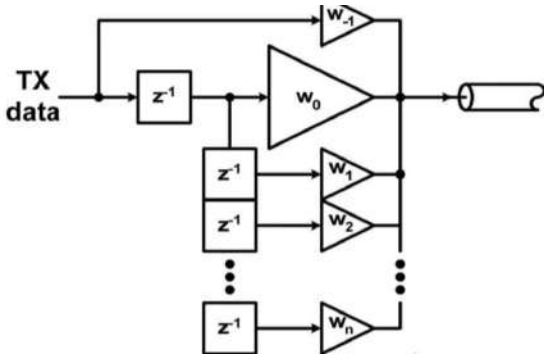


Fig 17. 11 FFE equalizer

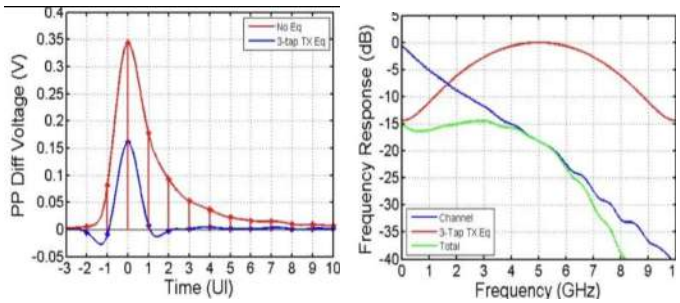


Fig 18. time-domain and frequency response before and after

In this project, a 3-tap FIR equalizer with 6-bit resolution is proposed, as illustrated in Figure 9. To implement the required weighted voltage levels, a regulator is used together with a set of TX voltage drivers configured with different impedance values to realize the tap coefficients. Figure 13 shows the system block of it.

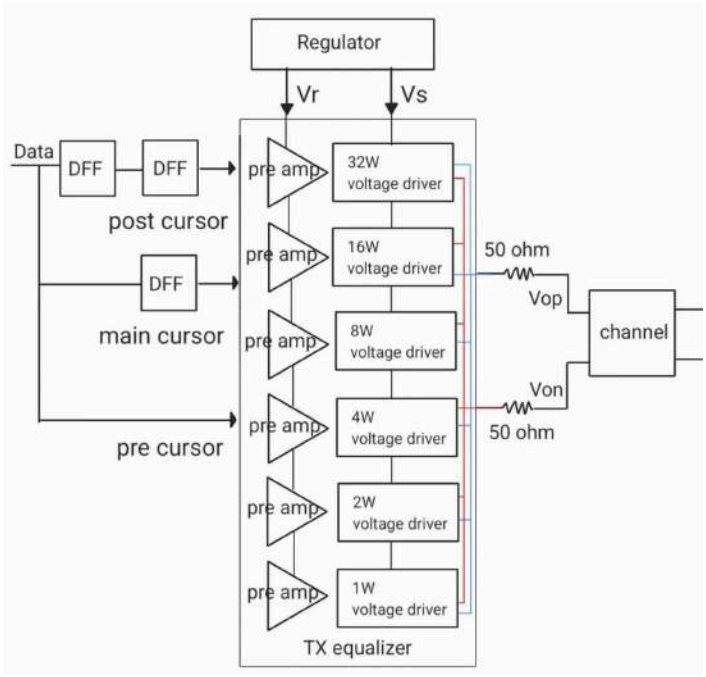


Fig 19. System block of 3 tap voltage mode equalization

In this design, equalizer tap coefficients are implemented using a set of binary-weighted TX driver segments (e.g.,32W, 16W, 8W, 4W, 2W, 1W), where the output impedance of each segment is inversely proportional to its size. These drivers are split into six segments, and by activating specific combinations, the desired tap magnitude is achieved. As all segments are always connected to either Vs or GND, the total output impedance remains constant at 50 Ω. During operation, the segments collectively form a voltage divider with 8 possible output levels, setting the effective de-emphasis coefficient α while maintaining stable output impedance.

Each weight driver connects to only one cursor (main, post, or pre), and the sign of the tap coefficient determines whether the positive or negative cursor connects to the driver's positive input. For example, a precursor coefficient of –0.1429 connects the negative precursor to the weight-8 and weight-1 drivers, giving a total weight of (8+1)/63. Although the activated combination changes the output voltage, the total output impedance remains constant at 50 Ω.

Channel (10GHz data)	Pre	Main	Post
T20	-0.1905	0.5714	-0.2381
	-(8+2+1)/63	32+4/63	-16/63
C4	-0.1429	0.5714	-0.2857
	-(8+1)/63	(32+4)/63	-(16+2)/63
B1	-0.0476	0.7143	-0.2857
	-2/63	32+8+4+1/63	-16/63

Table 1. Equalization coefficient of T20, C4 and B1 channel

Pre	Main	Post	Vo (VoP- VoN)
0	0	0	-0.143Vpp
0	0	1	-0.714Vpp
0	1	0	Vpp
0	1	1	0.429Vpp
1	0	0	-0.429Vpp
1	0	1	-Vpp
1	1	0	0.714Vpp
1	1	1	0.143Vpp

Table 2. Different combination voltage of equalizer C4 Channel

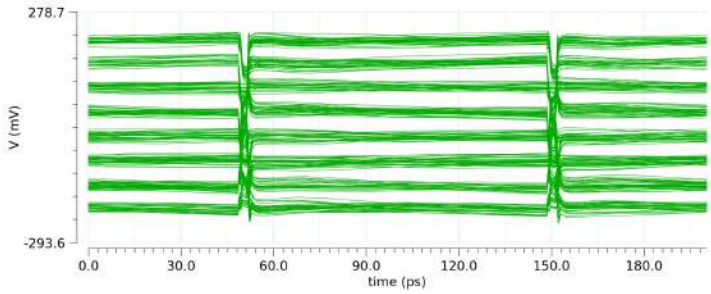


Fig 20. 8 voltage levels after equalizer before C4 channel

➢ **DC couple channel**

The two single-ended output signals of the channel without DC coupled are shown in Fig 22. A. Since no DC information is included in the s-parameter file for the channel, the DC level of both output signals are not equal to the expected value (Vpp/2).

Schematic in Fig 21. resolve this issue by extrapolating the missing DC information from the rest of the data in s-parameter file, the result is shown in Fig 22. B.

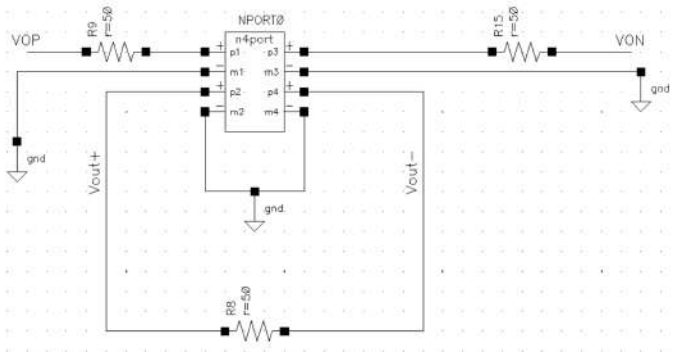


Fig 21. Channel with DC couple

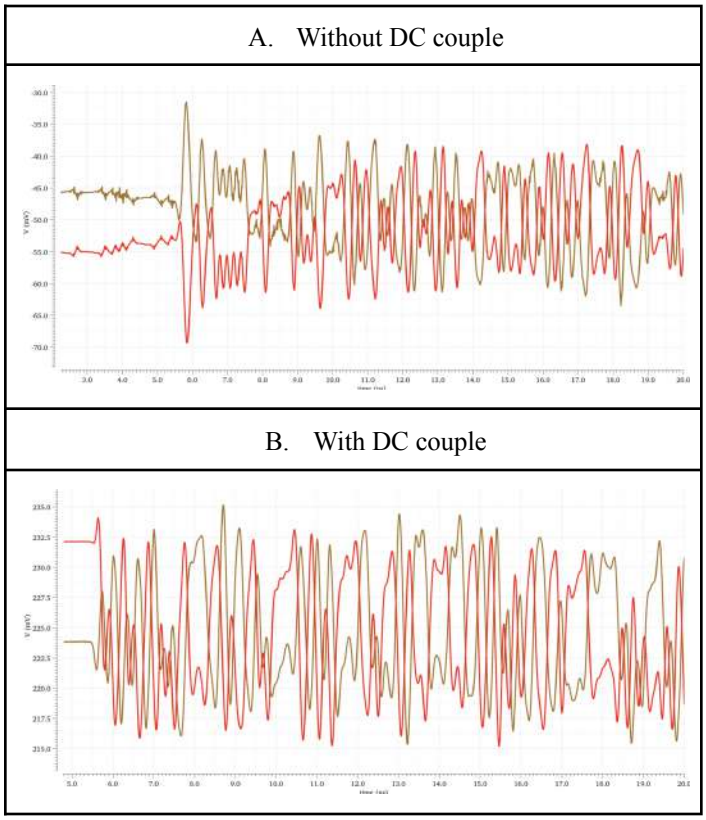


Fig 22. Channel output with and without DC couple

Schematic

The following schematic corresponds to the T20 channel coefficient. For other channel coefficients, the same procedure applies by adjusting the input node connected to the appropriate cursor.

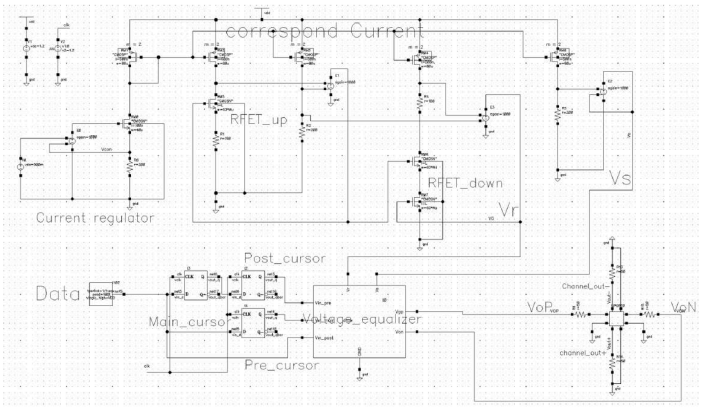


Fig 24. Full schematic with Regulator, 3-tap Equalizer & Channel

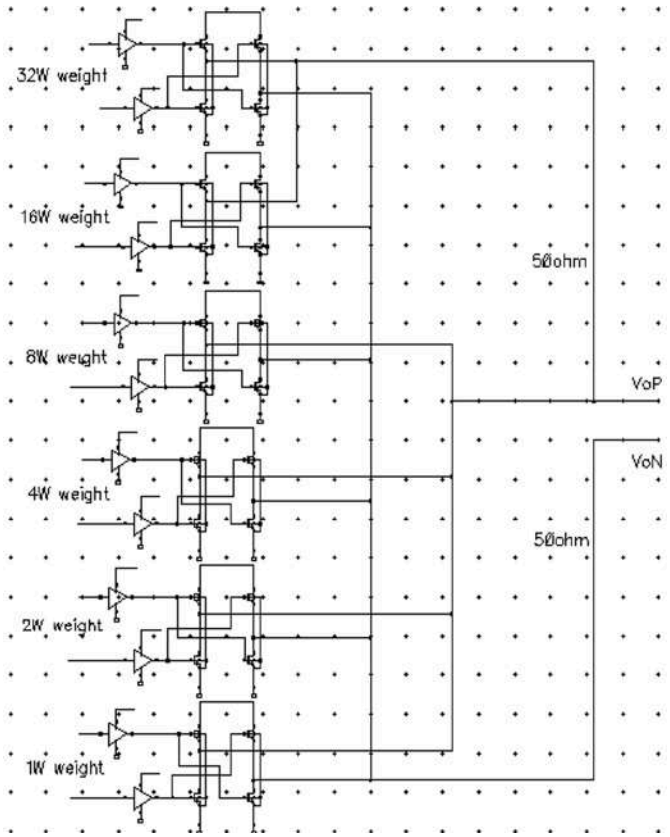


Fig 23. 3 Tap equalizer

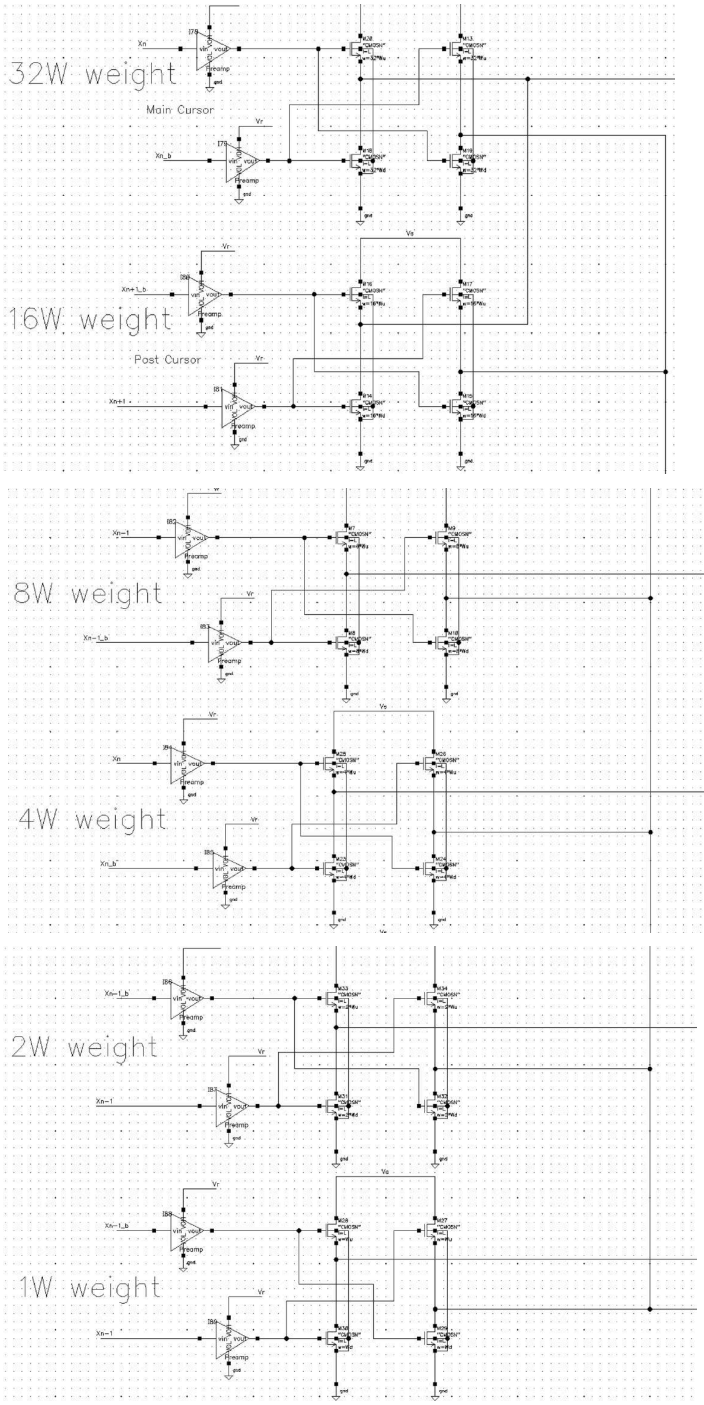
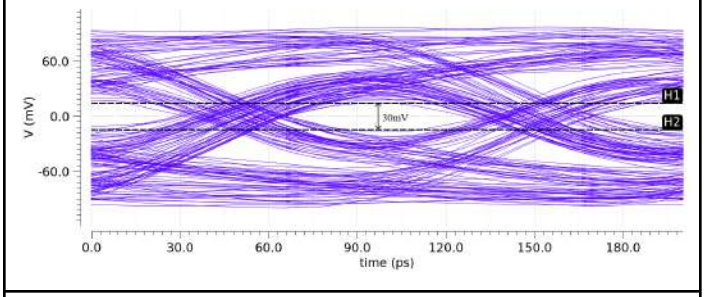


Fig 23-1. Weighted equalizer

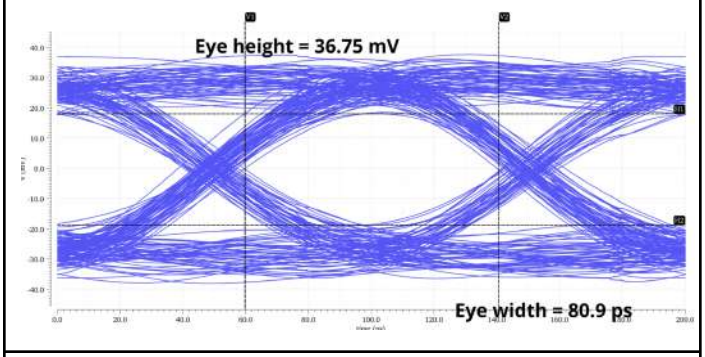
Simulation Results

We are looking for a 20mVppd and 0.3UI timing margin at a BER=10^{-12} on the RX side

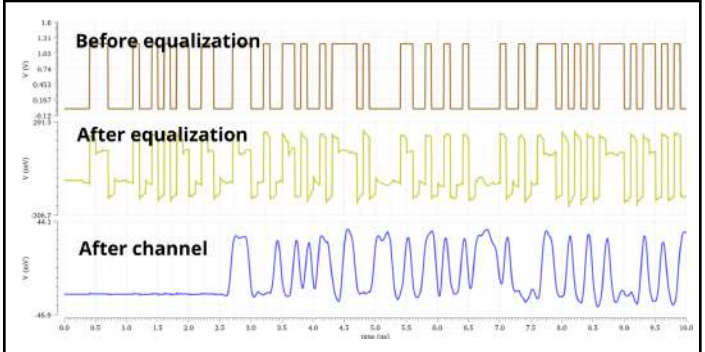
B1 without equalization



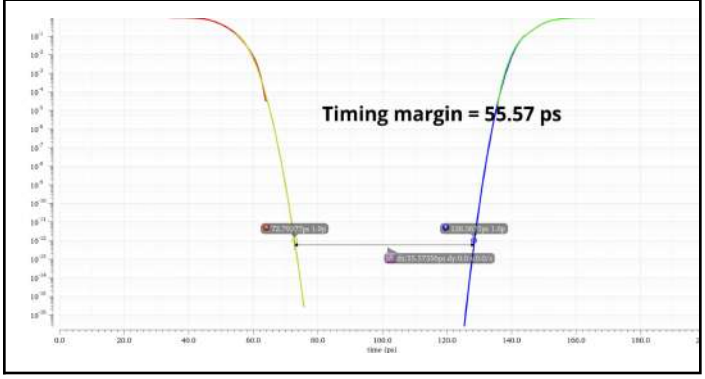
B1 with equalization



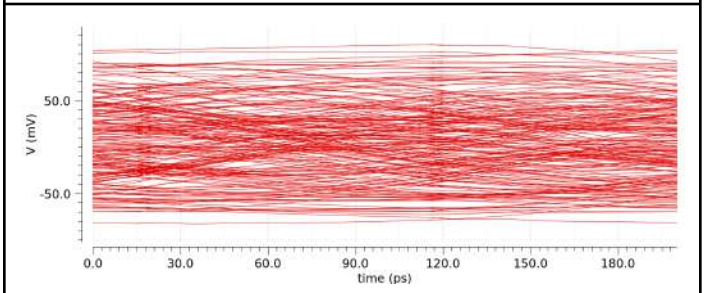
B1 Transient response with equalization



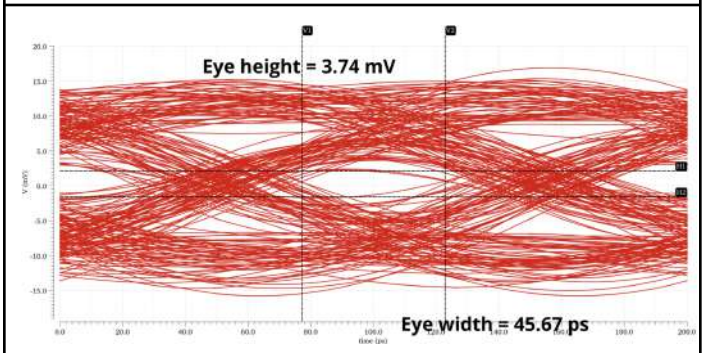
Bathtub for B1 channel at BER=10^{-12}



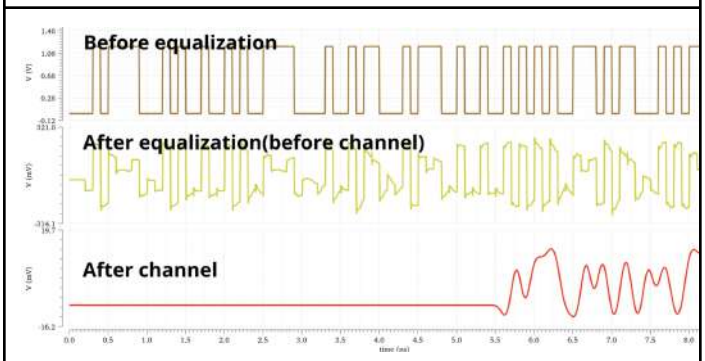
T20 without equalization



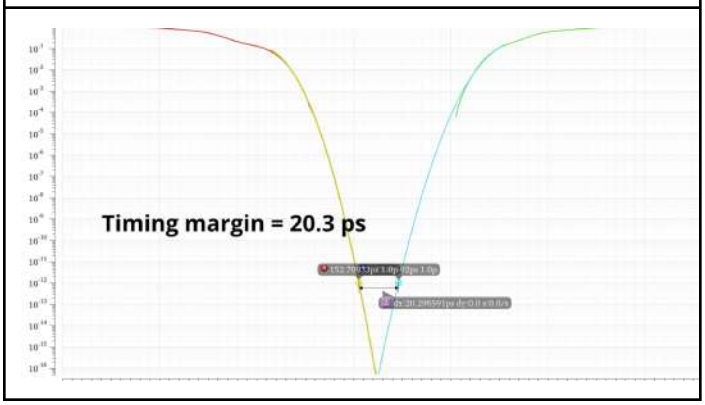
T20 with equalization



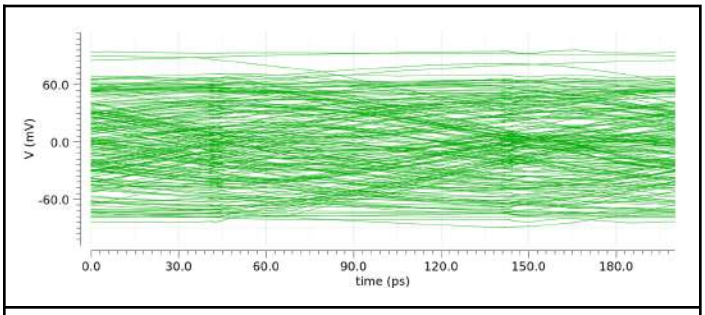
T20 Transient response with equalization



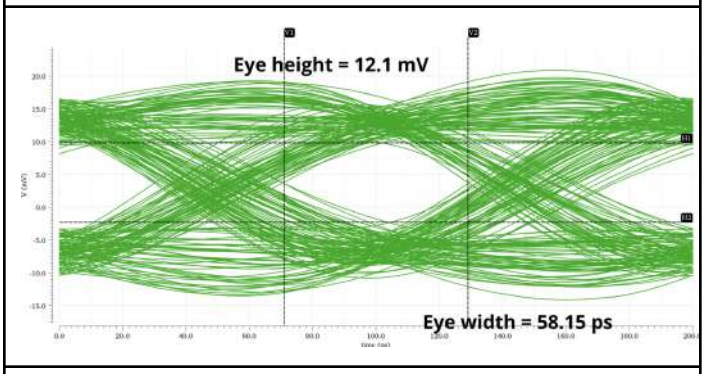
Bathtub for T20 channel at BER=10^{-12}



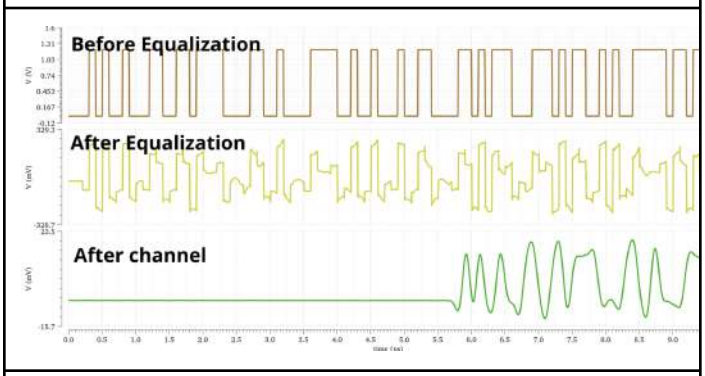
C4 without equalization



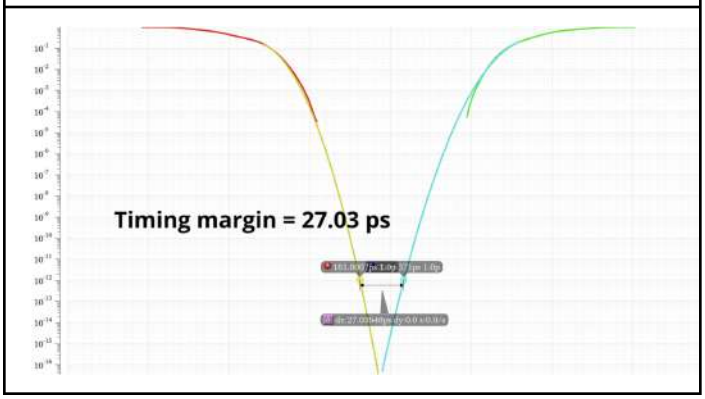
C4 with equalization



C4 Transient response with equalization



Bathtub for C4 channel at BER=10^{-12}



Comparison Table

Reference	Song 2014 [1]	Wong 2004 [2]	Hatamkhani [3]	This work
Technology	65nm	180nm	180nm	90nm
Driver	Voltage mode	Voltage mode	Voltage mode	voltage mode
Data rate	16 Gbps	3.6 Gbps	3.6 Gbps	10 Gbps
TX Tap	2-tap FIR	2-tap Pre Emphasis	2-tap Pre Emphasis	3-tap
Eye height	55mV	127mV	125mV	36.75mV
TX Power	16.8mW	9.66mW	9.66mW	5.56mW

Table 3. Comparison table

Active CTLE

A CTLE is commonly used at the receiver side to mitigate both precursor and post cursor ISI through high-pass filtering (Figure25). However, as an analog amplifier, it also amplifies noise along with the signal.

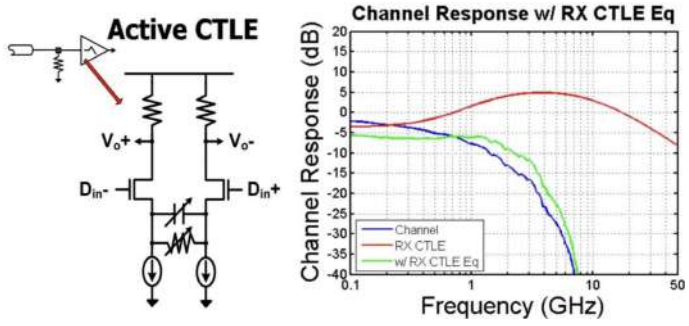
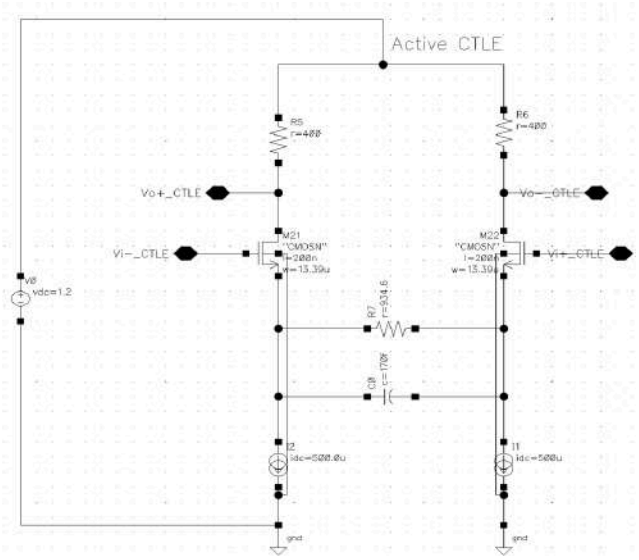


Fig 25. Active CTLE



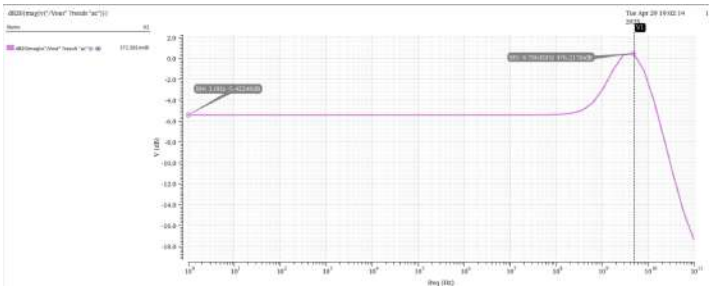


Fig 26. Frequency response for CTLE

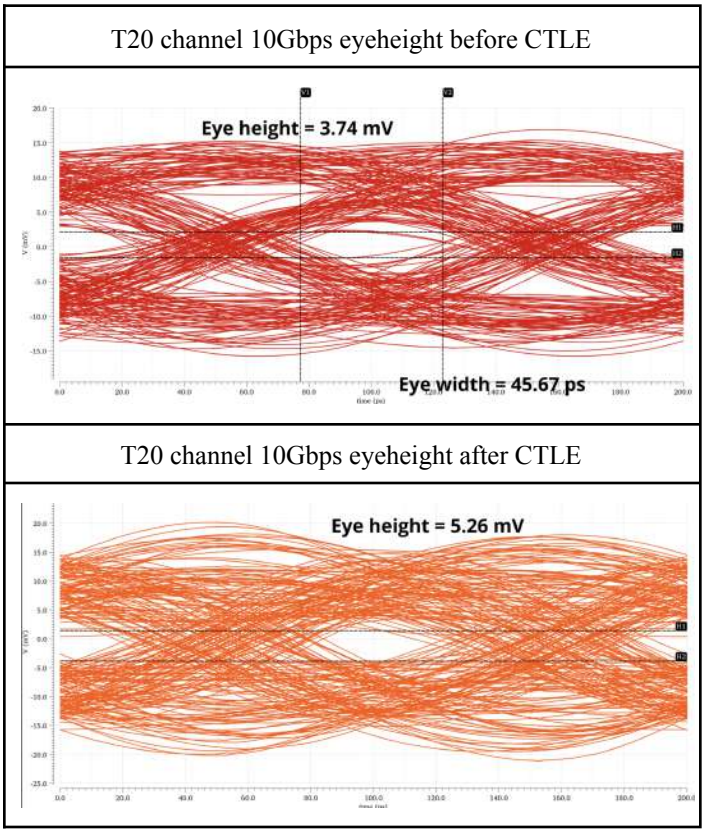


Fig 27. Eyeheight with and without CTLE

Reference

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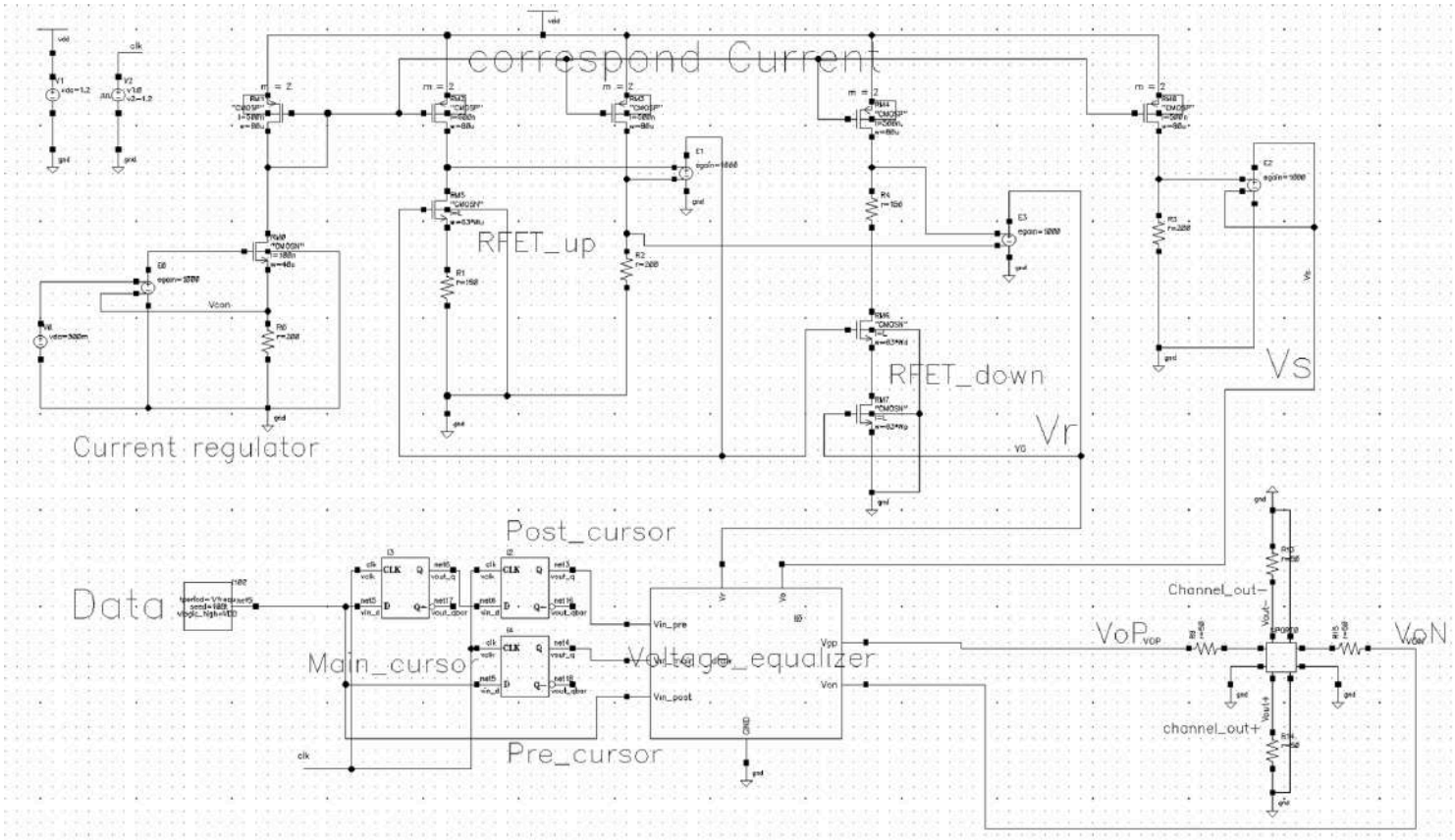
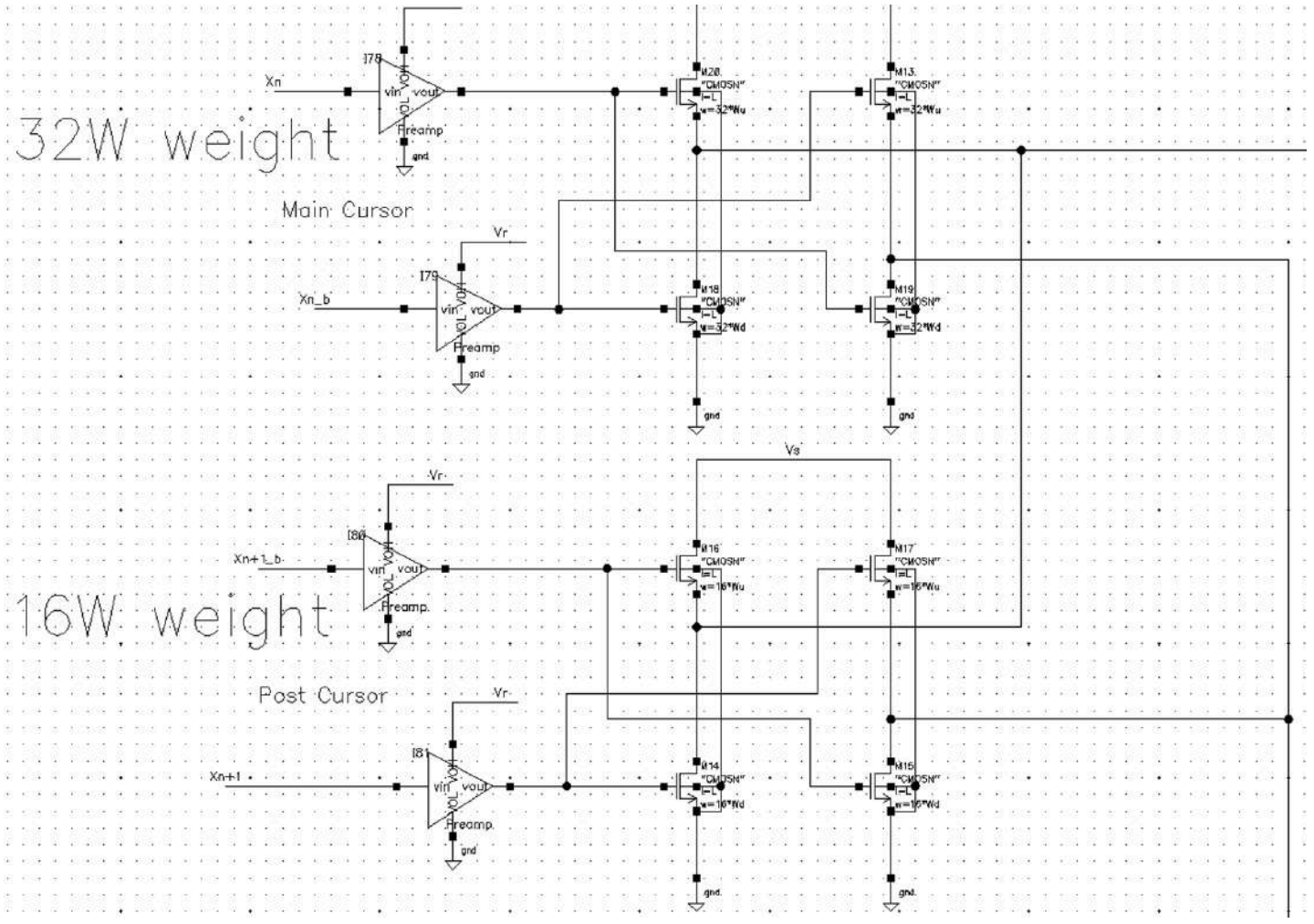
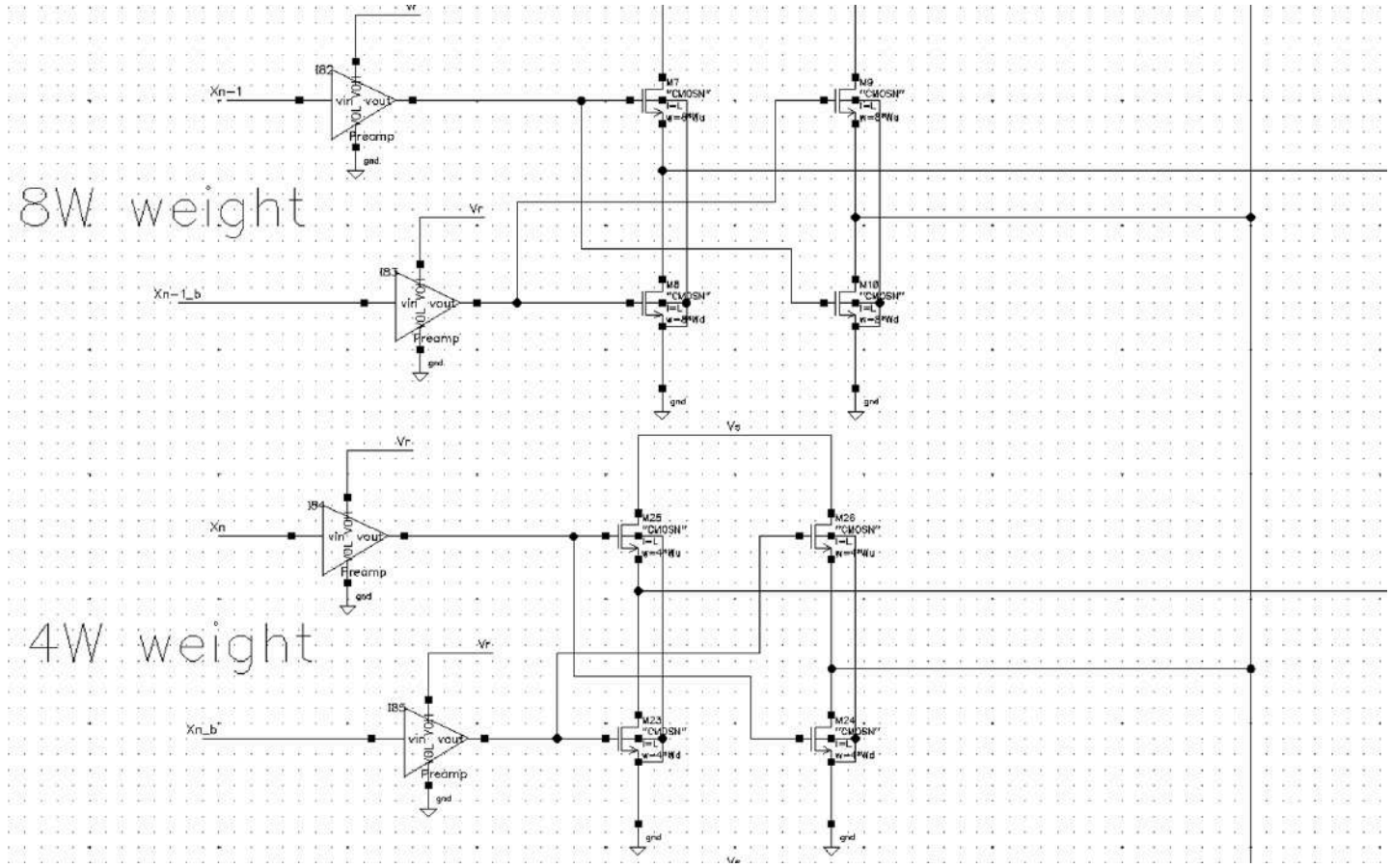
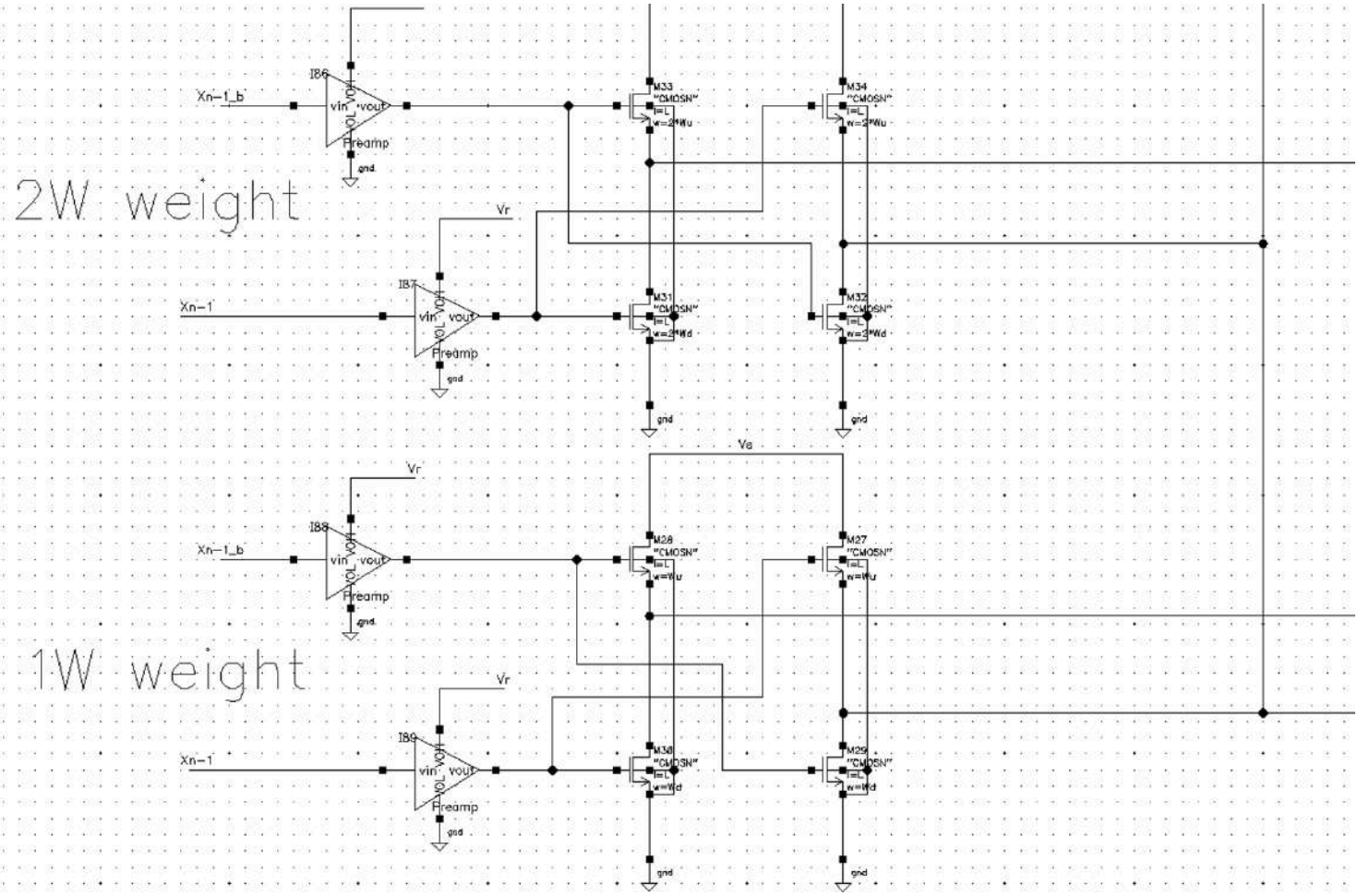

correspond Current
RFET_up
RFET_down
Current regulator
Vs
Vr
Post_cursor
Data
Main_cursor
Pre_cursor
Voltage_equalizer
Channel_out
VoP
VoN
channel_out+


32W weight
Main Cursor
16W weight
Post Cursor
Xn
Xn_b
Xn+1
Xn+1_b
Vr
Vs
Preamp
gnd


8W weight
4W weight
Xn-1
Xn-1_b
Xn
Xn_b
Vr
Ve
Vreamp
gnd
M7
M8
M9
M10
M25
M26
M23
M24


2W weight
1W weight
Xn-1_b
Xn-1
Vr
Ve
Vreamp
gnd
M33
M34
M31
M32
M28
M27
M30
M29