25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab6: Link Modeling with ADS

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Section:700

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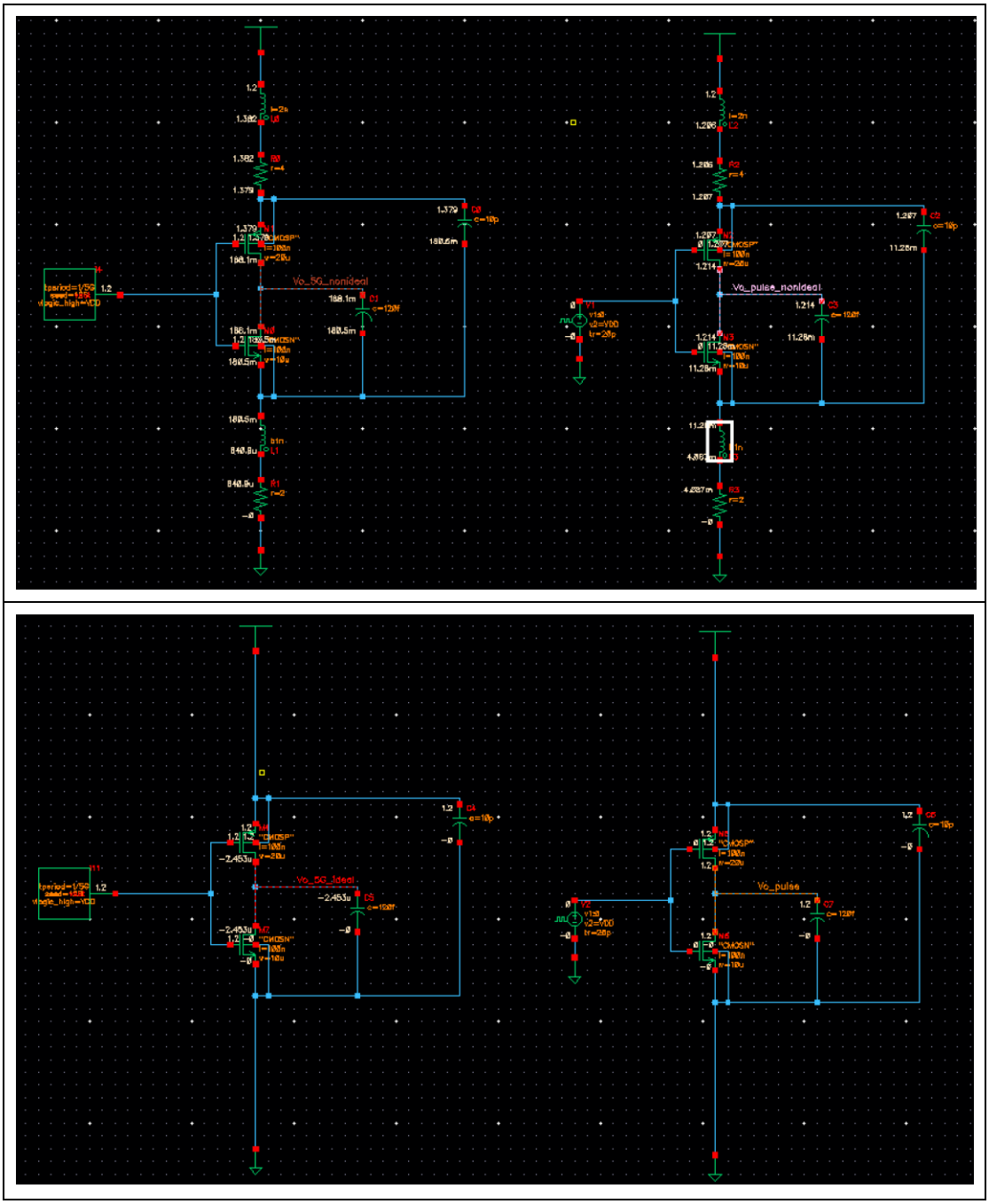
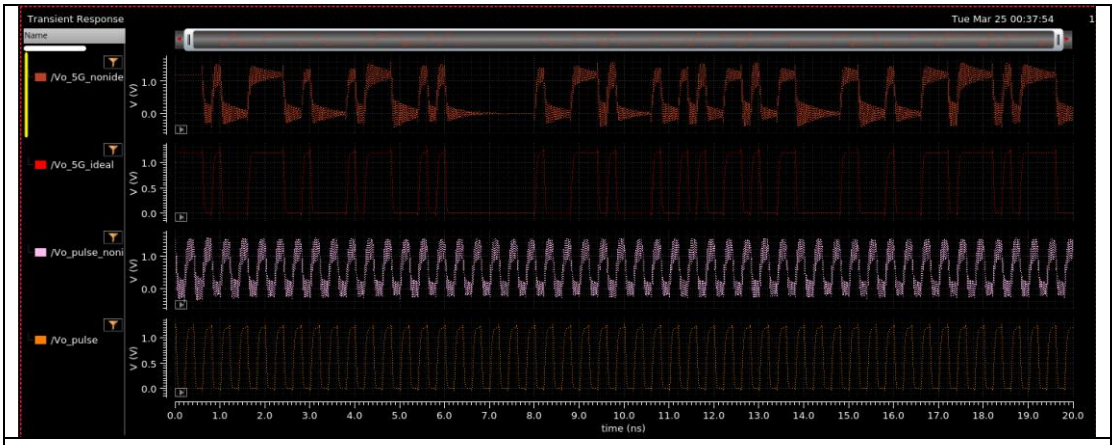
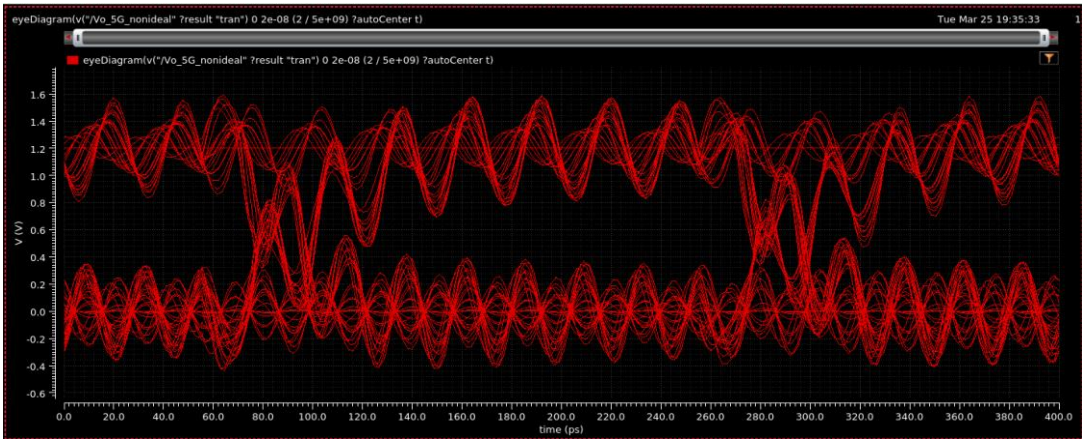
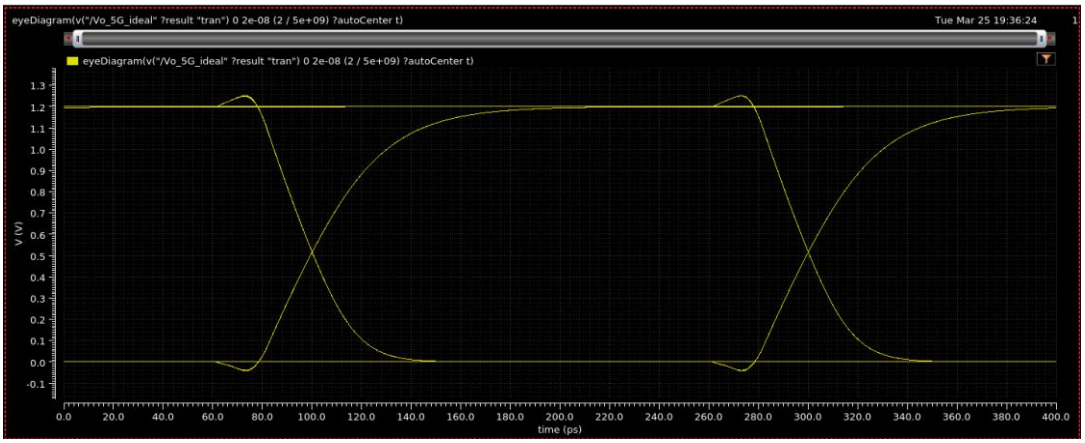
1. In digital circuit design, there are many switching signals. Finite supply impedance causes switching output noise. Build the circuit shown in Figure 28 with supply inductance and decoupling capacitance. Use Case 1: CLK (i.e. 1010 pattern) and Case 2: 7-bits PRBS as the input sources. CLK frequency is set to be 2.5GHz with 20ps rise/fall time. PRBS date rate is 5Gb/s with 20ps rise/fall time. Please plot the output eye diagrams. Compare the results with the case having ideal supply (zero supply impedance by removing all parasitics).




Transient Response
Tue Mar 25 00:37:54
/Vo_5G_nonide
/Vo_5G_ideal
/Vo_pulse_noni
/Vo_pulse
V (V)
time (ns)


eyeDiagram(v("/Vo_5G_nonideal" ?result "tran") 0 2e-08 (2 / 5e+09) ?autoCenter t)
Tue Mar 25 19:35:33
V (V)
time (ps)


eyeDiagram(v("/Vo_5G_ideal" ?result "tran") 0 2e-08 (2 / 5e+09) ?autoCenter t)
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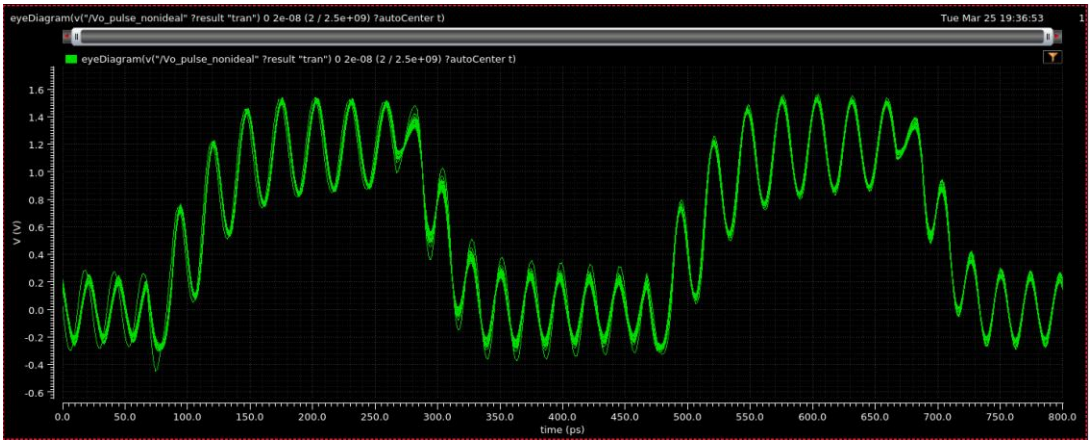
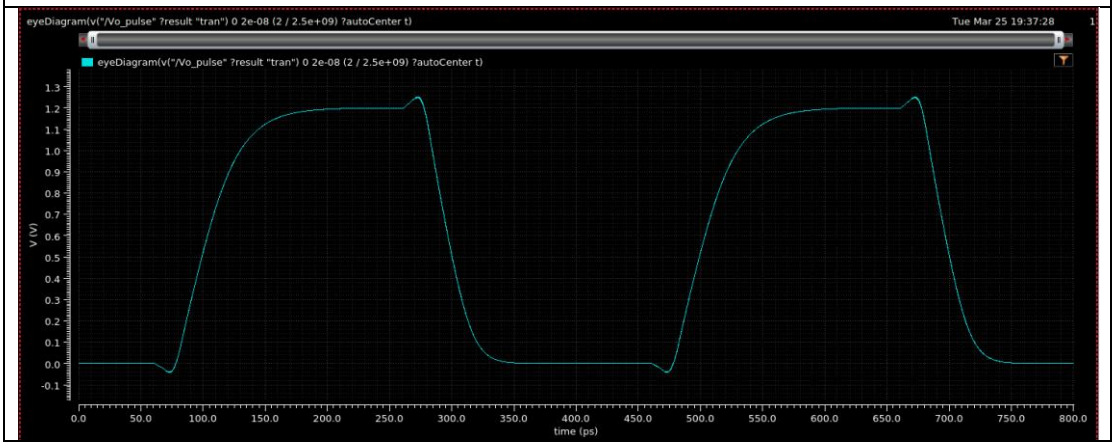
V (V)
time (ps)





2. Complete the noise and jitter budget tables.

Table 2 Noise Budget (V)

Parameter	Kn	RMS	Value (BER=10^{-12})
Peak Differential Swing			Q = 14.06 1
bounded RX Offset + Sensitivity			0.005
unbounded Power Supply Noise			0.004
bounded Residual ISI	0.03	X1	? 0.03
bounded Crosstalk	0.02	X1	? 0.02
unbounded Random Noise		0.002 X 14.06	? 0.02812
Attenuation	12dB	X10 $\frac{11}{10}$	? 0.2911
Total Noise			? 0.35822
Differential Eye Height Margin			? 0.132

bounded : 0.03 (ISI) + 0.02 (crosstalk) + 0.005 (offset) = 0.055 V.

+0.25V. _____

-0.25V. _____

Table 3 Jitter Budget (ps)

Component (BER=10^{-12})	RJ	DJ	TJ
TX+PLL	14.06 1	12	26.06?
Channel	21.09 1.5	25	46.09?
RX+CDR	28.12 2	12	40.12?
RSS TJ	37.85 ?	? 49	86.85?
	random	determin	

TX+ PLL = (rms) $\sqrt{1^2}$ X Q (14.06) = 14.06

Channel = $\sqrt{1.5^2}$ X Q = 21.09

RX+ CDR = $\sqrt{2^2}$ X Q = 28.12

RSS TJ : $\sqrt{1^2+1.5^2+2^2}$ = 37.85