# 25 Spring ECEN 720: High-Speed Links: Circuits and Systems Post-lab Report

## Lab5: Equalization Circuits

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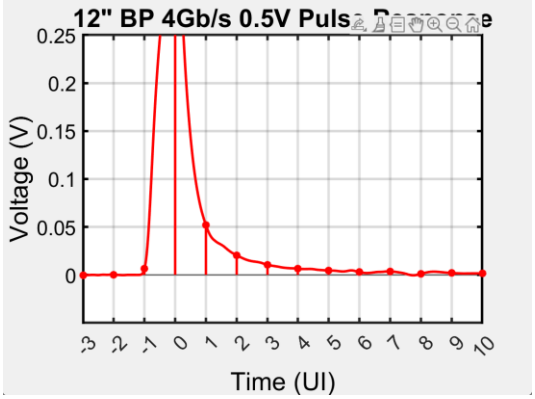
Section:700

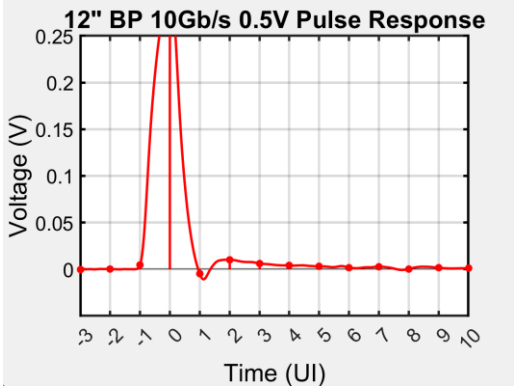
Professor: Sam Palermo

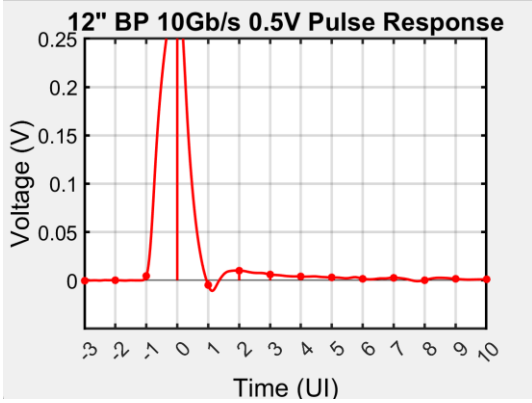
TA: Srujan Kumar Kaile

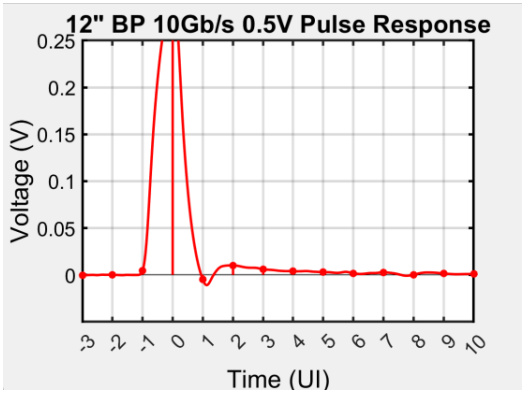
1. TX FIR Equalization. This problem investigates TX FIR equalization using the 12" Backplane channel "peters_01_0605_B12_thru.s4p" from course website. For parts (a) and (b), use the example MATLAB code "channel_data_pulse_pda.m" and produce the following 2 graphs:

a) Peak-Distortion Eye Height versus FIR tap number at 4G, 8G, and 16Gbps (3 lines). For the tap numbers, use 1-tap (no equalization), 2-tap (1-post), 3-tap (1-pre and 1-post), and 4-tap (1-pre, 2-post). Don't restrict the TX equalizer resolution for this graph.

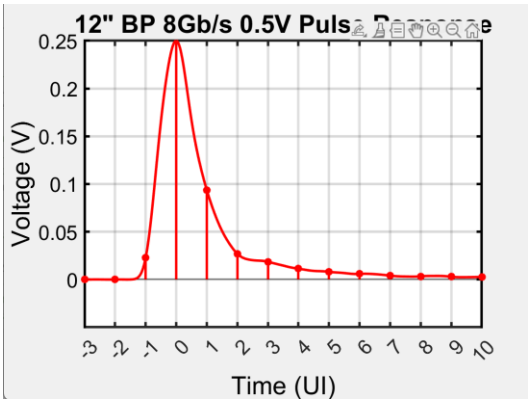
<table>
<tr>
<td> 

<br>pda_eye_height =<br>0.4501<br>4G-1tap (No equ)</td>
<td> 

<br>pda_eye_height =<br>0.4957<br>4G-2tap (1post)</td>
</tr>
<tr>
<td> 

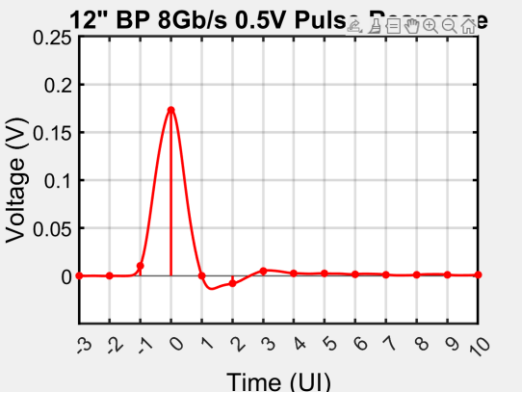
<br>pda_eye_height =<br>0.4957<br>4G-3tap (1pre&1post)</td>
<td> 

<br>pda_eye_height =<br>0.4957<br>4G-4tap (1pre&2post)</td>
</tr>
</table>



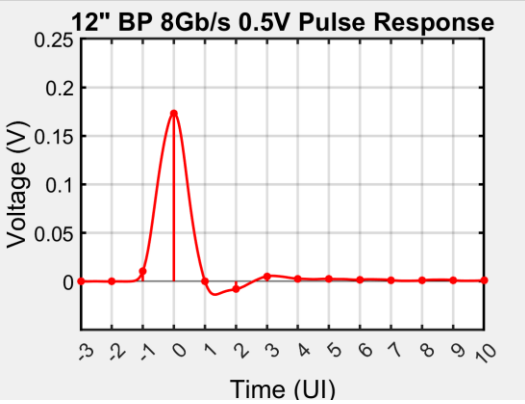

```
pda_eye_height =

    0.0302
```

8G-1tap (No equ)



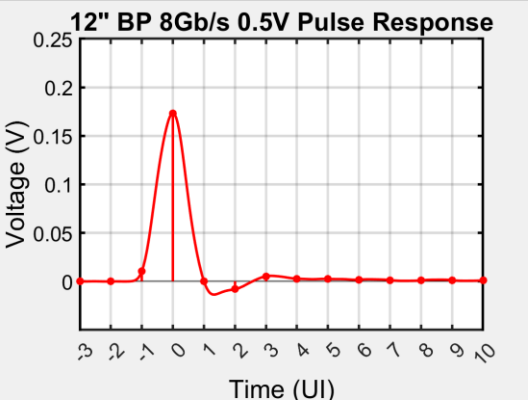

```
pda_eye_height =

    0.2241
```

8G-2tap (1post)



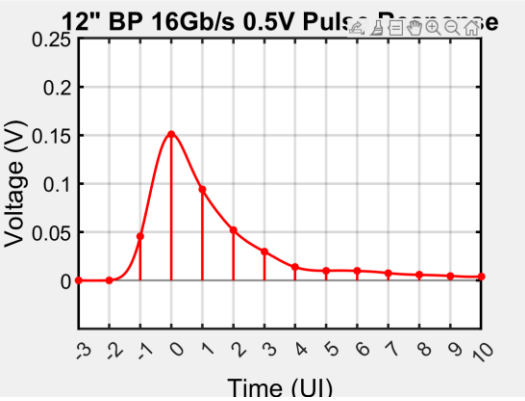

```
pda_eye_height =

    0.2241
```

8G-3tap (1pre&1post)

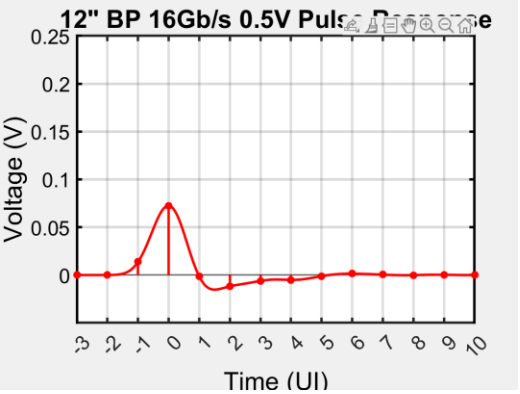



```
pda_eye_height =

    0.2241
```

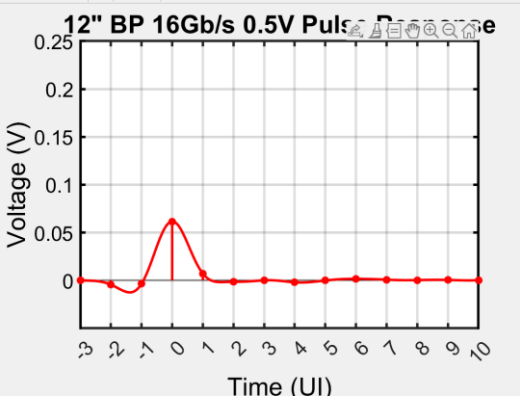
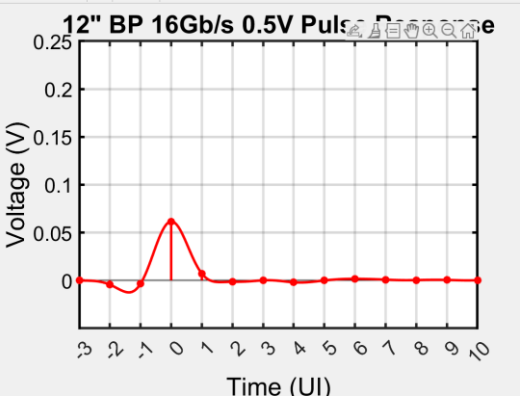
8G-4tap (1pre&2post)

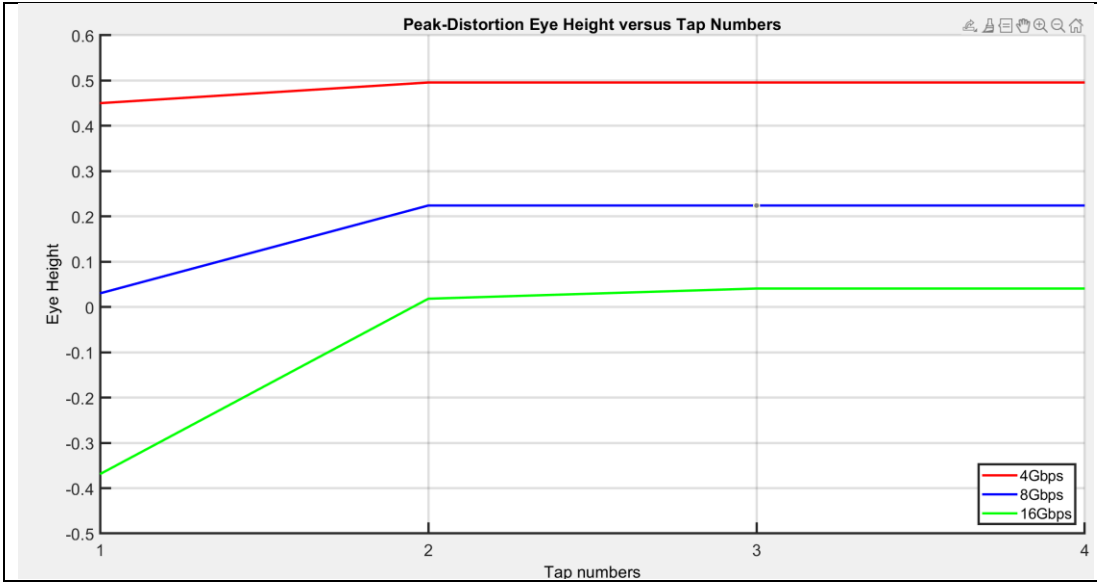



```
pda_eye_height =

   -0.3689
```

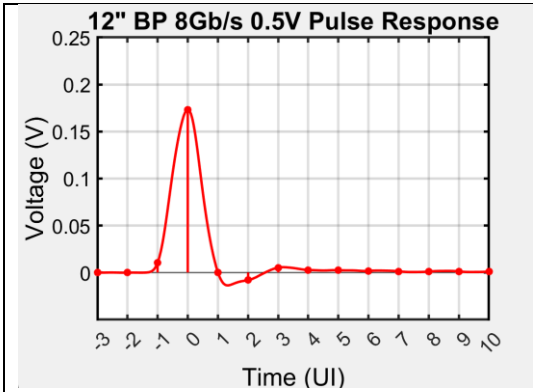



```
pda_eye_height =

    0.0183
```

| 16G-1tap | 16G-2tap (1post) |
| --- | --- |
|  <br>pda_eye_height =<br>0.0408 |  <br>pda_eye_height =<br>0.0408 |
| 16G-3tap (1pre&1post) | 16G-4tap (1pre&2post) |

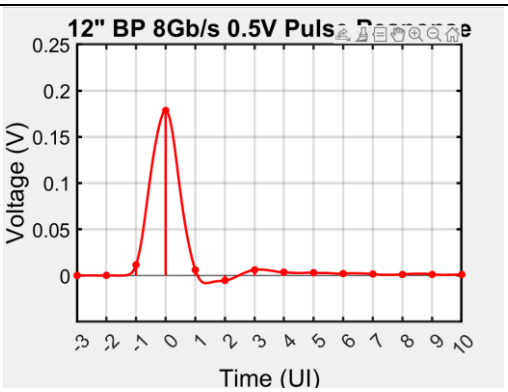



b) 8Gb/s Peak-Distortion Eye Height versus Equalizer Resolution with 2, 3, and 4-tap equalization (3-lines). For the tap resolution sweep, use 3, 4, 5, 6 bits, and also include the infinite resolution data. Note: The above MATLAB code also requires the “tx_eq.m” function. Also, this MATLAB code is only a reference code. Feel free to modify and improve upon the code as you wish.



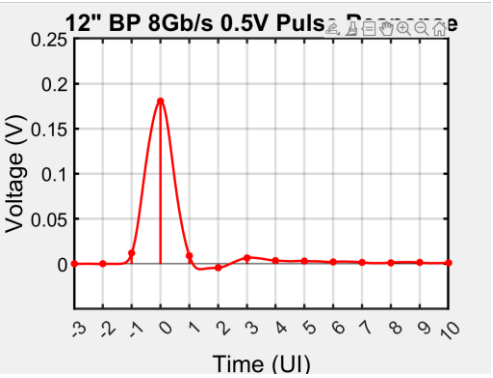

```
pda_eye_height =

    0.2241
```

8G 2tap (1post) 3bit resolution



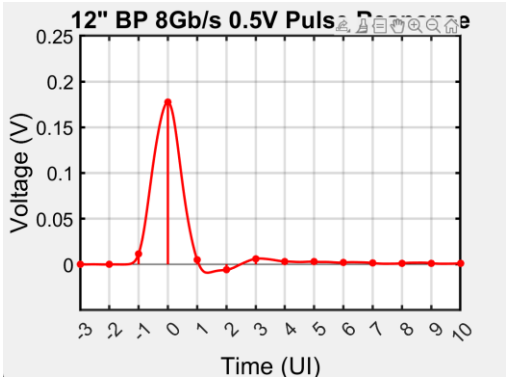

```
pda_eye_height =

    0.2190
```

8G 2tap (1post) 4bit resolution



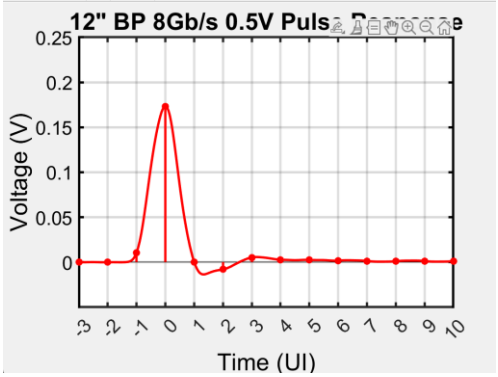

```
pda_eye_height =

    0.2165
```

8G 2tap (1post) 5bit resolution



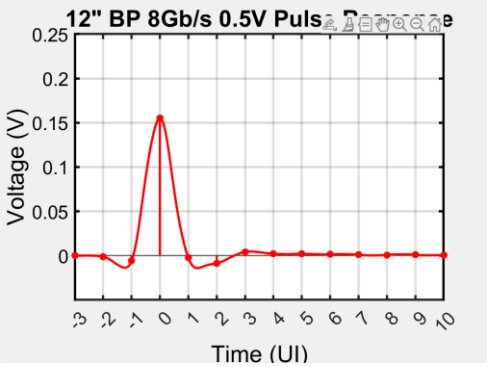

```
pda_eye_height =

    0.2199
```

8G 2tap (1post) 6bit resolution



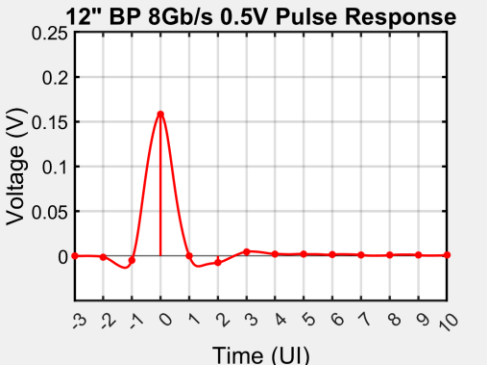

```
pda_eye_height =

    0.2241
```

8G 3tap (1post 1pre) 3bit resolution



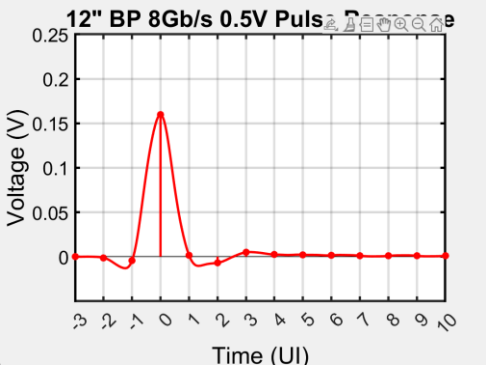

```
pda_eye_height =

    0.2010
```

8G 3tap (1post 1pre) 4bit resolution



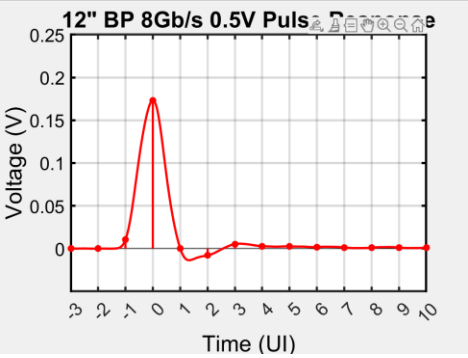

```
pda_eye_height =

    0.2129
```

8G 3tap (1post 1pre) 5bit resolution



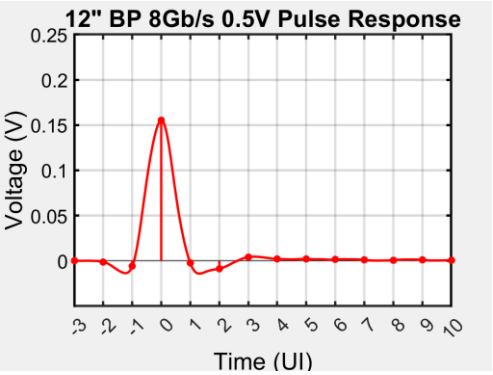

```
pda_eye_height =

    0.2129
```

8G 3tap (1post 1pre) 6bit resolution



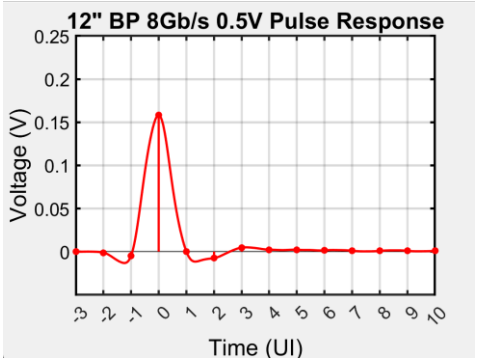

```
pda_eye_height =

    0.2241
```

8G 4tap (2post 1pre) 3bit resolution



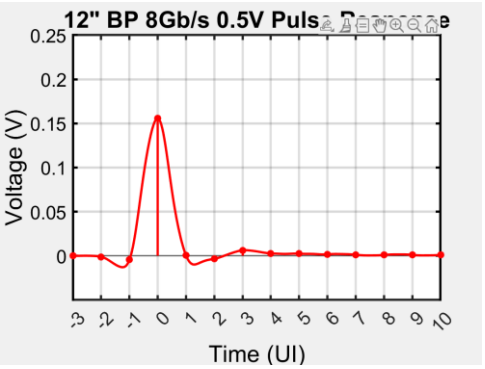

```
pda_eye_height =

    0.2010
```

8G 4tap (2post 1pre) 4bit resolution



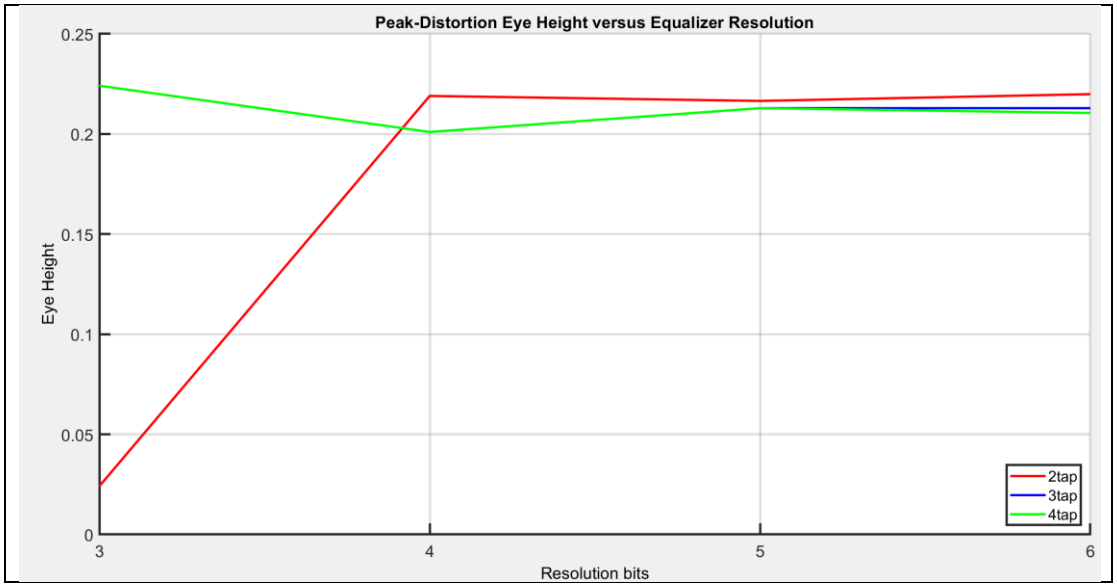

```
pda_eye_height =

    0.2129
```

8G 4tap (2post 1pre) 5bit resolution




```
pda_eye_height =

    0.2105
```

8G 4tap (2post 1pre) 6bit resolution




c) Design an 8Gb/s TX Driver with Equalization [4]. Modify one of your drivers from Lab3 to include FIR equalization.

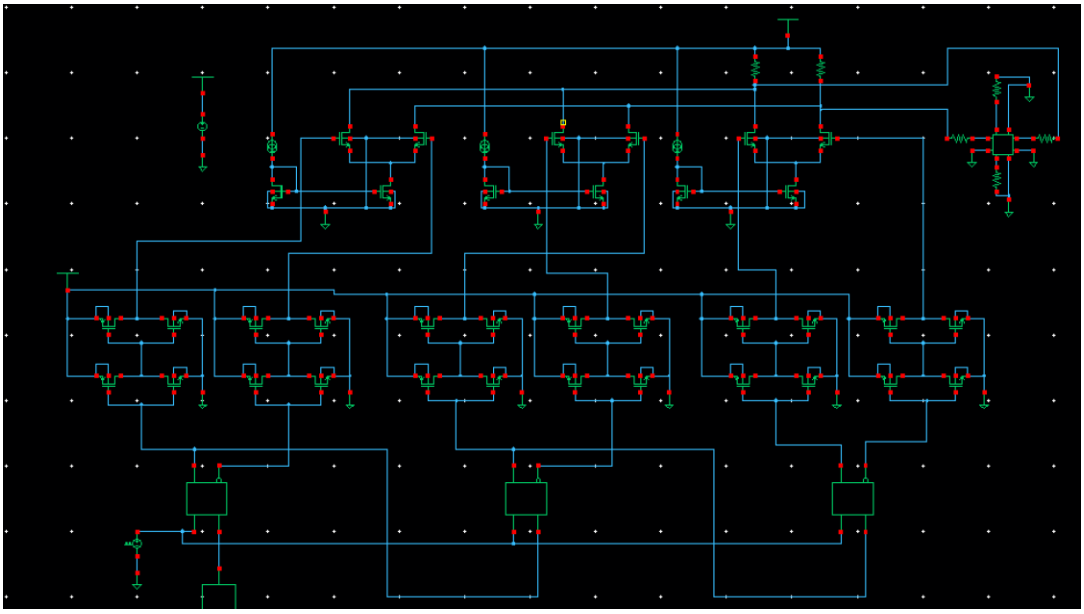
i. The maximum output voltage swing can be anywhere from 300mVppd (min.) to 1Vppd (max.). This gives you the flexibility to choose whichever driver you wish – from low-swing voltage-mode to current-mode.

ii. Use the results from part (a) and (b) to justify your tap number and resolution.

iii. Include two 8Gb/s PRBS eye diagrams – one without equalization (all weight on main cursor) and one with the proper equalization taps enabled. Import the s parameter file into your Cadence simulation to produce the eye diagrams. Make sure the channel is properly terminated at both ends. Note, as you will have some additional driver capacitance, the equalization taps may change slightly.

iv. The driver and at least one pre-driver stage should be full-transistor level design. The other blocks (PRBS, delay elements, etc) can be macro-models.

v. Report transmitter power consumption, power efficiency (mW/Gb/s), and 8Gb/s eye height and width.



ADE L (3) - lab5 TXFIR schematic@n01-zeus.olympus.ece.tamu.edu

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help cadence

27

Design Variables

| | Name | Value |
|---|---|---|
| 1 | VDD | 1.2 |
| 2 | DD | 1.2 |
| 3 | equ | 8G |
| 4 | 31 | 0 |
| 5 | 32 | 21m |
| 6 | 33 | 9m |
| 7 | /n | 50u |
| 8 | /p | 100u |

> Results in ...harrison900531/cadence/simulati

Analyses

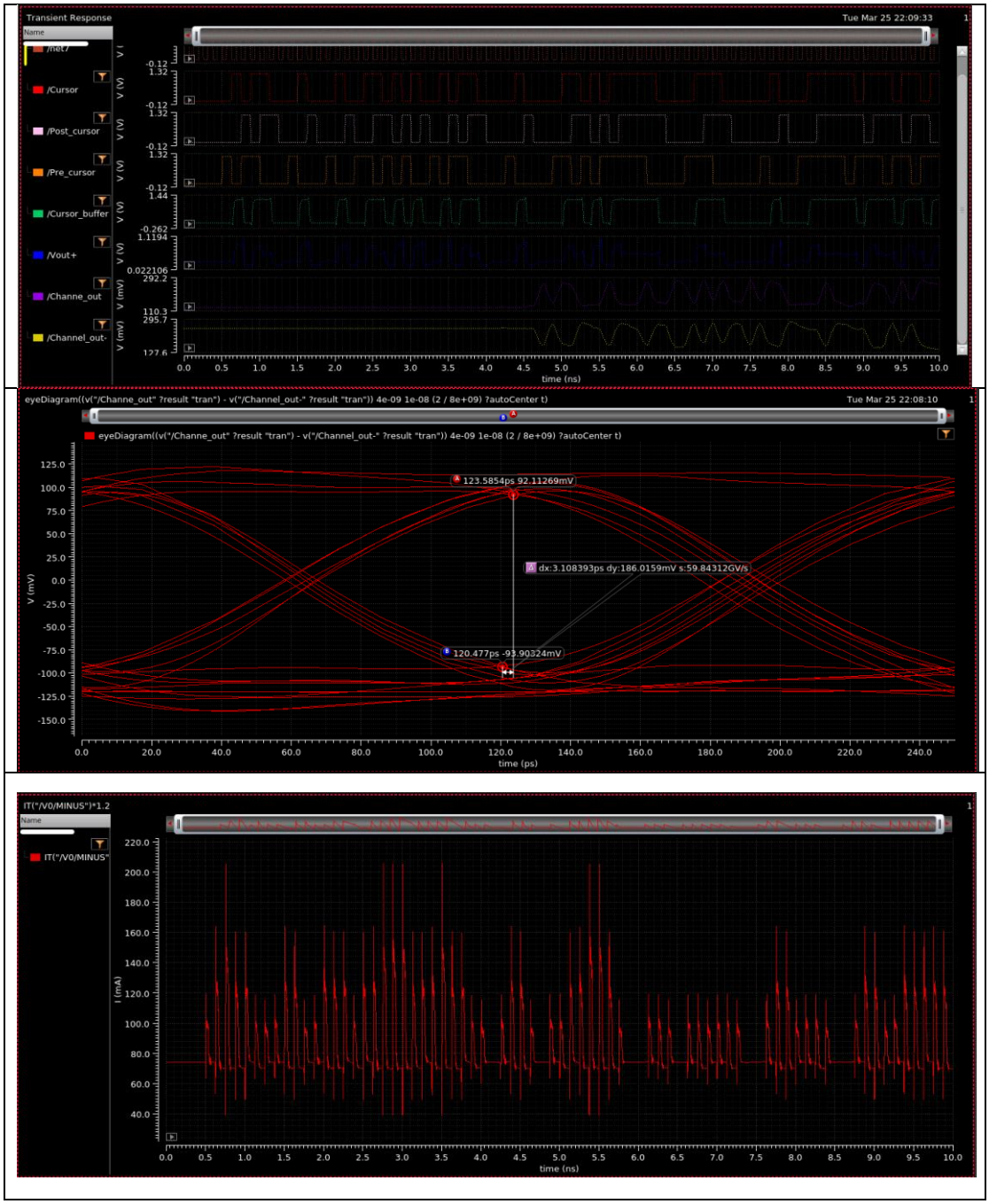
| | Type | Enable | Arguments |
|---|---|---|---|
| 1 | tran | ☑ | 0 10n |

Outputs

| | Name/Signal/Expr | Value | Plot | Save | Save Optior |
|---|---|---|---|---|---|
| 1 | net7 | | ☑ | ☑ | allv |
| 2 | Cursor | | ☑ | ☑ | allv |
| 3 | Post_cursor | | ☑ | ☑ | allv |
| 4 | Pre_cursor | | ☑ | ☑ | allv |
| 5 | Cursor_buffer | | ☑ | ☑ | allv |
| 6 | Vout+ | | ☑ | ☑ | allv |

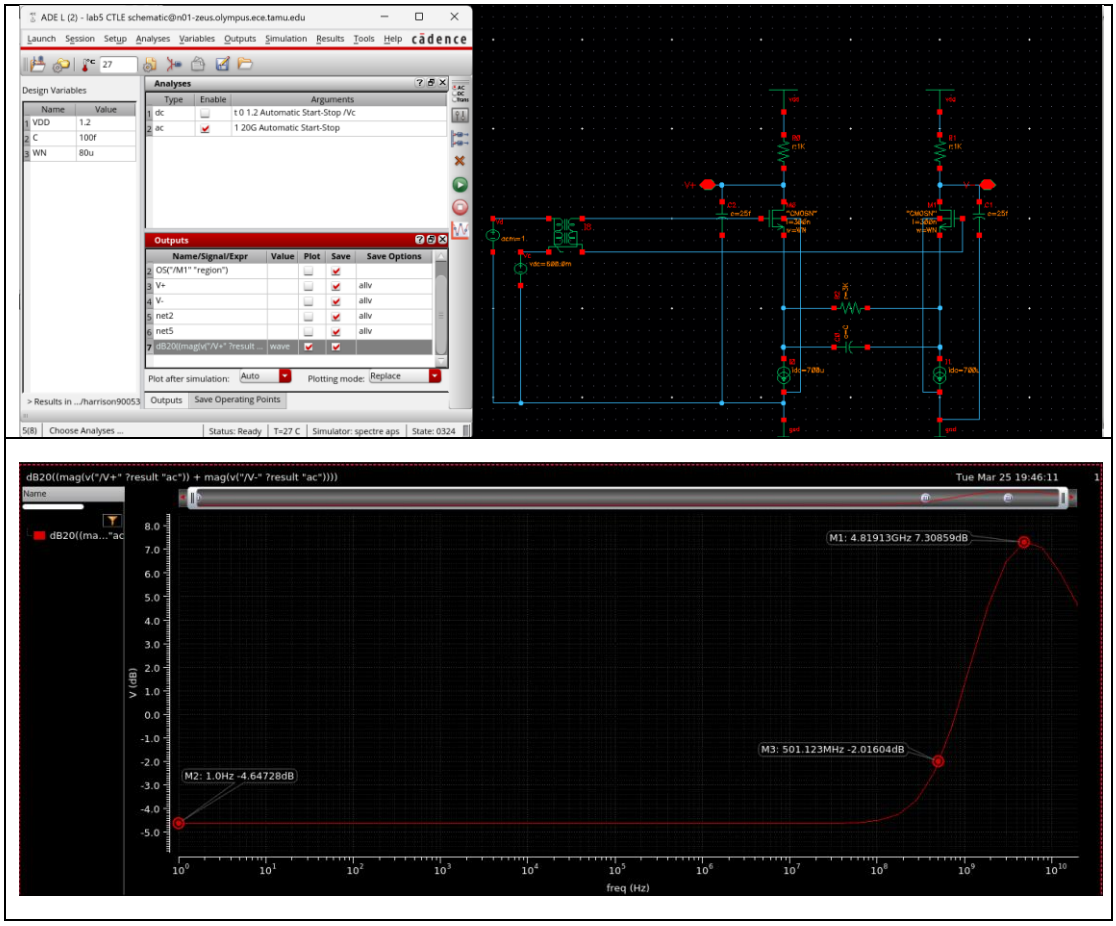
Plot after simulation: Auto  Plotting mode: Replace

11(22) | Netlist and Run | Status: Ready | T=27 C | Simulator: spectre aps | State: 0324

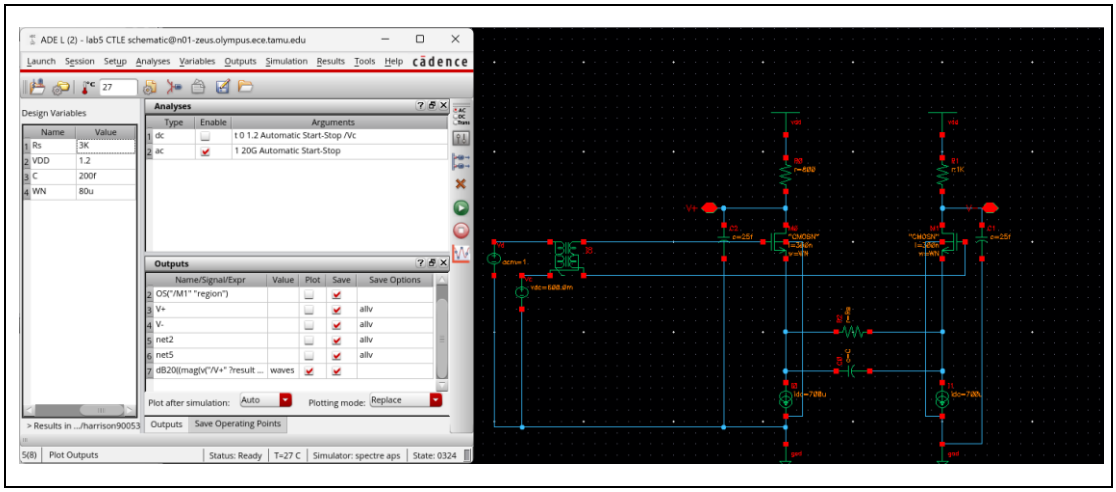


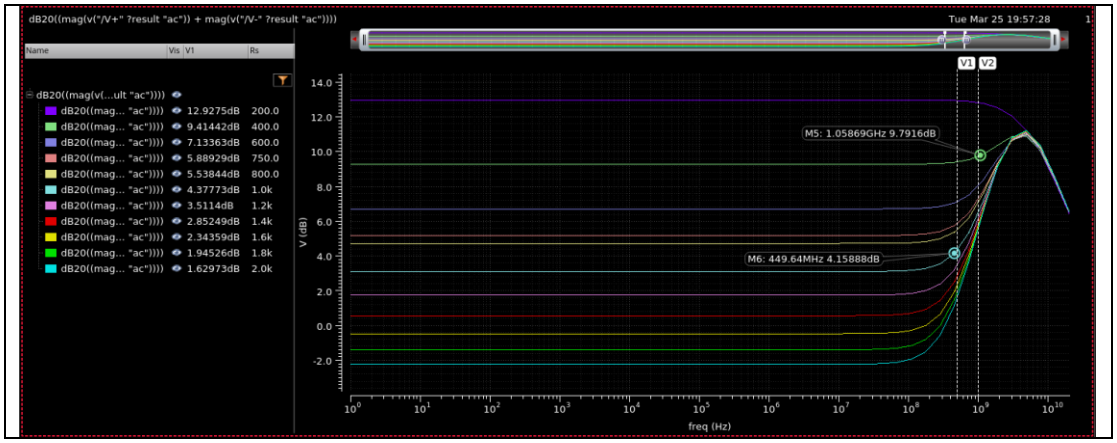

2. RX CTLE Equalization. Design an 8Gb/s active CTLE to meet the following specifications:

a) Min peak gain at Nyquist (4GHz) of 6dB

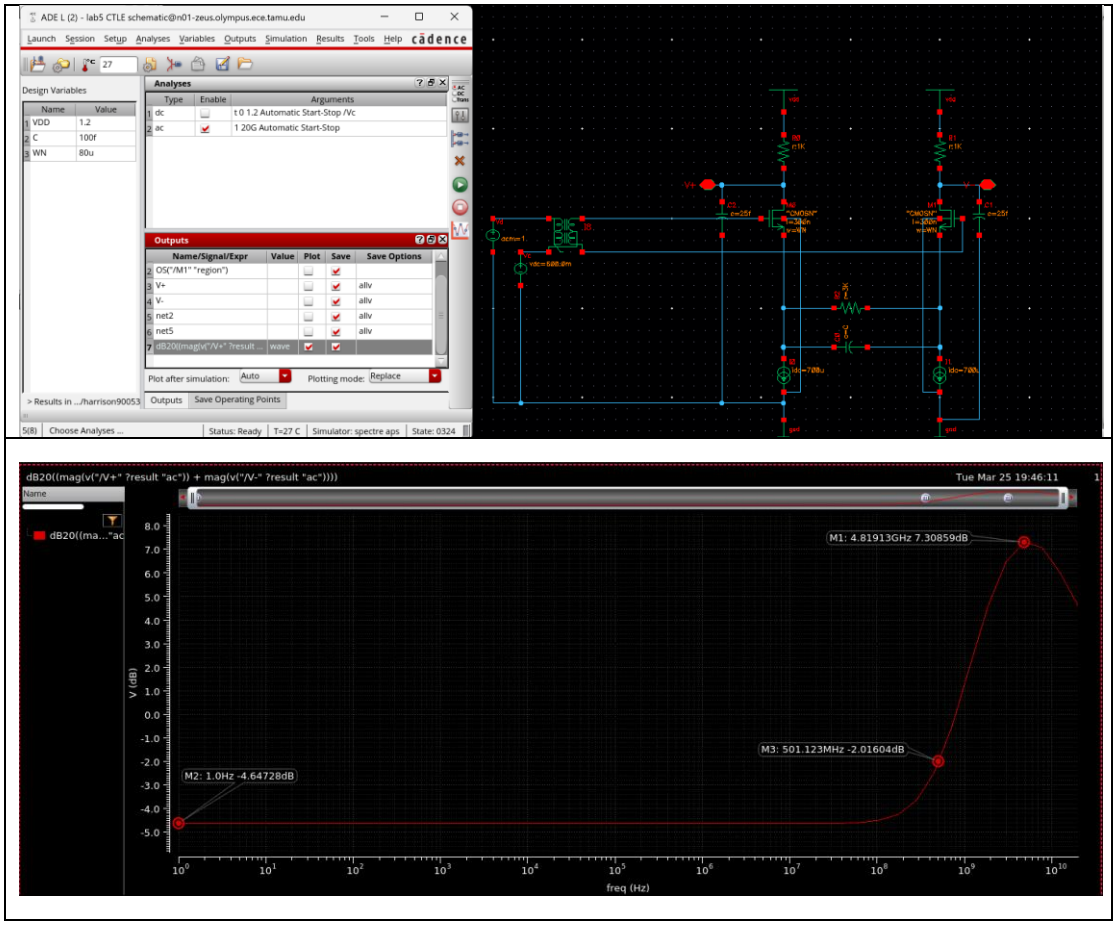



b) Zero frequency tunable from a minimum range of 500MHz to 1GHz

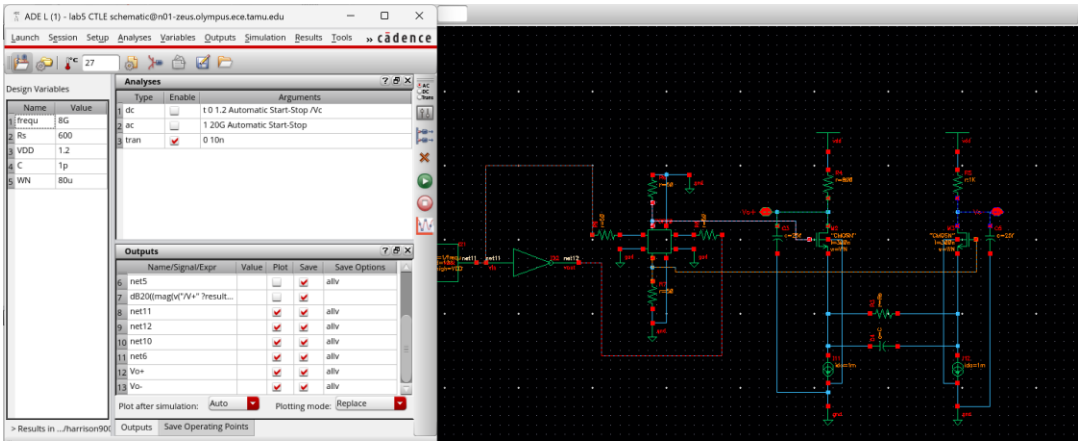


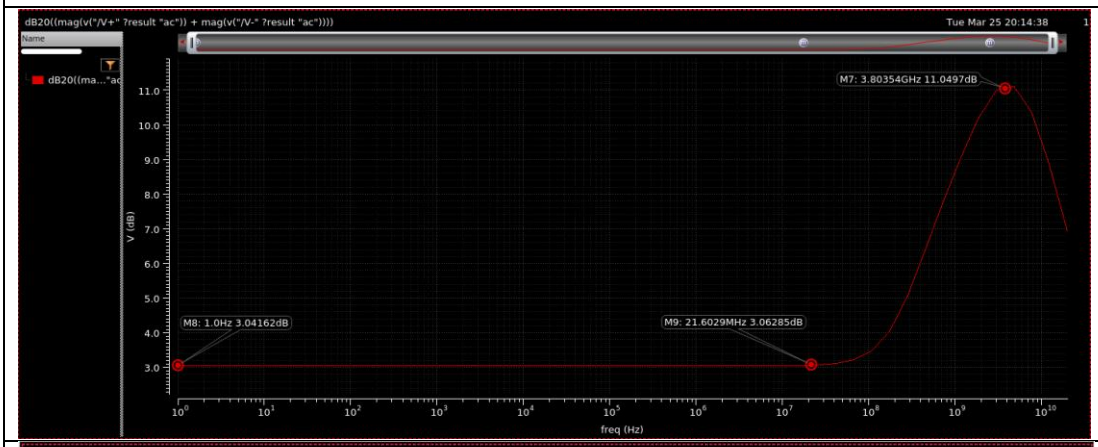


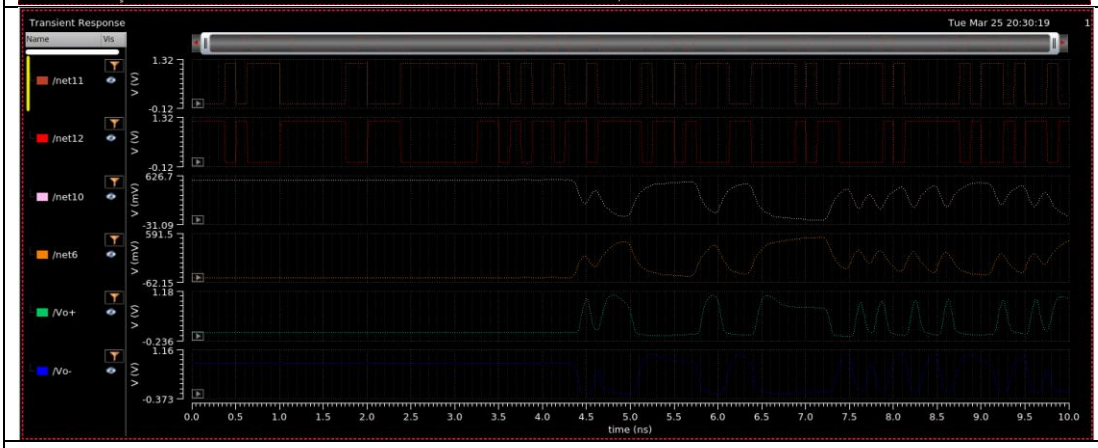

c) Minimum tunable peaking (magnitude difference between Nyquist and low frequency response) range of 12dB (Example: +6dB at Nyquist frequency and -6dB at low frequency).

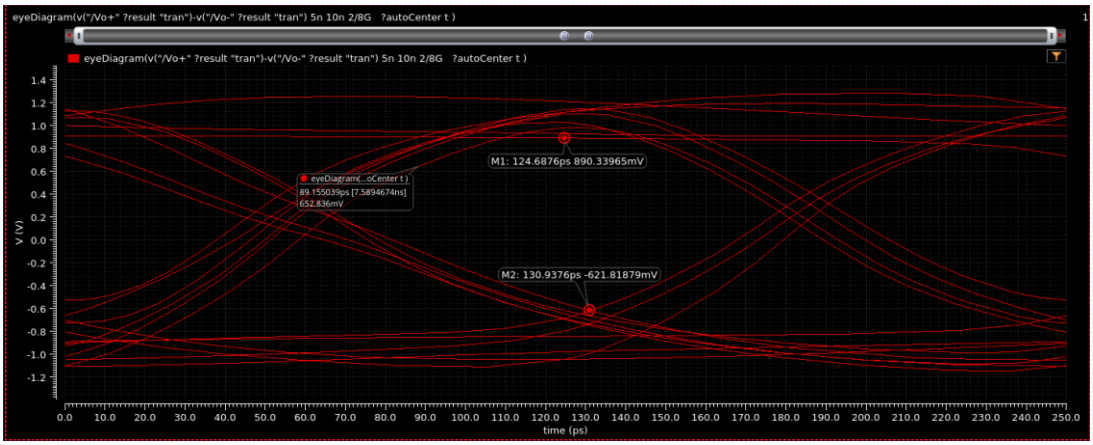


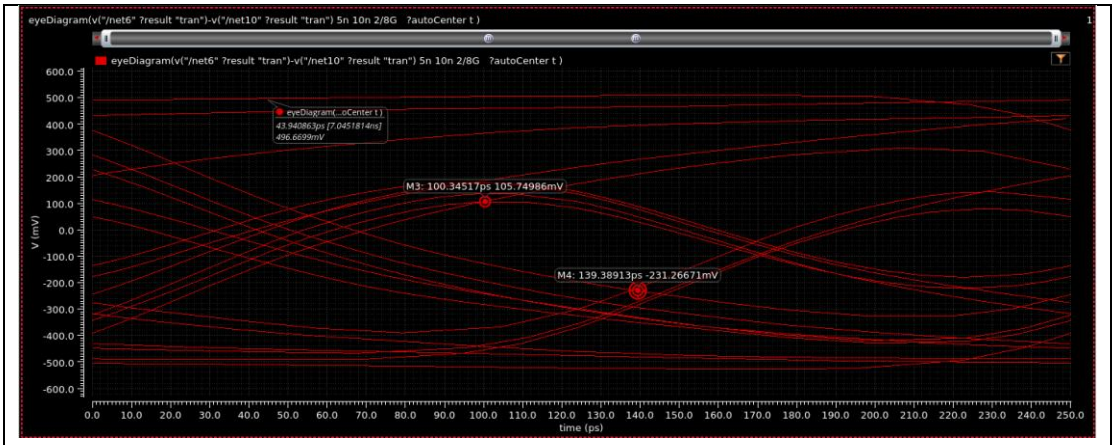

d) Load capacitor = 25fF i. Produce frequency response plots showing the zero and peaking tunability. ii. Produce an 8Gb/s PRBS eye diagram with the 12” Backplane channel output as the input to the CTLE. Optimize the CTLE settings for optimal eye opening.


ADE L (1) - lab5 CTLE schematic@n01-zeus.olympus.ece.tamu.edu
Launch Session Setup Analyses Variables Outputs Simulation Results Tools
cadence
Design Variables
Name Value
1 frequ 8G
2 Rs 600
3 VDD 1.2
4 C 1p
5 WN 80u
Analyses
Type Enable Arguments
1 dc t 0 1.2 Automatic Start-Stop /Vc
2 ac 1 20G Automatic Start-Stop
3 tran 0 10n
Outputs
Name/Signal/Expr Value Plot Save Save Options
6 net5 allv
7 dB20((mag(v("/V+" ?result... allv
8 net11 allv
9 net12 allv
10 net10 allv
11 net6 allv
12 Vo+ allv
13 Vo- allv
Plot after simulation: Auto
Plotting mode: Replace
Outputs
Save Operating Points

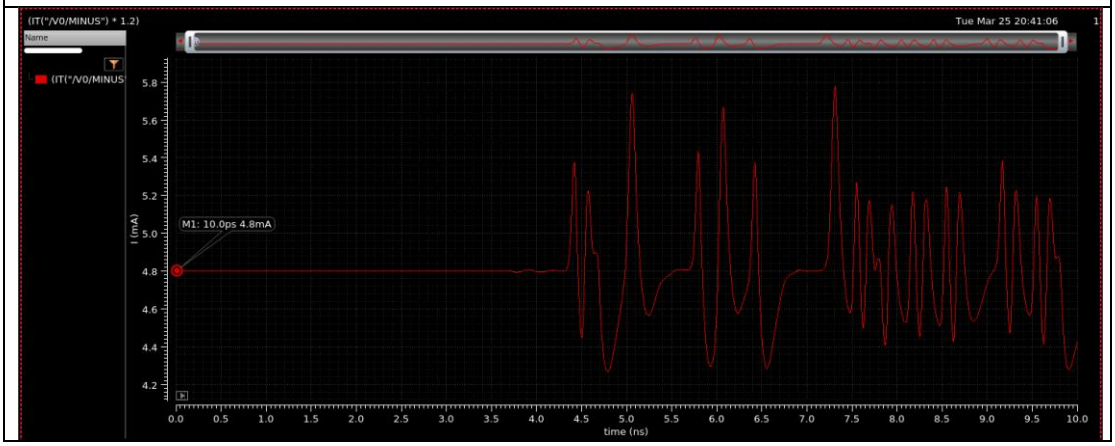

dB20((mag(v("/V+" ?result "ac")) + mag(v("/V-" ?result "ac"))))
Tue Mar 25 20:14:38
M7: 3.80354GHz 11.0497dB
M8: 1.0Hz 3.04162dB
M9: 21.6029MHz 3.06285dB
V (dB)
freq (Hz)


Transient Response
Tue Mar 25 20:30:19
/net11
/net12
/net10
/net6
/Vo+
/Vo-
V (V)
V (mV)
time (ns)


eyeDiagram(v("/Vo+" ?result "tran")-v("/Vo-" ?result "tran") 5n 10n 2/8G ?autoCenter t )
M1: 124.6876ps 890.33965mV
M2: 130.9376ps -621.81879mV
V (V)
time (ps)




No CTLE



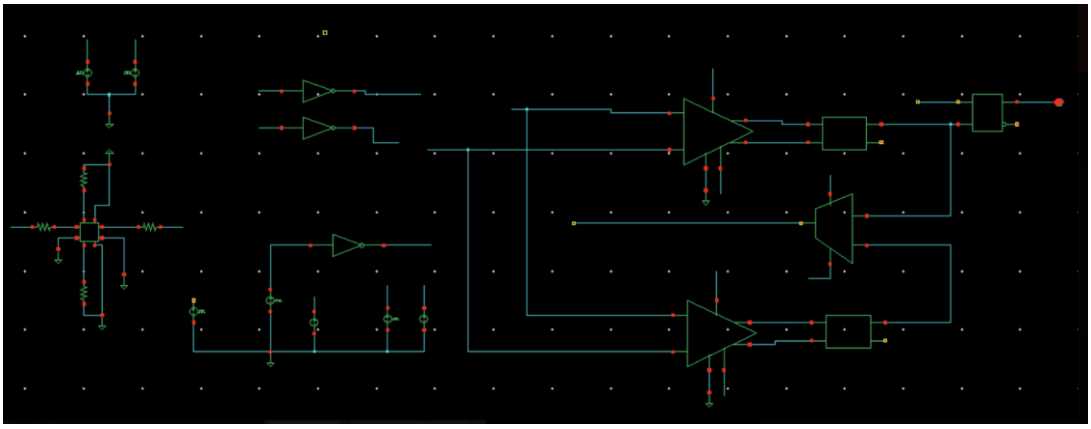

3. RX DFE Equalization. Design an 8Gb/s 2-tap DFE [2][3].

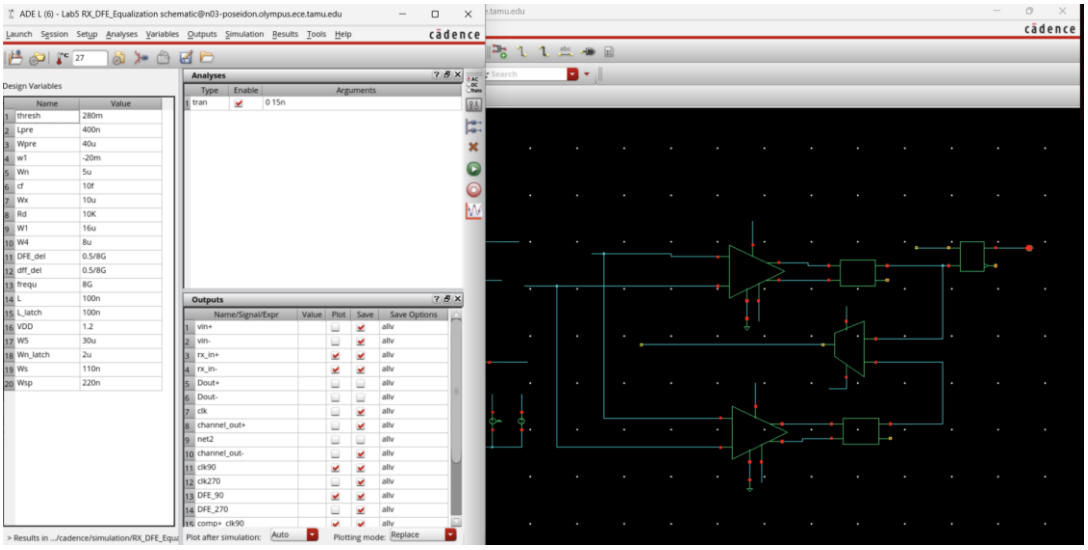
a) Use one of the comparators you designed in Lab4 in your design. Note, you probably have to speed this design up – as you will need a 4GHz clock if you implement a half rate design.

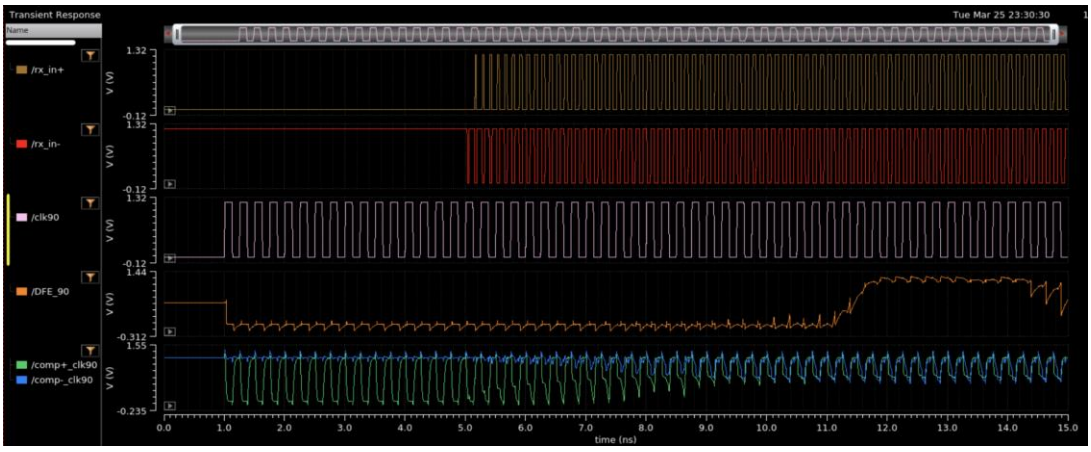
b) The only thing that has to be transistor level is the comparator. The rest of the blocks (summer, feedback taps, other logic) can be macro-models. Note, for the summer model make sure to capture the RC settling if you use a linear resistive load summer. Feel free to investigate an integrating architecture if you prefer.

c) Produce an 8Gb/s PRBS eye diagram at the summer output with the 12” Backplane channel output as the input to the DFE. Optimize the DFE settings for optimal eye opening at the input of the comparator (summer output).

d) Report DFE power, power efficiency (mW/Gb/s), and 8Gb/s eye height and width. e) Note, you have to synchronize the DFE with the incoming data stream. A good way to do this is with an initial “lone pulse” input pattern. Adjust your comparator clock to sample near the peak of the lone pulse. Then simulate with the PRBS data.




ADE L (6) - Lab5 RX_DFE_Equalization schematic@n03-poseidon.olympus.ece.tamu.edu
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help
cadence
Design Variables
Name Value
thresh 280m
Lpre 400n
Wpre 40u
w1 -20m
Wn 5u
cf 10f
Wx 10u
Rd 10K
W1 16u
W4 8u
DFE_del 0.5/8G
dff_del 0.5/8G
frequ 8G
L 100n
L_latch 100n
VDD 1.2
W5 30u
Wn_latch 2u
Ws 110n
Wsp 220n
Analyses
Type Enable Arguments
tran 0 15n
Outputs
Name/Signal/Expr Value Plot Save Save Options
vin+
vin-
rx_in+
rx_in-
Dout+
Dout-
clk
channel_out+
net2
channel_out-
clk90
clk270
DFE_90
DFE_270
comp+ clk90
Plot after simulation: Auto
Plotting mode: Replace


Transient Response
Tue Mar 25 23:30:30
/rx_in+
/rx_in-
/clk90
/DFE_90
/comp+_clk90
/comp-_clk90
1.32
-0.12
1.44
-0.312
1.55
-0.235
V (V)
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
11.0
12.0
13.0
14.0
15.0
time (ns)