Question 1: Using the "Direct Mapped Cache", assume that

- 4-blocks, 1 word/block, direct mapped
- Initial state is empty as shown below.

Index	V	Tag	Data
00	N		
01	N		
10	N		
11	N		

And the following addresses have been requested in the following sequences:

Request 1: Word Addresses 4, 5 and 7

Request 2: Word Addresses 0, 1 and 3

Request 3: Word Addresses 1, 2 and 3

Request 4: Word Addresses 3, 4 and 6

A) Show the cache state **Before** and **After** each time that addresses have been requested.

B) Calculate the Hit Ratio and Miss Ratio.

Hint: Follow the example in the next page and fill up all missing data accordingly and calculate the Hit and Miss ratios.

Request 1:

Word addr	Binary addr	Hit/miss	Cache block
4	100	Miss	00
5	101	Miss	01
7	111	Miss	21

Before			After				
Index	V	Tag	Data	Index	٧	Tag	Data
00	N			00	Y		Mem[100]
01	N			01	Y	1	Mem[101]
10	N			10	N		
11	N			11	Y	1	Mem[II]

Request 2:

Word addr	Binary addr	Hit/miss	Cache block
0	000	MISS	0
1	001	M155	· 1
3	011	Miss	21

Before			After				
Index	V	Tag	Data	Index	V	Tag	Data
00	Y	1	MCM[100]	00	γ	0	Mem[000]
01	~	1	MehTI	01	*	0	Mem[001]
10	7			10	2		
11	×	1	Mem[111]	11	Y	Q	Mem[oli]

Request 3:

Word addr	Binary addr	Hit/miss	Cache block
1	0.1	Hie	0
2	010	Mi 55	10
3	0 (1)	Hit	17

	Before			After			
Index	V	Tag	Data	Index	٧	Tag	Data
00	Y	0	Mem[000]	00	Y	0	Mem[000]
01	Y	0	MeMT001]	01	Y	0	mem[0017
10	N			10	Y	0	Mem[olo]
11	Y	0	McM[011]	11	Y	G	McM[OII]

Request 4:

Word addr	Binary addr	Hit/miss	Cache block
3	011	Hit	11
4	(00	Miss	0 0
6	110	Miss	10

	Before			After			
Index	V	Tag	Data	Index	V	Tag	Data
00	Y	0	mem[noo]	00	4		Mem[100]
01	Y	0	Memtools	01	Y	Q	Memto013
10	Y	0	MemTolo3	10	Y		MeME 1107
11	Y	0	Mem[011]	11	Y	0	Mem[911]