Question 1: What are the possible hazards in building Processor's Pipeline? Explain each possible hazard?

1- Structure Hazards:

Conflict for use of a resource

Pipeline with a single memory

Load/store requires data access.

Instruction fetch would have to stall for that cycle.

Pipelined data paths require separate instruction/data memories.

2- Data Hazards:

An instruction depends on completion of data access by a previous instruction.

2.1 - Forwarding (aka Bypassing):

Don't wait for it to be stored in a register!

Requires extra connections in the data path.

2.2 - Load-Use Data:

Can't always avoid stalls by forwarding.

If value not computed when needed

Can't forward backward in time!

3- Control Hazards:

Ranch determines flow of control:

3.1 -Fetching next instruction depends on branch outcome.

3.2 -Pipeline can't always fetch the correct instruction.