Sheng-Jung Yu

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Research Interests

Electronic Design Automation (Focused on Physical Design and Design for Manufacturability), Integrated Circuit Systems

Education

National Taiwan University (NTU) *Taipei, Taiwan*

B.S. in Electrical Engineering *09/2015 - 06/2019*

- Cumulative GPA: **4.28**/4.30.
- Major GPA: **4.29**/4.30.
- Class Rank: **1**/190.

Research Experience

***Undergraduate Research Assistant*, Electronic Design Automation Lab, Prof. Yao-Wen Chang** *Taipei, Taiwan*

Optical Network-on-Chip (ONoCs) Design Automation. *12/2018 - 11/2019*

- Proposed and implemented an **automated structural and physical co-design engine** for Optical Network-on-Chip System.
- Outperformed the state-of-the-art ONoCs work by 40% reduction in maximum insertion loss.

Optical Interconnect Routing *12/2017 - 11/2018*

- Proposed and implemented a **WDM-aware clustering algorithm** to minimize both insertion loss and wire length.
- Outperformed the state-of-the-art algorithm by 60% insertion loss reduction and 45% wire length reduction.

***Undergraduate Research Assistant*, Digital Circuits and Systems Lab, Prof. Chia-Hsian Yang** *Taipei, Taiwan*

Encryption IC design *04/2018 - 11/2019*

- Designed an accelerator for the end-to-end encryption Signal Protocol.
- Designed hardware architecture for cryptographics primitives including SHA-256, Elliptic Curve 25519, AES-256

***Undergraduate Research Assistant*, Iris Lab, Prof. Iris-Hui-Ju Jiang** *Taipei, Taiwan*

Timing-Aware Fill Insertion *04/2018 - 4/2019*

- Designed and Implemented an equivalent capacitance guided dummy fill insertion engine for 2018 ICCAD contest.
- Outperformed all contest winners and the state-of-the-art work by over 27%.
- Published a paper in ASPDAC-20 and the paper was nominated as best paper.

***R&D Intern*, Portwell, Inc.** *New Taipei City, Taiwan*

FPGA-CPU heterogeneous computing *07/2017 - 09/2017*

- Designed and Implemented feature points algorithm on heterogeneous computation using CPU and FPGA with OpenCL.
- Achieved a 20X acceleration compared with pure CPU computation.

Publications

1. **Sheng-Jung Yu**, Chen-Chien Kao, Chia-Han Huang and Iris Hui-Ru Jiang, "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability," in *Proc. of IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC-20)*, **(Best Paper Nominee)**
2. Yu-Sheng Lu, **Sheng-Jung Yu** and Yao-Wen Chang, "A Provably Good Wavelength-Division Multiplexing Aware Clustering Algorithm for On-Chip Optical Routing," (Submitted to DAC-20)
3. Yu-Sheng Lu, **Sheng-Jung Yu** and Yao-Wen Chang, "Optical Network Structure and Physical Routing Codesign," (Submitted to DAC-20)

Teaching

***Teaching Assistant*, Electrical Engineering Lab (Digital Circuit) (Fall 2018), Prof. Chia-Hsian Yang** *09/2018-01/2019*

- Instructed the students on the labs about random number generator.
- Answered questions about verilog and FPGAs.

Honors & Awards

2016-2019 **Dean's List, 8 times**, National Taiwan University
2018 **Top 10**, 2018 ICCAD Contest
2018 **2nd place**, CAD Contest, Ministry of Education, Taiwan
2018 **Best Presentation**, Final Project Contest of Machine Learning Course
2017 **3rd place**, Final Project Contest of Data Structure and Programming Course

Seleted Projects

Range-preserving Logic Relation Determinization [Report] [Slides] *12/2018-01/2019*

- Proposed and implemented a unate-splitting based algorithm to efficiently determinize a boolean relation.
- Outperformed two baseline approaches of maxSAT and maximum clique by over 100X CPU time

LED Display Controller [Report] *12/2018-01/2019*

- Designed and implemented an LED display controller with Pulse Width Modulation technique.
- Completed hardware design from Register-Transfer-Level to Layout.

Lane Tracking System [Demo] *12/2017-01/2018*

- Designed and implemented a real-time lane tracking system integrating motors, camera, VGA and FPGA.
- Designed an optimized hardware algorithm for Sobel operator and Hough transform.

Relevent Courses

Mathematics Convex Optimization, Linear Algebra, Discrete Mathematics, Probabilities and Statistics.
Hardware System Computer-aided VLSI System Design, Digital Signal Processing in VLSI Design, Integrated Circuit Design,
Design Automation Physical Design for Nanometer ICs, Logic Synthesis and Verification, Introduction to Electronic Design Automation
Computer Science Machine Learning, The Design and Analysis of Algorithm, Data Structure and Programming

Skills

Natural Languages Mandarin (Native), Taiwanese (Native), English (Proficient), Japanese (Intermediate, JLPT N3)
Programming Languages C/C++, Python, LaTeX, Matlab, Verilog
EDA tools nWave, ncverilog, Design Compiler, Innovus, SPICE