VLSI System Design (Graduate Level)

Fall 2025

HOMEWORK I

REPORT

Must do self-checking before submission:

◻ Compress all files described in the problem into one tar

◻ All SystemVerilog files can be compiled under SoC Lab environment

◻ All port declarations comply with I/O port specifications

◻ Organize files according to File Hierarchy Requirement

◻ No any waveform files in deliverables

Student name:

Student ID:

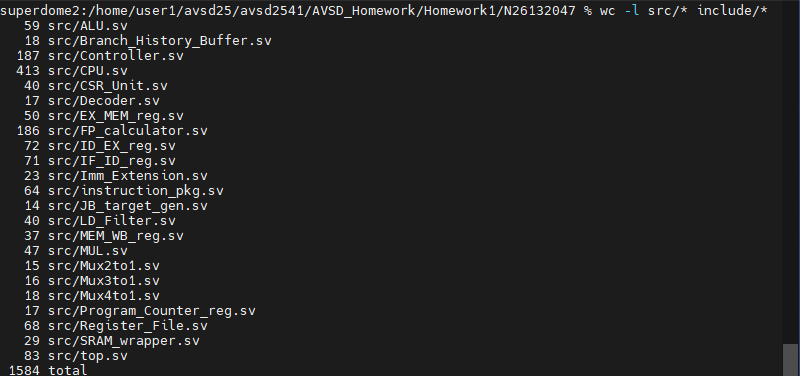
**Summary**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | | |
|  | | | | | RTL | | | synthesis |
| Top | CPU | | | |  | |  | |
| Synthesis result | | | | | | | | |
| Area | | | | Clock cycle(ns) | | | | |
|  | | | |  | | | | |
| Firmware & Software | | | | | | | | |
|  | | RTL pass | SYN pass | | | Execution time(ns) | | |
| Prog 0 | |  |  | | |  | | |
| Prog 1 | |  |  | | |  | | |
| Prog 2 | |  |  | | |  | | |
| Prog 3 | |  |  | | |  | | |
| Prog 4 | |  |  | | |  | | |
| Prog 5 | |  |  | | |  | | |
| Prog6 | |  |  | | |  | | |
| Superlint(number of inline messages) | | | | | | | | |
| Total lines | | Warning | Error | | | coverage(%) | | |
|  | |  |  | | |  | | |

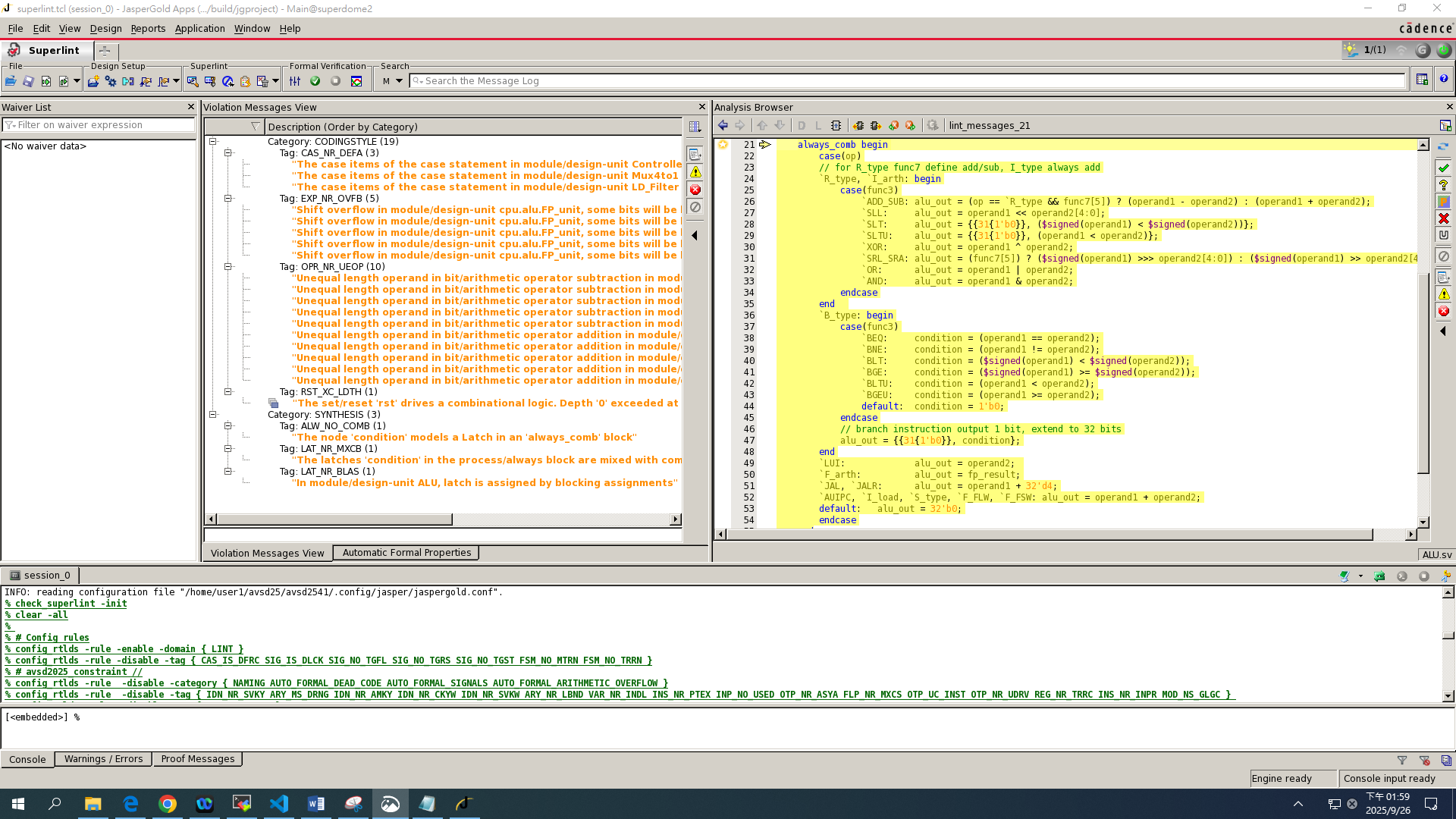
Table1. Summary of HW1

Write Your Text Summary Here:

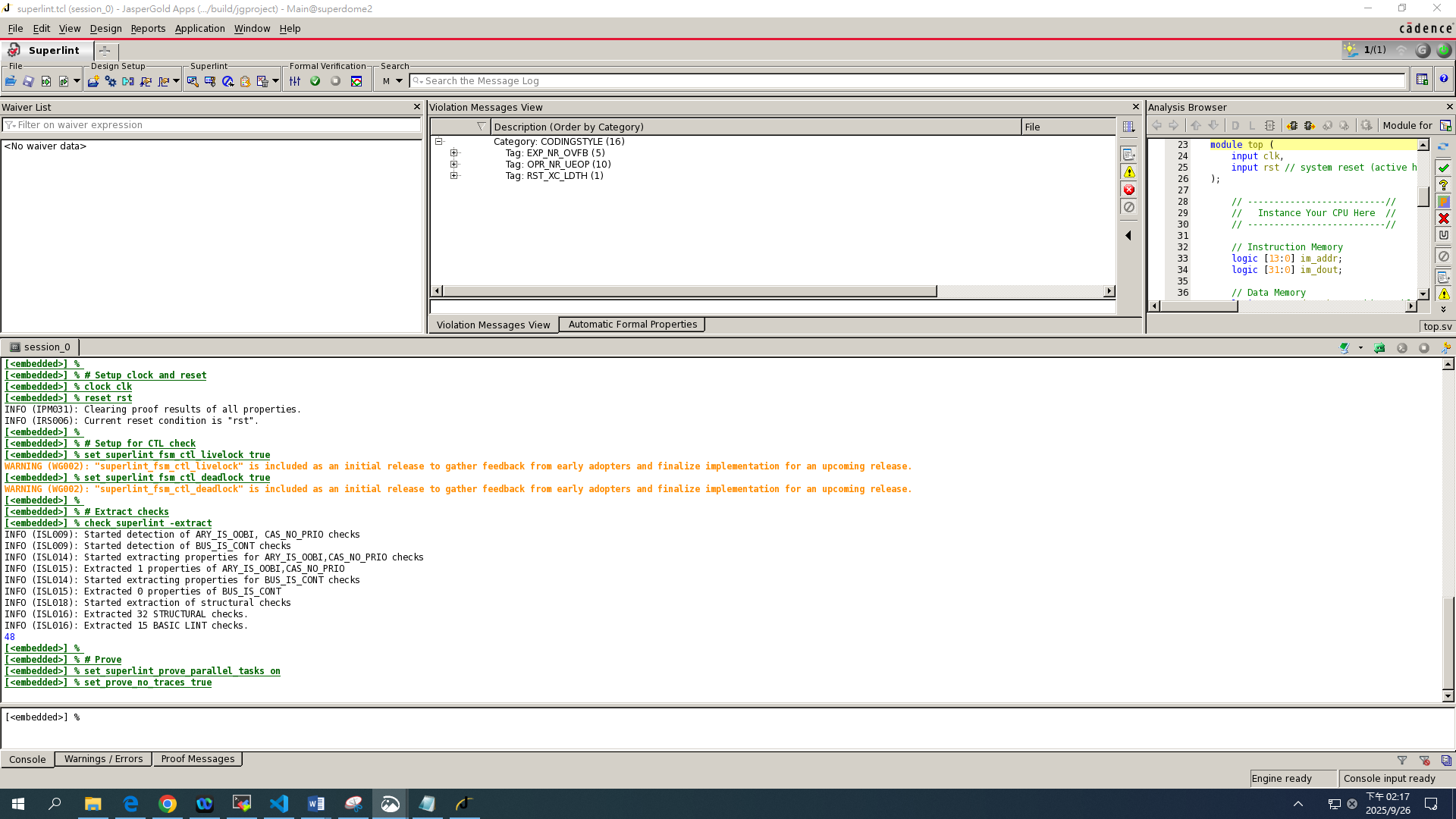
**Total line of code**



**Superlint**

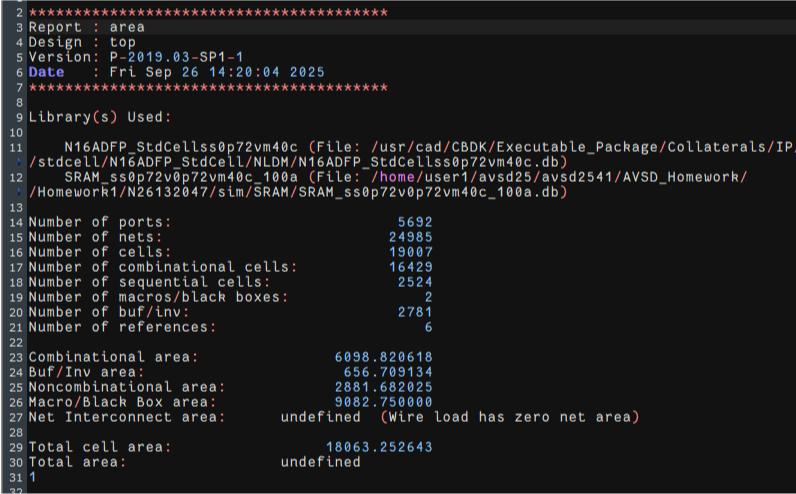
****

1. 原本我將logic condition來增加code可讀性，但出現latch->直接拿掉此變數
2. Case statement裡面我已經寫出每個case的輸出，但還是有寫default->拿掉default

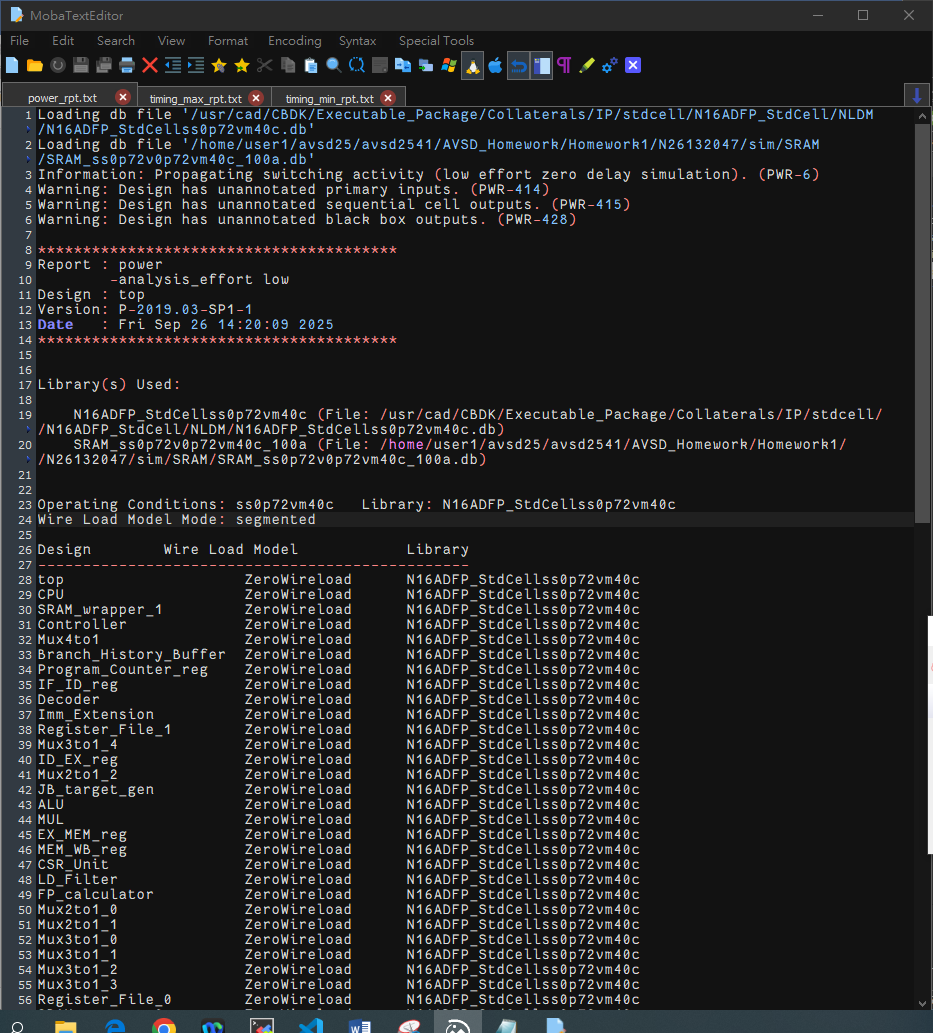


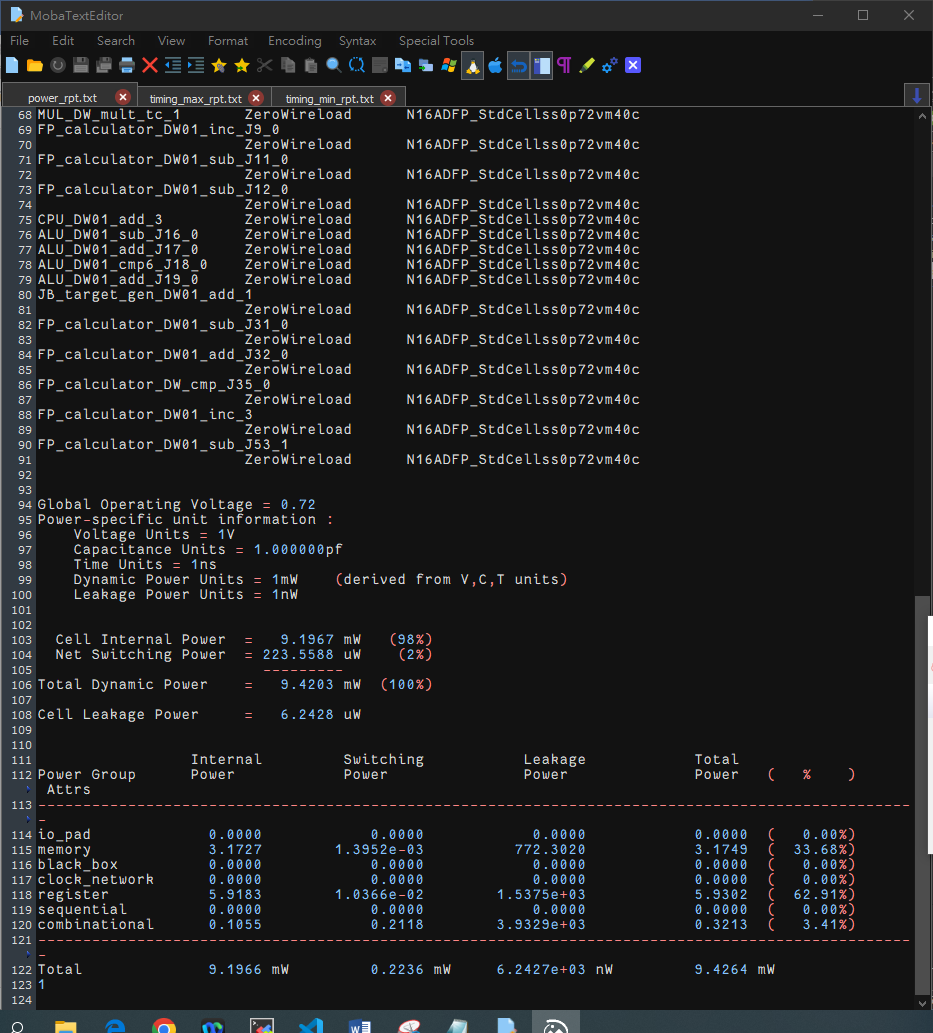
**Synthesize report**

1. Area Report



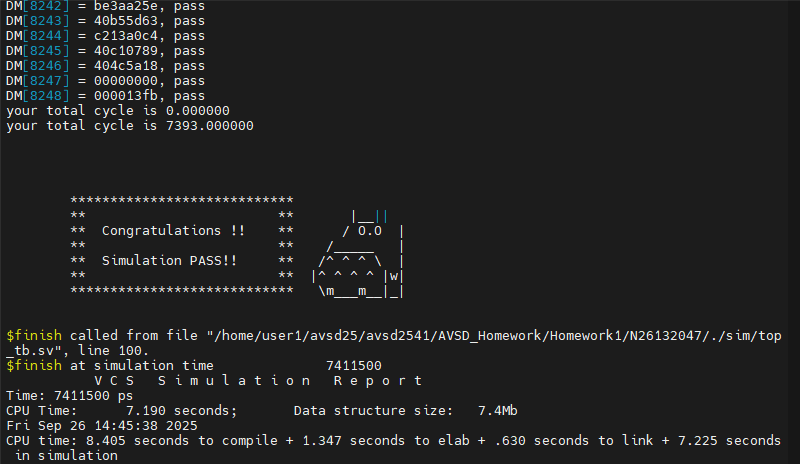
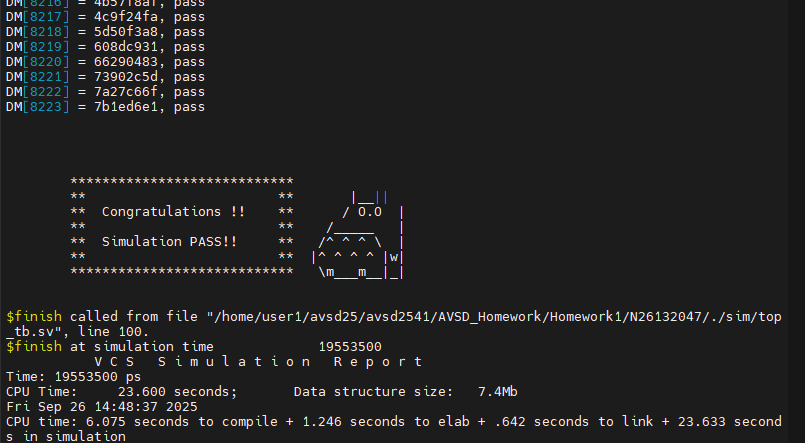
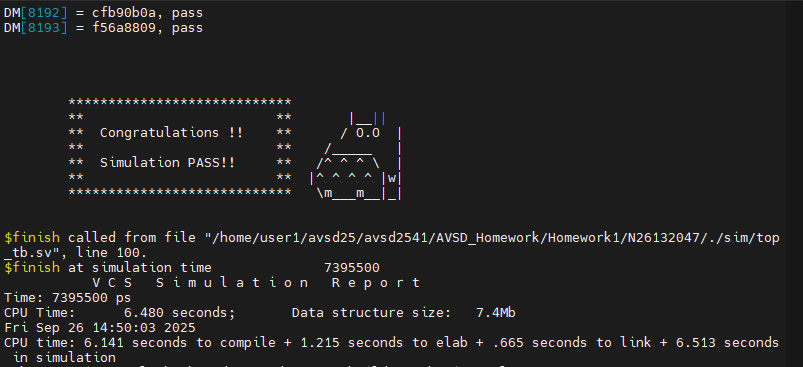
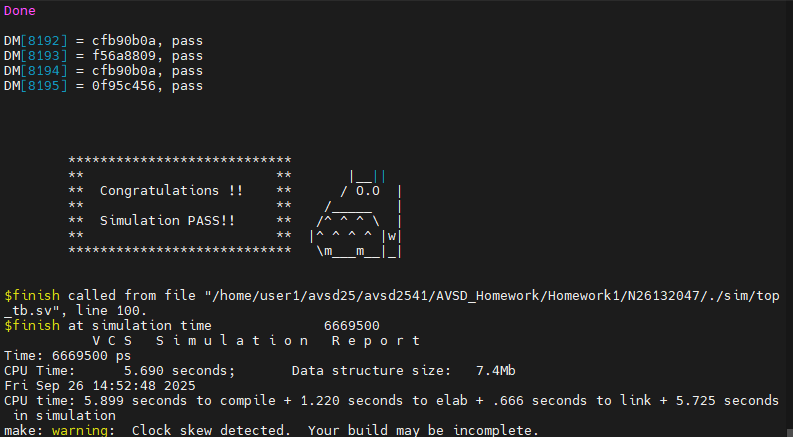
1. Power Report





1. Timing Max Report
2. Timing Min Report

**Simulation Result**

1. prog0 
2. prog1 
3. prog2 
4. prog3 
5. prog4 
6. prog5 
7. prog6 