Advanced VLSI System Design (Graduate Level)

Fall 2025

HOMEWORK II

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

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**Outline**

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* **Major Problem Encounter & Solution**
* **Future Work**
* **Lesson Learn**

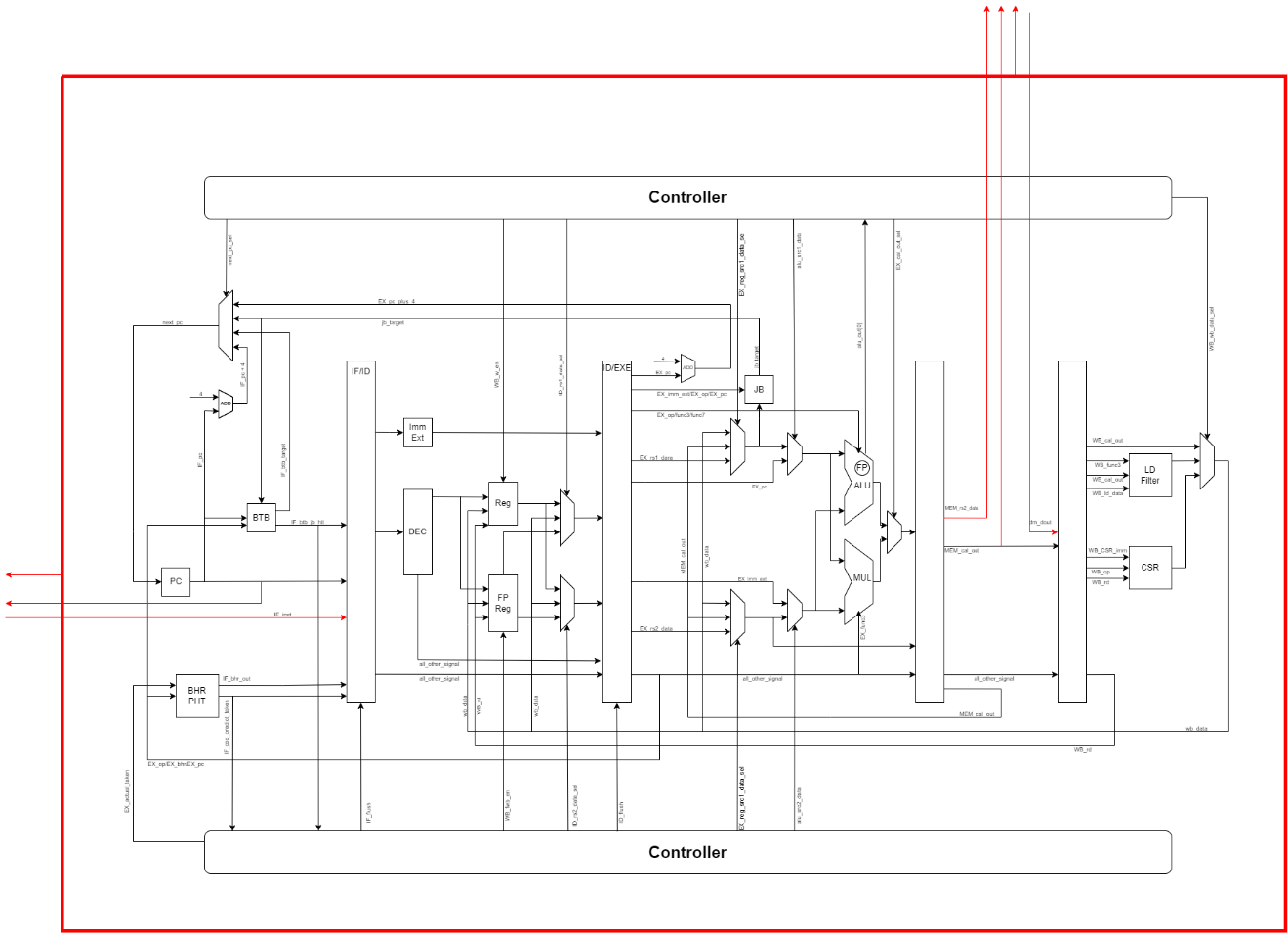
**Summary**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | | | | |
|  | | | | | | | RTL | | | synthesis |
| Top | CPU | | | | | | Pass | | Pass | |
| Synthesis result | | | | | | | | | | |
| Area | | | Clock cycle(ns) | | | | Power | | | |
|  | | |  | | | | 9.42mW | | | |
| Firmware & Software | | | | | | | | | | |
|  | | RTL pass | | SYN pass | | Execution time(ns) | | | | |
| Prog 0 | | Pass | | Pass | | 10724 | | | | |
| Prog 1 | | Pass | | Pass | | 34660 | | | | |
| Prog 2 | | Pass | | Pass | | 10473 | | | | |
| Prog 3 | | Pass | | Pass | | 11491 | | | | |
| Prog 4 | | Pass | | Pass | | 10112 | | | | |
| Prog 5 | | Pass | | Pass | | 9200 | | | | |
| Prog 6 | | Pass | | Pass | | 9135 | | | | |
| JasperGold | | | | | | | | | | |
| Master | | | Bridge | | Slave | | | | | |
| Pass | | | Pass | | Pass | | | | | |
| Superlint(number of inline messages) | | | | | | | | | | |
| Total lines | | Warning | | Error | | | | coverage(%) | | |
| 3440 | | 50 | | 0 | | | | 98.6% | | |

在本次作業中，我完成了 Master AXI, Bridge AXI 和 Slave AXI 的設計並全部通過 JasperGold 驗證，合成後也通過全部的測試程式

**Architecture-Master**

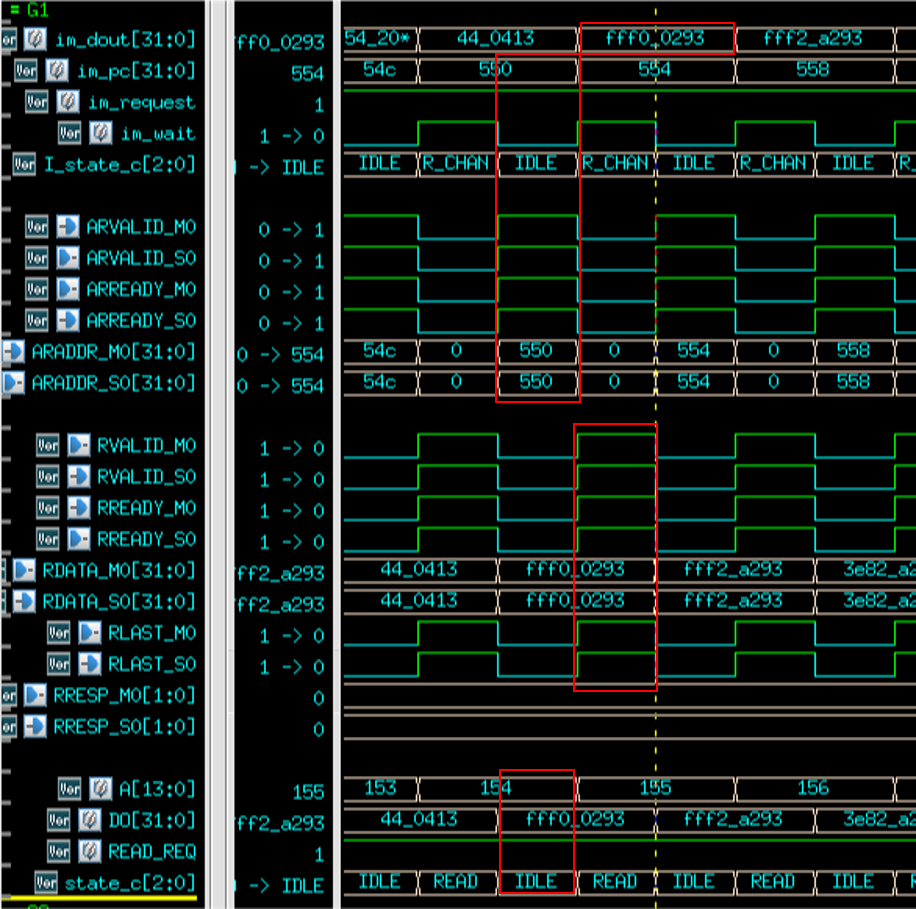
1. CPU Architecture

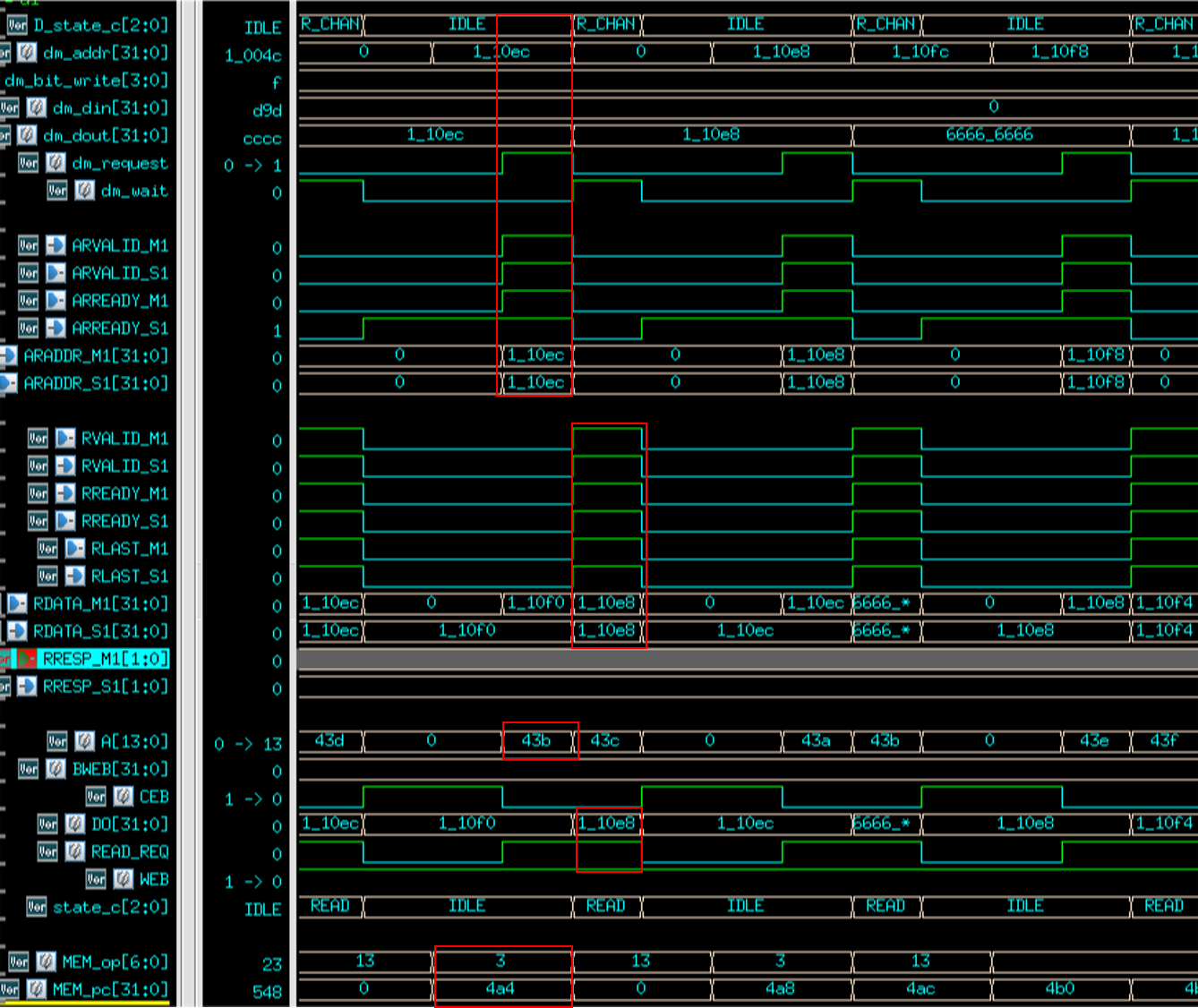


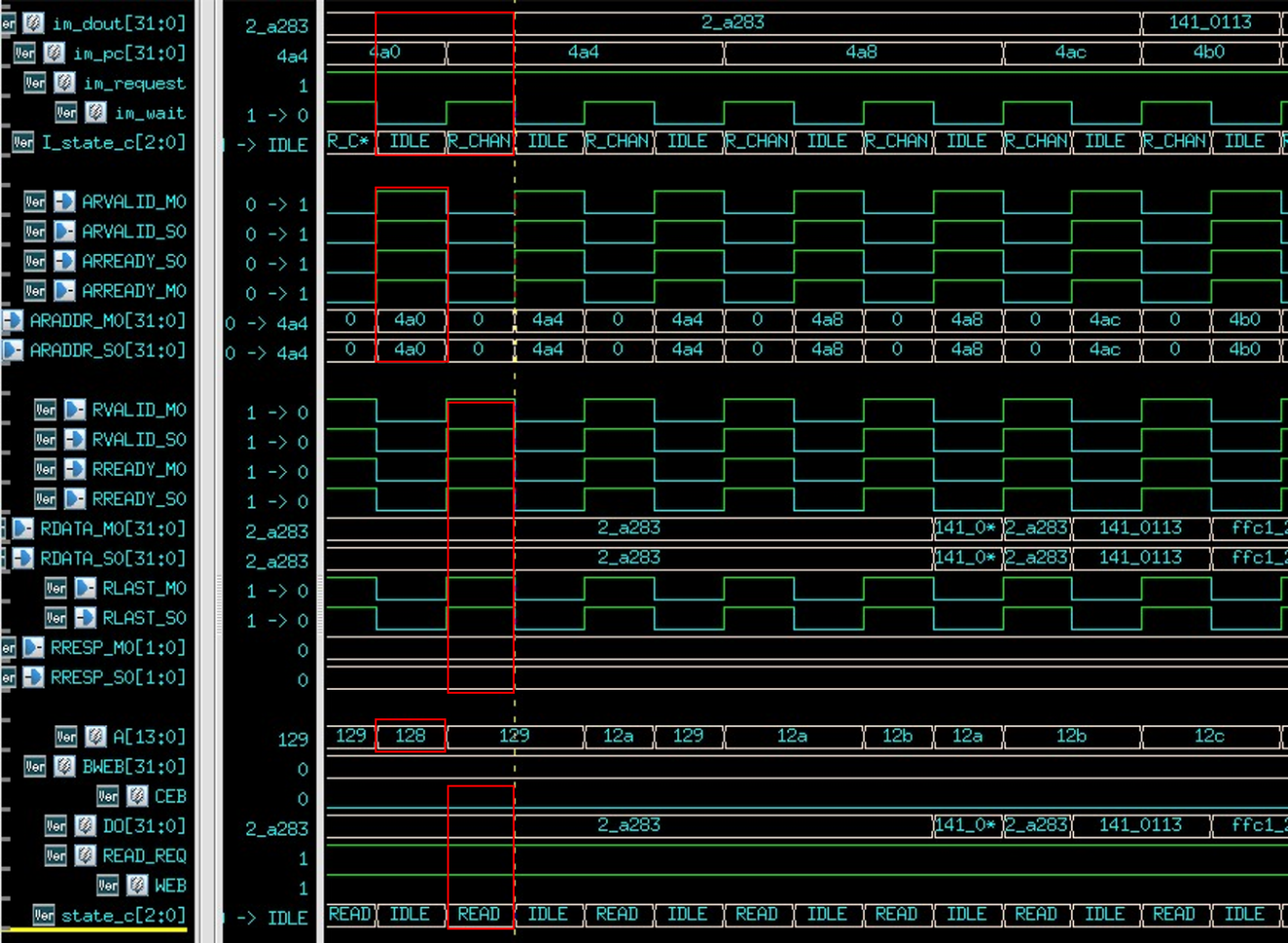
* 當CPU接上AXI後，處理指令的平均速度由原本的1指令1clock拉長到了1指令2clock，為了因應此改變，CPU的控制邏輯以及每個pipeline register都有小幅度的更動。

**Simulation Waveform**

1. M0-S0 read

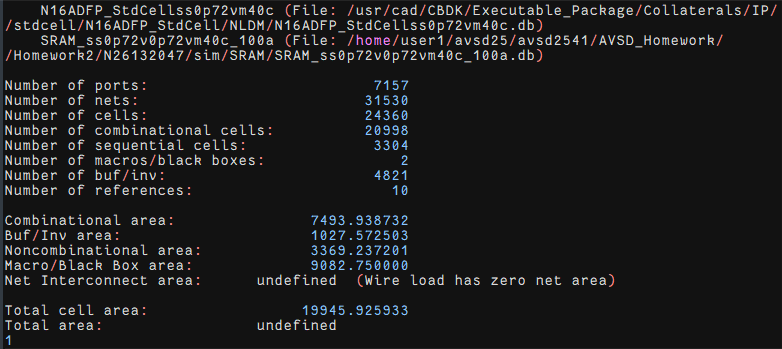


1. M1-S1 read
2. M1-S1 write

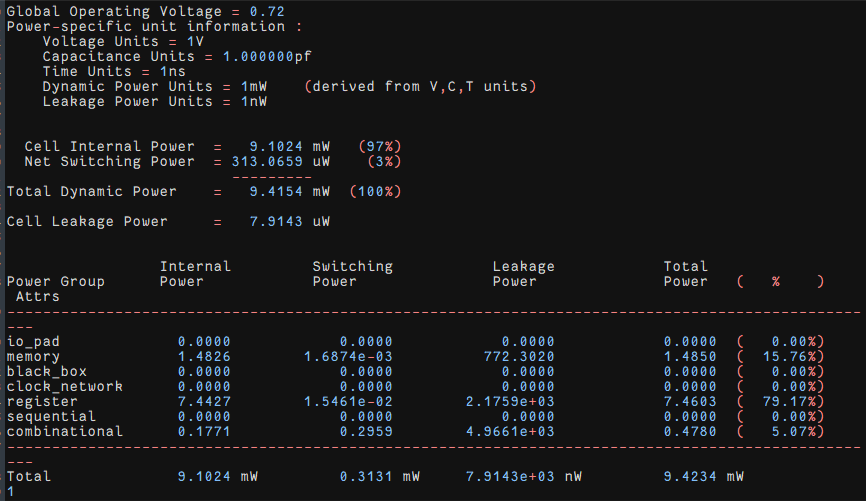


**Synthesize Report**

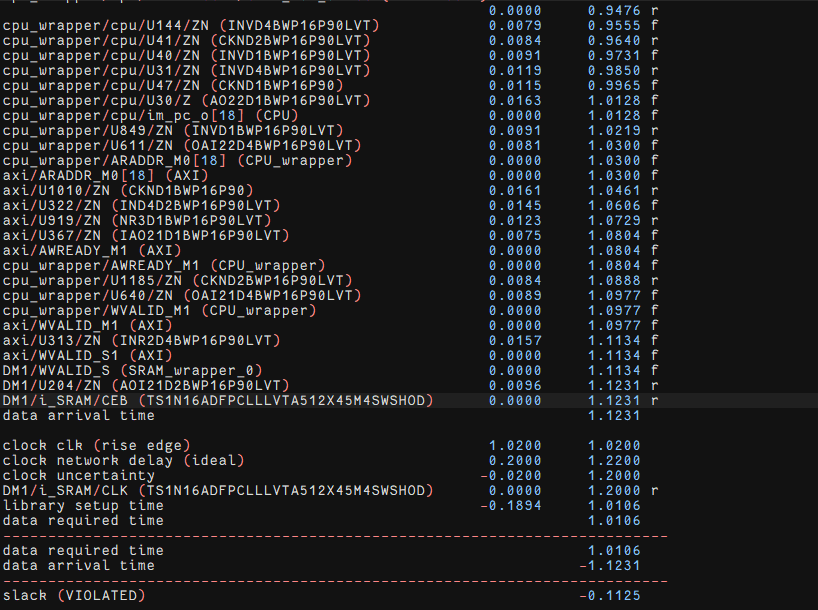
1. **Area Report**

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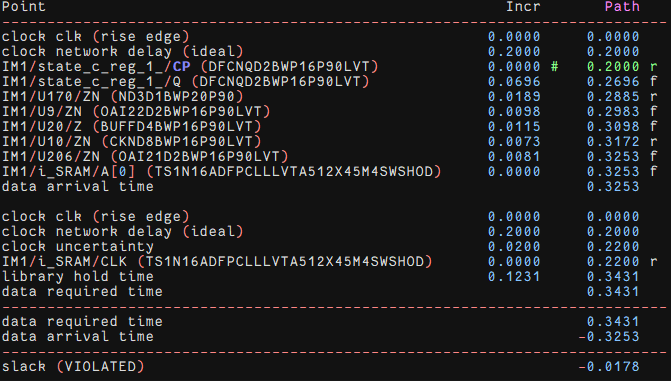
1. Power Report



1. Timing Max Report



1. Timing Min Report



**Simulation Result Screenshots**

|  |  |
| --- | --- |
| rtl0 | syn0 |
| rtl1 | syn1 |
| rtl2 | syn2 |
| rtl3 | syn3 |
| rtl4 | syn4 |
| rtl5 | syn5 |
| rtl6 | syn6 |