Advanced VLSI System Design (Graduate Level)

Fall 2025

HOMEWORK II

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

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**Outline**

* **Summary**
* **Architecture** 
  + **Master**
  + **AXI**
  + **Slave**
* **Simulation Waveform**
  + **Master**
  + **AXI**
  + **Slave**
* **JasperGold Screenshots**
  + **Master**
  + **AXI**
  + **Slave**
* **Synthesize Report**
  + **Area Report**
  + **Power Report**
  + **Max Timing Report**
  + **Min Timing Report**
* **Simulation Result Screenshots**
* **Major Problem Encounter & Solution**
* **Future Work**
* **Lesson Learn**

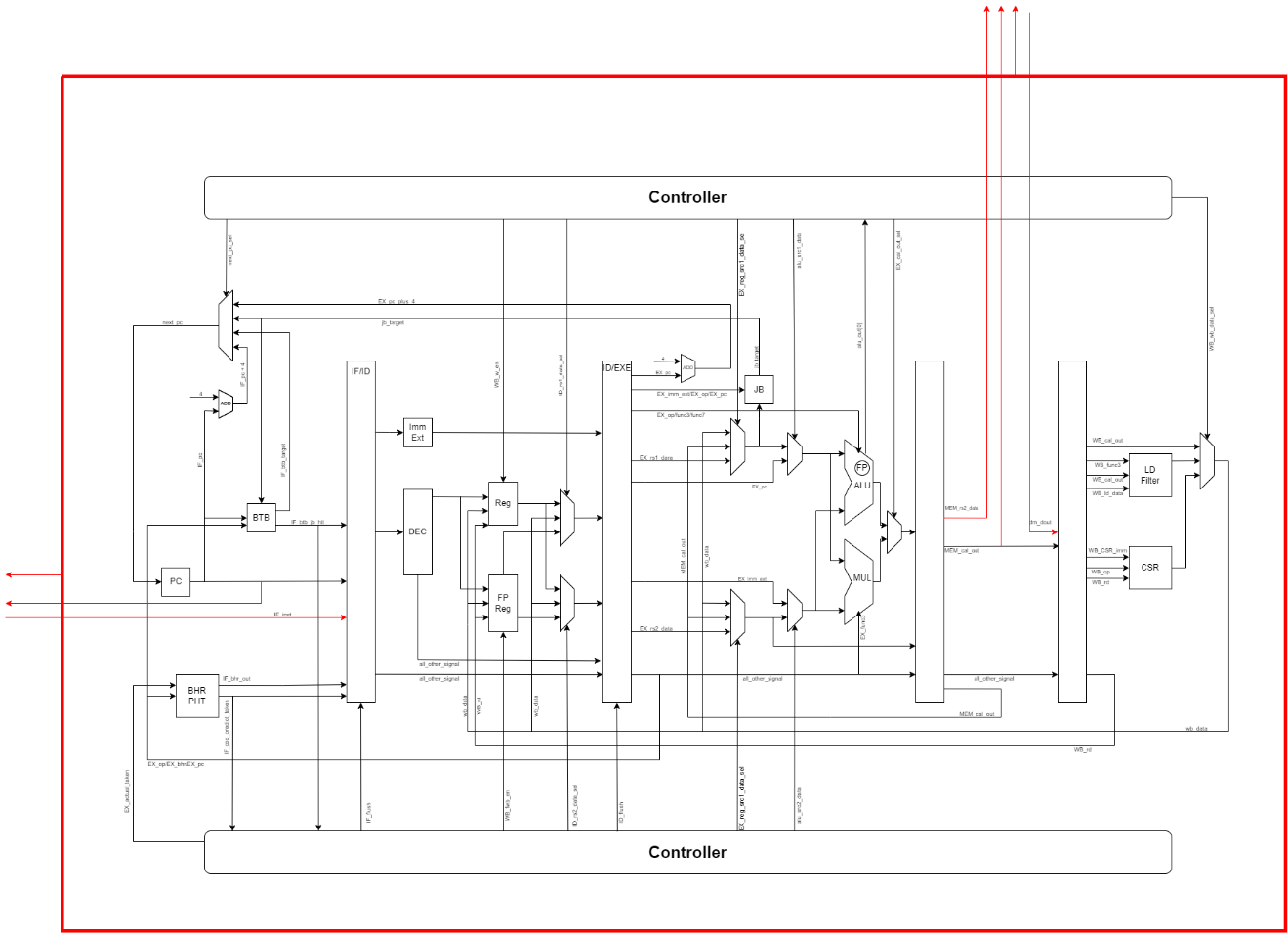
**Summary**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | | | | | |
|  | | | | | | | | RTL | | | synthesis |
| Top | CPU | | | | | | | Pass | | Pass | |
| Synthesis result | | | | | | | | | | | |
| Area | | | | | Clock cycle(ns) | | | | | | |
|  | | | | |  | | | | | | |
| Firmware & Software | | | | | | | | | | | |
|  | | RTL pass | | SYN pass | | | Execution time(ns) | | | | |
| Prog 0 | | Pass | | Pass | | |  | | | | |
| Prog 1 | | Pass | | Pass | | |  | | | | |
| Prog 2 | | Pass | | Pass | | |  | | | | |
| Prog 3 | | Pass | | Pass | | |  | | | | |
| Prog 4 | | Pass | | Pass | | |  | | | | |
| Prog 5 | | Pass | | Pass | | |  | | | | |
| Prog6 | | Pass | | Pass | | |  | | | | |
| JasperGold | | | | | | | | | | | |
| Master | | | Bridge | | | Slave | | | | | |
| Pass | | | Pass | | | Pass | | | | | |
| Superlint(number of inline messages) | | | | | | | | | | | |
| Total lines | | Warning | | Error | | | | | coverage(%) | | |
|  | |  | |  | | | | |  | | |

在本次作業中，我完成了 Master AXI, Bridge AXI 和 Slave AXI 的設計並全部通過 JasperGold 驗證，合成後也通過全部的測試程式

**Architecture-Master**

1. CPU Architecture



* 當CPU接上AXI後，處理指令的平均速度由原本的1指令1clock拉長到了1指令2clock，為了因應此改變，CPU的控制邏輯以及每個pipeline register都有小幅度的更動。