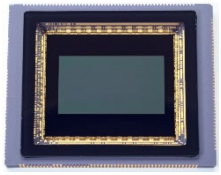
MST4625A / LTN4625A Datasheet

12 Megapixel sCMOS2.0™ Image Sensors



PRODUCT DESCRIPTION

The RGB color Maestro 4625A (MST4625A) and monochrome Lightning 4625A (LTN4625A) offer outstanding performance and features for professional video, machine vision, high-end security/surveillance and scientific applications.

FEATURES

- **12 Megapixel (4608 H x 2592 V) sCMOS2.0 Image Sensor**
- **Optical format**
  - APS-C (29mm diagonal)
- **Pixel Size:**
  - 5.5 µm x 5.5 µm
- **Frame rates**
  - 240 fps Rolling Shutter mode, 120 fps Global Shutter mode
- **Global reset mode**
- **Dual channel low/high gain architecture with data blending**
  - 2 x 11 bit ADCs blended for true 16 bit/pixel output
- **Ultra-low-light imaging**
  - < 1.5 e- noise RMS (Rolling Shutter)
- **Flexible windowing for higher frame rates**
  - Programmable ROI readout
- **Low dark current**
  - < 10 e-/pixel/second dark current @ 25°C
- **High sensitivity**
  - ≥ 45% peak RGB quantum efficiency, ≥ 60% peak monochrome quantum efficiency (QE)
- **High dynamic range**
  - > 88 dB intra-scene dynamic range
- **High speed serial SERDES interface**

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Table of Contents

List of Figures

List of Tables

1 Acronyms and General Features

1.1 Acronyms

5T	5 Transistor (i.e. our pixel design has 5 transistors on each pixel)
ADC	Analog-to-Digital Converter
BIST	Built-In Self-Test
CDS	Correlated Double Sampling
C_{fd}	Capacitance of the floating diffusion (also called the floating diffusion node), the place on the pixel where signal charge is stored for measurement
CLCC	Ceramic Leadless Chip Carrier (our package type)
DAC	Digital-to-Analog Converter
DCC	Duty Cycle Corrector
DN	Digital Number (the output of the sensor, which is the digitization of the pixel signal level)
e-	Electrons
EQ SPCD	“Equally Spaced”
ESD	Electro Static Discharge
FD	Floating Diffusion
FPGA	Field Programmable Gate Array
fps	Frames per second
FWC	Full Well Capacity (sometimes shortened to “fw” for “full well”)
Gbps	Gigabits per second
GS	Global Shutter
HG	High Gain
HROI	Region of Interest in the Horizontal direction
HSTL	High Speed Transceiver Logic specification, EIA/JESD8-6
IO	Input / Output
JTAG	Boundary Scan based on IEEE1149.1 Specification, formerly known as Joint Test Action Group (JTAG) Specification
LG	Low Gain
LSB	Least Significant Bit
LVCMOS	Low Voltage CMOS Logic compatible to JESD8-7A Specification
MAC	Medium Access Control sublayer, part of the data link layer in the Open Systems Interconnection (OSI) model
Mbps	Megabits per second
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
MTF	Modulation Transfer Function
PD	Photo-Diode

PEK	Product Evaluation Kit, a Fairchild-supplied camera system for evaluating the MST4625A or LTN4625A
PHY	Physical Layer of the Open Systems Interconnection (OSI) model
PLL	Phase Locked Loop
PRBS	Pseudo Random Binary Sequence
PRNU	Photo-Response Non-Uniformity
QE	Quantum Efficiency
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances
ROI	Region of Interest
RS	Rolling Shutter
SERDES	SERializer / DESerializer, a pair of circuit blocks for high speed data communications
SPI	Serial Peripheral Interface
TX	High speed Serializer (transmitter) operating higher than 1 giga-bit-per-second rate
VPTAT	Voltage Proportional To Absolute Temperature
VROI	Region of Interest in the vertical direction
XAUI	10 gigabit Attachment Unit Interface from IEEE803-3ae 10G Ethernet Specification (our proprietary Serdes protocol is similar to this standard)

Note: Not all of these acronyms are used in this datasheet, but they may be used in Application Notes or other technical communications relating to this product.

1.2 General Features

- 5T pixel
- Readable array size (including dark and transition): 4664 columns by 2652 rows
- Readable active array size: (excluding dark but including transition): 4640 columns by 2624 rows
- Main imaging array size: (excluding dark and transition): 4608 columns by 2592 rows
- Both Rolling Shutter and Global Shutter supported
- Simultaneous quad row readout (4 rows)
- 32 TX lanes, each operating at 3.125 Gbps
- Maximum 240 frames per second with full resolution with all 32 TX lanes
- Number of TX lanes scalable with frame rate:

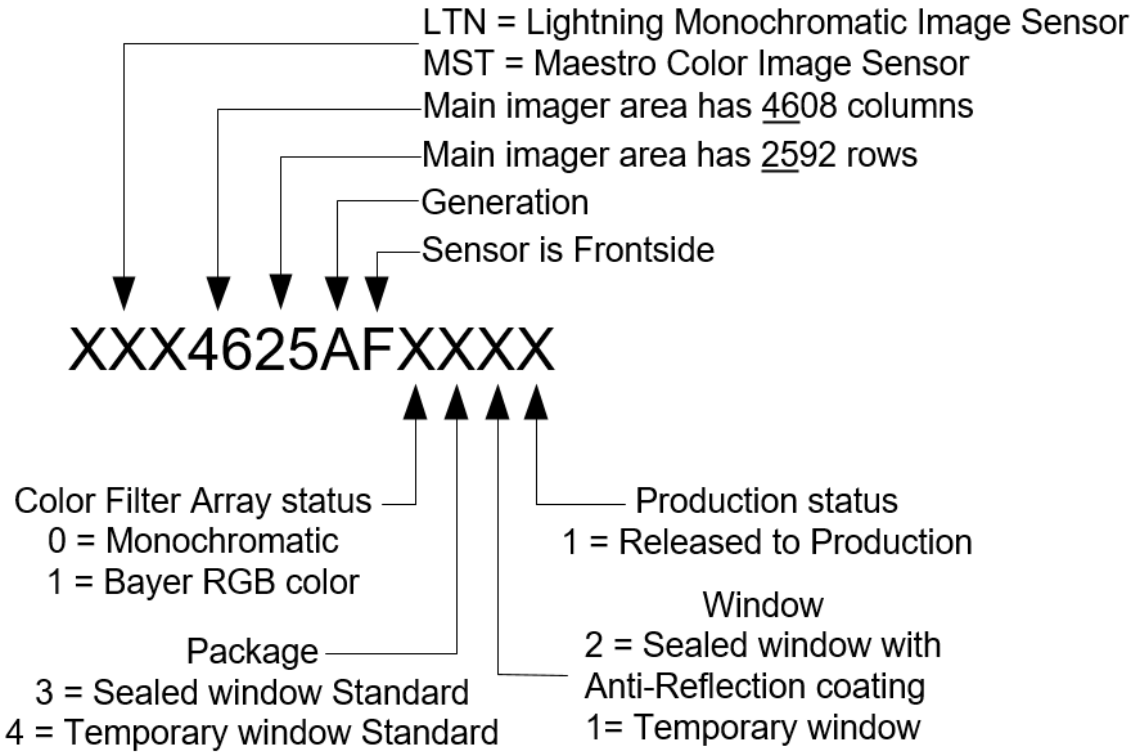
240fps:	32 TX lanes
180fps:	24 TX lanes
120fps:	16 TX lanes
60fps	8 TX lanes
30fps	4 TX lanes

- 3 rolling shutter external trigger modes; 1 global shutter external trigger mode
- SPI programming interface
- IEEE 1149.1 JTAG boundary scan for digital IO
- Full internal scan
- BIST for custom logic
- 3 Vertical Regions of Interest plus programmable virtual rows
- No Horizontal Region of Interest but column right edge cropping is supported
- Support for column circuit correction with injection DAC

1.3 Part Numbering and Available Parts

Table 1: Ordering Part Number

Part Number	Description
LTN4625AF0321	Monochrome, Standard Package, Sealed Window
LTN4625AF0411	Monochrome, Standard Package, Temporary Window
MST4625AF1321	Color Filter, Standard Package, Sealed Window
MST4625AF1411	Color Filter, Standard Package, Temporary Window



2 Electro-Optical Features and General Specifications

2.1 General Specifications

Table 2 contains typical values of general parameters for the MST4625A and LTN4625A image sensors.

Table 2: Parameters and Typical Values

Parameter	Typical value
Active array size	4608 horizontal (H) x 2592 vertical (V), main imager area 4664 horizontal (H) x 2652 vertical (V), all readable pixels (including dark and transition)
Pixel size	5.5 µm x 5.5 µm
Dimensions of active area	25344 microns (H) x 14256 microns (V), main imager area 25652 microns (H) x 14586 microns (V), all readable pixels
Dimensions of die	31210 microns (H) x 25640 microns (V), die circuit only 31250 microns (H) x 25680 microns (V), including seal ring 30670 microns (H) x 25800 microns (V), including saw street (estimate)
Distance between main imaging array optical center and die center	Optical center is 363.46 microns to the right of the die center
Distance between main imaging array optical center and package center	Optical center is 363.46 microns to the right of the package center and 14.3 microns above package center
Shutter type	Rolling Shutter, Global Reset, and Global Shutter (snapshot). ROI readout capabilities for all shutter types.
Maximum frame rate	240 fps (Rolling Shutter) 120 fps (Global Shutter)
Number of readout ports	32 TX lanes grouped in 4 groups of 8 (A0…A7, B0…B7, C0…C7, D0…D7) Each TX lane has 2 pins, one “p” and one “n” for the positive and negative signals of the differential voltage transmission
Minimum line time	6.304 µsec = [(1970 sys_clks per line)/(312.5 MHz sys_clk frequency)]
ADC resolution	2 x 11-bit

Parameter	Typical value
Column level amplifier gain	1x (Low gain output) 15x or 30x (High gain output)
Power consumption	< 6.5 W at Full-Frame 240 fps (full 22 bit data output)
I/O interface	1.8V LVCMOS and 1.8V HSTL
Package type	194 pin CLCC (for Standard package)
Temperature	-40 ºC to +55 ºC (operating, temp measured at junction) -40 ºC to +80 ºC (non-operating)

2.1.1 General part layout

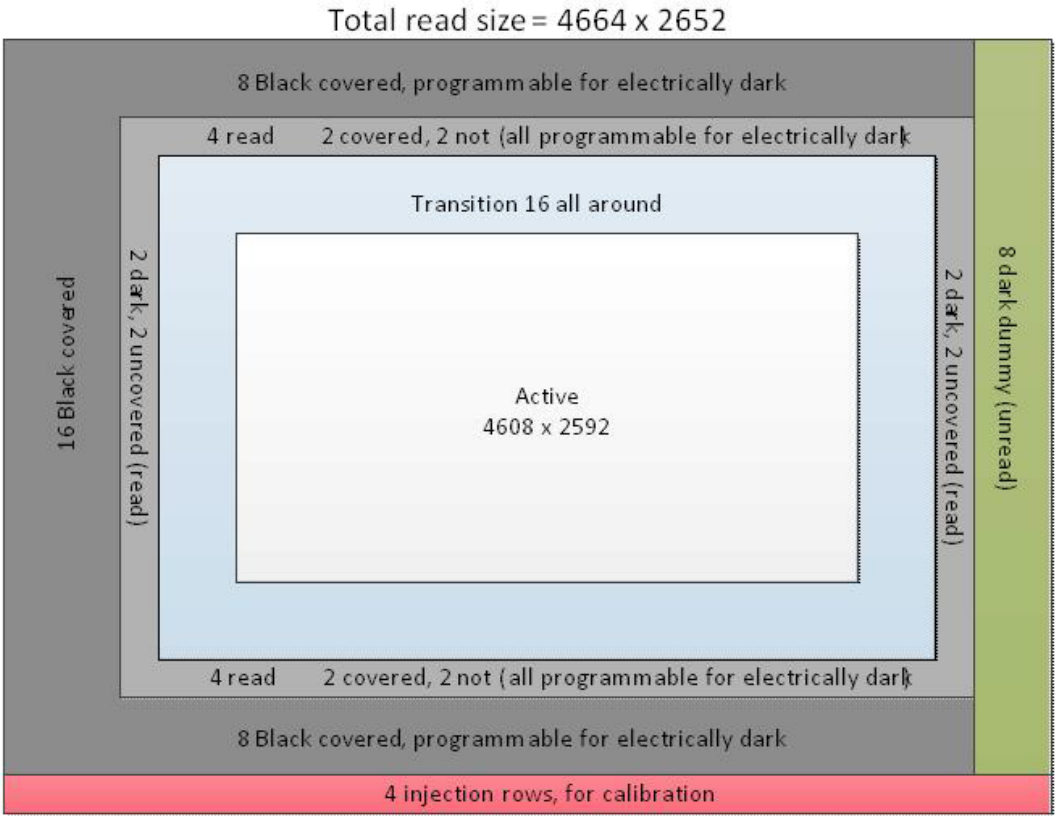


Figure 1. General sensor layout

Rows are numbered 0 to 2651 with Row 0 being on the top edge and Row 2651 being on the bottom edge. Columns are numbered 0 to 4663 with Column 0 being on the left side and Column 4663 being on the right side. Note that because the sensor is hardwired to read out 4 rows simultaneously, rows are grouped into 663 “Quad rows” numbered 0 to 662.

2.2 Electro-optical specifications

Table 3 contains the electrical-optical parameters and specifications for the MST4625A and LTN4625A image sensors.

Table 3: Electro-optical specifications

Parameter	Specification	Notes
Conversion gain	1.53 DN/e- for 30x HG 0.051 DN/e- for 1x LG	typical, not guaranteed
Intra-frame dynamic range	25000:1	14 stops (88 dB)
PRNU	< 3% RMS	at 75% of max output
Dark current	< 10 e-/pixel/sec	at 25ºC
Full well capacity (FWC)	≥ 40,000 e-	
Lag	< 1.5 e-	of maximum output
Non-linearity	< 1%	
Peak QE	≥ 45% for color sensor ≥ 60% for mono sensor	
Temporal read noise	< 1.5 e- RMS @ 6.3 µsec line readout time (Rolling Shutter), @T=30ºC	Median value of read noise distribution from high gain output (30x gain)
MTF	≥ 40%	

Note: The above specifications are from MST4625A and LTN4625A devices running in Rolling Shutter mode. Although the MST4625A and LTN4625A can run in Global Shutter mode, BAE does not guarantee any performance specifications for Global Shutter mode. Consult with Applications Engineering.

2.2.1 Monochromatic part layout

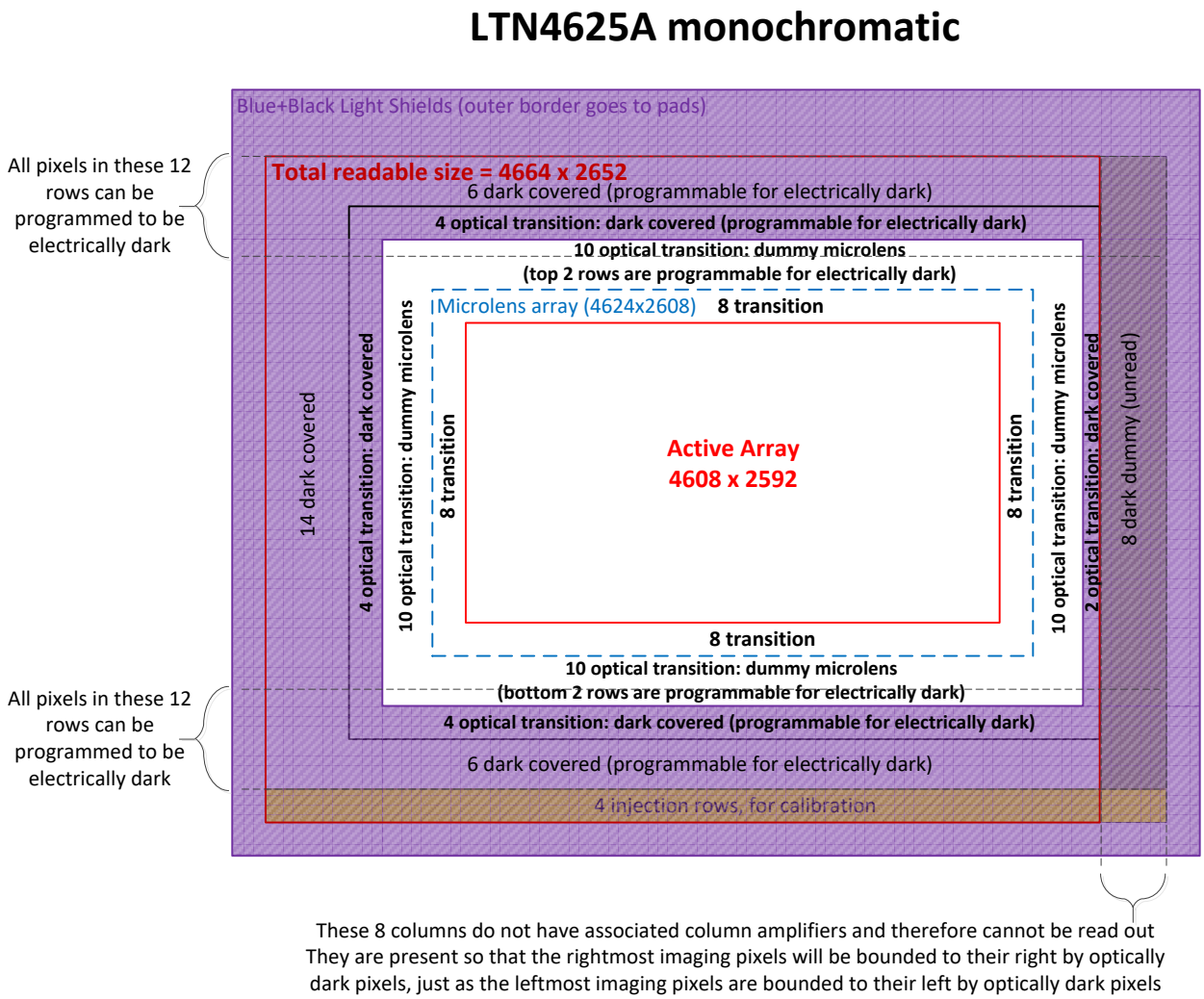


Figure 2. Monochromatic sensor layout

2.2.2 Monochromatic part Quantum Efficiency vs Wavelength

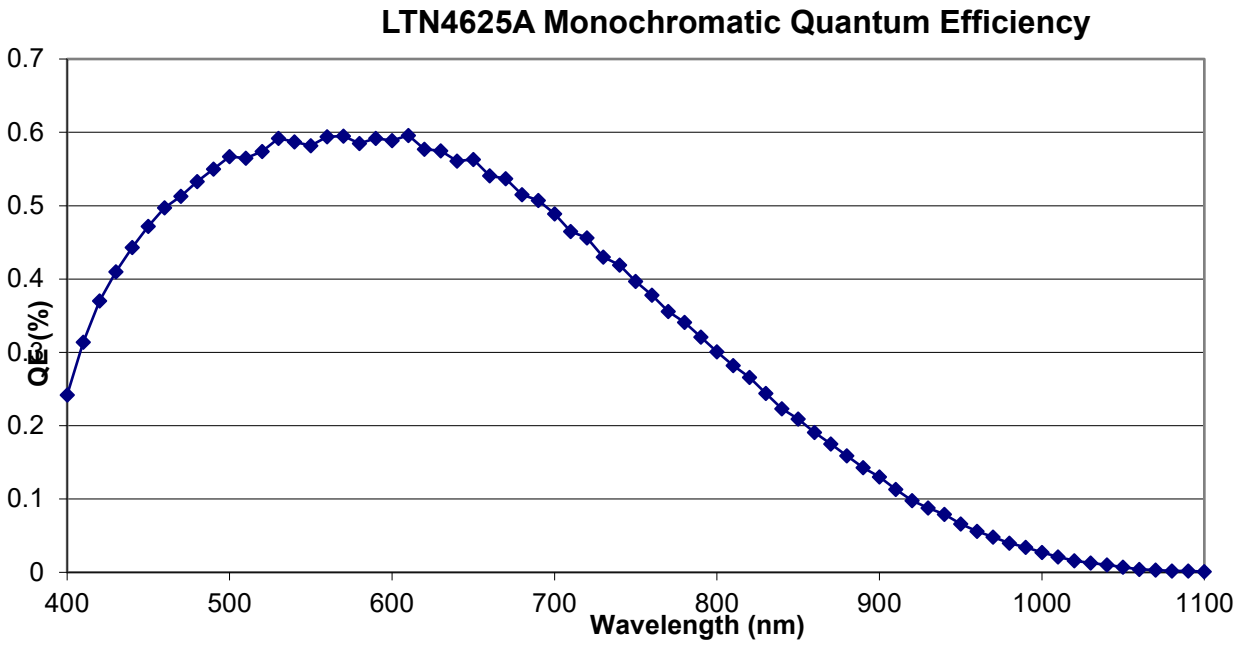


Figure 3. Monochromatic QE response

2.2.3 Color part layout

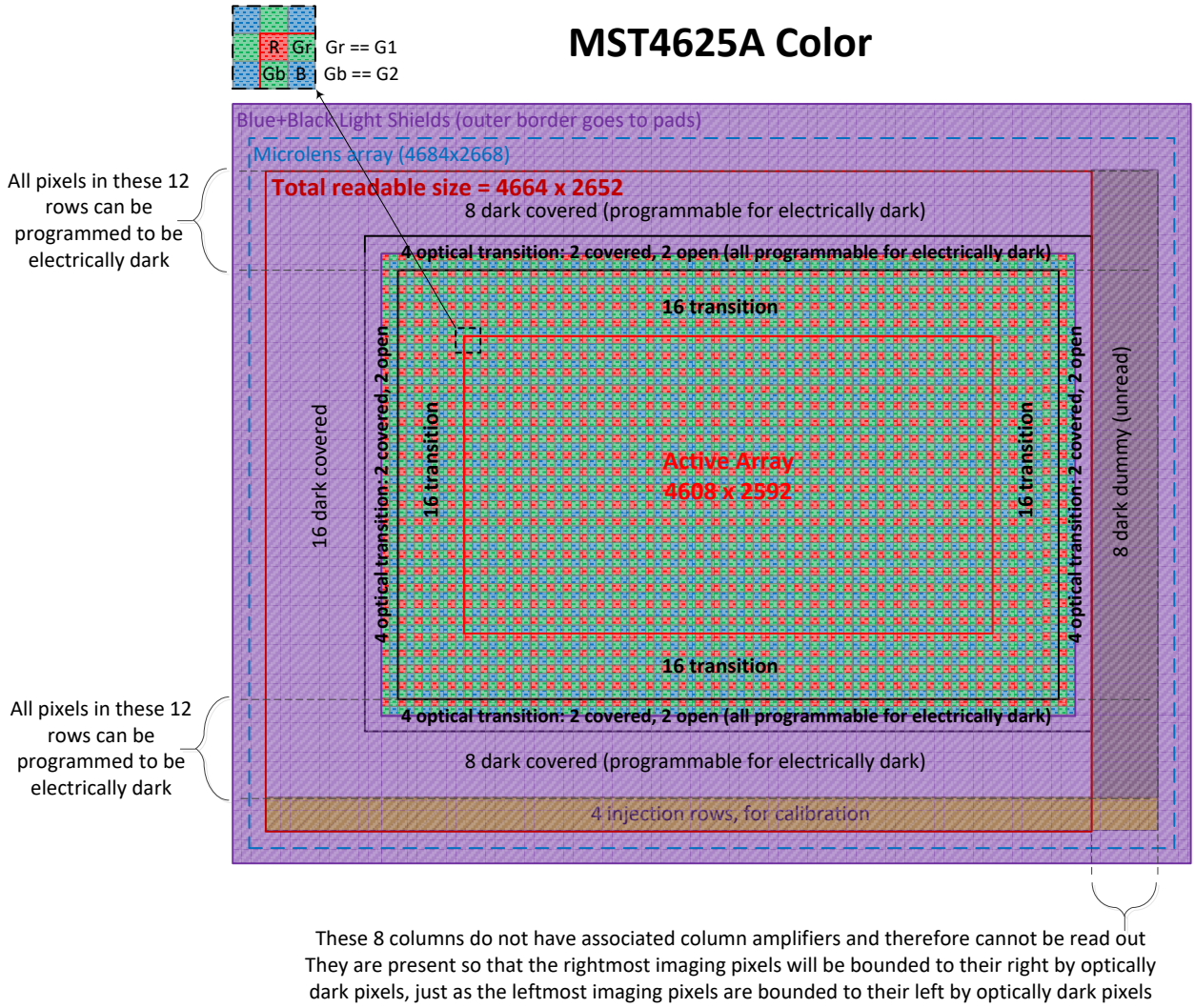


Figure 4. Color sensor layout

The total readable pixel array is 2652 rows by 4664 columns.

Zero based numbering is used, so the rows number from 0 to 2651 (top to bottom) and the columns number from 0 to 4663 (left to right).

The RGB color filter array covers a rectangular area covering rows 10 to 2637 (inclusive) and columns 18 to 4661 (inclusive).

A pixel's RGB status can be determined by whether the row is odd/even and whether the column is odd/even as described in Table 4.

Table 4: Color filter array RGB assignment

If the row number is	And the column is	Then the pixel is
Even	Even	Red
Even	Odd	Green (G1)
Odd	Even	Green (G2)
Odd	Odd	Blue

For example, the upper left pixel of the 4608 x 2592 active imaging area is Row 28 column 36, both even, and so the pixel is red.

2.2.4 Color part Quantum Efficiency vs Wavelength

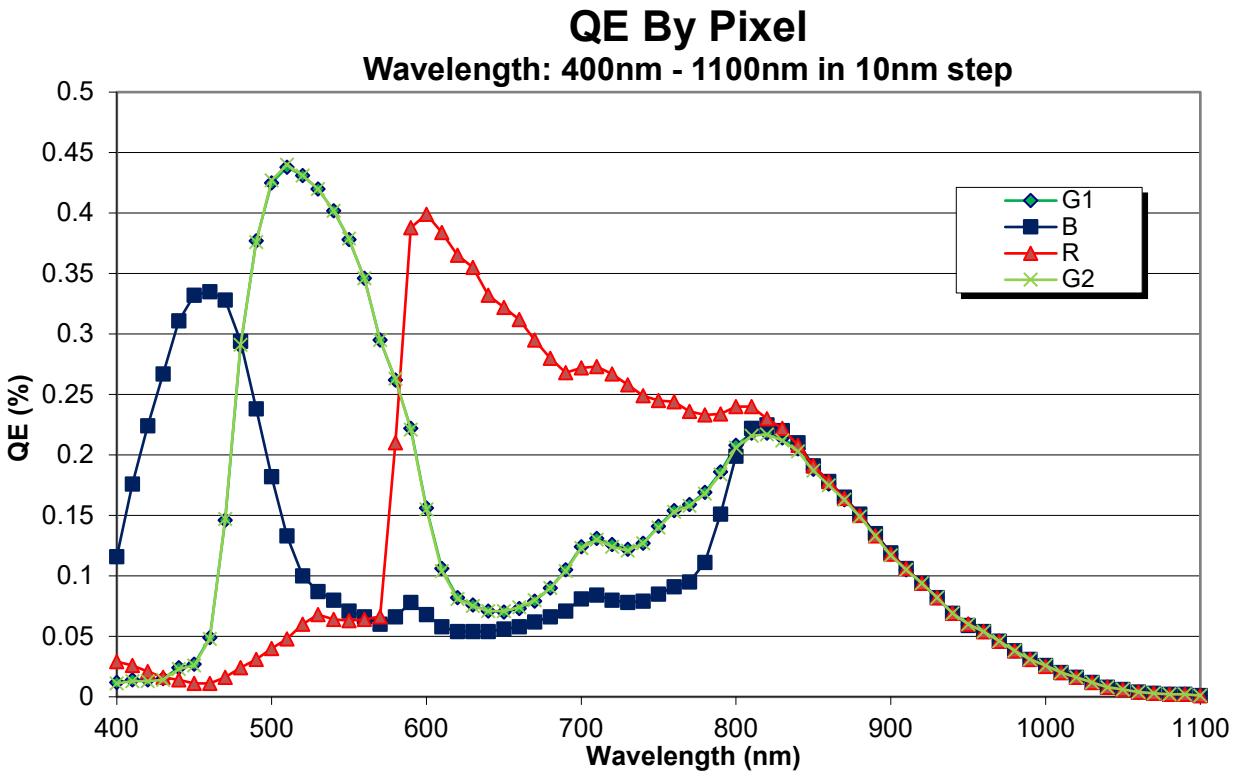


Figure 5. Color QE response

3 Electrical Specifications

3.1 DC Specifications

3.1.1 Power Inputs

Table 5: Power Input Parameters, Part 1

Pin name	Pin description	Nominal Voltage RS	Nominal Voltage GS	Adjustable Range for Voltage Regulator	Adjustment Resolution for Voltage Regulator
AVDD	AVDD analog supply	3.25	3.25	Not Applicable	Not Applicable
AVDD_PIX	Pixel source follower supply	3.6	3.6	3.0 V to 3.6 V	< 100 mV
DVDD	DVDD digital core supply	1.8	1.8	Not Applicable	Not Applicable
VDD_1V2	SERDES driver power supply	1.2	1.2	0.5 V to 1.8 V	< 50 mV
VDDM	Shift/Mux power supply	1.8	1.8	0.5 V to 2.0 V	< 100 mV
VRESET1	Primary pixel reset drain power supply	3.3	2.58	2.0 V to 3.6 V	< 1 mV
VRESET2	Secondary pixel reset drain power	3.3	2.80	2.0 V to 3.6 V	< 1 mV
VROW_POS	Row select driver positive supply	3.5	3.5	2.0 V to 3.6 V	< 50 mV
VRST_POS	Pixel reset gate driver power supply	3.5	3.5	2.0 V to 3.6 V	< 50 mV
VTX1_POS	TX1 positive supply	3.6 if 240 fps, else 3.3	3.6 if 240 fps, else 3.3	2.0 V to 3.6 V	< 50 mV
VTX1_NEG	TX1 negative supply	-0.4	+0.5	-1.0 V to +1.0 V	< 50 mV
VTX2_POS	TX2 positive supply	2.2	3.3	2.0 V to 3.6 V	< 50 mV
VTX2_NEG	TX2 negative supply	-0.4	+0.3	-1.0 V to +1.0 V	< 50 mV

Note 1: The absolute maximum that may be applied to any pin is 3.3 V + 10%, which is 3.63 V

Table 6: Power Input Parameters, Part 2

Pin name	Pin description	Suggested Regulator Architecture	Typical Current Draw for RS 240 fps (Average)	Required Power Rail Noise/Ripple
AVDD	AVDD analog supply	Low Noise LDO	870 mA	100 µV rms
AVDD_PIX	Pixel source follower supply	Low Noise LDO	110 mA	30 µV rms
DVDD	DVDD digital core supply	LDO (or DC/DC with LC filter)	1150 mA	5 mV pp
VDD_1V2	SERDES driver power supply	LDO	220 mA	5 mV pp
VDDM	Shift/Mux power supply	LDO (or DC/DC with LC filter)	310 mA	5 mV pp
VRESET1	Primary pixel reset drain power supply	Low Noise Op Amp	0.040 mA	30 µV rms
VRESET2	Secondary pixel reset drain power	Low Noise Op Amp	0.9 mA	30 µV rms
VROW_POS	Row select driver positive supply	Low Noise Op Amp	0.013 mA	30 µV rms
VRST_POS	Pixel reset gate driver power supply	Low Noise Op Amp	0.7 mA	30 µV rms
VTX1_POS	TX1 positive supply	Low Noise LDO	3.2 mA	15 µV rms
VTX1_NEG	TX1 negative supply	Low Noise LDO	2.0 mA	15 µV rms
VTX2_POS	TX2 positive supply	Low Noise LDO	3.7 mA	15 µV rms
VTX2_NEG	TX2 negative supply	Low Noise LDO	9.8 mA	15 µV rms

Note 1: Peak currents are supported by the large µF capacitors present near the voltage input package pins, with suggested values as shown in the sample circuit in Figure 6.

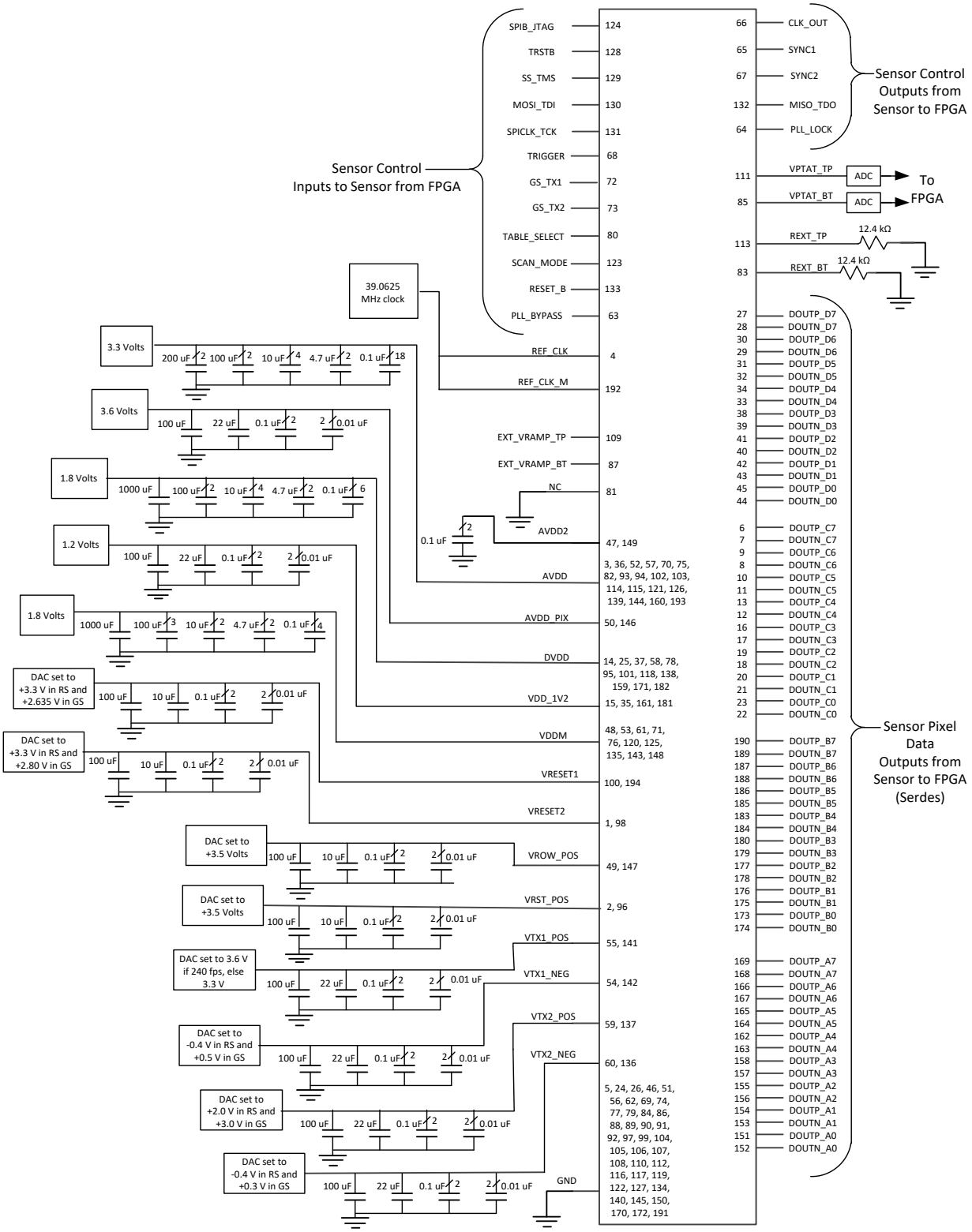


Figure 6. Sample Circuit showing Filter capacitors on Voltage inputs

3.1.2 Power Consumption

Table 7: Power Consumption (typical)

Shutter Mode	Gain channels active	30 fps	60 fps	120 fps	240 fps
Rolling Shutter	LG only	3670 mW	3797 mW	4032 mW	4826 mW
	HG + LG	4835 mW	5010 mW	5331 mW	6320 mW
Global Shutter	HG + LG	4778 mW	4946 mW	5263 mW	6238 mW

Note: In this table GS fps includes both Reset and Data frames, so that 240 fps GS means that 120 Reset frames and 120 Data frames are read out in one second, leading to 120 GS images in one second.

3.1.3 HSTL I/O DC Specifications

Table 8: HSTL DC Specifications

Symbol	Parameter	Min	Nom	Max	Conditions
V_{REF}	HSTL reference voltage	0.855	0.9	0.945	0.5*DVDD
V_{TT}	HSTL termination voltage	0.855	0.9	0.945	0.5*DVDD
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.1		DVDD + 0.3	V
$V_{IL(dc)}$	DC input logic low	-0.3		V_{REF} - 0.1	V
$V_{OH(dc)}$	DC output logic high	DVDD - 0.5			V
$V_{OL(dc)}$	DC output logic low			0.5	V
$I_{OH(dc)}$	Output minimum source DC current	-10 mA			@ $V_{OH(dc)}$= DVDD - 0.5
$I_{OL(dc)}$	Output minimum sink DC current	10 mA			@ $V_{OL(dc)}$= 0.5

3.1.4 LVCMOS I/O DC Specifications

Table 9: LVCMOS DC Specifications

Symbol	Parameter	Min	Nom	Max	Conditions
$V_{IH(dc)}$	DC input logic high	0.7*DVDD		DVDD + 0.3	V
$V_{IL(dc)}$	DC input logic low	-0.3		0.3*DVDD	V

3.2 Power Up Sequence

1. All pins at 0 and no powers applied.
2. Bring up digital and PLL power supplies (DVDD, VDD_1V2, and VDDM) to proper levels.
3. Enable REF_CLK running.
4. Release RESET_B and SS_TMS to 1.
5. Enable other power supplies.
6. Wait 0.2ms for PLL to achieve lock or monitor the PLL_LOCK status output for 1 and then wait an extra 200 REF_CLK cycles.

3.3 Power Down Sequence

Shut down all power supplies at the same time.

3.4 TX Driver

The gray box at left represents the SERDES output channels for a SERDES pair (for example DOUTP_A0 and DOUTN_A0). The gray box at right is the receiving electronics (e.g and FPGA) and the yellow box in the middle represents the PCB trace connections between the two.

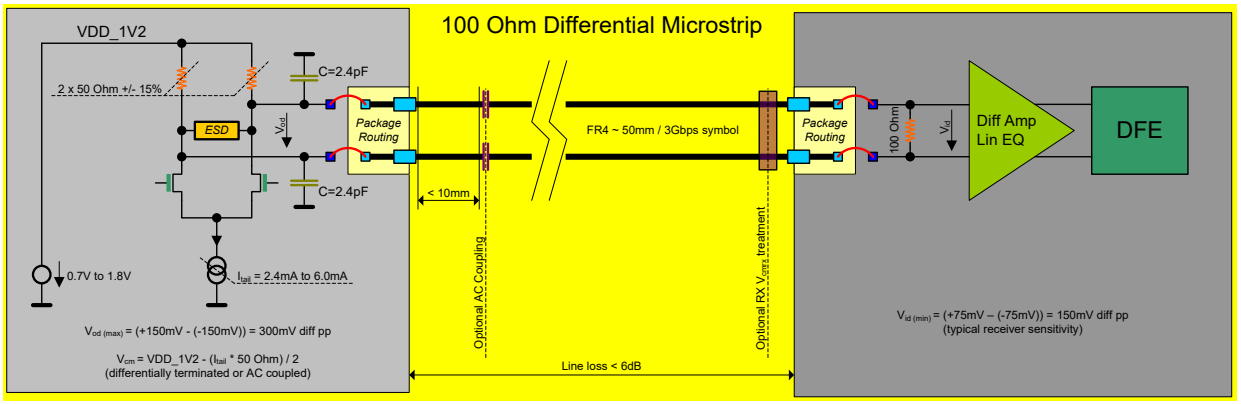


Figure 7. TX/RX Signal Path

Table 10: TX Power

Power						
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**	**Note**
AVDD	Power 3.3V	2.97	3.3	3.63	[V]	[+/-10%]; I < 3.0mA
DVDD	Power 1.8V	1.71	1.8	1.89	[V]	[+/- 5%] ; I < 80.0mA
VDD_1V2	CML Driver Power	0.7	1.0	1.8	[V]	Adjust for the desired CMM level (Note 1)

CML = Current Mode Logic

CMM = Common Mode

Note 1: The VDD_1V2 can be in the range of values. If the SERDES link is DC coupled the CMM (common mode) level must meet the FPGA CMM input range (the CMM can be tuned by varying the VDD_1V2 voltage in allowed range). If the link is AC coupled the VDD_1V2 is recommended at 1.2V. The CMM formula is in Figure 7 (driver side gray box).

Table 11: CML Driver

CML Driver						
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**	**Note**
DR_{DRV}	Driver Data Rate			3.125	[Gbps]	
V_{OD}	Out Launch Voltage	150		300	[mV]	Diff pp, 100 Ohm terminated(1)
V_{OCM}	Out CMM Voltage	0.6	1.0	1.6	[V]	Adjusted via VDD_1V2(2)
R_{OCT}	OCT R tuning	-15	0	15	[%]	Error from the (50 + 50) Ohm
t_{EMI_RF}	EMI rise / fall times	50	130	200	[ps]	With the bond wires
t_{DDS}	Drivers skew			10	[ps]	Any pair of channels
V_{ESDHBM}	ESD performance		2.0		[kV]	Human Body Model
V_{ESDCDM}	ESD performance		250		[V]	Charged Device Model
t_{J_ISI}	Driver ISI Jitter		3.0	7.6	[ps]	peak-to-peak
t_{J_TN}	Driver t_noise Jitter		0.5		[ps]	peak-to-peak
D_{PSJ}	Power Supply Jitter		0.83		[ps/mV]	Transferred from the rail ripple
(1)Output launch voltage V_{OD} is programmable in linear steps via the LAUNCH <1:0> input (00 = 150mV, 01 = 200mV, 10 = 250mV, 11 = 300mV). (2)V_{OCM} = VDD_12[A|B] – V_{OD}/2 or VDD_12[A|B] = V_{OCM} + V_{OD}/2. (e.g. If V_{OCM} = 1.0V, V_{OD} = 250mV then VDD_12[A|B] = 1.125V.)						

t_noise = temporal noise

OCT R tuning = On-chip-termination tuning (tuning the driver output impedance to 100 Ohm)

ISI = Inter-Symbol Interference

4 Timing Specifications

4.1 Serial Peripheral Interface (SPI) Pin Descriptions

Table 12: SPI Names and Descriptions

Pin Name	Package Pin Number	Direction	SPI Functionality
MISO_TDO	132	Output	SPI serial data output
SPICLK_TCK	131	Input	SPI clock
MOSI_TDI	130	Input	SPI serial data input
SS_TMS	129	Input	SPI chip enable (active low)

These 4 pins can operate either with JTAG or SPI protocols. The 4 pins operate with SPI functionality when the SPIB_JTAG input pin (package pin 124) is at logic 0.

TRSTB (package pin 128) is used with the JTAG interface. The JTAG interface is used for internal BAE testing, but the customer should use the SPI interface to communicate with sensor registers. In that case (where the customer exclusively uses SPI), tie TRSTB to logic 1 so it will not interfere with SPI communication.

4.1.1 SPI Interface Timing

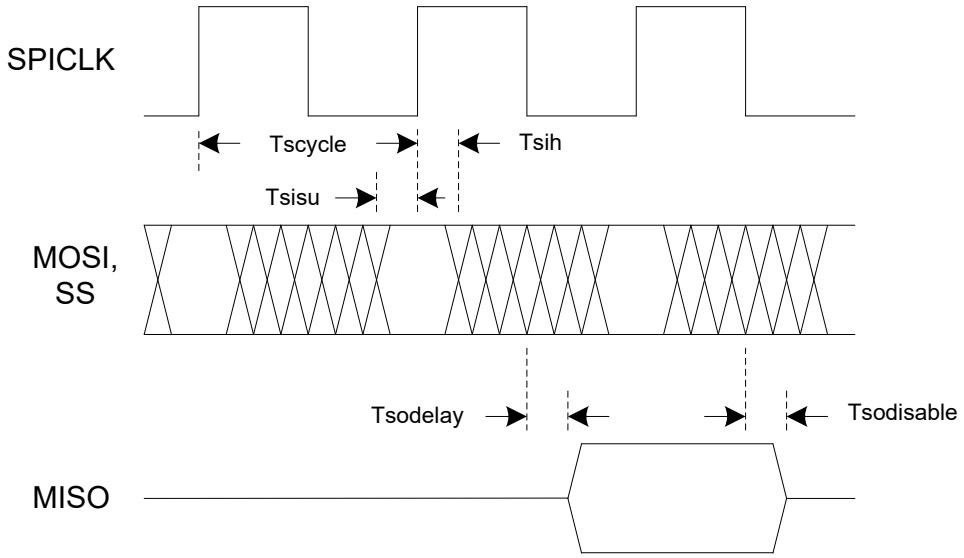


Figure 8. SPI Timing

Table 13: SPI Timing

Symbol	Description	Minimum	Maximum	Units	Note
Tscycle	SPICLK cycle time	50		ns	
DCsclk	SPICLK duty cycle	45	55	%	
Tsisu	SPI input setup	4		ns	
Tsih	SPI input hold	4		ns	
Tsodelay	SPI output delay		10	ns	
Tsodisable	SPI output disable		10	ns	

4.2 Reference Clock Timing

The Reference clock timing is defined in Table 13.

Table 14: Reference Clock Timing

Symbol	Description	Minimum	Typical	Maximum	Units	Note
Tref_clk_cycle	REF_CLK cycle time	10	25.6	40	ns	Note 1
DCref_clk	REF_CLK duty cycle	45		55	%	

Note 1: REF_CLK frequency (and cycle time) is dependent on the PLL divider setting (see PLL Configuration Register, Register 0x26). Maximum limit does not apply when PLL is bypassed.

4.3 Control Inputs

All control inputs (TRIGGER, RESET_B, TABLE_SELECT) are synchronized internally in the sensor. No IO timing for these inputs is needed.

4.4 Control Outputs

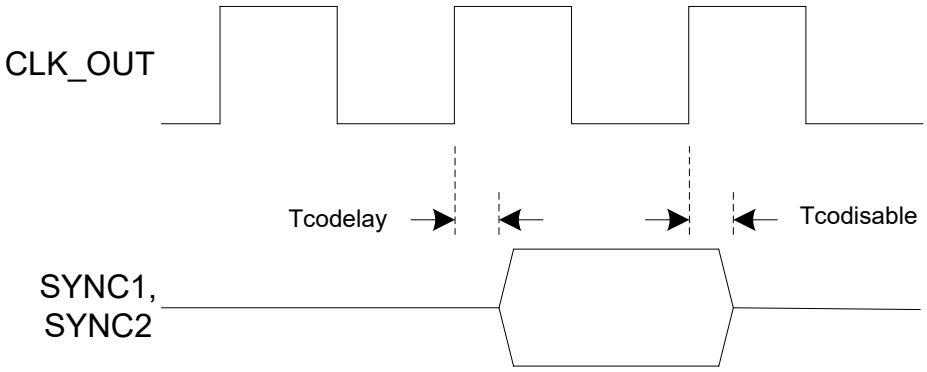


Figure 9. Control Outputs Timing

Table 15: Control Output Timing

Symbol	Description	Minimum	Maximum	Note
Tcodelay	Control output delay		1ns	Note 1
Tcodisable	Control output disable		1ns	

4.5 JTAG Interface

JTAG timing is shown in Figure 10 and Table 16.

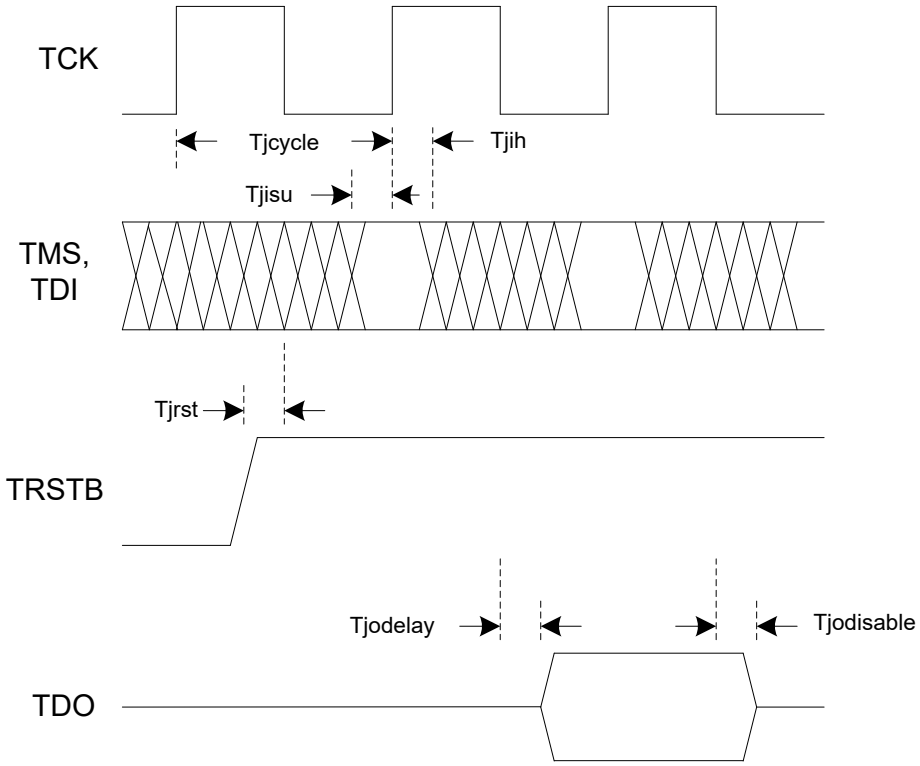


Figure 10. JTAG Interface I/O Timing

Table 16: Timing Parameter Definitions for SPI Interface I/O Timing

Parameter	Definition	Min	Max	Unit	Note
Tjcycle	TCK cycle time	100		ns	
Tjdc	TCK duty cycle	45	55	%	
Tjisu	JTAG input setup	4		ns	
Tjih	JTAG input hold	4		ns	
Tjrst	JTAG reset recovery				
Tjodelay	JTAG output delay		10	ns	
Tjodisable	JTAG output disable		10	ns	

5 Definition of Terms Used in Datasheet

5.1 Hard and Soft Reset

The sensor has a dedicated pin RESET_B and a register bit (Mode Register) to control sensor reset operation. The reset operation due to the assertion of RESET_B is called “hard reset”. The reset operation due to the programming of the Mode Register is called “soft reset”. Both resets initialize all the control functions of the sensor. The hard reset has additional functions beyond soft reset:

1. Force all register values back to default values (soft reset preserves previous register values);
2. Force the sensor to stay to reset state until PLL lock is achieved.

5.2 Region of Interest

There are 3 Vertical Regions of Interest (V-ROI) along the row axis. The ROI are programmable by the starting row address and ending row address. The scanning direction is always from starting address to ending address. The unit for the addresses is in grouping of 4 rows. Thus the complete readable array of 2640 rows is covered by 660 address groups. The regions cannot overlap each other.

There is another special region and that is virtual row region. The virtual rows are not physical rows and there is no pixel data for these rows. But by adding virtual rows, frame time can be extended. The virtual rows are programmed in unit of groups of 4 row at a time.

The regions are accessed in the following order: V-ROI1, V-ROI2, V-ROI3, virtual.

5.3 Horizontal Right Edge Cropping

The sensor does not support any horizontal column region. Columns are always read from the left edge of column 0 to the right. However the sensor does support the right edge cropping, i.e. columns from the far right side can be dropped from being read. The programming of the cropping edge is in units of 24-column.

5.4 Black Sun

A particularly annoying image artifact is called the black sun. In order to improve noise performance the sensor uses a “Correlated Doubling Sampling” (CDS) technique in which the floating diffusion node is sampled first for reference and then sampled again after the pixel charges are transferred from the photo-diode to the floating diffusion node. The first sample is then subtracted from the second sample with noise subtracted out in the process. However when the pixel is subjected to intense illumination such as facing toward the sun, both samples are saturated resulting in close to zero signal level after the subtraction process. Instead of appearing bright (saturated value), the result is black (zero value). This is called “black sun” artifact. The sensor has built in circuitry to detect this phenomenon and if enabled by the user, will force both the HG and the LG value to output full scale value when this happens.

5.5 Wavetables

Wavetable is a set of registers that defines waveforms for the targeted signals. The definition includes the initial value of the signal as well as the time into the row that the signal changes value. The use of wavetable allows the ability to update the critical waveform in the field for optimal performance.

There are two banks of wavetable registers in the sensor, bank A and bank B. The selection of which bank to use is through the pin TABLE_SEL which is sampled near the middle of a row time and becomes effective for the next row. Typically for Global Shutter operation, bank A is used for reference frame operation and bank B for data frame operation. Rolling Shutter uses only bank A.

Since the wavetables are in use continuously to control waveform generation, it is recommended that they not be changed unless the sensor is in soft reset. There is no blocking mechanism inside the sensor to protect them from changing while in active operation.

5.6 Serial Outputs

The sensor outputs its data through 32 high speed serial transmitters (TX lanes) operating at maximum rate of 3.125Gbps. The 32 TX lanes are partitioned into 4 groups of 8 lanes each, one group for each output row (there are 4 simultaneous rows being read out). The number of TX lanes within each group as a function of frame rate is shown in the following table:

Table 17: Frame Rate vs. Number of Lanes Per Row Group

Rate (Frames per Second) FPS	Number of TX lanes per row group
Full (240)	8
0.75 (180)	6
0.5 (120)	4
0.25 (60)	2
0.125 (30)	1

5.6.1 Data Packets

Pixel data are transmitted through each TX lanes in the form of packets. The 22 bits of pixel data (11 bits of Low Gain data and 11 bits of High Gain data) are packed into three 1 byte words (word0 = HG_data[7:0], word1 = {LG_data[4:0], HG_data[10:8]}, word2 = {2'b0, LG_data[10:5]}) and are sent with word0 and LSB first.

Packet Byte 0: Start of Packet Symbol (SOP). This is the K27.7 character.

Packet Byte 1: Identification Byte 0 (ID0). This is the least 8 bits of a 12-bit row sequence number within a frame. Lanes in Group A always have sequence number 0, 4, 8 and so on. Lanes in Group B have sequence number of 1, 5, 9 and so on. Lanes in Group C have sequence number of 2, 6, 10 and so on. Lanes in Group D have sequence number of 3, 7, 11 and so on. Row sequence number always resets to 0 for a new frame. Any soft reset or change of VROI setting resets the frame sequence count as well.

Packet Byte 2: Identification Byte 1 (ID1). This is a combination of 1 bit of reference (=1) or data (=0) frame indicator, 1 bit of last packet in a frame indicator, 2 bits of frame sequence number and the most significant 4 bits of the row sequence number. When the frame sequence number reaches 3, it resets back to 0.

Packet Byte 3 to N-3: Column pixel data. The 3 byte pixel data from a column is placed into the packet for a lane as a 3-byte chunk and the columns data are distributed among the

active lanes in a round-robin way. Thus for packet byte 3 in a 8 lane group, word0 of column 0 goes to lane 0, word0 of column 1 goes to lane 1, …., word0 of column 7 goes to lane 7. For packet byte 4, word1 of column 0 goes to lane 0, word0 of column 1 goes to lane1, …, word1 of column 7 goes to lane 7. The pattern repeats until all columns are done.

Packet Byte N-2: Cyclic Redundancy Check Byte 0 (CRC0). This is the 8 LSB of a 16-bit CRC[1] for the preceding packet words other than SOP.

Packet Byte N-1: Cyclic Redundancy Check Byte 1 (CRC1). This is the 8 MSB of the 16-bit CRC for the preceding packet works other than SOP.

Packet Byte N: End of Packet Symbol (EOP). This is the K29.7 character.

Pictorially, the packets for the 8 lanes look like this:

Table 18: Packets of Data vs. Lane Number

Word	Lane 7	Lane 6	Lane 5	Lane 4	Lane 3	Lane 2	Lane 1	Lane 0
word 0	SOP	SOP	SOP	SOP	SOP	SOP	SOP	SOP
word 1	ID0	ID0	ID0	ID0	ID0	ID0	ID0	ID0
word 2	ID1	ID1	ID1	ID1	ID1	ID1	ID1	ID1
word 3	c7_0	c6_0	c5_0	c4_0	c3_0	c2_0	c1_0	c0_0
word 4	c7_1	c6_1	c5_1	c4_1	c3_1	c2_1	c1_1	c0_1
word 6	c7_2	c6_2	c5_2	c4_2	c3_2	c2_2	c1_2	c0_2
word 7	c15_0	c14_0	c13_0	c12_0	c11_0	c10_0	c9_0	c8_0
word 8	c15_1	c14_1	c13_1	c12_1	c11_1	c10_1	c9_1	c8_1
word 9	c15_2	c14_2	c13_2	c12_2	c11_2	c10_2	c9_2	c8_2
:	:	:	:	:	:	:	:	:
word N-3	0	0	0	0	0	0	c_m_2	c_{m-1}_2
word N-2	CRC0	CRC0	CRC0	CRC0	CRC0	CRC0	CRC0	CRC0
word N-1	CRC1	CRC1	CRC1	CRC1	CRC1	CRC1	CRC1	CRC1
word N	EOP	EOP	EOP	EOP	EOP	EOP	EOP	EOP

Note 1: The 16-bit CRC uses a polynomial function of $x^{16} + x^{15} + x^2 + 1$.

5.6.2 Inter-packet Gap

When not transmitting active packets and not in hard reset, the transmitter continuously transmits COMMA symbol (K28.5).

5.6.3 Error Exception

5.6.3.1 Soft Reset or Activation of Low Power Mode in The Middle of Packet

When the sensor goes into soft reset or when low power mode is activated in the middle of a packet (the packet is terminated prematurely), the sensor will terminate the on-going packet with an End of Packet with ERROR symbol (K30.7) followed by the inter-packet gap.

5.6.3.2 Soft Reset or Activation of Low Power Mode in The Middle of a Frame and During Inter-packet Gap

When the sensor goes into soft reset or when low power mode is activated in the middle of inter-packet gap in the midst of a series of packets for a frame (the current on-going frame transmission is terminated prematurely), the sensor will transmit an End of Frame with ERROR symbol once on all active lanes instead of the usual COMMA symbol. The End of Frame with ERROR symbol is K28.1. The usual COMMA symbol will resume after the End of Frame with ERROR symbol.

5.6.4 Similarities between 4625 protocol and XAUI

The XAUI standard is designed as an interface extender for the 10 Gigabit Attachment Unit Interface XGMII. The XGMII provides full duplex operation at a rate of10 Gb/s between the MAC and PHY.

Fairchild's proprietary interface protocol resembles a simplified XAUI. It is electrically compatible with IEEE 802.ae specifications. The 4625 uses proprietary data packet transmission and supports the K characters listed below. The following two tables show similarities and difference between the 4625 and standard XAUI.

Table 19: Similarities of 4625 Interface Protocol and XAUI Standard

Characters	4625	Standard XAUI
K27.7	Start of Packet (SOP)	START
K28.5	COMMA (Alignment Symbol)	SYNC
K29.7	End of Packet (EOP)	TERMINATE
K30.7	ERROR	ERROR
K28.1	EOF with ERROR	EXTRA CODE
ENCODING	8B/10B	8B/10B

Table 20: Differences between 4625 Interface Protocol and XAUI Standard

Items	4625	Standard XAUI
Number of Lanes (RX)	0	4
Number of Lanes (TX)	32 (4 independent groups of 8)	4
Start of Packet	Transmitted on every lane	Transmitted on Lane 0
Packet Transmission	Proprietary	XGMII

6 Functional Description

6.1 Architectural Overview

6.1.1 Block Diagram

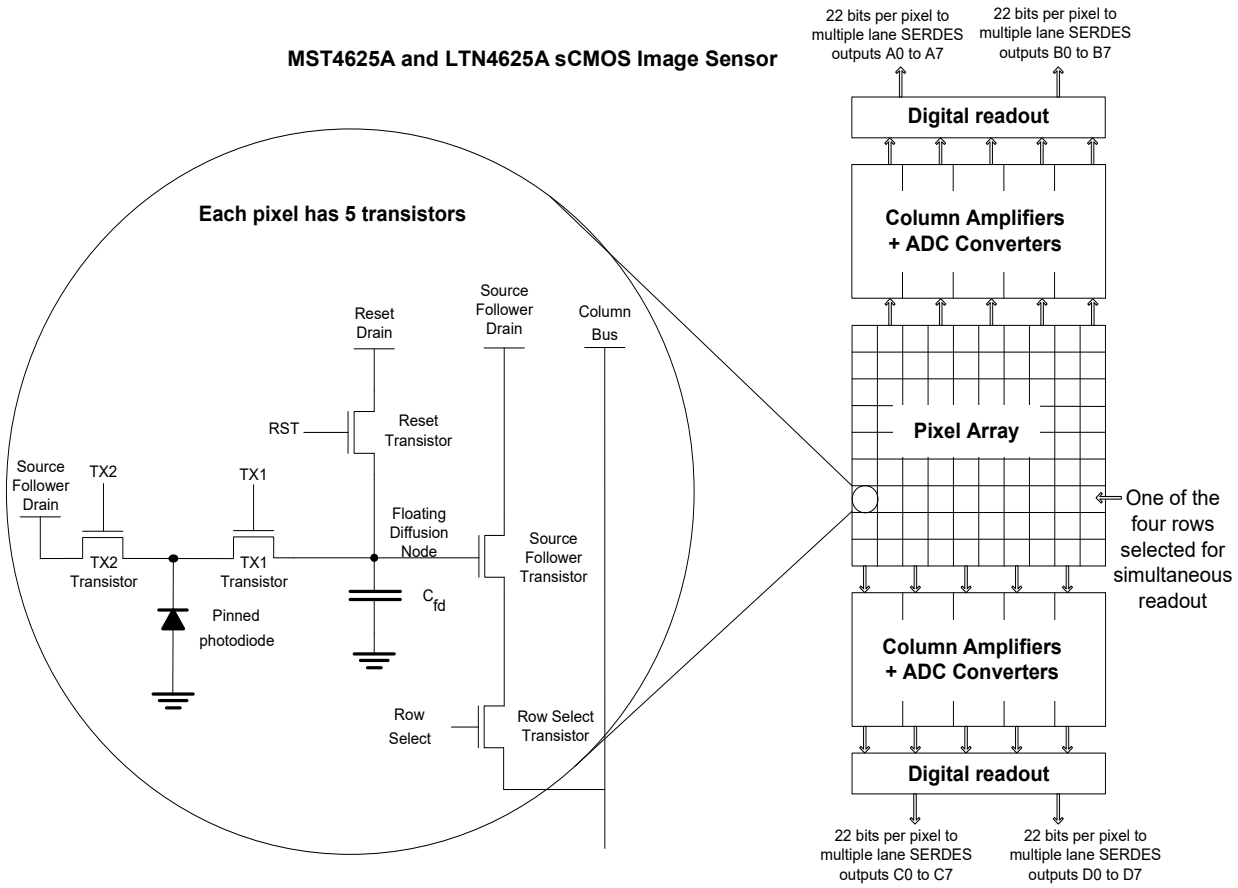


Figure 11. Block Diagram of MST4625A and LTN4625A

6.2 Functional Block Diagram

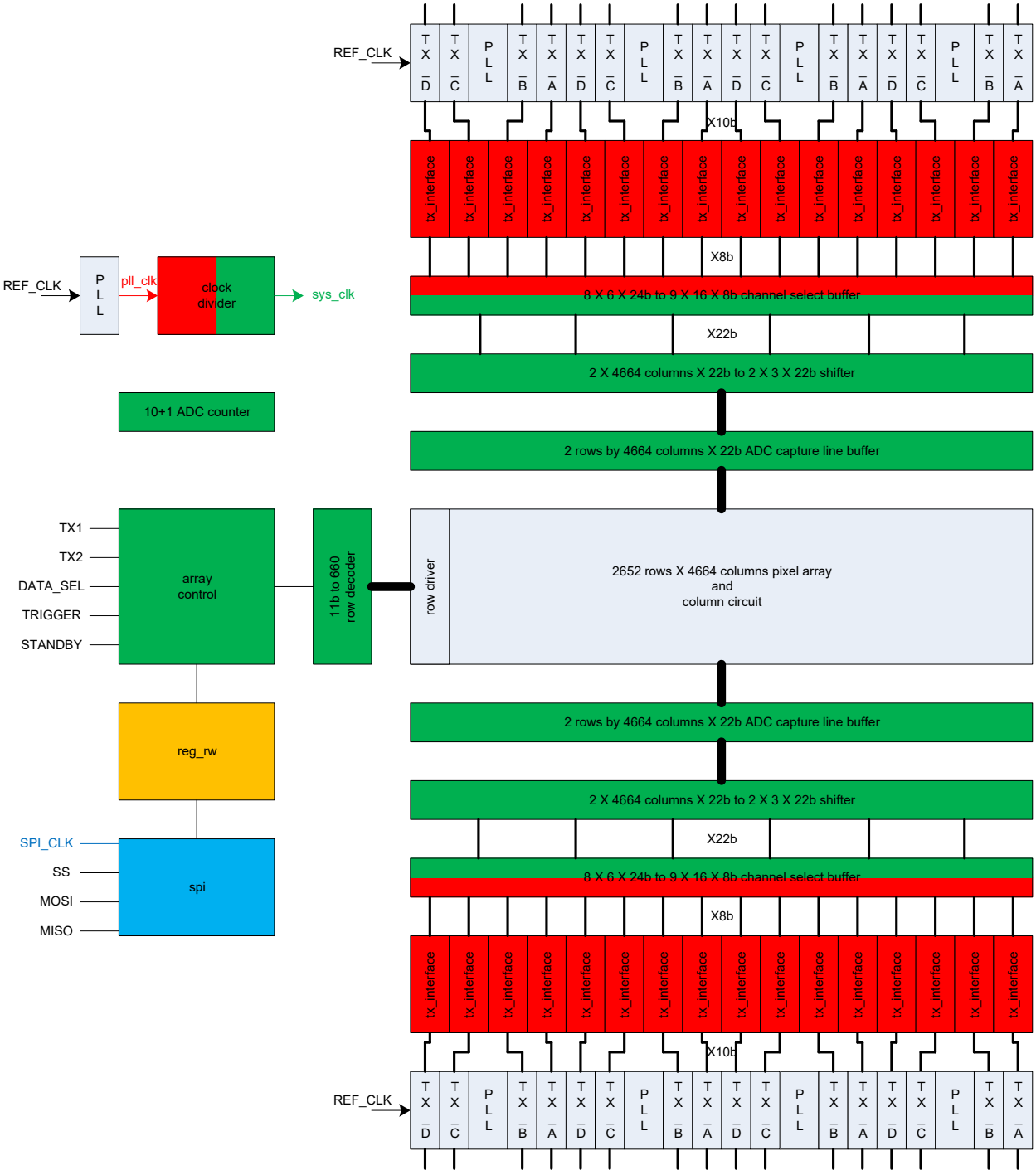


Figure 12. Functional Block Diagram

6.3 Device Architecture

6.3.1 Pixel Array Architecture

The active image area of the pixel array is 4608 pixels wide and 2592 pixels high, but there is also a 16 pixel wide border that is light sensitive and surrounds the active image area on all sides. There are 2 dark and 2 uncovered columns on each side. In addition there are 16 black covered columns on the left of the die and 8 dark dummy (unread) columns on the right side of the sensor.

The optically dark rows are covered with metal so light cannot enter. The electrically dark rows are also covered with metal so light cannot enter but in addition, all the pixels of these rows have the gates of their TX2 transistors tied high when programmed to do so. This makes them “electrically dark” as well as “optically dark”, because any charge in these dark rows (from dark current, for example) is removed via the TX2 charge dump, which is permanently active for these rows.

Columns are to 0 to 4663 (left to right), Rows are numbered from 0 to 2651 (top to bottom).

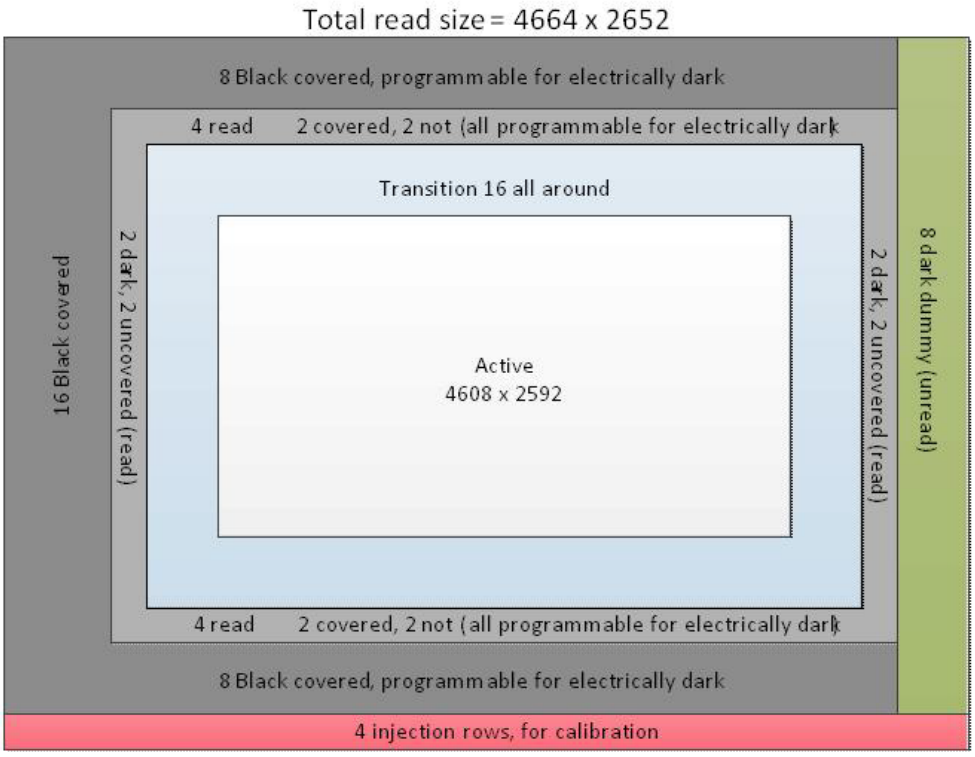


Figure 13. MST4625A and LTN4625A pixel array with column and row numbering

The uppermost row is row 0. The leftmost column is column 0.

6.3.2 Pixel Architecture

A schematic diagram of the 5T pinned photodiode pixel is shown in Figure 14 below. The pinned photodiode inside of each pixel starts to integrate charge as soon as the transfer gate TX1 is turned off, then when the transfer gate TX1 is turned on, the integrated charge in the photodiode is dumped onto the floating diffusion node and read out as a voltage signal by the source follower. The TX2 gate serves as both a global reset gate and a lateral anti-blooming protection gate.

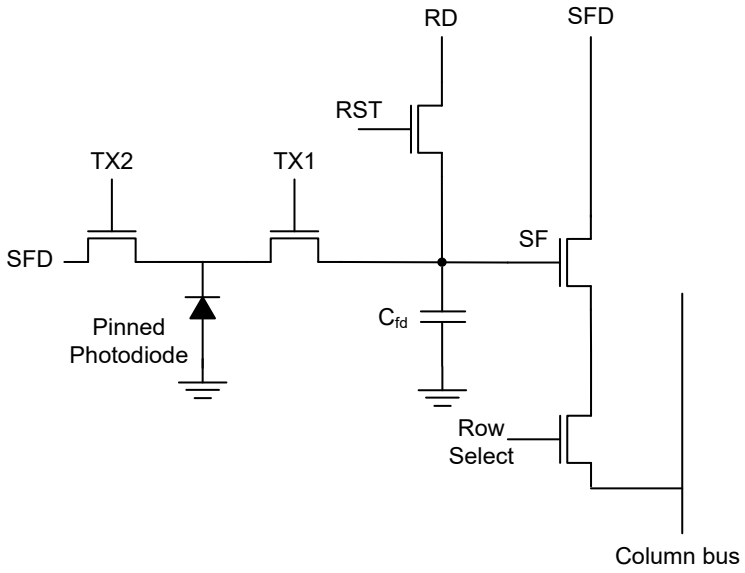


Figure 14. 5T pixel schematic

7 Packaging Specifications

7.1 Thermal Specifications

Table 21: Thermal Specifications

Parameter	Minimum	Maximum	Units
$T_{operation}$ (Temperature measured at junction)	-40	+55	ºC
Storage temperature range	-40	+80	ºC

The ceramic for the MST4625A and LTN4625A packages is Alumina A440, which has the following thermal properties:

Table 22: Thermal Properties of Package ceramic

Parameter	Value
Thermal expansion coefficient	7.1×10^{-6} ºK^{-1}
Thermal conductivity	14 Watts/m-ºK
Specific heat	770 J/kg-ºK

The package has had its R_{ja} and R_{jb} values measured according to the JESD51 standard:

Table 23: Package Thermal Resistance Values

Parameter	Thermal Resistance in °C/W
R_{ja} Thermal Resistance Junction to Air (still air)	10.4
R_{jb} Thermal Resistance Junction to Board	3.1

7.2 FX3 Sealed Window Standard Package drawings

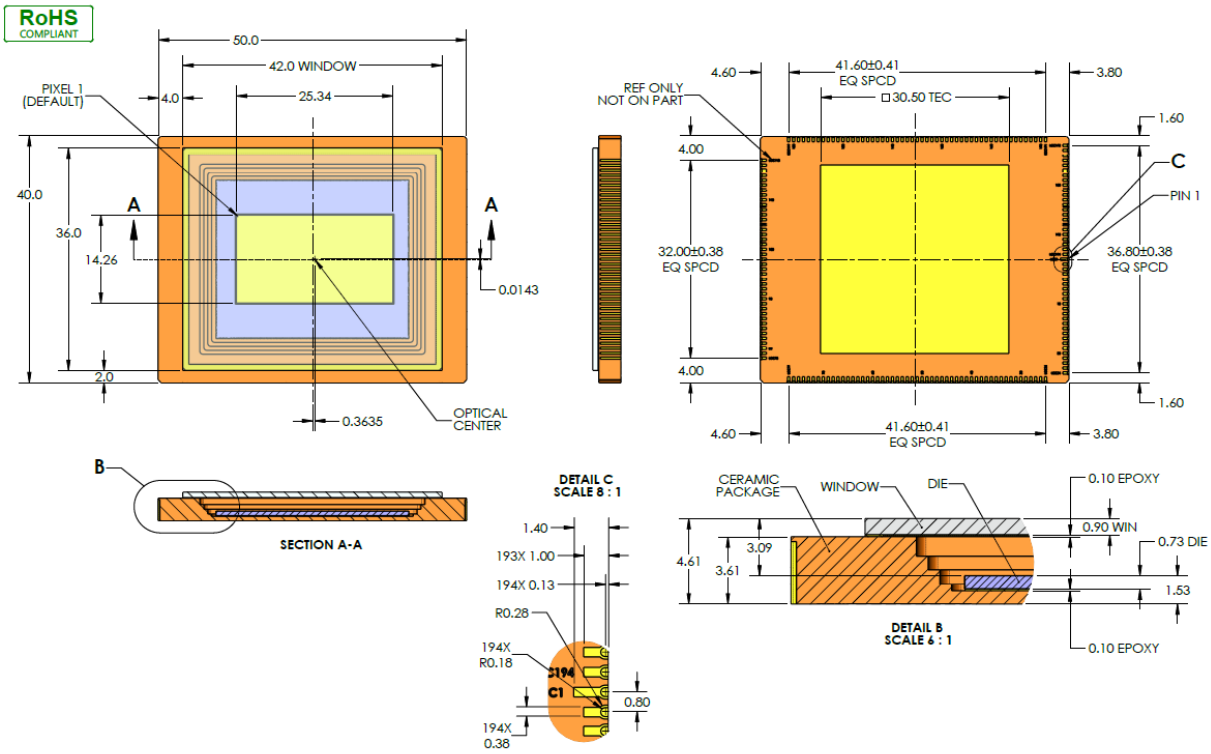


Figure 15. MST4625A and LTN4625A FX3 sealed window package overview

All dimensions in Figures 15 through 19 are in millimeters.

The FX3 standard package is shown in detail in Figure 16, Figure 17, Figure 18, and Figure 19.

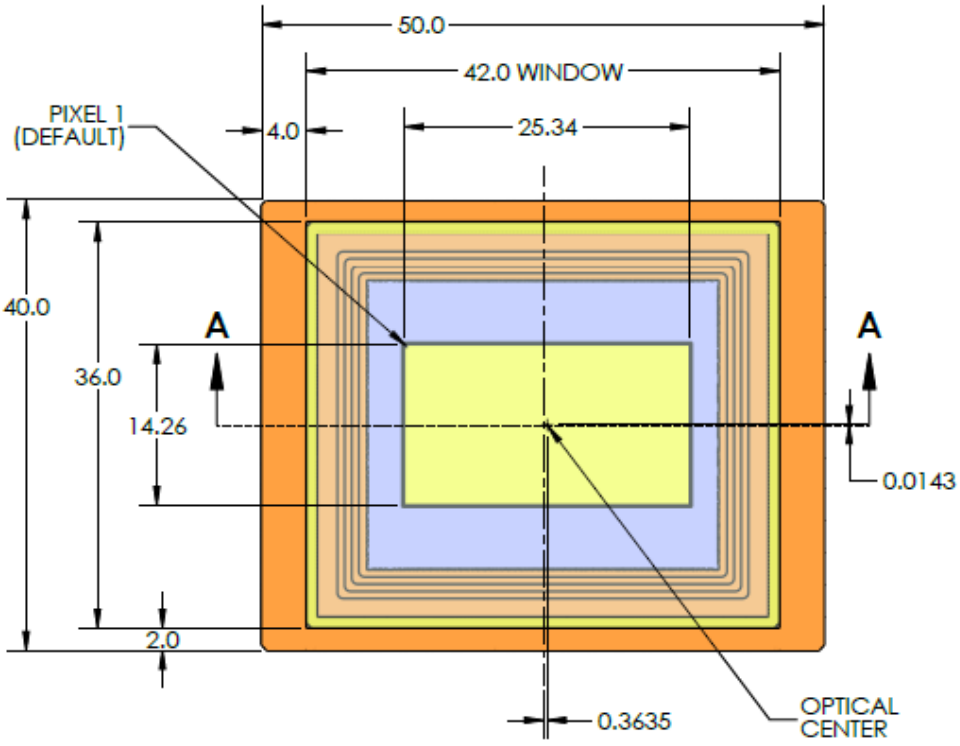


Figure 16. FX3 Sealed Window Standard package top view

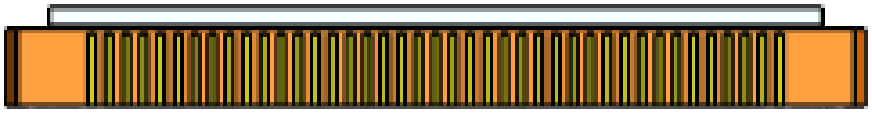
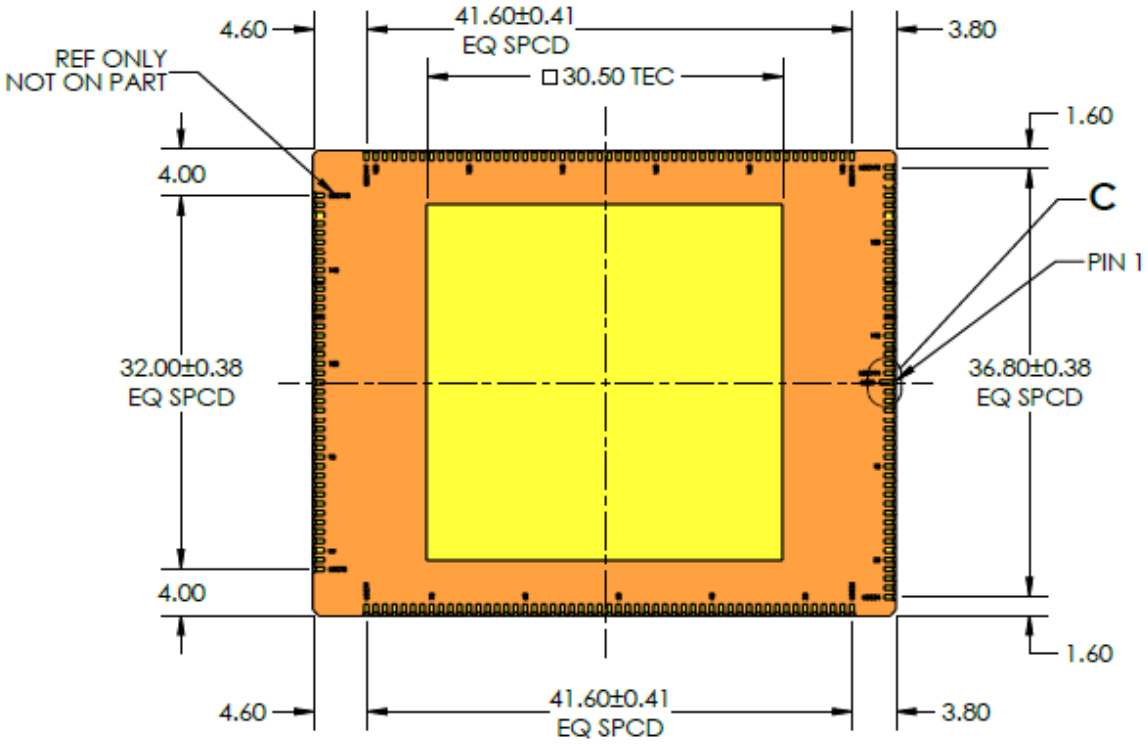


Figure 17. FX3 Sealed Window Standard package side view



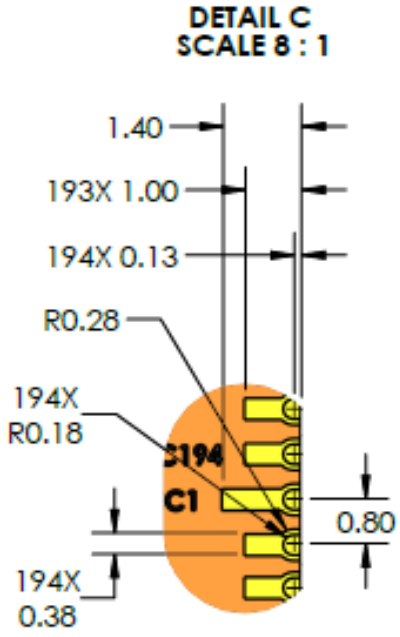


Figure 18. FX3 Sealed Window Standard package bottom view

A cross section of the sensor is shown in Figure 19.

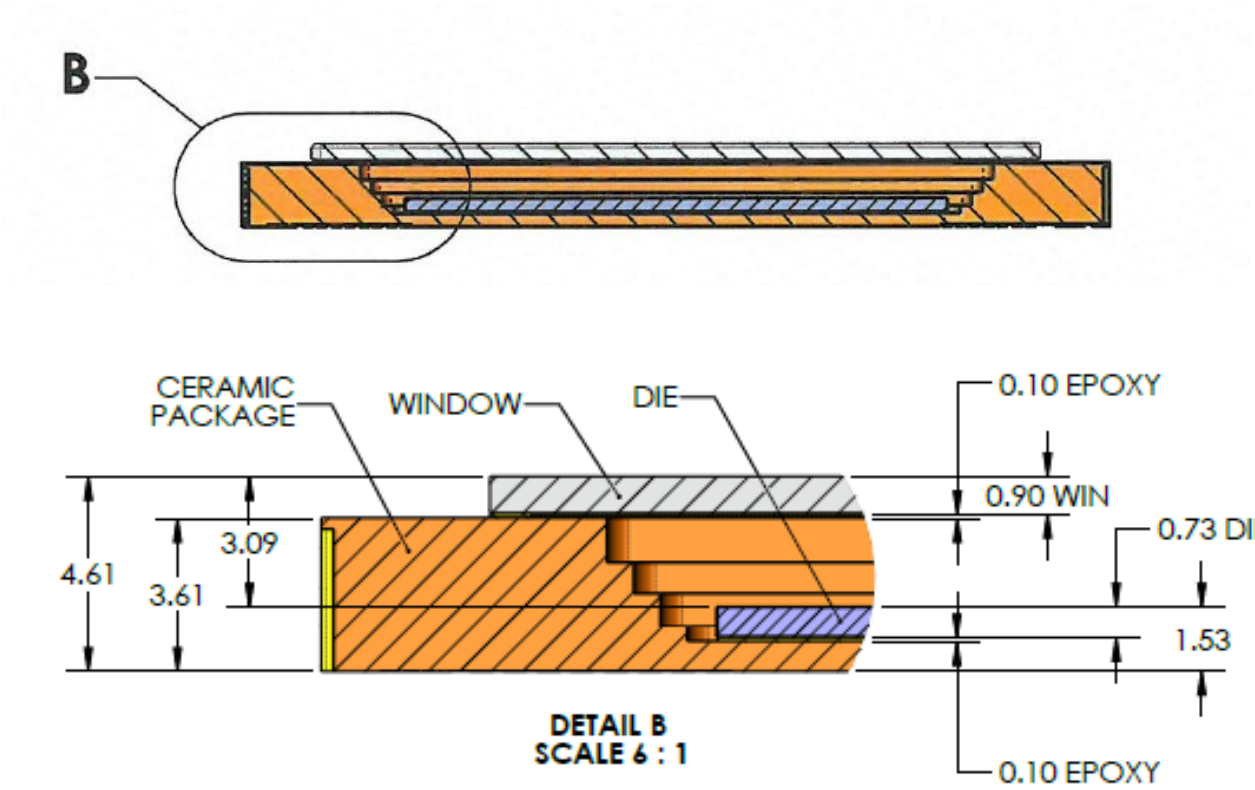


Figure 19. FX3 Sealed Window Standard package cross section

The sealed window has an Anti-reflection coating on each side of the glass.
The % Transmission specifications are:

Table 24. Transmission of Anti-reflection coated glass for sealed window part

Wavelength (nm)	Transmission of AR/AR coated glass (%)
365	> 50
400 - 900	≥ 97
900 - 1050	≥ 88
1050 - 1100	≥ 85

7.3 FX4 Temporary Window Standard package drawings

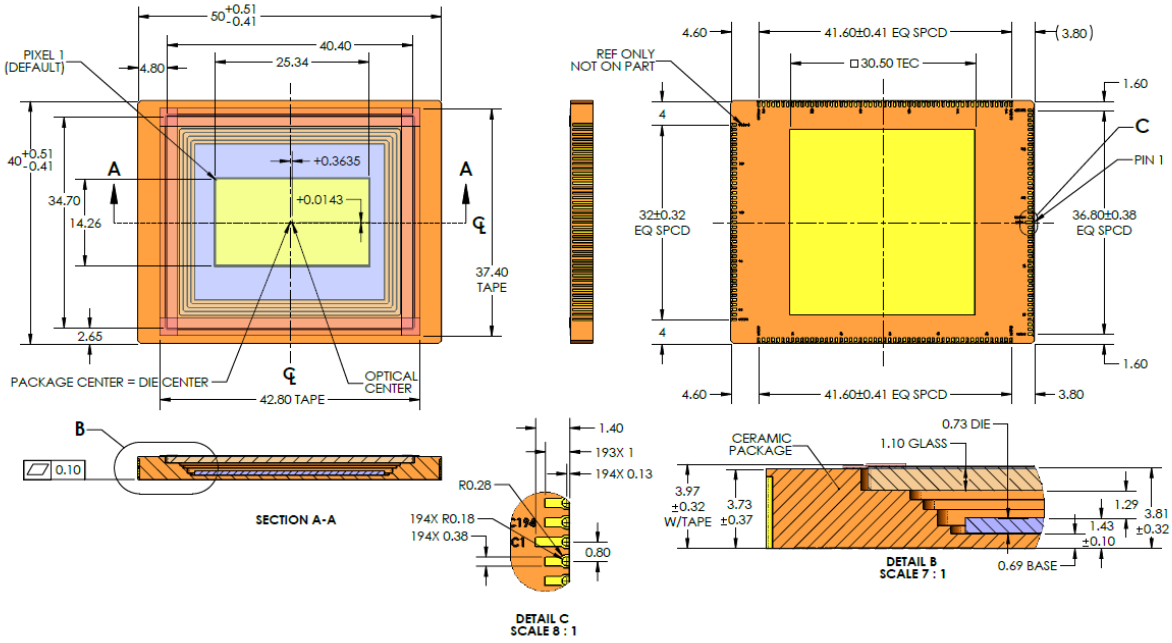


Figure 20. MST4625A and LTN4625A FX4 temporary window package overview

All dimensions in Figures 20 through 24 are in millimeters.

The FX4 standard package is shown in detail in Figure 21, Figure 22, Figure 23, and Figure 24.

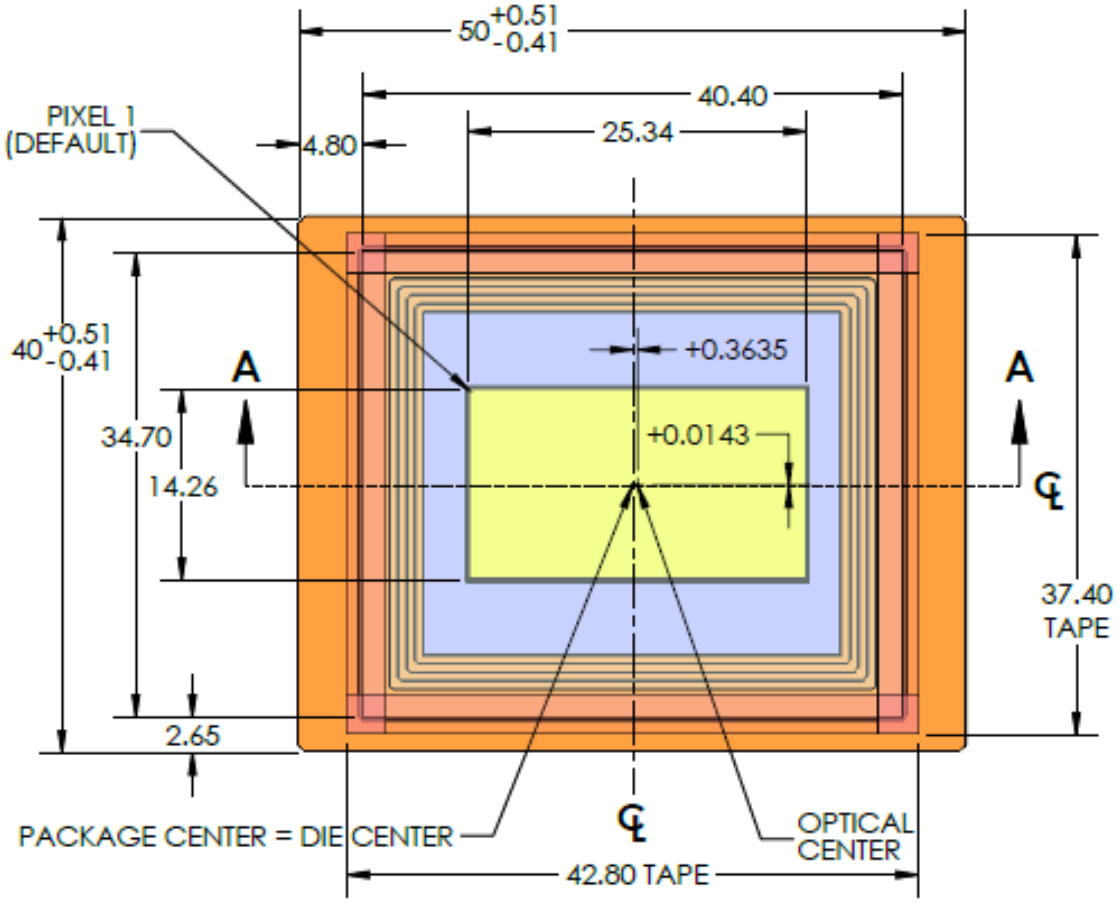


Figure 21. FX4 Temporary Window Standard package top view

Figure 22. FX4 Temporary Window Standard package side view

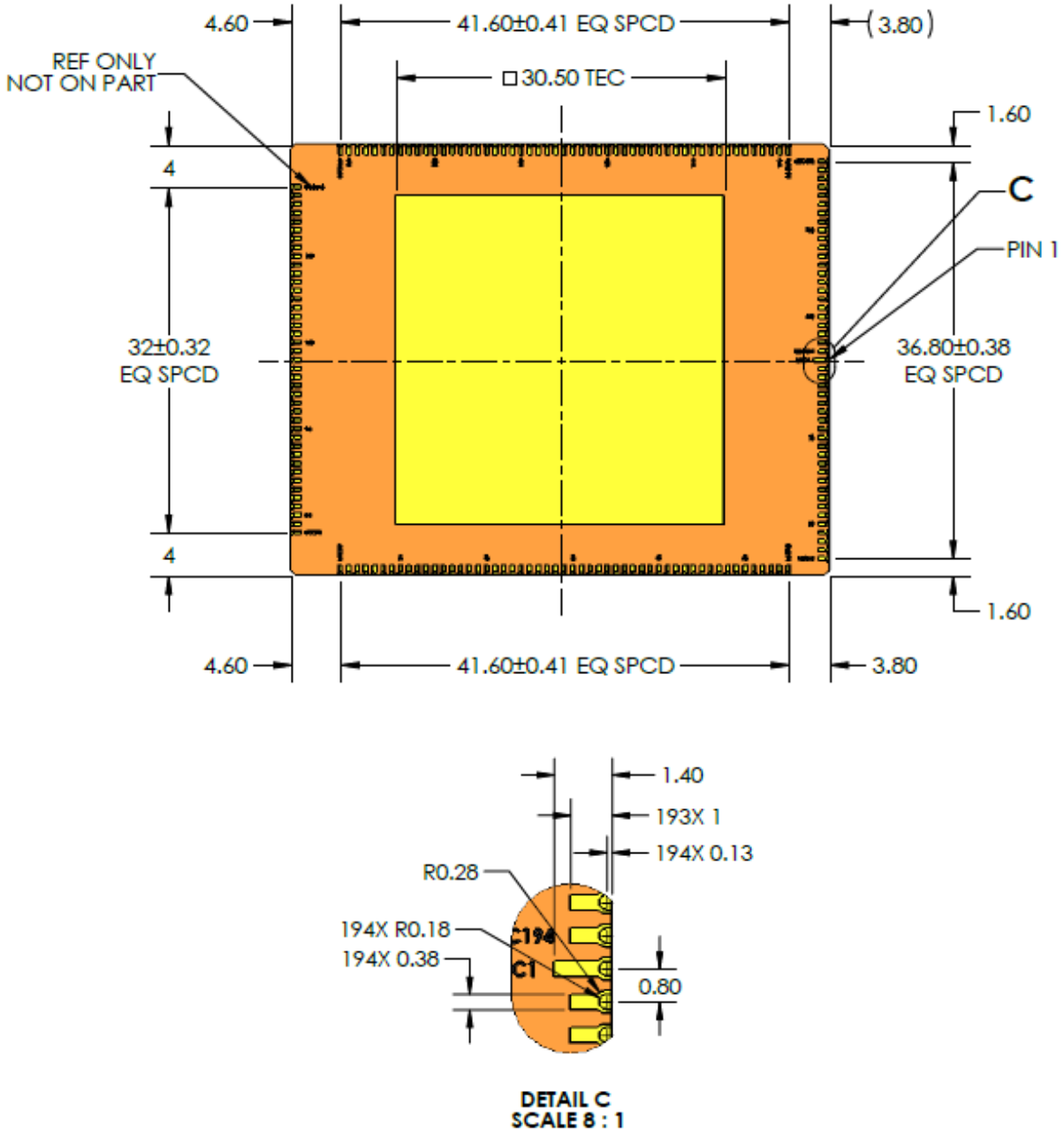


Figure 23. FX4 Temporary Window Standard package bottom view

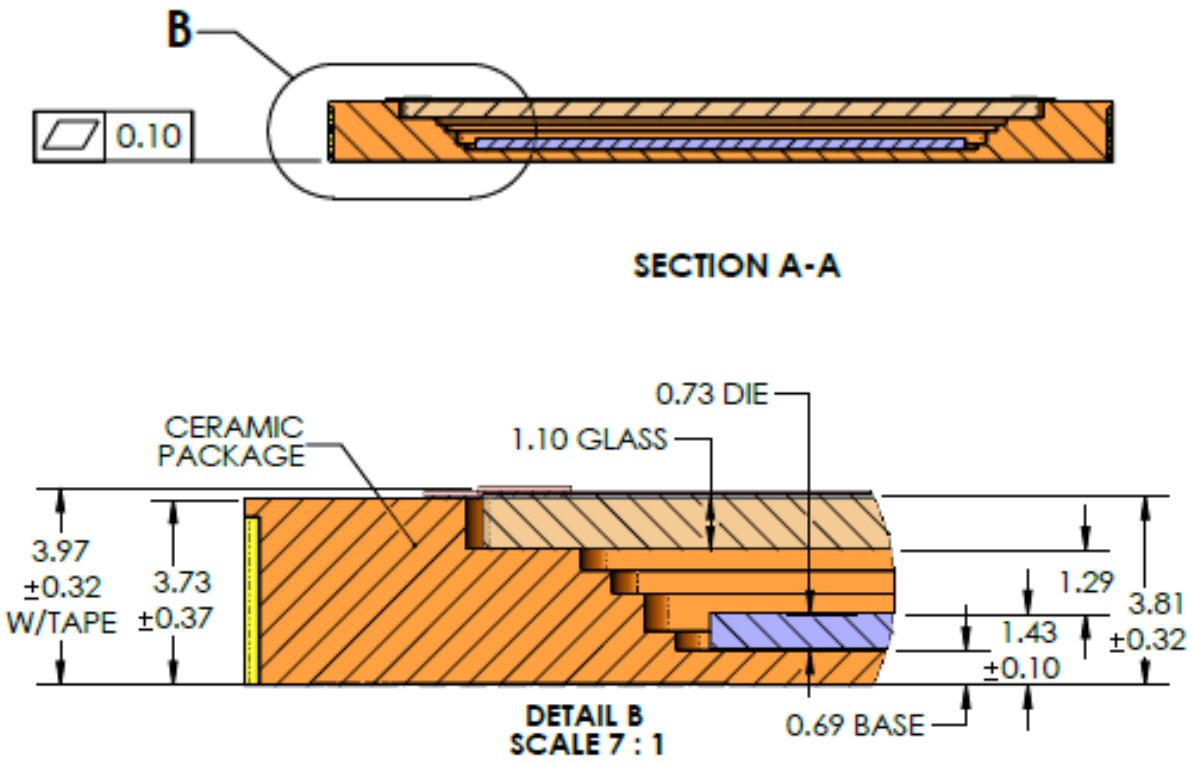


Figure 24. FX4 Temporary Window Standard package cross section

7.4 Standard Package Pad Diagram for both FX3 and FX4 packages

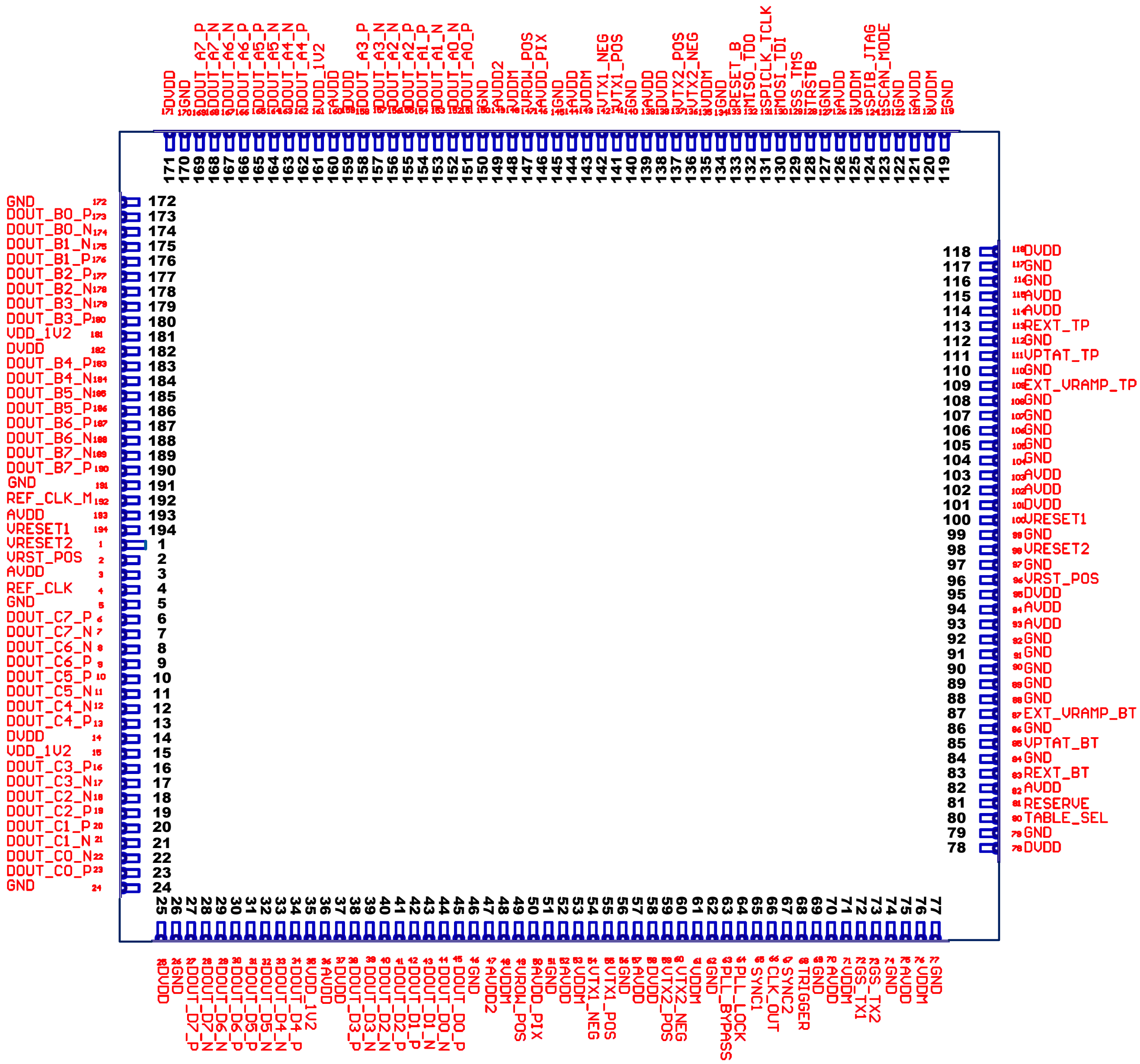


Figure 25. Standard Package Pad Diagram for both FX3 and FX4 packages

7.5 Handling Precautions

7.5.1 ESD Protection

To avoid damaging the device during handling, special care must be used with strict ESD controls. Use only ESD protected tools and ESD protected workstations. Operators must be equipped with approved ESD safe garments and use approved grounding equipment.

7.5.2 Moisture Protection

The Moisture Sensitivity Level (MSL) of the package is MSL 2, which means the package can resist moisture ingress under conditions of 30°C and 60% relative humidity for a year or more.

7.5.3 Soldering Requirements

For soldering the part, the temperature should not exceed 245°C for more than 60 seconds. Follow temperature ramp guidelines in JEDEC/IPC standard J-STD-020, current revision, for the IR/Convection oven reflow profile.

7.5.4 Socket Option

As an alternative to soldering, sockets for the 4625 are available from Andon Electronics (http://www.andonelect.com/). For both the FX3 and FX4 packages, Andon Electronics part number ***690-194-SM-G10-L14-X*** is used. Since the only physical difference between LTN and MST is the color filter array, the same socket is used for both.

7.5.5 Cleaning Requirements

For cleaning the window, first recognize the active area of the sensor. Only the window surface above the active area needs to be cleaned. Do not pour solvent or any liquid directly on to the window surface. Use a clean, lint-free swab. Dip the swab in methanol or isopropyl alcohol and carefully wipe the surface of the window. Clean, dry air can also be used to blow particle contamination off the window.

Cleaning the sensor active area surface itself is not possible with the MST4625A or LTN4625A with the epoxy-sealed window that covers the sensor's active area.

Cleaning the sensor active area surface itself is not recommended for the LTN4625A with the non-sealed window package, as it is very sensitive to damage.

For cleaning the sensor package, use a clean, lint-free swab, dipping the swab in methanol or isopropyl alcohol and carefully wiping the sensor package. Acetone can also be used to clean

the sensor package, but only if it can be kept away from the window seal epoxy. Clean, dry air can also be used to blow particle contamination off the window.

8 Signal Groups

8.1 Power and Ground (Standard Package)

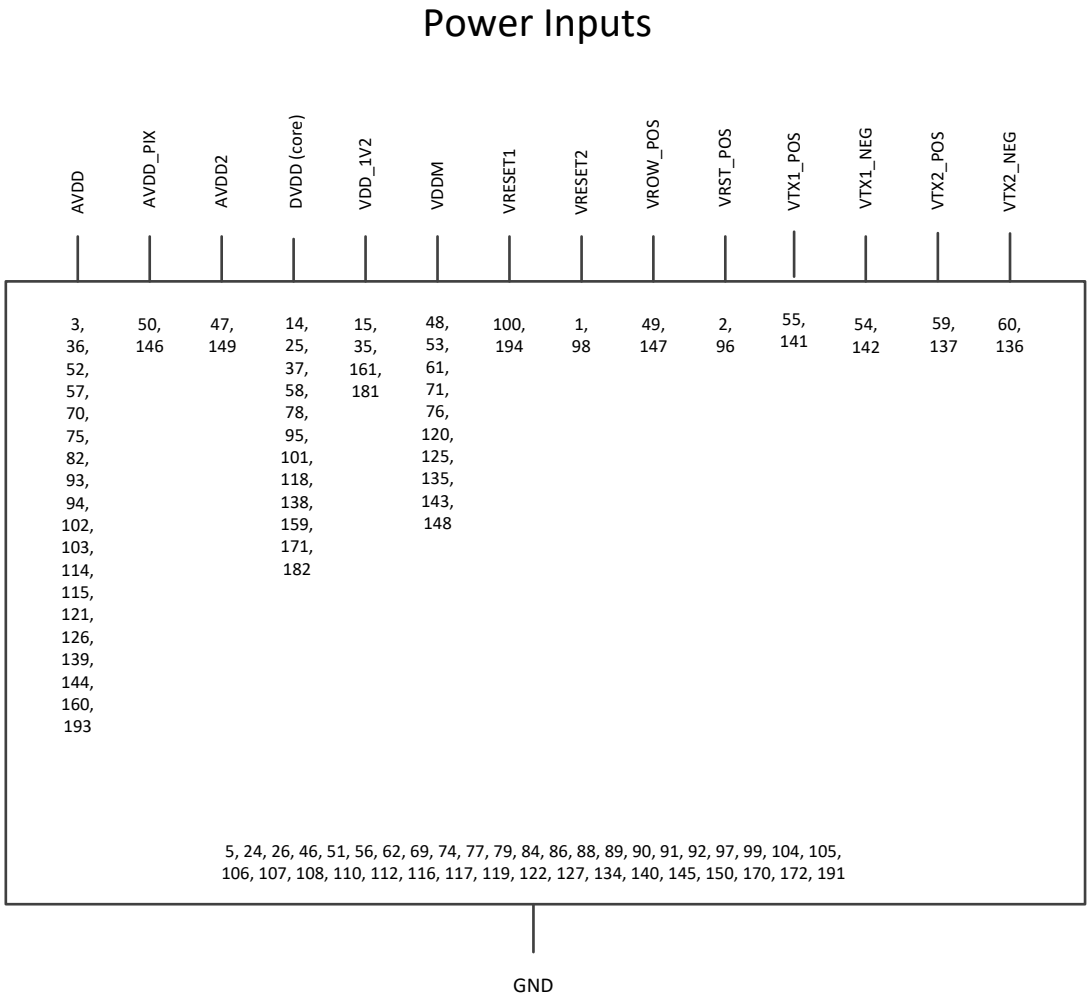


Figure 26. Power and Ground Connections

8.2 Signals (Standard Package)

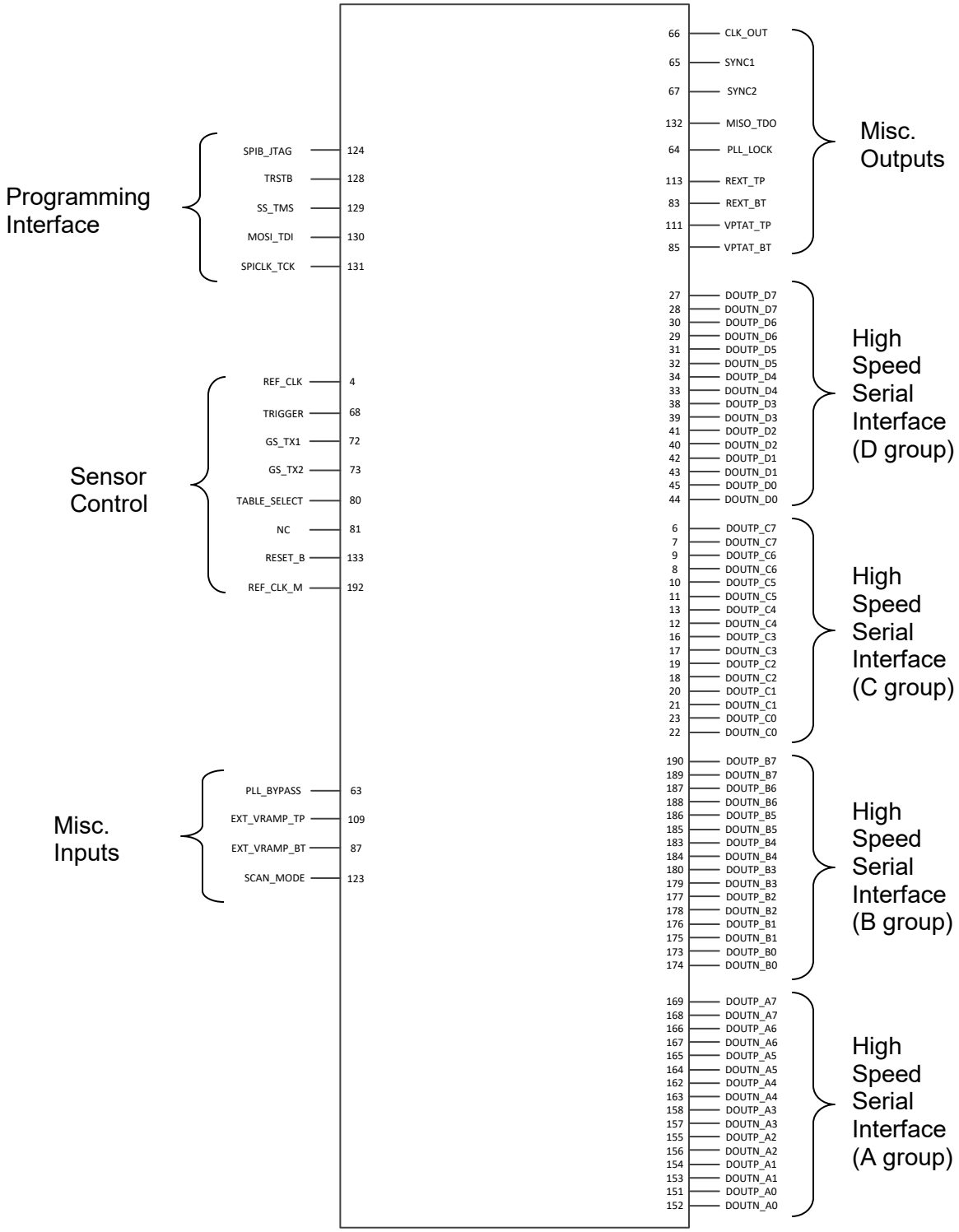


Figure 27. Signal Groups

8.3 Standard Package Pin List

The MST4625A and LTN4625A Standard package image sensors have 194 pins in a CLCC (Ceramic Leadless Chip Carrier) package. The tables shown below provide a complete description of the pin number, pin names and their function. Table 21 shows power and ground pins. Table 22 shows signal pins.

Table 25: Standard Package Pin List (Power and Ground)

Pin number	Pin name	Pin type	Pin description
3, 36, 52, 57, 70, 75, 82, 93, 94, 102, 103, 114, 115, 121, 126, 139, 144, 160, 193	AVDD	Power	AVDD analog supply
50, 146	AVDD_PIX	Power	Pixel source follower supply
47, 149	AVDD2	Power	Low noise column and row supply
14, 25, 37, 58, 78, 95, 101, 118, 138, 159, 171, 182	DVDD	Power	DVDD digital core supply
15, 35, 161, 181	VDD_1V2	Power	SERDES driver power supply
48, 53, 61, 71, 76, 120, 125, 135, 143, 148	VDDM	Power	Shift/Mux power supply
100, 194	VRESET1	Power	Primary pixel reset drain power supply
1, 98	VRESET2	Power	Secondary pixel reset drain power
49, 147	VROW_POS	Power	Row select driver positive supply
2, 96	VRST_POS	Power	Pixel reset gate driver power supply
55, 141	VTX1_POS	Power	TX1 drivers positive supply
54, 142	VTX1_NEG	Power	TX1 drivers negative supply
59, 137	VTX2_POS	Power	TX2 drivers positive supply
60, 136	VTX2_NEG	Power	TX2 drivers negative supply
5, 24, 26, 46, 51, 56, 62, 69, 74, 77, 79, 84, 86, 88, 89, 90, 91, 92, 97, 99, 104, 105, 106, 107, 108, 110, 112, 116, 117, 119, 122, 127, 134,	GND	Ground	GND common ground 0V (SERDES gnd, PLL gnd, digital gnd, I/O gnd, column drivers gnd)

Pin number	Pin name	Pin type	Pin description
140, 145, 150, 170, 172, 191			

Table 26: Standard Package Pin List (Signals)

Pin number	Pin name	Pin type	Pin description	Pin type
124	SPIB_JTAG	input	SPI/JTAG select, scan chain input	CMOS
128	TRSTB	input	Low active JTAG reset The customer should use the SPI communication protocol to read and write to sensor registers, making this pin redundant. Tie this pin to logic 1 so it will not interfere with SPI communication.	CMOS
129	SS_TMS	input	SPI chip enable, JTAG mode select	CMOS
130	MOSI_TDI	input	SPI/JTAG serial input	CMOS
131	SPICLK_TCK	input	SPI/JTAG clock	CMOS
4	REF_CLK	input	Local PLL clock input Recommended input is 39.0625 MHz, sharing a single oscillator with REF_CLK_M	CMOS
68	TRIGGER	input	Trigger mode select	CMOS
72	GS_TX1	input	Global shutter TX1	CMOS
73	GS_TX2	input	Global shutter TX2	CMOS
80	TABLE_SELECT	input	Wavetable select Logic 0 selects wavetable A, logic 1 selects wavetable B	CMOS
133	RESET_B	input	Low active chip reset	CMOS
192	REF_CLK_M	input	Reference clock for PLL synthesizer Recommended input is 39.0625 MHz, sharing a single oscillator with REF_CLK	CMOS
63	PLL_BYPASS	input	PLL bypass mode select	CMOS
109	EXT_VRAMP_TP	input	External Vramp (Top) The customer will almost certainly use the internal Vramp (controlled by Reg 0x24), making this pin irrelevant. Leave as NC (No Connect).	analog

Pin number	Pin name	Pin type	Pin description	Pin type
87	EXT_VRAMP_BT	input	External Vramp (Bottom) The customer will almost certainly use the internal Vramp (controlled by Reg 0x24), making this pin irrelevant. Leave as NC (No Connect).	analog
123	SCAN_MODE	Input	Scan mode select Used for BAE internal testing, customer should tie this pin to ground.	CMOS
64	PLL_LOCK	output	PLL lock output, goes to logic high when the Main PLL is locked	HSTL
65	SYNC1	output	Synchronization output 1	HSTL
66	CLK_OUT	output	Synchronization clock output	HSTL
67	SYNC2	output	Synchronization output 2	HSTL
132	MISO_TDO	output	SPI/JTAG serial output	HSTL
113	REXT_TP	output	External resistor (Top) 12.45 kΩ	analog
83	REXT_BT	output	External resistor (Bottom) 12.45 kΩ	analog
111	VPTAT_TP	output	Temperature sensor (Top) Outputs an analog voltage that varies linearly with temperature with a slope of 6.35mV/°C	analog
85	VPTAT_BT	output	Temperature sensor (Bottom) Outputs an analog voltage that varies linearly with temperature with a slope of 6.35mV/°C	analog
27	DOUTP_D7	output	SERDES channel D7 positive output	SERDES
28	DOUTN_D7	output	SERDES channel D7 negative output	SERDES
30	DOUTP_D6	output	SERDES channel D6 positive output	SERDES
29	DOUTN_D6	output	SERDES channel D6 negative output	SERDES
31	DOUTP_D5	output	SERDES channel D5 positive output	SERDES
32	DOUTN_D5	output	SERDES channel D5 negative output	SERDES
34	DOUTP_D4	output	SERDES channel D4 positive output	SERDES
33	DOUTN_D4	output	SERDES channel D4 negative output	SERDES
38	DOUTP_D3	output	SERDES channel D3 positive output	SERDES
39	DOUTN_D3	output	SERDES channel D3 negative output	SERDES
41	DOUTP_D2	output	SERDES channel D2 positive output	SERDES

Pin number	Pin name	Pin type	Pin description	Pin type
40	DOUTN_D2	output	SERDES channel D2 negative output	SERDES
42	DOUTP_D1	output	SERDES channel D1 positive output	SERDES
43	DOUTN_D1	output	SERDES channel D1 negative output	SERDES
45	DOUTP_D0	output	SERDES channel D0 positive output	SERDES
44	DOUTN_D0	output	SERDES channel D0 negative output	SERDES
6	DOUTP_C7	output	SERDES channel C7 positive output	SERDES
7	DOUTN_C7	output	SERDES channel C7 negative output	SERDES
9	DOUTP_C6	output	SERDES channel C6 positive output	SERDES
8	DOUTN_C6	output	SERDES channel C6 negative output	SERDES
10	DOUTP_C5	output	SERDES channel C5 positive output	SERDES
11	DOUTN_C5	output	SERDES channel C5 negative output	SERDES
13	DOUTP_C4	output	SERDES channel C4 positive output	SERDES
12	DOUTN_C4	output	SERDES channel C4 negative output	SERDES
16	DOUTP_C3	output	SERDES channel C3 positive output	SERDES
17	DOUTN_C3	output	SERDES channel C3 negative output	SERDES
19	DOUTP_C2	output	SERDES channel C2 positive output	SERDES
18	DOUTN_C2	output	SERDES channel C2 negative output	SERDES
20	DOUTP_C1	output	SERDES channel C1 positive output	SERDES
21	DOUTN_C1	output	SERDES channel C1 negative output	SERDES
23	DOUTP_C0	output	SERDES channel C0 positive output	SERDES
22	DOUTN_C0	output	SERDES channel C0 negative output	SERDES
190	DOUTP_B7	output	SERDES channel B7 positive output	SERDES
189	DOUTN_B7	output	SERDES channel B7 negative output	SERDES
187	DOUTP_B6	output	SERDES channel B6 positive output	SERDES
188	DOUTN_B6	output	SERDES channel B6 negative output	SERDES
186	DOUTP_B5	output	SERDES channel B5 positive output	SERDES
185	DOUTN_B5	output	SERDES channel B5 negative output	SERDES
183	DOUTP_B4	output	SERDES channel B4 positive output	SERDES
184	DOUTN_B4	output	SERDES channel B4 negative output	SERDES
180	DOUTP_B3	output	SERDES channel B3 positive output	SERDES
179	DOUTN_B3	output	SERDES channel B3 negative output	SERDES

Pin number	Pin name	Pin type	Pin description	Pin type
177	DOUTP_B2	output	SERDES channel B2 positive output	SERDES
178	DOUTN_B2	output	SERDES channel B2 negative output	SERDES
176	DOUTP_B1	output	SERDES channel B1 positive output	SERDES
175	DOUTN_B1	output	SERDES channel B1 negative output	SERDES
173	DOUTP_B0	output	SERDES channel B0 positive output	SERDES
174	DOUTN_B0	output	SERDES channel B0 negative output	SERDES
169	DOUTP_A7	output	SERDES channel A7 positive output	SERDES
168	DOUTN_A7	output	SERDES channel A7 negative output	SERDES
166	DOUTP_A6	output	SERDES channel A6 positive output	SERDES
167	DOUTN_A6	output	SERDES channel A6 negative output	SERDES
165	DOUTP_A5	output	SERDES channel A5 positive output	SERDES
164	DOUTN_A5	output	SERDES channel A5 negative output	SERDES
162	DOUTP_A4	output	SERDES channel A4 positive output	SERDES
163	DOUTN_A4	output	SERDES channel A4 negative output	SERDES
158	DOUTP_A3	output	SERDES channel A3 positive output	SERDES
157	DOUTN_A3	output	SERDES channel A3 negative output	SERDES
155	DOUTP_A2	output	SERDES channel A2 positive output	SERDES
156	DOUTN_A2	output	SERDES channel A2 negative output	SERDES
154	DOUTP_A1	output	SERDES channel A1 positive output	SERDES
153	DOUTN_A1	output	SERDES channel A1 negative output	SERDES
151	DOUTP_A0	output	SERDES channel A0 positive output	SERDES
152	DOUTN_A0	output	SERDES channel A0 negative output	SERDES

9 Shutter Operation

9.1 Rolling Shutter

Prior to the starting of integration, the pixels are reset one line at a time in a rolling reset operation. At the end of integration, the pixels are read out again one line at a time in a rolling readout operation. The time difference between the reset operation and the readout operation for a line is the integration time for that line. The two operations are the same to the pixel with the exception that for reset operation, no signal value needs to be read out and ADC converted and thus the pixel's floating diffusion does not need to be connected to the column circuitry in a reset operation. This also implies that a readout operation is also a reset operation by nature. Depending on the integration time setting which is done via register programming, both reset operation and readout operation can occur simultaneously but to different rows in the array. Since a row must be reset first and then readout, the integration time is less than or equal to the frame time and is programmed in unit of row time. Long integration can be achieved by (a) increasing the frame time by adding virtual rows, or (b) increasing the row time by changing the number of clocks per row and the wavetable to match the increased row time.

9.1.1 Rolling shutter readout

Rolling shutter is the standard readout method for CMOS image sensors. When RESET_B is de-asserted in rolling shutter mode, one row at a time is sequentially processed until the frame is completely read out. In video readout mode frames are continuously read out, separated only by a programmable frame blanking time. Note that the frame blanking time is determined by the number of pre-scan lines in each image. Readout of each row consists of four separate operations. The first operation is resetting the floating diffusion nodes in each pixel. The second operation is reading the reset voltage out via the source follower transistor in each pixel. The third operation is transferring charge from the pinned photodiode to the floating diffusion node, via TX1, and the last operation is reading out the signal voltage. At the edge of the array, column parallel circuitry amplifies, subtracts, and digitizes the row data. The difference between the reset voltage and the signal voltage is a form of correlated double sampling (CDS). CDS removes kTC, i.e. reset noise on the floating diffusion node, and suppresses the source follower 1/f noise. This readout mode achieves the lowest read noise available for the MST4625A and LTN4625A.

The CDS operation in rolling shutter mode is illustrated in Figure 28. The floating diffusion voltages of rows N-M, N-M+1, and N are shown. The reset sample for each row is S1 and the data sample for each row is S2. The final pixel value is the difference between S2 and S1.

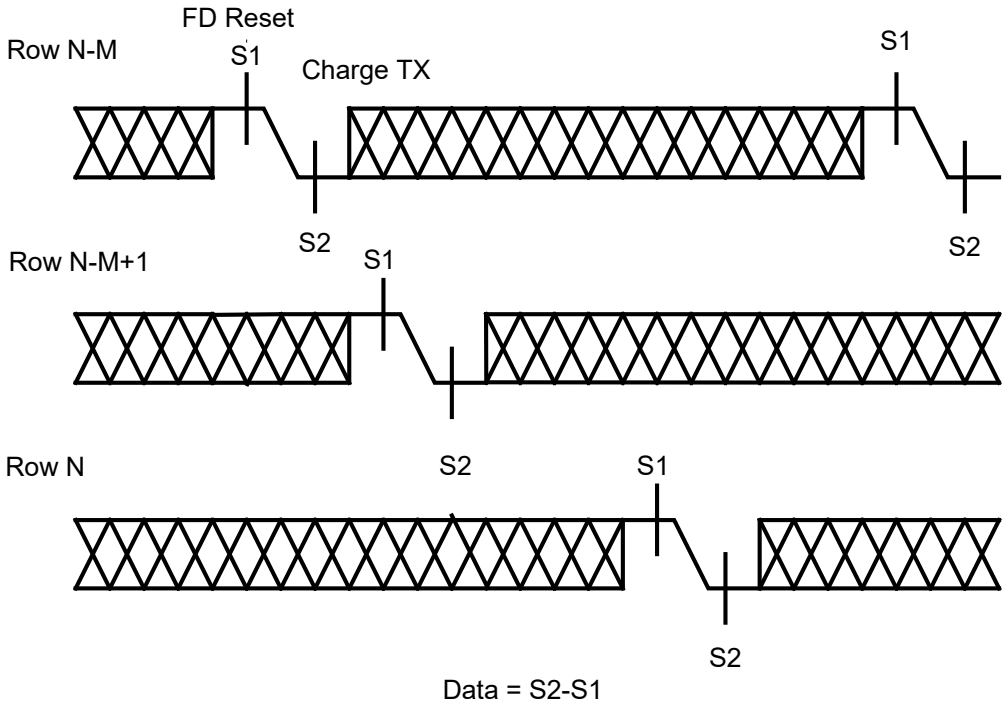


Figure 28. CDS Operation in Rolling Shutter Mode

In Rolling Shutter readout each row in the sensor integrates photo-charge for the same amount of time, but the exact time interval (i.e. integration start and stop points) is different. Moreover, the integration interval for row N+1 is shifted by one line time in comparison to row N.

Figure 30 (on the next page) illustrates this effect.

9.2 Basic Rolling Shutter Mode

The timing for Basic Rolling Shutter Mode is shown in Figure 29.

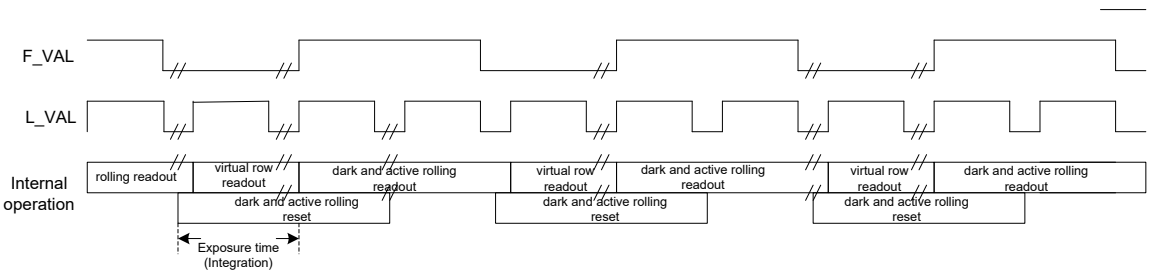


Figure 29: Rolling Shutter Frame Mode

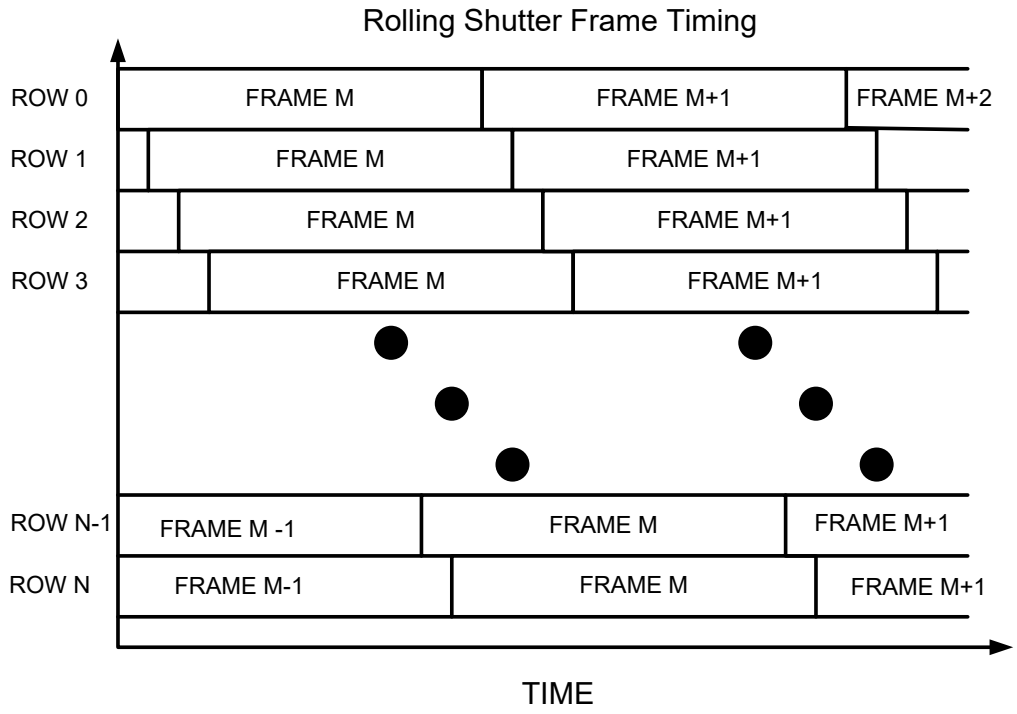
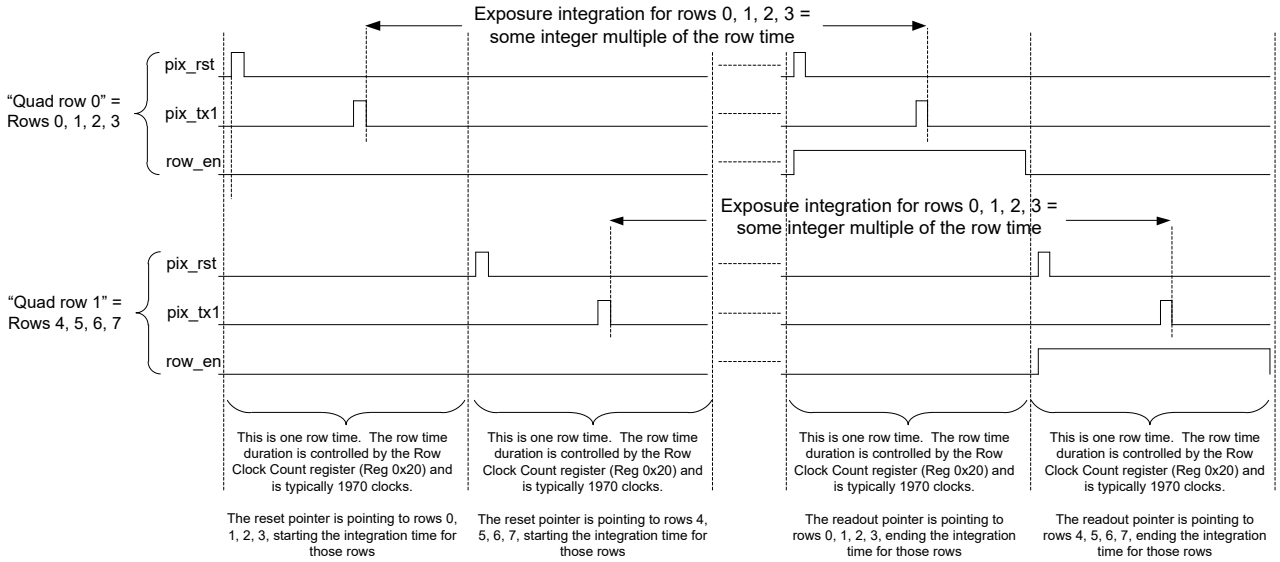


Figure 30. Rolling Shutter Frame Timing

9.2.1 Seamless Change of Integration Time in Rolling Shutter readout

Seamless change of integration time in Rolling Shutter readout mode is implemented on this sensor to allow standard auto-exposure algorithms to be implemented in a camera. This operation is always active in Rolling Shutter readout mode. Seamless change of integration time is implemented in the sensor by forcing the integration time of each row in each frame to be the same. This enables smooth video output when integration time is used as an electronic shutter. See Figure 31.



This diagram shows the Rolling Shutter readout pattern for the 4625 part. It is meant to show that the start and stop times for the integration time of each "quad row" are different even though the magnitude of the integration time will be the same for all pixels in a frame. This is just a typical Rolling Shutter readout:

1) Integration time is initiated by a "Reset pointer" addressing a row and emptying the pixel photodiode and floating diffusion node for each pixel in that row

2) The pixel photodiode for each pixel in this row will then "integrate", collecting photo-electrons until the Readout pointer arrives

3) Integration time comes to an end by the action of the "Readout pointer" addressing a row, measuring the floating diffusion node voltage before and after the tx1 charge transfer

The only unusual factor specific to the 4625 part is that the 4625 part is hardwired to read out 4 rows simultaneously, so the "Reset pointer" points to 4 rows at a time (or one "quad row" at a time) and the "Readout pointer" points to 4 rows at a time (or one "quad row" at a time).

In this example, the VROI of the 4625 is set up so that the first "quad row" consists of rows 0, 1, 2, and 3, the second "quad row" is rows 4, 5, 6, and 7, etc.
Of course, the VROI may be set up to begin the frame on any quad row of the customer's choosing, consistent with the register contents of the VROI settings registers.
The horizontal dashed lines in the center of the above drawing are meant to suggest this timing pattern continuing for additional "quad rows" (not pictured) to complete the frame readout.

Figure 31. Array Rolling Shutter Timing Overview

9.2.2 Rolling Shutter with External Trigger

There are 3 separate rolling shutter external trigger operation modes:

1. External trigger rolling shutter mode 1 (mode register, bit 2 = 0, bit 1, 0 = 01)
2. External trigger rolling shutter mode 2 (mode register, bit 2 = 0, bit 1, 0 = 10)
3. External trigger rolling shutter mode 3 (mode register, bit 2 = 0, bit 1, 0 = 11)

(mode register, bit 2 = 0, bit 1,0 = 00) indicates internal (free running mode.)

The basic rolling shutter mode is extended to be used in external trigger mode. An external pin TRIGGER is sampled internally to be used to control the sensor operation. The sampling point is at the end the line. Upon exit from the reset state (RESET_B = 1 , and mode register bit soft_reset_b), the sensor continuously idles on a virtual row waiting for trigger. The sensor launches the triggered operation when TRIGGER rises. When the operation completes, the sensor returns to idling on a virtual line waiting for the next trigger for the next operation. Triggered operation is defined as going through reading out all the V-ROI regions once in mode 1 to 3 and continuous in mode 4. In external trigger modes, horizontal and vertical ROI changes are not permitted while frames are being processed. Changes are allowed only when the sensor is idle with TRIGGER at 0.

Because of internal address calculation pipeline delay, there is always a fixed 1 line of latency between the sampling event and the launched array operation (pixel array being reset or read).

9.2.3 External Trigger: Rolling Shutter Mode 1

When TRIGGER rises, the sensor launches a rolling pixel reset operation. This rolling pixel reset operation is similar to a rolling readout operation where pix_rst and pix_tx1 are sequentially applied to the selected row by row to clear the floating diffusion and to transfer any accumulated charges thus effectively clearing the pixel. When the rolling reset operation completes, the sensor returns to idling waiting for the next trigger. When the next trigger comes in the form of TRIGGER falls, the sensor launches a rolling pixel readout operation reading the whole array row by. After the readout operation, the sensor returns back to idling waiting for the next trigger on TRIGGER. ROI changes are not allowed between TRIGGER rises and the completion of readout frame as the region being reset must match the region being readout in order to have consistent integration for the whole region.

Even though the starting of integration for each row differs, all rows have the same effective integration time, which is between the time a row is reset to the time the row is read. The time in between the first trigger and the second trigger approximates the integration time. Since rolling reset can be occurring at the same time as a different row is being read, it is not necessary to wait for the rolling reset to complete and to return to idling before the falling trigger is applied. Thus integration time in this mode can be less than a frame time.

Any change in illumination can only be done when the sensor is idling after the first rolling reset and before the start of the second rolling readout operations. This implies that integration time in this case has to be greater than 1 frame time to allow time for the change in illumination.

It is possible to have TRIGGER rises during the time that a readout is still on-going due to an earlier fall of TRIGGER (Scenario B in the following diagram). It is also possible for TRIGGER to fall before the end of the readout due to an earlier fall of TRIGGER (Scenario C in the following diagram), but in this case the integration time is no longer defined by the pulse width of TRIGGER since a new rolling readout cannot start right way until the on-going readout is finished. The integration time is then the time between the rising of TRIGGER and the start of

output (F_VAL rises) less three lines (one line for trigger latency and two lines for data output pipeline latency).

- It is recommended that TRIGGER rises only when readout is idling.
- Recommended minimum TRIGGER high time: 1 line
- Recommended minimum TRIGGER low time: 1 frame

9.2.4 External Trigger Timing Diagram: Mode 1

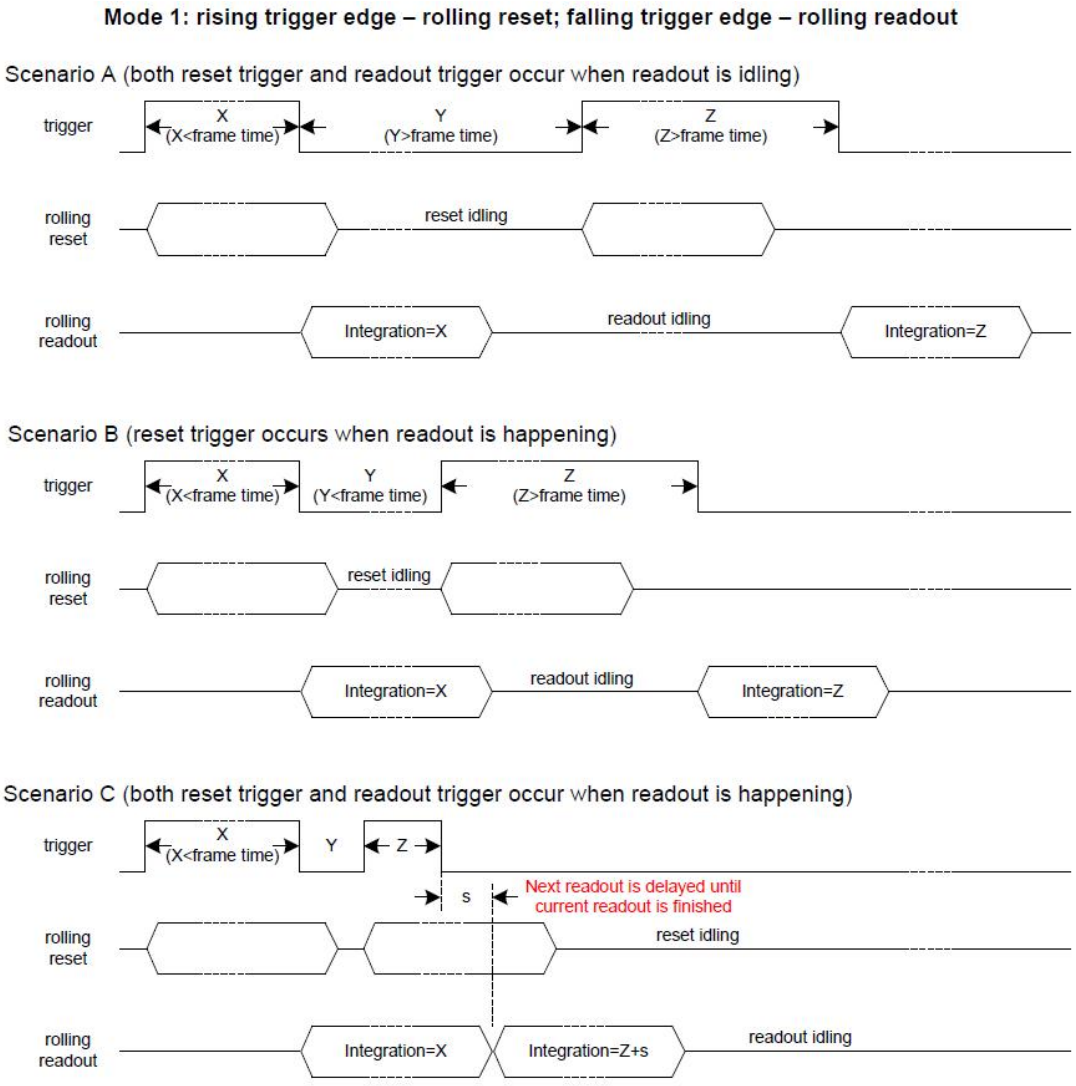


Figure 32. External Trigger Mode 1

9.2.5 External Trigger: Rolling Shutter Mode 2

When TRIGGER rises, the sensor launches a rolling pixel reset and readout operation reading the array row by row and provides a frame of data. When the rolling readout operation completes, the sensor returns to idling waiting for the next trigger. When the next trigger comes in the form of TRIGGER falls, the sensor launches another rolling pixel reset and readout operation reading the array row by row. After the readout operation, the sensor returns back to idling waiting for the next trigger on TRIGGER.

Even though the starting of integration for each row differs, all rows have the same effective integration time which is between the time a row is first read to the time the row is read again. The time in between the first trigger and the second trigger approximates the integration time. Since readout can only be happening to one row at a time, the first readout must be finished before the second readout can start. Thus integration time in this mode has to be greater than one frame time.

Any change in illumination can only be done when the sensor is idling between readouts.

- Recommended minimum TRIGGER high time: 1 frame
- Recommended minimum TRIGGER low time: 1 frame

This mode of operation can be used in conjunction with a user-controlled light source to create a mode of operation called “Global Reset”, in which, because the user-controlled light source is only active when the sensor is not reading out, motion artifacts characteristic of the Rolling Shutter readout mode will not be seen. For more information on Global Reset, contact cams.techsupport@baesystems.com

9.2.6 External Trigger Timing Diagram: Mode 2

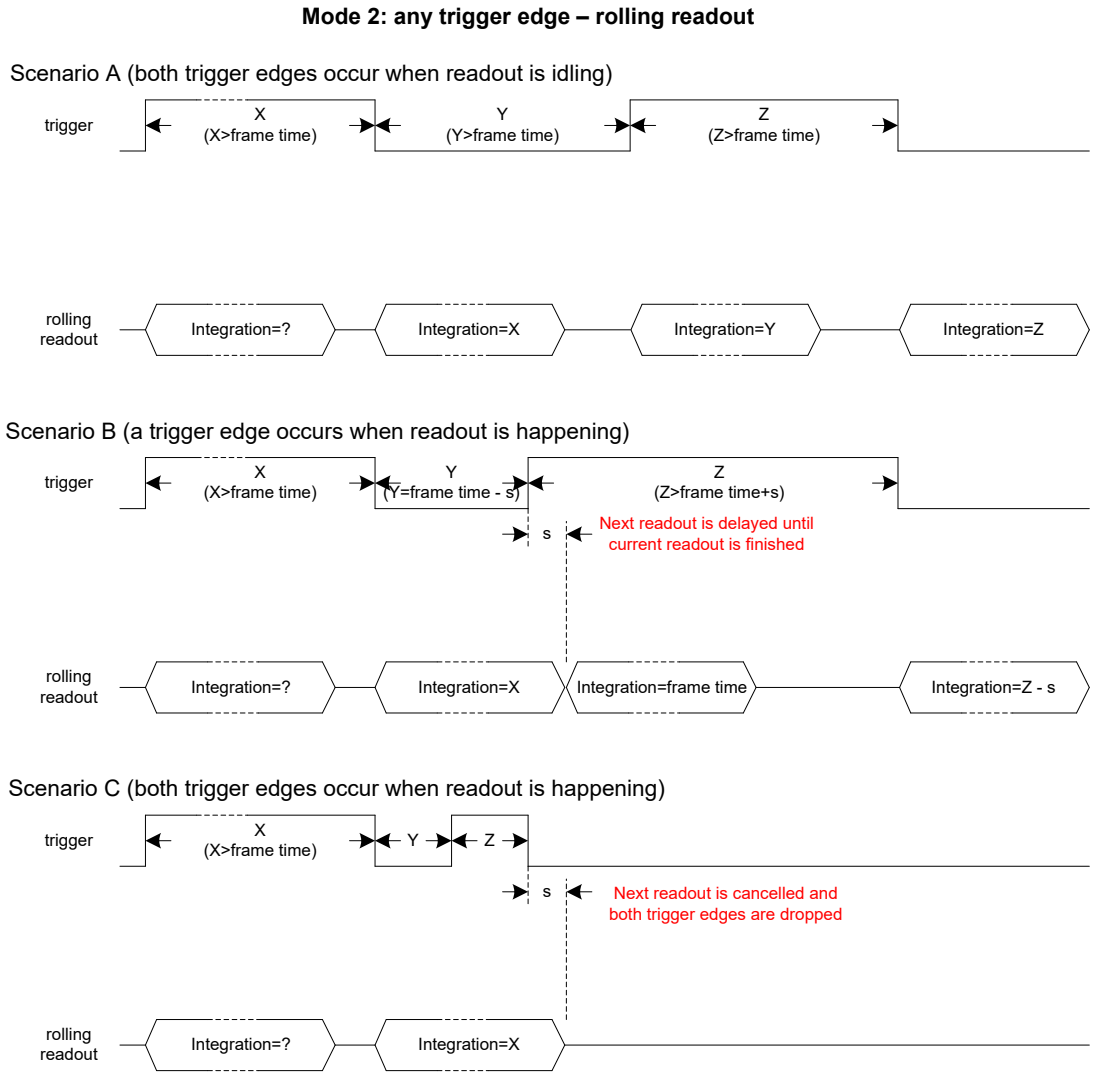


Figure 33. External Trigger Mode 2

9.2.7 External Trigger: Rolling Shutter Mode 3

In this mode, frames are sent as long as the TRIGGER pin remains high. This mode uses the normal mode of operation where the integration time is set by the integration register. When TRIGGER is deasserted, readout completes at the end of the current frame. In this mode, the first frame after TRIGGER rises is blank.

- Recommended minimum TRIGGER high time: 2 frames
- Recommended minimum TRIGGER low time: 2 lines

9.2.8 External Trigger Timing Diagram: Mode 3

Mode 3: rising trigger edge – continuous rolling readout; falling trigger edge – idle

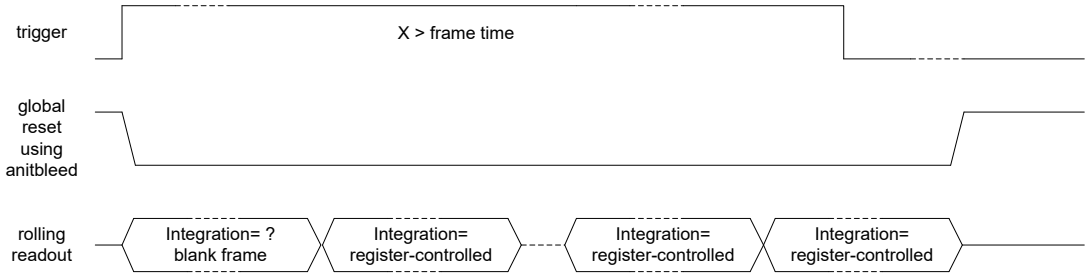


Figure 34. External Trigger Mode 3

9.2.9 External Trigger Timing Specifications

Table 27: Trigger Mode Definitions

Signal	Trigger Mode	Parameter	Description	Minimum	Note
TRIGGER	Mode 1	T_{high}	High Duration	1 line time	
		T_{low}	Low Duration	1 line time	
		T_{period}	Pulse Period	1 frame time + Thigh	
	Mode 2	T_{high}	High Duration	1 frame time	
		T_{low}	Low Duration	1 frame time	
		T_{period}	Pulse Period	2 frame time	
	Mode 3	T_{high}	High Duration	1 frame time + 1 line time	
		T_{low}	Low Duration	1 line time	
		T_{period}	Pulse Period	X frame time + 2 line time	X is an integer

9.3 Basic Global Shutter Mode

Global shutter consists of two different pixel operations. The first operation is called the reference operation. In this operation, the pixel is read out with and without the RST active while TX1 is low globally and TX2 is applied global to control the pixel to either prevent the pixels from integration or allow them to integrate. The two read values (one with RST active and one without) are CDS'ed internal to the sensor to derive a final readout value – the reference value. While the reference operation is going on, TX2 can be released from high to allow the photodiode to start integration for eventual data readout.

The second operation is called the data operation. Prior to the start of this operation (at end of the reference operation), TX1 is applied globally to transfer the integrated charges from the photodiodes to the floating diffusions. In the data operation, the voltage at the floating diffusion with the integrated charges is first readout and then the same floating diffusion is read again with RST active to clear the integrated charges. The two values (one with the integration and the second with RST active) are CDS'ed internal to the sensor to derive a final readout value – the data value.

The reference value is then subtracted from the data value external to the sensor to obtain the final global shutter value. It should be noted that because of the two operations involved in global shutter (reading a frame of reference data and a frame of integrated data), the effective maximum frame rate of global shutter is half of frame rate for rolling shutter.

Note also the sequence order of RST for the two operations. For the reference operation, the sequence order of RST is first active and then inactive for the two readings of the floating diffusion capacitance C_{fd}. For data operation, the sequence order of RST is first inactive and then active for the two readings of C_{fd}. The changing of sequence order is accomplished through the use of different wavetables, typically wavetable A for the reference operation and wavetable B for the data operation. In conjunction to the use of different wavetables, a "cross switch" control is also needed to control the polarity of the CDS operation (see Configuration Register).

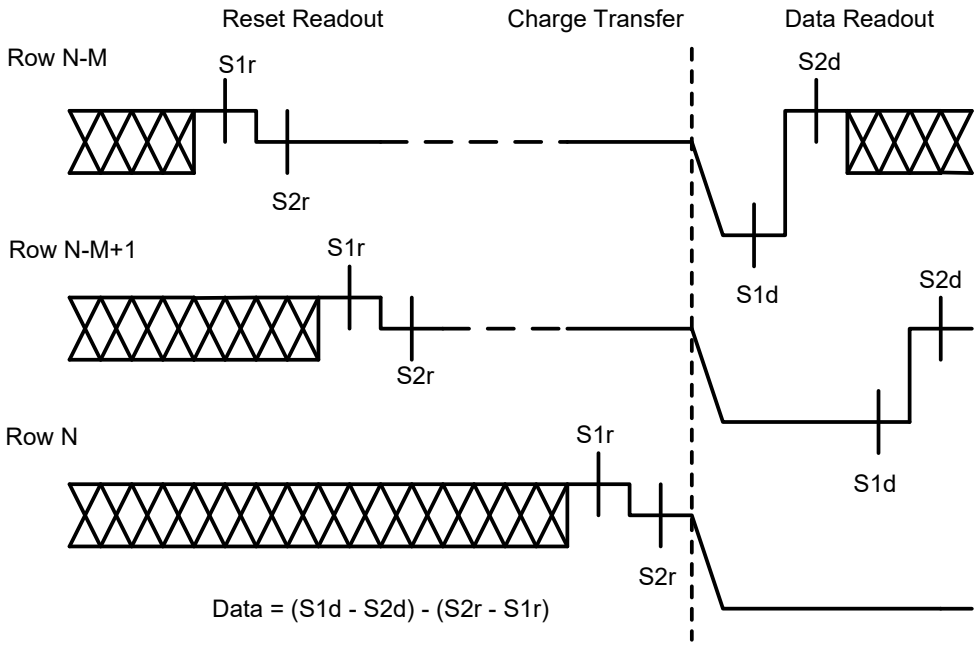


Figure 35. Correlated quadruple sampling operation

9.3.1 Externally Controlled Global Shutter

The activations of TX1, TX2 and the selection of which wavetable to be used are externally controlled via sensor pins, GS_TX1, GS_TX2 and TABLE_SEL. The user first activates GS_TX2 and the wavetable for reference operation. The sensor will carry out the reference operation and continuously output reference values in the form of reference frames. At the appropriate time before the end of the last reference frame taking into account of the sensor internal latency (typically 2 row times), GS_TX2 is de-asserted to allow the sensor to start integration. At the end of the last reference frame (again taking into account the internal latency), GS_TX1 is pulsed to transfer the integrated charges and the TABLE_SEL pin is toggled to select the alternate wavetable for data operation. The data is then read out for the data frame. The external controlled global shutter allows the most flexibility in integration time as the user controls the separation of GS_TX2 and GS_TX1 and not bound by any frame boundaries.

Synchronization of the GS_TX1, GS_TX2 and TABLE_SEL to the sensor's internal operation is keyed to the use external controlled global shutter. Two sensor output pins, SYNC1 and SYNC2 are provided to help the synchronization effort. Two pairs of internal status information are selectable to be output to these pins: 2 sys_clk cycle wide pulse to indicate beginning of last row in a frame on SYNC1 and 2 sys_clk cycle wide pulse to indicate beginning of every row on SYNC2, OR high during the second last row of a frame on SYNC1 and high during the charge sampling time for every row on SYNC2.

9.3.2 Internally Controlled Global Shutter

The externally controlled global shutter has the most flexibility but it requires user manipulation of 3 different pins. The sensor provides an alternate internally controlled global shutter mode which the following limitations:

- integration time is less or equal to frame time
- reference frame and data frame are always in pairs

With the internally controlled global shutter, the sensor computes the appropriate time to assert TX1, TX2, and TABLE_SEL. Integration time is set via register programming.

9.3.3 Global Shutter (External Trigger)

The basic operation of global shutter (external trigger) is similar to that of rolling shutter (external trigger), that is, a rising of TRIGGER launches a rolling read out of a frame while a falling of TRIGGER launches rolling reading of another frame. In external pin control mode, the external pins, GS_TX1, GS_TX2 and TABLE_SEL should be set appropriately so that one of the frames is a reference frame and the other is a data frame. Typically the first frame is the reference frame and the second frame is the data frame. The integration time is controlled by the separation of GS_TX2 and GS_TX1.

Global Shutter External Trigger – Pin Control

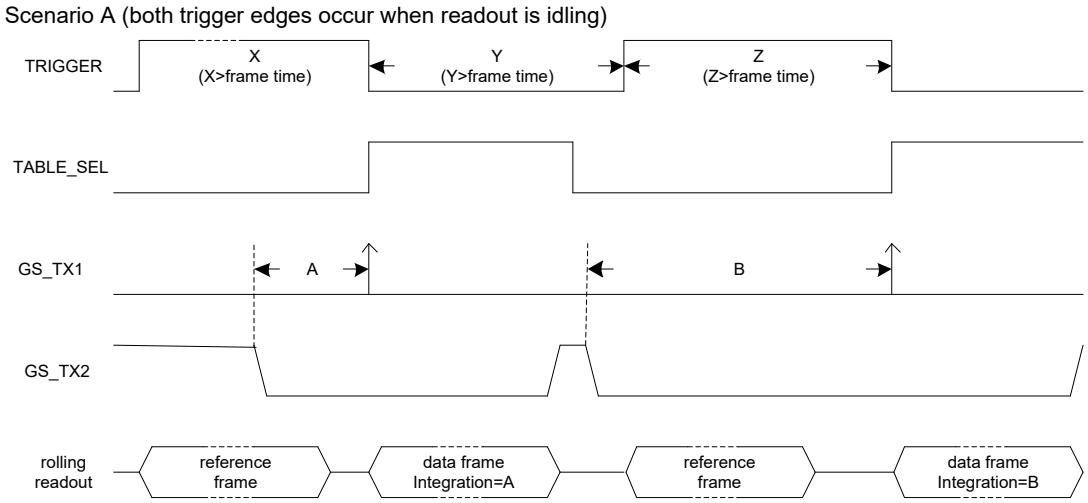


Figure 36. Global Shutter External Trigger -- Pin Controlled

The operation of global shutter using internal control is slightly different. The signals tx1, tx2 and table_sel are generated internally and integration time is controlled by a register.

Global Shutter External Trigger – Internal Control

Scenario A (both trigger edges occur when readout is idling)

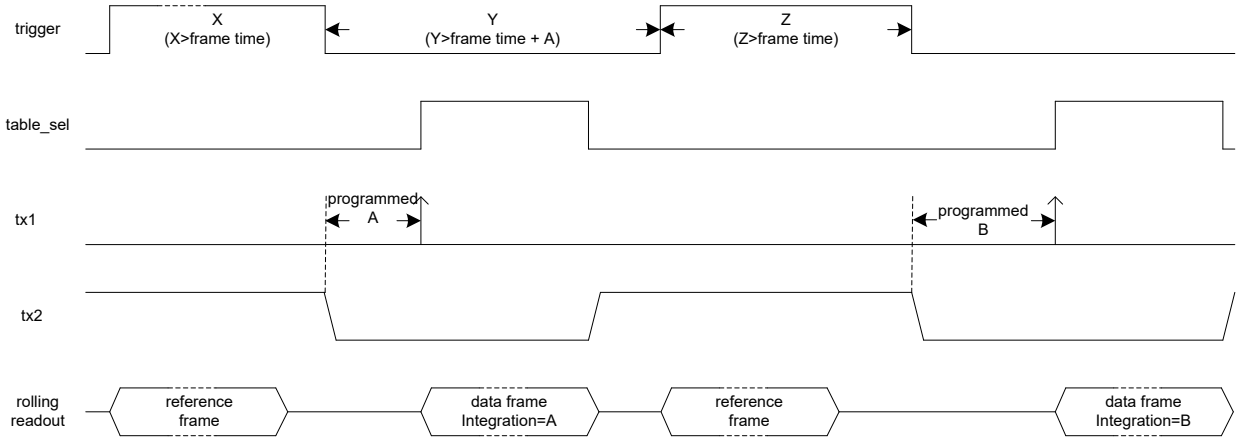


Figure 37. Global Shutter External Trigger -- Internally Controlled

10 Programming Access

Register programming is done via the Serial Peripheral Interface (SPI). SPI is a 4-pin serial-to-parallel programming interface for accessing the internal registers. This interface is activated when SPIB_JTAG is asserted to 0.

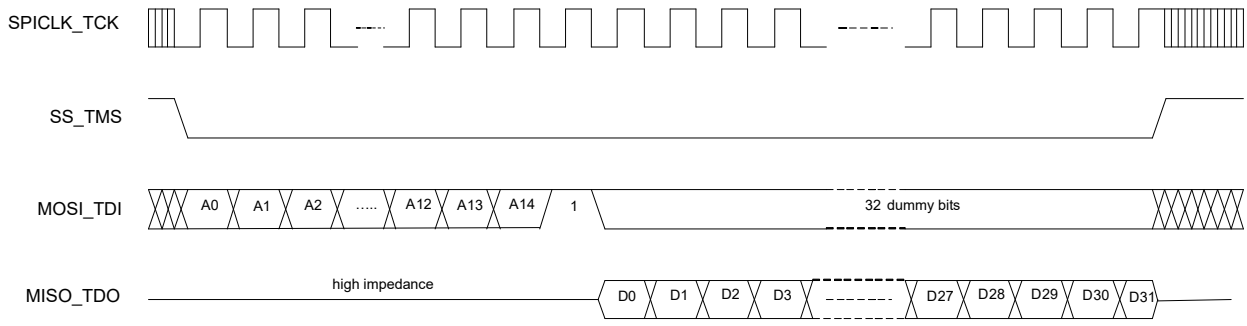
Pin SS_TMS enables the interface for command transaction when asserted to 0 and resets the interface when asserted to 1. Pin SPICLK_TCK is the interface clock. Pin MOSI_TDI is the serial input and pin MISO_TDO is the serial output. The SPICLK_TCK is assumed to not be a free running clock, i.e. the clock is only active while SS_TMS is 0, although the clock may be free running when SS_TMS is not asserted.

A command word consists of 32 bits of data and 16 bits of instruction, which are serially shifted into the interface with LSB first at the rising edge of SPICLK_TCK while SS_TMS is asserted to 0. The first 15 bits are the address for the Sensor register sent to the Sensor. The 16th bit sent sets the direction of the transfer. A 0 indicates the command is a write; so the next 32 bits are sent to the Sensor. The sensor stores the bits to the address sent in the command. If the direction bit is 1, the command is a read and 32 bits are sent from the Sensor. All 32 bits must be sent regardless of how many bits are really used by the register. The extra bits can be of any value for a write. The sensor always sends 0's for unused register bits.

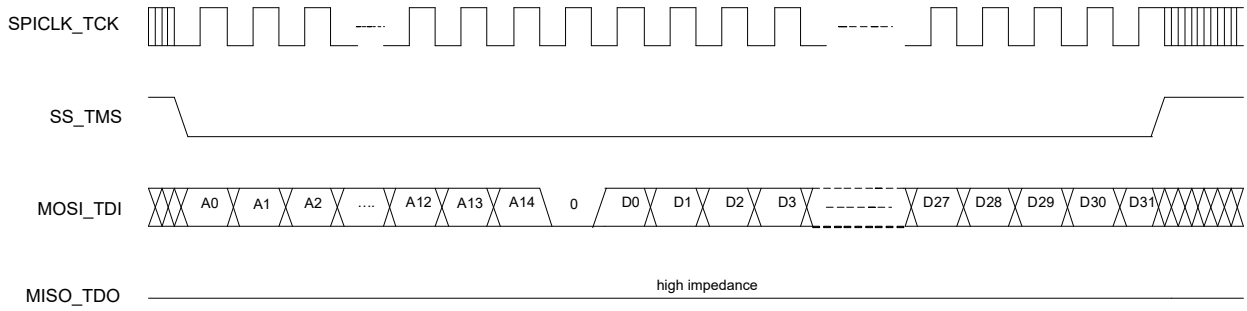
Table 28: Data and Instruction Mapped for SPI

47	46	45	….	18	17	16	15	14	13	….	1	0
Data							Instruction					
D[31]	D[30]	D[29]	….	D[2]	D[1]	D[0]	read=1 write=0	addr[14]	addr[13]	….	addr[1]	addr[0]

There is no restriction to the number of command words in a command transaction. The transaction ends when SS_TMS is asserted to 1 and the interface resets.



SPI Read Operation



SPI Write Operation

Figure 38. SPI Operations

11 Application Examples

11.1 Configuration for different frame rates and Number of TX lanes

The default setting is designed for at full resolution with 240 fps using 8 TX lanes running at 3.125 Gbps rate. It is possible to reduce the use of fewer number TX lanes at reduced frame rate by register programming. The following table describes the support scaling and the corresponding register settings.

Table 29: Example of Frame Rates and Numbers of TX Lanes

TX lanes	Frame rate (fps)	Configuration register [7:5] lane selection	Configuration register [9:8] sys_clk rate	Row clock count	Require changes in wavetable for optimum analog performance?
8 (default)	240 (default)	0 (default: 8 lanes)	0 (default: divided by 1)	default	NO
6	180	1 (6 lanes)	0 (divided by 1)	default + (col_size/8)	YES
4	120	2 (4 lanes)	1 (divided by 2)	default	NO
3	90	3 (3 lanes)	1 (divided by 2)	default + (col_size/8)	YES
2	60	4 (2 lanes)	2 (divided by 4)	default	NO
1	30	5 (1 lane)	3 (divided by 8)	default	NO

Some of the above configurations are not linear scalable from 240fps and thus require lengthening the row time by changing the row clock count register and associated wavetable.

11.2 Activation and Deactivation of PLL Bypass

When PLL bypass is activated, both the main PLL and the PLLs that control the TX lanes are placed into bypass. The fixed ratio divider between the PLL high frequency output and the low frequency output of 10 no longer applies. Therefore in order to maintain proper operation with TX lanes, the REF_CLK supplying the main PLL must be 10X slower than the REF_CLK going to the TX PLLs. This can be achieved by supplying two different frequency reference clocks to REF_CLK and REF_CLK_M.

To place the PLLs into bypass,

1. Assert soft reset by programming the Soft Reset Register bit 0 to 1.
2. Activate the bypass of the PLLs by either programming PLL Configuration Register bit 10 to 1 or assert the PLL_BYPASS pin to 1.
3. Release soft reset by programming the Soft Reset Register bit 0 to 0.

To bring PLLs out of bypass,

1. Assert soft reset by programming the Soft Reset Register bit 0 to 1.
2. De-assert the bypass of the PLLs by programming PLL Configuration Register bit 10 to 0 if it has been set and de-assert PLL_BYPASS pin to 0 if it has been asserted.
3. Release soft reset by programming the Soft Reset Register bit 0 to 0.

12 MST4625A and LTN4625A Register List

NOTE: The Default register values listed in the descriptions below are NOT the Optimized register settings. They are “default” in the sense that they are the values that are automatically loaded when the sensor is powered on, not in the sense that they are the expected best values for sensor operation. Please contact your BAE sales manager to make sure you have the latest Optimized register settings.

Table 30: Register List

Address	Register	Address	Register
0x0	Mode Register	0x24	Ramp Control
0x1	Configuration Register	0x25	Low Power Mode
0x2	Soft Reset Register	0x26	PLL Configuration
0x3	Context Register	0x27	Output Test Pattern
0xe	Chip Status	0x28	Column Segment Power Enable
0xf	Chip ID	0x29	TX Lane Configuration
0x10	HROI-A End Address	0x2a	Injection DAC Control
0x11	VROI1-A Start/End Address	0x2b	Debug
0x12	VROI2-A Start/End Address	0x2c	Column BIST Error Data 0
0x13	VROI3-A Start/End Address	0x2d	Column BIST Error Data 1
0x14	VROI4-A Virtual Row Size	0x2e	Column BIST Error Data 2
0x15	Integration CTRL-A	0x2f	Column BIST Error Data 3
0x16	HROI-B End Address	0x30	TX Data Invert
0x17	VROI1-B Start/End Address	0x40	Waveform Enable 0
0x18	VROI2-B Start/End Address	0x41	Waveform Enable 1
0x19	VROI3-B Start/End Address	0x42	Waveform Enable 2
0x1a	VROI4-B Virtual Row Size	0x43	Waveform Doubling

0x1b	Integration CTRL-B	0x44	Waveform Init 0
0x20	Row Clock Count	0x45	Waveform Init 1
0x21	Row Control Configuration	0x46 -> 0xa5	Wave Time 1A
0x22	Column Control Configuration	0xa6 -> 0x105	Wave Time 1B
0x23	Electrical Dark Config		

At power up, all registers are hardwired to auto-populate with default values. These default values are shown in the tables on pages 74 to 137. Contact BAE for Recommended Register Settings which may be different from the default values.

12.1 Mode Register

Name: modeReg Addr: 0x0 Reset: 0x00000000
Description: Mode register.

Bits	Default	Read / Write	Description
31:4	28'h0	r/o	Reserved
3	1'h0	r/w	Low power enable, active high, when high then the Low Power (lowPwrModeReg) register operation will take effect.
2	1'h0	r/w	Shutter Modes (See Note 1): 1'd0: Rolling Shutter. 1'd1: Global Shutter.
1:0	2'h0	r/w	Operating Modes (See Note 1): For Rolling Shutter Mode: Modes 1-3 wait till an edge of the TRIGGER pin occurs. Modes 1-2 produce one frame (reset or readout) for each edge of the TRIGGER pin. 2'd0: Sets internal trigger mode, ignores TRIGGER pin. 2'd1: Mode 1, TRIGGER pin rising edge -> rolling reset TRIGGER pin falling edge -> rolling readout. 2'd2: Mode 2, TRIGGER pin rising edge -> rolling reset & rolling readout TRIGGER pin falling edge -> rolling reset & rolling

Bits	Default	Read / Write	Description
			readout. 2'd3: Mode 3, TRIGGER pin rising edge -> frames are continuously processed the same as internal mode. TRIGGER pin falling edge -> at the end of the current frame image processing stops. For Global Shutter Mode: Modes 2-3 wait till an edge of the TRIGGER pin occurs 2'd0: External controlled (GS_TX1, GS_TX2, TABLE_SEL) global shutter 2'd1: Internal controlled global shutter 2'd2: External triggered and controlled (TRIGGER, GS_TX1, GS_TX2, TABLE_SEL) global shutter 2'd3: External triggered (TRIGGER) and internal controlled global shutter

Note 1 - Operating mode changes should only be done when soft reset is enabled.

12.2 Configuration Register

Name: configReg Addr: 0x1 Reset: 0x00000007
Description: Configuration register.

Bits	Default	Read / Write	Description
31:16	16'h0	r/o	Reserved
15:13	3'h0	r/w	Global Shutter internal tx2 pulsing options. (Note 3) 1'h0: tx2 is static 1 when sensor is not integrating, 1'h1: tx2 pulses every line when sensor is not integrating, 1'h2: tx2 pulses once every two lines when sensor is not integrating, 1'h3: tx2 pulses once every four lines when sensor is not integrating, 1'h4: tx2 pulses once every eight lines when sensor is not integrating, 1'h5: tx2 pulses once every sixteen lines when sensor is not integrating,

<table>
<tr><th>Bits</th><th>Default</th><th>Read / Write</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>1'h6: tx2 pulses once every thirty-two lines when sensor is not integrating,
1'h7: tx2 pulses once every sixty-four lines when sensor is not integrating.</td></tr>
<tr><td>12:11</td><td>2'h0</td><td>r/w</td><td>CDS cross switch control. Cross switch is used in the column amplifier to control the polarity of the CDS operation of the two sampled value, S1 sample and S2 sample.
2'h0: defined by wavetable usage. Wavetable A: (S2_sample-S1_sample). Wavetable B: (S1_sample-S2_sample)
2'h1: defined by wavetable usage. Wavetable A: (S1_sample-S2_sample). Wavetable B: (S2_sample-S1_sample)
2'h2: (S2_sample-S1_sample)
2'h3: (S1_sample-S2_sample)
Typically, value of 0 is used by global shutter where wavetable A for reference frame and wavetable B for data frame,
and by rolling shutter where only wavetable A is used. Value of 1 is complement of value 0. Value of 2 is used by rolling
shutter using both wavetables. Value of 3 is only used for internal testing.</td></tr>
<tr><td>10</td><td>1'h0</td><td>r/w</td><td>SYNC output configuration.
<table>
<tr><td>Bit 10 value</td><td>SYNC1</td><td>SYNC2</td></tr>
<tr><td>0</td><td>2 sys_clk cycle pulse at the beginning of the last row (real or virtual) of a frame being read out to indicate the end of frame.</td><td>2 sys_clk cycle pulse at the beginning of every row (real or virtual)</td></tr>
<tr><td>1</td><td>High for the duration when the second to last row (real or virtual) of a frame is being read out.</td><td>High during the time that the pixel is being sampled for every row.</td></tr>
</table></td></tr>
<tr><td>9:8</td><td>2'h0</td><td>r/w</td><td>Selects the sys_clk divider ratio from pll_clk. This setting is dependent
on the number of TX lanes in use. (Note 4)</td></tr>
</table>

Bits	Default	Read / Write	Description
			2'h0: divides pll_clk by 1, valid for 8,6,4,3,2,1 TX lane used 2'h1: divides pll_clk by 2, valid for 4,3,2,1 TX lane used 2'h2: divides pll_clk by 4, valid for 2,1 TX lane used 2'h3: divides pll_clk by 8, valid for 1 TX lane used
7:5	3'h0	r/w	Selects the number of TX lanes for transmission (Note 2) 2'h0: 8 lanes per row with total of 32 lanes 2'h1: 6 lanes per row with total of 24 lanes 2'h2: 4 lanes per row with total of 16 lanes 2'h3: 3 lanes per row with total of 12 lanes 2'h4: 2 lanes per row with total of 8 lanes 2'h5: 1 lanes per row with total of 4 lanes
4	1'h0	r/w	Black sun correction enable, active high, when high: 1) The voltage reference level for the analog black sun correction circuit is enabled. The analog black sun correction circuit protects the LG channel by comparing the voltage of the bitline prior to the TX1 charge transfer to a programmable voltage reference level. If the bitline dips below this level, the analog black sun circuit causes the LG ADC output to go to full scale (0x7FF) 2) The digital black sun correction circuit is enabled When enabled, the HG values will be forced to full scale (7FF) when the LG value is full scale. (The analog black sun correction is done on the LG channel only, and the digital black sun correction is done on the HG channel only.) See Figure 39
3	1'h0	r/w	Suppress inside active region bleeding in rolling shutter large frames and short exposure situation when high. Rolling shutter anti-bleed enable bit must be 1 also.
2	1'h1	r/w	Rolling shutter anti-bleed enable, active high, when high enable rolling shutter anti-bleeding.
1	1'h1	r/w	F_VAL suppression, active high, when active F_VAL (frame) is suppressed for one frame after ROI change or coming out of reset (blank_ena).

Bits	Default	Read / Write	Description
0	1'h1	r/w	Miscellaneous sensor output enable, active high, when high enables SYNC1, SYNC2, PLL_LOCK outputs.

Note 1: All configuration changes should be made when soft reset is asserted.

Note 2: The number of clocks per row (row clock count) is dependent on both tx lane width and sys_clk divider ratio. The multiplier for row clock count is (8 * sys_clk_div_ratio)/lane_width and the result must be greater or equal to 1. For example, for divided by 2, the sys_clk_div_ratio is 1/2.

Note 3: Only value 0 and 1 are supported for External triggered internal controlled global shutter (mode register bit [2:0] is 111). Other values are invalid for this mode.

Note 4: Changing sys_clk rate may cause corrupt pixel data in the first frame after the change as the analog circuits sync up with the new frequency. This side effect is mitigated if the change is done in soft reset and with blank_ena enabled as the first frame after soft reset is suppressed (blanked).

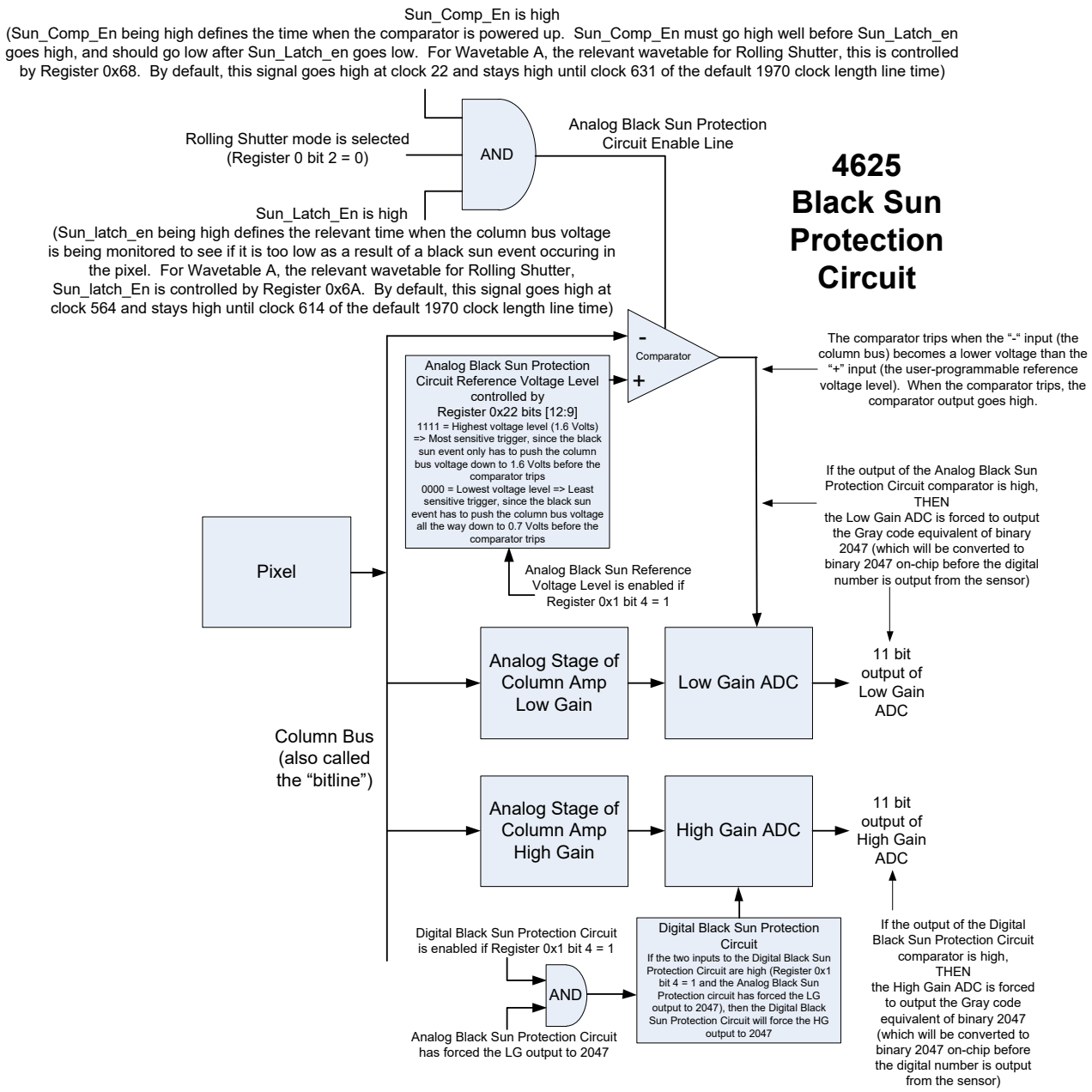


Figure 39. 4625 Analog and Digital Black Sun Protection Circuits

12.3 Soft Reset Register

Name: softResetReg Addr: 0x2 Reset: 0x00000000
Description: Soft Reset register.

Bits	Default	Read / Write	Description
31:1	31'h0	r/o	Reserved
0	1'h0	r/w	Soft reset register 1'h0: Soft reset inactive. 1'h1: Soft reset active. When this bit is set active, sensor is placed in reset state while maintaining all register contents.

12.4 Context Register

Name: contextSwitchReg Addr: 0x3 Reset: 0x00000001
Description: Context register.

Bits	Default	Read / Write	Description
31:1	31'h0	r/o	Reserved
0	1'h1	r/w	Context switch register, sets the ROI context to the A or B: 1'h0: Select context B register set. 1'h1: Select context A register set. When this bit is changed, the vertical and horizontal ROIs, and the integration time registers will switch to the new setting at the beginning of the next frame.

12.5 Chip Status

Name: chipStatusReg Addr: 0xe Reset: 0x00000000
Description: The chip status register contains various read only status bits (See Note 1).

Bits	Default	Read / Write	Description
31:9	23'h0	r/o	Reserved
8	1'h0	r/o	Duty Cycle Corrector Lock.
7	1'h0	r/o	First pixel row in a frame is being accessed for read operation.
6	1'h0	r/o	Last row in a frame (virtual or real) is being accessed for read operation.
5:3	3'h0	r/o	Power management sequencer state machine, state machine which governs the sequencing of the on chip power regulation: 3'h0: Power management reset state. 3'h1: Power management PLL wait state. 3'h2: Bypass wait state. 3'h4: Soft reset deassertion wait state 1. 3'h5: Soft reset deassertion wait state 2. 3'h7: Normal operation state. 3'h3,3'h6: Unused.
2	1'h0	r/o	Trigger idle when in external trigger mode: 1'h0: Means the trigger action is idle. 1'h1: Means the external trigger was received and the trigger action is taking place.
1	1'h0	r/o	Main PLL lock, active high, high means the Main PLL is locked to the reference clock.
0	1'h0	r/o	TX PLL lock, active high, high means the TX PLL is locked to the reference clock.

Note 1 - Read operation is asynchronous to the event being read.

12.6 Chip ID

Name: chipIdReg Addr: 0xf Reset: 0x15211013
Description: The chip id register contains the product family code and revision id.

Bits	Default	Read / Write	Description
31:26	6'h5	r/o	Product family code has the following description: 6'h5: Maestro / Lightning
25:12	14'h1211	r/o	Product part number coded in binary. 0x1121 = 4625
11:8	4'h0	r/o	Variant part number: 4'h0: Front side illumination.
7:4	4'h1	r/o	Major revision number indicates the number of all layer respins.
3:0	4'h3	r/o	Minor revision number indicates the number of metal only respins.

12.7 HROI-A End Address

Name: hroiAAddrReg Addr: 0x10 Reset: 0x000000c2
Description: Horizontal right edge cropping address for context A.

Bits	Default	Read / Write	Description
31:8	24'h0	r/o	Reserved
7:0	8'hc2	r/w	Horizontal right edge cropping address in the range of 0 to 194 and in units of 24 columns, takes effect on the next valid frame. The total number of columns accessed is (value + 1) * 24. Columns that are greater than the array width have pixel values of 0. Columns that are disabled will have pixel values of all 1.

12.8 VROI1-A Start/End Address

Name: vroi1AAddrReg Addr: 0x11 Reset: 0x00100001
Description: Vertical ROI 1 start/end address for context A.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI1 enable, active high, high enables VROI1 rows, takes effect on the next valid frame.
19:10	10'h0	r/w	VROI1 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h1	r/w	VROI1 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI1 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.9 VROI2-A Start/End Address

Name: vroi2AAddrReg Addr: 0x12 Reset: 0x00100e92
Description: Vertical ROI 2 start/end address for context A.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI2 enable, active high, high enables VROI2 rows, takes effect on the next valid frame.
19:10	10'h3	r/w	VROI2 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h292	r/w	VROI2 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI2 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.10 VROI3-A Start/End Address

Name: vroi3AAddrReg Addr: 0x13 Reset: 0x001a5295
Description: Vertical ROI 3 start/end address for context A.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI3 enable, active high, high enables VROI3 rows, takes effect on the next valid frame.
19:10	10'h294	r/w	VROI3 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h295	r/w	VROI3 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI3 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.11 VROI4-A Virtual Row Size

Name: vroi4ASizeReg Addr: 0x14 Reset: 0x00000000
Description: Vertical ROI 4 virtual row size for context A.

Bits	Default	Read / Write	Description
31:18	14'h0	r/o	Reserved
17:0	18'h0	r/w	VROI4 virtual row size in the range of 0 to 262,143 in units of 4 rows, takes effect on the next valid frame.

12.12 Integration CTRL-A

Name: integATimeReg Addr: 0x15 Reset: 0x00000000
Description: Integration time control register for context A.

Bits	Default	Read / Write	Description
31:18	14'h0	r/o	Reserved
17:0	18'h0	r/w	Integration time control register, controls the amount of integration in units of 4 rows. For rolling shutter mode, maximum value is the number of quad-rows in a frame minus 1, and 0 represents a full frame exposure. For global shutter mode 1 (non-triggered internal controlled global shutter), minimum allowable value is 1 and maximum allowable value is frame minus 1. For global shutter mode 3 (external triggered internal controlled global shutter), minimum allowable value is 1 and maximum allowable value is full size of the field. This takes effect on the next valid frame

12.13 HROI-B End Address

Name: hroiBAddrReg Addr: 0x16 Reset: 0x000000c2
Description: Horizontal right edge cropping address for context B.

Bits	Default	Read / Write	Description
31:8	24'h0	r/o	Reserved
7:0	8'hc2	r/w	Horizontal right edge cropping address in the range of 0 to 194 and in units of 24 columns, takes effect on the next valid frame. The total number of columns accessed is (value + 1) * 24. Columns that are greater than the array width have pixel values of 0. Columns that are disabled will have pixel values of all 1.

12.14 VROI1-B Start/End Address

Name: vroi1BAddrReg Addr: 0x17 Reset: 0x00100001
Description: Vertical ROI 1 start/end address for context B.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI1 enable, active high, high enables VROI1 rows, takes effect on the next valid frame.
19:10	10'h0	r/w	VROI1 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h1	r/w	VROI1 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI1 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.15 VROI2-B Start/End Address

Name: vroi2BAddrReg Addr: 0x18 Reset: 0x00100e92
Description: Vertical ROI 2 start/end address for context B.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI2 enable, active high, high enables VROI2 rows, takes effect on the next valid frame.
19:10	10'h3	r/w	VROI2 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h292	r/w	VROI2 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI2 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.16 VROI3-B Start/End Address

Name: vroi3BAddrReg Addr: 0x19 Reset: 0x001a5295
Description: Vertical ROI 3 start/end address for context B.

Bits	Default	Read / Write	Description
31:21	11'h0	r/o	Reserved
20	1'h1	r/w	VROI3 enable, active high, high enables VROI3 rows, takes effect on the next valid frame.
19:10	10'h294	r/w	VROI3 start address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.
9:0	10'h295	r/w	VROI3 end address in the range of 0 to 662 in units of 4 rows, takes effect on the next valid frame.

Note: VROI3 End Address is allowed to be less than, greater than or equal to the Start Address. Direction of scanning is always from start to end.

12.17 VROI4-B Virtual Row Size

Name: vroi4BSizeReg Addr: 0x1a Reset: 0x00000000
Description: Vertical ROI 4 virtual row size for context B.

Bits	Default	Read / Write	Description
31:18	14'h0	r/o	Reserved
17:0	18'h0	r/w	VROI4 virtual row size in the range of 0 to 262,143 in units of 4 rows, takes effect on the next valid frame.

12.18 Integration CTRL-B

Name: integBTimeReg Addr: 0x1b Reset: 0x00000000
Description: Integration time control register for context B.

Bits	Default	Read / Write	Description
31:18	14'h0	r/o	Reserved
17:0	18'h0	r/w	Integration time control register, controls the amount of integration in units of 4 rows. For rolling shutter mode, maximum value is the number of quad-rows in a frame minus 1, and 0 represents a full frame exposure. For global shutter mode 1 (non-triggered internal controlled global shutter), minimum allowable value is 1 and maximum allowable value is frame minus 1. For global shutter mode 3 (external triggered internal controlled global shutter), minimum allowable value is 1 and maximum allowable value is full size of the field. This takes effect on the next valid frame

12.19 Row Clock Count

Name: rowClkCountReg Addr: 0x20 Reset: 0x000007b2
Description: Row clock count register.

Bits	Default	Read / Write	Description
31:16	16'h0	r/o	Reserved
15:0	16'h7b2	r/w	The row clock count register holds the number of SYS_CLK counts for 1 quad-row time (See Note 2).

Note 1: The row clock count should only be changed when soft reset is asserted.

Note 2: The formula for calculating the row clock count value is ((SYS_CLK/fps)/rows) and where SYS_CLK is the sys_clk frequency in Hertz and with dividing ratio of 1 from pll_clk and where rows is the number of rows in a frame divided by 4. The result must be an even number. Another factor to consider is the amount of time to get a row of pixel data off chip with adequate time.

In serial operation, the number of clocks per row (row clock count) is dependent of both tx lane width and sys_clk divider ratio.

The multiplier for row clock count is (8 *sys_clk_div_ratio)/lane_width and the result must be greater or equal to 1. For example, for divided by 2, the sys_clk_div_ratio is 1/2.

12.20 Row Control Configuration

Name: rowConfigReg Addr: 0x21 Reset: 0x000001d5
Description: Row control configuration register.

Bits	Default	Read / Write	Description
31:9	23'h0	r/o	Reserved
8	1'h1	r/w	Enable 2V analog regulator, active high, when high enable the voltage regulator.
7	1'h1	r/w	Enable reset bias, active high, when high enable reset bias (See Note 2).
6	1'h1	r/w	Enable tx bias, active high, when high enable tx bias (See Note 2).
5:4	2'h1	r/w	Reset speed (RST_SPEED), sets the reset falling transition slew rate to: 2'h0 : 3000ns 2'h1 : 680ns 2'h2 : 460ns (Fairchild's PEK camera uses this option) 2'h3 : 220ns
3:2	2'h1	r/w	Tx1 speed (TX1_SPEED), sets the tx1 transition slew rate to: 2'h0 : 400ns (Fairchild's PEK camera uses this option) 2'h1 : 300ns 2'h2 : 200ns 2'h3 : 100ns
1:0	2'h1	r/w	Tx2 speed (TX2_SPEED), sets the tx2 transition slew rate to: 2'h0 : 400ns 2'h1 : 300ns 2'h2 : 200ns 2'h3 : 100ns (Fairchild's PEK camera uses this option)

Note 1: Row control configuration should only be changed when soft reset is asserted.

Note 2: This enable bit is combined with control from the Low Power (lowPwrModeReg) Register. A deassertion from either source will cause the disabling of the circuit.

12.21 Column Control Configuration

Name: colConfigReg Addr: 0x22 Reset: 0x00f0ee05
Description: Column control configuration register.

<table>
<tr><th>Bits</th><th>Default</th><th>Read / Write</th><th>Description</th></tr>
<tr><td>31:24</td><td>8'h0</td><td>r/o</td><td>Reserved</td></tr>
<tr><td>23</td><td>1'h1</td><td>r/w</td><td>Enable VPIXG, active high, high enables VPIX_GATE regulator (See Note 2).</td></tr>
<tr><td>22:17</td><td>6'h38</td><td>r/w</td><td>Select VPIXG voltage with 31.2mV step (note the default value is out of range it needs to be reprogrammed to the desired value):
6'h0-6'h2: Unused.
6'h3: 1.420V.
6'h4: 1.4512.
…
6'h36: 3.01V.
6'h37-6'h3f: Unused.
<table>
<tr><th>Hex value</th><th>VPIXG</th><th>Hex value</th><th>VPIXG</th><th>Hex value</th><th>VPIXG</th></tr>
<tr><td>3</td><td>1.42</td><td>15</td><td>1.9816</td><td>27</td><td>2.5432</td></tr>
<tr><td>4</td><td>1.4512</td><td>16</td><td>2.0128</td><td>28</td><td>2.5744</td></tr>
<tr><td>5</td><td>1.4824</td><td>17</td><td>2.044</td><td>29</td><td>2.6056</td></tr>
<tr><td>6</td><td>1.5136</td><td>18</td><td>2.0752</td><td>2A</td><td>2.6368</td></tr>
<tr><td>7</td><td>1.5448</td><td>19</td><td>2.1064</td><td>2B</td><td>2.668</td></tr>
<tr><td>8</td><td>1.576</td><td>1A</td><td>2.1376</td><td>2C</td><td>2.6992</td></tr>
<tr><td>9</td><td>1.6072</td><td>1B</td><td>2.1688</td><td>2D</td><td>2.7304</td></tr>
<tr><td>A</td><td>1.6384</td><td>1C</td><td>2.2</td><td>2E</td><td>2.7616</td></tr>
<tr><td>B</td><td>1.6696</td><td>1D</td><td>2.2312</td><td>2F</td><td>2.7928</td></tr>
<tr><td>C</td><td>1.7008</td><td>1E</td><td>2.2624</td><td>30</td><td>2.824</td></tr>
<tr><td>D</td><td>1.732</td><td>1F</td><td>2.2936</td><td>31</td><td>2.8552</td></tr>
<tr><td>E</td><td>1.7632</td><td>20</td><td>2.3248</td><td>32</td><td>2.8864</td></tr>
<tr><td>F</td><td>1.7944</td><td>21</td><td>2.356</td><td>33</td><td>2.9176</td></tr>
<tr><td>10</td><td>1.8256</td><td>22</td><td>2.3872</td><td>34</td><td>2.9488</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bits</th><th>Default</th><th>Read / Write</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>11</td><td>1.8568</td><td>23</td><td>2.4184</td><td>35</td><td>2.98</td></tr>
<tr><td>12</td><td>1.888</td><td>24</td><td>2.4496</td><td>36</td><td>3.0112</td></tr>
<tr><td>13</td><td>1.9192</td><td>25</td><td>2.4808</td><td colspan="2" rowspan="2"></td></tr>
<tr><td>14</td><td>1.9504</td><td>26</td><td>2.512</td></tr>
</table>
</td></tr>
<tr><td>16:15</td><td>2'h1</td><td>r/w</td><td>Amp_rst speed (AMP_RST_SPEED), sets the amp_rst transition slew rate to:
2'h0 : 90 nsec
2'h1 : 700 nsec
2'h2 : 1200 nsec
2'h3 : > 1200 nsec</td></tr>
<tr><td>14</td><td>1'h1</td><td>r/w</td><td>HG bias enable, active high, when high the bias for high gain column circuit is enabled (See Note 2). This bit also enables/disables the HG column multiplexer.</td></tr>
<tr><td>13</td><td>1'h1</td><td>r/w</td><td>LG bias enable, active high, when high the bias for low gain column circuit is enabled (See Note 2). This bit also enables/disables the LG column multiplexer.</td></tr>
<tr><td>12:9</td><td>4'h7</td><td>r/w</td><td>Black sun level (SUN_LVL[3:0]) setting, sets the black sun comparator reference level with 60mV step when Blk_sun correction is enabled (ConfigReg[4]==1):
4'h0: 0.7V.
4'h1: 0.76V
.
.
.
4'he: 1.54V
4'hf: 1.6V</td></tr>
<tr><td>8:5</td><td>4'h0</td><td>r/w</td><td>High gain bandwidth (HG_BWC[3:0]) setting with step size of 500fF:
4'h0: 0pF.
4'h1: 0.500pF.
.
.
.
4'hf: 7.5pF.</td></tr>
<tr><td>4</td><td>1'h0</td><td>r/w</td><td>Column amplifier high gain channel gain switch control.</td></tr>
</table>

Bits	Default	Read / Write	Description
			1'b0 : 30x gain, 1'b1 : 15x gain.
3	1'h0	r/w	Active high bitline boost enable.
2	1'h1	r/w	Active high Vref boost enable.
1	1'h0	r/w	Offset column bit line current, when high enable offset column bit line current.
0	1'h1	r/w	Bit line current enable, when high enable bit line current (See Note 2).

Note 1: Column control configuration should only be changed when soft reset is asserted.

Note 2: This enable bit is combined with control from the Low Power (lowPwrModeReg) Register. A deassertion from either source will cause the disabling of the circuit.

12.22 Electrical Dark Config

Name: ElecDarkConfigReg Addr: 0x23 Reset: 0x00000000
Description: Electrical dark configuration register.

Bits	Default	Read/ Write	Description
31:2	30'h0	r/o	Reserved
1	1'h0	r/w	Top electrical dark configuration: 0: Disable top dark rows as electrical dark. 1: Enable electrical dark.
0	1'h0	r/w	Bottom electrical dark configuration: 0: Disable bottom dark rows as electrical dark. 1: Enable electrical dark.

12.23 Ramp Control

Name: rampCtrlReg Addr: 0x24 Reset: 0x0093b9f8
Description: Ramp control configuration register.

Bits	Default	Read/ Write (Note1)	Description
31:26	6'h0	r/o	Reserved
25:21	5'h4	r/w	ADC count enable delay from start of ramp_start in units of 4 pll_clk to compensate for the analog delay of the ramp signal. (See Note 2).
20	1'h1	r/w	Bias 100uA enable, active high, high enables the 100uA bias (See Note 3).
19	1'h0	r/w	Bias reference select, low selects the bandgap, high selects the internal resistor.
18:16	3'h3	r/w	Band gap tuning adjust, corrects Vbg errors due to process variations, lower setting increases bandgap slope.
15	1'h1	r/w	Band gap enable, active high, high enables bandgap generator (See Note 3).
14	1'h0	r/w	External ramp select, active high, high selects the external ramp.
13	1'h1	r/w	Internal ramp enable, active high, enables Vramp generator (See Note 3).
12:8	5'h19	r/w	Ramp generator initialization pulse width in units of rows, takes effect on next reset deassertion.
7:4	4'hf	r/w	High Gain Voltage ramp end voltage setting with 47mV step: 4'h0: 1.610V. 4'h1: 1.657V. . . . 4'hf: 2.36V. This field controls the ramp end voltage only for the HG ramp generator. The LG ramp generator is controlled by output test pattern 1 bits [8:5] in the Output Test Pattern Register, Register 0x27. (See Note 2).

Bits	Default	Read/ Write (Note1)	Description
3:0	4'h8	r/w	High Gain Voltage ramp start voltage setting with 16mV step: 4'h0: 0.660V. 4'h1: 0.676V. . . . 4'hf: 0.916V. This field controls the ramp end voltage only for the HG ramp generator. The LG ramp generator is controlled by output test pattern 1 bits [4:1] in the Output Test Pattern Register, Register 0x27. (See Note 2).

Note 1: Ramp control configuration should only be changed when soft reset is asserted.

Note 2: Recommended Settings for this register are different than the defaults:

Bits	Function	Default setting	Recommended setting
25:21	Sets adc counter delay	00100	00111
7:4	Sets HG ramp end voltage	1111	1111
3:0	Sets HG ramp start voltage	1000	0111

Note 3: This enable bit is combined with control from the Low Power (lowPwrModeReg) register, deassertion from either source will cause the disabling of the circuit.

12.24 Low Power Mode

Name: lowPwrModeReg Addr: 0x25 Reset: 0x000000ff
Description: Low power mode register, when this register is activated through asserting of the corresponding bit in the mode register, the bits in this register control the powering down of the corresponding circuit blocks overriding any individual register settings.

Bits	Default	Read/ Write	Description
31:8	24'h0	r/o	Reserved
7	1'h1	r/w	Injection DAC power down, active high, high powers down the injection DAC via the EN_INJ_I pin.
6	1'h1	r/w	Regulator power down, active high, high powers down all the on chip regulators.
5	1'h1	r/w	Band gap power down, active high, high powers down band gap reference circuit.
4	1'h1	r/w	Analog bias power down, active high, high powers main bias block via the BIAS_100U_EN and the DAC_BUFFER_EN pins.
3	1'h1	r/w	Analog test port power down, active high, high powers down analog test port.
2	1'h1	r/w	Row bias power down, active high, high powers down the row bias circuit.
1	1'h1	r/w	Ramp generator power down, active high, high powers down the ramp generator.
0	1'h1	r/w	Column amplifier and ADC power down, active high, high powers down the column amplifier and ADC circuits.

12.25 PLL Configuration

Name: pllConfigReg Addr: 0x26 Reset: 0x0000817f
Description: PLL configuration register.

Bits	Default	Read/ Write	Description
31:17	15'h0	r/o	Reserved
16	1'h0	r/w	DCC clock out enable, when high, clock goes to CLK_OUT pin.
15	1'h1	r/w	Duty Cycle Corrector Enable, active high, high enables the duty cycle corrector which is used to ensure the clock to the adc_counter is 50/50 duty cycle. The DCC can only be enabled when PLL is not bypassed and sys_clk is at pll_clk frequency (sys_clk_rate=0)
14:13	2'h0	r/w	Main PLL feedback divider N1 setting (See Note 1,2): 2'h0: divide by 8. 2'h1: divide by 10 (not supported). 2'h2: divide by 16 (not supported). 2'h3: divide by 20 (not supported).
12	1'h0	r/w	REF_CLK pad power down, active high, high powers down the REF_CLK input pads.
11	1'h0	r/w	PLL power down, active high, high powers down the PLL (See Notes 1,3).
10	1'h0	r/w	PLL bypass enable, active high, high enables bypassing the PLL and uses the REF_CLK input to drive the core PLL_CLK (See Notes 1,3,4).
9:8	2'h1	r/w	TXPLL feedback divider N1 setting (See Note 1,2): 2'h0: divide by 8 (not supported). 2'h1: divide by 10. 2'h2: divide by 16 (not supported). 2'h3: divide by 20 (not supported).
7:4	4'h7	r/w	PLL feedback divider N2 setting (See Notes 1,2): 4'h0: divide by 1. 4'h1: divide by 2. 4'h2: divide by 3. .

Bits	Default	Read/ Write	Description
			. . 4'hf: divide by 16.
3:2	2'h3	r/w	PLL pre-divider M setting (See Note 1,2): 2'h0: divide by 4. 2'h1: divide by 2. 2'h2: divide by 1. 2'h3: divide by 1.
1:0	2'h3	r/w	PLL post-divider P setting (See Note 1,2): 2'h0: divide by 4 (not supported). 2'h1: divide by 2. 2'h2: divide by 1. 2'h3: divide by 1.

Note 1: Even though any PLL setting (bypass, feedback divider, post divider) can be changed on the fly, output clock glitches may result, thus it is recommended that the chip be placed in reset via the soft reset mode bit while PLL settings are changed.

Note 2: The combination of post divider and feedback divider settings control the PLL_CLK frequency. The PLL has a built in VCO the frequency of which is a function of the REF_CLK and PLL settings.

The frequency of the VCO clock = (REF_CLK*N1*N2)/M.

The TX lane clock frequency = VCO clock/P.

The digital pll_clk frequency = ((REF_CLK*N2/M)).

The frequency (REF_CLK/M) >= 25MHz

The VCO clock frequency must be within the range of 1.5 GHz and 3.3GHz.

In order for the high speed serial transmission to work properly, the TX clock must be at a fixed ratio of 10 to the digital pll clock. Thus for the TX PLL, when P is 1, N1 must be 10 or when P is 2, N1 must be 20. P of 4 is not supported. For the main PLL, only N1 of 8 is supported.

Note 3: If the PLL is powered down when not in bypass mode, the PLL_CLK stops and there is no way for the chip to wake up other than an external hard reset via the RESET_B pin. To avoid this situation it is recommended that the PLL be placed in bypass mode and then powering down the PLL. The REF_CLK will then be supplied to the chip and allow waking up of the PLL in reverse, i.e. powering up the PLL and then take it out of bypass mode.

Note 4: When PLL is bypassed, it is recommended that sys_clk divider ratio in Configuration Register be set to a ratio of divided by 1 so that sys_clk can operate at reference clock rate. It is also recommended that the pre-divider M be set to 1 so that the PLL output clock is at the input frequency.

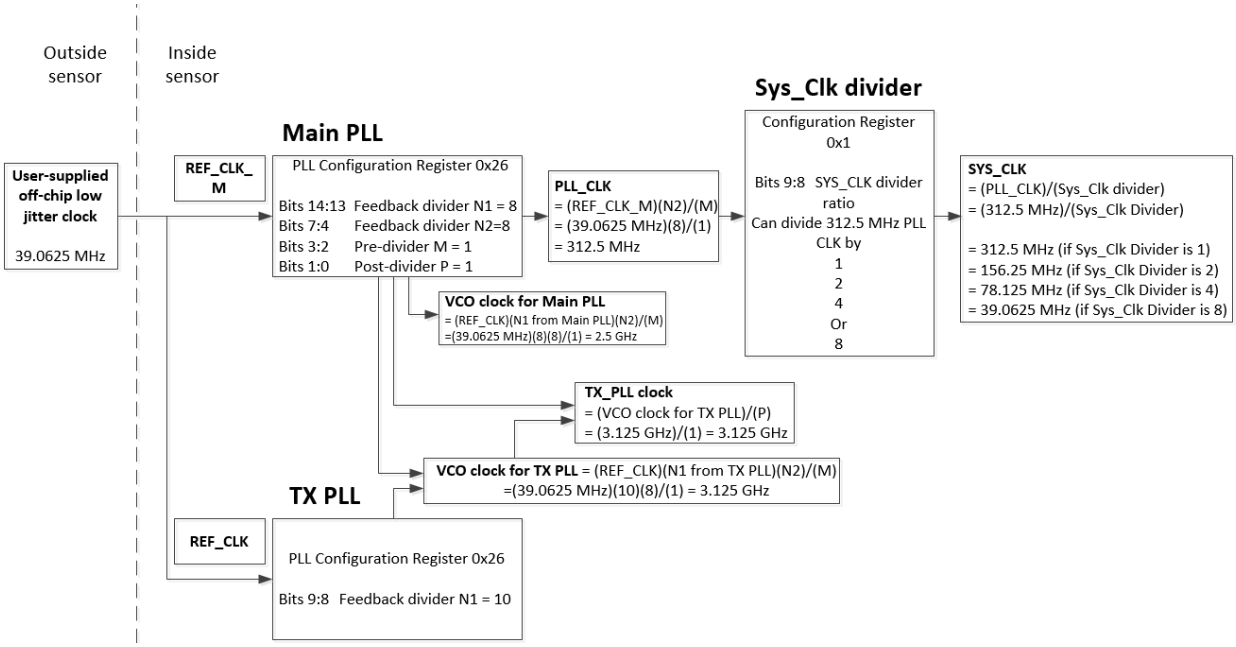


Figure 40. Diagram of PLLs and clock generation

When the Main PLLis stable, the PLL_LOCK package pin (64) goes high and the Chip Status Register (Reg 0xE) bit 0 goes high.
When the TX PLL is stable the Chip Status Register (Reg 0xE) bit 1 (TXPLL_LOCK) goes high.

Actually there are 8 TX PLLs, with each TX PLL having an associated 4 Data lines (A0..A3, A4..A7, B0..B3, B4..B7, C0..C3, C4..C7, D0..D3, D4..D7) and TXPLL_LOCK is the “AND” sum of all of the eight TX PLLs being stable. In the case that less than the full 32 data lines are used, the unused TX PLLs are taken out of this “AND” sum.

12.26 Output Test Pattern

Name: testPatReg Addr: 0x27 Reset: 0x00155555
Description: Output test pattern control register

Bits	Default	Read/ Write	Description
31:24	8'h0	r/o	Reserved
23:22	2'h0	r/w	Output test pattern select: 2'h0: No test pattern insertion This is the normal operating mode, since it is only rarely that the user will want to output a test pattern instead of data from the pixel array. In this mode bits [21:0] of this register have the following functions:

<table>
<tr><th>Bits</th><th>Default</th><th>Read/ Write</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>Bits</td><td>Function</td></tr>
<tr><td>21:20</td><td>No function</td></tr>
<tr><td>19:12</td><td>Control of LG ramp settings</td></tr>
<tr><td>11:4</td><td>No function</td></tr>
<tr><td>3</td><td>Global Shutter hot/blinking pixel reduction circuit enable</td></tr>
<tr><td>2:0</td><td>Bitline Clamp voltage</td></tr>
</table>

For the following options (bits [23:22] = 01, 10, or 11), the function of this register is to control a test pattern output. There is no contradiction with the earlier functions, since when the test pattern is output, the digital output is controlled by the test pattern generator, and the earlier functions (ramp settings for the LG ADC, GS hot/blinking pixel reduction circuit, and bitline clamp), while still valid, are irrelevant to the sensor output.

Test Pattern options:
2'h1: Gray scale pattern.
2'h2: Alternating column pattern 1, even columns with programmed test pattern 0 value, odd columns with programmed test pattern 1 value.
2'h3: ADC count debug, even column with adc_count[10:1] equals pattern 0, odd columns with adc_count[10:1] equals pattern 1.
</td></tr>
<tr><td>21:11</td><td>11'h2aa</td><td>r/w</td><td>Dual function: Either Low Gain Ramp Control or Test Pattern 1, depending on the Register 0x27 bits [23:22] setting.

If register 0x27 bits [23:22] = 00, then these bits control the Low Gain Ramp:
<table>
<tr><td>Bits</td><td>LG ramp generator control function</td><td>Recommended Settings</td></tr>
<tr><td>21:20</td><td>No function</td><td>Not applicable</td></tr>
<tr><td>19:16</td><td>Sets Ramp End voltage</td><td>1111</td></tr>
<tr><td>15:12</td><td>Sets Ramp Start voltage</td><td>1101</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bits</th><th>Default</th><th>Read/ Write</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><td>11</td><td>No function</td><td>Not applicable</td></tr>
</table>

If register 0x27 bits [23:22] = 01, then these bits [21:11] are irrelevant. The LG ramp function doesn’t matter because a test pattern is being output. But the test pattern being output doesn’t use bits [21:11]: it is a gray scale ramp from left to right, with each column’s DN value increasing by 1 DN moving left to right.

If register 0x27 bits [23:22] = 10 or 11, then these bits control the Test pattern 1 value:
<table>
<tr><td>Bits</td><td>Test pattern 1 function</td></tr>
<tr><td>21:11</td><td>Bits [10:0] of Output test pattern 1</td></tr>
</table>

Test pattern 1 value to be inserted in the pixel datapath. When used as seed for PRBS generation in column BIST test, the value cannot be all 0. When the sensor is outputting a test pattern, the functionality of these bits in determining the LG ramp generator is still valid, but it is irrelevant in the sense that the sensor will output the test pattern, which does not depend on the ramp voltage settings.
</td></tr>
<tr><td>10:0</td><td>11'h555</td><td>r/w</td><td>If register 0x27 bits [23:22] = 00, the 4 LSB [3:0] serve as analog control functions:
<table>
<tr><td>Bit(s)</td><td>Analog Control Function</td></tr>
<tr><td>10:4</td><td>No function</td></tr>
<tr><td>3</td><td>When set to 1, enables global shutter hot/blinking pixel reduction circuit</td></tr>
<tr><td>2:0</td><td>Bitline Clamp voltage level selection (Note 1)
000 = Bitline Clamp is off
001 => Bitline Clamp is at lowest voltage setting
…
111 => Bitline Clamp is a highest voltage setting</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bits</th><th>Default</th><th>Read/ Write</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>If register 0x27 bits [23:22] = 01, then these bits [10:0] are irrelevant. The GS hot/blinking pixel reduction circuit and bitline clamp don’t matter because a test pattern is being output. But the test pattern being output doesn’t use bits [10:0]: it is a gray scale ramp from left to right, with each column’s DN value increasing by 1 DN moving left to right.

If register 0x27 bits [23:22] = 10 or 11, then these bits control the Test pattern 0 value:
<table><tr><td>Bits</td><td>Test pattern 0 function</td></tr><tr><td>10:0</td><td>Bits [10:0] of Output test pattern 0</td></tr></table>
Test pattern 0 value to be inserted in the pixel datapath. When used as seed for PRBS generation in column BIST test, the value cannot be all 0.</td></tr>
</table>

Note 1: If the photo-electron signal from the pixel were of such a large magnitude that the Column Amplifier input was at or near 0 Volts, the “bitline GND” might actually be driven below 0 Volts. (See Figure 41.) To protect against this possibility the 4625 has a “Bitline Clamp” Protection Circuit that imposes a register-programmable limit on how low in voltage this point in the circuit may go.

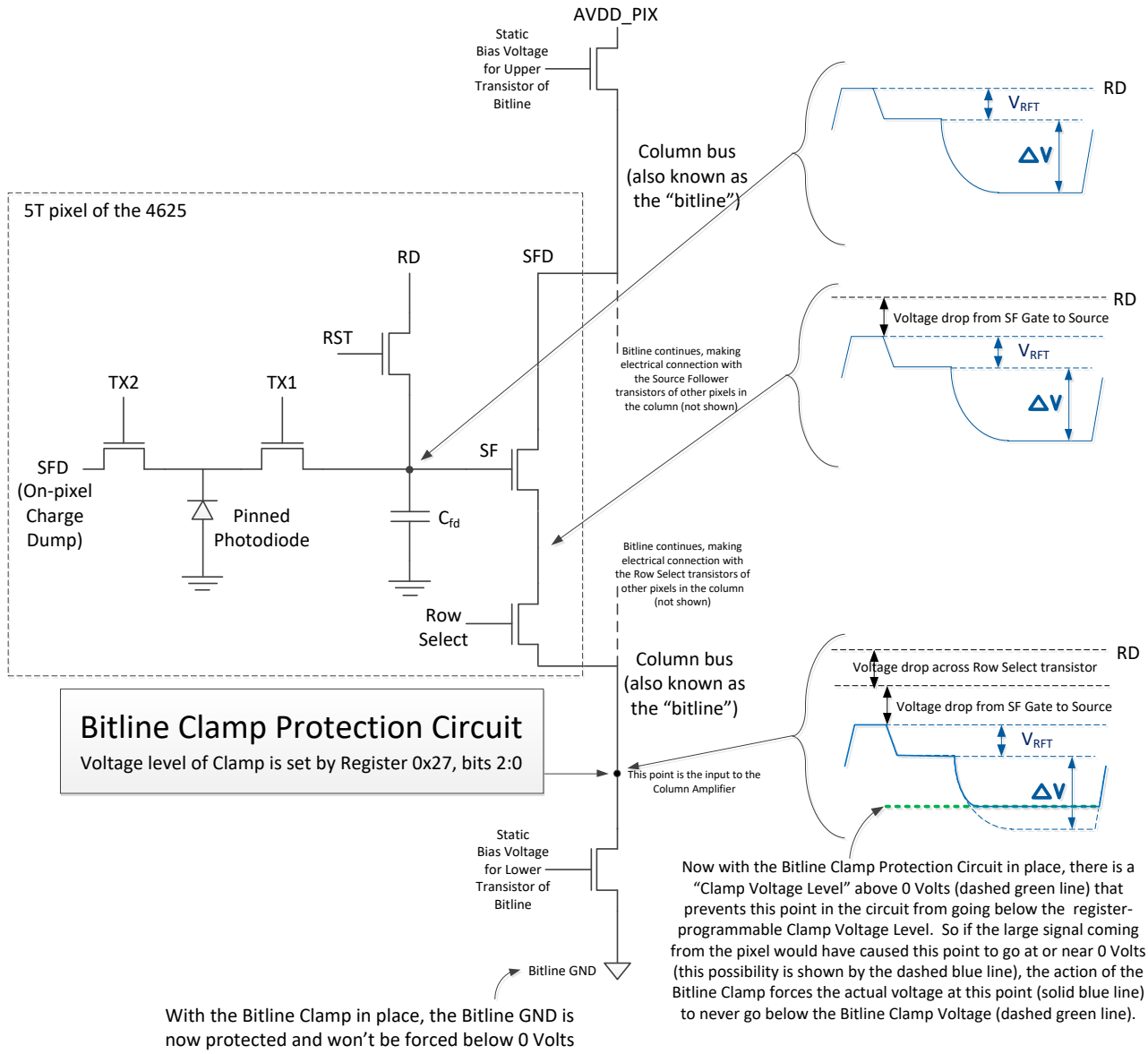


Figure 41. Bitline Clamp location and function

12.27 Column Segment Power Enable

Name: colseqEnaReg Addr: 0x28 Reset: 0xffffffff
Description: Column Segment Power Enable control register.

Bits	Default	Read/ Write	Description
31:0	32'hffffffff	r/w	Column Segment Power Enable. Unused column segments can be powered down to reduce power consumption. Each bit enables column power to a segment of 146 columns. Power down columns always output full scale value (2048). bit 31: 1 enables powers to columns 4526 to 4671; 0 disables powers to the same columns. bit 30: 1 enables powers to columns 4380 to 4525; 0 disables powers to the same columns. bit 29: 1 enables powers to columns 4234 to 4379; 0 disables powers to the same columns. . . bit 2 : 1 enables powers to columns 292 to 437; 0 disables powers to the same columns. bit 1 : 1 enables powers to columns 146 to 291; 0 disables powers to the same columns. bit 0 : 1 enables powers to columns 0 to 145; 0 disables powers to the same columns.

12.28 TX Lane Configuration

Name: txlaneConfReg Addr: 0x29 Reset: 0x73c407ff
Description: TX Lane Configuration Register

Bits	Default	Read/ Write	Description
31	1'h0	r/o	Reserved
30:29	2'h3	r/w	TX driver launch amplitude adjustment. 2'h0 : TBD 2'h1 : TBD 2'h2 : TBD 2'h3 : 300mV differential peak-to-peak

Bits	Default	Read/ Write	Description
28:25	4'h9	r/w	TX driver termination trimming setting. 4'h0 : TBD 4'h1 : TBD . . 4'h9 : 100 ohm . . 4'h14: TBD 4'h15: TBD
24	1'h1	r/w	CRC initialization value. The CRC value at beginning of each packet will be initialized to 16 bits of this value.
23	1'h1	r/w	Swap CRC input, active high, when high enable the MSB/LSB swap on data going into the CRC generator.
22	1'h1	r/w	Swap CRC output, active high, when high enable the MSB/LSB swap on CRC word coming out from the CRC generator.
21	1'h0	r/w	Link Test Inject CRC error, active high, when high enable the injection of CRC error once per packet.
20	1'h0	r/w	Link Test Inject data error, active high, when high enable the injection of encoder data error once per packet.
19	1'h0	r/w	Link Test Inject disparity error, active high, when high enable the injection of run time disparity error once per packet.
18	1'h1	r/w	tx clock enable, active high, high enable the tx driver high speed clock.
17	1'h0	r/w	tx driver test mode serial odd_data
16	1'h0	r/w	tx driver test mode serial even_data
15:14	2'h0	r/w	tx driver test mode select, selects various mode of test 2'd0: normal operation 2'd1: tx PRBS test 2'd2: tx parallel static word (taken from seed[9:0]) test 2'd3: tx serial even/odd data test
13	1'h0	r/w	Start PRBS serial streaming, active high, when asserted continuously streaming PRBS data to serial port.

Bits	Default	Read/ Write	Description
12	1'h0	r/w	PRBS serial stream enable, active high, when asserted enable the generator for streaming of PRBS data to serial port.
11	1'h0	r/w	PRBS packet data enable, active high, when asserted enable the replacement of packet data with PRBS data.
10:0	11'h7ff	r/w	PRBS Seed for the PRBS generator in the digital logic as well as in the TX driver even lanes. When TX driver test mode is 2, the 10 LSB is used as static test parallel data for the TX driver. TX driver odd lanes has a fixed seed of 7FF

12.29 Injection DAC Control

Name: injDACReg Addr: 0x2a Reset: 0x00380000
Description: Injection DAC Control Register

Bits	Default	Read/ Write	Description
31:22	10'h0	r/o	Reserved
21:20	2'h3	r/w	Analog test mode injection DAC output select to go to INJ_TST pad, active high. 00 : injection DAC final output with switching between selected level and VRST 01 : injection DAC LG level will be output to INJ_TST 10 : injection DAC HG level will be output to INJ_TST 11 : no output, INJ_TST is high Z.
19	1'h1	r/w	Injection DAC reference enable (EN_INJ_I_REF), active high, when high enable injection DAC reference (See Note 1).
18:16	3'h0	r/w	Injection DAC reference current level (I_INJ_REF), adjusts the full scale level voltage swing with a 149mV step: 3'h0: 596mV. 3'h1: 745mV. . . . 3'h7: 1788mV.

Bits	Default	Read/ Write	Description
15:10	6'h0	r/w	Injection level high gain mode: High Gain 1LSB step = Max Signal / 2032. High Gain Signal can take 64 levels. 6'h0: 0 signal (connected to AVDD_RST). 6'h1: Max Signal * (1 / 2032). . . . 6'h3f: Max Signal * (63 / 2032).
9:3	7'h0	r/w	Injection level low gain mode: Low Gain 1LSB step = Max Signal / 127. Low Gain Signal can take 124 levels. 7'h0 - 7'h3: 0 signal (connected to AVDD_RST). 7'h4 : Max Signal * (4 / 127). 7'h5 : Max Signal * (5 / 127). . . . 7'h7f : Max Signal * (127 / 127).
2	1'h0	r/w	Injection range select has the following definition: 1'h0: Select high gain range. 1'h1: Select low gain range.
1	1'h0	r/w	Subrange Enable, active high when high enable sub-LSB injection.
0	1'h0	r/w	Subrange level select (FINE_RANGE), has the following definition: 0: Injection is 1/16 of nominal by reducing reference current by 1/16 1: Injection is 1/512 of nominal by reducing reference current by 1/512.

Note 1: This enable bit is combined with control from the Low Power (lowPwrModeReg) register, deassertion from either source will cause the disabling of the circuit.

12.30 Debug

Name: debugReg Addr: 0x2b Reset: 0x40000fe6
Description: Debug register

Bits	Default	Read/ Write	Description
31	1'h0	r/w	Force DCC enable independent of any other condition.
30: 28	3'h4	r/w	Row update state machine state duration. The row state machine sends data to the row decoder. The duration is equivalent to the time allocated for setup and hold time of signals in relationship to the clock at the received end. The value is in units of sys_clk cycle and a value of 0 is not allowed.
27	1'h0	r/w	CLK_OUT phase inversion, active high
26	1'h0	r/w	Reserved
25	1'h0	r/w	Reserved
24	1'h0	r/w	Column BIST enable, active high, high enables the built-in self test for the column shift logic. The test uses the two programmable test patterns in Output Test Pattern Register as seeds to two pseudo-random pattern generators as the alternate column pattern for odd and even columns, one set of patterns per row, until the test is disabled. The result is read from the bist result registers.
23	1'h0	r/w	Digital test port enable, active high, high enables internal digital signals to be muxed to the DOUT pins.
22: 20	3'h0	r/w	Digital test port block select: 3'h0: Array_ctrl_top 3'h1: Row frame control block. 3'h2: Array_ctrl 3'h3: (not used) 3'h4: Output datapath top (bot) 3'h5: (not used) 3'h6: Output group (bot) 3'h7: TX interface (bot lane0).
19: 16	4'h0	r/w	Digital test port mux, selects internal signals to be muxed onto the DOUT pins, the following describes the signals for each internal block: Array Control Top Block

Bits	Default	Read/ Write	Description
			---------- 4'h0: {row_start,sync1_pipe[1:0],sync2_pipe[1:0], line_desc[0].shutter_mode,line_desc[0].ref_frame,line_desc[0]. blank, line_desc[0].new_roi,line_desc[0].real_row,line_desc[0].first_ro w, line_desc[0].last_real_row,line_desc[0].last_row,line_desc[0].idl e_row, line_desc[0].inject_row} 4'h1: {5'h0,anti_bleed_lclr,anti_bleed_lset,anti_bleed_gclr,anti_bleed _gset, pix_rsttx1_lclr,pix_rsttx1_lset,pix_rsttx1_gclr,pix_rsttx1_gset, row_active_ena,row_decoder_clk} 4'h2 - 4'hf : 15'h0 Row Frame Control Block ---------- 4'h0: {4'b0,idle_row,row_start,last_row_minus1,roi_reg_update_pulse , roi_regs_updated,next_frame_has_new_roi,near_end_of_row,tr igger_sync, trig_curr,trigger_rise,trigger_fall} 4'h1: {2'b0,read_row_init,reset_row_init,timer_start,reset_row_clear, pending_read_trigger,new_roi_frame,gs_tx1_int,gs_tx2_int, table_sel_int,real_row,last_row,last_real_row,last_row_minus1} 4'h2: {5'b0,read_row_active,read_row[9:0]} 4'h3: {5'b0,reseta_row_active,reseta_row[9:0] 4'h4: {5'b0,reseta_row_active,resetb_row[9:0] 4'h5 - 4'hf: 15'h0 Array Control Block ---------- 4'h0: {row_start,row_update_start,near_end_of_row,table_sel_sampl ed, row_en,pix_rst_row,pix_tx1_row,pix_tx2_row, pix_rst_vsw_row,s1,s2,amp_reset[1:0], avdd_pix_smpl,bit_bias_smpl} 4'h1:

Bits	Default	Read/ Write	Description
			{2'b0,adc_buff_smpl,adc_buff_en,adc_comp_rst,sun_comp_en, sun_latch_en, ramp_start_top,ramp_rst_top,ramp_init_top,inj_signal, adc_count_ena,cross_switch,column_start,adc_transfer} 4'h2: {row_clock_counter[14:0]} 4'h3 - 4'hf: 15'h0 Output Datapath Block (Bottom) ---------- 4'h0: {4'b0,shift_active,shift_n_hold_b[0],col_start_sync,line_desc_3. horiz_right_edge[7:0]} 4'h1 - 4'hf: 15'h0 Output Group Block (Bottom) ---------- 4'h0: {2'b0,shift_active,col_data_valid_dly[1],col_data0_buf[10:0]} 4'h1: {3'b0,col_data_valid_dly[3],col_bin_data0[10:0]}) 4'h2: {3'b0,wr_data_valid[0],col_mux_data0[10:0]} 4'h3: {4'b0,PRBS_pack_data_ena,PRBS_pack_data[9:0]} 4'h4: {3'b0,PRBS_strm_data_ena,PRBS_strm_run,PRBS_strm_data[9:0]} 4'h5 - 4'hf: 15'h0 TX Interface Block (Bottom) ---------- 4'h0: {4'b0,data_valid,2'b0,data[7:0]} 4'h1: {4'b0,packet_payload_valid,2'b0,packet_payload[7:0]} 4'h2: {4'b0,~idle_dly[3],1'b0,packet[8:0]} 4'h3: {fifo_ena,tx_init,2'b0,disparity,encoded_packet[9:0]} 4'h4: {error_PRBS_ena,injection_crc_ena,injection_enc_ena,1'b0,err or_crc_freq[10:0]} 4'h5: {4'b0,error_enc_freq[10:0]} 4'h6: {inj_crc_error_mask[14:0]} 4'h7: {5'b0,inj_data_error_mask[9:0]} 4'h8: {crc_int[14:0]} 4'h9: {crc[14:0]} 4'ha - 4'hf: 15'h0

Bits	Default	Read/ Write	Description
15	1'h0	r/w	Analog test port enable, active high, high enables analog test port.
14: 13	2'h0	r/w	Analog test port channel select, binary code corresponds to mux input: 2'h0: selects AOUT0_TP TBD AOUT0_BT TBD AOUT1_TP TBD AOUT1_BT TBD AOUT2_TP TBD AOUT2_BT TBD AOUT3_TP TBD AOUT3_BT TBD AOUT4_TP TBD AOUT4_BT TBD AOUT5_TP TBD AOUT5_BT TBD AOUT6_TP TBD AOUT6_BT TBD 2'h1: selects AOUT0_TP TBD AOUT0_BT TBD AOUT1_TP TBD AOUT1_BT TBD AOUT2_TP TBD AOUT2_BT TBD AOUT3_TP TBD AOUT3_BT TBD AOUT4_TP TBD AOUT4_BT TBD AOUT5_TP TBD AOUT5_BT TBD AOUT6_TP TBD AOUT6_BT TBD 2'h2: selects AOUT0_TP TBD AOUT0_BT TBD AOUT1_TP TBD AOUT1_BT TBD AOUT2_TP TBD

Bits	Default	Read/ Write	Description
			AOUT2_BT TBD AOUT3_TP TBD AOUT3_BT TBD AOUT4_TP TBD AOUT4_BT TBD AOUT5_TP TBD AOUT5_BT TBD AOUT6_TP TBD AOUT6_BT TBD 2'h3: selects AOUT0_TP TBD AOUT0_BT TBD AOUT1_TP TBD AOUT1_BT TBD AOUT2_TP TBD AOUT2_BT TBD AOUT3_TP TBD AOUT3_BT TBD AOUT4_TP TBD AOUT4_BT TBD AOUT5_TP TBD AOUT5_BT TBD AOUT6_TP TBD AOUT6_BT TBD
12:5	8'h7f	r/w	PLL lock high detection threshold, sets the number of REF_CLKs of consecutive high PLL locks to declare an active PLL lock.
4:1	4'h3	r/w	PLL lock low detection threshold, sets the number of REF_CLKs of consecutive low PLL locks to declare an inactive PLL lock.
0	1'h0	r/w	PLL lock no wait enable, active high, high enables power up sequencer to continue without waiting for the PLL lock signal to become active.

12.31 Column BIST Error Data 0

Name: bistErr0Reg Addr: 0x2c Reset: 0x00000000
Description: BIST error 0 register for bottom row 0

Bits	Default	Read/ Write	Description
31:18	14'h0	r/o	Reserved.
17	1'h0	r/o	Column BIST Error for bottom row 0.
16:6	11'h0	r/o	Column BIST sequence count at first error for bottom row 0. The sequence count is in units of 3-column
5:0	6'h0	r/o	Column BIST error detail at first error for bottom row 0. bit 5: stream 2 low gain data error, bit 4: stream 2 high gain data error, bit 3: stream 1 low gain data error, bit 2: stream 1 high gain data error, bit 1: stream 0 low gain data error, bit 0: stream 0 high gain data error,

12.32 Column BIST Error Data 1

Name: bistErr1Reg Addr: 0x2d Reset: 0x00000000
Description: BIST error 1 register for bottom row 1

Bits	Default	Read/ Write	Description
31:18	14'h0	r/o	Reserved.
17	1'h0	r/o	Column BIST Error for bottom row 1.
16:6	11'h0	r/o	Column BIST sequence count at first error for bottom row 1. The sequence count is in units of 3-column
5:0	6'h0	r/o	Column BIST error detail at first error for bottom row 1. bit 5: stream 2 low gain data error, bit 4: stream 2 high gain data error, bit 3: stream 1 low gain data error, bit 2: stream 1 high gain data error, bit 1: stream 0 low gain data error, bit 0: stream 0 high gain data error,

12.33 Column BIST Error Data 2

Name: bistErr2Reg Addr: 0x2e Reset: 0x00000000
Description: BIST error 2 register for top row 0

Bits	Default	Read/ Write	Description
31:18	14'h0	r/o	Reserved.
17	1'h0	r/o	Column BIST Error for top row 0.
16:6	11'h0	r/o	Column BIST sequence count at first error for top row 0. The sequence count is in units of 3-column
5:0	6'h0	r/o	Column BIST error detail at first error for top row 0. bit 5: stream 2 low gain data error, bit 4: stream 2 high gain data error, bit 3: stream 1 low gain data error, bit 2: stream 1 high gain data error, bit 1: stream 0 low gain data error, bit 0: stream 0 high gain data error,

12.34 Column BIST Error Data 3

Name: bistErr3Reg Addr: 0x2f Reset: 0x00000000
Description: BIST error 2 register for top row 1

Bits	Default	Read/ Write	Description
31:18	14'h0	r/o	Reserved.
17	1'h0	r/o	Column BIST Error for top row 1.
16:6	11'h0	r/o	Column BIST sequence count at first error for top row 1. The sequence count is in units of 3-column
5:0	6'h0	r/o	Column BIST error detail at first error for top row 1. bit 5: stream 2 low gain data error, bit 4: stream 2 high gain data error, bit 3: stream 1 low gain data error, bit 2: stream 1 high gain data error, bit 1: stream 0 low gain data error, bit 0: stream 0 high gain data error,

12.35 TX Data Invert

Name: txDataInvReg Addr: 0x30 Reset: 0x00000000
Description: TX Data Invert Control register

Bits	Default	Read / Write	Description
31:0	32'h0	r/w	Invert the transmitted data effectively swapping the two differential outputs. There is one bit for each TX lane. bit 31: 1 enables data inversion for DOUT group D lane 7 bit 30: 1 enables data inversion for DOUT group D lane 6 bit 29: 1 enables data inversion for DOUT group D lane 5 . . bit 2 : 1 enables data inversion for DOUT group A lane 2 bit 1 : 1 enables data inversion for DOUT group A lane 1 bit 0 : 1 enables data inversion for DOUT group A lane 0

12.36 Waveform Enable 0

Name: waveEna0Reg Addr: 0x40 Reset: 0x55555555
Description: Waveform enable 0 register

Bits	Default	Read / Write	Description
31:0	32'h55555555	r/w	Waveform control signal enable 2 bits per signal: 2'h0: Start/stop 1, 0 disabled. 2'h1: Start/stop 1 disabled, start/stop 0 enabled. 2'h2: Start/stop 1 enabled, start/stop 0 disabled. 2'h3: Start/stop 1 enabled, start/stop 0 enabled. Bits[1:0] are for Signal 0 . . . Bits[31:30] are for Signal 15

12.37 Waveform Enable 1

Name: waveEna1Reg Addr: 0x41 Reset: 0x00055555
Description: Waveform enable 1 register

Bits	Default	Read/ Write	Description
31:0	32'h55555	r/w	Waveform control signal enable 2 bits per signal: 2'h0: Start/stop 1, 0 disabled. 2'h1: Start/stop 1 disabled, start/stop 0 enabled. 2'h2: Start/stop 1 enabled, start/stop 0 disabled. 2'h3: Start/stop 1 enabled, start/stop 0 enabled. Bits[1:0] are for Signal 16 . . . Bits[29:28] are unused for Signal 30 Bits[31:30] are for Signal 31

12.38 Waveform Enable 2

Name: waveEna2Reg Addr: 0x42 Reset: 0x00000000
Description: Waveform enable 2 register

Bits	Default	Read/ Write	Description
31:0	32'h0	r/w	Waveform control signal enable 2 bits per signal: 2'h0: Start/stop 1, 0 disabled. 2'h1: Start/stop 1 disabled, start/stop 0 enabled. 2'h2: Start/stop 1 enabled, start/stop 0 disabled. 2'h3: Start/stop 1 enabled, start/stop 0 enabled. Bits[1:0] are for Signal 32 . . . Bits[11:10] are unused for Signal 37 Bits[13:12] are unused for Signal 38 Bits[15:14] are unused for Signal 39 . . . Bits[31:30] are for Signal 47

12.39 Waveform Doubling

Name: waveDblReg Addr: 0x43 Reset: 0x00000000
Description: Waveform doubling register

Bits	Default	Read/ Write	Description
31:8	24'h0	r/o	Reserved
7:0	8'h0	r/w	Waveform doubling control, active high, when high wave signals are paired together to provide more wave edges: bit[0]: Wave signals 0 and 40 are paired together. . . . bit[6]: Wave signals 6 and 46 are paired together. bit[7]: Wave signals 7 and 47 are paired together.

12.40 Waveform Init 0

Name: waveInit0Reg Addr: 0x44 Reset: 0x00110820
Description: Waveform init 0 register

Bits	Default	Read/ Write	Description
31:0	32'h110820	r/w	Waveform control signal initialization for signals 0 to 31: 1'h0: Initialize the signal to 0 at beginning of row. 1'h1: Initialize the signal to 1 at beginning of row. bit[0]: Controls signal initialization for Signal 0. . . . bit[30]: unused for Signal 30. bit[31]: Controls signal initialization for Signal 31.

12.41 Waveform Init 1

Name: waveInit1Reg Addr: 0x45 Reset: 0x00000000
Description: Waveform init 1 register

Bits	Default	Read/ Write	Description
31:16	16'h0	r/o	Reserved
15:0	16'h0	r/w	Waveform control signal initialization for signals 32 to 47: 1'h0: Initialize the signal to 0 at beginning of row. 1'h1: Initialize the signal to 1 at beginning of row. bit[0]: Controls signal initialization for Signal 32. bit[1]: Controls signal initialization for Signal 33. . . . bit[14]: unused for Signal 46. bit[15]: Controls signal initialization for Signal 47.

12.42 Wave Time 1A

Name: waveTime1AReg
Addr: 0x46 -> 0xa5

Reset: 0x04a00001
Description:
The wave time 1A register array provides a set of timing pulses for the pixel array,
a maximum of two pulses can be programmed for each wavetable output, the minimum is zero:
Register address 15'h46 is for waveform Signal 0 first toggle1/toggle2 pair.
Register address 15'h47 is for waveform Signal 0 second toggle1/toggle2 pair.
.
.
.
Register address 15'h82 is unused for waveform Signal 30 first toggle1/toggle2 pair.
Register address 15'h83 is unused for waveform Signal 30 first toggle1/toggle2 pair.
.
.
.
Register address 15'h90 is unused for waveform Signal 37 first toggle1/toggle2 pair.
Register address 15'h91 is unused for waveform Signal 37 first toggle1/toggle2 pair.
Register address 15'h92 is unused for waveform Signal 38 first toggle1/toggle2 pair.
Register address 15'h93 is unused for waveform Signal 38 first toggle1/toggle2 pair.
Register address 15'h94 is unused for waveform Signal 39 first toggle1/toggle2 pair.
Register address 15'h95 is unused for waveform Signal 39 first toggle1/toggle2 pair.
.
.
.
Register address 15'ha4 is for waveform Signal 47 first toggle1/toggle2 pair.

Register address 15'ha5 is for waveform Signal 47 second toggle1/toggle2 pair.

Table 31: Wavetable A signals

Reg address (dec)	Reg address (hex)	Default Toggle 1 (15:0)	Default Toggle 2 (31:16)	Signal name	First/Second toggles
70	46	16'h1	16'h4a0	pix_rst_gs_row	first toggles
71	47	16'h0	16'h0	pix_rst_gs_row	second toggles
72	48	16'h1	16'h6d	pix_rst_rs_row	first toggles
73	49	16'h0	16'h0	pix_rst_rs_row	second toggles
74	4A	16'h6ad	16'h7b0	pix_tx1_gs_row	first toggles
75	4B	16'h0	16'h0	pix_tx1_gs_row	second toggles
76	4C	16'h31d	16'h3ba	pix_tx1_rs_row	first toggles
77	4D	16'h0	16'h0	pix_tx1_rs_row	second toggles
78	4E	16'h6ad	16'h7b0	pix_tx2_gs_row	first toggles
79	4F	16'h0	16'h0	pix_tx2_gs_row	second toggles
80	50	16'h0	16'h0	pix_tx2_rs_row	first toggles
81	51	16'h0	16'h0	pix_tx2_rs_row	second toggles
82	15'h52	16'h442	16'h4fe	pix_rst_vsw_row	first toggles
83	15'h53	16'h0	16'h0	pix_rst_vsw_row	second toggles
84	15'h54	16'h0	16'h0	rst_clamp_row	first toggles
85	15'h55	16'h0	16'h0	rst_clamp_row	second toggles
86	15'h56	16'h1	16'h30d	s1	first toggles
87	15'h57	16'h0	16'h0	-	-
88	15'h58	16'h1	16'h69b	s2	first toggles
89	15'h59	16'h0	16'h0	-	-
90	15'h5A	16'h1	16'h7e	amp_reset0	first toggles
91	15'h5B	16'h0	16'h0	-	-
92	15'h5C	16'h13a	16'h6ac	amp_reset1	first toggles
93	15'h5D	16'h0	16'h0	-	-
94	15'h5E	16'h1	16'h4f	avdd_pix_smpl	first toggles
95	15'h5F	16'h0	16'h0	-	-
96	15'h60	16'h1	16'h5f	bit_bias_smpl	first toggles
97	15'h61	16'h0	16'h0	-	-
98	15'h62	16'h6b4	16'h7a2	adc_buf_en	first toggles
99	15'h63	16'h0	16'h0	-	-
100	15'h64	16'h6c3	16'h791	adc_buff_smpl	first toggles
101	15'h65	16'h0	16'h0	-	-

102	15'h66	16'h61	16'h6b4	adc_comp_rst	first toggles
103	15'h67	16'h0	16'h0	-	-
104	15'h68	16'h16	16'h277	sun_comp_en	first toggles
105	15'h69	16'h0	16'h0	-	-
106	15'h6A	16'h234	16'h266	sun_latch_en	first toggles
107	15'h6B	16'h0	16'h0	-	-
108	15'h6C	16'hd8	16'h4d8	ramp_start	first toggles
109	15'h6D	16'h0	16'h0	-	-
110	15'h6E	16'h1c	16'h5ba	ramp_rst	first toggles
111	15'h6F	16'h0	16'h0	-	-
112	15'h70	16'h78a	16'h78e	adc_transfer	first toggles
113	15'h71	16'h0	16'h0	-	-
114	15'h72	16'h3	16'h4	column_start	first toggles
115	15'h73	16'h0	16'h0	-	-
116	15'h74	16'h1	16'h792	row_en	first toggles
117	15'h75	16'h0	16'h0	-	-
118	15'h76	16'h787	16'h788	cross_sample_ena	first toggles
119	15'h77	16'h0	16'h0	-	-
120	15'h78	16'h31d	16'h6ae	inj_signal	first toggles
121	15'h79	16'h0	16'h0	-	-
122	15'h7A	16'h0	16'h0	-	-
123	15'h7B	16'h0	16'h0	-	-
124	15'h7C	16'h0	16'h0	-	-
125	15'h7D	16'h0	16'h0	-	-
126	15'h7E	16'h0	16'h0	-	-
127	15'h7F	16'h0	16'h0	-	-
128	15'h80	16'h0	16'h0	-	-
129	15'h81	16'h0	16'h0	-	-
130	15'h82	16'h0	16'h0	-	-
131	15'h83	16'h0	16'h0	-	-
132	15'h84	16'h0	16'h0	-	-
133	15'h85	16'h0	16'h0	-	-
134	15'h86	16'h0	16'h0	-	-
135	15'h87	16'h0	16'h0	-	-
136	15'h88	16'h0	16'h0	-	-
137	15'h89	16'h0	16'h0	-	-
138	15'h8A	16'h0	16'h0	-	-
139	15'h8B	16'h0	16'h0	-	-
140	15'h8C	16'h0	16'h0	-	-

141	15'h8D	16'h0	16'h0	-	-
142	15'h8E	16'h0	16'h0	-	-
143	15'h8F	16'h0	16'h0	-	-
144	15'h90	16'h0	16'h0	-	-
145	15'h91	16'h0	16'h0	-	-
146	15'h92	16'h0	16'h0	-	-
147	15'h93	16'h0	16'h0	-	-
148	15'h94	16'h0	16'h0	-	-
149	15'h95	16'h0	16'h0	-	-
150	15'h96	16'h0	16'h0	pix_rst_gs_row	first toggles
151	15'h97	16'h0	16'h0	pix_rst_gs_row	second toggles
152	15'h98	16'h0	16'h0	pix_rst_rs_row	first toggles
153	15'h99	16'h0	16'h0	pix_rst_rs_row	second toggles
154	15'h9A	16'h0	16'h0	pix_tx1_gs_row	first toggles
155	15'h9B	16'h0	16'h0	pix_tx1_gs_row	second toggles
156	15'h9C	16'h0	16'h0	pix_tx1_rs_row	first toggles
157	15'h9D	16'h0	16'h0	pix_tx1_rs_row	second toggles
158	15'h9E	16'h0	16'h0	pix_tx2_gs_row	first toggles
159	15'h9F	16'h0	16'h0	pix_tx2_gs_row	second toggles
160	15'hA0	16'h0	16'h0	pix_tx2_rs_row	first toggles
161	15'hA1	16'h0	16'h0	pix_tx2_rs_row	second toggles
162	15'hA2	16'h0	16'h0	pix_rst_vsw_row	first toggles
163	15'hA3	16'h0	16'h0	pix_rst_vsw_row	second toggles
164	15'hA4	16'h0	16'h0	rst_clamp_row	first toggles
165	15'hA5	16'h0	16'h0	rst_clamp_row	second toggles

Bits	Default	Read/ Write	Description
31:16	16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0	r/w	Waveform control signal toggle 2 in number of system clocks, default values are listed from highest address to lowest address.

Bits	Default	Read/ Write	Description
	16'h0 16'h6ae 16'h0 16'h788 16'h0 16'h792 16'h0 16'h4		

Bits	Default	Read/ Write	Description
	16'h0 16'h78e 16'h0 16'h5ba 16'h0 16'h4d8 16'h0 16'h266 16'h0 16'h277 16'h0 16'h6b4 16'h0 16'h791 16'h0 16'h7a2 16'h0 16'h5f 16'h0 16'h4f 16'h0 16'h6ac 16'h0 16'h7e 16'h0 16'h69b 16'h0 16'h30d 16'h0 16'h0 16'h0 16'h4fe 16'h0 16'h0 16'h0 16'h7b0 16'h0 16'h3ba 16'h0 16'h7b0 16'h0 16'h6d		

Bits	Default	Read/ Write	Description
	16'h0 16'h4a0		
15:0	16'h0 16'h0	r/w	Waveform control signal toggle 1 in number of system clocks, default values are listed from highest address to lowest address.

Bits	Default	Read/ Write	Description
	16'h0 16'h0 16'h0 16'h0 16'h0 16'h31d 16'h0 16'h787 16'h0 16'h1 16'h0 16'h3 16'h0 16'h78a 16'h0 16'h1c 16'h0 16'hd8 16'h0 16'h234 16'h0 16'h16 16'h0 16'h61 16'h0 16'h6c3 16'h0 16'h6b4 16'h0 16'h1 16'h0 16'h1 16'h0 16'h13a 16'h0 16'h1 16'h0 16'h1 16'h0 16'h1 16'h0 16'h0		

Bits	Default	Read/ Write	Description
	16'h0 16'h442 16'h0 16'h0 16'h0 16'h6ad 16'h0 16'h31d 16'h0 16'h6ad 16'h0 16'h1 16'h0 16'h1		

Note 1: The following shows what signals the wavetable output is connected to and how the waveform doubling works:

pix_rst_gs_row = wave_table_out[0] | (wave_doubling[0] & wave_table_out[40]) (Note 2)
pix_rst_rs_row = wave_table_out[1] | (wave_doubling[1] & wave_table_out[41]) (Note 2)
pix_tx1_gs_row = wave_table_out[2] | (wave_doubling[2] & wave_table_out[42]) (Note 2)
pix_tx1_rs_row = wave_table_out[3] | (wave_doubling[3] & wave_table_out[43]) (Note 2)
pix_tx2_gs_row = wave_table_out[4] | (wave_doubling[4] & wave_table_out[44]) (Note 2)
pix_tx2_rs_row = wave_table_out[5] | (wave_doubling[5] & wave_table_out[45]) (Note 2)
pix_rst_vsw_row = wave_table_out[6] | (wave_doubling[6] & wave_table_out[46])
rst_clamp_row = wave_table_out[7] | (wave_doubling[7] & wave_table_out[47])
s1 = wave_table_out[8]
s2 = wave_table_out[9]
amp_reset0 = wave_table_out[10]
amp_reset1 = wave_table_out[11]
avdd_pix_smpl = wave_table_out[12]
bit_bias_smpl = wave_table_out[13]
adc_buf_en = wave_table_out[14]
adc_buff_smpl = wave_table_out[15]
adc_comp_rst = wave_table_out[16]
sun_comp_en = wave_table_out[17]
sun_latch_en = wave_table_out[18]
ramp_start = wave_table_out[19] (Note 3)
ramp_rst = wave_table_out[20]
adc_transfer = wave_table_out[21] (Note 3)
column_start = wave_table_out[22] (Note 3)
row_en = wave_table_out[23]
cross_sample_ena = wave_table_out[24] (Note 3)
inj_signal = wave_table_out[25]

Note 2: The gs and rs versions of the signal are multiplexed together to one signal controlled by the shutter mode.

Note 3: While most of the wavetable signals are scalable with row clock count, these few signals are to be fixed in duration and anchored in fixed time to either the beginning or end of line.

12.43 Wave Time 1B

Name: waveTime1BReg Addr: 0xa6 -> 0x105 Reset: 0x06b40442
Description:
The wave time 1B register array provides an alternate set of timing pulses for the pixel array,
a maximum of two pulses can be programmed for each wavetable output, the minimum is zero:
Register address 15'ha6 is for waveform Signal 0 first toggle1/toggle2 pair.
Register address 15'ha7 is for waveform Signal 0 second toggle1/toggle2 pair.
.
.
.
Register address 15'he2 is unused for waveform Signal 30 first toggle1/toggle2 pair.
Register address 15'he3 is unused for waveform Signal 30 first toggle1/toggle2 pair.
.
.
.
Register address 15'hF0 is unused for waveform Signal 37 first toggle1/toggle2 pair.
Register address 15'hF1 is unused for waveform Signal 37 first toggle1/toggle2 pair.
Register address 15'hF2 is unused for waveform Signal 38 first toggle1/toggle2 pair.
Register address 15'hF3 is unused for waveform Signal 38 first toggle1/toggle2 pair.
Register address 15'hF4 is unused for waveform Signal 39 first toggle1/toggle2 pair.
Register address 15'hF5 is unused for waveform Signal 39 first toggle1/toggle2 pair.
.
.
.
Register address 15'h104 is for waveform Signal 47 first toggle1/toggle2 pair.
Register address 15'h105 is for waveform Signal 47 second toggle1/toggle2 pair.

Bits	Default	Read/ Write	Description
31:16	16'h0 16'h0	r/w	Waveform control signal toggle 2 in number of system clocks, default values are listed from highest address to lowest address.

Bits	Default	Read/ Write	Description
	16'h0 16'h0 16'h0 16'h6ad 16'h0 16'h788 16'h0 16'h792 16'h0 16'h4 16'h0 16'h78e 16'h0 16'h5ba 16'h0 16'h4d8 16'h0 16'h0 16'h0 16'h0 16'h0 16'h6b4 16'h0 16'h791 16'h0 16'h7a2 16'h0 16'h5f 16'h0 16'h4f 16'h0 16'h6ac 16'h0 16'h7e 16'h0 16'h69b 16'h0 16'h430 16'h0 16'h0 16'h0 16'h0		

Bits	Default	Read/ Write	Description
	16'h0 16'h0 16'h0 16'h7b0 16'h0 16'h3ba 16'h0 16'h7b0 16'h0 16'h6d 16'h0 16'h6b4		
15:0	16'h0 16'h0	r/w	Waveform control signal toggle 1 in number of system clocks, default values are listed from highest address to lowest address.

Bits	Default	Read/ Write	Description
	16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h442 16'h0 16'h787 16'h0 16'h1 16'h0 16'h3 16'h0 16'h78a 16'h0 16'h1c 16'h0 16'hd8 16'h0 16'h0 16'h0 16'h0 16'h0 16'h61 16'h0 16'h6c3 16'h0 16'h6b4 16'h0 16'h1 16'h0 16'h1		

Bits	Default	Read/ Write	Description
	16'h0 16'h13a 16'h0 16'h1 16'h0 16'h1 16'h0 16'h1 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h0 16'h6ad 16'h0 16'h31d 16'h0 16'h6ad 16'h0 16'h1 16'h0 16'h442		

Note 1: The following shows what signals the wavetable output is connected to and how the waveform doubling works:

pix_rst_gs_row = wave_table_out[0] | (wave_doubling[0] & wave_table_out[40]) (Note 2)
pix_rst_rs_row = wave_table_out[1] | (wave_doubling[1] & wave_table_out[41]) (Note 2)
pix_tx1_gs_row = wave_table_out[2] | (wave_doubling[2] & wave_table_out[42]) (Note 2)
pix_tx1_rs_row = wave_table_out[3] | (wave_doubling[3] & wave_table_out[43]) (Note 2)
pix_tx2_gs_row = wave_table_out[4] | (wave_doubling[4] & wave_table_out[44]) (Note 2)
pix_tx2_rs_row = wave_table_out[5] | (wave_doubling[5] & wave_table_out[45]) (Note 2)
pix_rst_vsw_row = wave_table_out[6] | (wave_doubling[6] & wave_table_out[46])
rst_clamp_row = wave_table_out[7] | (wave_doubling[7] & wave_table_out[47])
s1 = wave_table_out[8]
s2 = wave_table_out[9]
amp_reset0 = wave_table_out[10]
amp_reset1 = wave_table_out[11]
avdd_pix_smpl = wave_table_out[12]
bit_bias_smpl = wave_table_out[13]
adc_buf_en = wave_table_out[14]
adc_buff_smpl = wave_table_out[15]
adc_comp_rst = wave_table_out[16]

sun_comp_en = wave_table_out[17]
sun_latch_en = wave_table_out[18]
ramp_start = wave_table_out[19] (Note 3)
ramp_rst = wave_table_out[20]
adc_transfer = wave_table_out[21] (Note 3)
column_start = wave_table_out[22] (Note 3)
row_en = wave_table_out[23]
cross_sample_ena = wave_table_out[24] (Note 3)
inj_signal = wave_table_out[25]

Note 2: The gs and rs versions of the signal are multiplexed together to one signal controlled by the shutter mode.

Note 3: While most of the wavetable signals are scalable with row clock count, these few signals are to be fixed in duration and anchored in fixed time to either the beginning or end of line.

13 Revision History

Table 32: Revision History

Date	Revision	Description
December 2014	1	Initial Release
March 2017	2	Updated QE and Mechanical drawings
October 2017	3	Updated QE to 1100 nm, updated list of available parts
January 2018	4	Modified color QE plot, updated typical conversion gain values, updated recommended applied voltages, updated Register x27
March 2018	5	Merged LTN4625A and MST4625A datasheets
May 2018	6	Modified Reg 0x21 and 0x22. Suffix "_B3" added to part names. Modified Figure 26. Added Figures for Black Sun Protection and Bitline Clamp. Changed Reg 0x24 and Reg 0x27 recommended ADC Ramp settings. Modified LG and HG conversion gain numbers. Modified bit description for Black Sun enable (Reg 0x1 bit 4). Added section comparing Serial output to XAUI. Expanded Acronym list.
September 2020	7	Drop _B3 from part number names. Add LTN4625AF0411 as an available part number and add FX4 package drawings. Drop LTN4625AF0311 as an available part.
July 2022	8	Updated available parts list, FX3 sealed package drawings, FX3 sealed window %Transmission specifications

14 Disclaimer

BAE Systems reserves the right to make any changes to this product during an existing contract period providing it does not materially affect the form, fit or function of a Customer's next assembly product with BAE Systems' previously released design.

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