Accelerating Architectural Simulation Via Statistical Techniques: A Survey

Qi Guo, Tianshi Chen, Yunji Chen, and Franz Franchetti

***Abstract*—In computer architecture research and development, simulation is a powerful way of acquiring and predicting processor behaviors. While architectural simulation has been extensively utilized for computer performance evaluation, design space exploration, and computer architecture assessment, it still suffers from the high computational costs in practice. Specifically, the total simulation time is determined by the simulator's raw speed and the total number of simulated instructions. The simulator's speed can be improved by enhanced simulation infrastructures (e.g., simulators with high-level abstraction, parallel simulators, and hardware-assisted simulators). Orthogonal to these work, recent studies also managed to significantly reduce the total number of simulated instructions with a slight loss of accuracy. Interestingly, we observe that most of these work are built upon statistical techniques. This survey presents a comprehensive review to such studies and proposes a taxonomy based on the sources of reduction. In addition to identifying the similarities and differences of state-of-the-art approaches, we further discuss insights gained from these studies as well as implications for future research.**

***Index Terms*—Architectural simulation, design space exploration (DSE), regression, statistical methods.**

I. Introduction

When designing a processor, designers have to estimate architectural behaviors of the design before implementation and manufacture, so that the processor can meet specific design objectives. As one of the most prevalent methodologies for addressing this problem, architectural simulation has been extensively deployed since it offers designers a balance of cost, timeliness, and flexibility [1]. Application scopes of architectural simulation include but are not limited to performance evaluation, functional validation, design space exploration (DSE), and assessment of architectural innovations. In industry, all leading processor manufacturers have devised their own cycle-accurate simulators to the design of processor. For example, IBM maintains Mambo simulation environment [2], which is designed for IBM PowerPC systems, ranging from embedded system (e.g., IBM's 32-bit embedded 405GP [3]) to supercomputer (e.g., BlueGene). AMD develops SimNow simulator [4] that emulates AMD Athlon 64 and AMD Opteron uniprocessor and multiprocessor systems. Intel also uses HAsim [5] to evaluate future processor products. Architectural simulation also plays a critical role in academic research of computer systems, since it enables validations of novel research ideas without manufacturing real chips. One piece of evidence is that more than 80% papers presented at premier conferences of computer architecture research, ISCA/HPCA/Micro (2009–2011), utilized architectural simulators to validate the proposed ideas.

While the importance of architectural simulation has been widely acknowledged, the speed of architectural simulator is notoriously slow. Specifically, the speed of a cycle-accurate simulator is typically between 1 KIPS (thousand instructions per seconds) and 1 MIPS (million instructions per second) [6], which are several orders of magnitude slower than the native execution. To improve the simulator's speed, many concrete simulators have been proposed, including simulators with high abstract level (e.g., Sniper [7], [8]), parallel simulators (e.g., P-Mambo [9], SlackSim [10], and Graphite [6]), and hardware-assist simulators (e.g., FPGA-Accelerated Simulation Technologies [11], ProtoFlex [12], research accelerator for multiple processors [13], and ScalableCore [14]). An overview of the above simulators can be found in [6] and [8]. Nevertheless, even with the help of such enhanced simulators, architects and researchers still cannot afford the total simulation time in their practice. The reason is that the total simulation time is determined not only by the simulator's speed, but also by the total number of simulated instructions.

To reduce the total number of simulated instructions, recently many approaches have been proposed. The key idea of these approaches is to extract a small subset of the representative instructions from the complete set of simulated instructions by using various statistical techniques (e.g., sampling theory, regression analysis, and machine learning). Since these approaches only need to simulate a reduced number of instructions, we called them as partial simulation approaches hereinafter. Apparently, partial simulation approaches are completely orthogonal to the afore-mentioned approaches that need to greatly modify the simulators, and they can be easily applicable to state-of-the-art simulators to further improve simulation efficiency. In the rest of this survey, we will comprehensively review the partial simulation approaches.

Formally, the total number of simulated instructions (I) can be expressed as $I = N \times T$, where N is the number of instructions per simulation run and T is the number of

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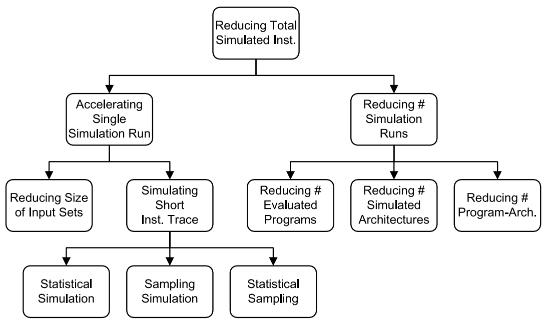

Reducing Total Simulated Inst.
Accelerating Single Simulation Run
Reducing # Simulation Runs
Reducing Size of Input Sets
Simulating Short Inst. Trace
Reducing # Evaluated Programs
Reducing # Simulated Architectures
Reducing # Program-Arch.
Statistical Simulation
Sampling Simulation
Statistical Sampling

Fig. 1. Taxonomy of partial simulation approaches.

simulation runs.[1] Based on this observation, we propose a detailed taxonomy as shown in Fig. 1, where existing partial simulation approaches are categorized into two classes. The first class focuses on reducing the number of instructions per simulation run (N), and the second class tries to reduce the number of simulation runs (T). In the first class, the approaches are further classified into two kinds, since N is mainly determined by the simulated program and its related input sets. The first kind of approaches reduce the size of input sets to reduce the simulation time, for example, the execution time of train input set could be only 25% of that of the ref input set [15]. The second kind of approaches reduce the simulation time by detailedly simulating a short instruction trace instead of the original instruction trace. There are three main approaches to achieve this goal: 1) statistical simulation; 2) sampling simulation; and 3) statistical sampling. Statistical simulation only simulates a small program synthesized from the original program based on its statistical characteristics. Sampling simulation only simulates representative traces from the original program trace. Statistical sampling simulates a small subset of instruction traces from the original program trace via statistical sampling theory. According to the reported results, these approaches can reduce the simulated instructions by about two or three orders of magnitude.

The second class of approaches focus on reducing the number of simulation runs (T). In practice, T is further determined by the number of evaluated programs and the number of simulated architectures. The main way to reduce the number of evaluated programs is called benchmark subsetting, which finds representative benchmarks among a large set of benchmarks with statistical techniques such as principle component analysis and clustering analysis. On the other hand, to reduce the number of simulated architectures, several paradigms have been proposed, such as regression modeling, ranking modeling, heuristic searching, and analytical modeling. These approaches are mainly used for DSE, i.e., finding the optimal architectures from a large architectural design space in the presence of design constraints. The key idea of these approach is to selectively simulate only a small number of architectures rather than the whole design space. In addition to the above approaches, researchers also propose several approaches to reduce both the number of evaluated programs and the number of simulated architectures simultaneously.

[1]Traditionally, the practitioners need to undergo multiple simulation runs to obtain the desired results. For example, the researchers have to run several different benchmarks on the simulators to sufficiently validate their ideas. Another more notable example is that the architects have to run thousands, even millions of simulations to explore the exponential architectural design space to find the optimal design tradeoffs.

II. Background

A. Architectural Simulator

The architectural simulators that are widely used in computer architecture research can be roughly divided into two kinds, including trace-driven simulator and execution-driven simulator.

1) Trace-Driven Simulator: In traditional trace-driven simulators, at first, traces (i.e., time-ordered records of dynamic execution stream of instructions) are collected from real applications. Then, such traces are served as inputs to drive the trace simulators to model the behaviors of the target architectures, where functional simulation is separated from detailed timing simulation. Since applications are not functionally executed in the trace-driven simulators, it can obtain a slight speed advantage over the execution-driven simulators [1]. Moreover, trace-driven simulators are relatively easier to implement than other alternatives, since they only need to consider minimal amount information that is critical to the replay of programs. However, the main drawback of trace-driven simulators is that they cannot accurately model the speculation which is common in modern superscalar architectures. Moreover, in the multicore era, trace-driven simulators suffer from the inability of capturing timing-dependent behaviors of multithreaded applications [16].

2) Execution-Driven Simulator: The execution-driven simulators combine the functional simulation and detailed timing simulation together to obtain the simulated results. Execution-driven simulators take an executable binary rather than a trace as the input, and they are extensively used in the design of modern processors. One of the most famous execution-driven simulators is SimpleScalar, which was first written by Todd Austin in 1994, and its first release was assembled, debugged, and documented by Doug Burger in 1996 at the University of Wisconsin–Madison [17]. SimpleScalar provides five execution-driven simulators in the release, ranging from the simplest (and fastest) functional simulator to a detailed, out-of-order (OOO) superscalar processor simulator. RSIM [18] is another execution-driven simulator mainly targeting shared-memory multiprocessors with instruction-level parallelism (ILP) processors. It executes the instructions OOO together with the timing model, and it supports accurate memory consistency and wrong path simulation. Actually, RSIM sacrifices simulation speed for accuracy.

To facilitate the design of multicore processors, several multicore execution-driven simulators have been developed. One of the most notable examples is SuperESCalar simulator (SESC). SESC can characterize a variety of architectures, including dynamic superscalar processors, chip-multiprocessors (CMPs), processor-in-memory, and speculative multithreading architectures. The main targets of SESC are to provide a fastest simulator, make the code understandable and extensible, and offer many flexible configurations for architects. Simics is a commercial full system simulator [19], and it can support detailed simulation of multiprocessors with the help of general execution-driven multiprocessor simulator (GEMS) [20]. Currently, GEMS is no longer maintained, and the main efforts are shifted to the development of gem5 simulator system [21], which merges the advantages of M5 [22] and GEMS. The gem5 simulator provides a highly configurable simulation framework, multiple instruction set architectures, diverse CPU models, and a flexible memory system for modeling modern processors. MARSSx86 is a fast, cycle-accurate, full-system multicore simulator for x86-64 architecture [23], and it is built upon PTLsim [24].

Another kind of simulators heavily rely on dynamic binary instrumentation tools (e.g., Pin [25]) to feed information to the timing models. For example, CMP$im [26] employs the Pin tool to generate memory information on-the-fly to feed the cache model for the investigation of the cache system on multiprocessors. Other examples include Graphite [6], Sniper [8], and ZSim [27]. Since the applications are functionally emulated/executed on the host natively, these simulators are relatively fast. For example, ZSim can achieve up to 300 MIPS to model a chip with 1024 OOO cores.

B. Usage of Architectural Simulation

The application scopes of architectural simulation are very broad, including performance evaluation, functional validation, DSE, assessment of architectural innovations, as well as software performance tuning.

1) Design Space Exploration: DSE is widely considered as one of the fundamental problems during the design of computer systems. The silicon advances significantly increase the complexity of processors, which leads to a large number of design parameters (e.g., cache size, reorder buffer size, and number of cores) to decide. This problem is further exacerbated for heterogeneous architecture [28]. In DSE, cycle-accurate architectural simulators are indispensable tools for evaluating complicated and subtle design tradeoffs with respect to large design spaces, and handling various design constraints (e.g., power/area/thermal constraints and quality of service requirements). In order to achieve efficient and effective DSE, architectural simulators should be portable, flexible, accurate, and fast.

2) Assessment of Architectural Innovations: Assessment of architectural innovations relies heavily on architectural simulation during the early design phase. In the absence of a real system, architectural simulation offers a cost-effective way of evaluating architectural innovations. For instance, photonic interconnection network has been acknowledged as one of the most promising techniques to provide low-latency, ultrahigh-bandwidth, and low-power network for intracore communications. However, silicon-photonic integration is still expensive and has to face several challenges in manufacture. Under this circumstance, several photonic on-chip interconnect network simulators, e.g., PhoenixSim [29], have been developed to evaluate the effectiveness of such architectures.

3) Software Performance Debugging and Tuning: Although the architectural simulation is mainly employed for the architectural design of processors, it can also support various tasks in software engineering, including performance analysis, debugging, and testing of software. For example, Albertsson and Magnusson [31] proposed to leverage full system simulation (i.e., Simics simulation environment [19]) to build a temporal debugger to analyze real-time properties of software [30], [31]. In the above debugger, the predictable, nonintrusive debugging environment for checking temporal errors should be attributed to the deterministic characteristics of deployed architectural simulators.

C. Statistical Methods

1) Statistical Concepts: Here, we introduce several basic statistical concepts that are closely related with partial simulation approaches. Sampling theory and hypothesis testing are two of the core concepts in statistic. Both of them are utilized to provide statistically rigorous approximation to the estimated results offered by simulators.

TABLE I
SAMPLING VARIABLES

	Population Variables	**Sample Variables**
size	N	n
mean	μ	$\bar{x}$
standard deviation	σ	s
variation coefficient	c_v	$\widehat{c}_v$
confidence level	-	C
confidence interval	-	$\pm\theta$

a) Sampling theory: In practice, statistical analysis is conducted on a chosen subset of the entire population, since it is usually impossible to get all data from the entire population. A subset of the entire population is also called a sample, and how to choose a sample to estimate the property of the entire population is investigated by sampling theory. In our application, sampling theory is used to determine a proper sample of instructions that can best characterize the property of all simulated instructions [32].

As a basic type of sampling techniques, simple random sample (SRS) is widely used, where each individual of the population has the same possibility to be chosen. Table I gives the statistical variables that are used to characterize the property of population and sample in SRS. In SRS, a sample of n individuals are selected at random from a population of N individuals. The analysis of the entire population is usually conducted on the n sampled individuals, and the true population mean μ is estimated by the sample mean $\bar{x}$. The variation coefficient c_v is the standard deviation σ normalized by mean, that is, $c_v = \sigma/\mu$ and $\widehat{c}_v = s/\bar{x}$ are calculated for the population and the sample, respectively. Similar to the standard deviation, variation coefficient can also be used to measure the dispersion of a probability distribution. However, the standard deviation can be directly used to construct confidence interval, which is expressed as an interval to indicate the reliability of a mean estimate. In more detail, confidence interval can be calculated as $\theta = z(\sigma/\sqrt{n})$, where z is the upper $(1-C)/2$ critical value for the standard normal distribution. Here C could be interpreted in such a way that there is a C probability that $\bar{x}$ is with the range of $\pm\theta$ of μ. Thus, for a sample with given standard deviation σ and size n, the achieved confidence interval varies along with specified confidence level.

b) Statistical hypothesis testing: Another important concept in statistics is statistical hypothesis testing (SHT), which is a systematic method to make decisions using experimental data. The most representative usage of SHT in computer architecture is to evaluate the performance comparisons of different simulation runs [33], even native computer systems [34].

There are several components to define when conducting the hypothesis testing, as shown in Table II. Hypothesis testing always begins with a statement of the value of a population statistic containing the condition of equality, e.g., $\mu = 0.5$, and such statement is called as null hypothesis, denoted as H_0. On contrary, the alternative hypothesis is the statement that must be accepted if the null hypothesis H_0 is rejected (i.e., false). Based on null hypothesis, one can calculate the probability of the observation under H_0, which is called p-value. Once p-value is less than a user specified significance level,

TABLE II
TERMS IN SHT

	Term	Notes
null hypothesis	H_0	A statement of a population parameter
alternative hypothesis	H_1	The statement accepted if H_0 rejected
significance level	α	degree of confidence
p-value	p	determine whether or not reject H_0

α (the most commonly used values are 5% and 1%), the null hypothesis will be rejected at the given level of significance. In this condition, the alternative hypothesis will be accepted to reach a statistically rigorous conclusion.

2) Regression Analysis: Regression analysis focuses on characterizing the relationship (i.e., regression function) between a dependent variable and one or more independent variables. It is mainly used for prediction and forecasting, e.g., predicting the performance (dependent variable) of architectural parameters (independent variables) in architectural simulation, which may partially overlap with the field of machine learning that will be detailed later. There are two kinds of regression techniques: 1) parametric and 2) nonparametric regression. Parametric regression implies that the form of regression function is predefined, only the corresponding parameters should be estimated from the observed data. On contrary, nonparametric regression does not give assumptions on the concrete form of the regression functions, thus, large sample size is required to construct the model structure and model estimates. Actually, both parametric (e.g., linear regression) and nonparametric regression (e.g., spline function) have been utilized for performance/power modeling to accelerate architectural simulation.

Linear regression is one of the most notable parametric regression techniques, where the dependent variable is a linear combination of the parameters (rather than the independent variables). A general linear regression model can be written as

$$y_i = \beta_1 x_{i1} + \beta_2 x_{i2} + \cdots + \beta_p x_{ip} + \epsilon_i$$

where x_{ij} is the ith observation on the jth independent variable, and ϵ is an error term. The main task of regression analysis is to determine the concrete value of $\beta_j (1 \leq j \leq p)$ via, typically, least square approaches.

Interpolation is a technique to create new data points within the range of a set of already known data points, which is basically a nonparametric regression technique. Spline interpolation is a special interpolation technique where smooth piecewise polynomial function, called spline, is utilized to predict the value of dependent variable. Spline is divided into polynomial intervals, and such intervals are connected by knots. Actually, the number and location of knots are critical to the approximation between the spline function and real data.

3) Machine Learning: Machine learning focuses on the study of algorithms that can automatically improve the performance through experience [35]. It has already been widely used in the community of computer architecture, e.g., resource allocation [36], task scheduling [37], hardware reconfiguration [38], and architectural optimization [39]. Here, we present several basic but critical concepts of machine learning.

In a traditional machine learning problem, given a training set consisting of n training data, each data is a pair of objects denoted as $(\mathbf{x}_i, y_i)$, where $\mathbf{x}_i \in \Re^d$ is the training example and $y_i \in \Re$ is the corresponding label of $\mathbf{x}_i$, learning algorithms (learners) try to find an appropriate inferred function (or model) $f : \Re^d \rightarrow \Re$ that implements the optimal mapping. Then, for a new example $\mathbf{x}_j$, learned function could generate the predicted output y_j as $f(\mathbf{x}_j)$. In particular, for a binary classification task the label y_i is a binary variable such as $y_i \in \{-1, 1\}$. In contrast, in a regression task the label y_i is a continuous variable. Actually, such a learning problem is a typical supervised learning problem since the learning process is performed on supervised training data, i.e., training examples and their corresponding labels. On the other hand, unsupervised learning indicates that the training set only contains training examples without labels, and the learning process is conducted directly on the original example $\mathbf{x}_i$. According to these concepts, it is easy to derive the definition of semisupervised learning, that is, the training set contains both labeled and unlabeled training examples. Actually, all three kinds of learning techniques stated above have been leveraged to accelerate the architectural simulation by researchers in the community of computer architecture.

III. Accelerate Single Simulation Run

As stated, the simulation cost of a single simulation run is primarily determined by the evaluated program and its input sets. Thus, there are two categories of approaches to accelerate a single simulation run, that is, reducing size of input sets and simulating a short instruction trace. We will detail each category in the following sections.

A. Reducing Size of Input Sets

The first category of approaches to accelerate single simulation run is to reduce the size of input sets. MinneSpec [40] is one of the earliest investigations that fall in this category, which is a reduced input set for standard SPEC CPU2000 benchmark suite. SPEC CPU2000 benchmark suite contains three standard data sets: 1) test; 2) train; and 3) ref, whose scales increase in order. Among these data sets, programs running with the ref data set exhibit the most similar behaviors to real-life applications, and MinneSpec tries to provide a small data set to reasonably mimic the behavior of the ref data set. MinneSpec is developed by modifying the input commands, providing new input files, or modifying/truncating/replacing ref files for all benchmarks in SPEC CPU2000. By comparing several statistical characteristics, such as the instruction mixture and memory behaviors, of MinneSpec with the original ref data set, the authors found that MinneSpec can reasonably mimic the behavior of ref data sets of SPEC CPU2000 benchmarks. However, although MinneSpec has been recognized by SPEC and distributed with Version 1.2 of SPEC CPU2000, it is not widely used for evaluating existing modern architectures. Eeckhout *et al.* [41] later validated that such reduce input sets are only representative for some programs, but not for others.

Hsu *et al.* [42] compared several statistical characteristics, e.g., instruction per cycle (IPC), execution paths, and path coverage, among test, train, and ref, and they found that both test and train input sets have significant different characteristics to that of ref data sets for several benchmarks. Thus, such input data sets may not be suitable for profile-based optimization or validation of research ideas, since the results of performance evaluation conducted on these data sets could be misleading.

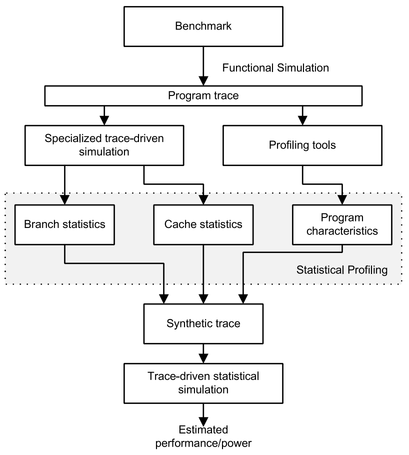


Fig. 2. General framework of statistical simulation process.

B. Simulating Short Instruction Trace

This category of approaches focuses on simulating a shorter instruction trace than the original instruction trace of a given program and its inputs. There are three different approaches, i.e., statistical simulation, sampling simulation, and statistical sampling.

1) Statistical Simulation: The basic idea of statistical simulation [43], [44] is to reconstruct a synthetic, small program based on the statistical profiles (e.g., distribution of instruction types and branch behaviors) that are extracted from the detailed simulation of the original benchmark. Thus, simulation efficiency can be improved by replacing the original large-scale program with a small synthetic version. Typically, statistical simulation consists of four steps: 1) program trace generation; 2) statistical profiling; 3) synthetic-trace generation; and 4) trace-driven simulation [44], as shown in Fig. 2. At first, the program traces of given benchmarks can be generated by functional simulation. Then, the profiling tools extract a set of statistical characteristics from such traces, and there are two kinds of statistical profiling tools to accomplish this task. The first is the microarchitecture-independent profiling tools that only analyze the functional operations of the program instructions and produce microarchitecture-independent characteristics, such as instruction mix and instruction dependencies. The second tool is specialized cache/branch predictor simulators to collect the cache and branch behaviors from the program trace, and these characteristics are closely related to concrete architectures. The complete set of such statistical characteristics are then used to generate a synthetic trace with the same statistical properties. Finally, such synthetic traces can be efficiently executed on a trace-driven simulator to obtain corresponding performance/power results. Obviously, the effectiveness of statistical simulation should be measured by comparing the simulated performance/power results of the original program traces and the corresponding synthetic traces. For SPECint95 benchmarks, statistical simulation results in about 10% and 5% relative error for IPC and power, respectively, while the number of simulated instructions can be reduced by several orders of magnitude.

The selection of statistical characteristics is very crucial to the accuracy of statistical simulation. Initially, basic block size, instruction mixture, cache hit rate, etc., are treated as statistical characteristics in a statistical simulator high-level synthesized (HLS) [45]. In addition to such statistical characteristics, Eeckhout *et al.* [46] proposed to utilize control flow graph to characterize the control flow behaviors to enhance the accuracy of statistical simulation. Besides, they also showed that delayed update[2] should be considered when characterizing branch behavior. Based on the experiments conducted on an eight-way superscalar processor, the average error is 6.6% and 4% for predicting performance and energy, respectively, using SPECint 2000 benchmarks.

To facilitate the design of CMPs, Genbrugge and Eeckhout [48], [49] further extended statistical simulation to multithreaded programs. They proposed several statistical characteristics of the cache access behaviors, for example, the probabilities of set access and per-set least recently used stack distance. Besides, they also showed that it is important to model the time-varying behavior to accurately capture the conflict behavior in accessing shared resources. Experimental results demonstrate that the average IPC prediction error is less than 5.5% while the simulation speed-up can achieve 40× to 70×.

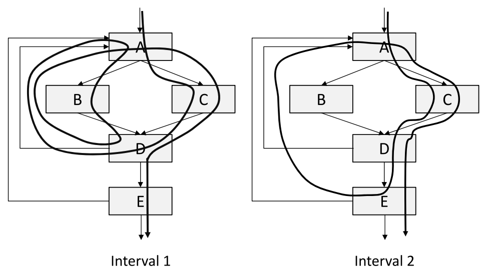
Hughes and Li [50] also extended statistical simulation to multithreaded programs for CMPs. They proposed to build synchronized statistical control flow graphs with the behaviors of interthread synchronization and sharing patterns, so as to capture the interactions between threads. Moreover, the memory access is captured by thread-aware data reference models, and the branch behavior is captured by wavelet-based branching models. For the evaluated SPLASH-2 benchmarks, this approach results in IPC errors from 3.8% to 9.8% and the simulation time has been reduced by more than an order of magnitude.

Recently, graphics processing units (GPUs) have been employed to speed-up the general-purpose applications, leading to GPGPU computing. However, as GPGPU architectures have many parallel hardware threads, current sequential cycle-accurate GPU simulators such as GPGPU-Sim [51] take a long time for simulation. To speed-up the simulation of GPGPU architectures, Yu *et al.* [52] proposed to synthesize small benchmarks with a reduced number of iterations compared against the original workloads. To generate such small benchmarks, several static and dynamic characteristics are collected from the original workloads. Experimental results show that the speed-up of this approach is 88× on average compared with GPGPU-Sim.

2) Sampling Simulation: Different from statistical simulation that reconstructs new small synthetic programs, sampling simulation directly extracts a small fraction of representative instructions from the original instruction trace. Compared with the full simulation with billions of instructions, this approach only needs to simulate several millions of instructions. The most well-known approach is SimPoint [53].

SimPoint is proposed by Sherwood *et al.* [53], [54] based on the concept of basic block vectors (BBVs). For a given interval of execution (e.g., 100 million instructions), a BBV is an array where each element represents a basic block in the original program. More specifically, each element in a BBV is the weighted count of how many times the related basic block has been executed in this interval. Thus, BBV is

[2]It refers to the timing to update the predictor with branch results [47]. In a typical pipelined processor, the branch is predicted in the fetch stage, but the predictor is updated in the commit stage.



	A B C D E
Interval 1	<3, 1, 2, 3, 1>
Interval 2	<2, 0, 2, 2, 2>
Manh. Dist	<1, 1, 0, 1, 1> = 4

Fig. 3. Illustrative example to compute the similarity between two execution intervals.

an architecture-independent metric that can characterize the behavior of arbitrary execution intervals in a program. To compare the behaviors of execution intervals, the Manhattan distance is utilized to measure the similarity between different BBVs. An illustrative example to demonstrate the computation of similarity between two execution intervals is shown in Fig. 3. There are two execution intervals in this example. For interval 1, since basic block A has been executed for three times, the value of its corresponding element in BBV is 3. We can easily determine the value of other elements in the BBVs of intervals 1 and 2. Then, the similarity (i.e., Manhattan distance) of these two execution intervals is calculated as 4.

Based on the similarity metric of different intervals, K-means clustering analysis is conducted to find the representative intervals that are closest to the center of corresponding cluster for simulation, and these simulation intervals are called simulation points. After conducting detailed simulations on the set of simulation points, a weighted average for IPC can be computed to approximate the performance of the entire program's execution. Experimental results show that by creating multiple simulation points (≤ 10), the average IPC error is only 3% compared with the entire execution. Moreover, the detailed tuning of SimPoint is also discussed in [55].

Van Biesbrouck *et al.* [56] further extended the SimPoint methodology to estimate the performance of simultaneous multithreading machines. The key idea is using the co-phase matrix to represent the combinations of execution phases from different programs that are running simultaneously, and each entry in the matrix is the combination of the phase-IDs, called as co-phase identifier. Then, the co-phase matrix is used to determine fast-forwarding of threads between samples, and estimate the performance of detailed simulation as well. On the evaluated program pairs, this approach results in an error rate of 4% on average, at the costs of only 1% of the full simulation.

The profiled information of SimPoint is collected via simulation techniques, which may not be able to reproduce the complex execution environment required by some real applications. Besides, it is often hard to port the latest version of complicated applications to simulators. To address such problems, a toolkit called PinPoint is created by Patil *et al.* [57]. PinPoint is built upon SimPoint methodology and a dynamic instrumentation tool, Pin [25], to automatically find the representative execution intervals at run time on commodity computers.

Huang *et al.* [58] proposed to employ the sampling technique for reducing the simulation cost of GPGPU architectures. The proposed sampling technique includes interlaunch sampling and intralaunch sampling, to select representative kernel launches and instructions within one kernel launch, respectively. The interlaunch sampling is achieved by selecting a kernel launch from a group of kernels having similar characteristics. The intralaunch sampling is achieved by selecting the thread blocks with approximate performance. On the evaluated kernels, the sample size of TBPoint is 2.6% with a sampling error as 0.47%.

3) Statistical Sampling: In contrast to SimPoint that uses clustering analysis to find representative traces, there are also several studies employing statistical sampling theory to reduce simulation traces. Conte *et al.* [59] proposed the state-reduction method to statistically sample the simulation traces, which is, to the best of our knowledge, the first piece of work that applies statistical sampling to processor simulation. The accuracy of the approach is guaranteed by reducing the sampling bias (e.g., standard error) and nonsampling bias (e.g., branch predictor state).

Sampling microarchitecture simulation (SMARTS) selects a small subset of instruction traces from the original instruction trace with a specified confidence interval via statistical sampling theory [32], [60]. In SMARTS, a sampling unit is defined as U consecutive instructions in the program's instruction trace. When the total number of instructions is L, the number of total sampling units N equals L/U. According to statistical sampling theory, the required confidence on the estimation of cycle per instruction (CPI) of the entire program execution can be determined by the number of samples (recall n in Table I) from N sampling units, and number of samples n can be dynamically adjusted according to the coefficient of variation of CPI ($\widehat{V}_{\text{CPI}}$). In SMARTS, suppose sampling begins at offset j, that is, detailed simulation is performed at unit j and lasts for U instructions. Then, SMARTS fastforwards $U(k-1) - W$ instructions with only functional simulation, and subsequently W instructions for warming-up are executed via detailed simulation. Experimental results show that for typical applications, a sample size of $n = 10\,000$ units with unit size $U = 1000$ can achieve 99.7% confidence of $\pm 3\%$ error.

In SMARTS, to produce unbiased estimates, the functional warming period is the dominant part of entire simulation. To eliminate the functional warming bottleneck, Wenisch *et al.* [61] further proposed TurboSMARTS, which chooses a minimal subset of warmed states and stores them in checkpoints. Therefore, subsequent experiments can directly load the states from such checkpoints to improve the simulation efficiency. TurboSMARTS maintains the same accuracy of existing simulation sampling approaches while achieves over 250$\times$ speedup.

4) Multiprocessor Sampling: SimFlex [62], [63], which is a fast and accurate full-system simulator built upon Simics simulation environment, applies SMARTS methodology to rapidly choose a representative sample of each workload. A key innovation of SimFlex is that it applies statistical sampling techniques to multiprocessor programs. A multiprocessor program execution consists of multiple instruction streams with nondeterministic communications among them, which makes it hard to find the optimal sample of the full program. SimFlex tackles this problem by focusing on the critical path of multiprocessor execution. In more detail, in order to estimate the execution time of the full program, it is unnecessary to consider none-critical-paths since they do not contribute to the overall execution time. By only considering the program sections on the critical path, the sampling process can be treated as a (uniprocessor-like) interleaving of executions across different processors.

In traditional instruction-based sampling such as SimPoint and SMARTS, the original execution is sampled based on a fixed length of instructions, leading to the divergence of execution progress among threads. In this case, the overlap of different threads may not be the representation of the actual behavior of a multithread application. On contrary, the time-based sampling (TBS) samples the original execution based on a fixed number of cycles, preserving the progressed time of the original execution [64]. Therefore, TBS is able to sample the simulation of multicore processors with no limitation in terms of application type (e.g., multithreaded, multiprogrammed, or both) and architecture heterogeneity. TBS is further implemented as an open source simulator, called enhanced SESC or ESESC. Similarly, Carlson *et al.* [65] proposed to track simulated time rather than instruction count for multithreaded applications. Besides, they also consider the application synchronization events during the fast-forwarding to improve the prediction of application execution. Recently, Carlson *et al.* [66] further proposed BarrierPoint to accelerate sampling simulation by using globally synchronizing barriers in multithreaded applications. The key idea of BarrierPoint is that it only simulates a selected number of representative interbarrier regions, from which the total application execution time can be predicted. BarrierPoint automatically identifies most representative regions by conducting clustering analysis on the microarchitectural independent characteristics of all regions. Compared with prior TBS techniques, BarrierPoint is more efficient since it eliminates full-application functional simulation and it can be simulated in parallel.

IV. Reducing Total Simulation Runs

In the design phase of processors, the total number of simulation runs can be determined by the number of evaluated programs and the number candidate architectures. Thus, the reduction of total simulation runs can be considered from these two aspects.

A. Reducing Evaluated Programs

In the recent years, the number of computer applications increases significantly, which results in a large number of benchmarks to evaluate during the design phase of computer systems. For example, the designers of general-purpose processors often need to consider SPEC CPU benchmark suits (e.g., SPEC CPU2000/2006), MiBench, and PARSEC in performance evaluation. It is quite time-consuming to simulate all these programs due to extremely slow simulation speed. The situation is further exacerbated with the ever-increasing scale of the input sets of modern programs. Therefore, many investigations try to reduce the number of evaluated programs during architectural design based on the observation that there always exists statistical redundancy among benchmarks.

Eeckhout *et al.* [67] proposed to use principal components analysis (PCA) as a statistically rigorous way to select a representative subset from a benchmark suite. In their paper, several program characteristics are proposed to characterize each benchmark. These characteristics include instruction mix, branch prediction accuracy, *D*-/*I*-cache miss rate, sequential flow breaks, and ILP. Such characteristics are extracted via profiling tools at first. Then, PCA is employed to obtain the uncorrelated principal components, which can reduce the dimensionality of the data and generate better clustering results. Finally, different benchmarks are clustered based on the Euclidean distances. Through choosing one benchmark from each cluster, a representative subset of the benchmark suit can be constructed.

Eeckhout *et al.* [68] further proposed to use several microarchitecture-independent characteristics to find a set of representative program phases for simulation. Such microarchitecture-independent program characteristics are also used to measure the similarity among benchmarks, and then clustering analysis is utilized to group similar benchmarks together [69]. Following the basic idea of benchmark subsetting, only representative programs in each group are used to subset the original benchmark suite for efficient simulation. For the SPEC CPU2000 benchmark suite, by using eight representative programs to subset the entire benchmark suite, the error in average IPC is less than 5%, and by using five representative programs to subset all the 32 MiBench and MediaBench benchmarks, the error in average IPC is less than 3.9%. Actually, the proposed microarchitecture-independent characteristics can be used not only for finding representative program subset but also for performance prediction [70], performance optimization [71], and compiler optimization [72].

Yi *et al.* [73] proposed to use the Plackett and Burman (P&B) design to determine the critical parameters of the performance. The effects of parameters are determined by the magnitudes that are computed by using the P&B matrix and the simulated results (e.g., execution time). Then, the similarity among benchmarks is measured by the rank of effects of all parameters. Finally, such similarity is utilized to determine the representative benchmarks for simulation.

Phansalkar *et al.* [74], [75] analyzed the redundancy and application balance in the SPEC CPU2006 benchmark suite. They applied multivariate statistical analysis techniques such as PCA and hierarchical clustering analysis (HCA) to identify the similarity among SPEC CPU2006 programs. According to their evaluation, using four and six benchmarks to subset the entire CINT2006 benchmarks lead to 5.8% and 3.8% average performance errors, respectively. Also, using six and eight benchmarks to subset the entire CFP2006 benchmarks achieve 10.8% and 7% average performance errors, respectively.

Jin and Cheng [76] also proposed a benchmark subsetting methodology and conducted a case study using a bioinformatic benchmark suite called ImplantBench. Their methodology contains two steps. First, factor analysis is employed to reduce the dimensionality of benchmark characteristics and HCA is utilized to demonstrate the inherent correlation and similarities among programs. In the second step, a distance-based program selection strategy is proposed to select the subset of benchmarks given desired workspace variance coverage. Moreover, Jin and Cheng [77], [78] further proposed a general benchmark subsetting framework based on evolutionary algorithms, where a subset of given benchmark suite can be generated based on the microarchitecture-independent characteristics, desired workload space coverage, and total execution time.

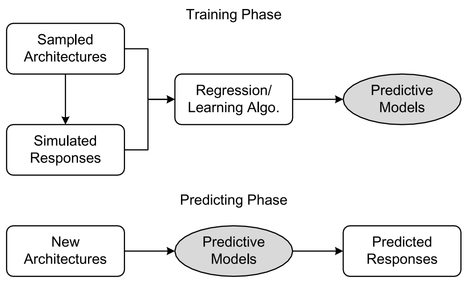


Fig. 4. Reducing simulated architectures via predictive modeling techniques.

B. Reducing Simulated Architectures

1) Predictive Modeling: In the design phase of processors, there always exists a large number of candidate architectures for evaluation. To reduce the candidate architectures, Yi *et al.* [73] proposed to use the P&B design to determine the critical parameters of the performance. To further reduce the simulated architectures, predictive modeling techniques have been proposed recently. The basic idea of predictive modeling technique is to simulate a subset of architectures to build predictive models that can rapidly estimate the performance/power of all candidate architectures.

The basic flow of applying predictive models for DSE can be divided into two phases: 1) the training phase and 2) the predicting phase as illustrated in Fig. 4. In the training phase, a small fraction of architectures in the entire design space are sampled for simulation to obtain the simulated processor responses (e.g., performance, power, and area). Then, the simulated architectures will be treated as the training data to build predictive models via various learning/regression algorithms. In the predicting phase, such predictive models can be utilized to predict the responses of any architectures that are not involved in the training phase without additional simulation runs. Since the responses of all candidate architectures can be estimated by the predictive models, it is relatively trivial to find the optimal architecture via directly comparing the predicted results of all architectures.

Joseph *et al.* [79] first proposed to use linear regression models to characterize the relationship between design parameters and processor performance. Since linear regression models can directly quantify different impacts of design parameters on performance, it can provide more insights and opportunities for performance optimization. To validate this approach, they conduct experiments on a design space containing 26 different variable design parameters. According to the built linear model, it can be concluded that the depth of pipeline, reorder buffer, and the size of issue queue are three most critical design parameters on the processor performance for the evaluated design space.

Although linear models are shown to be capable to provide accurate estimation of the significance of design parameters and their combination, they cannot accurately capture the nonlinear relationship between design parameters and processor responses. Thus, a widely used nonlinear model, radial basis function (RBF) networks, is used to construct accurate predictive models at low simulation costs [80]. According to experiments on SPEC CPU2000 benchmark suite, such nonlinear models only result in 2.8% average error in CPI across the design space. Lee and Brooks [81] also observed that there exists nonlinear relationship between architectural parameters and performance. They proposed to use spline functions for building predictive models. More specifically, restricted cubic splines are utilized to capture the complex, highly curved relationships between parameters and performance/power. They conducted experiments on a design space that contains nearly 1 billion architectures, and by sampling 4000 architectures for training model, the mean prediction errors for performance and power are 4.1% and 4.3%, respectively. In fact, spline function is also used for Pareto frontier analysis, pipeline depth analysis, and processor heterogeneity analysis [82], [83]. Recently, spline function is also used by Wu and Lee [84] to construct predictive models to explore the hardware–software co-spaces.

Lee *et al.* [85] further proposed the composable performance regression (CPR) to efficiently build scalable models for multiprocessors. This paper focuses on efficiently predicting the performance of multiworkloads running on multiprocessors, while previous predictive modeling techniques only estimate the performance of a single (either single-threaded or multithreaded) workload. The CPR model consists of uniprocessor, contention, and penalty models to produce the performance estimation of multiprocessors at the costs of a small number of simulations. In more detail, given a set of benchmarks $B = B_1, \ldots, B_n$ running on a n-core multiprocessor, at first CPR iteratively estimates the performance of each benchmark in B. For one specific benchmark B_i, CPR framework also predicts its contention indicator when it contends with other benchmarks in the set B for shared resources (such as LLC, memory controller). Finally, a penalty model is used to combine the baseline performance of B_i and the contention indicator together to obtain the estimated performance of B_i when running with other benchmarks in the set B. Actually, the uniprocessor model and contention models are also trained by cubic spline function on the full parameter space and shared resource space, respectively.

Artificial neural networks (ANNs) are considered as one of the most powerful and popular learning algorithms in real applications. İpek *et al.* [86], [87] proposed to utilize ANNs to capture the relationship between architectural parameters and performance/power. Besides, to reduce the number of sampling architectures to build a model meeting specific accuracy constraints, intelligent sampling is used to achieve an efficient training process. The experiments on the design spaces of a memory subsystem and a CMP system validate that ANN-based regression models generally predict IPC with 1%–2% error, while reducing the required simulation runs by two orders of magnitude compared with the full simulation.

Cook and Skadron [89] advocated to use genetic programming (GP) to create polynomial functions (or response surface) to characterize the relationship between the performance and architectural parameters. The original GP is used to optimize a population of programs based on evolutionary biology. A distinguish feature of this approach is that the predictive function is modeled as a expression tree, where each node represents a user-defined operator (e.g., simple arithmetic operators, a square operator, and a logarithmic operator) or a design parameter. Then GP imposes evolutionary process (i.e., selection, crossover, and mutation) to this expression tree to obtain the predictive functions. Thus, the predictive functions are built automatically and explicitly. They conducted experiments on the data sets investigated in [81] and [86], and experimental results demonstrate that this approach can obtain highly accurate predictive functions at the cost of a few detailed simulation runs.

In contrast to previous predictive modeling techniques that are only evaluated by the prediction accuracy on different architectures, another kind of work focuses on improving the quality of predicted Pareto set that represents the architectures with best performance/energy tradeoffs. Palermo *et al.* [90] investigated four regression models, i.e., linear regression, shepard-based interpolation, ANNs, and RBFs, to predict the performance and energy. The Pareto sets found by these predictive models are compared with the actual Pareto set with the metric average distance from reference set.[3] Experimental results demonstrate that ANNs achieve the best performance among investigated four models in their proposed DSE framework.

Actually, the afore-mentioned approaches only consider supervised learning techniques to model the relationship between design parameters and processor responses, that is, only simulated architectures are utilized for model construction. Inspired by recent advances on semisupervised learning,[4] Guo *et al.* [91] proposed the co-training model tree (COMT) approach to exploit unlabeled architectures to improve the accuracy of predictive models. To be specific, COMT works in a co-training style, where two learning models label unlabeled architectures for each other. According to their experiments, COMT outperforms ANN-based model given the same number of simulated architectures via random sampling. Moreover, Chen *et al.* [92] proposed the COAL approach that combines semisupervised learning and active learning[5] together to further improve the performance of predictive models.

In addition to the above regression-based approaches, recently Chen *et al.* [93] proposed a ranking-based approach for DSE. The key observation is that architects mostly need the relative ranking of two architectures, rather than accurately estimating the performance of each architecture. Thus, by formulating the DSE as a ranking problem, ArchRanker is proposed to train ranking models to predict the relative ranking of architectures. Experimental results show that ArchRanker can not only more accurately predict the relative ordering of two architectures, but also require much fewer simulation runs to obtain the same accuracy compared with ANN-based regression models. To facilitate the design of heterogeneous systems, Mariani *et al.* [94] proposed the DRuiD framework to rank different heterogeneous architectures for a target functionality. Specifically, DRuiD uses machine learning approaches (i.e., random forests and genetic algorithms) to determine the most suitable computational element (e.g., the hardware accelerator implemented on the FPGA) to be used for a certain application kernel.

With the developing of machine learning techniques, it is expected that more opportunities could be provided to further reduce the number of simulated architectures for training accurate predictive models.

2) Heuristic Searching: In contrast to predictive modeling techniques that explicitly construct approximate functions between design parameters and processor responses, another methodology uses heuristic searching algorithms (e.g., evolutionary algorithms) to directly find the most promising architectures under design constraints. In other words, such methodology treats DSE as a multiobjective optimization (MOO) problem, and by solving this problem, the number of indispensable simulated architectures can be significantly reduced.

In order to identify the promising architectures with best performance/energy tradeoffs for a superscalar architecture, Palermo *et al.* [95] formed this problem as an MOO, and proposed a DSE framework based on heuristics algorithms. Moreover, the authors compared the effectiveness of three heuristic algorithms: 1) random search; 2) simulated annealing; and 3) tabu search, to reduce the overall simulation runs. Experimental results show that the proposed framework can reduce the number of simulation runs up to three orders of magnitude compared to an exhaustive search strategy.

Ascia *et al.* [96] combined multiobjective evolutionary algorithms and fuzzy systems together to reduce the simulation costs of an SoC platform. Multiobjective evolutionary algorithms are used as exploration heuristic to approximate the Pareto set, and fuzzy systems are used to accelerate the evaluation of each configuration via predicting the performance rather than simulation. They conducted experiments on a highly parameterized SoC platform, and experimental results demonstrate that this approach can improve the quality of Pareto set and reduce simulation costs for a given set of multimedia applications.

Recently, Mariani *et al.* [97] proposed an iterative DSE approach to derive the most promising architectures via correlation-based models. In each iteration, only the architecture with the maximal expected improvement over present Pareto set is considered for simulation. This architecture with maximal expected improvement is selected by using a single objective genetic algorithm. Such an evolutionary process continues until the Pareto set is unchanged or a maximum number of simulation runs has been reached. Comparing with several mature MOO algorithms (including the notable NSGA-II [98]), this approach can speed up the overall exploration phase up to 65%.

Mariani *et al.* [99] proposed the DeSpErate++ framework to exploit predictive models to improve the DSE efficiency on a parallel computing platform. More specifically, an estimation of distribution algorithm is applied to heuristically identify the distribution of optimal design configurations in the design space. Orthogonally, a predictive model such as ANN is exploited to predict the simulation time of architectural configurations to organize their schedule over a parallel computing system.

Actually, in [90], [96], [97], and [99], predictive modeling (such as those described in Section IV-B1) is exploited in orthogonality to heuristic optimization approaches (such as the ones described in [95] and [98]) to achieve high DSE efficiency.

3) Analytical Modeling: In contrast to afore-mentioned empirical models such as ANNs that treat the processor as a "black box," mechanistic analytical models are derived from the internal mechanisms of processors to estimate the performance without detailed full simulation. Karkhanis and Smith [100] proposed a first-order model to predict the performance of superscalar processors. The basic idea is to first count the miss events (e.g., branch misprediction

[3]It measures the distance to the actual Pareto set of entire design space.

[4]As stated in Section II-C3, semisupervised learning techniques leverage unlabeled training examples to enhance the prediction accuracy given limited labeled training examples.

[5]In active learning, selected unlabeled architectures are actively sent for simulation to improve the modeling accuracy.

and cache misses) through relatively simple trace-driven simulation, and then the performance penalties caused by such miss events are added to the ideal CPI.

Eyerman *et al.* [101] proposed interval analysis to first divide the program execution into discrete intervals by miss events, then determine the performance of each interval based on the corresponding miss events, and finally aggregate the performance of all intervals to obtain the overall performance. In contrast to prior studies that model the performance based on the issue rate, Eyerman *et al.* [102] further presented a simplified interval model that is built upon the dispatch width.

As in-order processors gain more attentions due to the energy concern, Breughe *et al.* [103] built an analytical model for scalar in-order processors by considering both miss events and hazards due to dependencies. After that, Breughe *et al.* [104] further built a mechanistic analytical model for superscalar in-order processors. The model also takes the profiled program characteristics (e.g., instruction mix, cache miss rates, and branch misprediction rates) as the input, while it is greatly enhanced with modeling functional unit contention and interinstruction dependences.

The above work requires profiling to obtain architecture-dependent characteristics such as cache misses, and the corresponding profiling cost cannot be neglected for a large design space. To reduce the profiling cost, Van den Steen *et al.* [105] constructed an analytical model based on architecture independent (while program dependent) profiles, including instruction mix and dependences, memory behavior, and branch behavior. Such profiles are sent to the analytical model, together with the architecture parameters such as pipeline depth, to obtain both the performance and power estimation.

Processor queueing model [106] is another example of analytical model. Although the queuing model also relies on processor parameters (e.g., memory latency) and program characteristics (e.g., loads per instruction), it mainly focuses on the interactions between the pipeline, buffers, and caches in the memory hierarchy. The queuing model is validated against cycle-accurate simulators, and it can be easily integrated into a multiprocessor system model.

C. Reducing Both Programs and Architectures

The aforementioned approaches manage to cut down the total number of simulation runs by reducing either the number of evaluated programs or the number of simulated architectures. To further reduce the number of simulation runs, Dubach *et al.* [107] and Khan *et al.* [108] independently proposed signature-based approaches. The key of these approaches is incorporating several simulated responses on a small number (e.g., 8 or 32) of typical architectures, named as signatures, for each program during the training process. Then, when encountering a new program, only a small number of simulation runs are required to obtain its signature. With the help of such signature, the responses of the new program can be predicted without additional simulation runs. Although the basic ideas of these two work are similar, Dubach *et al.* [107] used linear models to combine several models trained from different programs, while Khan *et al.* [108] directly treated the signatures as the inputs of the learning algorithm.

Fig. 5 compares the number of simulation runs of the signature-based approaches and traditional predictive modeling approaches. Conventionally, the total number of simulation runs is $m \times N$, where m is the number of simulated

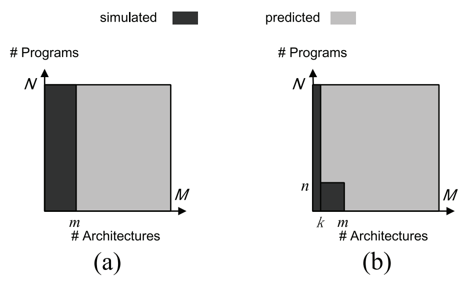


Fig. 5. Comparison of (a) traditional predictive modeling techniques and (b) signature-based approaches.

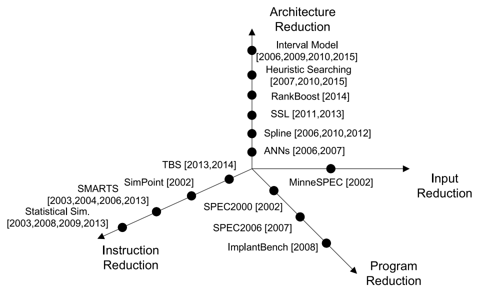


Fig. 6. Comparison of different fast simulation methodology via statistical techniques.

architectures and the N is the number of evaluated programs. In comparison, the total number of simulation runs of the signature-based approaches is $m \times n + (N - n) \times k$, where m is the number of simulated architecture, n is the number of trained programs, N is the number of evaluated programs, and k is the size of signature (e.g., 8). Thus, it can be observed that the total number of simulation runs could be significantly reduced, especially when more programs should be evaluated.

In addition to exploring the program and architecture co-design space, researchers also manage to explore the joint space consisting of not only architectural options but also various compiler and hardware circuit options. Dubach *et al.* [109] utilized predictive modeling (i.e., support vector machines) to explore the joint space of architecture and compiler options. Azizi *et al.* [110] proposed to use spline functions to explore the joint space of architecture and circuits. The joint space of program and processor architecture is also explored by spline functions in [84].

V. Summary and Comparison

Fig. 6 presents the above partial simulation approaches via statistical techniques from another perspective. It is notable that all those approaches can be classified in four orthogonal dimensions. In the first dimension, the approaches improve simulation efficiency via reducing the input size, where the most representative approach is MinneSPEC [40]. In the second dimension, the approaches speed-up simulation by reducing the number of simulated dynamic instructions of each program. Statistical simulation, sampling simulation, and statistical sampling are three main paradigms in this category. The approaches in the third dimension manage to reduce the number of programs for evaluation, where clustering analysis technique is most widely used to select a small but representative subset from the original benchmark suite. Finally, in the fourth dimension, the approaches reduce the number of simulated architectures via predictive modeling

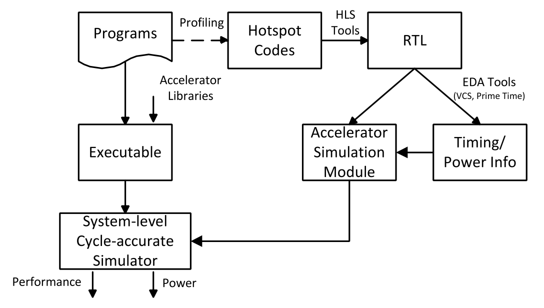


Fig. 7. Design and evaluation flow of accelerator-centric architecture.

techniques. To construct such predictive models, various statistical regression techniques, including linear regression, spline function, and machine learning techniques, have been extensively studied by researchers. Moreover, the number of simulated architectures can also be reduced by heuristic searching and analytical modeling.

It is possible to combine these afore-mentioned approaches from different dimensions to achieve a more efficient fast simulation methodology. For example, given a DSE task for N target programs, the total number of simulated instructions should be $M \times N \times P$, where M is the number of architectures in the entire design space and P is the average number of dynamic instructions of each program. To accelerate the architectural simulation, in the first step, architects can enforce benchmark subsetting techniques on all target programs, and only reserve $n(n < N)$ programs for evaluation. Then, statistical simulation or statistical sampling techniques can be used to reduce the number of simulated instructions by several orders of magnitude [i.e., the average number of instructions is only $p(p << P)$]. Finally, only a small proportion of all possible architectures [e.g., $m(m << M)$] need to simulate for constructing predictive models. With the help of such predictive models, it is no necessary to conduct simulations on remaining architectures. Therefore, the total number of simulated instructions can be reduced from $M \times N \times P$ to only $m \times n \times p$, which can improve the simulation efficiency by several orders of magnitude.

VI. Implications for Future Accelerator-Centric Architectures

As the transistor densities continue to scale exponentially, a chip cannot be fully powered at one time given limited chip-level power budget, which results in the dark silicon problem. To address this problem, customized and specialized hardware accelerators would be very promising and have been investigated by many researchers. Actually, heterogeneous chips containing application-specific accelerators are becoming increasingly common in mobile system, server, and desktop systems [111], [112]. Fig. 7 shows a typical design and evaluation flow of accelerator-centric architectures [113], [114]. The first step is profiling the target program to get its hotspot codes (e.g., the most time-consuming functions). Then, several HLS tools (e.g., AutoPilot [115]) are used to directly convert the C code to synthesizeable Verilog. After that, the Verilog designs of the accelerators are simulated by register transfer level (RTL) simulation tools to get their timing and power characteristics. With such timing and power information, cycle accurate simulation modules of the accelerators can be generated and plugged into the system-level cycle-accurate simulator such as Simics [19]. Once the system-level simulator is built, the executable binary of the target program, which is compiled with the accelerator libraries, is evaluated on such simulator to generate the overall performance and power estimation.

According to the design flow as shown in Fig. 7, there are several challenges to efficiently design accelerator-centric architectures. The first one is how to efficiently generate an accelerator given a target program. In addition to using tools, such as AutoPilot and Spiral [116], to automatically generate the Verilog designs of accelerators, many researchers also designed the application-specific accelerators manually, such as thin servers with smart pipes [117] for memcached and Q100 [118] for database applications. The second challenge is to determine which programs should be accelerated, since there always exists a tradeoff between generality and efficiency of processors. The third challenge is how to accurately and efficiently evaluate different design options of accelerators, so as to find optimal designs under specific performance/power/area constraints. Here, we discuss the implication of reviewed partial simulation approaches on addressing the later two challenges.

Although specialized architectures gain significant efficiency at the cost of generality, it is still expected that more applications can benefit from such architectures given limited area and power budget. This problem can be formulated as to find a representative subset of many widely used applications, which has been extensively investigated by the benchmark subsetting techniques. Inspired by the benchmark subsetting techniques, we may use several statistical techniques (e.g., PCA and clustering analysis) to guide the selection of target applications for hardware acceleration. A typical work that uses this methodology to design accelerators is the 10×10 project, which exploits workload analysis to drive the design of heterogeneous architecture containing customized accelerators [119], [120]. The project is built upon detailed analysis of program characteristics, such as operations, data types, and control flows. By conducting clustering analysis on such extracted characteristics from various benchmark suites, several clusters are carefully selected and supported by customized microengines.

Similar to the design of general-purpose processors, there also exists many tunable parameters for the design of accelerators. For example, during the design of DRAM-aware fast Fourier transform (FFT) accelerator, there are many different parameters such as FFT radix and streaming width [121]. Conventionally, RTL simulation is indispensable to evaluate different design options. However, the simulation costs are intractable due a large number of design options for evaluation. To address this issue, Shao *et al.* [122] proposed a pre RTL approach to efficiently evaluate the performance and power of accelerator designs. In addition to such high-level models for fast DSE, we also believe that several partial simulation approaches, such as predictive modeling, can also be deployed to further cut down the RTL simulation costs. As shown in Fig. 4, only a sampled number of accelerator configurations are analyzed by the RTL-based synthesis flow to generate corresponding performance and power estimation. Then, predictive models can be constructed with various statistical techniques. Finally, the performance/power of all other accelerator configurations can be directly predicted by such models without any costly simulation runs.

VII. Conclusion

In this paper, we review recent advances on partial simulation techniques. The basic idea of these techniques is to simulate a small subset of the representative instructions from the complete set of simulated instructions by using various statistical techniques, such as basic statistical concepts (sampling theory and non-parametric hierarchical performance testing [34]), statistical analysis techniques (PCA and clustering analysis), regression techniques (linear regression and spline function), and machine learning techniques (RBF, ANNs, and evolutionary algorithms). Technically, these techniques tradeoff accuracy for speed, and they can be categorized into four orthogonal dimensions, that is, input size reduction, dynamic instruction reduction, program reduction, and architecture reduction. Also, these approaches can be combined together to obtain a more efficient simulation methodology. We believe that partial simulation methodology can also play an important role during the design of future accelerator-centric architectures.

Acknowledgment

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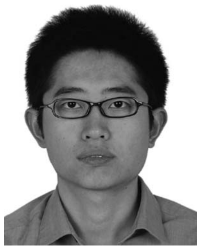

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