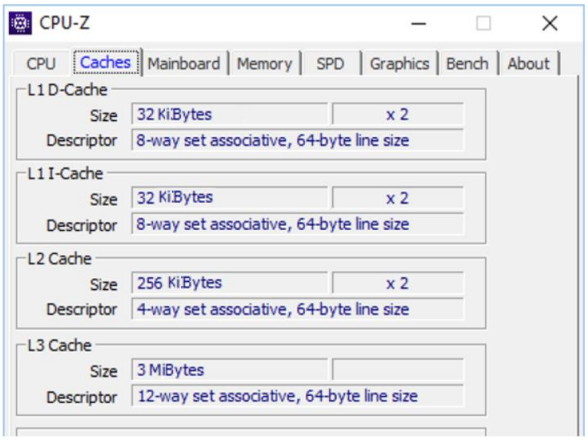
Question 1 ✓ *Saved*

Obtain the number of cache lines and cache sets for the **L3** Cache given below?

1 KiB = 2^{10}
1 MiB = 2^{20}
1 GiB = 2^{30}



# of lines (e.g 2096) = 49152

# of sets (e.g 2096) = 4096

Question 2 ✓ *Saved*

Given the following information:

Memory	4 GiB
L3 cache	8 MiB
Cache line size	128 B
Method	Direct mapping
Addressing mode	Byte addressable

Answer the following question:

1) How many bits are used for addressing each byte of memory? **e.g. 64** 32

2) How many bits are used for addressing each byte of the L3 cache? **e.g. 64** 23

3) How many bits are required to address each byte within a cache line? **e.g. 64** 7

4) How many cache lines are present in the memory? **e.g. 2^12** 2^25

5) How many cache lines are present in the L3 cache? **e.g. 2^12** 2^16

For the memory Address 0xA0B12FC0 obtain:

Tag in hex **e.g. 0xAB**

0xA0B

Memory Index (MI) in hex **e.g. 0x0231**

0127E

Cache Index (CI) in hex **e.g. 0xEF12**

0xC0

Question 3 ✓ *Saved*

Assuming **A = 12** and **B = 15**, and considering the control signals, given in the following table, obtain the output (function) of ALU for each case.

ALU (list of operations)							
F0	F1	ENA	ENB	INVA	INC	Output (Function)	
1	1	1	1	1	1		O1
1	1	1	0	1	1		O2
1	1	0	0	1	0		O3
1	1	0	1	1	0		O4

O1 e.g. 45 or -45 = 4

O2 e.g. 45 or -45 = -11

O3 e.g. 45 or -45 = 0

O4 e.g. 45 or -45 = 15

Question 4 ✓ *Saved*

What numeric (octal) value corresponds to the permission string rwxr-x--x e.g. 341 ?

751

Question 5 ✓ *Saved*

Which command changes the permission of the file data.txt so that only the owner can read and write, while everyone else has no access?

- ○ chmod 777 data.txt
- ○ chmod 400 data.txt
- ◉ chmod 600 data.txt
- ○ chmod 644 data.txt

Question 6 ✓ *Saved*

A developer is running a user program that needs to access a hardware device (for example, writing to an I/O port). When the program executes an instruction to access the device, the CPU immediately triggers a protection fault.

6 What mechanism should the operating system provide to safely allow this operation?

3 Which privilege ring is the user program running in when this fault occurs?

1 Which ring is allowed to directly access the hardware?

1. 0
2. 1
3. 2
4. 3
5. Allow direct hardware access from user mode
6. Use a system call to request the kernel to perform the operation
7. Run the program temporarily in Ring 0
8. Disable CPU protection checks

Question 7 ✓ *Saved*

The EFLAGS register currently contains the hexadecimal value:
0x00000246
Based on this value, which of the following flags are set (1)?

- ○ Sign Flag (SF) and Overflow Flag (OF)
- ○ Carry Flag (CF) and Zero Flag (ZF)
- ○ Parity Flag (PF) and Interrupt Enable Flag (IF)
- ● Parity Flag (PF), Zero Flag (ZF), and Interrupt Enable Flag (IF)

Question 8 ✓ *Saved*

Which of the following instructions should be allowed only in kernel mode?

2 ⌄	Read the time-of-day clock.
1 ⌄	Change the memory map.
1 ⌄	Set the time-of-day clock.
1 ⌄	Disable all interrupts.

1. Kernel Mode
2. User Mode

Question 9 ✓ *Saved*

A CPU has a 3-stage pipeline with stage delays of 3 ns, 4 ns, and 7 ns. What is the pipeline clock cycle time if the pipeline operates synchronously?

- ○ 4 ns
- ○ 3 ns
- ● 7 ns
- ○ 14 ns

Question 10 ✓ *Saved*

Correct Match-the-Following (Cache Memory)

4	Direct mapping
1	Cache hit
2	LRU
3	Cache miss

1. Data found in cache memory
2. Cache block replacement policy
3. Data not found in cache memory
4. Each memory block maps to exactly one cache line