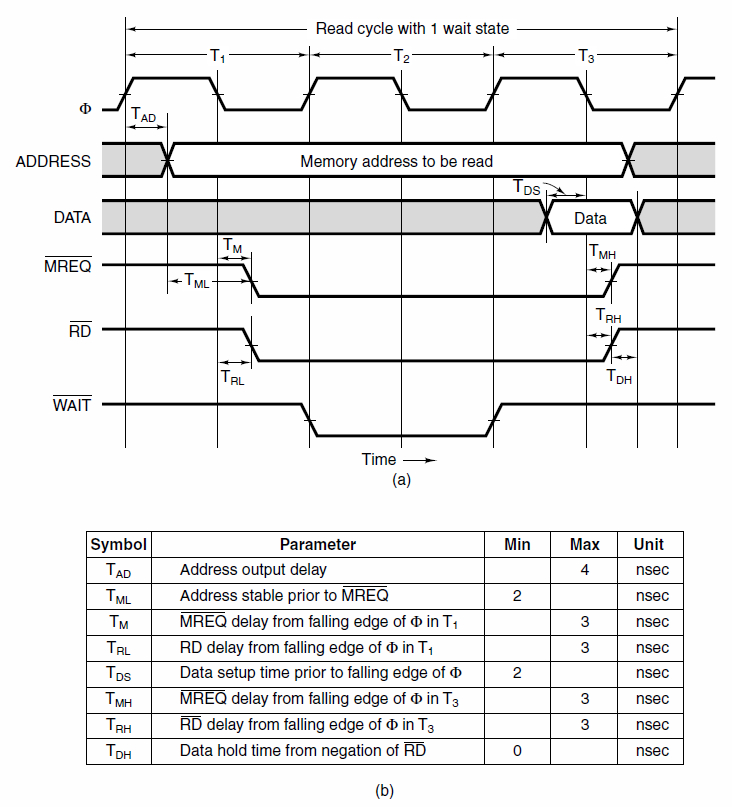
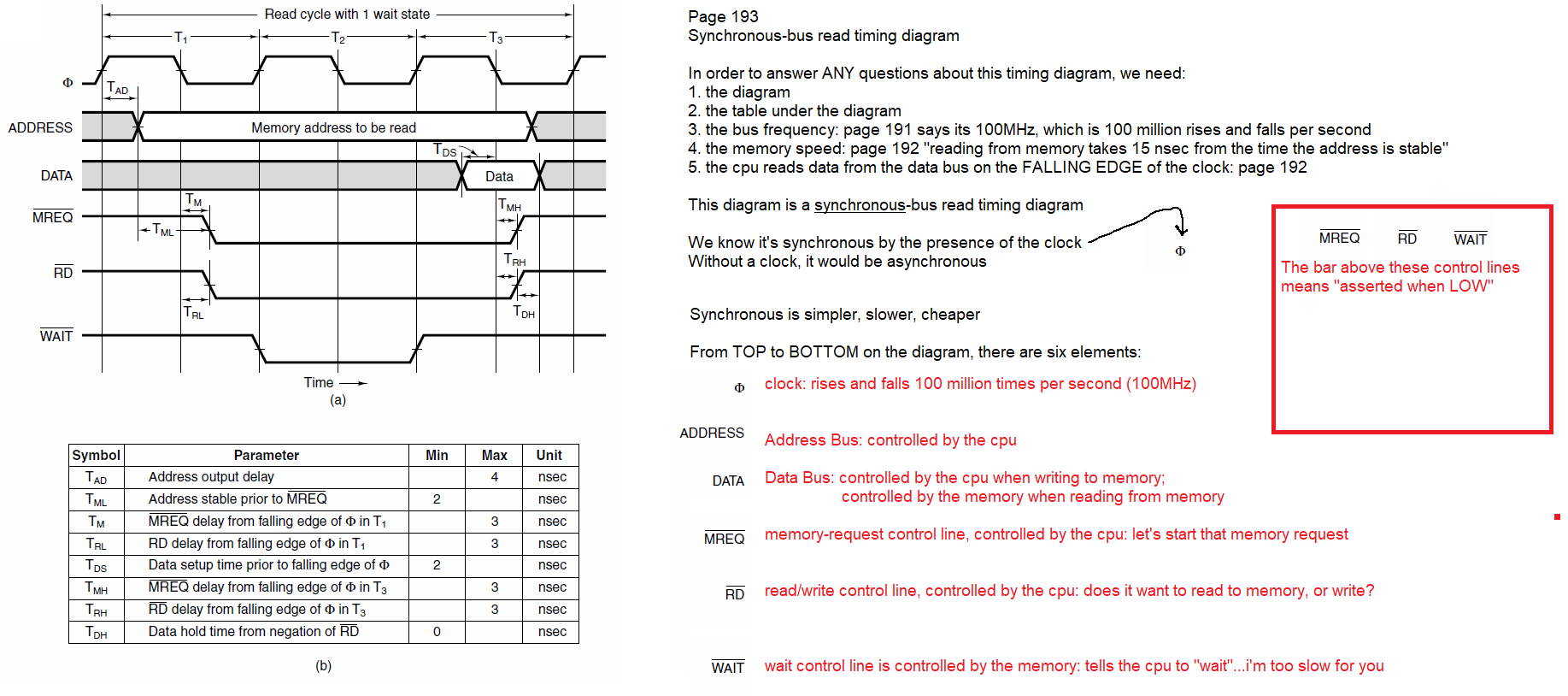
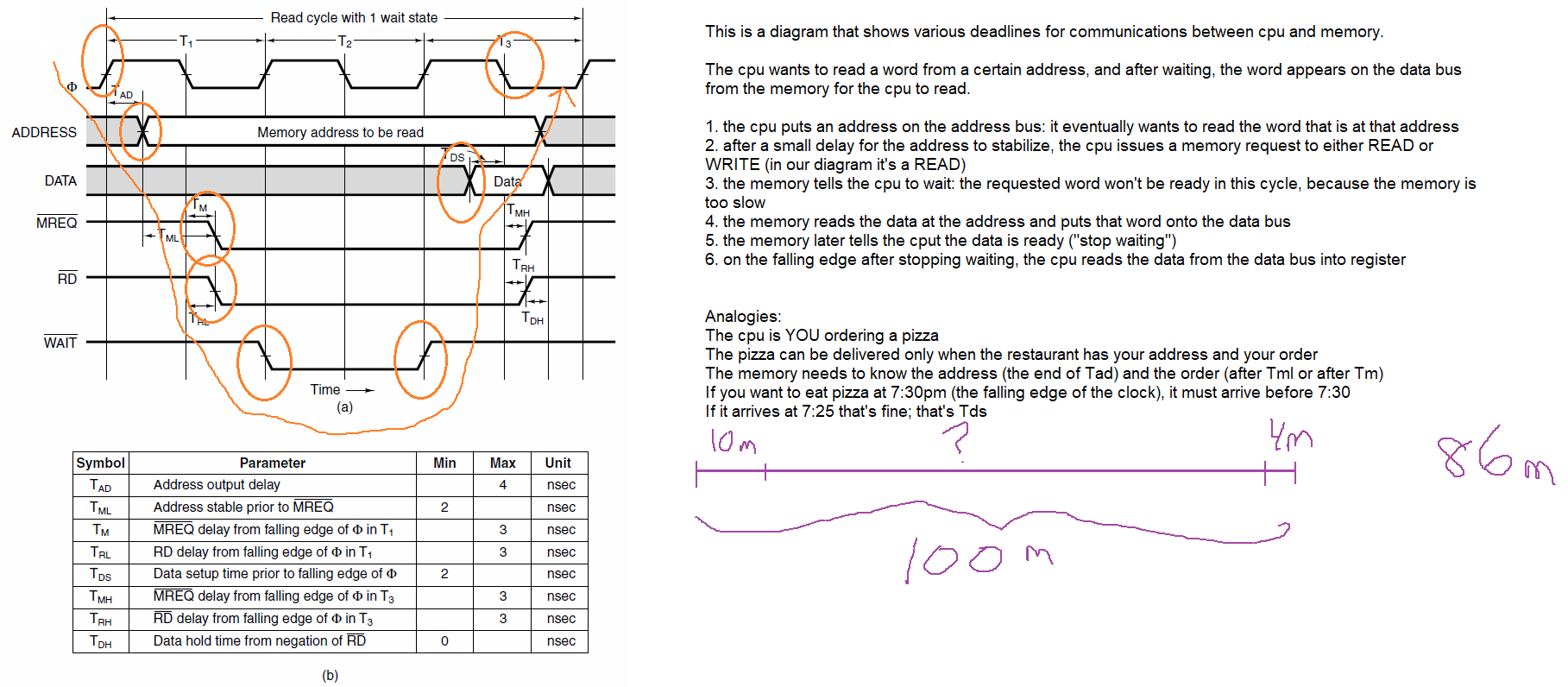
Lesson 7

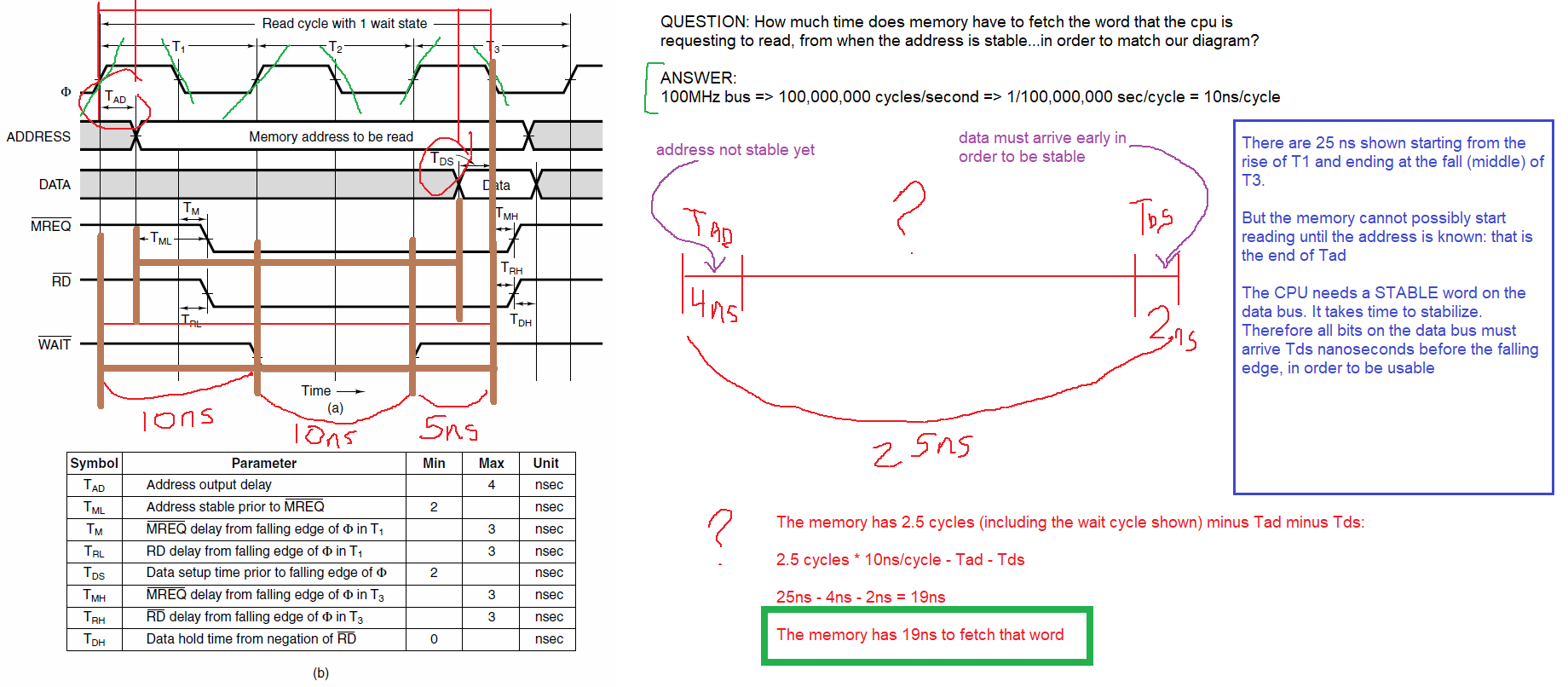
Today is the first lesson after the midterm, so it’s the first lesson that is on the final exam.



Homework: using your own analogies and your own words, describe how an Asynchronous bus read timing diagram works (page 195 textbook). Homework answer should be about 1 page including pictures



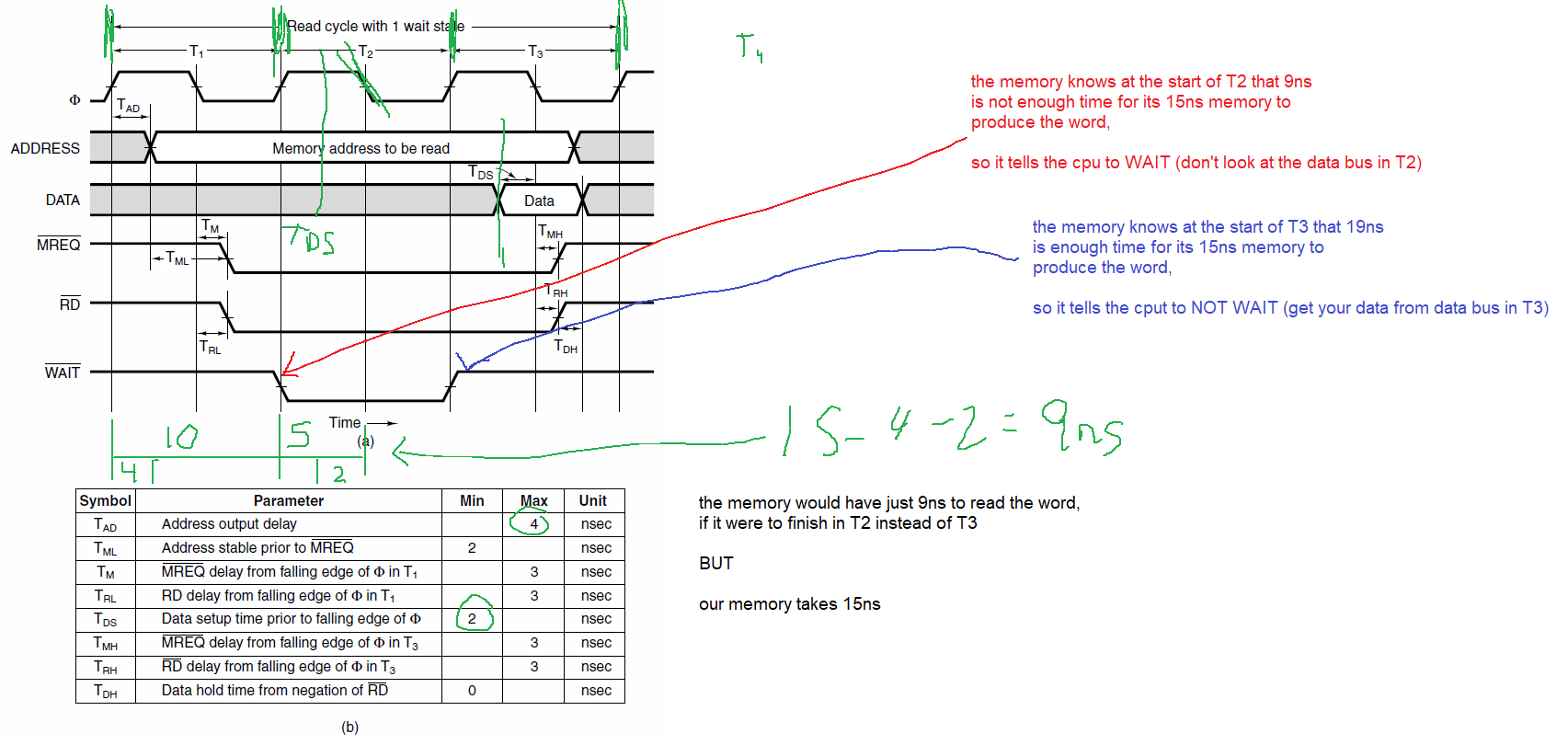




From page 192: “In our example, we will further assume that reading from memory takes 15

nsec from the time the address is stable”. We have 19ns! The memory can do it in 15ns. This is fine. It would be a problem if we had less than 15ns available. But, we have 19ns. We have 4ns “spare time”.

If we wanted all of this reading finished at the falling edge of T2 instead of the falling edge of T3, we would have one fewer clock cycle. We would therefore have only 9ns instead of 19ns

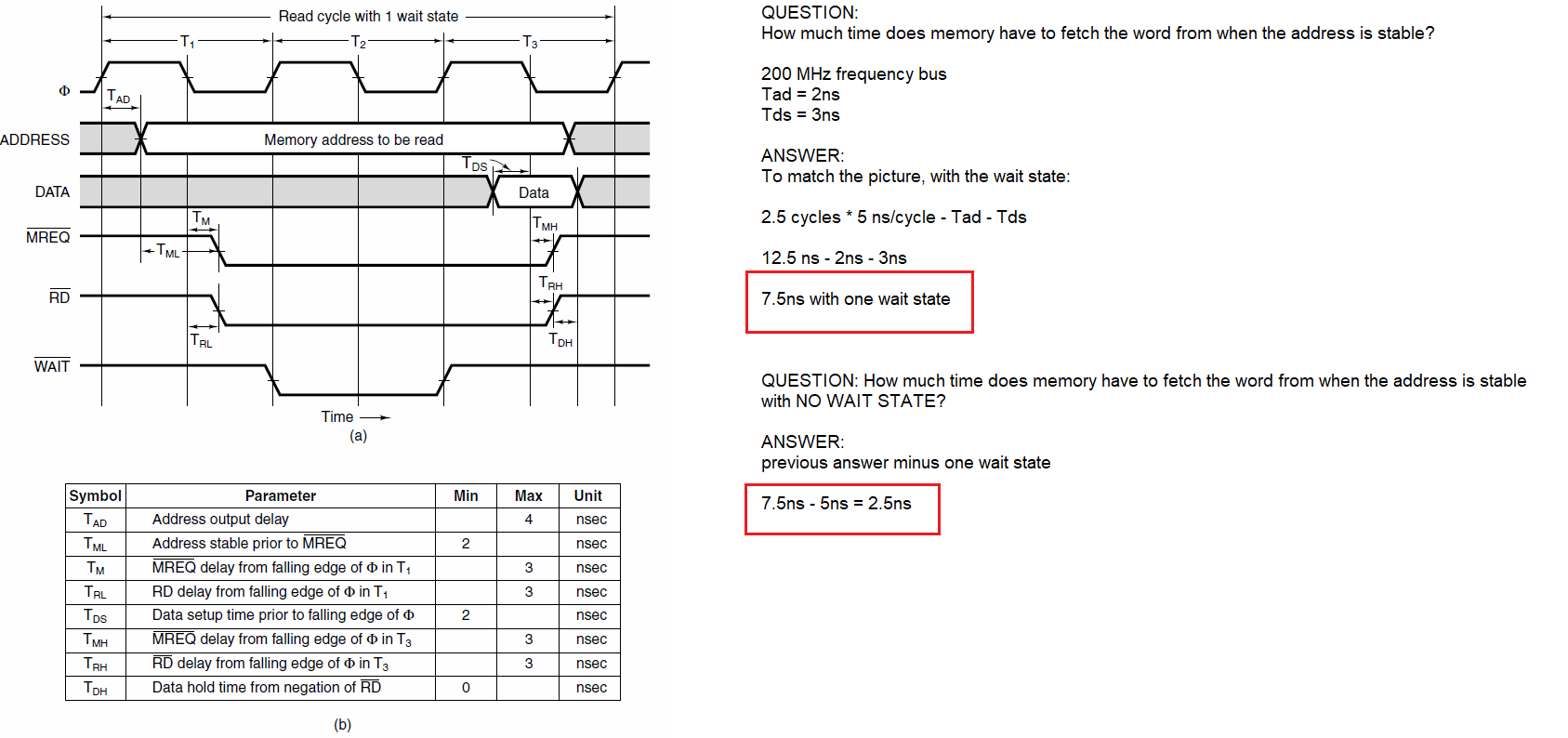


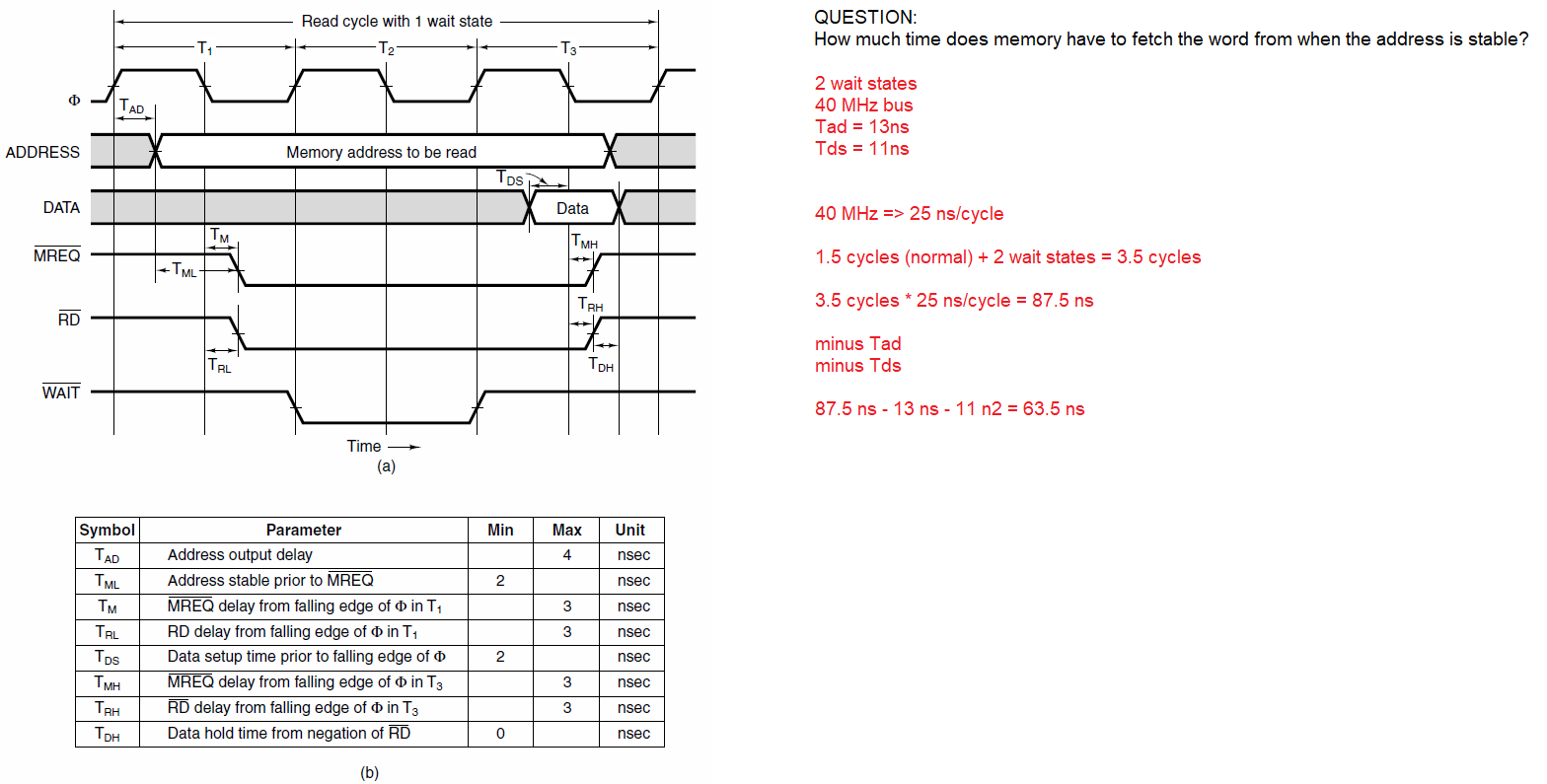
QUESTION: what if we wanted to read the data in T4 instead? How much time would the memory have to get its word? ANSWER: 29ns (just add another 10ns cycle to the 19ns answer above)

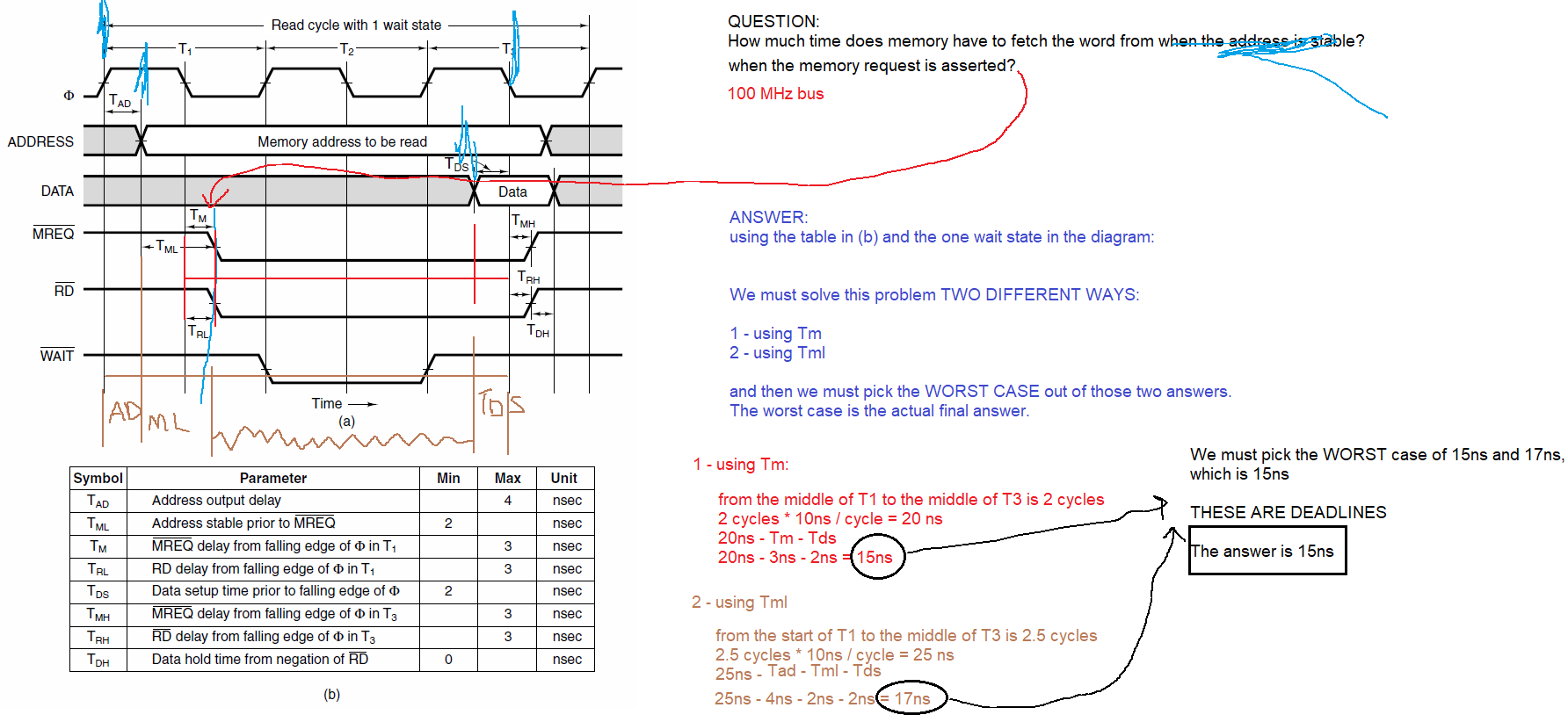
Fill in this table:

|  |  |
| --- | --- |
| **Frequency (Hz)** | **Period (sec/cycle)** |
| 100MHz | 10 ns |
| 50MHz | 20 ns |
| 2Hz (2 cycles per second) | 500 ms |
| 40kHz | 25 usec = 25 microseconds |
| 25MHz | 40 ns |
| 125MHz | 8 ns |
| 30 kHz | 33.3333333 microseconds |
| 50 Hz | 20 msec |
| 12.5 MHz | 80 nanoseconds |

Practice: <https://www.sensorsone.com/frequency-to-period-calculator/>







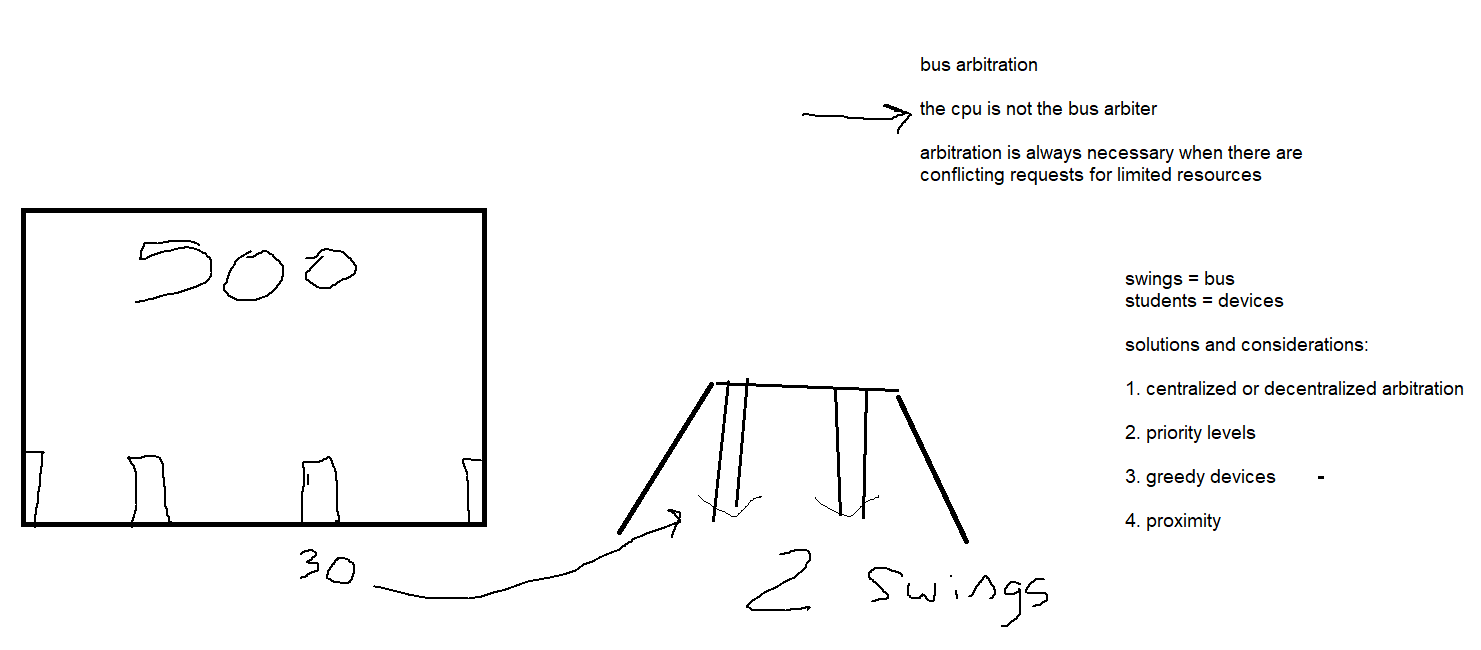
QUESTION: How much time does memory have to fetch a word from when the memory request is asserted? 50MHz bus. Tad is 6ns, Tds is 5ns, Tm is 4ns, Tml is 3ns. Two wait states.

ANSWER: 50 MHz => 20 ns/cycle

Using Tm: 1 cycle + 2 waits = 3 cycles \* 20ns/cycle = 60ns – Tm – Tds = 60-4-5 = 51 ns

Using Tml: 1.5 cycles + 2 waits = 3.5 cycles \* 20ns/cycle = 70ns – Tad – Tml – Tds = 70-6-3-5 = 56ns

The answer is the worst case, which is 51ns



100 MHz frequency = 100 000 000 cycles/second

period = 1/frequency

period = 1/100000000 = 1/100000000th of a second per cycle = 10ns / cycle

100MHz frequency --> 10ns/cycle

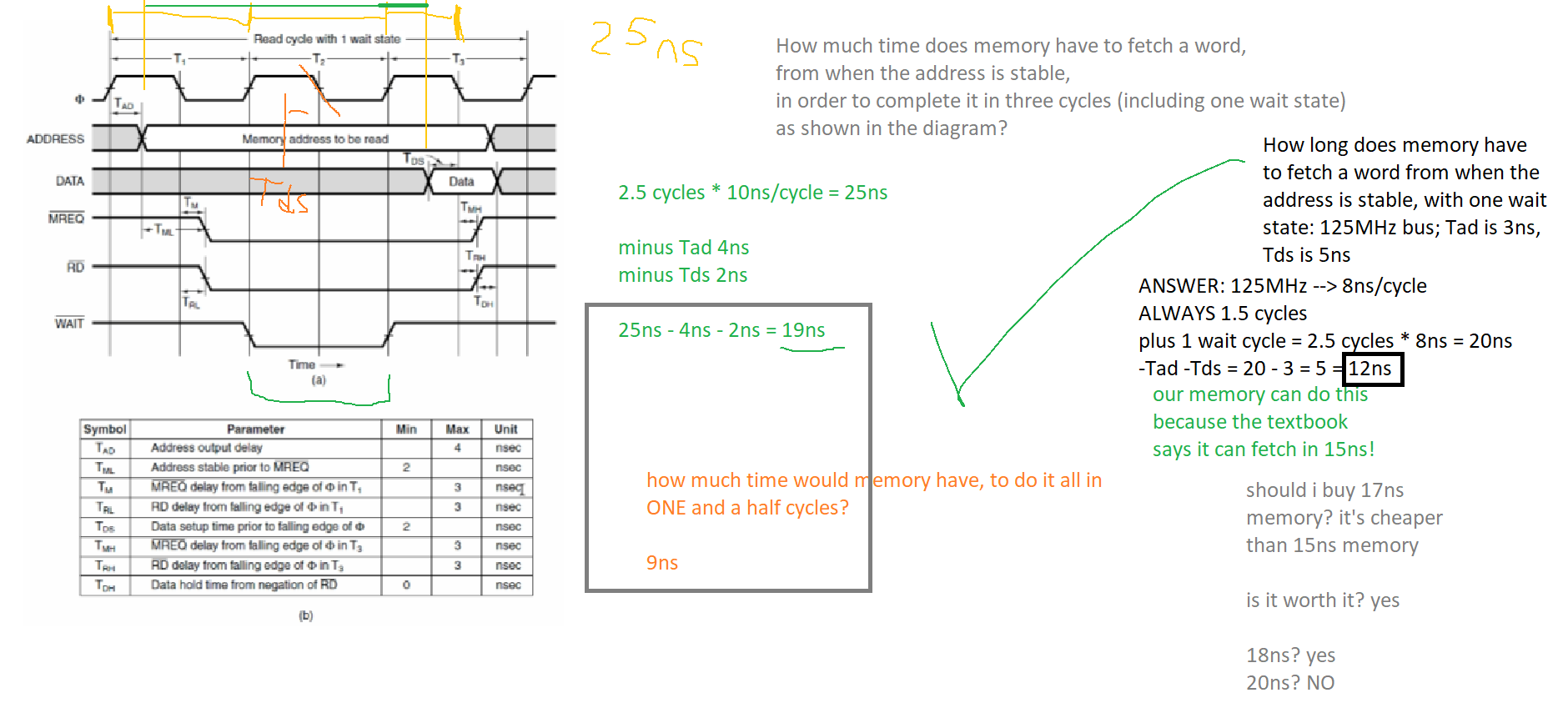
125MHz frequency --> 8ns/cycle

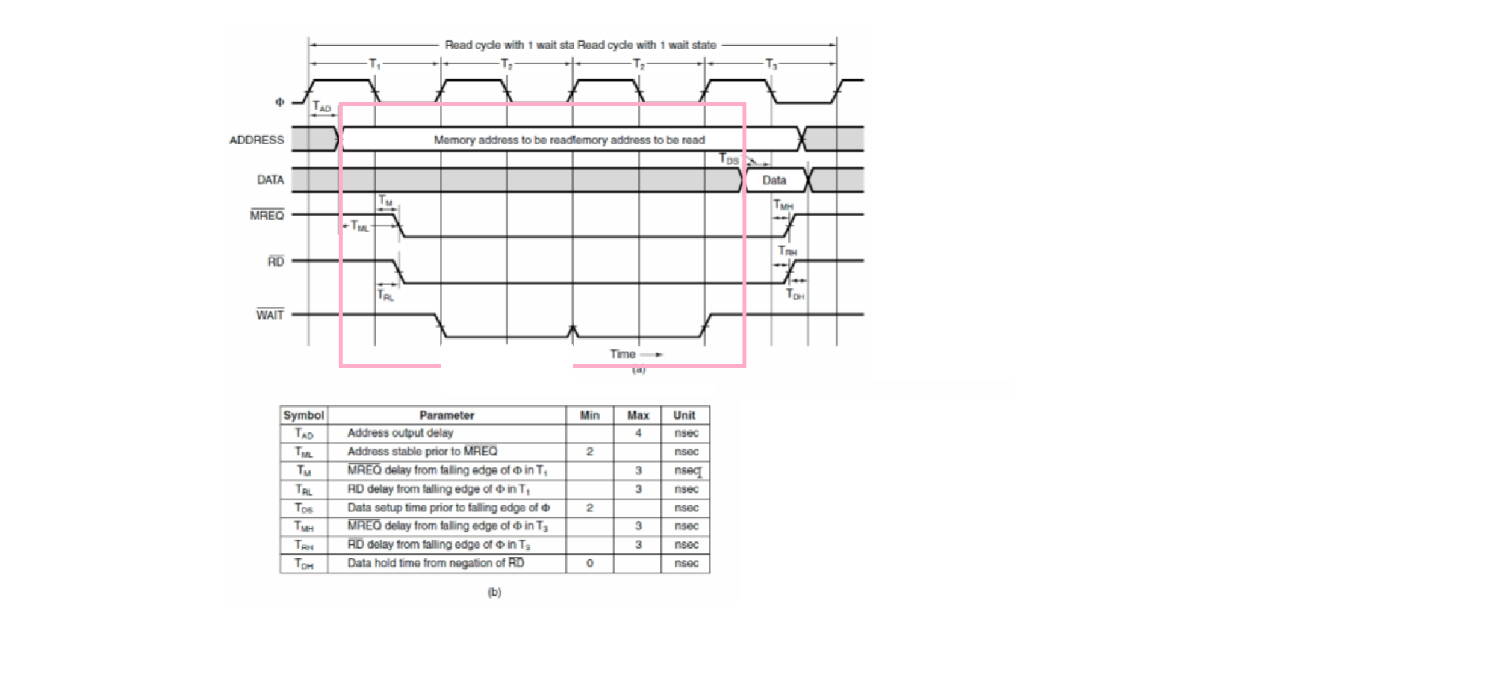
200MHz frequency --> 5ns/cycle

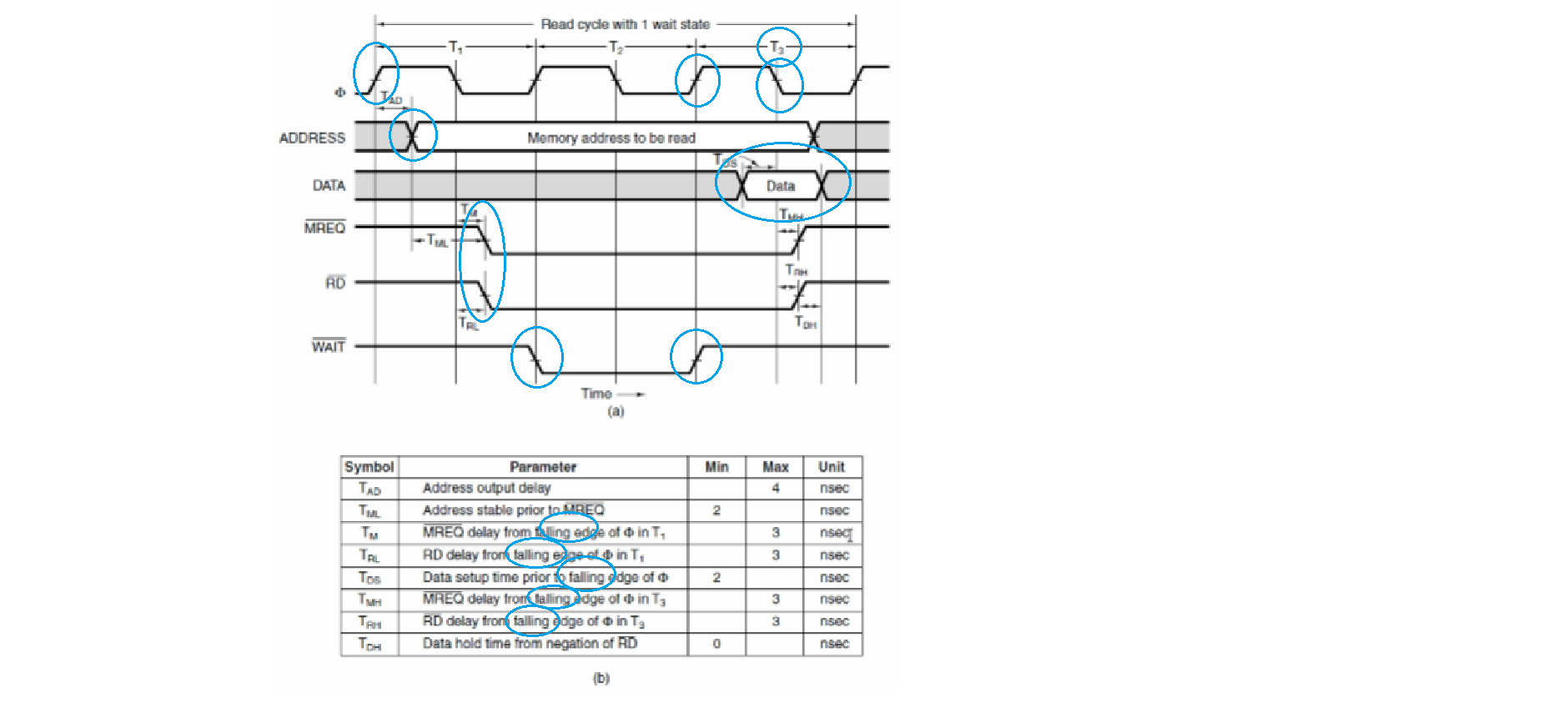
250MHz --> 4ns/cycle

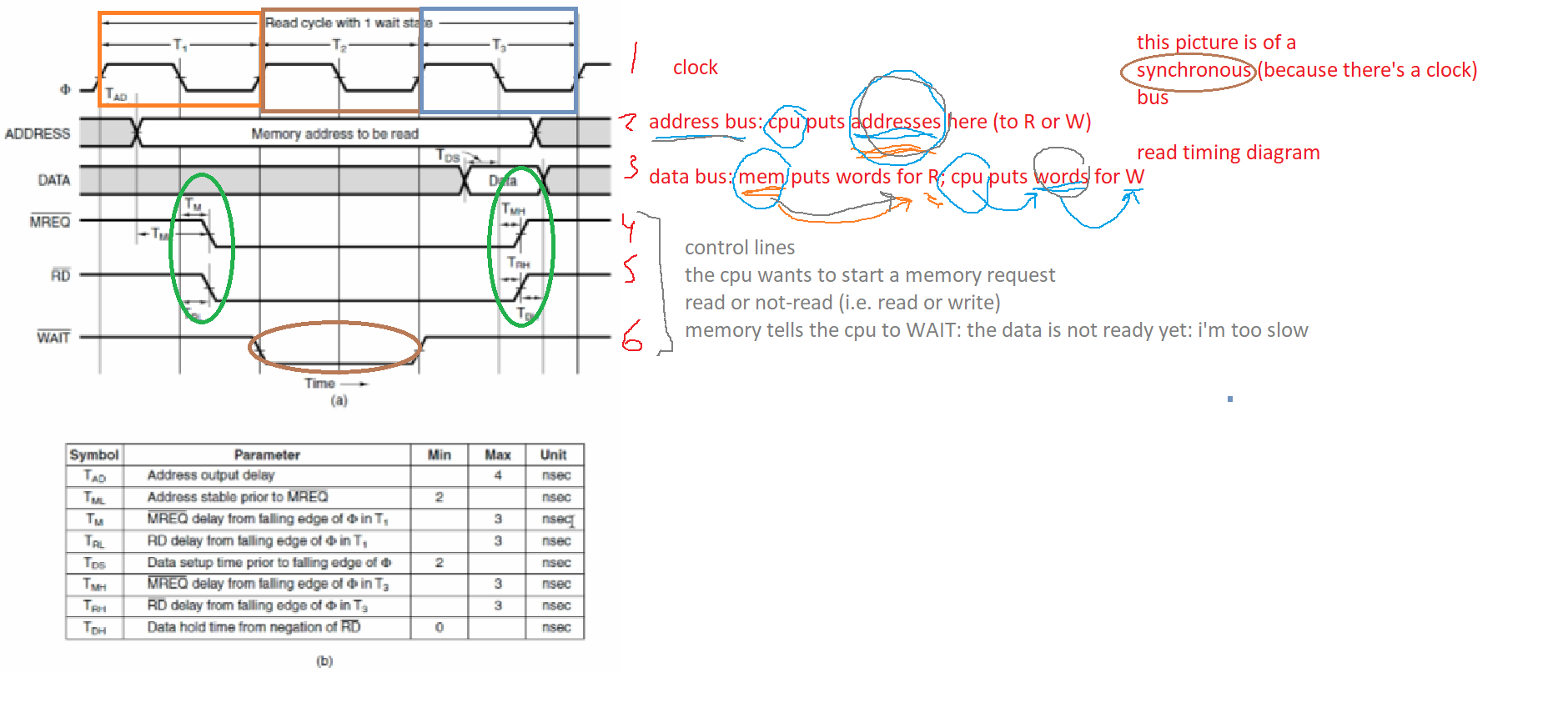
40MHz --> 25ns/cycle

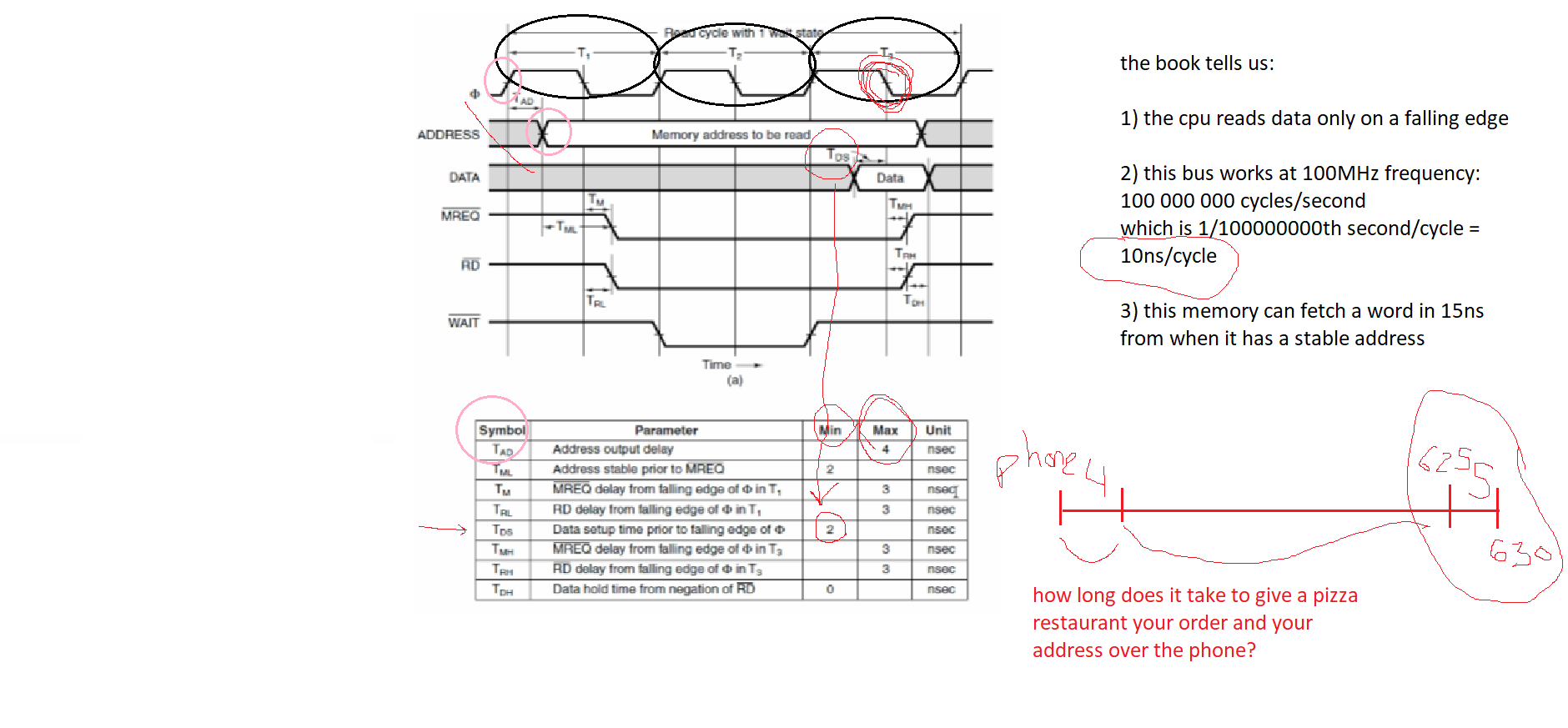
50MHz --> 20ns/cycle

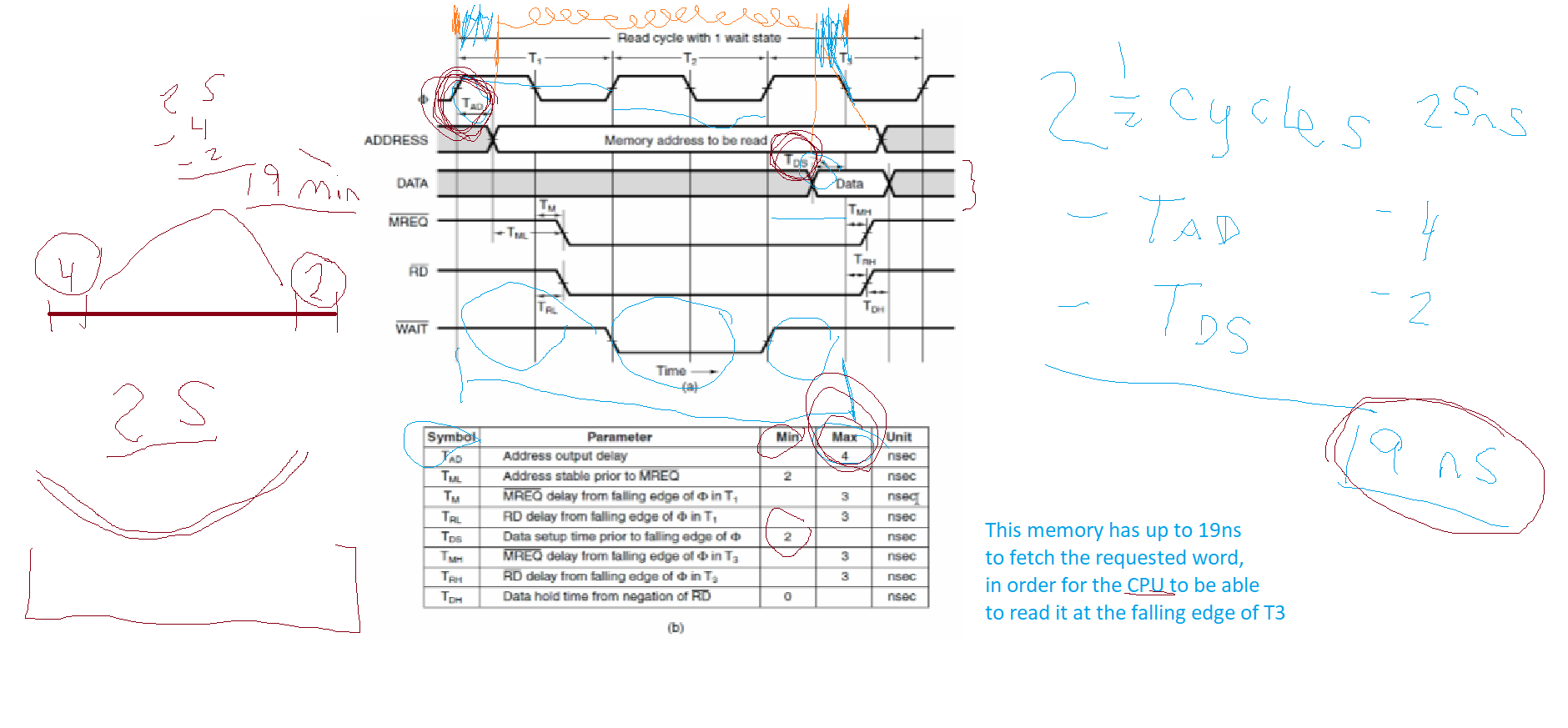


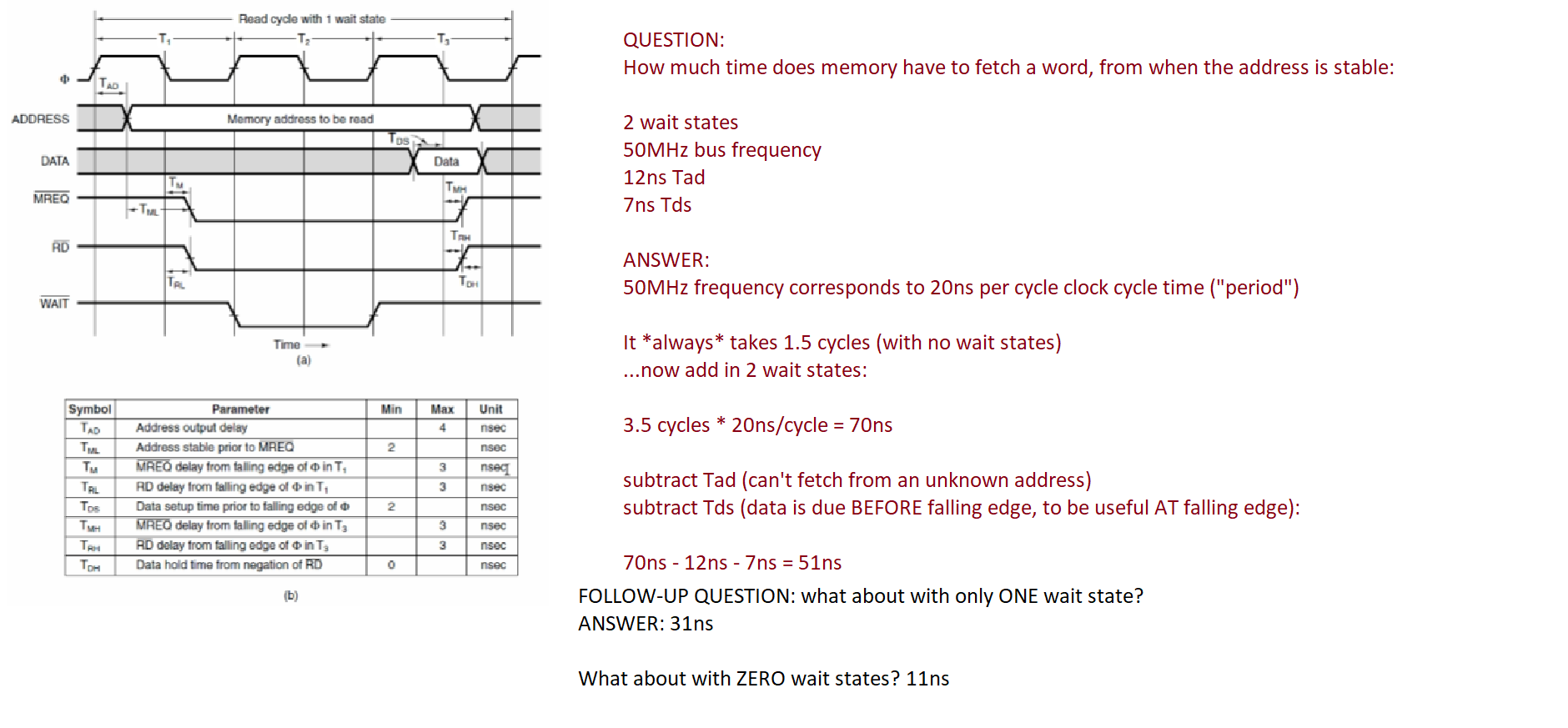


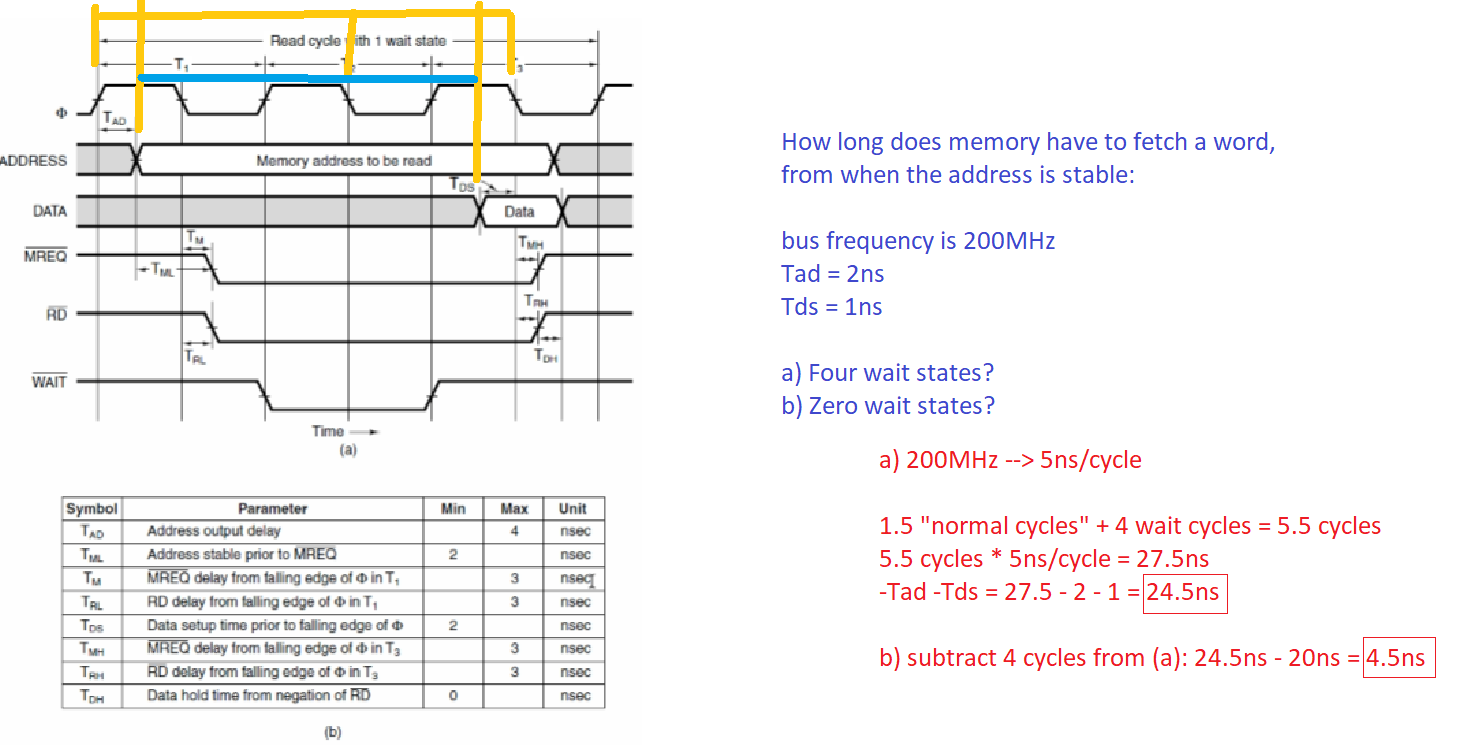


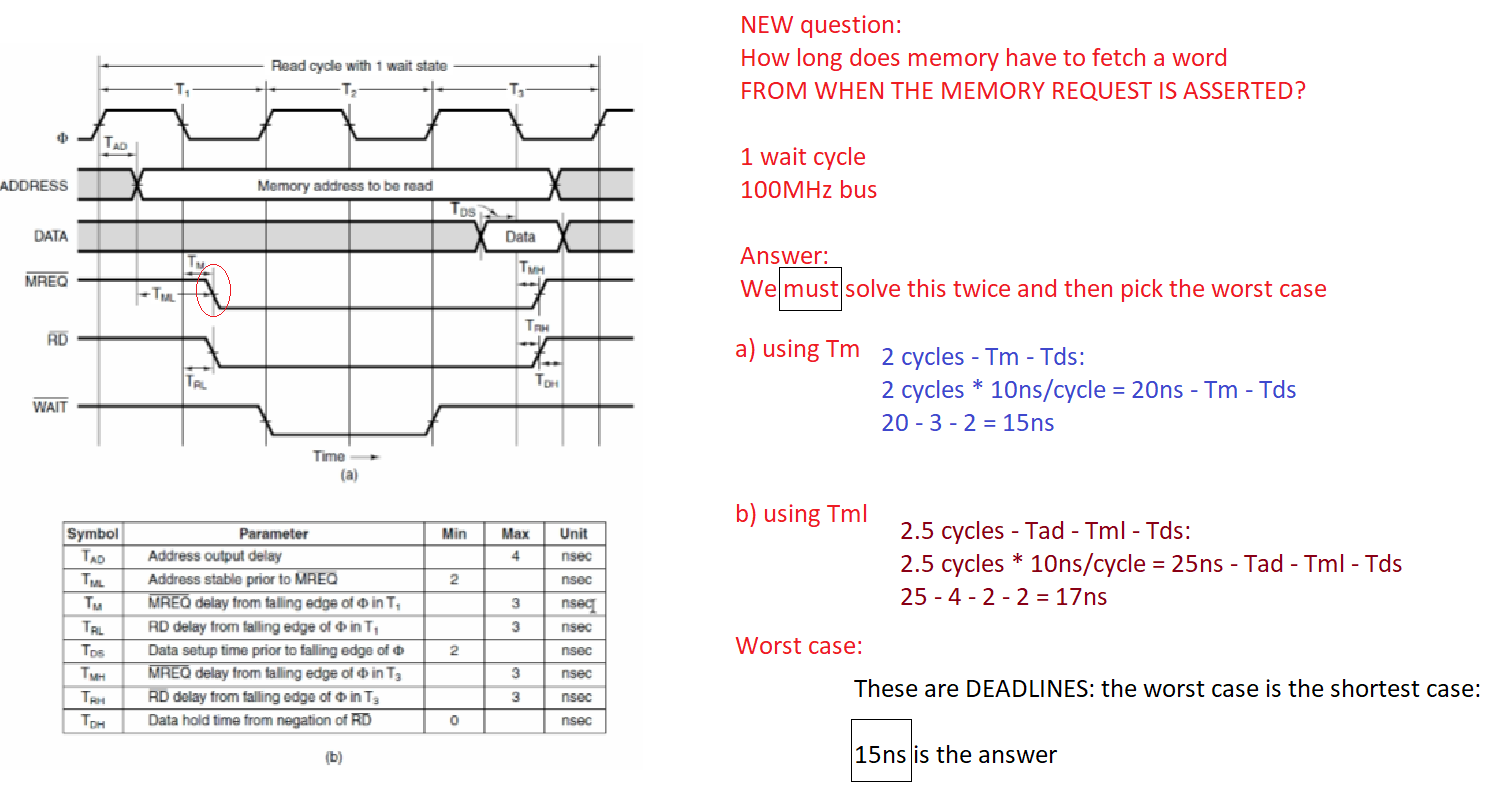












NEW QUESTION:

How long does memory have to fetch a word from:

1. When the memory address is stable
2. When the memory request is asserted

40ns bus period; Tad = 2 ns; Tm = 4ns; Tml = 6ns; Tds = 7ns. Zero wait states

ANSWER:

1. 1.5 cycles \* 40ns/cycle – Tad – Tds = 60ns – 2ns – 7ns = 51ns
2. Solve twice:

* Using Tm: 1 cycle \* 40ns/cycle – Tm – Tds = 40ns – 4ns – 7ns = 29ns
* Using Tml: 1.5 cycles \* 40ns/cycle – Tad – Tml – Tds = 60ns – 2ns – 6ns – 7ns = 45ns

Pick the lower of these times, which is the worst case: 29ns