64-Tap 16-bit Dual-Clock Fixed-to-Floating-Point Finite Impulse Response Filter Design

CSEE W4823 Fall 2024 Project

Group 9
Yuan Jiang (yj2848)
Hongxin Xu (hx2389)

❑ Architecture - FIR core Testbench

- **Inputs:**
  - Provides clk1 (10 kHz) and clk2 (640 kHz) clock signals.
  - Generates input stimulus din (16-bit FX) and preloads coefficients (16-bit FX) into memory from Matlab .txt files.

- **Top-Level FIR Core Modules:**
  - **FIFO**: Stores input data at clk1 and bridges asynchronous clock domains with clk2.
  - **CMEM**: Pre-loaded 64 coefficients.
  - **IMEM_reg**: Holds the 64 most recent input samples for convolution.
  - **ALU**: Performs MAC and converts FX16 to FP16.
  - **FSM**: Controls the states: IDLE, LOAD_COEF, PROCESS, and DONE.

- **Outputs:**
  - The filtered output dout (FP16) is generated and validated using valid_out signal.
  - Compares outputs with precomputed values (.txt file).
  - Flags mismatches and tracks error count / accuracy.

❑ Metrics of the FIR Filter

Metrics	Results
Throughput	10 kS/s
Maximum Clock Frequency	34.03 MHz
Power Consumption	1.868×10^{-5} W
Energy Efficiency	0.549 pJ/S
Area	86547.7 mm^2
Accuracy	Worst case: 95.30189 % | Average: 99.92025 %

Methods source: Lecture 07, "Advanced Logic Design," Fall 2024 CSEE W4823, by Prof. Mingoo Seok, pp.9.