CSEE 4824 Final Project

3-Way Superscalar R10K Out-of-Order Processor

Group #6, Columbia University

Yuan Jiang (yj2848) Yuxi Zhang (yz4935) Junfeng Zou (jz3850)
Lingxi Zhang (lz2991) Zhelin Su (zs2709) Hongrui Huang (hh3084)

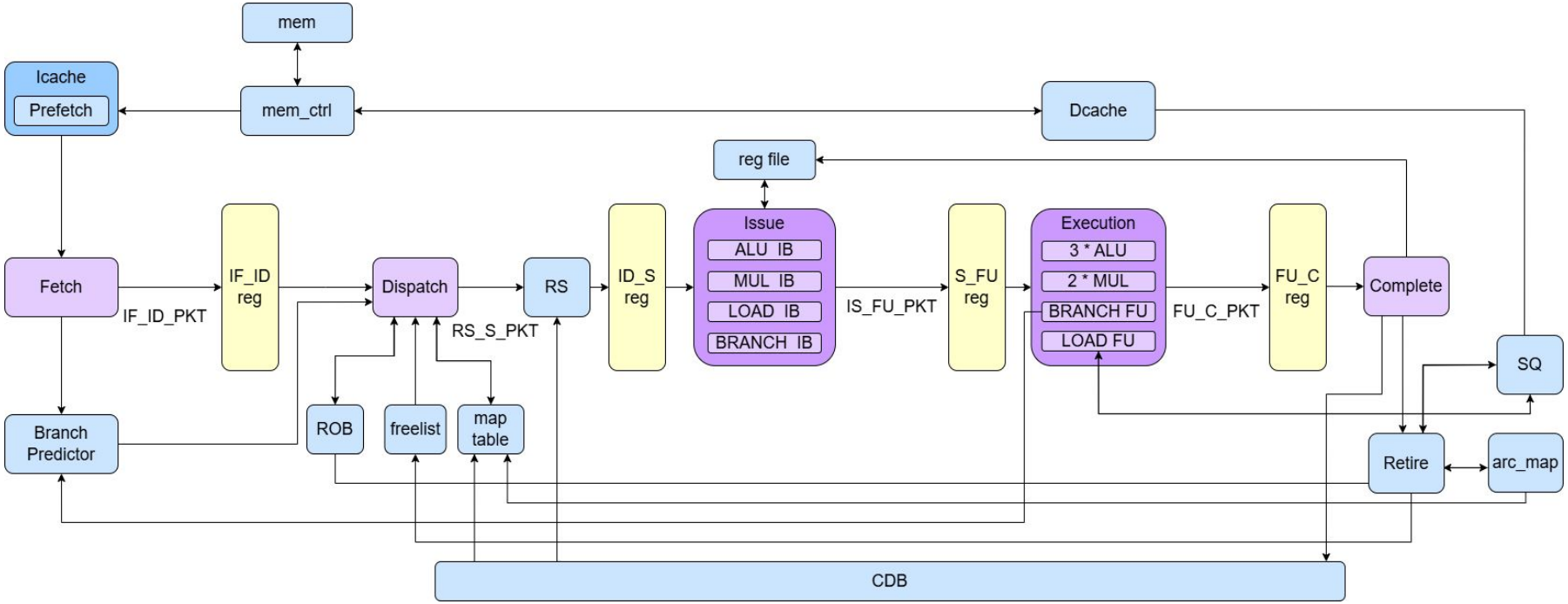
Features

- **Advanced feature**
  3-way superscalar execution
  Advanced Tournament Branch Predictor

- **Simple features**
  2-way set-associative non-blocking Data cache (write-back, write-allocate) with MSHRs
  Non-blocking Instruction cache with prefetching (write-back, write-allocate)
  2-bit bimodal Predictor
  Store queue with store to load forwarding and in order store retirement

- **Basic features**
  4 issue queues for each type of function unit (ALU MUL LOAD BRANCH)

Overall Architecture



Fetch stage

- Non Blocking I cache with prefetching
- Branch Prediction

Non-blocking I-Cache with prefetching

Non-blocking I-Cache

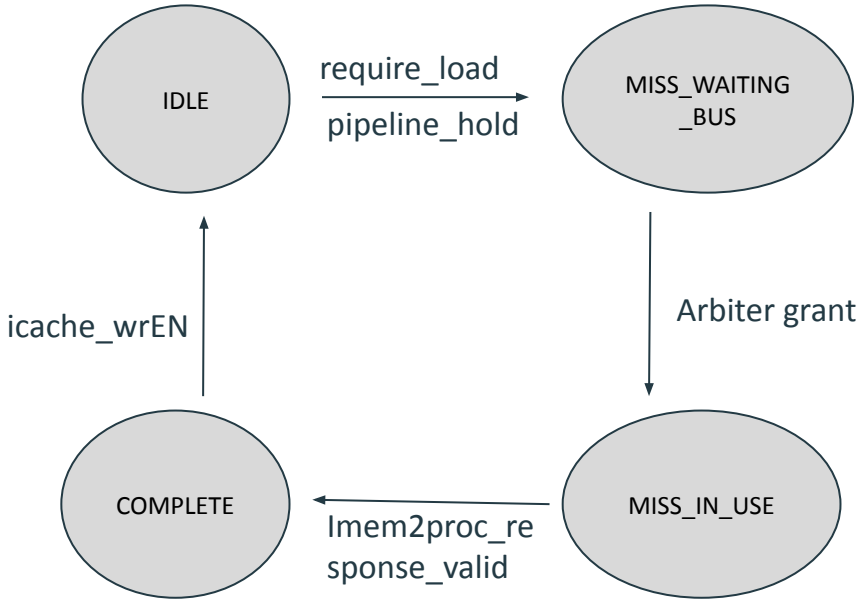
- Provides 3 parallel fetch ports with independent index lookups

MSHR (Depth = 8)

- Uses an 8-entry MSHR to track up to 8 misses to exploit memory-level parallelism

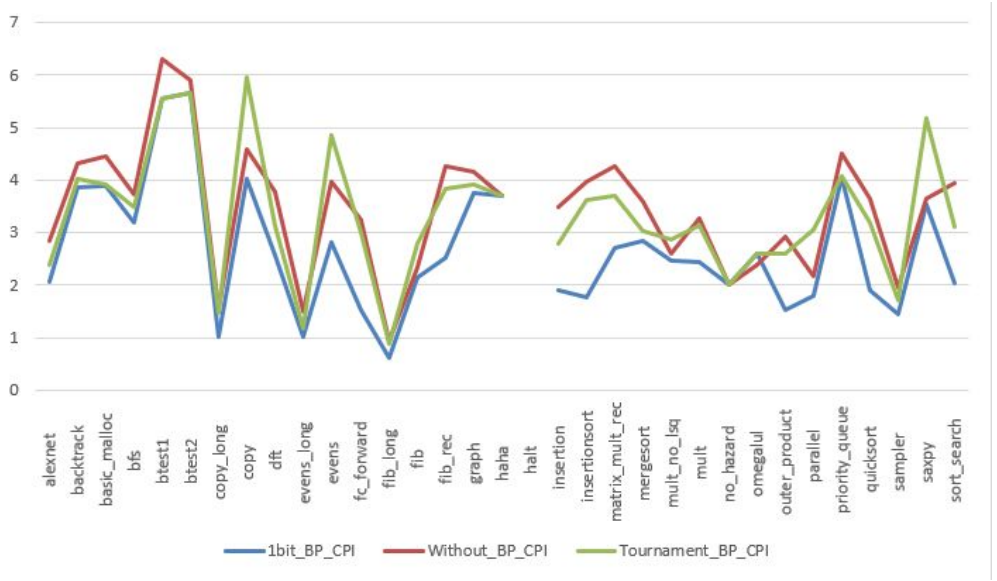
Bus Arbitration

- Actual fetches always win arbitration over speculative prefetches.



Branch prediction

- Tournament (submitted): Local bimodal + Gshare + 2-bit Chooser
- Limited improvement or even worse than simple predictor
- multiple prediction tables and the associated chooser logic may introduce latency and complexity



Dispatch stage

- Allocate instructions
- Stall to dispatch according to structural hazard

Dispatch stage

Allocate instructions:

Freelist --> free pr

ROB <-- dispatch entry; update tail

RS <-- dispatch entry; update tail

Map table <-- maptable_new_ar; maptable_new_pr

Stall dispatch according to structural hazard:

assign dis_stall = rs_stall | rob_stall | ~free_pr_valid | sq_stall;

Issue stage

- Routes instructions from RS to FUs
- Instantiation of 4 types of issue queues: ALU, Mult, Load, Branch
- Each queue reorders valid packets, prevents overflows, and issues instruction only when FU is ready

Execution stage

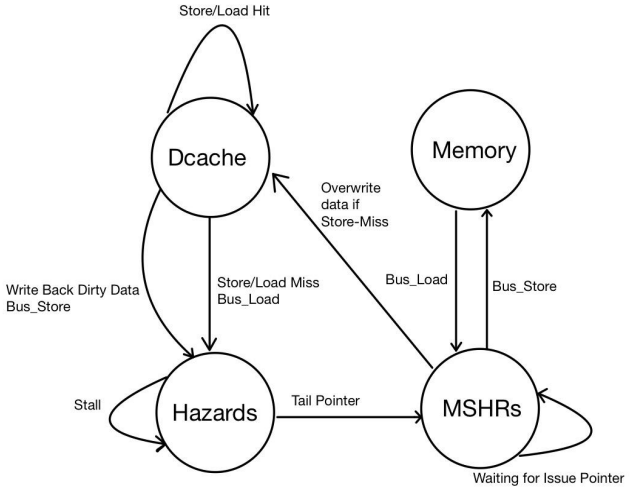
- Instantiation of 8 FUs:
  - 3 ALUs for non-mult/non-load instructions
  - 2 FP Mults (4-stage pipelined)
  - 2 Load units (with store-to-load forwarding from SQ)
  - 1 Branch unit (with update direction and pc to BP)

Store queues

- Holds store instructions until they are ready to be retired
- Keeps track of valid entries using head and tail pointers, dispatches new stores without stalling, and provides allocation indices for new entries
- Age logic: Identify older stores to support store-to-load forwarding in-order store

Non-blocking 2-way 16 sets Dcache

- Structure:
  - Dcache: 2-way set-associative, 16 sets (256B total)
  - MSHRs: 8 entries, circular FIFO (head/issue/tail pointers)
- How:
  - Store/Load Miss → Create BUS LOAD with dirty = 1
  - Dirty Eviction → Create BUS STORE
- Data Hazards:
  - Load-Load: Merge if same block in-flight
  - Load-Store: Detect match, force load to miss
  - Store-miss: Overwrite data from memory to Dcache
- Stall SQ if MSHR nearly full



Complete stage

- Uses priority selectors to determine up to 3 FU complete order
- Notifies the ROB and CDB with complete results
- Issues structural hazard when number of empty entries not enough

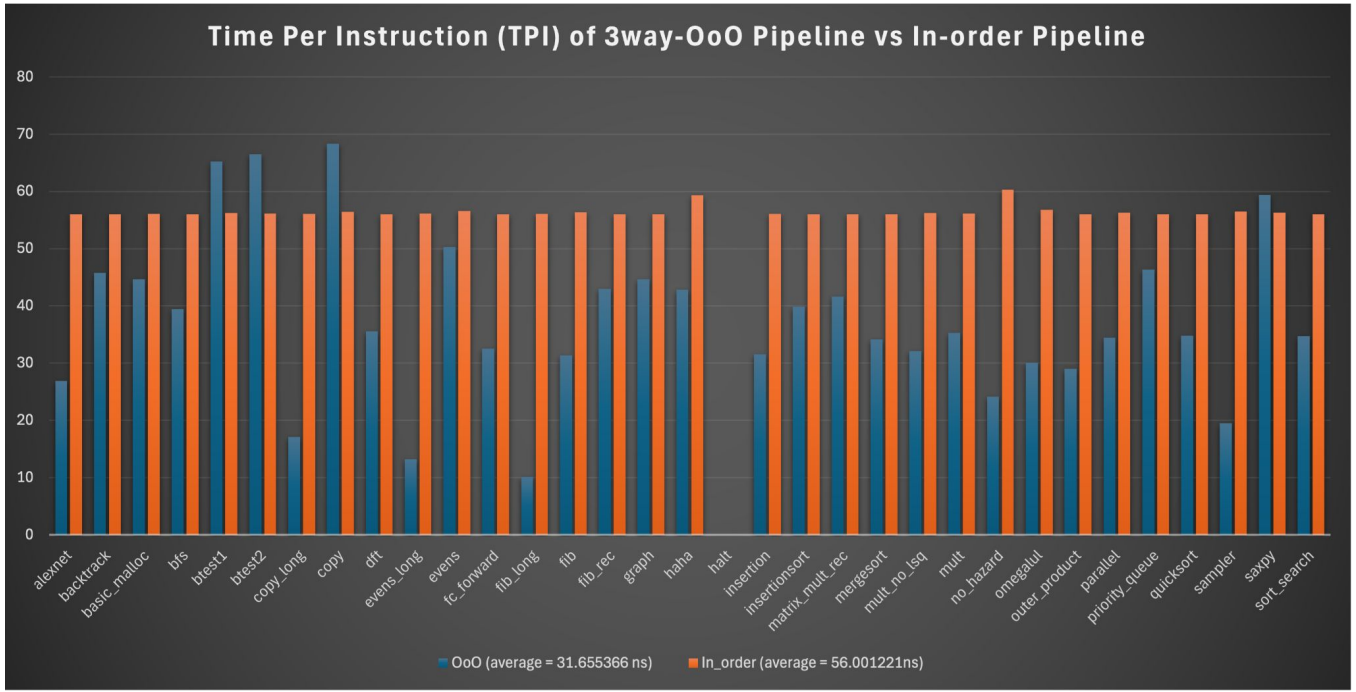
Summary – Design Specification

Design Specifications:

RS	ROB	PR	AR	Freelist	LSQ	GHR	PHT	MSHR
16 entries	32 entries	64 regs	32 regs	32 entries	8 entries	32 entries	4 entries	8 entries

FUs	Cache Assoc.	I- & D-cache	Prefetcher
4 ALUs, 2 Mults 1 Load, 1 Store	2	256B	1 stride

Summary - Benchmark Study



CPI:2.826
CLK: 11.2ns
TPI: 31.655ns

Lessons learned: what we would do next/differently?

- BP optimization: resizing predictor tables to mitigate aliasing conflicts, tuning indexing strategies, and reducing the complexity of update logic.
- Load Queue Implementation: adding a load queue to enable more efficient detection of memory dependencies and to reduce unnecessary load-related stalls.
- Prefetch optimization: developing an adaptive prefetching strategy that dynamically adjusts prefetch depth based on real-time application behaviors to reduce unnecessary memory accesses and resource overhead

Team 6: 3-way Superscalar R10K Processor

- Advanced features: 3-way superscalar execution
- Simple features: 2-way set-associative non-blocking Data cache, Non-blocking Instruction cache with prefetching, 2-Bit Bimodal Branch Predictor, Store queue
- Basic features: 4 issue queues for each type of function unit (ALU MUL LOAD BRANCH)
- Average CPI is 2.826 and clock period is 11.2ns
- Yuan Jiang, Yuxi Zhang, Junfeng Zou, Lingxi Zhang, Zhelin Su, Hongrui Huang